DESIGN OF A 12-BIT 3 GS/s CURRENT STEERING DAC

by

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DESIGN OF A 12-BIT 3 GS/s CURRENT STEERING DAC

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To the memory of my high school classmate Koray...

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ABSTRACT

DESIGN OF A 12-BIT 3 GS/s CURRENT STEERING DAC

Even if digital circuits are ubiquitous thanks to the easier design and test automation, the real world is an analog place. DACs are the circuit blocks which allow converting the signals which are easily processed in digital domain to the analog domain. Local oscillators, arbitrary waveform generators and other modern communication systems utilize high speed DACs. Current steering DACs are the prevalent architectures for high-speed applications. Spectral purity of the DAC output is the main performance consideration and degraded by dynamic and static errors. In this thesis work a 12-bit 3 GS/s current steering DAC designed in 65nm CMOS process is presented. The design of the blocks in the DAC are examined through considering dynamic and static error mechanisms. Simulation results show that the DAC has SFDR up to 60 dB with the power consumption of 922 mW for typical process conditions and 3 GHz operating clock frequency. Besides, during measurements the DAC reaches SFDR up to 65 dB and has a power consumption of 830 mW. Finally, the active area of the DAC is 1 mm^2.

ÖZET

12-BIT 3 GS/s AKIM ANAHTARLAMALI DAC TASARIMI

Sayısal devreler daha kolay tasarım ve test otomasyonları sayesinde her alanda yaygınlaşmış olmasına rağmen, gerçek dünya analog bir yerdir. DAC devreleleri, sayısal domende kolayca işlenmiş işaretlerin tekrar analog domene dönüştürülmesini sağlarlar. Yerel osilatörler, işaret üreteçleri ve diğer modern haberleşme sistemleri yüksek hızlı DAC kullanırlar. Akım anahtarlamalı DAC mimarisi, yüksek hızlı uygulamarda en sık ratlanan mimaridir. DAC için en önemli kriter, çıkış işaretinin spektral performansıdır ve statik ve dinamik hatalar çıkış spektral performansını düşmesine sebep olmaktadırlar. Bu tez çalışmasında 65nm CMOS proseste tasarlanmış 12-bit çözünürlükte 3 GS/s çalışma frekansında DAC sunulmaktadır. DAC bloklarının tasarımı, statik ve dinamik hata mekanizmaları göz önünde bulundurularak gerçekleştirilmiştir. Benzetim sonuçlarında 3 GHz çalışma frekansı ve tipik proses koşulu için 60 dB'ye varan SFDR elde edilmiş ve DAC güç tüketimi 922 mW olarak gözlemlenmiştir. Yapılan ölçümlerde ise DAC'ın 65 dB'ye kadar varan SFDR ve 830 mW güç tüketiminin olduğu görülmüştür. Son olarak, DAC'a ait toplam aktif alan 1 mm^2 dir.

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LIST OF SYMBOLS

A_0	Reference value of a DAC
A_{os}	Offset value of a DAC
BW	Resolution bandwidth
c_m	Each bit of the thermometer coded input
f_{clk}	Clock frequency
f_{IN}	Input frequency in coherent sampling
f_{SAMPLE}	Sampling frequency in coherent sampling
F_S	Sampling frequency
g_m	Transconductance
I_{TAIL}	Tail current of a differential pair
N_{DNL}	Noises arises from DNL error
N_j	Noise arises from random jitter
N_q	Noise arises from quantization error
N_{RECORD}	Number of samples in coherent sampling
$N_{Thermal}$	Noise arises from thermal noise
N_{WINDOW}	Number of input cycles which fit into the sampling window
R_L	Load resistor
r_{out}	Output resistance
V_{outn}	Negative output voltage
V_{outp}	Positive output voltage
V_{REF}	Reference voltage
V_{IDIF}	Differential input voltage
V_{ICM}	Input common mode voltage
Δ	Voltage corresponding to one LSB
$\Delta_r(k)$	Difference between two adjacent analog outputs of the DAC

LIST OF ABBREVIATIONS

ABE	Analog Back End
ADC	Analog to Digital Converter
AFE	Analog Front End
CDLV	Code-dependent Output Loading Variations
CDST	Code-dependent Switching Transients
CML	Current Mode Logic
DAC	Digital to Analog Converter
DDFS	Direct Digital Frequency Synthesizer
DDR	Dual Data Rate
DEM	Dynamic Element Matching
DNL	Differential Nonlinearity Error
DQS	Differential Quad Switching
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
IMD	Intermodulation Distortion
INL	Integral Nonlinearity Error
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
RRBS	Random Rotation-Based Binary-Weighted Selection
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
VLSI	Very Large Scale Integration
ZOH	Zero Order Hold

1. INTRODUCTION

1.1. Motivation

Easier design and test automation is achieved by digital circuits owing to better noise, supply voltage, and process variation immunity performances with respect to their analog equivalents [9]. Besides, speed, functionality per chip, and power dissipation performances improve along with scaling of the very large scale integration (VLSI) process and that makes digital circuits omnipresent [9]. Nonetheless, since only analog signals exist in the real world, conversion between the analog and digital domains is required [1]. This conversion between two domains is achieved through analog-to-digital converter (ADC) and digital-to-analog converter (DAC) blocks as depicted in Figure 1.1.

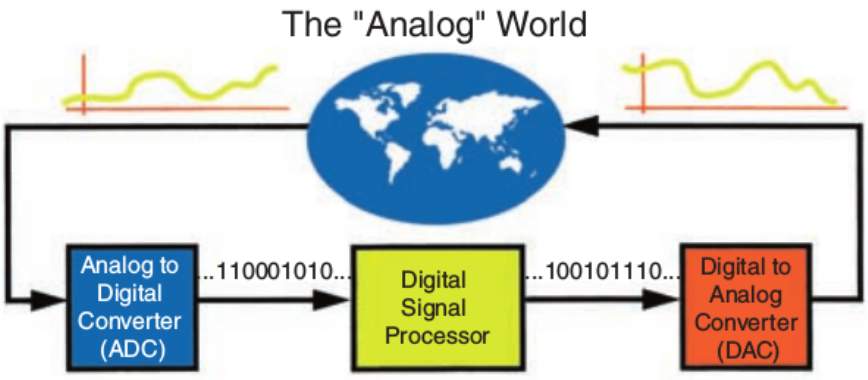

Figure 1.1. Information conversion cycle between the analog and digital domains [1].

Most modern communication systems, for instance local oscillators, arbitrary waveform generators, wired and wireless transmitters demand DACs [18]. Very high speed and bandwidth requirements become a necessity along with the trend of substituting a large part of analog functions such as analog front-end (AFE) and analog back-end (ABE) by their digital signal processing counterparts [19].

In wideband applications such as signal generation and multi-carrier communication systems, current-steering DACs are the most common architectures [20]. The

ability of driving a resistive load without the requirement for a voltage buffer is the reason that makes current source switching architecture to be the preferable one for high speed and high resolution applications [21]. On the other hand, current steering DAC output suffers from the distortion arising from static and dynamic error mechanisms [22].

Since the spurs at the DAC output spectrum affect the information content of the DAC output signal, the key performance issue is spectral purity which is defined as spurious free dynamic range (SFDR) [21]. Static and dynamic errors give rise to a drop in SFDR at the DAC output spectrum. Thus, this thesis attempts to design a high speed 12-bit current steering DAC with proper spectral performance for modern communication applications.

1.2. Background

Matching of current sources along with their output resistances are the dominant factors that decide static linearity of a current steering DAC [23]. When the signal frequency gets higher, nonlinear switching transients become a larger part of the clock cycle; hence, dynamic errors increase with signal frequency [21]. At high frequencies, output parasitic capacitance of the current sources [19], [20], [22], clock feed-through [22], major carry glitch [21], and coupling of control signals to the output [24] are the dominant considerations that can give rise to dynamic errors. Code-dependent switching transients (CDST) and code-dependent output-loading variation (CDLV) also have important role in dynamic errors [23].

Conventional binary DACs are very simple as there is no need for decoding circuits, but glitch energy especially during mid-code transition deteriorates the performance [3]. Thermometer coding reduces major carry glitch, since only unit-current cells are switched instead of larger order weighted ones. However, thermometer decoding increases digital complexity which reduces the maximum operating speed of the DAC [25].

In [2], threshold voltage-compensated current source is offered to diminish current source variations leading to linearity error. Figure 1.2 illustrates the switched current source with threshold-voltage compensation. The difference of the threshold voltages of M_2 and M_c takes place in the square law current equation. Thus, effect of the threshold voltage variation on the output current is reduced. However, it requires two extra reference voltages of V_{R1} and V_{R2}.

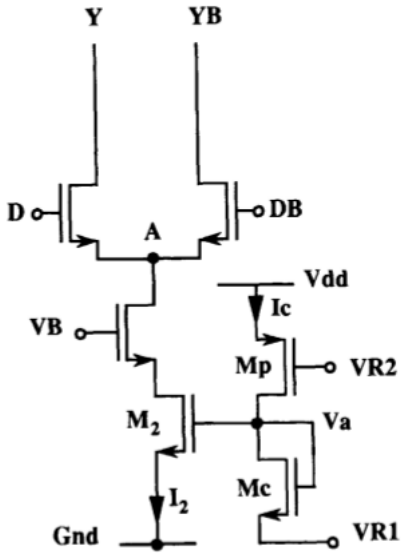

Figure 1.2. Switched current source with threshold-voltage compensation [2].

[3] and [20] apply random-rotation based binary weighted selection (RRBS) based dynamic element matching (DEM) method to mitigate current source mismatch effect. The working principle of the RRBS along with the conventional binary-selection is depicted in Figure 1.3. In the case of RRBS, the current source groups are selected randomly by rotating the control bits right with random number (R#) of steps while conventional binary-weighted selection fixes the controlled current groups. Even if RRBS reduces the mismatch effect of the current sources, it requires pseudo random number generator and rotator that give rise to design complexity.

A calibration method to enhance static linearity via tuning the currents is proposed in [4] as depicted in Figure 1.4. Calibration current allows proper calibration via generating linear voltage steps on the resistor R_C. The work proposed in [26] also exploits full analog background calibration to diminish static and low varying er-

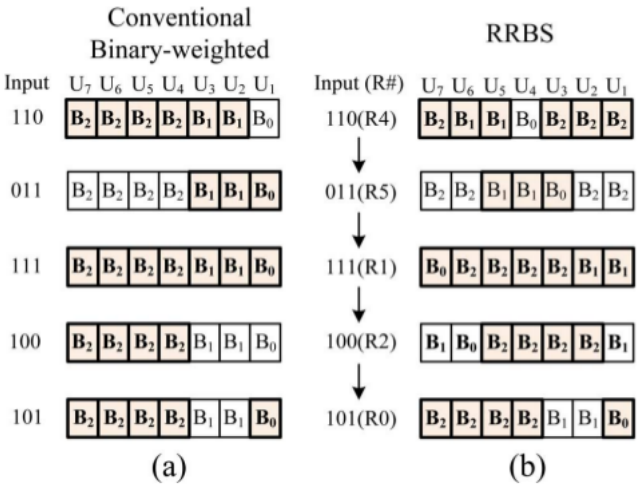

Figure 1.3. Operating principle of the (a) conventional binary-weighted method and (b) random rotation-based binary-weighted selection(RRBS) method where R# represents the number of right-rotation steps [3].

rors. Nevertheless, calibration increases design complexity and area, as well. Besides, matching of the current sources becomes non-dominant on the performance at higher frequencies thus DEM or calibration techniques are not beneficial at these frequencies [19].

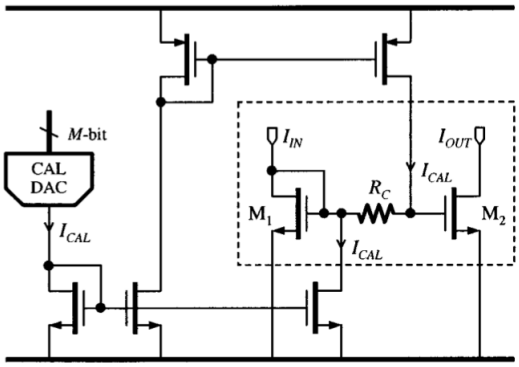

Figure 1.4. Simple trimmable current mirror(dash line) and calibration current circuitry [4].

Switching event becomes input code dependent when toggling of the switches does not occur at every edge of the clock cycle which causes noise in the signal band. However, this noise will take place at the conversion clock frequency instead of the signal band when the switch is toggled at each clock edge [5]. The work proposed

in [5] exploits differential quad-switching (DQS) to satisfy code-independent switching activity. Figure 1.5 depicts the circuit and example waveforms belonging to DQS. [27] also achieves code-independent switching activity via quad-switch architecture in which direction of the output current is reverted on the second half of the clock cycle. However quad switching demands four switching transistors instead of two along with the digital circuitry to drive these circuits at each clock edge.

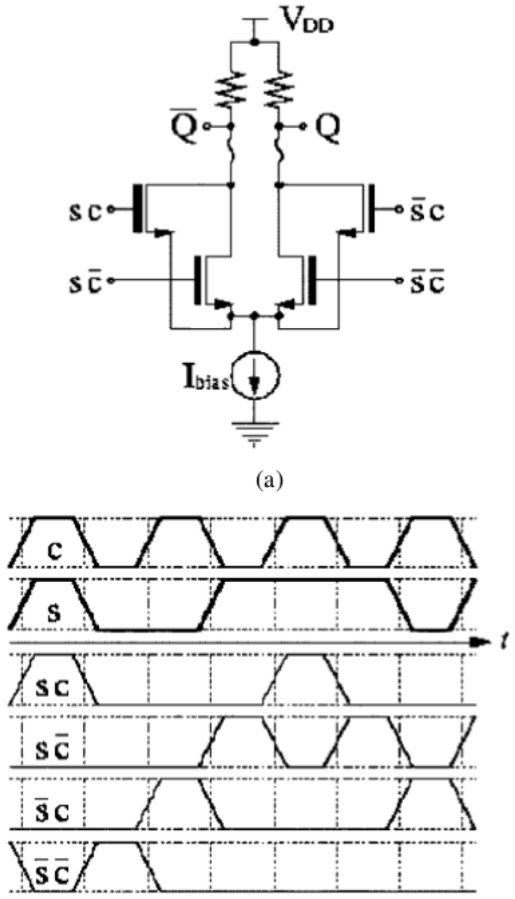

Figure 1.5. (a) Simplified circuit based on DQS (b) example waveforms of DQS [5].

In this work, size and layout of the current source transistors are decided properly to improve static linearity. Besides, segmented structure, code-independent switching architecture and additional cascode-transistor pair at the DAC output which will be mentioned in section 1.3, are employed to enhance the spectral performance.

1.3. Objectives of the Thesis and Organization

The aim of this thesis is to design a 12-bit 3 GS/s current-steering DAC through managing static and dynamic errors to achieve proper spectral performance for modern communication applications. The DAC is implemented in 65nm 1P9M CMOS process.

Segmented structure is applied such that most significant four bits are implemented as thermometer coded whereas the remaining least significant eight bits are implemented as binary weighted. Thus, major carry glitches are reduced at the cost of sacrificed digital design complexity. Furthermore, all digital sections are implemented in current-mode logic (CML) to exploit the benefits of lower power consumption at high speeds, high common-mode noise rejection, low substrate-cross talk and low supply [28].

Cascode current sources are applied to get a higher output impedance at low frequencies. Current source transistors are sized properly and laid out in a matrix form to reduce current source mismatch. Furthermore, a cascode-transistor pair with a DC current is added to both positive and negative current output nodes. These cascode transistors will always draw DC current to enhance the output impedance of current sources at both low and high frequencies as proposed in [19]. Since the dc current of the output cascode transistors sustains their gate-source capacitances which remain unchanged during switching, they do not bring about distortion [19]. Furthermore, $g_m \cdot r_{out}$ gain of these cascode transistors helps to attenuate the parasitic effects of the switch transistors [19]. This cascode transistor pair also reduces the clock feed-through and coupling of control signals to the output by the amount of cascode intrinsic gain.

Conventional differential pairs are utilized as switches. Toggling of these switches at both rising and falling clock edges is achieved via time-interleaving the digital input data with its inversion on a clock cycle. This current direction reversing process on the second half of the clock cycle increases the power of the image in second and third Nyquist band while weakening the signal at the first Nyquist band [27]. Hence, this code-independent switching makes it possible to get output at higher frequencies with

no requirement of increasing DAC operating frequency. Active area of the DAC is 1 mm^2 and it has power consumption of 922 mW.

The organization of this thesis as follows: Chapter 2 describes basic digital to analog conversion concept. This chapter also contains the performance specifications and basic architectures of DAC. Chapter 3 explains the design and implementation of the related work. The simulation set-up and results are given in Chapter 4. Chapter 5 demonstrates the measurement set-up and results. Finally, Chapter 6 concludes the thesis.

2. DIGITAL TO ANALOG CONVERSION

2.1. Basic DAC

The block diagram of a basic DAC is given in Figure 2.1.

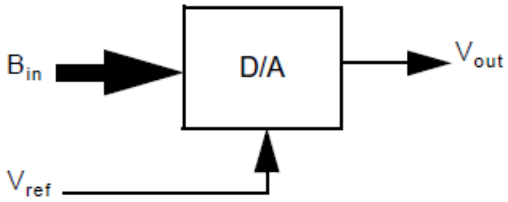

Figure 2.1. Basic DAC block diagram [6].

B_{in} represents the digital input in binary form consisting of N-bits. The relationship between bits and B_{in} is as shown in equation 2.1.

$$B_{in} = b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \cdots + b_N \cdot 2^{-N} \tag{2.1}$$

Here, the most significant bit is b_1 whereas the least significant one is b_N. Output voltage corresponding to the any digital input B_{in} is generated by using equation 2.2.

$$V_{out} = B_{in} \cdot V_{ref} \tag{2.2}$$

V_{ref} is the reference voltage that determines the output voltage range. As seen in input-output characteristic of a 2-bit DAC shown in Figure 2.2, each least significant

bit (LSB) code increment or decrement results into a voltage change which is defined as V_{LSB}. Calculation of V_{LSB} is given in equation 2.3 [6].

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{2.3}$$

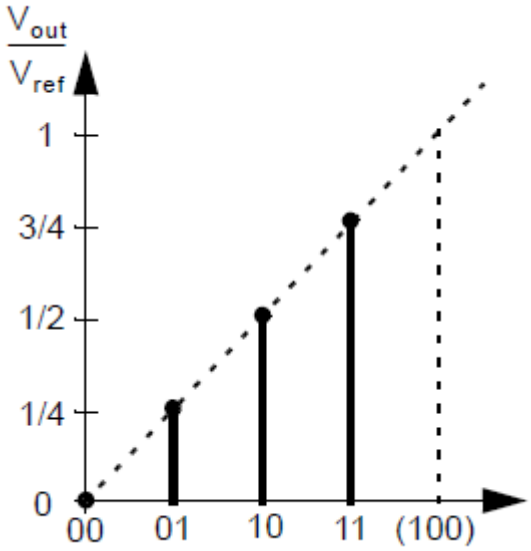

Figure 2.2. 2-Bit DAC transfer characteristic [6].

2.2. Static DAC Performance Specifications

2.2.1. Offset Error

Offset error is the difference between outputs of a real and ideal DAC which corresponds to zero digital input. Figure 2.3 shows an example of a 3-bit DAC which has one and a quarter offset error. Offset error can be eliminated via trimming as all the input codes are affected by offset error equally [7]

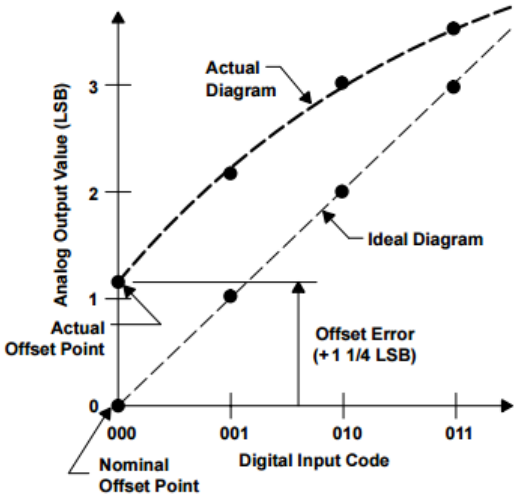

Figure 2.3. Offset error of a linear 3-bit DAC [7].

2.2.2. Gain Error

Gain error is the definition for the error on the slope of an ideal data converter which is defined as the ratio between full scale digital code and full scale analog range. Deviation of this slope from the ideal value explains the gain error [8]. Figure 2.4 illusrates gain error of a digital-to-analog converter.

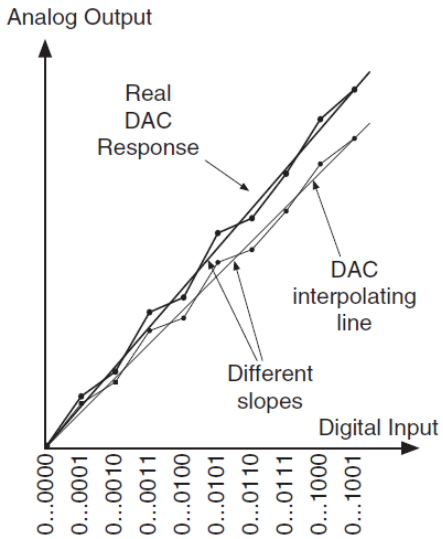

Figure 2.4. Gain error of a digital to analog converter [8].

2.2.3. Integral Non-Linearity Error

Deviation between straight line of the real and the ideal DAC describes the integral non-linearity error (INL). The straight-line is either the line that crosses both the first and final points of the DAC transfer response or the one that fits the transfer response most properly in terms of having minimum difference to the curve. Both definitions are valid for the transfer response in which offset and gain errors are removed [6]. Both end-point and best-fit INL description is illustrated in Figure 2.5.

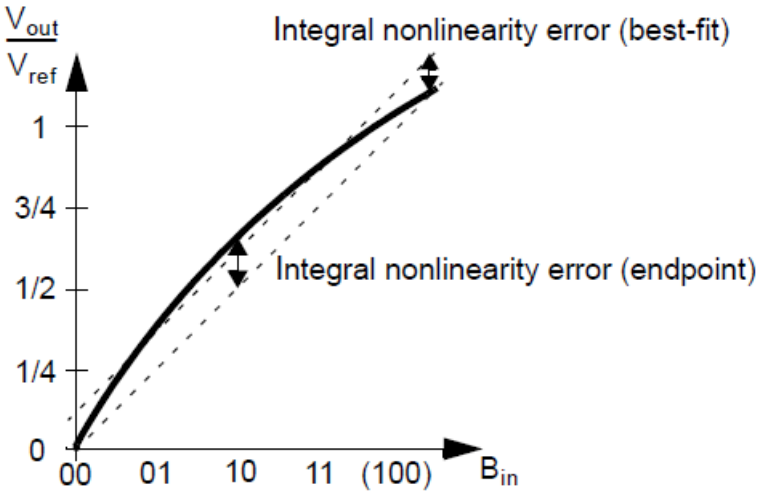

Figure 2.5. INL in a 2-bit D/A converter [6].

2.2.4. Differential Non-Linearity Error

Deviation of the difference between two analog output values corresponding to two consecutive digital inputs from 1 LSB voltage is defined as differential non-linearity (DNL) error. An n bit DAC will have 2^n digital inputs hence $2^n - 1$ DNL value is achieved by using the formula given in equation 2.4 [13].

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta} \tag{2.4}$$

Here $\Delta_r(k)$ describes the difference between two adjacent analog outputs and Δ describes one LSB voltage. An example illustrating DNL error in a 3-bit DAC is given in Figure 2.6.

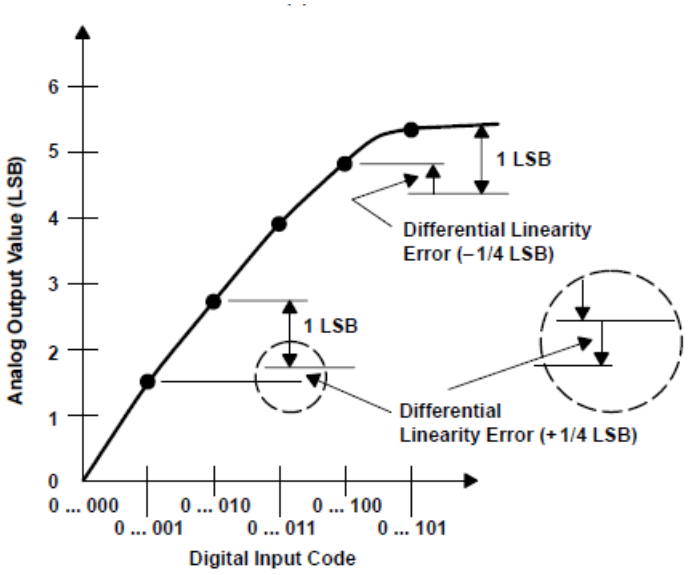

Figure 2.6. Differential nonlinearity error of a linear DAC [7].

2.2.5. Monotonicity

Monotonicity is the specification which is satisfied by a DAC if the output always keeps increasing with increasing digital input or vice versa. In other words, a monotonic DAC has a transfer curve such that it always has a transfer curve with positive slope.

2.3. Dynamic DAC Performance Specifications

2.3.1. Settling Time

When an input code transition occurs, it takes a certain time until the output settles to the output voltage corresponding to this new input. This certain time difference is defined as settling time. Settling time is one of the factors that decides the maximum operating rate of the DAC. It should be smaller than the clock period so that, output can settle to its final value before clock period

2.3.2. Glitch Impulse Area

When the input changes to a new code, the output does not settle to a new code smoothly. Some irrelevant transition behaviour arises which are called glitches during this transition. Glitch impulse area defined as the maximum of the area under those glitches which also called as glitch energy [9]. An example depicting both settling time and glitch energy is given in Figure 2.7.

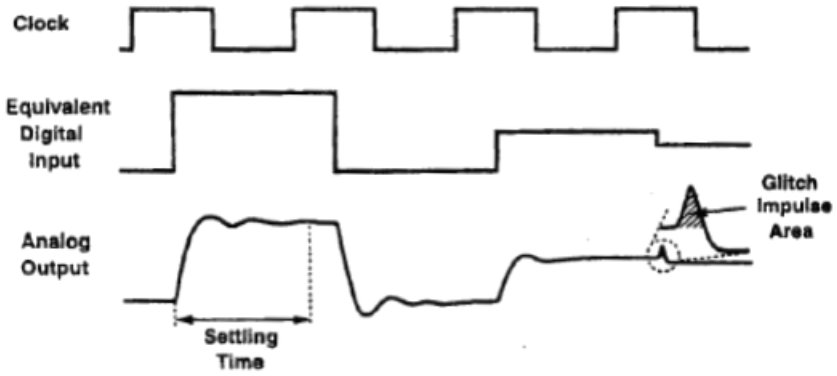

Figure 2.7. Dynamic parameters of D/A converters [9].

2.4. Frequency Domain DAC Performance Specifications

Signal-to-noise ratio (SNR), signal to noise and distortion ratio (SNDR), effective number of bits (ENOB), spurious free dynamic range (SFDR) and intermodulation distortion (IMD) are the specifications commonly used for characterizing the performance of DACs considering the DAC output spectrum. All of them are examined in the desired Nyquist frequency band which is decided by the operating frequency of the DAC [11].

2.4.1. Signal-to-Noise Ratio

Ratio of the signal power to the integrated noise power defines the signal-to-noise ratio (SNR) specification of a DAC. The noise power mostly arises from DNL error (N_{DNL}), random jitter (N_j), quantization noise (N_q) and thermal noise ($N_{Thermal}$) .

Its units are in dB and it is defined as given in equation 2.5 [11].

$$SNR = 10\log(\frac{P_{signal}}{N_q + N_{DNL} + N_{Thermal} + N_j}) \tag{2.5}$$

Maximum possible SNR value occurs when only the quantization noise is present as the noise source for the N bit converter. Under this assumption, maximum SNR is calculated as given in equation 2.6 [29].

$$SNR_{dB(max)} = 6.02_{dB} \cdot N + 1.76_{dB} \tag{2.6}$$

Figure 2.8 illustrates the theoretical SNR level for an ideal 12 bit ADC using 4096 point Fast Fourier Transform (FFT). However, FFT noise floor is not equal to this theoretical SNR level. This difference is a result of the processing gain of the FFT that is defined as the correction factor of the theoretical SNR value when only the bandwidth in which the signal of interest takes place is selected by filtering. Since quantization noise components outside this bandwidth will be filtered out, SNR value will be increased as much as processing gain. Processing gain is calculated by using equation 2.7 [10].

$$Processing\,gain = 10\log(\frac{F_S}{2 \cdot BW}) \tag{2.7}$$

FFT behaviour resembles an analog spectrum analyzer with a resolution bandwidth which is equal to the sampling frequency (F_S) over a number of FFT points

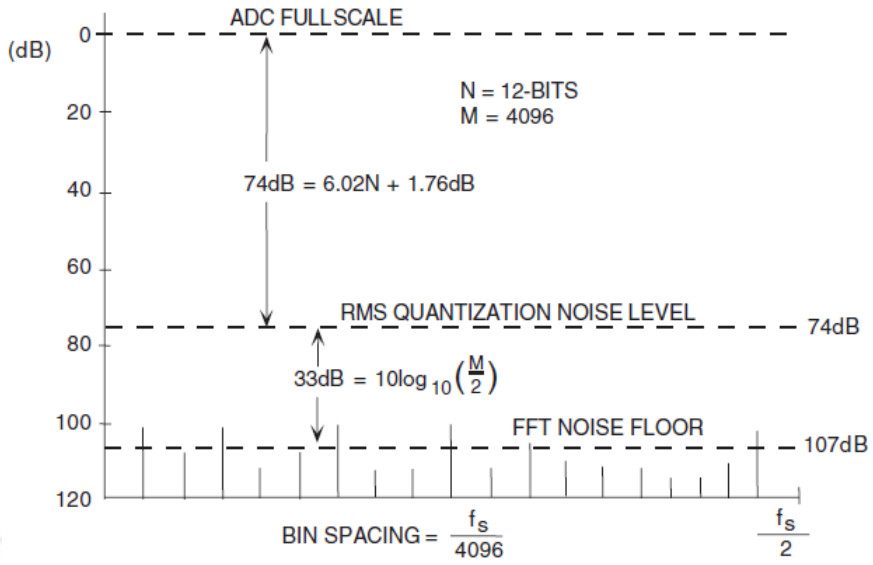

Figure 2.8. Noise floor for an ideal 12-bit ADC using 4096 point FFT [10].

(N) [10]. Hence, the processing gain of an N-point FFT equals to $10\log(\frac{N}{2})$ which is the amount of the difference between quantization and FFT noise floors.

2.4.2. Signal-to-Noise and Distortion Ratio

Signal-to-Noise and Distortion Ratio (SNDR) is the ratio of root-mean square of the output signal to the root-sum-square of the harmonic components (except DC) and noise. Thus, SNDR is almost the same as SNR excluding nonlinear terms arising from the input signal [8].

Figure 2.9 depicts the relationship between signal amplitude and SNDR. In the case that the signal amplitude is too small such that it is negligible with respect to the noise, SNDR becomes noise limited and converges to SNR. Until a certain level SNDR increases with increasing signal amplitude under the constant noise assumption. Then it has a maximum and starts to drop as harmonics become superior to noise and their power goes up faster than the fundamental [6].

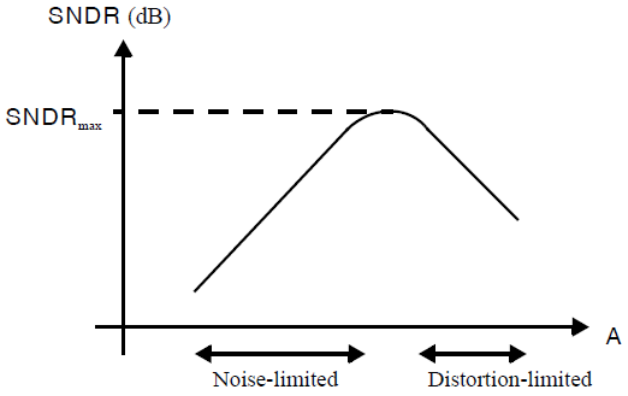

Figure 2.9. Variation of SNDR with signal amplitude in an analog circuit [6].

2.4.3. Spurious Free Dynamic Range

The measurement of the desired output power with respect to the largest spur in the desired bandwidth defines the spurious free dynamic range (SFDR) [11]. The spectrum given in Figure 2.10 demonstrates SFDR of a 12-bit DAC.

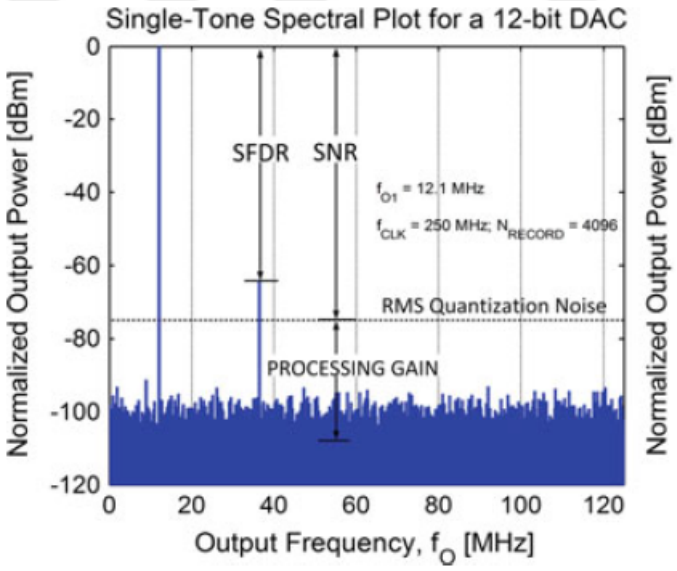

Figure 2.10. Spectral plot of a 12-bit DAC [11].

2.4.4. Effective Number of Bits

Effective number of bits (ENOB) is the metric utilized to compare the dynamic ranges of the digital-to-analog or analog-to-digital converters having the same amount of bit resolution [13]. ENOB is defined by using the measured signal to noise and distortion ratio as provided in equation 2.8.

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \tag{2.8}$$

2.4.5. Intermodulation Distortion

Intermodulation distortion (IMD) is the measurement of the ratio between the desired output signal power and the nth-order intermodulation product. These intermodulation products are the tones which are created due to inter-tone harmonic mixing in the case that two or more signals are applied at the input of the DAC [11]. Figure 2.11 illustrates second and third-order intermodulation products for $f_1 = 5$ MHz and $f_2 = 6$ MHz.

2.5. Basic DAC Architectures

2.5.1. Decoder Based DAC

In a decoder based DAC architecture, 2^N reference signals are generated for N bit input. The desired reference signal level is decided by the binary input of the DAC and passed to the output [6]. A resistive divider which is an example of decoder based DAC is provided in section 2.5.5.

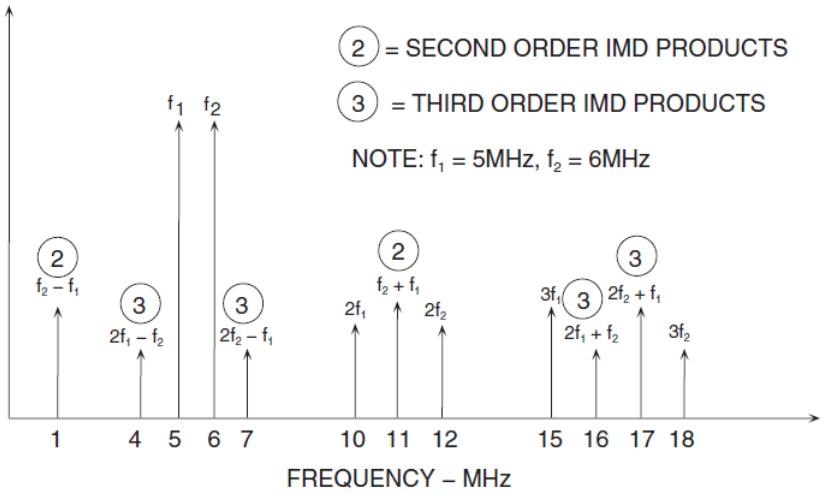

Figure 2.11. Second and third-order IMD products for $f_1 = 5$ MHz and $f_2 = 6$ MHz [10].

2.5.2. Binary Weighted DAC

Binary weighted elements such as resistors, capacitors or current sources are employed in a binary weighted DAC [30]. Each bit of the digital input controls these binary weighted elements. A binary weighted DAC with an offset A_{os} is provided in Figure 2.12. Here, $b_i(nT)$ are the input bits at the time nT where T represents the DAC update period. The output signal is provided in equation 2.9 in which A_0 and A_{os} are reference and offset values respectively [12].

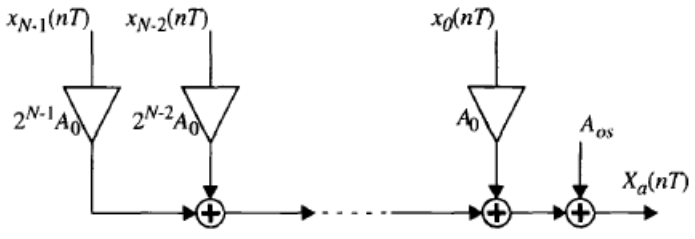

Figure 2.12. Binary weighted DAC with an offset of A_{os} [12].

$$X_a(nT) = A_{os} + A_0[b_0(nT) + 2 \cdot b_1(nT) + \cdots + 2^{N-1} \cdot b_{N-1}(nT)] \tag{2.9}$$

Implementing two adjacent bits by components which are very different from each other may give rise to monotonicity errors. Besides, switching larger significant bits in a binary weighted structure causes larger DNL errors. The largest DNL error occurs when the most significant bit is switched during mid-code change [6].

2.5.3. Unary Weighted DAC

Unary weighted, which is also known as thermometer coded, DAC switches equally weighted elements to generate output. Figure 2.13 illustrates a signal flow graph of thermometer coded DAC architecture. Here, A_0 and A_{os} are reference and offset values respectively as mentioned in section 2.5.2.

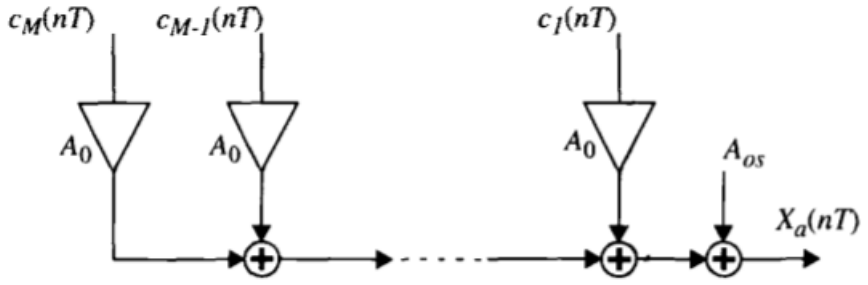

Figure 2.13. Signal flow graph of the thermometer coded DAC [12].

Output of a thermometer DAC is formulated in equation 2.10 [30]. Here, c_m represents each bit of the thermometer coded input. $2^N - 1$ bit thermometer code corresponds an N bit binary code. Thermometer code representation of a 3-bit binary code is provided in Table 2.1. As seen in this table, the number of ones is equal to the decimal value of the binary code.

$$A(nT) = A_{os} + A_{\mathrm{o}} \cdot \sum_{m=1}^{M} c_m(nT) \tag{2.10}$$

Table 2.1. Thermometer code corresponding of 3-bit binary code.

	Binary Input	Thermometer Coded Output
1	000	0000000
2	001	0000001
3	010	0000011
4	011	0000111
5	100	0001111
6	101	0011111
7	110	0111111
8	111	1111111

Matching of the elements in thermometer coded DAC is easier than the binary weighted one since they are equally-weighted. Besides, thermometer coded DAC has better INL and DNL performances along with monotonic transfer function [12].

2.5.4. Segmented DAC

Segmented DAC employs both binary and unary weighted elements together. Unary implementation provides lowering the glitch energy and DNL errors along with the cost of decoding logic complexity. Segmentation architecture makes it possible to compromise between pros and cons of unary implementation [24]. Since DNL errors and glitch energy increases with significance of the bits in a binary weighted DAC, unary weighted implementation is applied to desired number of most significant bits whereas rest of the bits are implemented via binary weighted elements.

2.5.5. DAC Architectures Based On Implementation

2.5.5.1. Resistor Divider. An n-bit resistor divider DAC consists of a resistive voltage divider including n unit resistors to generate equally segmented voltage levels. One of these voltage levels is selected as the output voltage via a decoder by using digital input. Figure 2.14 demonstrates a resistor-ladder divider. Since, the minimum voltage level of the voltage divider is non-zero, it has an offset error. An output buffer should be applied the output to isolate resistive divider from the load. Hence, selected voltage level sees high impedance instead of load. Delay of the switching network together with divider delay are the most dominant factors on operation speed [6]. Thus, increasing input resolution will degrade high speed performance. Besides, number of resistors and switches grows exponentially with input resolution.

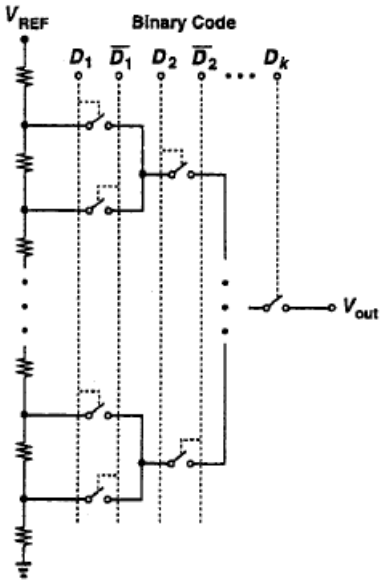

Figure 2.14. Resistor-ladder DAC with binary input [9].

2.5.5.2. R-2R Ladder DAC. $R-2R$ ladder network is a solution for the exponential growth in number of resistors in a resistor divider DAC. Instead of 2^n, $3n$ resistors are required for an n-bit $R-2R$ ladder DAC in which an $R-2R$ cell takes place for each bit along with the $2R$ termination resistor. Voltage and current mode operation can be achieved via $R-2R$ ladder DAC [8].

Figure 2.15 depicts both current and voltage mode operations.Each node divides the voltage or the current at the input by two since the resistance to the left and right of that node always equals to $2R$. Calculation of the output voltage and current for voltage and current modes are provided in equations 2.11 and 2.12 [8]. A buffer should be applied at the output to isolate output load from the network as mention in resistive divider section whereas output current can be converted to voltage by using a current to voltage converter.

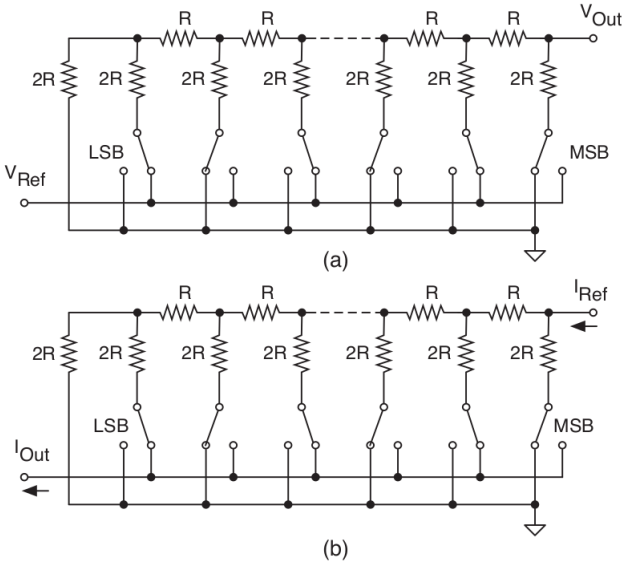

Figure 2.15. Voltage mode and current mode R-2R ladder networks [8].

$$V_{out} = \frac{V_{Ref}}{2} \cdot b_{n-1} + \frac{V_{Ref}}{4} \cdot b_{n-2} + \cdots + \frac{V_{Ref}}{2^{n-1}} \cdot b_1 + \frac{V_{Ref}}{2^n} \cdot b_0 \tag{2.11}$$

$$I_{out} = \frac{I_{Ref}}{2} \cdot b_{n-1} + \frac{I_{Ref}}{4} \cdot b_{n-2} + \cdots + \frac{I_{Ref}}{2^{n-1}} \cdot b_1 + \frac{I_{Ref}}{2^n} \cdot b_0 \tag{2.12}$$

2.5.5.3. Charge Redistribution DAC. Figure 2.16 illustrates a binary weighted capacitor DAC. It consists of capacitors that share output node. On the other hand, their other terminals are switched to either V_{ref} or ground. S_{reset} switch is closed and all zero digital input is applied at the beginning of each conversion thus all the capacitors are discharged [13].

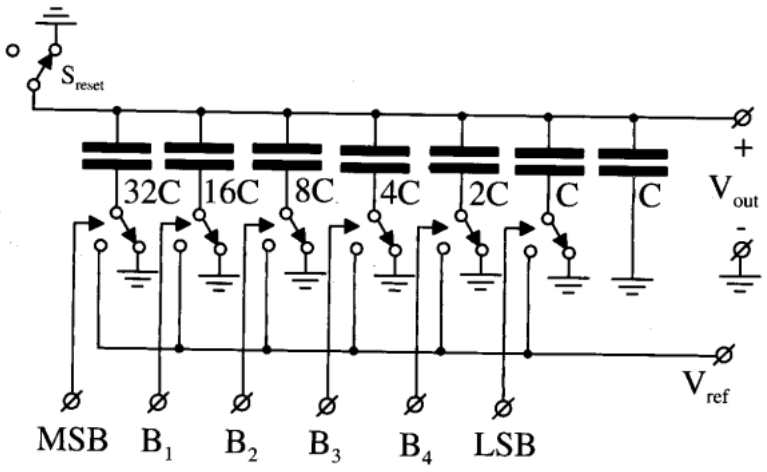

Figure 2.16. Binary weighted capacitor D/A converter [13].

For a digital input such that only i_{th} bit B_i is high and rest of the bits are low is applied during conversion, the circuit performs a capacitive divider network as seen in Figure 2.17. The output voltage for this digital input is given in equation 2.13.

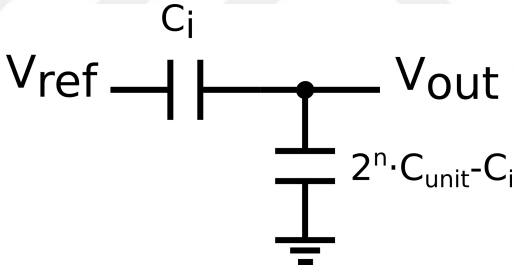

Figure 2.17. Capacitive divider network when only one bit B_i is high.

$$V_{out} = V_{ref} \cdot \frac{C_i}{2^n \cdot C_{unit}} \tag{2.13}$$

In a binary-weighted configuration C_i is weighted according to the significance of the corresponding bit as given in equation 2.14. Hence, the output voltage corresponding to any combination of digital input can be calculated via superposition principle as formulated in equation 2.15.

$$C_i = 2^i \cdot C_{unit} \tag{2.14}$$

$$V_{out} = \frac{V_{ref}}{2^n}(B_0 \cdot C_{unit} + B_1 \cdot 2C_{unit} + \cdots + B_{n-1} \cdot 2^{n-1}C_{unit}) \tag{2.15}$$

2.5.5.4. Current Steering DAC. Current steering DACs exploit current source elements to generate analog outputs. Figure 2.18 illustrates 3-bit unary and binary weighted current sources performing a current steering architecture. Digital inputs switch currents generated by the current sources either to output or to ground. Thus, total current at the output is decided by the digital input. Switching the currents between two outputs instead of switching on or off makes it more suitable for high speed applications due to the lower glitch and disturbance [10].

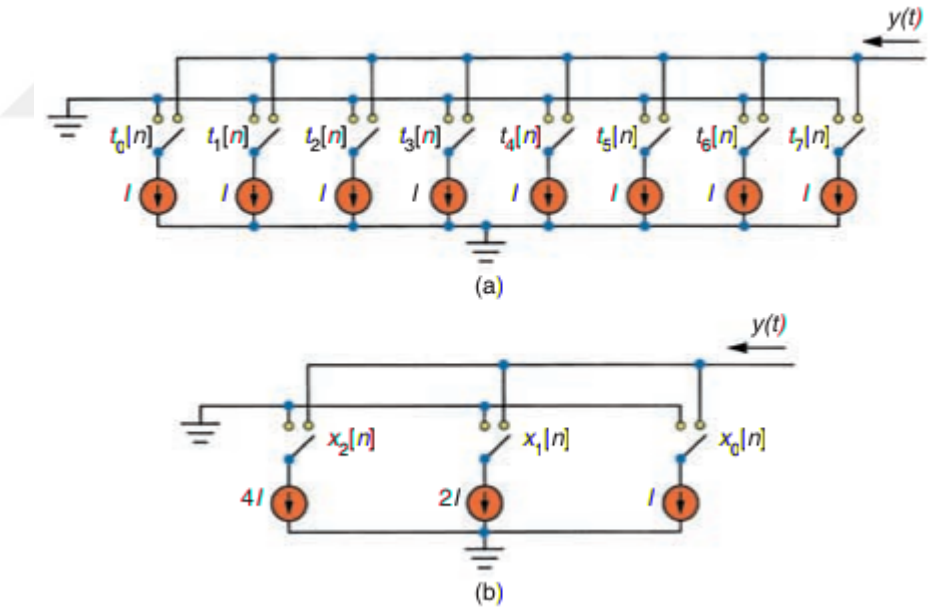

Figure 2.18. 3-bit DAC architecture with unary(a) and binary(b) weighted current sources [1].

3. DESIGN OF THE 3 GS/s CURRENT STEERING DAC

The block diagram of the DAC is depicted in Figure 3.1. The digital code input of the DAC is received through A, B, C, and D channels with a data rate of one-fourth of the clock frequency. These channels are serialized via the input multiplexer so that data with a data rate of the clock frequency is achieved.

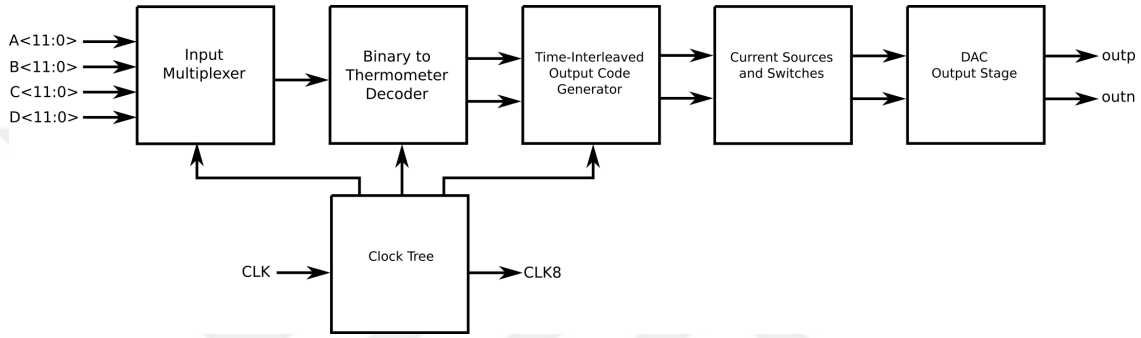

Figure 3.1. DAC top level block diagram.

Serialized input data is processed through binary to thermometer decoder and time-interleaved output code generator blocks and the generated output codes drive current switches. DAC output stage generates the DAC output. The clock tree generates the required clock signals to the digital sections. Besides, it generates CLK8 output signal which is used to synchronize the digital inputs.

3.1. Bias Generation

3.1.1. Voltage Reference Generator

The traditional band-gap reference circuit produces voltage about 1.25V which is approximately equal to the band-gap voltage of silicon [31]. On the other hand, since the supply voltage used in biasing is 1.2V, the traditional band-gap circuit is not applicable for a voltage reference. [32] and [31] propose voltage reference circuits for low voltage operation. Nevertheless, start-up circuit in a band-gap circuit may risk the whole chip, if it does not operate properly at the start up. On the other hand,

the required reference voltage in this application does not have a strict specification on voltage, process and temperature variation dependency like band-gap references. Thus, the reference voltage is generated from the supply voltage by applying a simple resistive divider circuit which is depicted in Figure 3.2. Capacitor C is employed to eliminate high-frequency disturbances to the reference voltage.

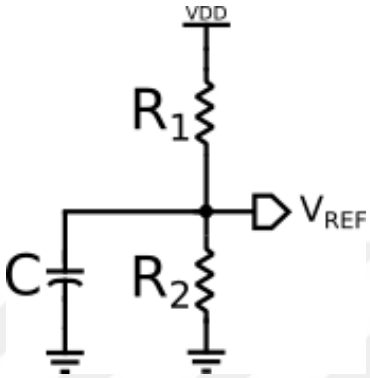

Figure 3.2. Reference voltage generator.

3.1.2. Current Reference Generator

Current references generate conversion current which is steered by the switches and current required for current-mode logic via employing the voltage generated by the voltage reference.

Figure 3.3 illustrates the current reference generator for DAC conversion and CML current. Negative feedback through the op-amp and common-source stage allows R_1 to have a voltage drop which is equal to V_{REF}. Then, the current drawn by R_1 is mirrored and $bias_{CML}$ and $bias_{DAC}$ current mirror gate voltages are generated. Here, the type of resistor R_1 is same as the load resistors of the DAC and current-mode logic. Thus, CML and DAC output swing will not be affected by process, temperature and voltage variations. In both circuits V_{REF} is applied to the inverting input of the op-amps through a series resistor which constructs another filter with the input capacitance of the op-amp which allows further attenuation of the high frequency disturbances at V_{REF}.

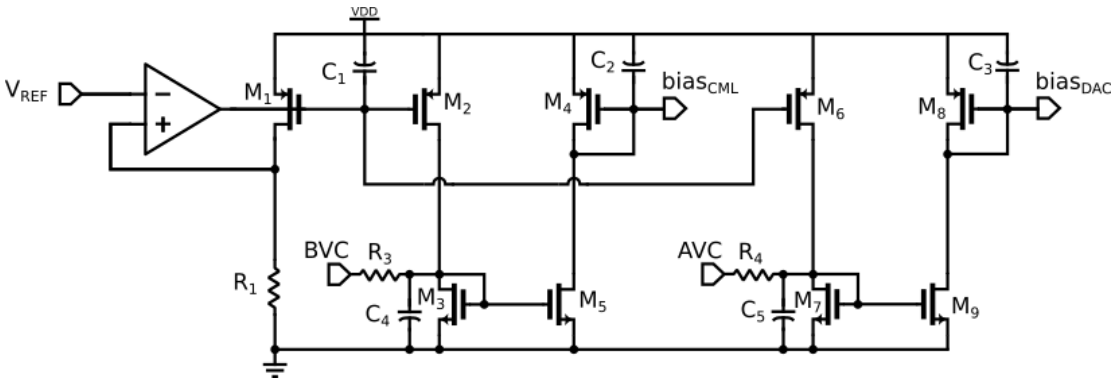

Figure 3.3. DAC conversion and current-mode logic current reference generator.

CML cells employed in the clock tree have higher tail currents. Load resistances of these CML circuits have to be smaller with increasing tail currents to maintain constant output swing. Lower load resistance requires smaller length of the resistance or larger width. However, unless the sheet resistance is low enough, width of the resistance needs to be unnecessarily large to achieve lower resistance value. Thus, another type of resistor with lower sheet resistance is employed in CML cells in the clock tree. Since, a different type of resistance is utilized and constant CML swing is desired, another current reference circuit is employed to generate current reference. Figure 3.4 depicts current reference circuit for biasing CML cells in the clock tree. It is the same as the current reference for DAC conversion and other CML cells except the type of the resistance.

A low voltage active-loaded differential amplifier is applied as the op-amp in both current references. Cascading the op-amp with a common-source stage results in a two stage negative feedback loop in which stability is a crucial consideration. The op-amp, common-source stage, and compensation capacitance C_1 have to provide feedback loops in both circuits to have at least 60° phase margain. Simulation results show that in all process, temperature and voltage variation corners, circuits have more than 85° phase-margin.

Current-mirror reference voltage of $bias_{DAC}$ provides biasing voltage of the current sources for DAC conversion current, whereas $bias_{CML}$ is the bias voltage for the

CML blocks except the ones in the clock tree. Two different bias voltages are generated for the CML blocks in the clock tree. The reason for two different bias voltages is that some part of the clock tree has to be kept in operation, whereas the rest of the clock tree has to be turned off when the DAC is disabled. In the disable mode, $bias_{CLK-CML}$ output is pulled-up to VDD while $bias_{CLK-CML-1}$ is not. The input AVC and BVC are added to set DAC conversion and CML currents manually when it is necessary. These inputs are also applied through a RC network to mitigate high frequency disturbances.

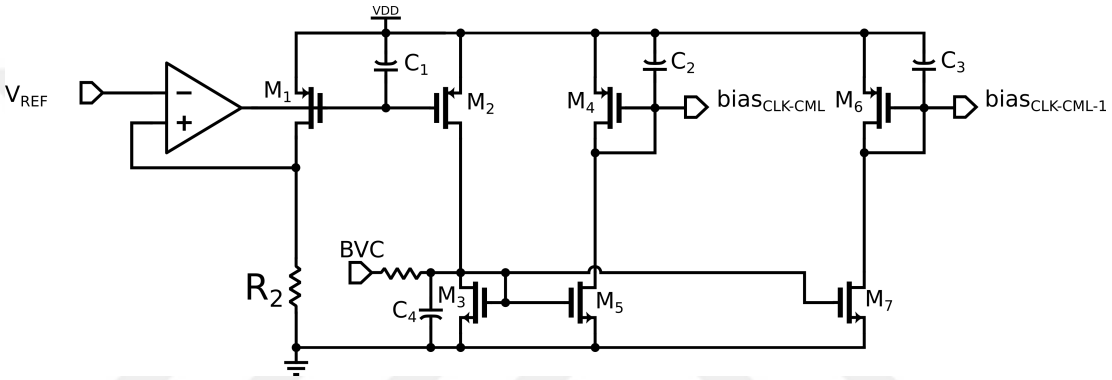

Figure 3.4. Current reference generator for the CML in clock tree.

3.1.3. Bias Circuit

Schematic of the bias circuit is seen in Figure 3.5. Bias circuit has a $DISn$ input which pulls-up $bias_{DAC}$, $bias_{CML}$ and $bias_{CLK-CML}$ bias reference voltages to VDD when DAC is disabled. As mentioned in section 3.1.2, $bias_{CLK-CML-1}$ is allowed to generate bias for the part of clock tree which is needed to continue operating when the DAC is disabled.

Cascode current sources are employed as DAC conversion current. There are three different types of switch and cascode blocks named as Swi_wCas, Swi_wCas_2 and Swi_wCas_3. Bias circuit applies replicas of these switches and cascode blocks so that cascode and diode transistor bias voltages are generated in the same condition with the switches and current sources during the operation. For instance, I_{LSB}, which is the corresponding amount of the current of Swi_wCas_3, is generated via $bias_{DAC}$ biasing

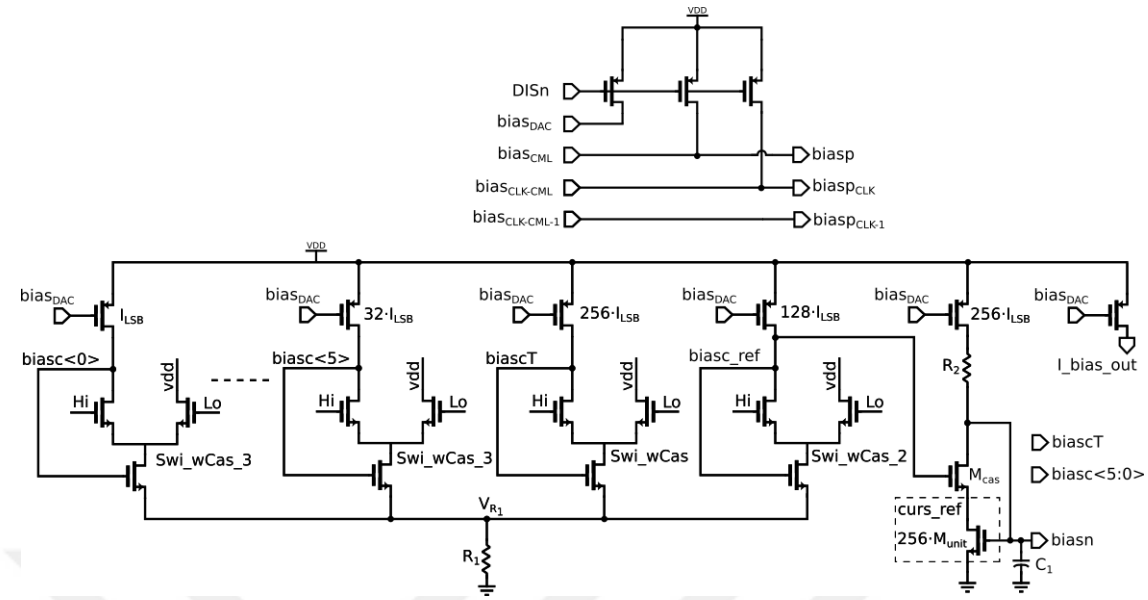

Figure 3.5. Bias circuit.

voltage to achieve cascode bias voltage. This current is drawn from one side of the switches in Swi_wCas_3 by applying logical high and low to the switches. Thus, cascode transistor biasing voltage is achieved as given in equation 3.1. When $biasc < 0 >$ is applied to the gate of the cascode transistor in Swi_wCas_3, drain-source voltage of the current mirror transistor of the cascode current source will be equal to V_{R1}. Rest of the cascode gate biasing voltages $biasc < 1 : 5 >$ and $biascT$ are generated as the same way with $biasc < 0 >$.

$$V_{biasc<0>} = V_{R_1} + V_{GS_{swi<0>}} \tag{3.1}$$

Type of R_1 is selected the same as the one applied in current reference which generates $bias_{DAC}$ biasing voltage. Thus, the effects of process, temperature and voltage variations on V_{R1} are minimized. As V_{R1} determines the drain-source voltage of the current mirror transistors in cascode current sources of DAC conversion current, R_1 value is decided such that V_{R1} is above the drain-source saturation voltage by a certain

margin. Hence, current-mirror transistors will always operate in the saturation region.

To achieve biasing voltage of the current mirror transistors, $256 \cdot I_{LSB}$ current is drawn to the $curs_ref$ transistor which has 256 times the total width of the unit current mirror transistor. On the other hand, M_{cas} has a gate voltage of $biasc_ref$. Since $biasc_ref$ voltage is generated in the same way with other cascode biasing voltages and M_{cas} has the same current density with a unit cascode transistor, $curs_ref$ transistor will have the same drain-source voltage with the current-mirror transistors. Hence having the same source-drain voltage with the reference current mirror transistor will eliminate the channel-length modulation effect.

Moreover, difference between source-drain voltages of the PMOS transistors which generate currents for $biasc_ref$ and $biasn$ due to the low output resistance of these transistors has also to be minimized. R_2 which has the same type as that in the $bias_DAC$ generator is employed to reduce the difference between the source-drain voltages. Consequently, I_bias_out is generated to provide continuous DC current to the output cascode transistors.

3.2. Current-Mode Logic

A CML gate draws constant current from the supply. For a certain input code, output is generated by directing this current to the one of the resistor loads according to the input code. In mixed-signal applications CML is more appropriate than CMOS since it has insignificant dI/dt effects owing to the constant current [33]. Moreover, CML circuits have much smaller voltage swing than conventional CMOS and this allows much lower dynamic power consumption at higher frequencies than static CMOS [34]. As seen in Figure 3.6, CMOS power consumption gets much higher than CML after the sample rates of 150 or 200 MS/s. Therefore, all digital sections are implemented in CML instead of static CMOS.

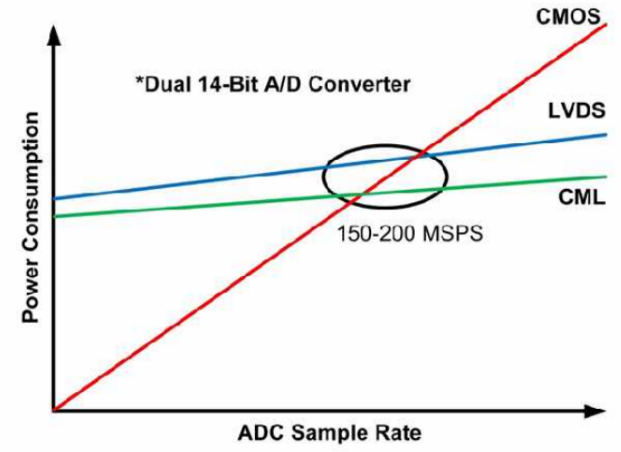

Figure 3.6. CMOS, CML and LVDS power consumption comparison [14].

3.2.1. Buffer

CML buffer is basically a resistor-loaded differential pair. Figure 3.7 depicts the schematic diagram of the buffer. In the case that input is high, all the tail current is drawn by M_1 turning off M_2. Thus, out_p and out_n voltages become as given in equations 3.2 and 3.3. CML voltage swing, difference between voltage levels of positive and negative nodes, is decided by the tail current and the load resistor. CML buffer is also capable of implementing an inverting function by swapping the positive and the negative outputs.

$$V_{outp} = VDD \tag{3.2}$$

$$V_{outn} = VDD - I_{TAIL} \cdot R_L \tag{3.3}$$

3.2.2. AND Gate

Figure 3.8 depicts a two input AND in CML. The tail current is directed to M_1 only in the case that both A and B inputs are high. Hence, output is high only for the condition that both inputs are high. During the rest of the A and B combinations, tail

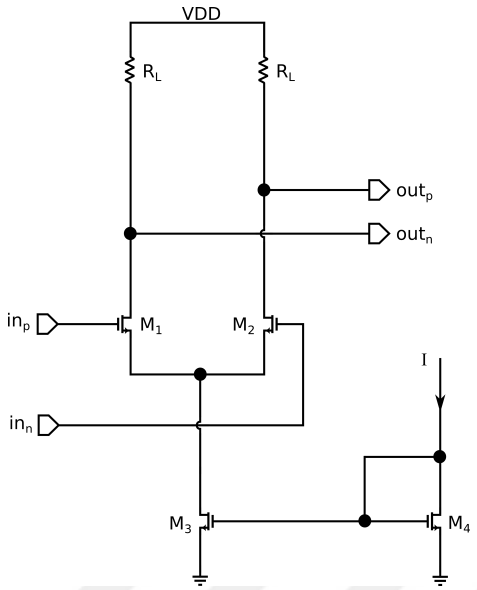

Figure 3.7. Buffer in CML.

current is always drawn by M_2 or M_4 so that low level output is generated.

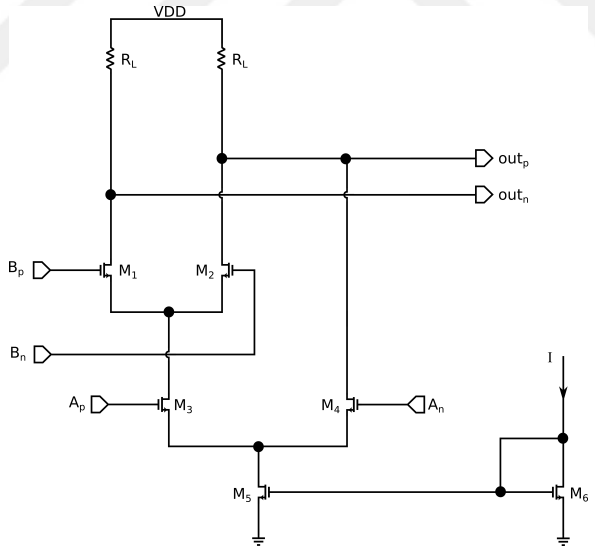

Figure 3.8. AND-gate in CML.

Here, transistors should be sized properly such that M_3 is always in the saturation region when both A and B inputs are high. Unless M_3 is in the saturation region, it will not be capable of drawing the whole tail current. Then, M_4 will draw some current which cause positive output voltage to drop.

3.2.3. OR Gate

Schematic of a two input OR in CML is given in Figure 3.9. Here, tail current is directed to M_2 only when both A and B inputs are low. Hence, output is low only for the condition that both inputs are low. In the case of other input combinations, M_1 draws the whole tail current and output is high. Moreover, transistors sizes should be decided such that M_3 is always in saturation region when both inputs are low for the same reason mentioned for AND in section 3.2.2

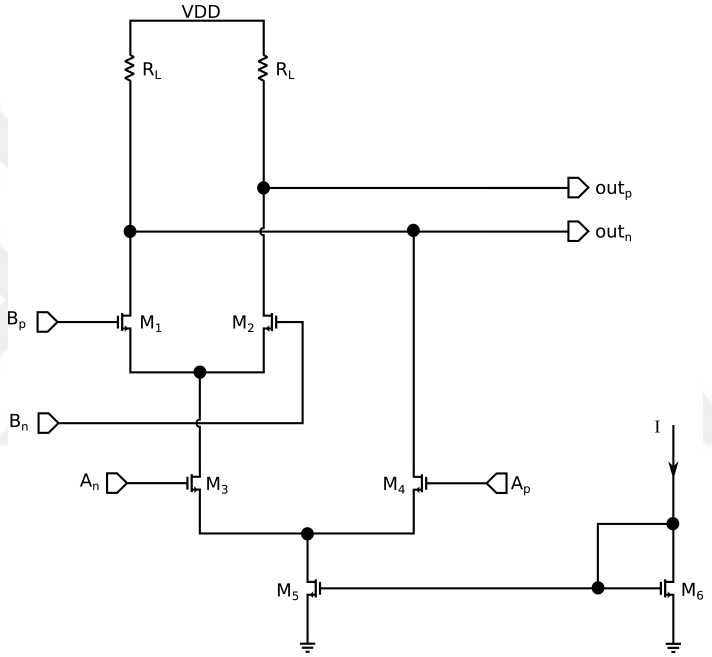

Figure 3.9. OR-gate in CML.

3.2.4. Latch

Schematic of a latch in CML is given in Figure 3.10. The latch operates such that during the track phase, when *clk* input is high, the tail current provided by M_3 is transferred to $M_1 - M_2$ by M_5. Having a tail current leads the differential pair $M_1 - M_2$ to work as a buffer, hence the input is transferred to the output. During the hold phase, when *clk* is low, since M_6 is ON, the tail current is transferred to the $M_3 - M_4$ pair which performs a positive feedback. Thus, output at the beginning of hold phase is preserved thanks to the positive feedback sustained by $M_3 - M_4$.

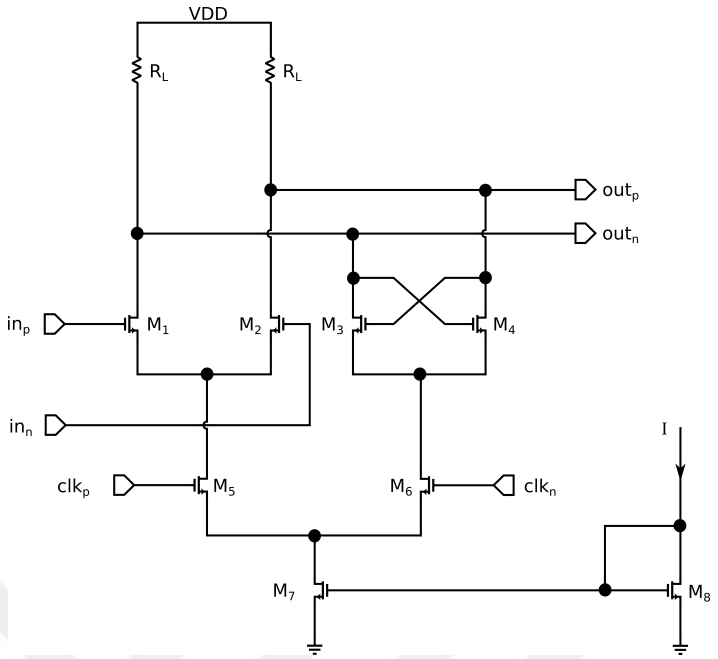

Figure 3.10. Latch in CML.

For proper operation, M_5 and M_6 have to be sized carefully to be able to work in saturation region. For example, when *clk* is high M_5 has to be able to draw all of the tail current. It will have a drain voltage as given in equation 3.4. If the drain-source voltage of M_5 drops such that it causes M_5 to go into triode region, some portion of the tail current will be drawn by M_6. Current drawn on the load resistor will result in a voltage drop at the output when it has to be at the supply voltage level. The amount of this voltage drop will result in an error if it causes the voltage level to drop below the proper logic high voltage level.

$$V_{D_5} = V_{high} - V_{GS_2} \tag{3.4}$$

3.2.5. Multiplexer

Figure 3.11 depicts the schematic of a two input CML multiplexer. Multiplexing either in_0 or in_1 is decided by *sel* input via directing the tail current either to the differential pairs $M_1 - M_2$ or $M_3 - M_4$. In the case that *sel* is low, M_5 will be ON and passes the tail current to $M_1 - M_2$. In this way, in_0 will be transferred to the output. Similarly, whenever *sel* is high, input in_1 will be passed to the output via $M_3 - M_4$ and M_6. Here, M_5 and M_6 should be sized carefully for the same consideration as mentioned for the latch in 3.2.4.

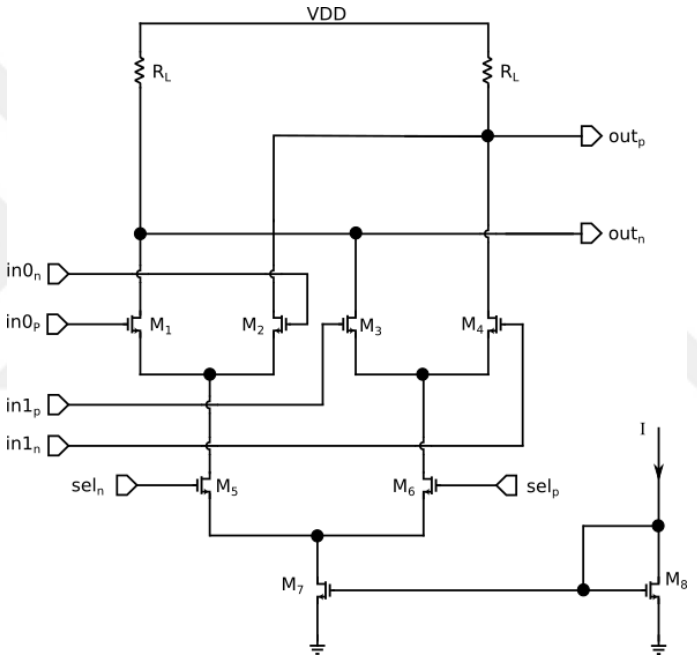

Figure 3.11. Multiplexer in CML.

3.3. Input Multiplexer

3.3.1. 2 to 1 Multiplexer with Latch

The block diagram of the 2 to 1 multiplexer with latch is given in Figure 3.12. First, in_1 and in_2 are latched when *sel* is low. Then in_0 is latched again when *sel* is high. Multiplexer inputs are latched such that they remain unchanged during multiplexing operation. When *sel* is high in_1 is multiplexed to the output. As the latch which

samples in_1 in hold mode during multiplexing, it will be transferred to the output of multiplexer successfully. Multiplexing in_0 works in the same way when *sel* input is low owing to the second latch in hold mode. Time diagram clarifying this multiplexing process is given in 3.13.

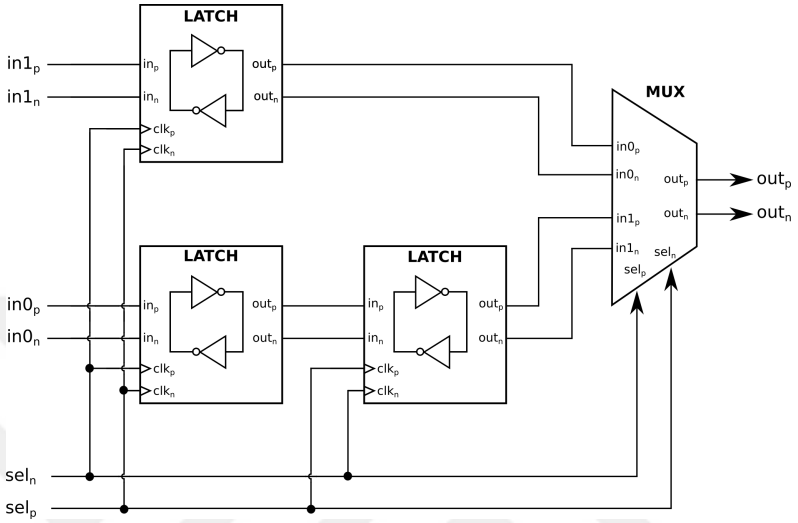

Figure 3.12. 2-1 Multiplexer with latch.

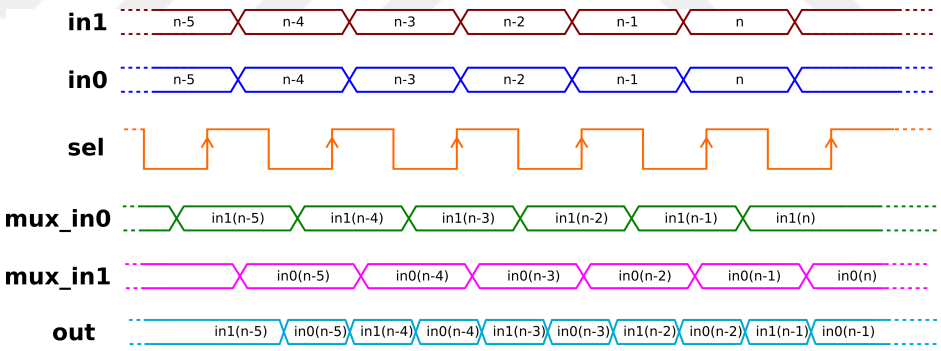

Figure 3.13. 2-1 Multiplexer with latch time diagram.

3.3.2. 4 to 1 Multiplexer

Figure 3.14 depicts a 4 to 1 multiplexer. It consists of two stage 2 to 1 multiplexers with latch. Digital data of the DAC is received through time interleaved A, B, C and D channels. Each of these four channels has a data rate of one-fourth of the operating clock frequency. In this block, these channels are serialized into one channel having a data rate which is equal the clock frequency.

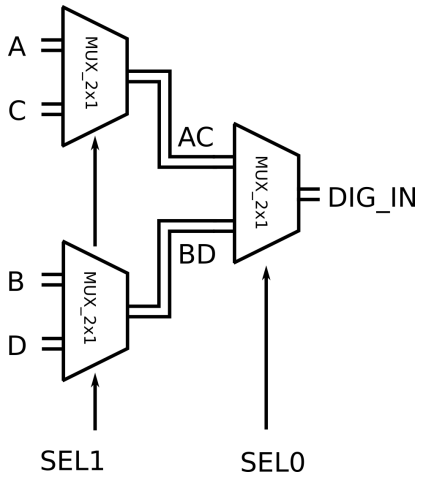

Figure 3.14. 4 to 1 Multiplexer.

At the first stage A-C and B-D channel pairs are sampled and multiplexed by $SEL1$. Since the frequency of $SEL1$ is one-fourth of the clock frequency AC and BD signals have a data rate which is half of the clock frequency. Then, AC and BD are sampled and multiplexed by $SEL0$ which has a frequency of half the clock frequency. Thus, A, B, C, and D channels are serialized into DIG_IN output. DIG_IN has a data rate which is the clock frequency. Figure 3.15 illustrates the timing diagram of this serializing process.

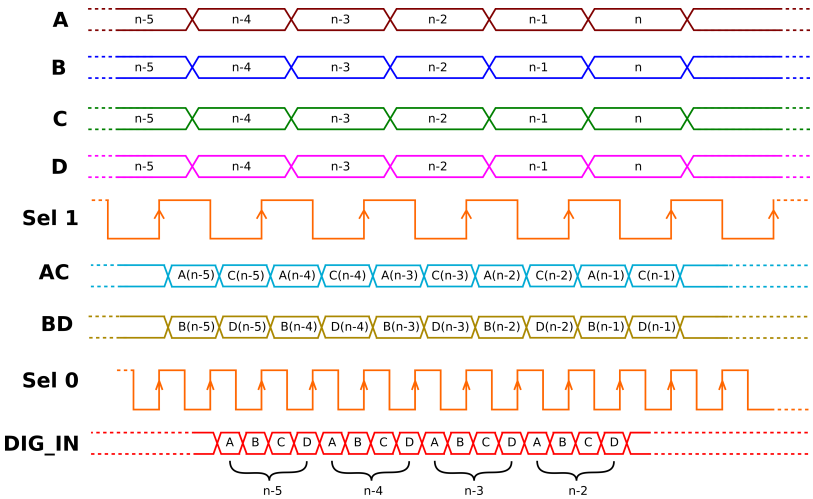

Figure 3.15. 4-1 Multiplexer time diagram.

3.4. Clock Tree

Block diagram of the clock tree in which the required clock signals are generated is given in Figure 3.16. Clock input of the system is a sinusoidal waveform with zero common mode voltage. At first, clock signal is terminated by clock termination circuit so that it has a common mode level suitable for the current mode logic applied in DAC. Then, it is amplified via CML buffers such that a square waveform is obtained.

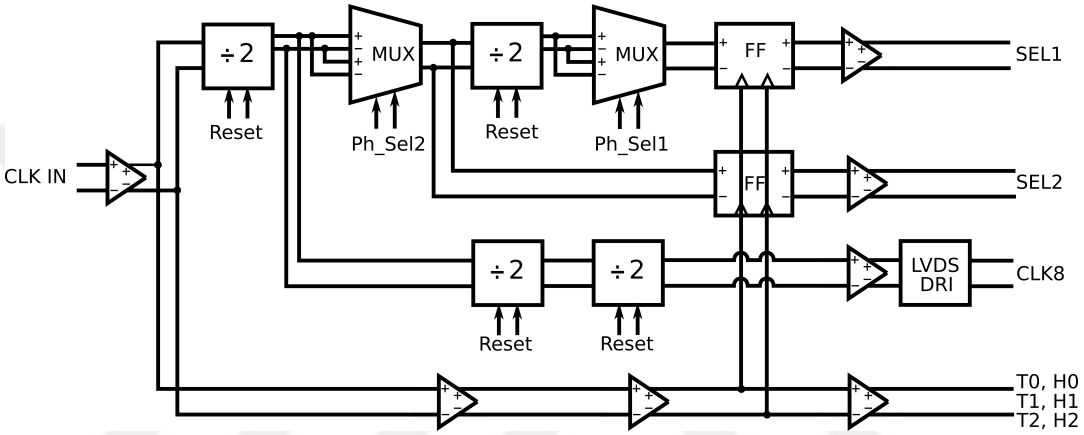

Figure 3.16. Clock tree block diagram.

$SEL1$ and $SEL2$ sample and select signals of the input multiplexer are generated by dividing the input clock. Each divider is followed by a multiplexer to select either divider output or its inversion via Ph_Sel2 and Ph_Sel1 select inputs. Dividing and multiplexing process of the clock signal results in four consecutive signals with 90 degrees phase difference. As illustrated in Figure 3.17, four combinations of the Ph_Sel1 and Ph_Sel2 inputs provides 90 degrees phase shifting while sampling the data inputs of the DAC. $SEL1$ and $SEL2$ are sampled by clock signal again to be synchronized with clock signal. During operation, the combination which allows most suitable sampling of the data input signals will be selected.

$CLK8$ is the output signal which allows synchronizing the digital inputs at A, B, C, and D channels. It has a frequency of one-eight of the clock frequency and it is in low voltage differential signalling standard trough a LVDS driver.

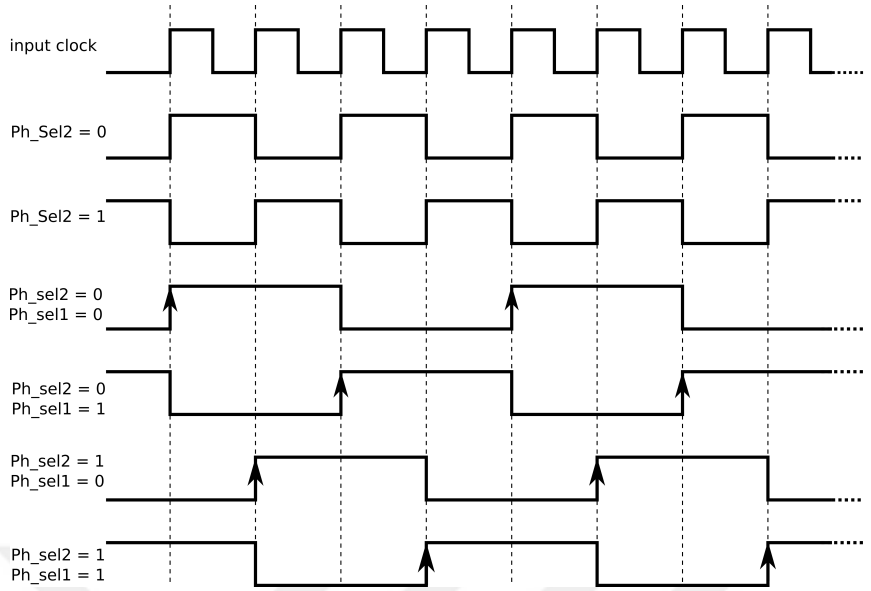

Figure 3.17. Time diagram of generating four different sampling signals.

Table 3.1 illustrates the LVDS input specifications of the Xilinx VIRTEX-7 FPGA. An LVDS driver which satisfies the requirements given in Table 3.1 is designed as seen in Figure 3.18. It has a tail current of 14 mA so that it has 350 mV differential output and 850 mV common mode voltage when it is terminated by an LVDS receiver. Additionally, $R_1 - R_2$ resistances and $C_1 - C_2$ capacitances are employed to reduce the ringing due to the bonding wire inductances.

Table 3.1. LVDS DC specifications [17].

	Symbol	DC Parameter	Min	Typ	Max	Units
1	V_{IDIF}	Differential input voltage	100	350	600	mV
2	V_{ICM}	Input common mode voltage	0.3	1.2	1.425	V

Clock tree has three other outputs $T0$, $T1$, $T2$ which have the same frequency with input clock. These signals are buffered such that they will be able to drive the synchronous parts at desired operating frequency.

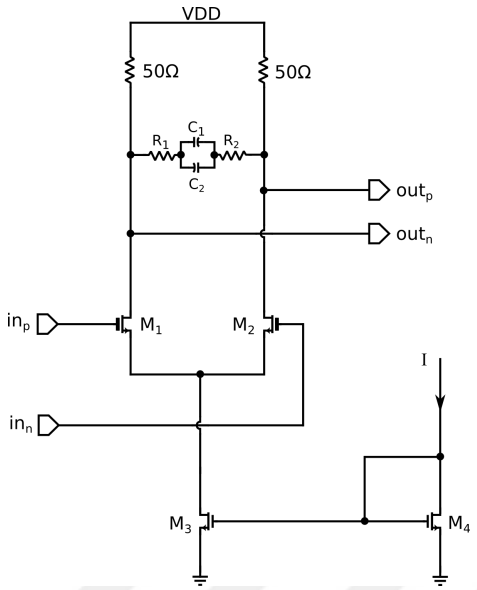

Figure 3.18. LVDS driver.

3.5. Binary to Thermometer Decoder

Figure 3.19 depicts the block diagram of the binary to thermometer decoder. $D < 11 : 0 >$ digital input which is generated by input multiplexer is first latched by $T0$. After that, most significant four bits of this synchronized bus is decoded to thermometer code via a combinational binary to thermometer decoder. Remaining least significant eight bits are buffered to make them delayed as much as binary to thermometer decoder combinational delay. Then, thermometer-decoded bits and delayed least significant seven bits are latched by $T1$ and $T < 1 : 15 >$ and $B < 8 : 1 >$ synchronized signals are obtained. Inversion of $T < 1 : 15 >$ and $B < 8 : 1 >$ are latched by complement of $T1$ clock signal to generate $T_Bar < 1 : 15 >$ and $B_Bar < 8 : 1 >$. Timing diagram of this binary to thermometer decoding process is provided in Figure 3.20.

Binary to thermometer decoder combinational block is the bottleneck of the whole system in terms of operation frequency. For proper operation, thermometer outputs have to settle to their final values when the latches at the output of the binary to thermometer decoder go into hold mode. To verify this condition, all possible 256 code-transitions of the most significant four bits are applied. Then, the eye diagram of the 15 thermometer outputs and hold signal is examined. Eye diagrams obtained in

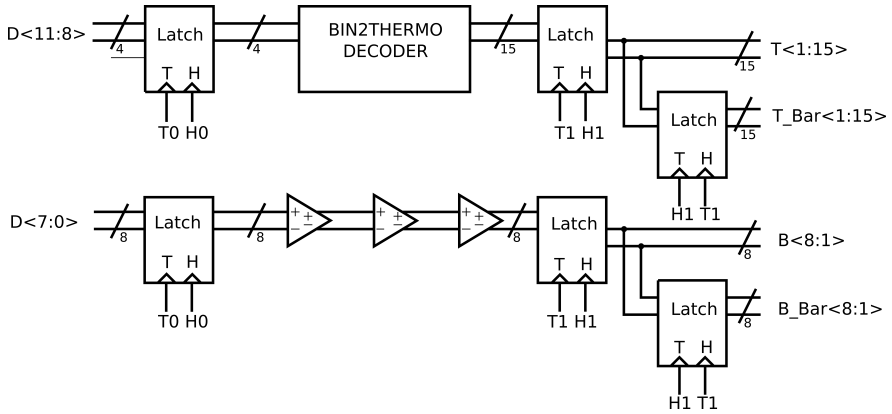

Figure 3.19. Binary to thermometer decoder block diagram.

different process, corner and temperature conditions are given in Figures 3.21-3.23.

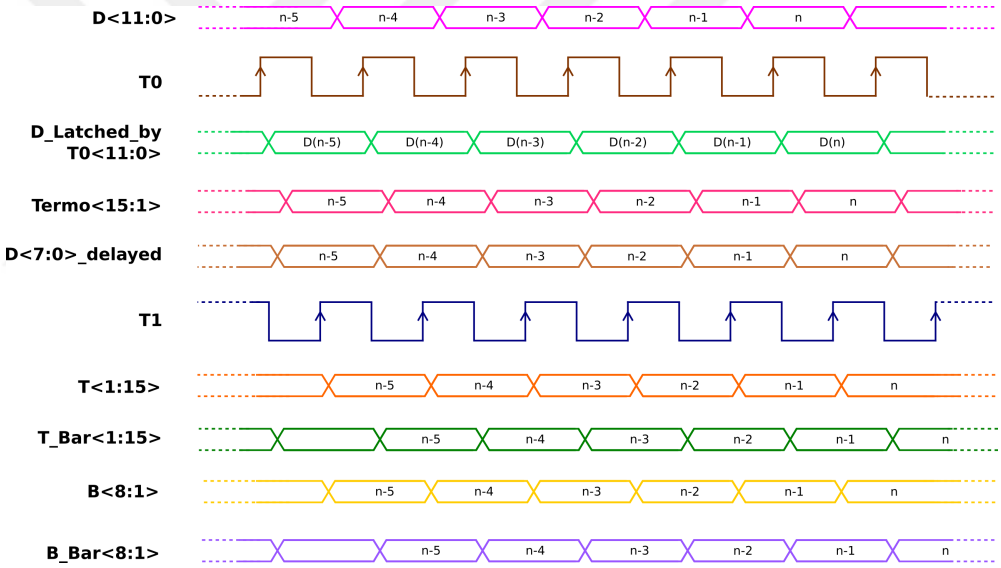

Figure 3.20. Binary to thermometer decoding time diagram.

Figure 3.21 illustrates that thermometer outputs of the combinational block are sampled properly at 3 GHz frequency at the worst corner where the whole circuit works in the slowest condition. The circuit is also forced to work at 3.4 GHz and still operates properly at the worst corner as depicted in 3.22. Finally, Figure 3.23 depicts that the eye opening increases by going to the fastest working conditions with lowest operating temperature, highest supply voltage and fastest process corner as expected.

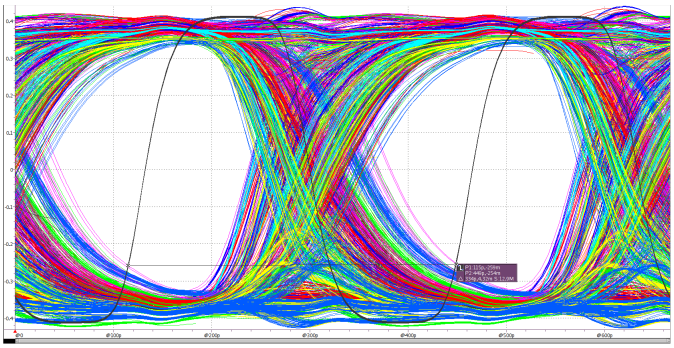

Figure 3.21. Eye diagram of the latching thermometer coded outputs for f_{clk} = 3 GHz, T = 100°C, vdd = 1.08 V at ss process corner.

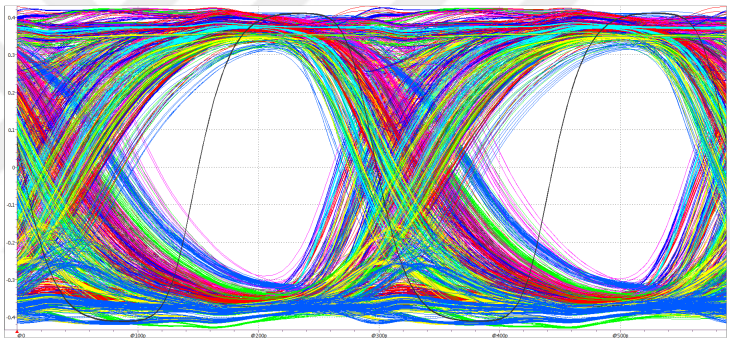

Figure 3.22. Eye diagram of the latching thermometer coded outputs for f_{clk} = 3.4 GHz, T = 100°C, vdd = 1.08 V at ss process corner.

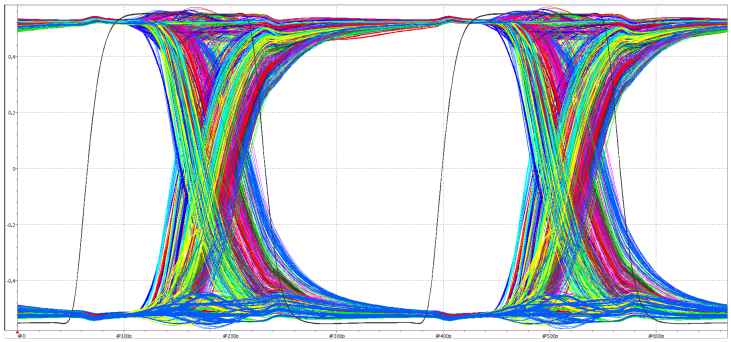

Figure 3.23. Eye diagram of the latching thermometer coded outputs for f_{clk} = 3 GHz, T = -40°C, vdd = 1.32 V at ff process corner.

3.6. Time-Interleaved Output Code Generator

The block diagram of time-interleaved output code generator is depicted in Figure 3.24. Thermometric codes $T < 1 : 15 >$ corresponding to the most significant four bits and their inverses $T_Bar < 1 : 15 >$ at the output of binary to thermometer decoder are time-interleaved via multiplexing by $T2$. Least significant eight bits $B < 8 : 1 >$ and their inverses $B_Bar < 8 : 1 >$ are also time-interleaved in the same way. Since $T2$ has a frequency which is equal to clock frequency, time-interleaved outputs $T_out < 1 : 15 >$ and $B_out < 1 : 15 >$ has a data rate of double the clock frequency.

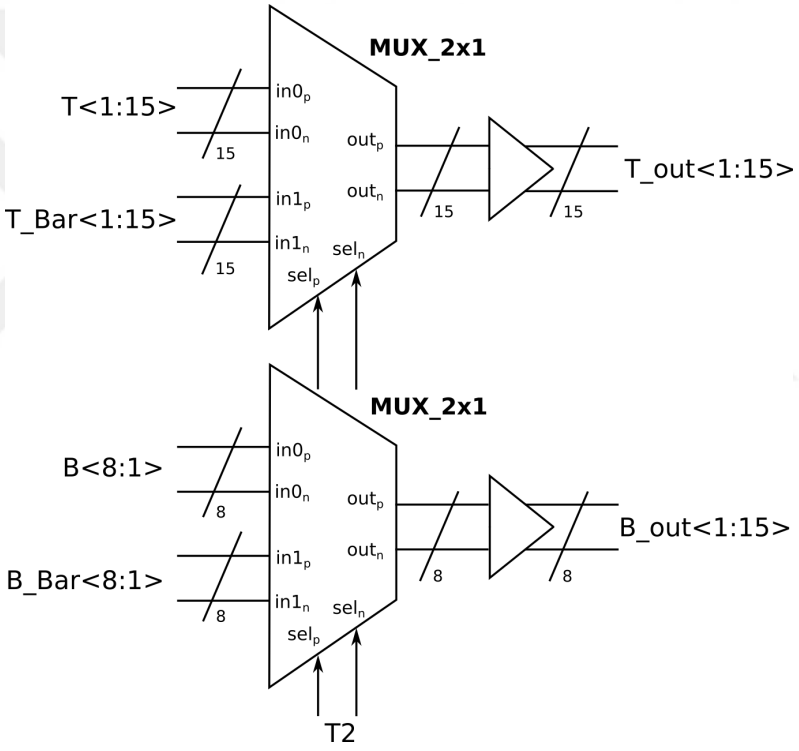

Figure 3.24. Time-interleaved output code generator.

Figure 3.25 illustrates the timing-diagram of the time-interleaved output code generation process. This time-interleaving process allows DAC current sources to be switched at each edge of the clock signal. Thus, switching becomes input code-independent.

In the case of zero-order hold (ZOH) response, the output level preserves its value during the sampling period T_S. This time-domain characteristic corresponds to a

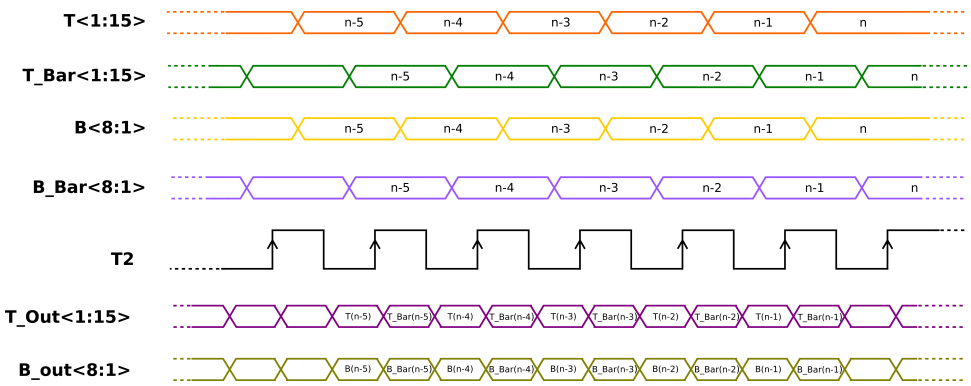

Figure 3.25. Time-interleaved output code generator time diagram.

frequency domain response as provided in equation 3.5 [15]. As depicted in Figure 3.26, zero-order hold frequency response is only available to get outputs at first Nyquist zone $(0 - f_s/2)$ due to the higher attenuation at second $(f_s/2 - f_s)$ and third $(f_s - 3 \cdot f_s/2)$ Nyquist zones.

$$A_{ZOH}(f) = \frac{\sin(\pi \cdot \frac{f}{f_s})}{\pi \cdot \frac{f}{f_s}} = sinc(\pi \cdot \frac{f}{f_s}) \tag{3.5}$$

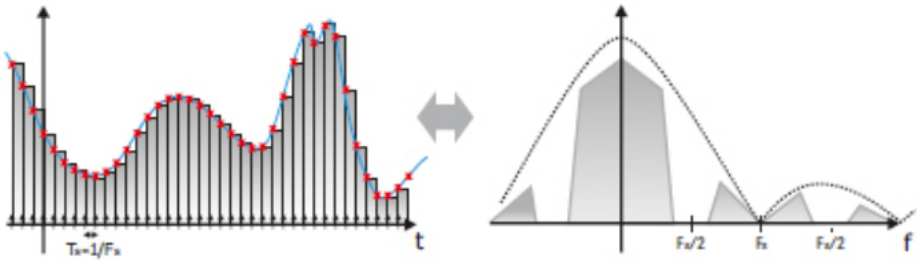

Figure 3.26. DAC zero-order-hold output in the (a)time and (b)frequency domains [15].

The time-interleaving process of the DAC output code and its inversion allows the DAC output code to occupy only the half of the sampling period and its inversion takes place in the rest. This behaviour is called the RF mode and results in a frequency response of the DAC as given in equation 3.6 [35].

$$A_{RF}(f) = \frac{\sin(\pi \cdot \frac{f}{f_s})}{\pi \cdot \frac{f}{f_s}} \cdot \sin(\pi \cdot \frac{f}{f_s}) \tag{3.6}$$

Figure 3.27 illustrates the output spectrum of the DACs in RF and zero-order hold modes. In contrast to the DAC in zero-order hold mode, the frequency response of the DAC in RF mode has more attenuation in the first Nyquist zone and less attenuation in the second and third Nyquist zones. Hence, this mode allows the user to get outputs at the second and third Nyquist zones.

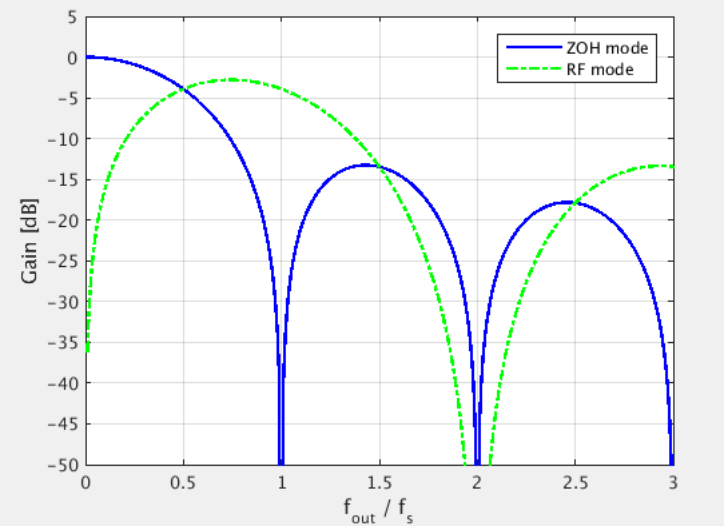

Figure 3.27. Frequency responses of DACs in ZOH and RF modes.

3.7. DAC Current Sources and Switches

Figure 3.28 illustrates DAC current sources and switches. Switches are controlled by time-interleaved thermometric and binary codes such that when the code is high for a certain bit, whole the current is directed to positive current output and vice versa when the code is low.

Cascode current sources are applied as the DAC current sources to achieve high output impedance. At higher frequencies, output impedance decreases due to the ca-

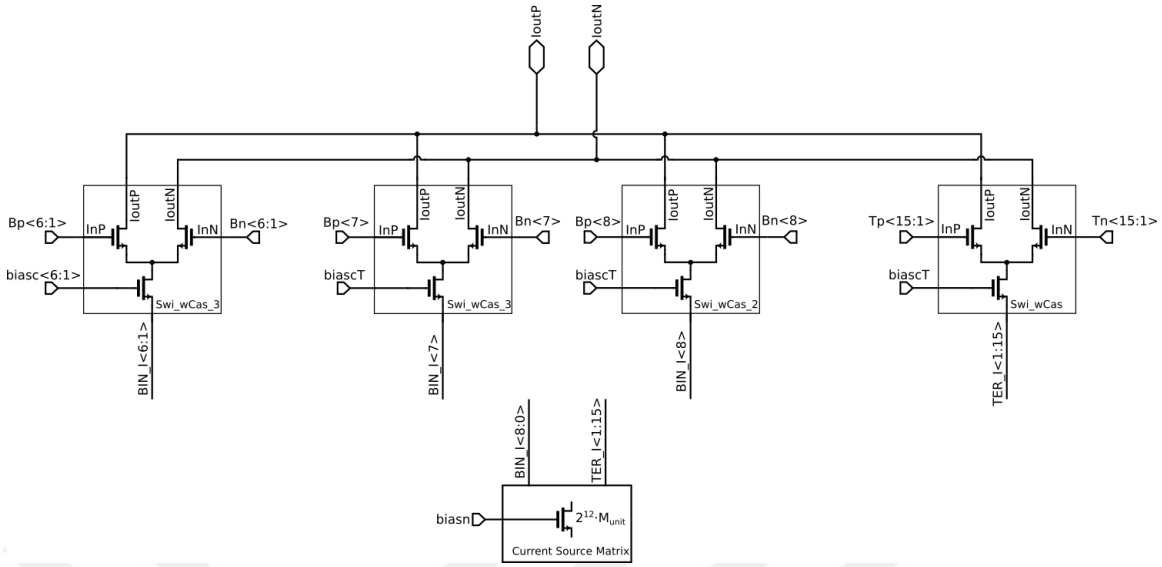

Figure 3.28. DAC current sources and switches.

pacitances of the output node. This capacitance arises from the parasitic capacitance of the drain terminal of the cascode transistor, the source terminal of the switch transistors and the wire connecting them. The cascode and switch transistors are placed as close as possible in the layout to minimize the output capacitance.

Three different cascode and switch transistor blocks are designed which are named Swi_wCas, Swi_wCas_2 and Swi_wCas_3. Transistor sizes are the only difference between these blocks. Swi_wCas stands for thermometric codes $T < 1 : 15 >$, Swi_wCas_2 stands for most significant binary code $B < 8 >$ and Swi_wCas_3 stands for least significant seven bits $B < 7 : 1 >$. The underlying reason for three different blocks is to force the current source transistors to have equal drain-source voltage.

Transistors used in Swi_wCas, Swi_wCas_2 and Swi_wCas_3 are sized such that they have equal current density. Having equal current density results in equal gate-source voltage for cascode and switch transistors. Thus, current-source transistors will have the same amount of drain-source voltage and channel length modulation effect will be minimized. On the other hand, Swi_wCas_3 is applied for the least significant seven bits which means that the least significant six bits do not have the same current density. Nonetheless, the amounts of the currents which stand for the least significant

six bits are relatively smaller than the higher order ones. Currents of these amounts will not create significant gate-source voltage drop on both switch and cascode transistors. Thus, current source transistors corresponding to the least significant seven bits will be almost equal and current length modulation effect is minimized.

Length of cascode and switch transistors in all three blocks are chosen as the minimum length available in the process. Thus, width of these transistors does not need to be too large to allow sufficient drain-source voltage headroom to the current source transistors. Having smaller width will result in smaller output parasitic capacitance to the cascode current sources.

Output resistance and drain-source saturation voltage are the key parameters on deciding current source transistor sizes. Output resistance increases with increasing transistor length. However, increasing length requires larger width to sustain the same amount of drain-source saturation voltage. So, there is a trade-off between output resistance and transistor sizes. Current source transistor sizes are decided such that they have a proper output resistance and drain-source saturation voltage.

The current source transistor corresponding to a bit consists of a unit current source which stands for the least significant bit. For example, the current source of thermometric coded bit consists of 255 unit current source transistors, whereas the current source for the least significant third bit employs 4 units. Current source transistors are laid out in a matrix style along with dummy transistor blocks around the matrix to minimize mismatch effects. Furthermore, source terminal connections of the unit current sources are laid out in a H-tree form to minimize the gate-source voltage mismatch. Figure 3.29 depicts the layout of the current source matrix.

The current source matrix consists of 5184 unit transistors. 4096 of them stand for the unit current source transistor. The remaining 1088 transistors constitute the outer dummy block. Each of the indices $1-15$ represent 256 unit current source blocks for thermometric codes. On the other hand, the index 0 stands for the 256 unit current sources belonging to the least significant eight bits along with the dummy one.

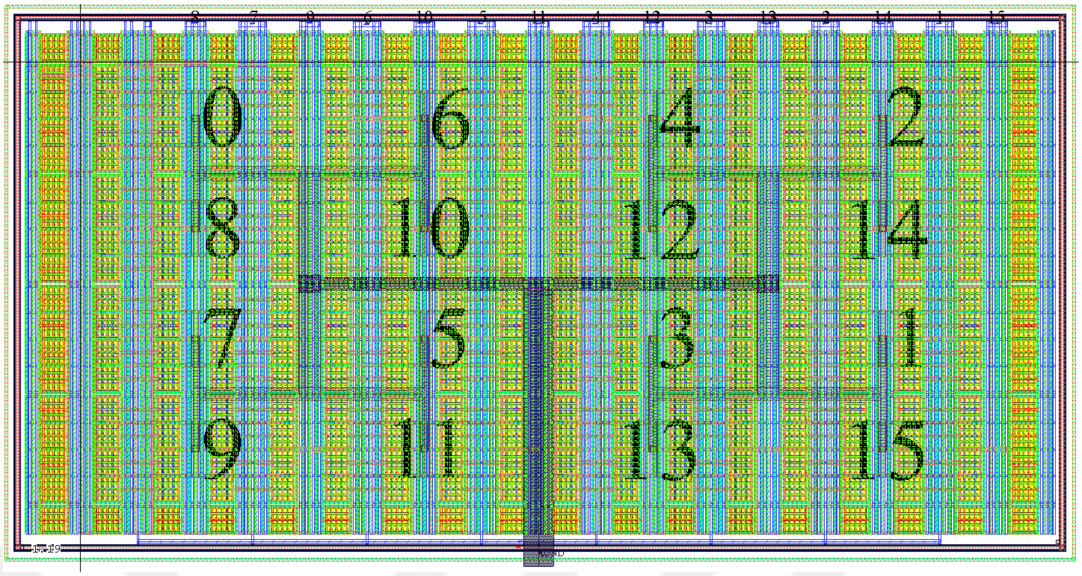

Figure 3.29. DAC current source matrix layout.

3.8. DAC Output Stage

Figure 3.30 depicts the schematic of the output stage of the DAC. $IoutP$ and $IoutN$ inputs are the DAC currents which are generated by switching current sources as mentioned in section 3.7. These current inputs are buffered to the output via cascode transistors M_{14} and M_{15}.

Differential DAC output is generated by converting DAC currents $IoutP$ and $IoutN$ to differential voltages on 50Ω load resistors. Since, the supply voltage for the DAC output is 2.5 V, M_{14} and M_{15} have to be thick-oxide transistors. Cascode current sources including $M_3 - M_{13}$ are employed to provide a DC current of 6 mA to the cascode transistors M_{14} and M_{15}. Having some DC current allows switching without distortion by satisfying constant gate-source voltage to M_{14} and M_{15} [19]. Output cascode transistors also bring about enhanced output impedance and reduced parasitic effects of the switch transistors [19]. Besides, they reduce the clock feed-through and coupling of control signals to the output.

Gate voltage of the output cascode transistors is achieved through a resistive divider. The amount of this voltage and the sizes of the cascode transistors are decided

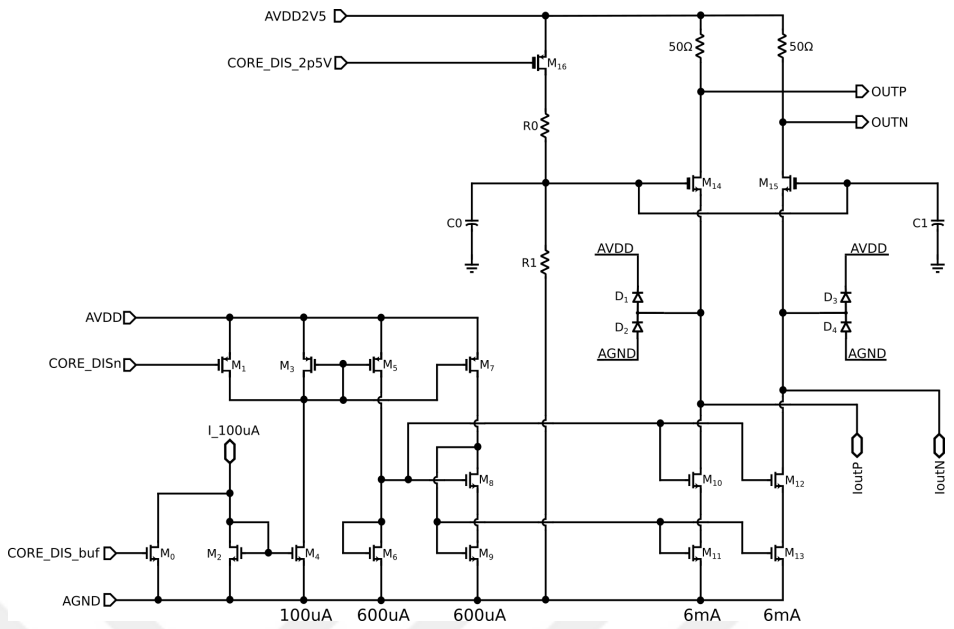

Figure 3.30. DAC output stage.

such that output cascode transistors, transistors belonging to DAC current sources, and DC current sources will always operate in saturation region. It also required to be satisfied that source voltage level of cascode transistors does not exceed 1.2 V because transistors which belong to DC and DAC current sources are the type of thin-oxide. The diodes $D_1 - D_4$ allow further protection by limiting maximum source voltage level of the cascode transistors. On the other hand, M_0, M_1 and M_{16} are utilized to disable the current sources and resistive divider when it is desired.

4. SIMULATION

4.1. Coherent Sampling

To achieve a proper FFT operation, the input is required to replicate itself periodically. If the input signal is not periodic as assumed, transition from the current to the next consecutive sequence will not be continuous as depicted in Figure 4.1 [8]. This corresponds to spectral leakage at the output spectrum such that the energy, which has to be at the input signal frequency, disperses to the adjacent frequencies [8].

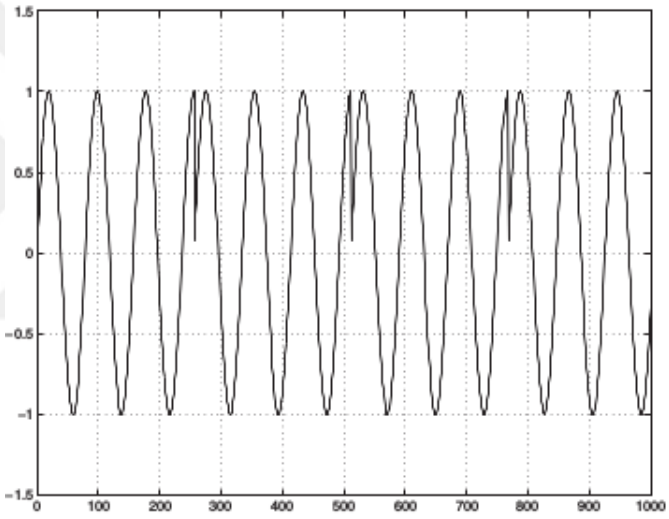

Figure 4.1. A signal that misses N-periodicity leads to discontinuities [8].

Windowing the input signal is a technique to minimize the spectral leakage [16]. However, windowing may not provide a single tone at the output spectrum when the input is a sine wave. Thus, coherent sampling should be applied to prevent spectral leakage [8].

If the input sampling window consists of an integer number of cycles of a periodic signal, it is called coherent sampling. Equation 4.1 defines the relationship between the input sine wave and the sampling frequency [16].

$$\frac{f_{IN}}{f_{SAMPLE}} = \frac{N_{WINDOW}}{N_{RECORD}} \tag{4.1}$$

Here, N_{RECORD} corresponds to the number of samples which has to be power of 2 and N_{WINDOW} defines the number of input cycles which fit into the sampling window. Besides, N_{WINDOW}/N_{RECORD} should be irreducable so that repeated codes will not occur. [16]. Figures 4.2 - 4.3 illustrate FFT plots for coherent and non-coherent sampled input signals.

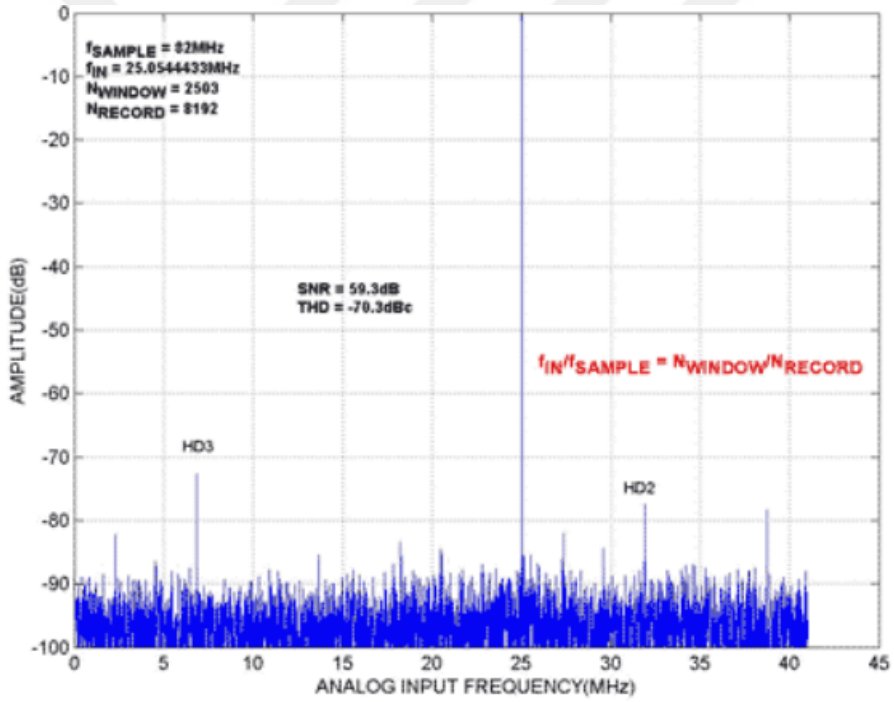

Figure 4.2. FFT plot for coherently sampled input signal [16].

As depicted in Figures 4.2 and 4.3, there is only a spike at the frequency of the input in the case of coherent sampling, whereas spectral leakage occurs for the non-coherent one.

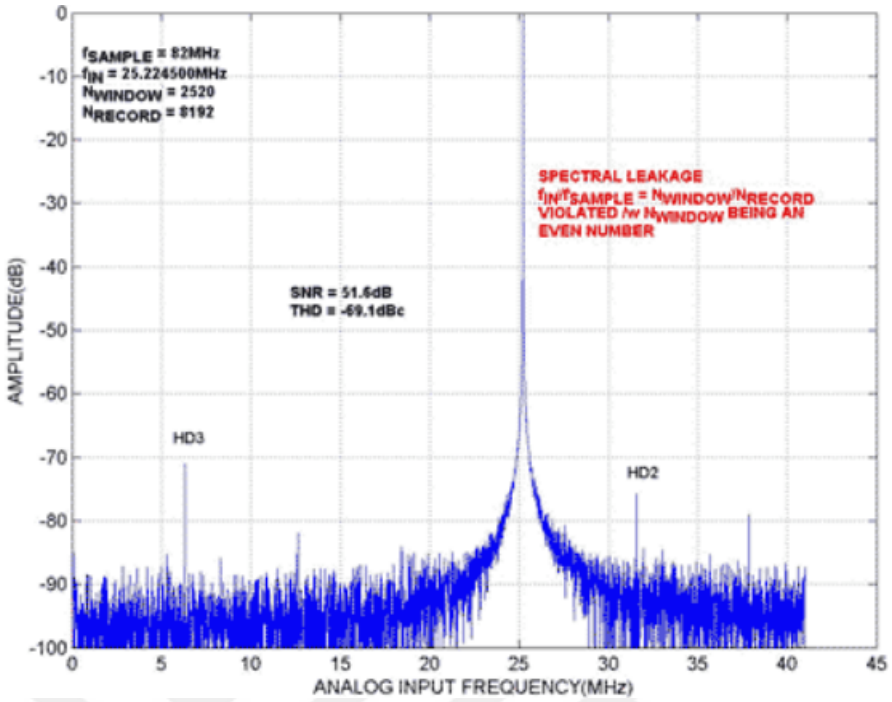

Figure 4.3. FFT plot for non-coherently sampled input signal [16].

4.2. Simulation Set-Up

Figure 4.4 depicts the block diagram of the simulation set up. Input signal *in* is a 12-bit sine wave digital input which has a data rate of one-fourth of the clock frequency. This input is directly applied to the D channel of the DAC, whereas inputs of A, B, and C channels are obtained via delaying the input *in*. As a result of the delaying process, *nth* sample of the inputs of the channels will be obtained as given in equations 4.2 - 4.5. Thus, serializing sine wave inputs at A, B, C, and D into one channel generates a sine wave which has a data rate of the clock frequency as mentioned in 3.3.2.

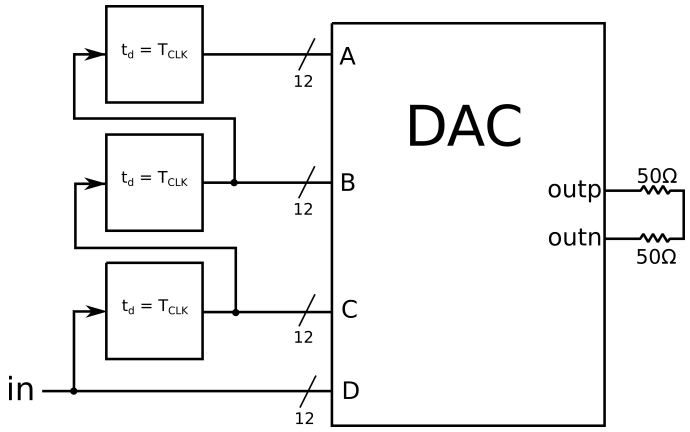

Figure 4.4. Simulation set-up of the DAC.

$$A[n] = sin(2\pi f_{in}(t - 3T_{CLK})) \tag{4.2}$$

$$B[n] = sin(2\pi f_{in}(t - 2T_{CLK})) \tag{4.3}$$

$$C[n] = sin(2\pi f_{in}(t - T_{CLK})) \tag{4.4}$$

$$D[n] = sin(2\pi f_{in}(t)) \tag{4.5}$$

Single-ended DAC output is generated as given in equation 4.6.

$$out = outp - outn \tag{4.6}$$

4.3. Simulation Results

During simulations f_{in} is decided such that coherent sampling condition is satisfied. Simulation time has to be larger than N_{RECORD} sample duration so that all of the required samples can be achievable by FFT. Hence, higher N_{RECORD} will result in higher simulation time to run. On the other hand, N_{RECORD} should be large enough

for modelling the DAC. Thus, N_{RECORD} is decided as 512 according to this trade-off. Chosen N_{WINDOW} and corresponding f_{IN} values for 3 GHz sampling frequency are provided in Table 4.1.

Table 4.1. N_{WINDOW} and corresponding f_{in} values for f_{SAMPLE} = 3 GHz.

	N_{WINDOW}	f_{IN} [MHz]
1	11	64.453125
2	53	310.546875
3	73	427.734375
4	97	568.359375
5	127	744.140625
6	149	873.046875
7	173	1013.671875
8	193	1130.859375
9	223	1306.640625

Post-layout simulations are run for the netlists in which worst case parasitic capacitance extraction is taken into the account. Figures 4.5 - 4.7 illustrates DAC output spectrums for N_{WINDOW} = 53. Figures 4.8 - 4.10 depict the SFDR results for the input frequencies given in Table 4.1. Simulation results show that the DAC has SFDR up to 60 dB for typical process corner and 25°C temperature.

Current drawn from both 1.2 V and 2.5 V supply voltages during simulation for typical process and 25°C temperature condition are given in Table 4.2. Thus, the DAC consumes 922 mW power at these process and temperature condition.

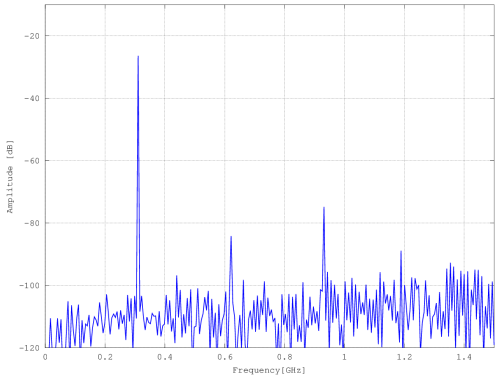

Figure 4.5. First Nyquist spectrum of DAC output for $N_{WINDOW} = 53$, $f_{SAMPLE} = 3$ GHz, T = 25°C, vdd = 1.2 V at tt process corner.

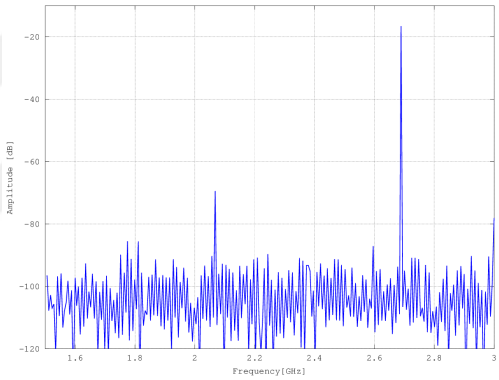

Figure 4.6. Second Nyquist spectrum of DAC output for $N_{WINDOW} = 53$, $f_{SAMPLE} = 3$ GHz, T = 25°C, vdd = 1.2 V at tt process corner.

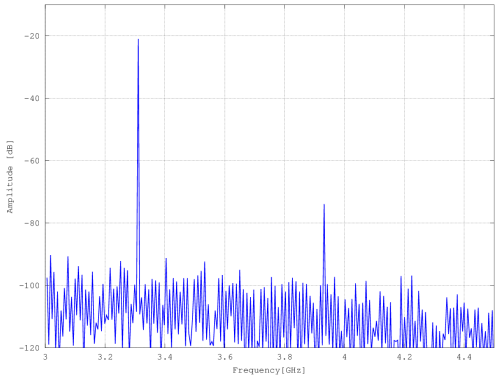

Figure 4.7. Third Nyquist spectrum of DAC output for $N_{WINDOW} = 53$, $f_{SAMPLE} = 3$ GHz, T = 25°C, vdd = 1.2 V at tt process corner.

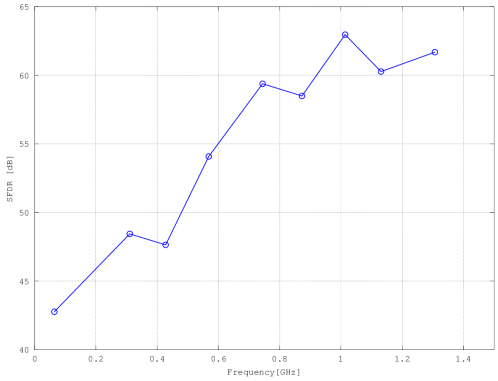

Figure 4.8. First Nyquist band SFDR values for f_{SAMPLE} = 3 GHz, T = 25°C, vdd = 1.2 V at tt process corner.

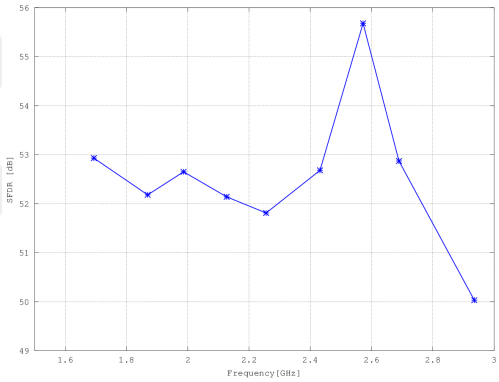

Figure 4.9. Second Nyquist band SFDR values for f_{SAMPLE} = 3 GHz, T = 25°C, vdd = 1.2 V at tt process corner.

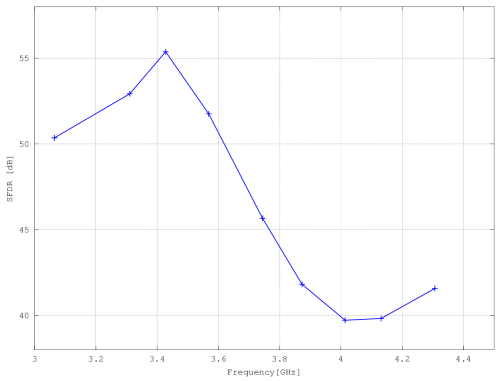

Figure 4.10. Third Nyquist band SFDR values for f_{SAMPLE} = 3 GHz, T = 25°C, vdd = 1.2 V at tt process corner.

Table 4.2. Current which are drawn from the supplies during the simulation.

	Supply Voltage	Current
1	1.2 V	710 mA
2	2.5 V	28 mA

5. MEASUREMENT

Measurement set-up block diagram of the DAC is depicted in Figure 5.1.

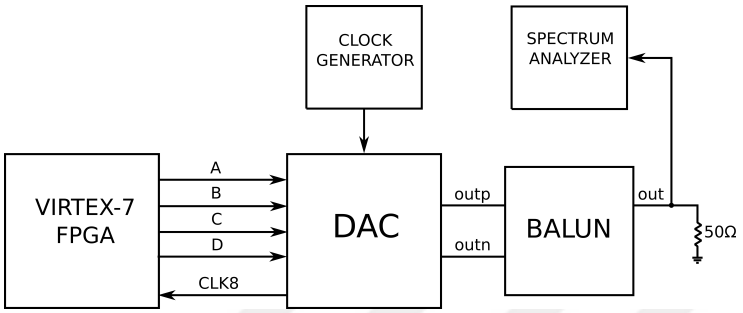

Figure 5.1. Block diagram of the measurement set-up of the DAC.

Time-interleaved sine wave inputs at A, B, C, and D channels are generated through a direct digital frequency synthesizer (DDFS) on VIRTEX-7 field programmable gate array (FPGA). These inputs are synchronized with $CLK8$ which has the frequency of one-eight of the operating clock frequency. Since data is transferred on both rising and falling edge of the $CLK8$, A, B, C, and D channels operate at dual data rate (DDR). Hence, they have a data rate of one-fourth of the clock frequency as desired.

A balun is employed to convert DAC differential output to single ended signal. Balun is a device which allows transformation between two-terminal balanced (none of its terminals are connected to ground) and imbalanced (one of its terminals are connected to ground) impedances [36]. For operation without reflection, 100Ω differential output impedance of the DAC should be terminated by two-terminal balanced impedance of 100Ω. Therefore, balun is decided such that it has 2:1 balanced to imbalanced impedance transformation ratio. Hence, the balun allows 100Ω balanced impedance termination to the DAC when it has a imbalanced load of 50Ω.

Figure 5.2 shows the measurement set-up. Output of the balun is connected to the Agilent PXA N9030A Spectrum Analyzer. Agilent N6705B Power Supply is utilized as the power supply while the clock input is generated through Rohde&Schwarz SMA100A

clock generator.

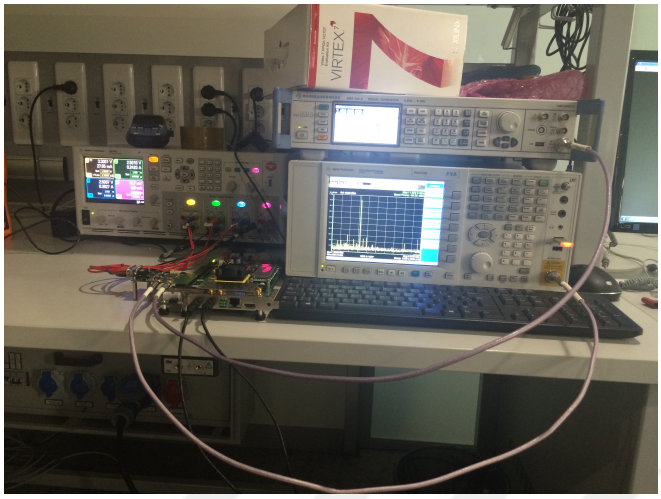

Figure 5.2. DAC measurement set-up.

When a certain input frequency is applied to the DAC, start and stop frequency of the spectrum analyzer are set such that they cover the interested Nyquist zone. Then, signal power is found by searching the peak of the selected frequency region. Similarly, highest spur is decided by searching the next peak. Then, SFDR is obtained by calculating the difference between the signal and spur powers. Figure 5.3 depicts the SFDR measurement at second Nyquist zone with the applied input frequency of 1.203 GHz and the clock frequency of 3 GHz.

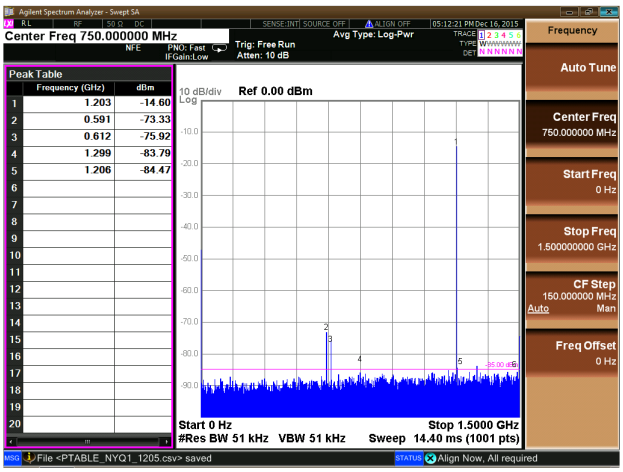

Figure 5.3. First Nyquist spectrum measurement of the DAC for $f_{clk} = 3$ GHz and $f_{in} = 1.203$ GHz.

Input signal frequency is swept from 105 MHz to 1.455 GHz with a step size of 50 MHz when the clock frequency is 3 GHz. Therefore, the performance of any Nyquist zone can be observed with a resolution of 50 MHz. Besides, these measurements are repeated for four different temperatures of $-40°C$, $30°C$, $85°C$ and $100°C$. Hence, thermal performance is also characterized. Figures 5.4 - 5.6 illustrate the first, second, and third Nyquist spectrum measurement of the DAC for $f_{clk} = 3$ GHz. It is seen that the DAC achieves SFDR up to 65 dB.

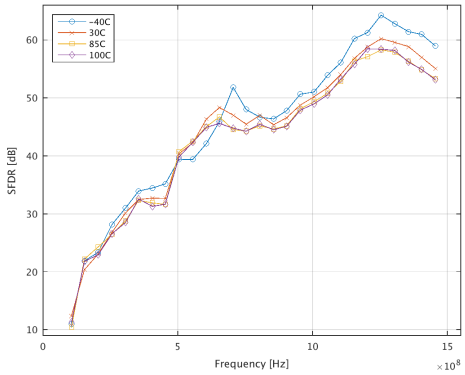

Figure 5.4. First Nyquist spectrum measurement results for $f_{clk} = 3$ GHz.

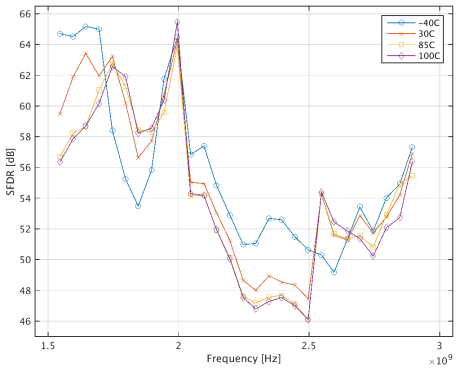

Figure 5.5. Second Nyquist spectrum measurement results for $f_{clk} = 3$ GHz.

Operating clock frequency is increased to 3.4 GHz and 3.8 GHz to observe the higher frequency performance. The spectral performance of the first three Nyquist zones for 3.4 GHz and 3.8 GHz operating frequency are measured as seen in Figures 5.7-5.12. It is seen that the DAC reaches SFDR up to 65 dB for 3.4 GHz and 3.8 GHz operating frequencies too.

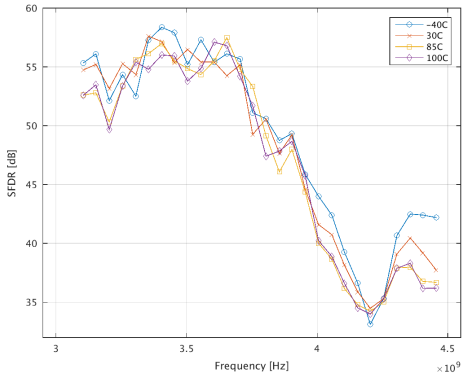

Figure 5.6. Third Nyquist spectrum measurement results for $f_{clk} = 3$ GHz.

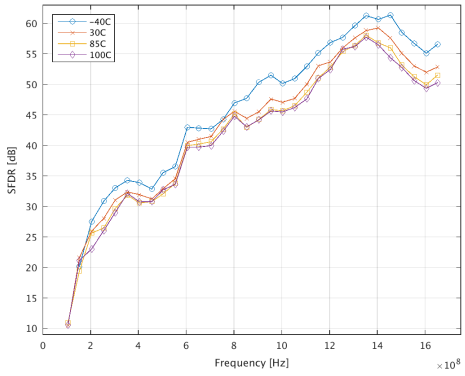

Figure 5.7. First Nyquist spectrum measurement results for $f_{clk} = 3.4$ GHz.

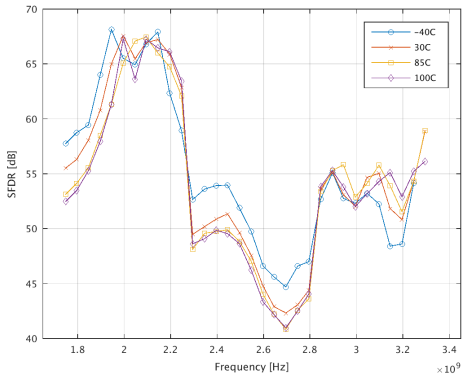

Figure 5.8. Second Nyquist spectrum measurement results for $f_{clk} = 3.4$ GHz.

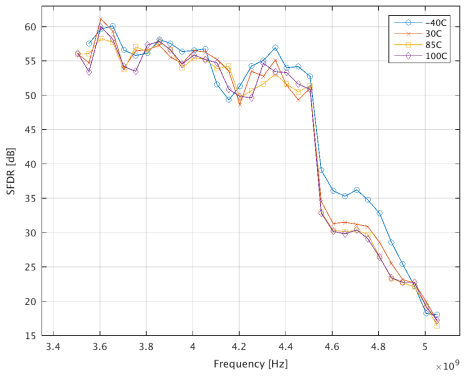

Figure 5.9. Third Nyquist spectrum measurement results for $f_{clk} = 3.4$ GHz.

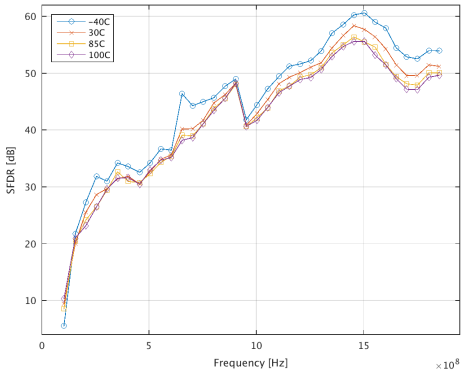

Figure 5.10. First Nyquist spectrum measurement results for $f_{clk} = 3.8$ GHz.

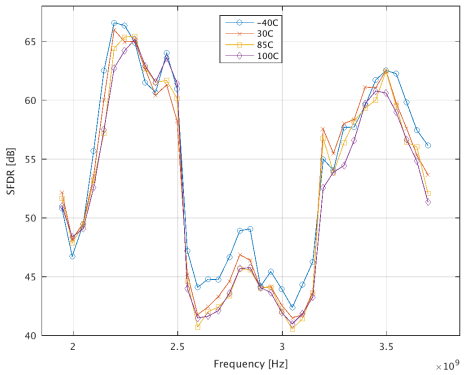

Figure 5.11. Second Nyquist spectrum measurement results for $f_{clk} = 3.8$ GHz.

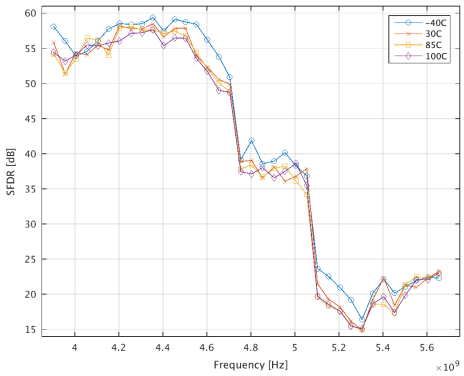

Figure 5.12. Third Nyquist spectrum measurement results for $f_{clk} = 3.8$ GHz.

Table 5.1 illustrates the current drawn from the supply voltages. It shows that, the DAC has a power consumption of 830 mW for measurements at 30°C.

Table 5.1. Current which are drawn from the supplies during the measurement.

	Supply Voltage	Current
1	1.2 V	634 mA
2	2.5 V	28 mA

6. CONCLUSION

In this thesis work, a 12-bit 3 GS/s current steering DAC in 65nm CMOS process is presented. The DAC is designed to achieve a proper spectral performance for modern communication systems. Dynamic and static errors which degrade the spectral performance are examined.

Digital to analog conversion concept along with the basic architectures and performance specifications are explained in detail. Current mode logic which is utilized in all digital sections is introduced briefly. DAC architecture and current source type decisions are explained. All the blocks in the DAC are examined comprehensively. Besides, bias generation of the DAC is also explained in detail.

At the first hand, the DAC is implemented in schematic level. Then, the layout is generated manually. Post-layout simulations which take the parasitic effects of the layout into the account are run to see the spectral performance. Coherent sampling which allows FFT results without spectral leakage is employed when simulating the DAC. Coherent sampling is also explained in detail.

Post-layout simulation results indicate that the DAC consumes 922 mW and has SFDR up to 60 dB for 3 GHz operating clock frequency and typical process conditions. On the other hand, measurement results show that DAC reaches SFDR up to 65 dB and has a power consumption of 830 mW for 3 GHz operating clock frequency. Furthermore, operating frequency is increased to 3.4 and 3.8 GHz to see higher speed behaviour of the DAC. It is seen that, the DAC has SFDR up to 65 dB for 3.4 and 3.8 GHz operating frequencies as well.

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