DESIGN OF HIGH EFFICIENCY BUCK CONVERTERS

by

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ABSTRACT

DESIGN OF HIGH EFFICIENCY BUCK CONVERTERS

Buck converters are used for battery operated systems which supply a wide current range and very low output voltage ripple even when the input voltage changes by more than two orders of magnitude. The converter has to sustain an excellent power efficiency and be able to support load current switching from *0A* to I_{max} with minimum output voltage ripple. Increasing the power efficiency in a switching buck converter requires decreasing the power losses in both light and heavy load operations. However, the light load efficiency is the major concern since portable systems spend their majority of time in idle mode. This work introduces a novel method for increasing efficiency in buck converter systems by utilizing an adaptive output stage size selection technique which decides on the active number of stage segments by comparing capacitive and resistive losses. It takes into account the input supply voltage variation, operating frequency, gate capacitance, actual R_{ON} information and load current and finds optimal stage size to obtain optimal efficiency in a switching converter. This is the only work in the literature which conducts high efficiency in light loads without changing the modulation scheme or frequency of switching converter. Two patent applications have been made throughout this work as *US14695492*: Method for an Adaptive Transconductance Cell Utilizing Arithmetic Operations and *US14712941*: High Efficiency DC/DC Converter with Adaptive Output Stage.

ÖZET

YÜKSEK VERİMLİ DÜŞÜREN DÖNÜŞTÜRÜCÜ TASARIMI

Düşüren dönüştürücüler, giriş gerilimi iki kattan fazla değişse bile geniş bir akım ve çok düşük çıkış gerilim dalgalanması sağlayabilen, pille çalışan sistemlerde kullanılır. Dönüştürücü, mükemmel bir güç verimi sağlamalı ve *0A*'den maksimum akıma kadar değişebilen çıkış akımlarını asgari çıkış gerilim dalgalanması ile sağlayabilmelidir. Bir anahtarlamalı dönüştürücünün güç verimini artırmak, hafif ve ağır akım şartlarının ikisinde de güç kaybını azaltmayı gerektirir. Ancak, taşınabilir sistemler zamanlarının çoğunu bekleme modunda geçirdikleri için, hafif akım verimi esas sorundur. Bu çalışma, kapasitif ve dirençli kayıpları karşılaştırarak çıkış katı bölümlerinin aktif sayısına karar veren bir adaptif çıkış katı seçim tekniği kullanarak, düşüren dönüştürücü sistemlerinde verimi artırmak için yeni bir yöntem getirmiştir. Geliştirilen yöntem, giriş besleme gerilimindeki değişimi, çalışma frekansını, kapı kapasitesini, gerçek direnç bilgisini ve çıkış akımını dikkate alır ve bir anahtarlamalı dönüştürücüde optimum verim için optimum çıkış katı büyüklüğünü bulur. Bu, modulasyon şemasını veya anahtarlamalı dönüştürücünün frekansını değiştirmeden düşük akımlarda yüksek verimi sağlayan literatürdeki tek çalışmadır. Bu çalışma boyunca, *US14695492* numaralı "Aritmetik operasyonları kullanan adaptif transkonduktans hücresi yöntemi" adlı ve *US1471294* numaralı "Adaptif çıkış katı ile yüksek verimli DC/DC dönüştürücüler" adlı iki adet patent başvurusu yapılmıştır.

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LIST OF SYMBOLS

C_{esr}	ESR resistance of output capacitor of buck converter
C_{load}	Output capacitor of buck converter
C_{gg}	Gate capacitance of MOSFET
C_{out}	Output capacitance of buck converter
C_{ox}	Oxide thickness of MOSFET
F_{GBW}	Gain bandwidth frequency
f_p	Pole of a negative feedback control loop
F_{SW}	Switching frequency
f_z	Zero of a negative feedback control loop
g_m	Transconductance of MOSFET
$I_{control}$	Control current in current mode feedback loop
I_{DDQ}	Quiescent current
$I_{DDQ,OFF}$	Leakage current
I_L	Coil current
I_{Lavg}	Sense current of adaptive output buck converter
I_{LOAD}	Load current of buck converter
I_{out}	Output current of buck converter
I_{seg}	Segment current of adaptive output buck converter
I_{sense}	Sense current of adaptive output buck converter
L	Inductor of buck converter
L_{coil}	Inductor of buck converter
N	Number of segments of adaptive output buck converter
n_f	Number of segments of adaptive output buck converter
P_C	Capacitive power
P_R	Resistive power
R_{ind}	Series DC resistance of coil
R_{ON}	On resistance of MOSFET
T_{SW}	Switching period
V_{DD}	Supply voltage

V_{err}	Error voltage
V_{fb}	Feedback voltage of buck converter
V_{out}	Output voltage of buck converter
V_{ov}	Overdrive voltage of MOSFET
V_{ref}	Reference voltage of buck converter
V_{sense}	Voltage drop on PMOS driver of adaptive buck converter
η	Efficiency
μ_n	Mobility of NMOS
μ_p	Mobility of PMOS
σ	Sigma

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
AGS	Adaptive Gate Swing
BM	Burst Mode
CCR	Capacitor-based Charge Recycling
CMC	Current Mode Control
CMOS	Complementary Metal Oxide Semiconductor
D	Duty Cycle
DC	Direct Current
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FF	Fast NMOS - Fast PMOS
FNSP	Fast NMOS - Slow PMOS
GM	Gain Margin
HIGH	High Passive Elements
IC	Integrated Circuit
LDO	Low Drop Out Regulator
LOW	Low Passive Elements
MC	Monte Carlo
MIMCAP	Metal-Insulator-Metal Capacitor
MOSCAP	Metal Oxide Semiconductor Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N Channel Metal Oxide Semiconductor
NOM	Nominal Passive Elements
PFM	Pulse Frequency Modulation
PM	Phase Margin
PMOS	P Channel Metal Oxide Semiconductor
PS	Pulse Skip
PVT	Process-Voltage-Temperature
PWM	Pulse Width Modulation

SIDO	Single Inductor Double Output
SIMO	Single Inductor Multiple Output
SNFP	Slow NMOS - Fast PMOS
SPS	Segmented Power Stage
SRFF	Set Reset Flip Flop
SS	Slow NMOS - Slow PMOS
TYP	Typical Corner

1. INTRODUCTION

Buck converters have become the most common and one of the most critical design blocks in portable electronic systems based on the increasing demand in battery operated electronic systems in last decade. They are complex systems providing high efficiency voltage conversion. On the other hand, they extend the battery life by reducing heat losses. Buck converters provide a wide current range with high efficiency and very low output voltage ripple even if their input voltages change by more than two orders of magnitude. The main design challenge is to design a system which is flexible and efficient at the same time. To address that challenge, the main motivation of this work focuses on increasing the efficiency in buck converter systems by using adaptive techniques.

1.1. Principles of Buck Converter Operation

The buck converter is the single most common DC/DC voltage converter in use. It is also called step-down converter and converts an input voltage to a lower output voltage with high efficiency thanks to a switch and an inductor. The same function is also performed by other regulators such as LDO (Low Drop Out) regulators, but they consume the same amount of supply current with the load whereas buck converters draw less supply current than the output load. Figure 1.1 indicates a comparison between an LDO and an ideal buck converter.

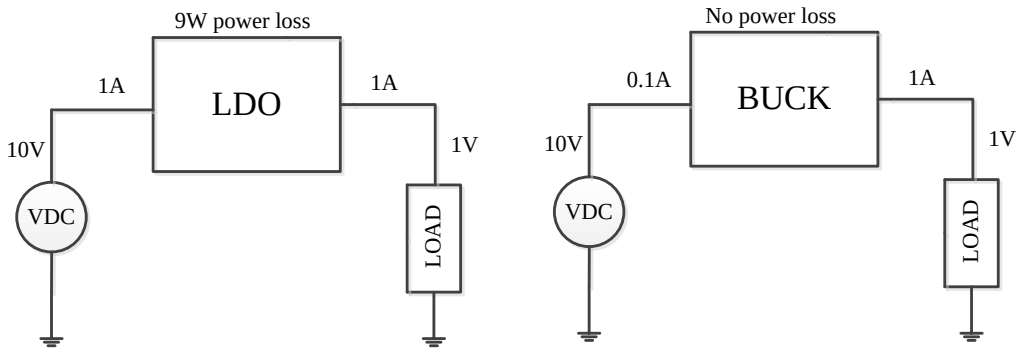

Figure 1.1. LDO vs buck converter.

The inductor element which is used in buck converters is the main element for achieving high efficiency in buck converters since it can store energy in its magnetic field. In other words, it can store current. Figure 1.2 demonstrates operation of an ideal buck converter [1].

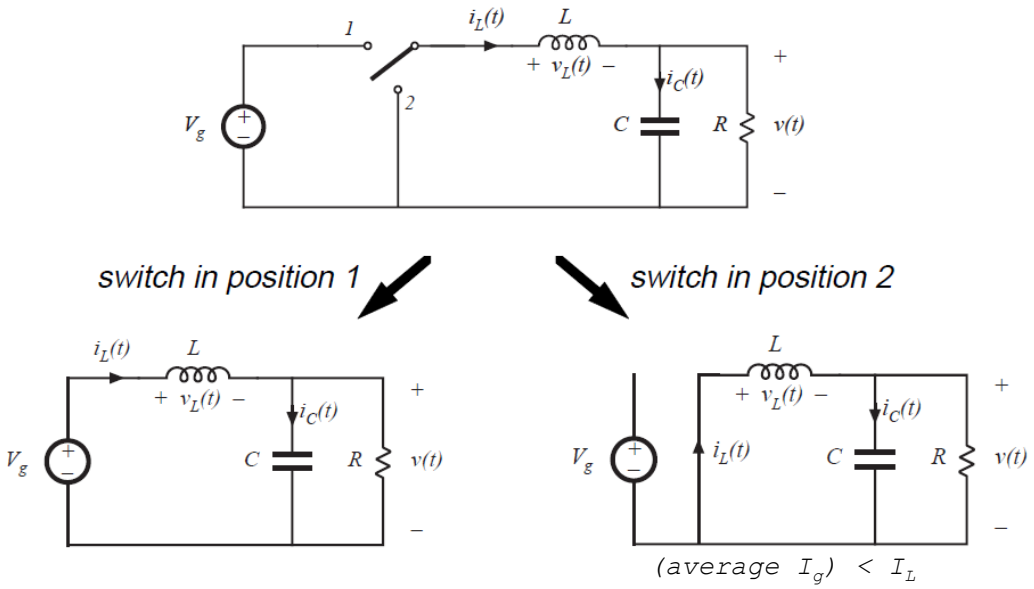

Figure 1.2. Ideal buck converter operation [1].

The buck converter system works in two switch positions. In case of switch position one, the inductance is connected to the input voltage source and drains a current I_L. This current passes through the inductor, charging the capacitor and sourcing the load. Inductance current linearly increases during this time. In the case of switch position two, the inductance is connected to the ground but it still continues to source the current to the load due to its nature. The stored inductor current in the previous switch position decreases linearly in this phase. In this phase, the average current from the source is less than the load current since input voltage source remains disconnected.

Figure 1.3 demonstrates the voltage drop on the inductor and current of inductor in time for the two phases which are mentioned above. The change in the inductor current by time is a function of voltage drop with the following equation:

$$V_L(t) = L\frac{di_L(t)}{dt} \tag{1.1}$$

Since I_L increases in switch position one and decreases by the same amount in switch position two, there is a relation between the input voltage and the output voltage given by:

$$0 = DV_g - (D + D')V \tag{1.2}$$

$$0 = DV_g - V \tag{1.3}$$

where D is the duty cycle which is the ratio of phase one to total switching period. Then, the Equation 1.2 leads to:

$$V = DV_g \tag{1.4}$$

When duty cycle is lower than one *(D < 1)*, the output voltage is less than input voltage which means that the step down converter operation is achieved.

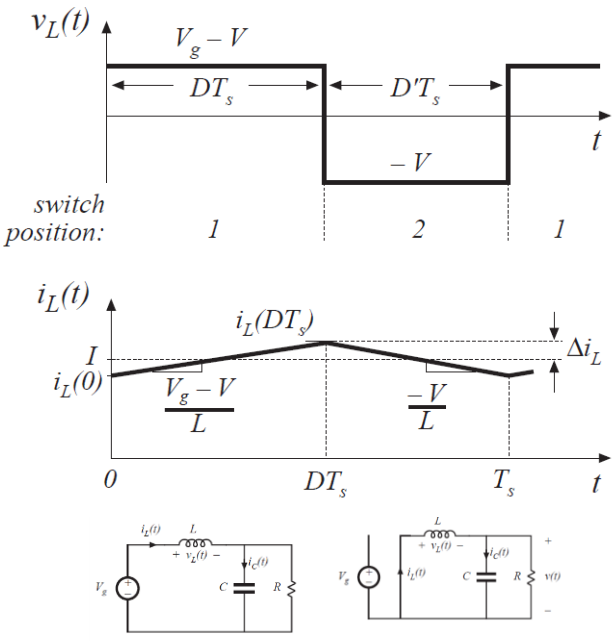

Figure 1.3. Voltage drop on inductor, inductor current and switch positions [1].

Buck converters are called “regulators” if the switches are implemented inside the chip and they are called “controllers” if the switches are used outside the chip. They are called “synchronous” if both switches are implemented using transistors and “asynchronous” if the bottom switch is implemented with a diode. In each of those categories, the buck converters are implemented and used with their own merits and drawbacks. However, synchronous buck regulators are the ones that yield a better efficiency than the others. Figure 1.4 demonstrates a typical example of synchronous buck regulator with CMOS implementation for the switches.

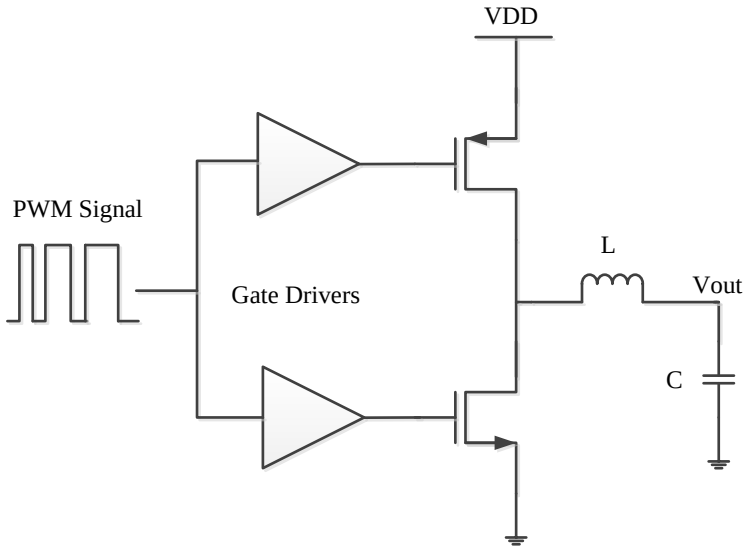

Figure 1.4. CMOS synchronous buck regulator.

In a CMOS synchronous buck regulator, the gates of the switch transistors are driven by a switching signal with a duty cycle *D*. This duty cycle is controlled by a control loop which tries to equalize the output voltage to a reference voltage. Two main control loop methods are voltage mode control and current mode control methods.

1.1.1. Voltage Mode Control

An error amplifier compares the buck output voltage with a reference voltage and generates an output error voltage called V_{err}. The V_{err} is fed into the input of PWM comparator. PWM comparator compares the V_{err} signal with a generated sawtooth signal

and generates a switching output which switches with a duty cycle *D*. Figure 1.5 demonstrates an example diagram for a voltage mode control loop and PWM output signal generation.

When the buck output voltage V_{out} is lower than the reference level, then V_{err} signal increases and PWM comparator generates a signal with increased duty cycle. The increasing in duty cycle results in an increase in output voltage V_{out} at the end.

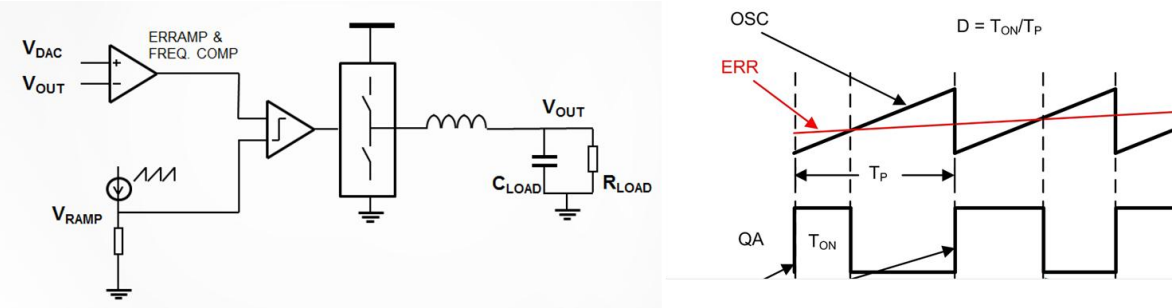

Figure 1.5. Voltage mode control loop and PWM comparator.

1.1.2. Current Mode Control

In current mode control, the feedback is taken from the output current, not the voltage [2]. An example diagram explaining current mode control is shown in Figure 1.6. An error amplifier again compares the output voltage V_{fb} to a reference voltage V_{ref} and generates a control current $I_{control}$. $I_{control}$ is compared to the output current I_{out} and PWM signal is generated as a result of this comparison. As it is drawn in Figure 1.6, whenever the I_L crosses the $I_{control}$, the PMOS switch turns off and it waits for the next clock signal edge to turn on. After it again turns on, I_L starts to increase.

Figure 1.6 is an example of "peak current mode control" since $I_{control}$ is compared to the peak value of inductor current. Other techniques are also possible such as average current control or valley current controls which simply compare the average of the inductor current or dip of the inductor current [3]. The feedback, in current mode control, is taken from the inductance in two ways. One is taking it with a series resistance with the inductor and the other is sensing the current from the switch transistors directly [4-6].

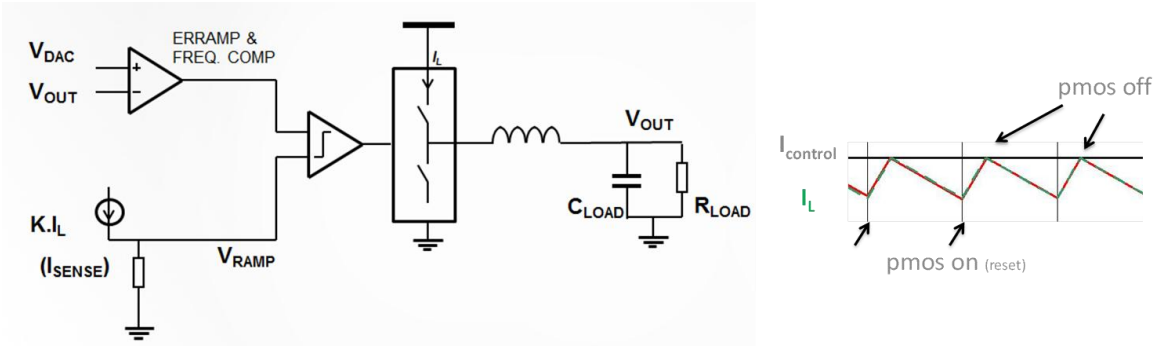

Figure 1.6. Current mode control and PWM generation.

There are benefits of current mode control over voltage mode control since; the current mode control (CMC) loop forces the peak current to be the same for each switch cycle. The other benefit is that the inductor together with the CMC loop behaves as a current source. In voltage-mode control, L and C_{out} forms a complex pole pair. Therefore, stabilization of voltage mode buck converters requires Type II, sometimes Type III compensation. CMC is simpler to stabilize from that point of view since it can be stabilized with Type I or Type II compensation. Additionally, power stages can be connected in parallel for higher power applications. In CMC, power stages can be forced to share the current equally. Finally, CMC is less sensitive to supply variations since there is automatic feed-forward from input voltage.

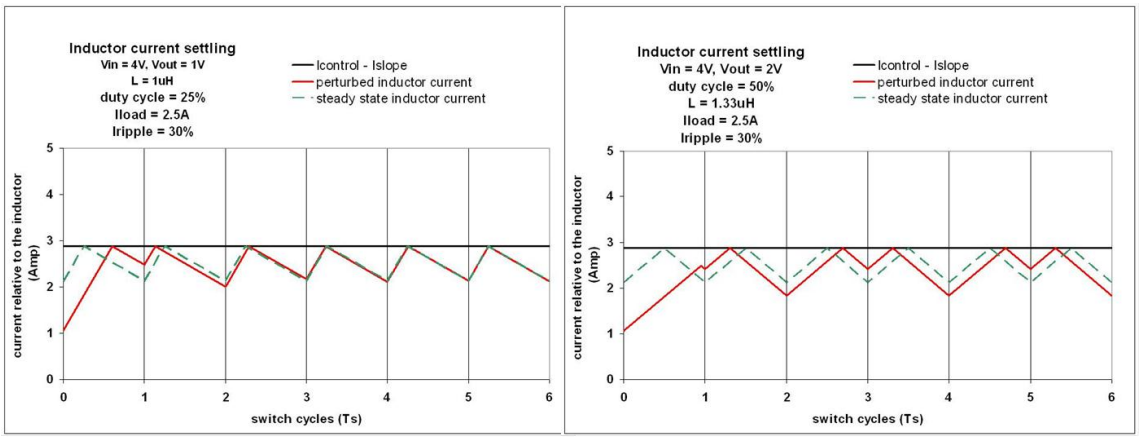

Figure 1.7. Inductor current perturbation response for different duty cycles [7].

Although there are several benefits of CMC over voltage mode control, a big problem arises in this control technique which is called sub-harmonic oscillation, as shown with Figure 1.7.

The problem fully depends on duty cycle *(D)*. When the duty cycle is less than *0.5* the problem does not appear, it only appears in duty cycles higher than *0.5*. The reasoning behind this is the following: when *D* is smaller than *0.5*, the rising slope of inductor current is more than the falling slope. Even if a perturbation is inserted to the inductor current; the perturbation can vanish in time. In the right hand side of the Figure 1.7, there is a case where *D* equals to *0.5* so that the rising and falling slopes of the inductor current are equal. In that case, any perturbation does not vanish in time. This problem is some kind of oscillation and output consists of some frequency components which are the sub harmonics of switching frequency (F_{SW}). Therefore, the problem is named "sub harmonic oscillation".

There is a solution to this problem called "Slope Compensation". In slope compensation method, a generated sawtooth signal is added to the control current ($I_{control}$) to equalize the difference of rising and falling slopes of $I_{control}$ - I_L. The timing diagram of currents and the implementation of slope compensation method are shown in Figure 1.8. There are extensive researches which try to optimize the methods and parameters in slope compensation [8-9].

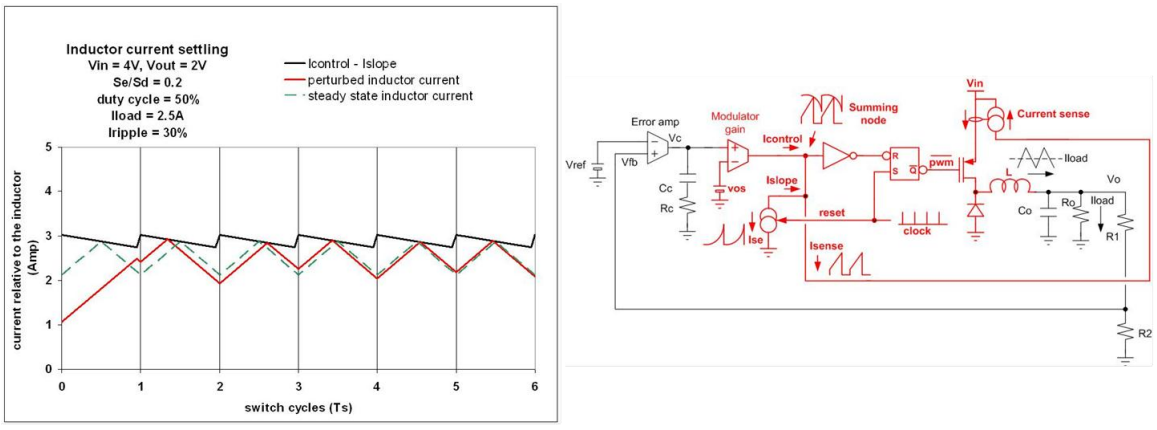

Figure 1.8. Slope compensation [7].

Other than voltage mode and current mode control, there are other complex control modes such as V^2 control [10], or hysteretic control [11-12]. However, voltage mode control is preferred for implementation in this work since it is the simplest to implement, it is not necessary to include the privileged features of current mode control or the other control methods to validate the idea of this work. The other reason to use voltage mode control instead of current mode control is that segmentation is used in the output stage of the adaptive buck converter so that one segment's sense current is enough to calculate the resistive power according to the equations. However, for current mode control, the total load current must be sensed for the control loop instead of only one segment's current. This would require additional summation blocks so that the complexity of this block is another issue for such a case.

1.1.3. Stability Analysis

Since there is a negative feedback loop system in buck converter designs, system stability is an issue to be taken care of. However, any AC analysis cannot be directly performed on the switching circuit. Either the traditional transient/pulse response method could be performed or the AC analysis is performed on the switching model of buck converter not the buck switching circuit itself. Numerous different techniques of the last decades are also proposed to perform stability check through AC analysis [13-15]. In voltage mode control scheme, the switching system has two poles at the resonant frequency of buck converter as:

$$f_{p1,2} = \frac{1}{2\pi\sqrt{LC}} \tag{1.5}$$

where L is the inductor and C is the output capacitor. The system has one zero as well from the Equivalent Series Resistance (ESR) of output capacitor as:

$$f_z = \frac{1}{2\pi C_{esr} C_{load}} \tag{1.6}$$

where the C_{esr} is the ESR resistance of the output capacitor and C_{load} is the output capacitor itself. Type II and Type III compensations are commonly used for stabilization of voltage mode control.

In the current mode control scheme, the system has a single dominant pole at:

$$f_{p1} = \frac{1}{2\pi}\left(\frac{1}{RC} + \frac{T_{SW}}{LC}(m_c D' - 0.5)\right) \tag{1.7}$$

where m_c is a parameter due to compensating slope. There are also two other non-dominant poles which are results of sub harmonic oscillation at:

$$f_{p2,3} = \frac{1}{2T_{SW}} \tag{1.8}$$

There is a zero due to the output capacitor same as the voltage mode case at:

$$f_z = \frac{1}{2\pi C_{esr} C_{load}} \tag{1.9}$$

where the C_{esr} is the ESR resistance of the output capacitor and C_{load} is the output capacitor itself. Thanks to the single dominant pole in CMC, Type I or Type II compensation is enough to stabilize current mode controlled buck converters.

1.1.4. Buck Converter Variations

There are multi-phase buck converter topologies in literature which incorporate multiple output stages and multiple inductors working with shifted phases. They all connect to the same output voltage of course [16]. The fundamental advantages of multi-phase buck converters are that they can provide increased output currents due to increased transistor sizes, they provide less output voltage ripple, and they provide more continuous current sink from the source because of shifted phases so that less electromagnetic interference (EMI) is obtained in such systems. A demonstration of an example of two

phase buck output stage and output current of different output phases versus time are depicted in Figure 1.9. The duty cycle of both phases is *50%* in the example.

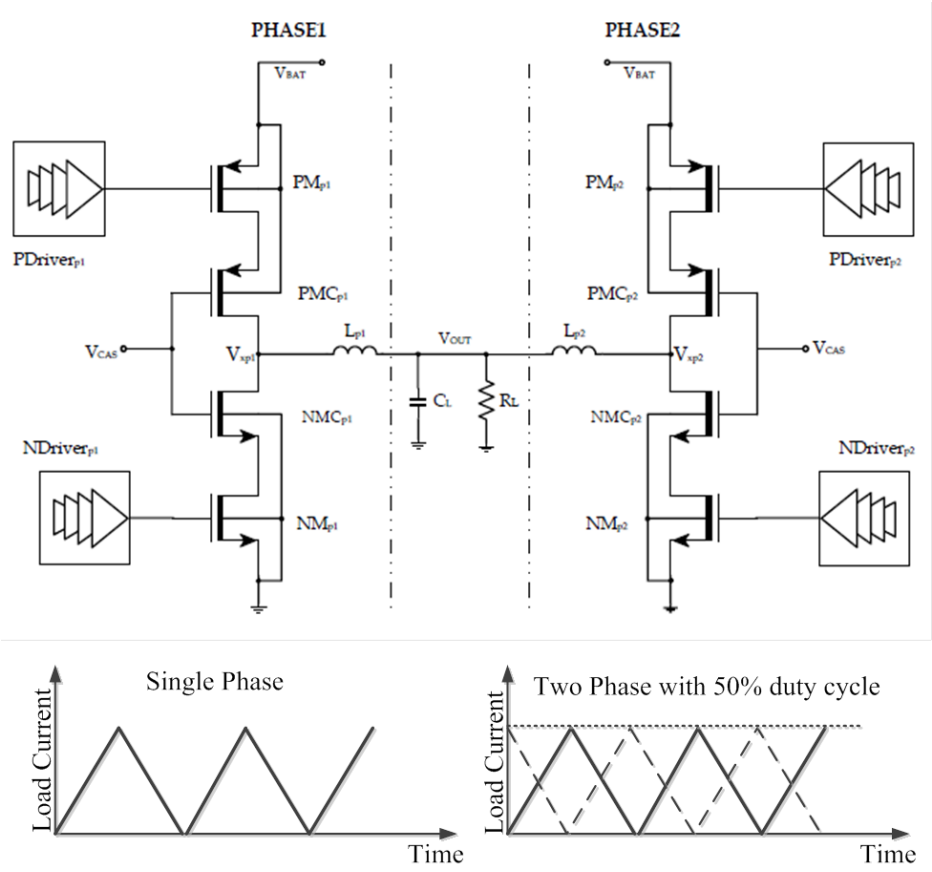

Figure 1.9. Two phase buck converter output stage and output current vs. time [16].

There are also other variations of buck converters such as single inductor double output (SIDO) or single inductor multiple outputs (SIMO). They use a single inductor and distribute the inductor current to multiple output nodes [17]. The control system is implemented digitally and it calculates time sharing of the inductor current switching for the different output nodes until the output nodes reach their target reference. In SIMO buck converters, all output voltage nodes may have different reference voltages and may sink different amount of load currents [17]. This feature defines the complexity of the control loop. Therefore, digital implementation is almost necessary. An example SIMO operation is given in Figure 1.10.

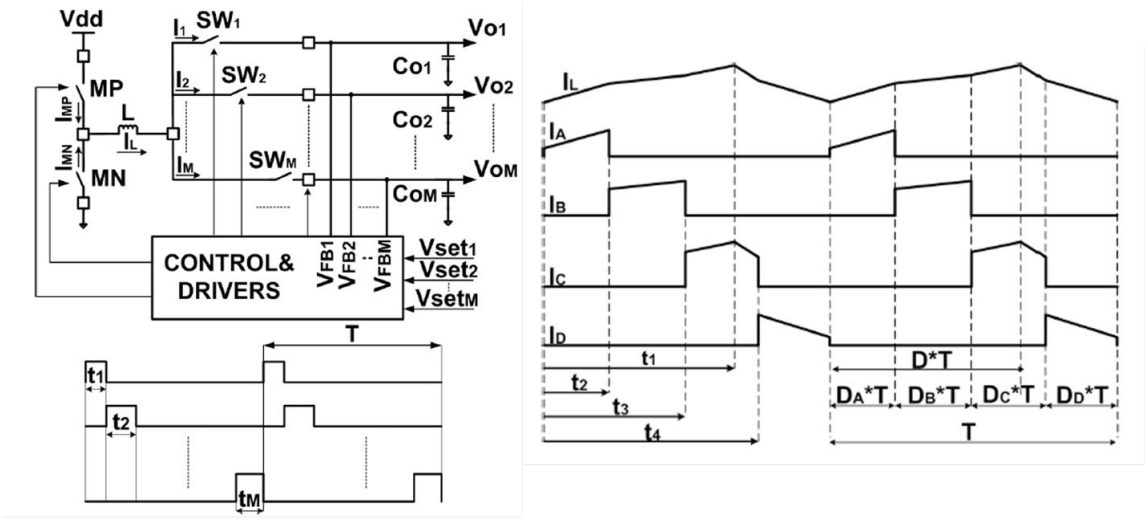

Figure 1.10. SIMO buck operation principle [17].

1.2. Previous Works on Efficiency Improvement

Buck converters are one of the fundamental design blocks in integrated power management ICs for battery powered devices since they are optimized to achieve the highest possible battery life, where the load current requirements include switching from *0A* to *40A* in a couple of microseconds. Those switching may not be known beforehand. So, the designed system has to be flexible and efficient at the same time. There are many works in the literature related to designing CMOS integrated circuits in order to sustain high efficiency over a wide load range.

Power losses are the main reasons for efficiency loss in a system. The mechanisms of power loss for a synchronous buck converter are indicated in Figure 1.11. Conduction losses dominate for high load operation. Thus, for higher efficiency in especially high loads, low R_{ON} MOSFETs and low resistance inductors are needed. Under light loads, the main loss mechanism is different and MOSFET switching and gate-drive losses become significant. Therefore, the efficiency decreases with decreasing load current. The light load efficiency is at least as important as heavy load efficiency since digital integrated circuits work mostly in the idle mode.

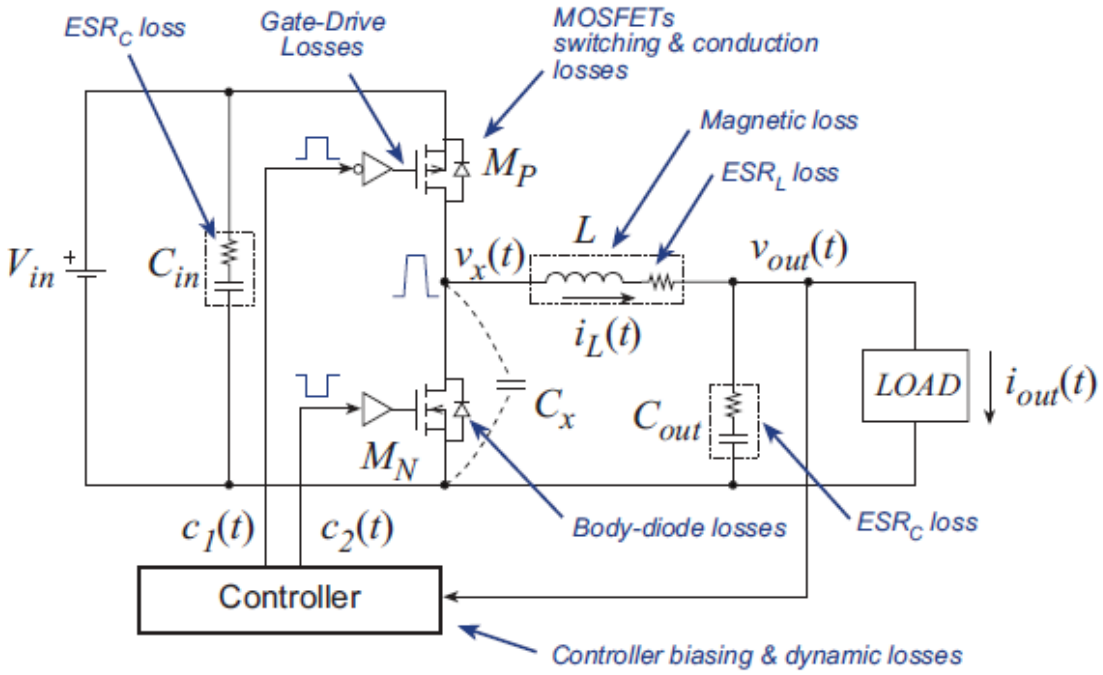

Figure 1.11. Mechanisms of power loss in a synchronous buck converter [7].

Over the years, many researches have been conducted to improve light load efficiency with some circuit and system level methods. Beside new design techniques, recent advances in power MOSFETs, integrated Schottky diodes, new magnetic materials to implement low resistance inductors and high density/low ESR capacitor designs are used for efficiency improvements.

As it has been mentioned before, there are extensive design methodologies for improving the efficiency for synchronous buck converters such as variable frequency, fixed frequency, and adaptive dead time techniques such that all of them create a base for this study.

1.2.1. Variable Frequency Techniques

The variable frequency techniques are commonly used in switching converters to mainly decrease the gate drive loss are the pulse frequency modulation (PFM), pulse skip, and burst mode control.

These techniques are quite useful; on the other hand, they generally cause poor output voltage regulation and electromagnetic interference (EMI) concerns because the load is dependent on the switching frequency.

1.2.1.1. Pulse Frequency Modulation (PFM). Pulse frequency modulation is the phenomenon that results in reducing the switching frequency at light loads to mitigate the switching and gate drive losses [18-27]. PFM mode is the most widely used method in fact; most commercially available low power DC/DC converters are capable of switching into PFM mode. The automatic switching with internal sensing mechanisms or external mode selection between different modes is possible [18-27]. The example of an operation diagram for PFM mode is given in Figure 1.12.

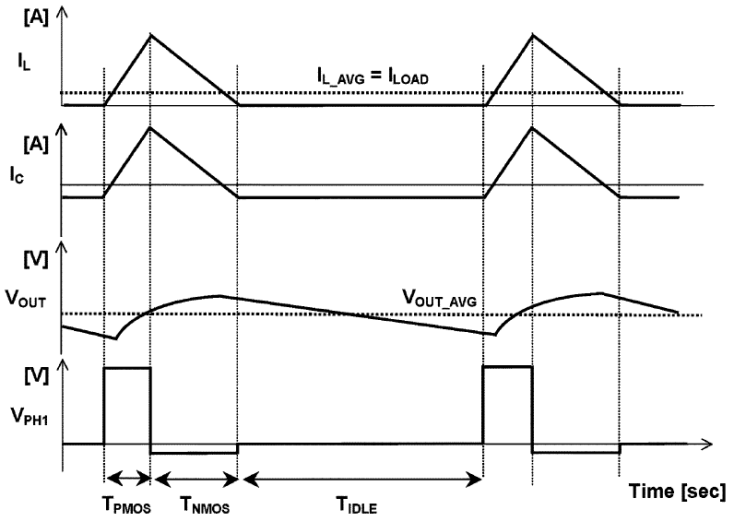

Figure 1.12. Pulse frequency modulation [21].

One of the techniques of output voltage regulation is to use a fixed on-time *(t_{on})* and automatically controlling off-time *(t_{off})*, such that output voltage reaches a set threshold value which is seen in Figure 1.12. Using a hysteretic approach, the PFM controller can be designed using only a single low power analog comparator and has been demonstrated with a current consumption as low as $4\mu A$ [22]. One other technique is generating t_{on} and t_{off} using power efficient delay lines [23].

1.2.1.2. Pulse Skip and Burst Mode Control. The Burst Mode (BM) and Pulse Skip Mode are variations of Pulse Frequency Modulation (PFM). Burst of pulses periodically introduces to the system to be able to charge the output capacitor and regulate the output voltage V_{out} in Burst Mode [28]. Burst mode operates with a fixed duty cycle pulse during the burst operation. It can also operate with programmed load current control. BM results in lower peak inductor current for the same load current and frequency. The burst time can be defined as total time for train of pulses (t_{burst}) which is shown in Figure 1.13, can be adjusted to optimize frequency.

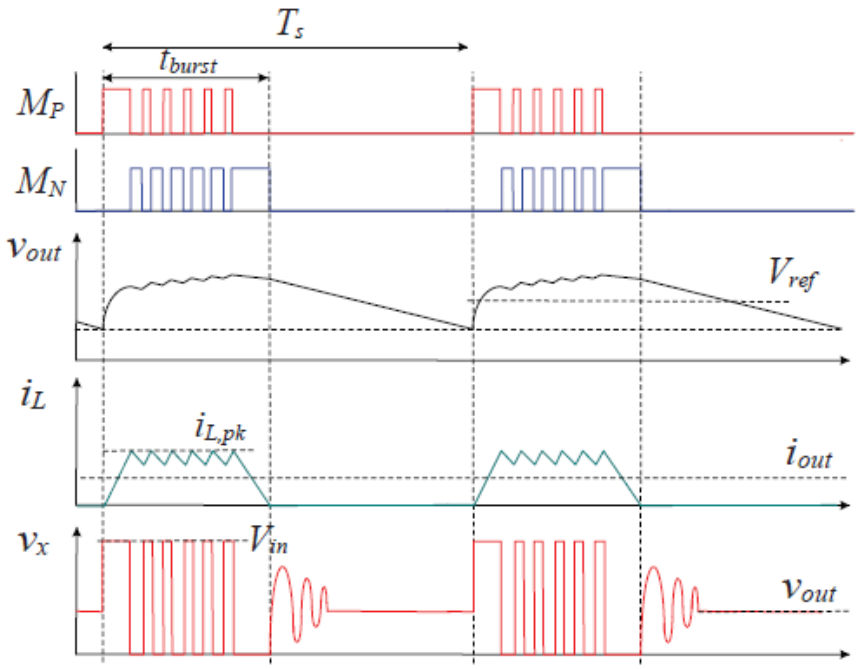

Figure 1.13. Burst mode control [7].

The other method is Pulse Skip technique which works with the principle of periodically skipping part of the switching signal while the loop continues its normal operation [29-30].

1.2.2. Fixed Frequency Techniques

Fixed frequency techniques are the techniques to reduce gate drive losses by using a fixed operation frequency such as adaptive gate swing, resonant gate driver, charge recycling, or segmented power stages.

1.2.2.1. Adaptive Gate Swing. Aim of this technique is to reduce gate drive losses by decreasing the gate drive voltage at light loads. The trade-off of decreasing the gate voltage is increased R_{ON} and increased circuit complexity [31-32]. The circuit that is driving the gate voltages is a controller basing its control mechanism to the load current [33-36]. Whenever there is light load condition, the gate drive voltage is decreased.

1.2.2.2. Resonant Gate Driver. Resonant gate drivers demonstrate more than 5% increase in efficiency over a wide load range utilizing the help of an inductor [36-48]. However, an additional inductor is used for this technique to resonate the gates and due to that inductor, temperature and process variations are significant. This is the drawback of resonant gate drivers.

1.2.2.3. Charge Recycling. Capacitor-based charge recycling (CCR) has been used for power reduction in various digital circuits and energy harvesting systems [49-51]. For the buck converters, the existing output capacitor C_{out} is proposed to use for charge recycling [52]. The ideal CCR architecture and ideal waveforms are indicated in Figure 1.14.

Using the CCR techniques, the overall efficiency improvement of a buck converter is up to *3-5%* for *100mA* load. Precise closed loop control of the timing in the charge recycling circuit is required to achieve reduction in gate driver losses by this technique. The control loop should take into account process, voltage and temperature (PVT) variations.

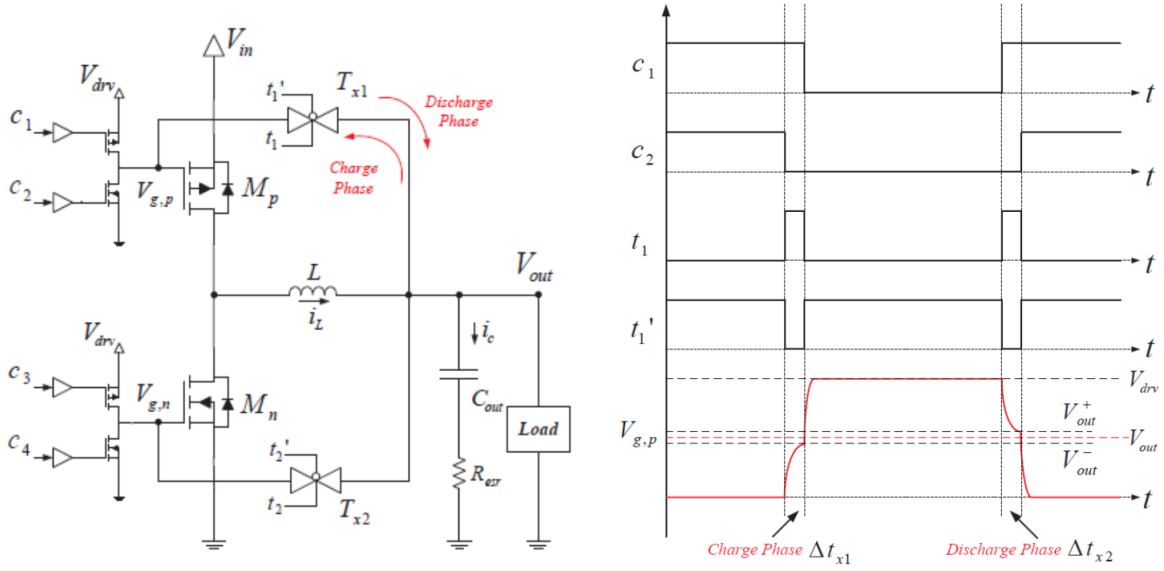

Figure 1.14. Charge recycling driver stage and waveforms [52].

1.2.2.4. Segmented Power Stage. The output stages of the switching converters consist of segments or fingers. Some portions of this segmented power stages (SPS) can be turned off at light load to optimize the trade-off between the effective gate capacitance and R_{ON} off pass devices. This is called "Switched-width" concept and was first proposed by [53] and then developed by [54-61] which includes analog and digital control loops. In all of the implementations which are mentioned in [53-61], the load currents are sensed and larger output devices are used according to the increasing load demand. The segments are created by separating the gate of the power MOSFETs in the layout. Figure 1.15 shows an example of a segmented output stage.

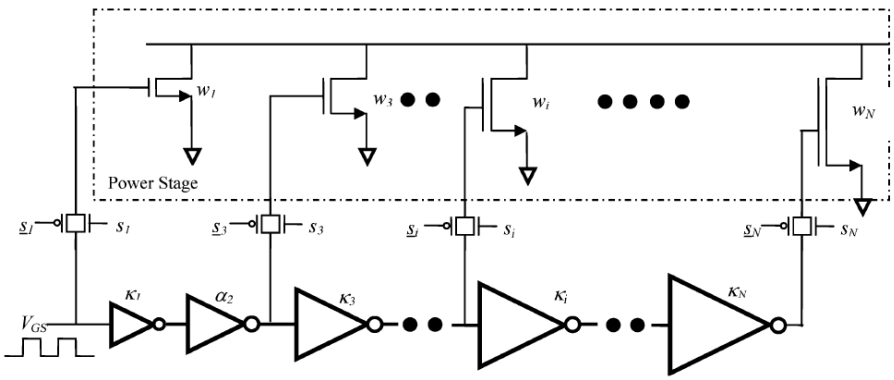

Figure 1.15. Segmented output stage example – NMOS section [54].

Segmented power stages can also include the gate drivers as well. The effective size and drive strength of gate drivers are adjusted for a fixed size power MOSFET [62-63]. The efficiency is even better with this one and it is also more suitable for applications with non-segmented discrete power transistors.

1.2.3. Adaptive Dead Time Techniques

The non-overlapping timing of output driver transistors is called “dead time” and excess dead time of output PMOS and NMOS leads to efficiency loss since the body diodes conduct during this time. The dead time minimization techniques have been proposed which utilize the adaptive techniques for timing optimization [64-73]. Thanks to the adaptive dead time techniques the overall efficiency is increased by *1-2%* additionally.

1.3. Proposed Work

The idea of this work is to use an adaptive output stage which decides on the active number of segments/fingers by comparing capacitive and resistive power losses on the output drivers. To be able to do that, it incorporates the input voltage, operating frequency, gate capacitance, actual R_{ON} information and the load current. It finds the optimal number of segments in all possible operating conditions.

According to the operation principle, first the capacitive power loss of a switching MOSFET with number of fingers (n_f) and assuming first order approximation given by the equation:

$$P_C = n_f C_{gg} f V_{DD}^2 \tag{1.10}$$

Resistive power loss of a MOSFET with number of fingers (n_f) and assuming first order approximation given by:

$$P_R = \frac{I_L^2 R_{ON}}{n_f} \tag{1.11}$$

where R_{ON} is the switch resistance and I_L is the drain current.

Figure 1.16 compares capacitive and resistive power loss of a typical buck driver transistor *(L=0.25µm)* for I_L*=100mA* and V_{DD} swept from *2.5V* to *5.5V* which is a typical supply voltage range for single-cell battery operated portable systems.

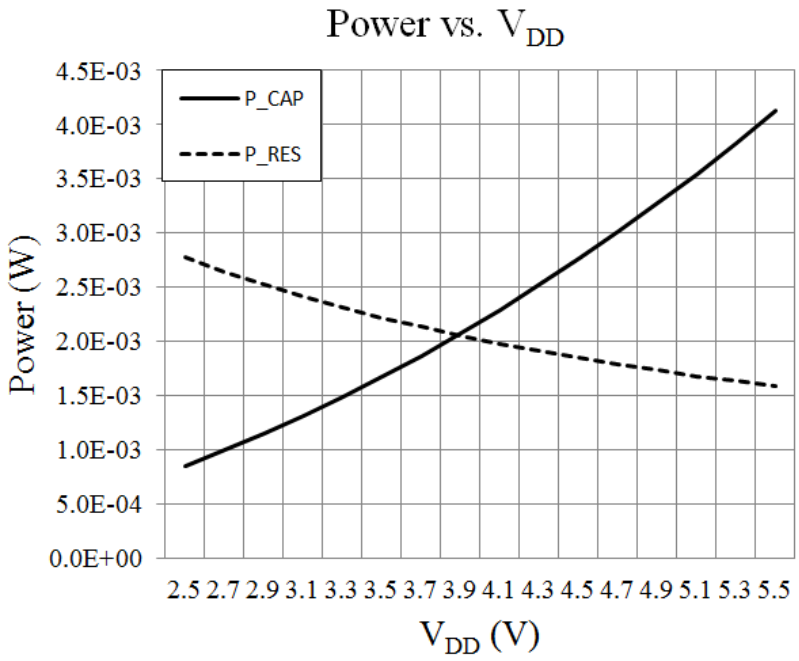

Figure 1.16. Capacitive and resistive power loss comparison.

The proposed adaptive output stage decides on active number of segments (fingers) by comparing capacitive and resistive power losses, and reaching optimum efficiency. For example, it increases the number of segments when load current (thus resistive loss) increases.

The proposed comparison procedure is as follows:

$$P_C <> P_R \tag{1.12}$$

$$n_f C_{gg} f V_{DD}^2 <> \frac{I_L^2 R_{ON}}{n_f} \tag{1.13}$$

Then, the V_C is defined such that:

$$V_C = \frac{I_R \Delta t}{C_{gg}} \tag{1.14}$$

to be implemented as the voltage of a capacitor C_{gg} charged by a reference current I_R (i.e. *100nA*) for a time frame of *t*. Also considering;

$$I_L \frac{R_{ON}}{n_f} = V_{sense} \tag{1.15}$$

where V_{sense} is the average voltage drop on the driver transistor drain and source terminals. Equation 1.13 now can be expressed as:

$$n_f \frac{I_R V_{DD}}{V_C} = \frac{I_L V_{sense}}{V_{DD}} \tag{1.16}$$

Then, the inductor current I_L can be defined as the current in one segment multiplied with the segment number as:

$$I_L = I_{seg} n_f \tag{1.17}$$

where I_{seg} is the current in one of the unit pass transistors.

If Equation 1.17 is inserted to the Equation 1.16, the following equation is obtained:

$$\frac{I_R V_{DD}}{V_C} = \frac{I_{seg} V_{sense}}{V_{DD}} \tag{1.18}$$

where I_R/V_C is to be implemented as an adaptive g_m block and V_{DD} as the input of this g_m block. Additionally, I_{seg}/V_{DD} is to be implemented as another adaptive g_m block and V_{sense} as the input of this g_m block.

As a summary, this work proposes a novel adaptive output stage size selection technique which will decide on the active number of output stage segments by comparing capacitive (switching) and resistive power losses; taking into account input supply voltage, operating frequency, gate capacitance, actual R_{ON} information, and load current, thus finding the optimal efficiency for the switching converter in all possible operating conditions compensating device variations due to aging, process, temperature, etc…[7].

Chapter 2 describes the system level design to realize the proposed work including all of the required block's definitions and specifications to be able to have a working adaptive output stage buck converter system.

Chapter 3 introduces the adaptive capacitive and adaptive resistive g_m blocks which are significant for realization of adaptive selection of output stages in buck converter.

Chapter 4 mentions about the control loop techniques and the design of loop components used in control loop design.

Chapter 5 includes design of all other necessary blocks to have a buck converter system including PWM comparator, ramp generator, V_{sense} sample and hold circuit, pre-driver and driver, current sense block.

Chapter 6 demonstrates the top level system simulation test bench and results. The comparison between this work and the other works in the literature is also done in this chapter.

Finally, Chapter 7 concludes this study and proposes future research directories.

2. SYSTEM LEVEL DESIGN

The proposed adaptive output stage buck converter technique is validated in a real simulation setup by building and simulating the adaptive output buck design which includes a voltage mode control loop given by Figure 2.1.

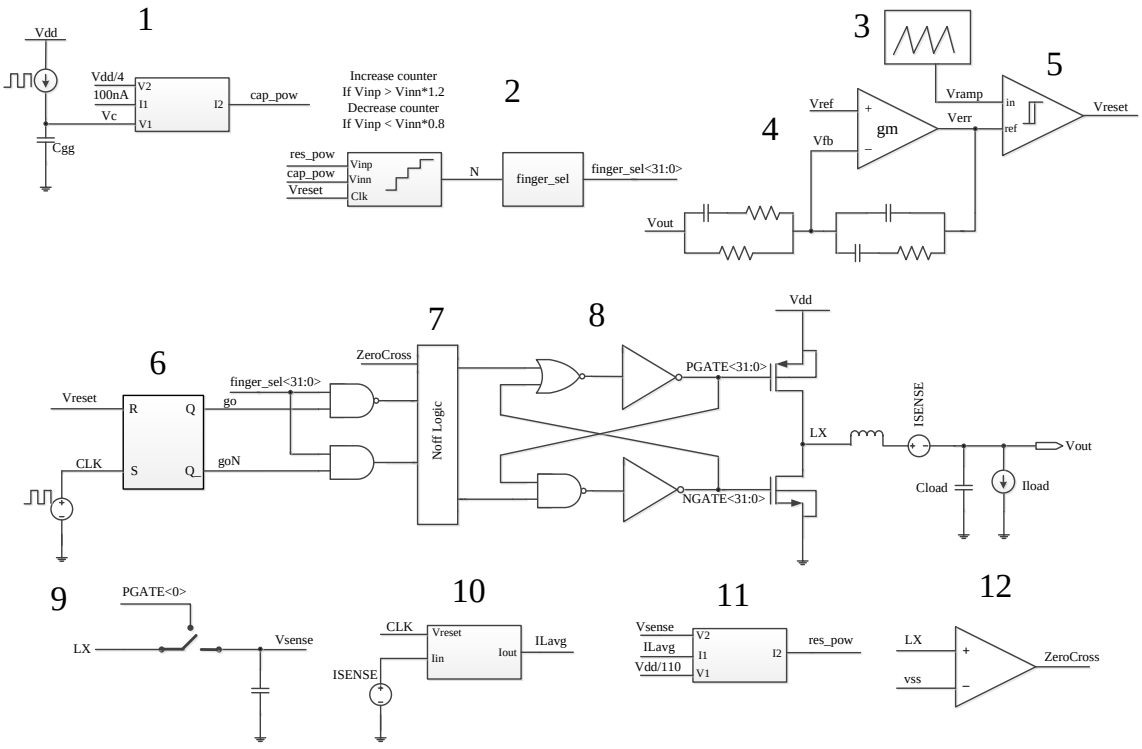

Figure 2.1. Adaptive output buck converter system model.

The system level setup is composed of an adaptive capacitive g_m block, a current comparator, a ramp generator, an error amplifier with its compensation network, a PWM latched comparator, a SR Flip Flop (SRFF), a N_{off} Logic, an adaptive stage pre-driver and driver, a V_{sense} sample and hold circuit, a current sense block, an adaptive resistive g_m block, and an active diode comparator.

Adaptive capacitive g_m block is shown in Figure 2.1 with the number one. It generates the capacitive current I_2. A current pulse of time duration t charges a PMOS capacitor C_{gg} which is half of the output stage PMOS device in terms of size and generates

the ΔV_2 input voltage of adaptive capacitive g_m block called V_C in Figure 2.1. ΔI_1 input of the adaptive g_m block is *100nA* fixed current such that g_m of the block is defined as I_1/V_C. The other voltage input of adaptive g_m block is *¼* of V_{DD} so, the output capacitive current I_2 equals to $V_{DD}I_1/4V_C$.

The current comparator is indicated in Figure 2.1 as the number two component. It is a comparator with hysteresis and counter inside it which compares resistive and capacitive power terms coming from the adaptive resistive and adaptive capacitive g_m blocks and decides the number of selected branches called *N*. This comparator is implemented with Verilog-A code and it is defined such that *N* will increase by one if resistive loss is *20%* more than capacitive loss and *N* will decrease by one if resistive loss is *20%* less than capacitive loss. This comparator can also be implemented in different ways.

The ramp generator is given as the number three in Figure 2.1. It is for creating the slope ramp to use it in the input of PWM comparator to compare it with error voltage to be able to create the PWM signal.

The error amplifier and the compensation network are shown in Figure 2.1 as the number four component. They are for creating the error voltage by comparing the output feedback voltage with a pre-set reference voltage. The compensation network is a Type III compensation which stabilizes the control loop.

PWM comparator is shown in Figure 2.1 as the number five component. It creates a "*Vreset"* signal which is a Pulse Width Modulation (PWM) signal and will be used for the drivers.

SRFF is the number six component in Figure 2.1 and it generates the duty cycle with inputs *"Vreset"* and *"clk"*.

N_{off} Logic is the number seven component in Figure 2.1. It is for creation of gate drive signals for PMOS and NMOS output drivers considering case of inductor current crosses *0A*. Basically, it inputs the "*ZeroCross*" digital signal and turns off the NMOS driver whenever the inductor current crosses zero.

Adaptive output stage pre-driver is shown in Figure 2.1 as the number eight component and non-overlapping signal generation for both pass devices is implemented together with finger selection logic.

V_{sense} sample and hold circuit is given as the number nine component in Figure 2.1. It senses the voltage drop on the PMOS driver circuit when the PMOS is on. The output of this block is given as V_{sense} in Equation 1.15.

The output current sense block is demonstrated as the number 10 component in Figure 2.1. It is implemented by monitoring the current on PMOS when it is on.

Adaptive resistive g_m block is given in Figure 2.1 as the number 11 component. It is implemented to obtain $g_m = I_1 / V_1$ such that I_1 equals to the output current of current sense block (I_{Lavg}) and ΔV_1 equals to a ratio of supply voltage which is $V_{DD} / 110$. The second input of adaptive resistive g_m block (ΔV_2) equals to the V_{sense} which is the voltage drop on the output driver PMOS transistor when it is on. Therefore, the output resistive current of this block ΔI_2 equals to $V_{sense} 110 I_{Lavg} / V_{DD}$.

The active diode comparator which is also known as zero cross comparator is shown in Figure 2.1 as the number 12 component and it detects the zero crossing of the inductor current and giving an output signal called "*ZeroCross*" whenever the inductor current crosses zero.

In reference to Figure 2.1, the sub blocks in the top level system model of the adaptive output buck converter are defined as explained above and also specified for the top level design concerns.

The specifications for each sub block are summarized in the following table [7]:

Table 2.1. Specifications for sub-blocks of adaptive output buck converter system.

Number of the component	Block Name	Specifications
1	Adaptive Capacitive g_m	g_m: 0.1µA/V – 0.5µA/V
2	Current Comparator with Hysteresis and Decoder	Input current: 250nA – 16µA Typical Hysteresis is %20
3	Ramp Generator	Ramp voltage is between 100mV and 1.8V Trimmability in ramp voltage levels Switching frequency is 3MHz
4	Error Amplifier	I_{DDQ} < 10µA 1σ input offset < 10mV Gain > 60dB Input Voltage Range < 1.5V
5	PWM Latching Comparator	t_{prop} < 20ns I_{DDQ} < 10µA 3σ input offset < 10mV Latching Functionality
6	RS Flip Flop	One with digital library is enough
7	N_{off} Logic	gatN signal must be off whenever the zeroCross signal is high
8	Adaptive Pre-driver Stage for Pass Devices	must consider non-overlapping timing
9	V_{sense} Sample & Hold Circuit	To be designed together with the resistive Adaptive g_m stage
10	Current Sense	To be designed together with output stage/pass devices
11	Adaptive Resistive g_m	g_m: 5µA/V – 35µA/V V_{in}: 10mV – 100mV
12	Active Diode	Typical t_{prop} < 20ns I_{DDQ} < 10µA 1σ input offset < 8mV Input Voltage Range ~ 0V Trimmable input offset is required

3. CIRCUIT DESIGN OF ADAPTIVE CAPACITIVE AND RESISTIVE GM

The proposed adaptive g_m technique can be utilized to generate arithmetic functions such as multiplication and division as it is stated in *US14695492* numbered patent "Method for an Adaptive Transconductance Cell Utilizing Arithmetic Operations" [74]. In adaptive output stage buck converter application, it is used to calculate the capacitive and resistive power losses of the switching converter so that they can be compared to find the optimum output stage size.

The block diagram of the proposed adaptive g_m topology is given in Figure 3.1. The transconductance cell g_{m1} on the left side has an input difference ΔV_1 and a forced output current ΔI_1. The loop which is formed by connecting the output of g_{m1} to the input of the bias cell determines the bias current of g_{m1} differential pair such that the g_m of the cell equals to $\Delta I_1 / \Delta V_1$. A second transconductance cell g_{m2} is also introduced to the system which has an input voltage ΔV_2. The same bias with the first cell is used in the second transconductance cell with identical input differential pair and similar device sizes. Thus, the output current produced at the output of the second stage becomes:

$$\Delta I_2 = g_{m1} \Delta V_2 = \frac{\Delta I_1}{\Delta V_1} \Delta V_2 \tag{3.1}$$

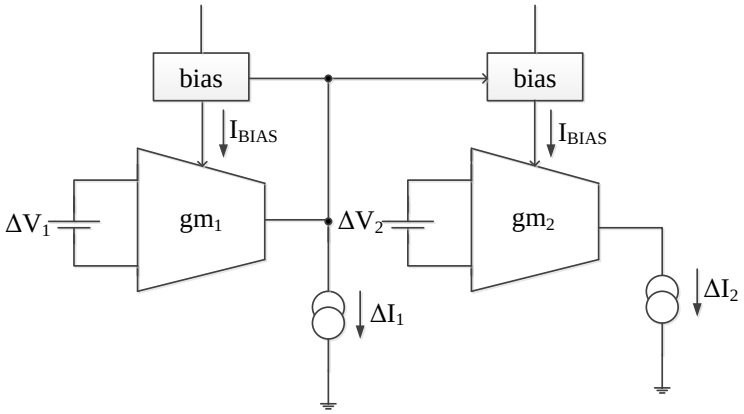

Figure 3.1. Adaptive transconductance circuit block diagram.

Transistor level implementation of the block diagram for the adaptive capacitive g_m cell case is given by Figure 3.2; the symmetric OTA on the left side of the schematic generates the bias loop forming $g_{m1} = \Delta I_1 / \Delta V_1$. The symmetric OTA on the right side of the schematic uses the bias of the first cell and having the input ΔV_2, generates the output current:

$$\Delta I_2 = \frac{\Delta I_1}{\Delta V_1} \Delta V_2 \tag{3.2}$$

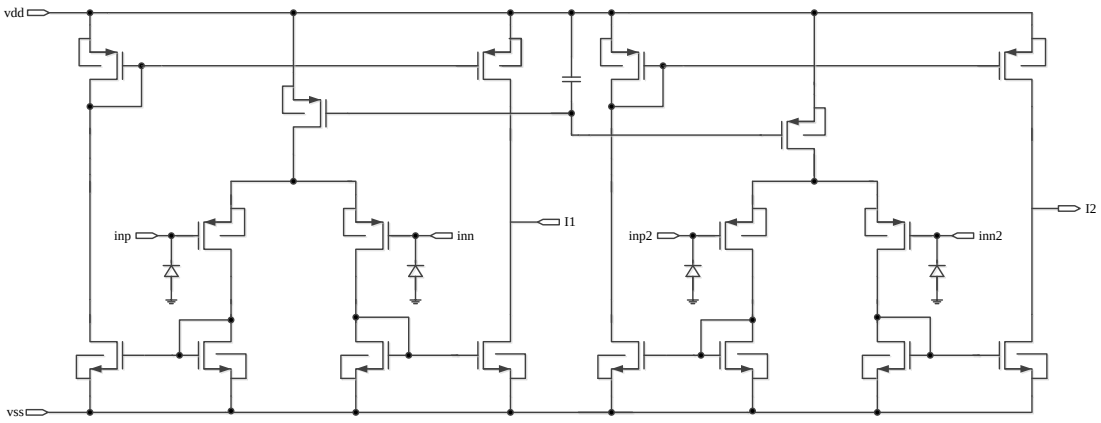

Figure 3.2. Schematic of adaptive capacitive g_m circuit.

The voltage inputs of the adaptive capacitive g_m cell are defined as ΔV_1= *(inp-inn)* and ΔV_2= *(inp2-inn2)* referring the Figure 3.2. ΔV_1 is connected to a PMOS capacitance which is a small replica of output PMOS unit driver to be able to sense its gate capacitance and ΔV_2 is connected to a fixed voltage reference which is a ratio of V_{DD}. This ratio will be called *M* from now on and it will be selected according to the operating points of the circuit. ΔI_1 is the current input for the symmetric OTA in the left hand side and its value is decided after some operating point analyses of the circuit considering efficiency, speed and quiescent current trade-off as *100nA*. According to those inputs, the equation becomes:

$$\Delta I_2 = \frac{100nA}{\Delta V_1} \frac{V_{DD}}{M} \tag{3.3}$$

To be able to set the unknown parameters in the equation, first thing that is taken care of is the operating point voltages of the inputs such that the ΔV_1 voltage in the one of the inputs of the adaptive capacitive g_m block is almost *0.8V* in the typical application since it must be higher than the threshold of PMOS capacitance that is used at the input. Because the PMOS capacitance varies *20%* with the process, *640mV – 960mV* range for the ΔV_1 must be covered. The circuit is adjusted such that a linear behaviour of the current is obtained in this *640mV – 960mV* voltage region. Other than ΔV_1, ΔV_2 is the second parameter that needs to be set. Since it equals to V_{DD} / M, the value of the M is set extracting the linear operation region of the adaptive capacitive g_m cell.

After the definition of the specifications, sizing the differential input transistors is the key step for the design. The g_m is defined by $\Delta I_1 / \Delta V_1$ so, the maximum possible g_m is *0.156μS* and the minimum possible g_m is *0.104μS* according to the ΔI_1 and ΔV_1 specifications. g_m is calculated with the equation in the following in saturation region:

$$g_m = 0.5 \mu_p C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \tag{3.4}$$

$\mu_p * C_{ox}$ is *27.44μS* in the process that is used during the design. For the saturation region the V_{ov} range for the saturation region is $0.25V < V_{ov} < 1.2V$. If it is inserted to the Equation 3.4 together with maximum and minimum values for g_m, the W / L range becomes $0.00526 < W / L < 0.182$. In the design, W / L is used as *0.0074* for the operation point concerns of the other devices in the design. To be able to have *0.0074* as W / L ratio, the length of the transistor must be *135μm* if the width is *1μm*. Such a ratio is not feasible to implement in layout. Therefore, ten series transistors with *13.5μm* length are used in layout implementation.

DC simulations are run to extract all the parameters. First simulation is for finding the linear region for ΔV_1. Figure 3.3 shows a comparison between the ΔI_2 current calculated with the equation and the ΔI_2 current extracted from the simulation for a given ΔV_1 range. The ideal ΔI_2 currents are shown with dotted lines and the extracted ΔI_2 currents are shown with solid lines in waveforms.

The reason of the discrepancy of plots for region where ΔV_1 is smaller than *350mV* between calculated ΔI_2 and simulated ΔI_2 is that the bias transistor with the given sizing cannot achieve the bias current for the required g_m. On the other hand, for region where ΔV_1 is greater than *1V*, the linearity of the input differential pair accounts for the discrepancy of plots meaning that the input transistors cannot work in saturation region anymore after *1V*.

The linearity of the capacitive current over input voltage variance is also measured under different supply voltage levels and the same linearity is achieved in the supply levels varying from *2.8V* to *4.8V*. Figure 3.5 indicates the behaviour of capacitive current over input voltage in different supply voltages. It is guaranteed that for the region that is desired DC simulation results are shown to be in line with Equation 3.2 where it is seen that $g_{m1} \sim 1/\Delta V_1$.

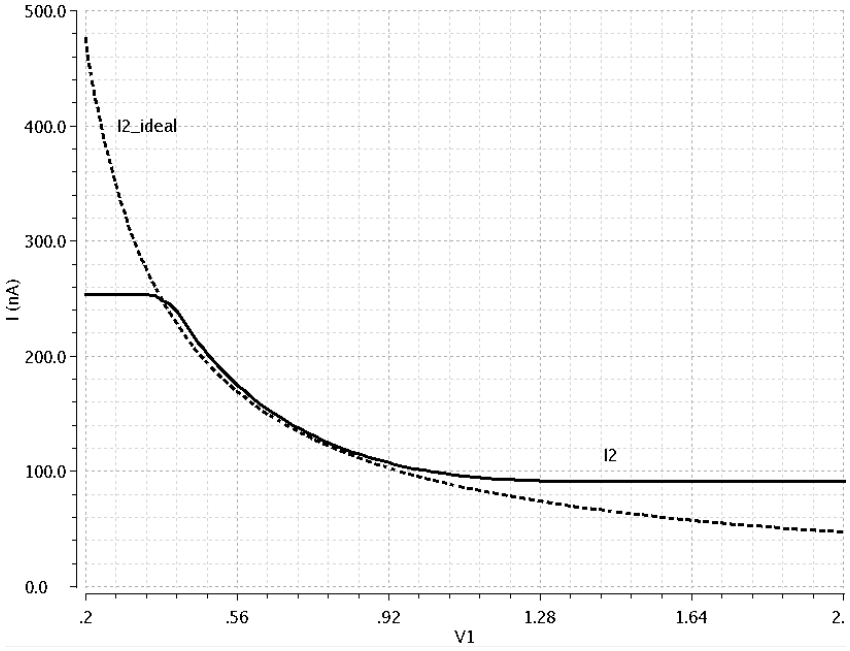

Figure 3.3. I_2 vs V_1 under typical conditions for adaptive capacitive g_m circuit.

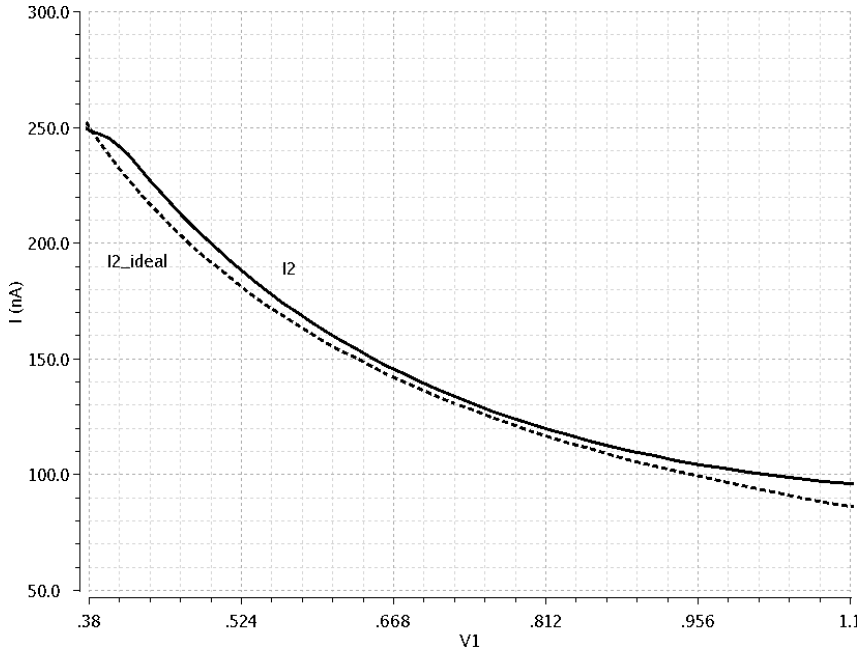

Figure 3.4. I_2 vs V_1 under typical conditions (zoomed into the linear region).

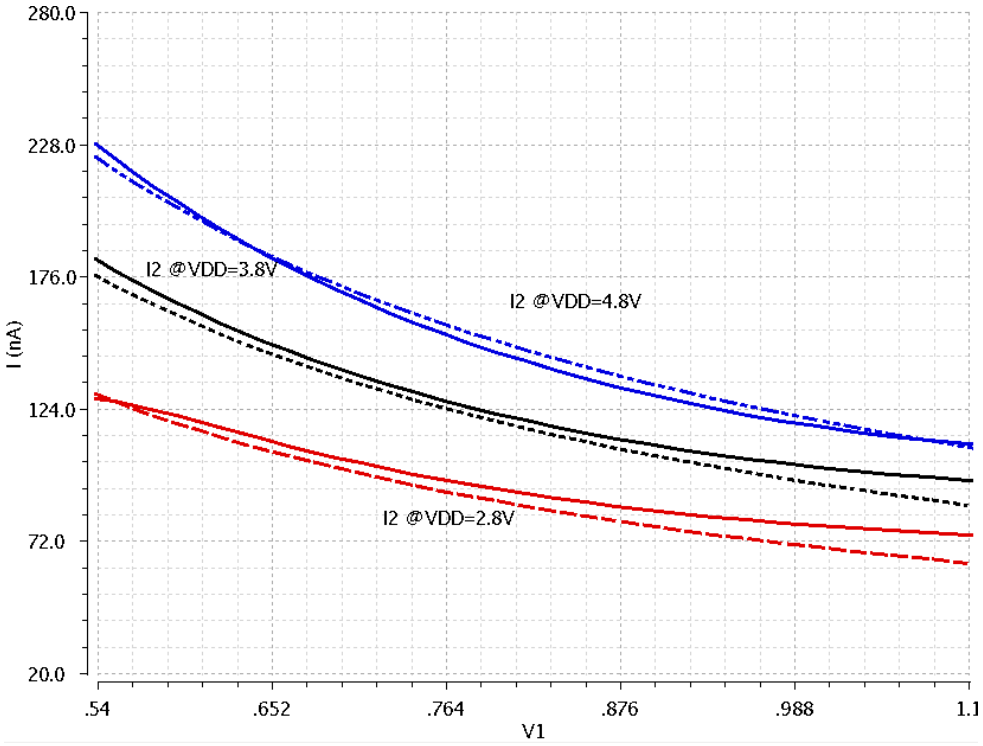

Figure 3.5. I_2 vs V_1 for various V_{DD} values for adaptive capacitive g_m circuit.

As it is mentioned before, the *M* value is the important parameter that must be set in the design. To be able to set it, the concern is finding the linear region of the other input voltage. In other words, the ΔV_2 input of the circuit works in the linear region when ΔV_1 that is set before works in the linear region as well. For that reason, the waveform in Figure 3.6 is extracted in simulations for three different input voltage values in ΔV_1 input as *640mV*, *800mV* and *960mV*.

Results show that the linear region of ΔV_2 is around *1V* because the ΔV_2 input corresponds to the V_{DD} / M value which is set in the beginning. The *M* factor is found as *4* for V_{DD} variance between *2.8V – 4.8V*.

The same simulation is run for typical *800mV* in the ΔV_1 input and various V_{DD} supply values between *2.8V* to *4.8V*. Results show that a clear linearity is achieved in capacitive current output (ΔI_2) until the *1V* in ΔV_2 input. The waveforms for V_{DD} sweep are shown in Figure 3.7.

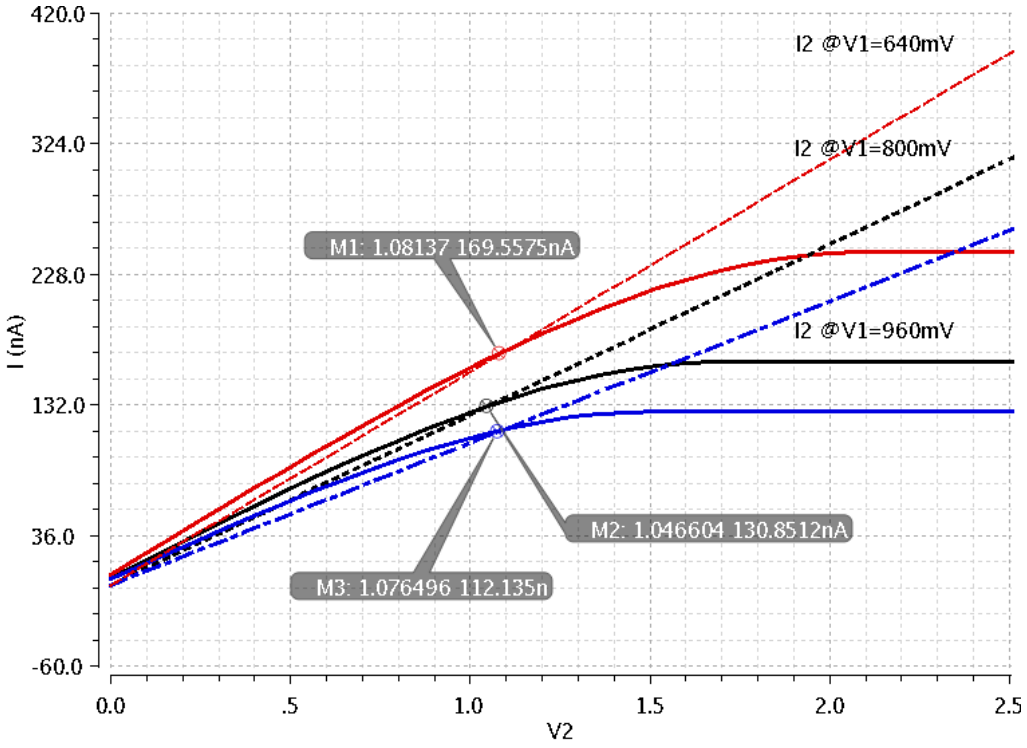

Figure 3.6. I_2 vs V_2 for various V_1 values for adaptive capacitive g_m circuit.

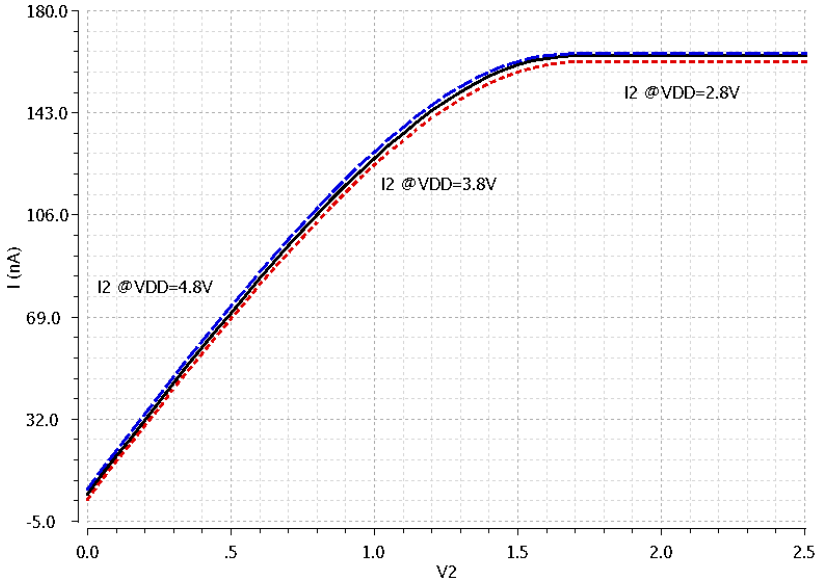

Figure 3.7. I_2 vs V_2 for various V_{DD} values for adaptive capacitive g_m circuit.

Transistor level implementation of the block diagram for the adaptive resistive g_m cell case is given in Figure 3.8; the symmetric OTA on the left side of the schematic generates the bias loop forming $g_{m1} = \Delta I_1 / \Delta V_1$. The symmetric OTA on the right side of the schematic uses the bias of the first cell and having the input ΔV_2, generates the output current:

$$\Delta I_2 = \frac{\Delta I_1}{\Delta V_1} \Delta V_2 \tag{3.5}$$

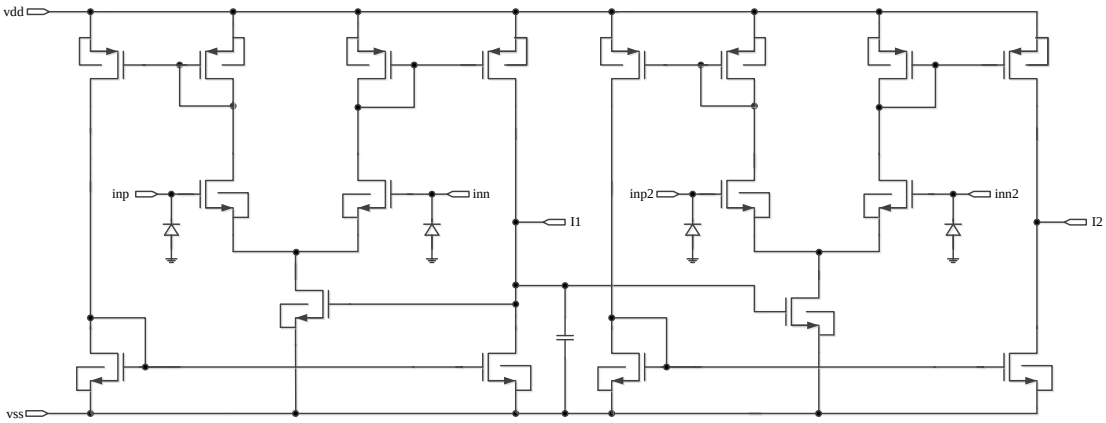

Figure 3.8. Schematic of adaptive resistive g_m circuit.

The specifications for the adaptive resistive g_m cell are derived together with the current sense block and driver circuit since the inputs to the circuit are generated by those blocks. The current input of the adaptive resistive g_m, ΔI_1 is the output of current sense block. Considering the maximum and minimum values for current per segment which are *10mA* and *31.25mA*, the output current of current sense block varies between *250nA* to *781.5nA* (since the current sense ratio is $I_{seg} / I_{sense} = 40K$) which is the specification for ΔI_1 input of adaptive resistive g_m block.

The other input ΔV_2 is the voltage drop on the PMOS output driver when it is on. Therefore, the range for ΔV_2 is defined by the R_{ON} of the PMOS transistor multiplies by the segment current flowing through the PMOS. The segment current varies between *10mA* and *31.25mA*, on the other hand, the R_{ON} of the PMOS varies by the change of supply voltage and the variation amount is between *1.41*Ω and *2.06*Ω. From those calculations, ΔV_2 variation is between *14mV* and *65mV*. This is the specification for second input voltage of adaptive resistive g_m circuit.

The third input is the ΔV_1 input of the block which is a fixed voltage reference and it can be defined as V_{DD} / M with a division ratio M like in adaptive capacitive g_m circuit. When it is inserted to the equation, new equation becomes:

$$\Delta I_2 = \frac{\Delta I_1 M}{V_{DD}} \Delta V_2 \tag{3.6}$$

The value of the M is defined by circuit operation conditions such that the circuit works more linearly when the two voltage inputs are as close to each other as possible. That is why, the M ratio is derived by equating $\Delta V1$ to $\Delta V2$, and it is found as *110*.

After definition of the specifications, sizing the differential input transistors is the key step for the design. The g_m is defined by $\Delta I_1 / \Delta V_1$ so, the maximum possible g_m is *31.2μS* and the minimum possible g_m is 5.68μS according to the ΔI_1 and ΔV_1 specifications. g_m is calculated with the equation in the following in saturation region:

$$g_m = 0.5\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2 \tag{3.7}$$

$\mu_n * C_{ox}$ is $54.88\mu S$ in the process that is used during the design for a given NMOS size. For the saturation region, the V_{ov} range is $0.25V < V_{ov} < 1.2V$. If it is inserted to the Equation 3.7 together with the maximum and minimum values for g_m, the W/L range becomes $0.15 < W/L < 18.5$. In design, W/L is used as 20 for the operation point concerns of the other devices in the design.

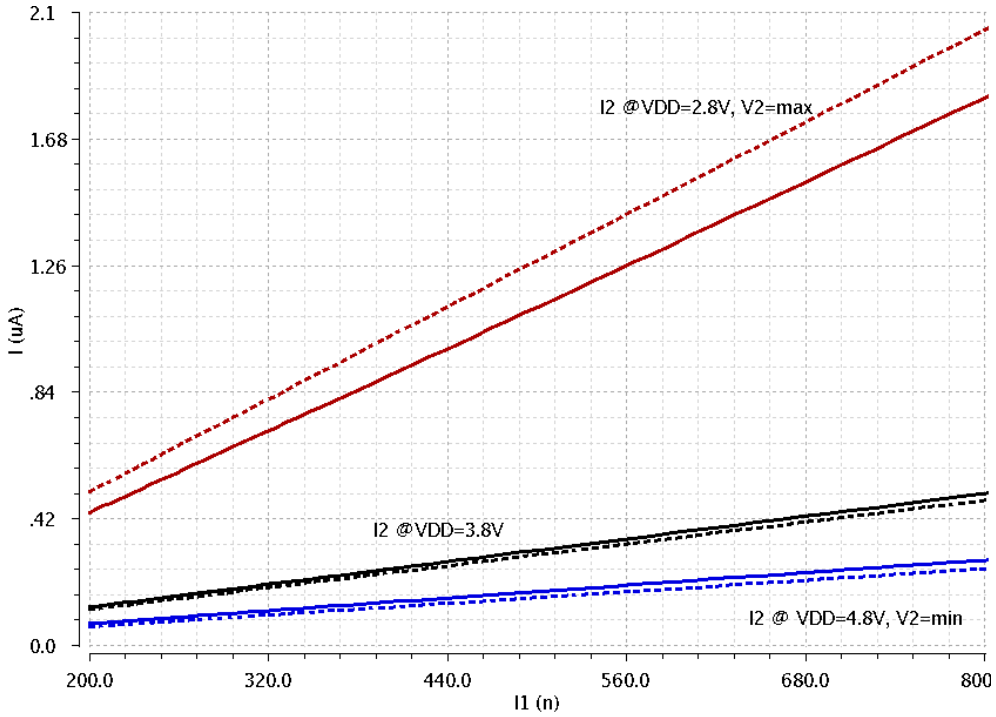

Figure 3.9. I_2 vs I_1 for various V_{DD} and V_2 values for adaptive resistive g_m circuit.

The simulation results show that the circuit is operational within the specifications. Figure 3.9 indicates the resistive output current behaviour over input current in various supply voltage and ΔV_2 inputs. Within the specified range for ΔI_1 input, the linear relation between ΔI_2 vs ΔI_1 can be seen in the Figure 3.9. Figure 3.10 shows the resistive output current behaviour over ΔV_2 input for various ΔI_1 input and V_{DD} values. Again, the linear relation between ΔI_2 vs ΔV_2 holds within the specification range. Figure 3.11 depicts the resistive output current behaviour over supply voltage in different ΔI_1 and ΔV_2 inputs. Inverse linear behaviour is observed in waveform as expected.

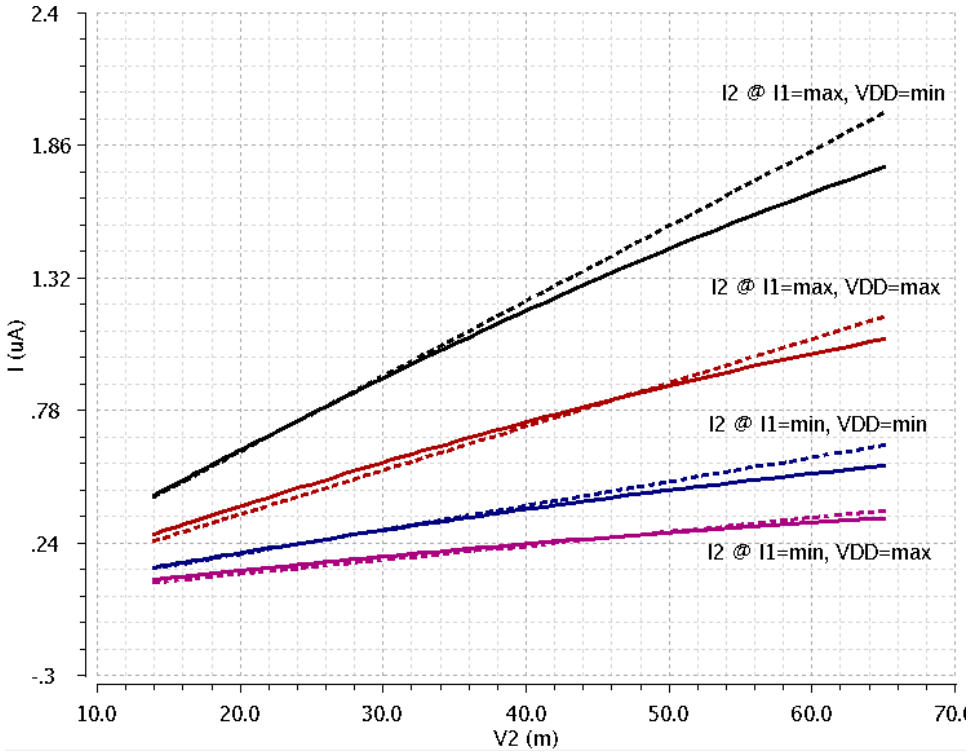

Figure 3.10. I_2 vs V_2 for various I_1 and V_{DD} values for adaptive resistive g_m circuit.

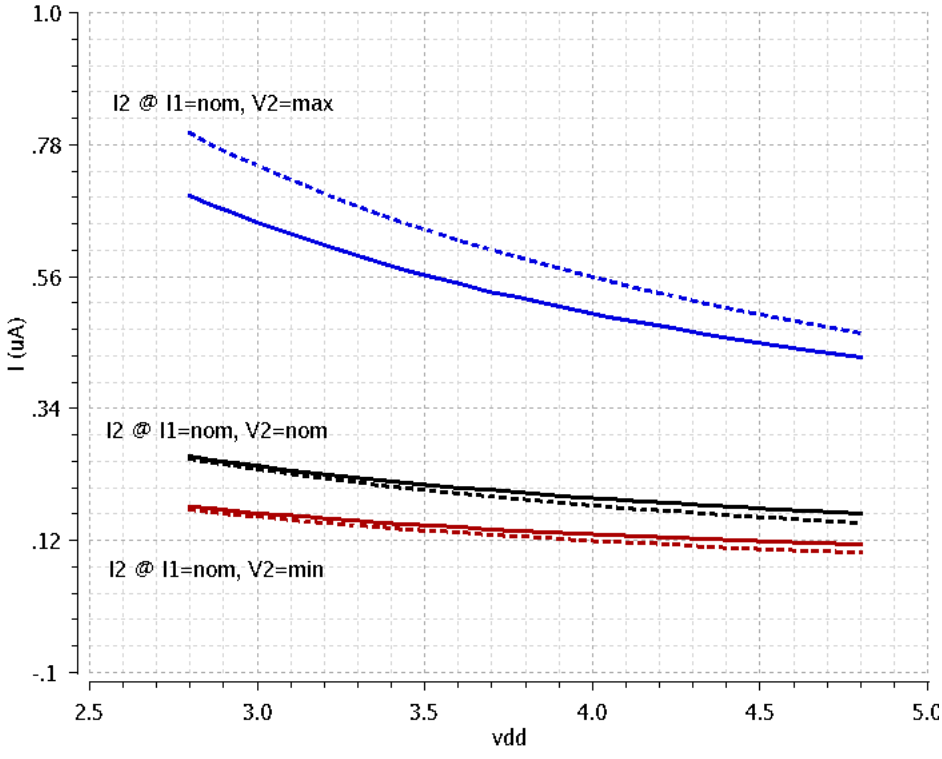

Figure 3.11. I_2 vs V_{DD} for various I_1 and V_2 values for adaptive resistive g_m circuit.

4. CIRCUIT DESIGN OF THE CONTROL LOOP

System level specifications of the error amplifier are an input range smaller than *1.5V* (V_{in} < *1.5V)*, a DC gain higher than *60dB*, *1σ* DC offset smaller than *10mV*, and the total supply current smaller than *10μA* (I_{DDQ} < *10μA)*. The schematic design of the error amplifier is shown in Figure 4.1. It consists of basic differential input stage and one stage NMOS amplifier. The compensation of the amplifier is done separately with Type III compensation so there is no compensation inside the error amplifier itself in the Figure 4.1.

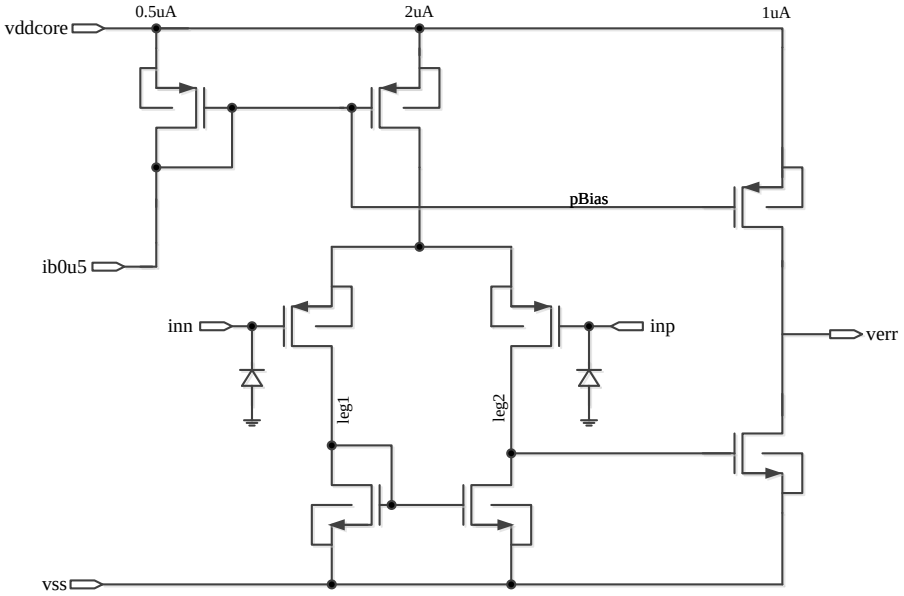

Figure 4.1. Schematic of the error amplifier.

A transient simulation setup is realized to check the functionality of the error amplifier and also to check the quiescent current consumptions when the amplifier is enabled and disabled. A DC simulation setup is realized to check the offset performance of the comparator and also the operating points.

Table 4.1 indicates a summary of measured specification parameters including corner cases.

Table 4.1. Summary of PVT simulation results of the error amplifier.

Expressions		Value	Corners			
			Supply Voltage (V)	active	Bias Current (nA)	Temp (°C)
I_{DDQ} (µA)	max	3.067	1.65	FF	525	70
	min	2.077	1.35	SS	475	0
	typ	2.652	1.5	TT	500	27
I_{DDQ_OFF} (pA)	max	1658	1.65	FF	525	70
	min	57.11	1.35	SS	475	0
	typ	118.9	1.5	TT	500	27
Input DC offset (µV)	typ	58	1.5	TT	500	27

A Monte Carlo simulation is also run to check the possible process and mismatch variations in the offset performance of comparator. The MC simulation is run in the typical corner by choosing the both process and mismatch options in simulator. The resultant histogram of the MC runs can be seen in Figure 4.2. According to the MC results, DC offset mean is *-451.46µV* and *1σ* standard deviation is *4.93mV* which is below the *10mV* specification.

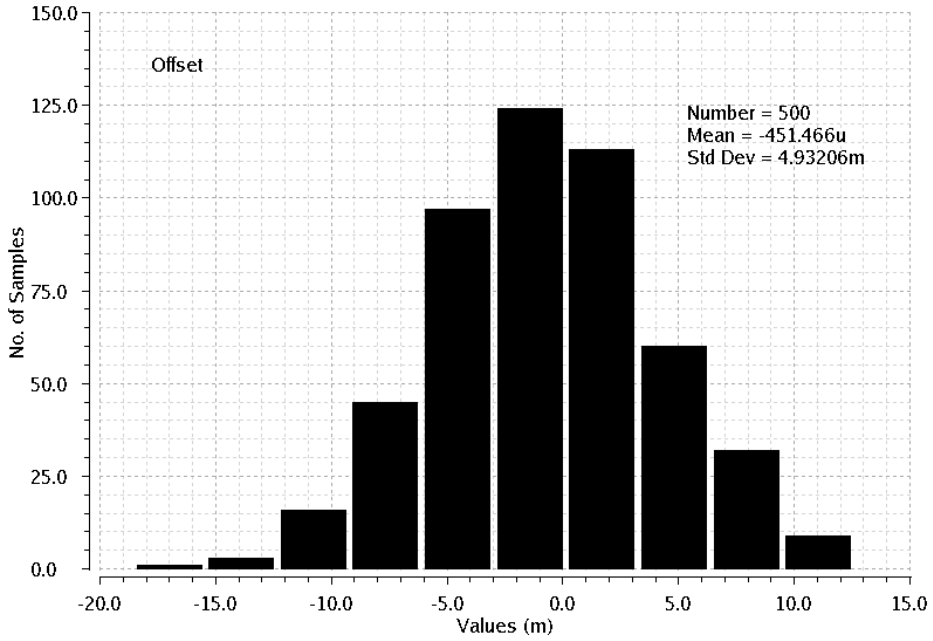

Figure 4.2. MC simulation results of DC offset.

Since buck converters are negative feedback closed loop systems, there is a need for a compensation network which closes the loop and stabilizes the system [75]. The basic blocks contributing to the closed loop system are the modulator, output filter and the compensation network itself which is shown in Figure 4.3.

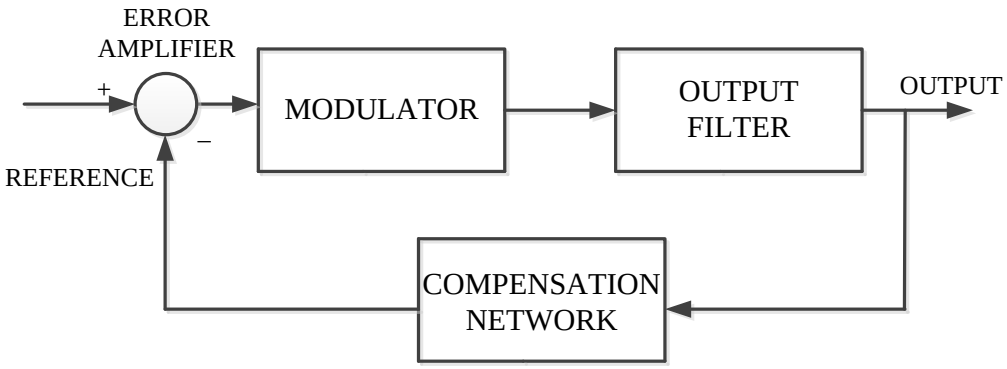

Figure 4.3. Basic building blocks of the buck converter.

The system without the compensation network is an open loop system and its gain is defined in the following equation:

$$GAIN_{OPENLOOP} = GAIN_{MODULATOR} GAIN_{FILTER} \tag{4.1}$$

$$GAIN_{OPENLOOP} = \frac{V_{in}}{\Delta V_{OSC}} \frac{1 + sC_{esr}C_{load}}{1 + s(C_{esr} + R_{ind})C_{load} + s^2 L_{coil}C_{load}} \tag{4.2}$$

where the V_{in} is the input voltage of buck converter, ΔV_{OSC} is the peak to peak voltage of the oscillator, C_{load} is the output capacitor, C_{esr} is the Equivalent Series resistance (ESR) of the output capacitor, L_{coil} is the output inductor and R_{ind} is the DC resistance of the output inductor.

According to the transfer function of open loop, it shows a double pole of an output filter and also a single zero which is a function of ESR of output capacitor and itself. An open loop system gain plot of a buck converter is indicated in Figure 4.4. Due to the double pole at the resonant frequency of filter, the Phase Margin (PM) is almost $0°$ which results in an unstable system. Another disadvantage is that the resonant frequency changes

with variations in output capacitor and the inductor. This variation is unwanted since it changes the PM corner to corner a lot. Predictable bandwidth and unconditional stability are required for switching converter systems. Therefore, a compensation network needs to be designed with gain roll-off at slope of *-20dB/decade*, crossing *0dB* at the desired bandwidth (BW) and a Phase Margin greater than *45°* [75]. For synchronous or non-synchronous buck converters, the bandwidth should be between two times resonant frequency and *0.1* times switching frequency [76]. Therefore, the gain bandwidth is designed such that it is always between *70kHz* and *300kHz* since the resonant frequency is *35kHz* and switching frequency is *3MHz*.

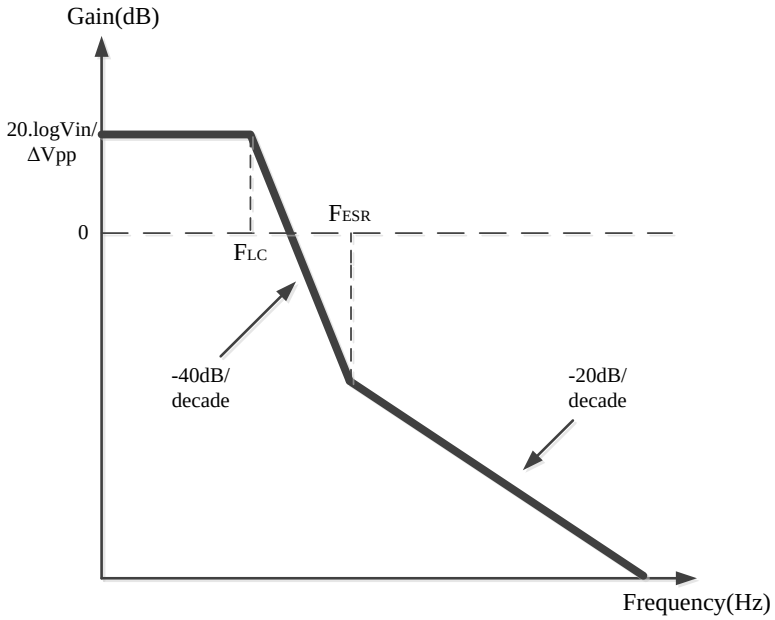

Figure 4.4. Open loop system gain.

A usual Type III compensation network is applied to the switching buck converter. According to the Type III compensation which is shown in Figure 4.7, the compensation gain is the following:

$$GAIN_{TypeIII} = \frac{R_1 + R_3}{R_1 R_3 C_1} \frac{(s + \frac{1}{R_2 C_2})(s + \frac{1}{(R_1 + R_3)C_3})}{s.(s + \frac{C_1 + C_2}{R_2 C_1 C_2})(s + \frac{1}{R_3 C_3})} \tag{4.3}$$

As it is seen from graph in Figure 4.5, the Type III compensation utilizes two zeroes to give phase boost of *180°*. This is *90°* for Type II compensated networks and *90°* phase boost is not always enough to remove the effects of output filter of buck converter which has double pole [75].

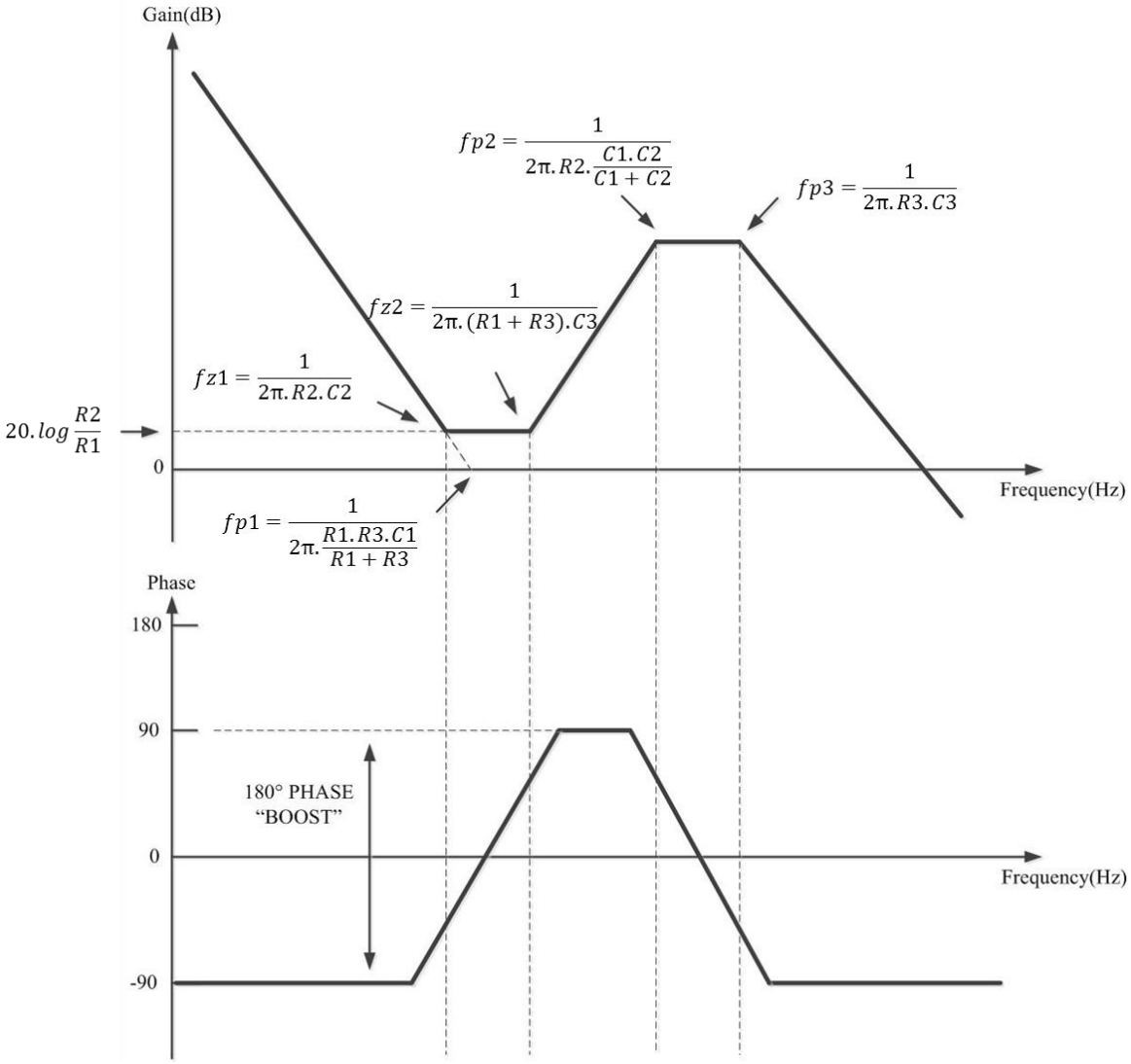

Figure 4.5. Generic type III network - gain and phase.

For the design of a Type III network, the system level equation includes the buck converter gain equation as well. The equation of the system gain for the buck converter is the following:

$$GAIN_{System} = \frac{R_1+R_3}{R_1R_3C_1}\frac{(s+\frac{1}{R_2C_2})(s+\frac{1}{(R_1+R_3)C_3})}{s(s+\frac{C_1+C_2}{R_2C_1C_2})(s+\frac{1}{R_3C_3})}\frac{V_{in}}{\Delta V_{OSC}}\frac{1+sC_{esr}C_{load}}{1+s(C_{esr}+R_{ind})C_{load}+s^2L_{coil}C_{load}} \quad (4.4)$$

During the design, the first pole is placed to the origin for DC regulation. Then, the first zero is placed just before the resonant frequency. It was *0.5* times the resonant frequency. After that, the second zero is placed at the exact resonant frequency. After that poles must be placed according to Figure 4.6, so that the second one is placed at the ESR zero. Therefore, it can cancel the effect of zero of the filter. Finally, the third pole is placed at half switching frequency [75-76].

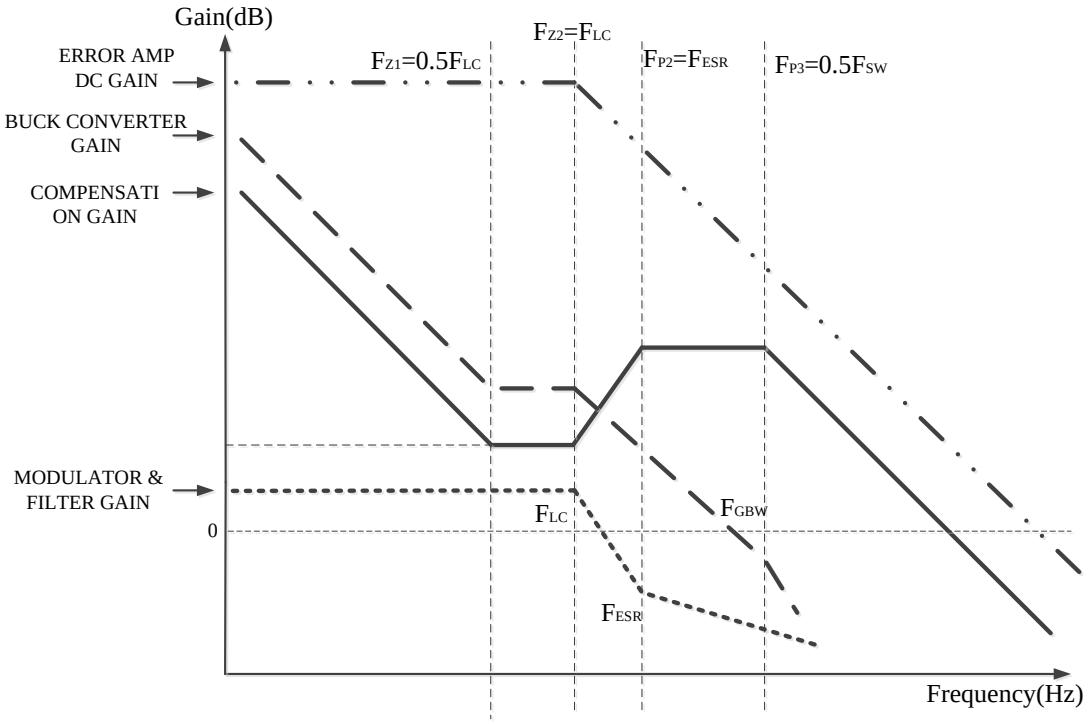

Figure 4.6. Type III compensated network.

For the design of the compensation network, a system model is realized including the error amplifier, a switching model and a Type III compensation network. A switching model for the buck converter needs to be designed since the actual circuit is not a linear circuit and AC analyses cannot be run for a nonlinear circuit. It basically uses linear

equations to model the switching state of the buck converter and it takes the error amplifier output, input voltage, number of segments (*N*) as inputs and calculates duty cycle (*D*) and outputs the output voltage of buck. The reason to include *N* as parameter is that the output stage of buck converter changes adaptively according to the load current for the idea of adaptive buck converter and the output impedance changes for different load demands as well. Therefore, *N* input is for making sure that the R_{ON} changes according to the load current. Figure 4.7 indicates the system AC model of adaptive buck converter. The AC loop break is used in the loop to be able to break it. The capacitors in the implementation are MIMCAPs. They are used in implementation rather than using the MOSCAPs to obtain less parasitic and due to the area concerns. MIMCAPs can be put above everything else in layout because of their high metal levels.

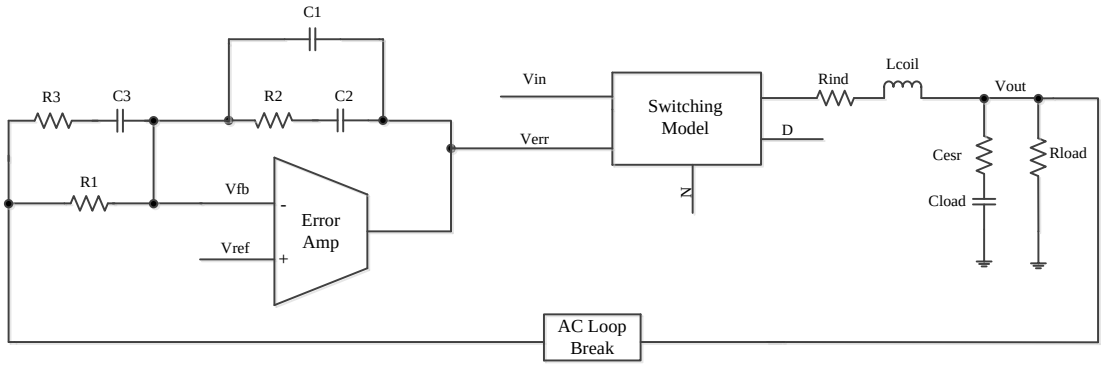

Figure 4.7. Type III compensation and system model of buck converter.

During the simulations, the DC gain, phase margin, gain margin, gain bandwidth frequency parameters are measured. Table 4.2 shows a summary of results and Figure 4.8 shows the gain and phase for typical corner case.

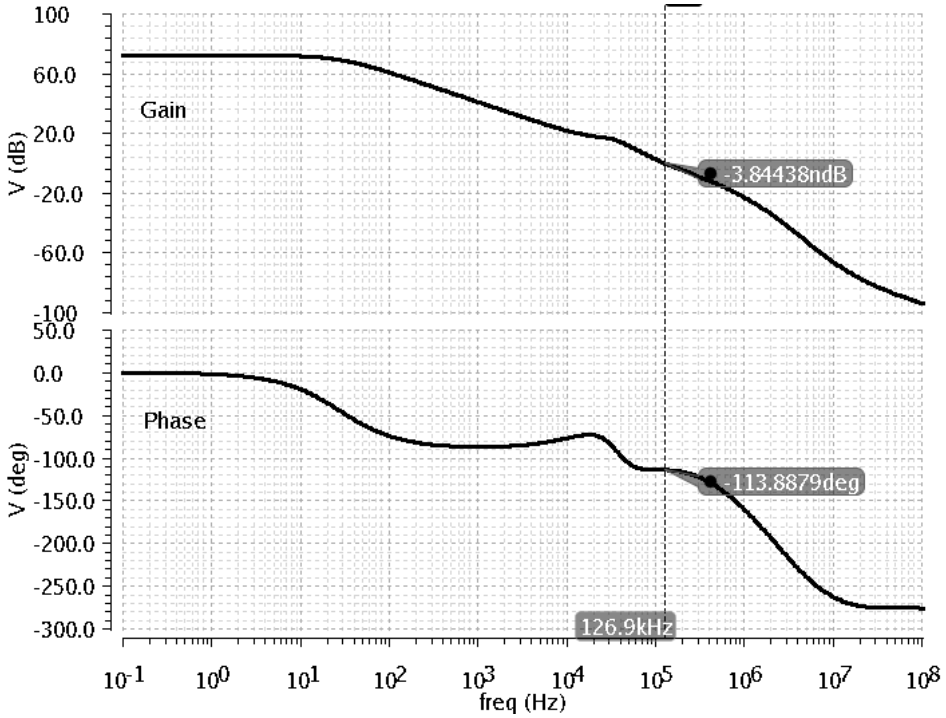

Figure 4.8. Gain and phase of the system in typical corner.

Table 4.2. Summary of PVT simulation results of AC model.

Expressions		Value	Corners								
			V_{in} (V)	V_{ref} (V)	vddcore (V)	C_{load} (µF)	C_{esr} (mΩ)	R_{ind} (mΩ)	active	passive	Temp (°C)
PM (dB)	max	78.22	2.8	1.2	1.65	25	10	40	SS	HIGH	0
	min	28.8	4.8	1.2	1.35	15	1	40	SNFP	HIGH	70
	typ	66.12	3.8	1	1.5	20	5	50	TT	NOM	27
GM (dB)	max	37.2	2.8	0.9	1.65	25	10	40	FF	LOW	70
	min	40m	4.8	1.2	1.35	25	1	60	SS	LOW	70
	typ	28.96	3.8	1	1.5	20	5	50	TT	NOM	27
F_{GBW} (kHz)	max	284.5	4.8	1.2	1.35	15	10	40	FNSP	HIGH	70
	min	69.3	2.8	0.9	1.35	25	1	60	FF	LOW	70
	typ	126.3	3.8	1	1.5	20	5	50	TT	NOM	27
DC Gain (dB)	max	71.68	4.8	1.2	1.65	25	10	50	SS	NOM	0
	min	62.19	2.8	0.9	1.35	15	1	50	FF	NOM	70
	typ	68.86	3.8	1	1.5	20	5	50	TT	NOM	27

Another method to control the system stability is to check transient simulations and analyse the ringing in the transient waveforms. For that purpose, a disturbance pulse is added to the feedback voltage node in the setup seen in Figure 4.7 and any possible effect on the circuit is analysed. The disturbance current is indicated in Figure 4.9 as *100nA* with $50\mu s$ period. The output voltage of buck converter and the inductor current have disturbance effect. However, any ringing which is a result of PM below $45°$ is not observed. From the transient analysis point of view, the circuit is stable.

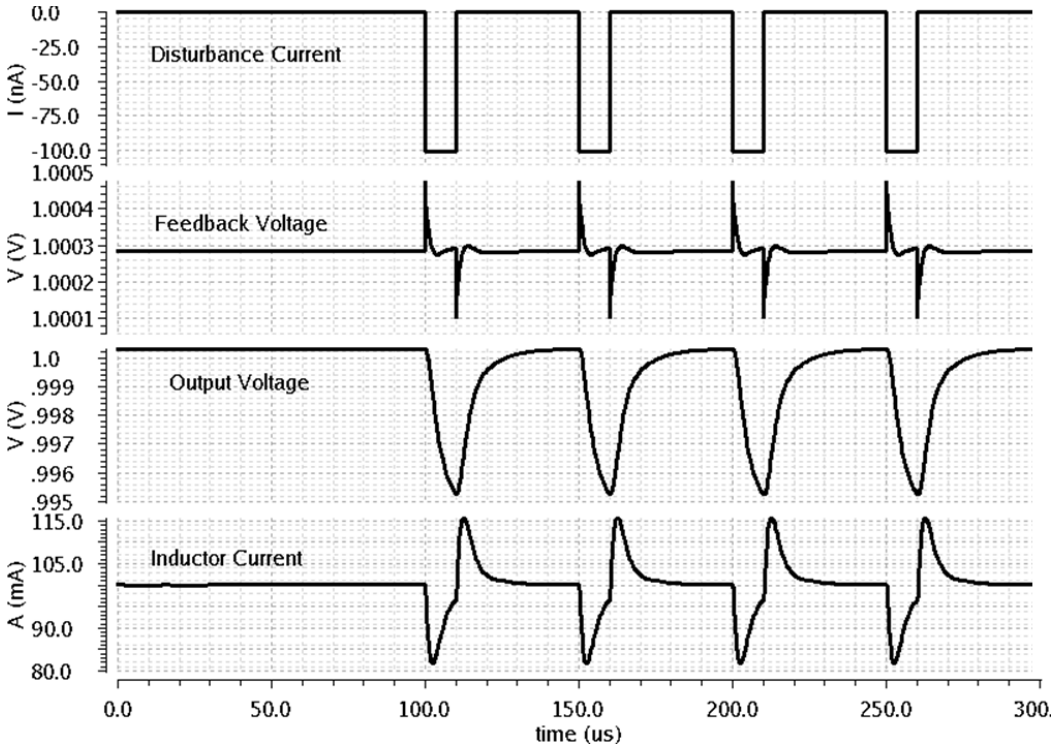

Figure 4.9. Transient behaviour of the model with perturbation to the system.

5. CIRCUIT DESIGN OF THE OTHER BLOCKS

The other sub blocks that help to make the adaptive output buck converter are PWM comparator, ramp generator, V_{sense} sample and hold circuit, pre-driver and driver, current sense block and active diode comparator. Those are the blocks that are not specific for this work. However, they are still necessary to be able to have a working setup.

5.1. PWM Comparator

The PWM comparator is a latching comparator with below *20ns* propagation delay, below *10mV* 3σ input DC mismatch and below $10\mu A$ quiescent current specifications. A two stage comparator is designed to implement it with a digital latching functionality. The latching function is required to prevent a false triggering caused by a possible supply ringing. If supply parasitic is not included to the supplies, supply ringing is not a problem, and so, there is no need to the latching function.

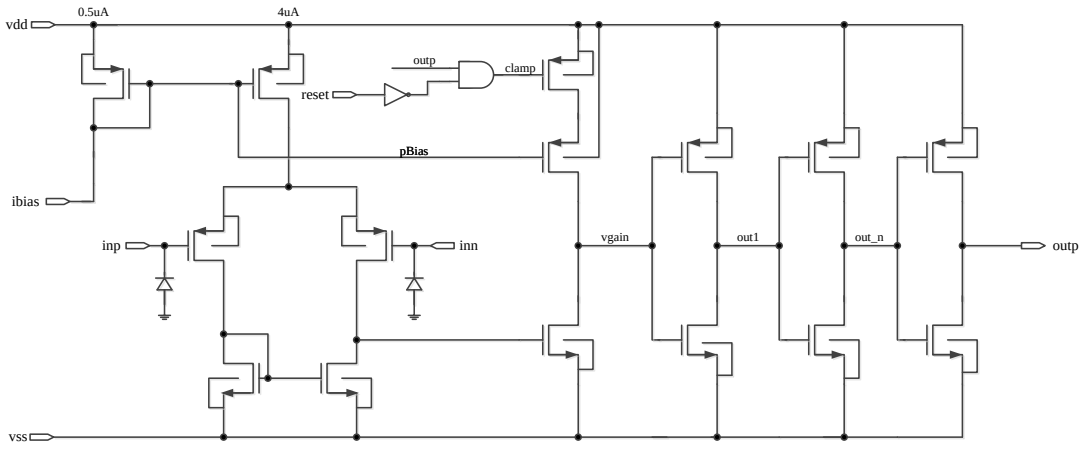

Figure 5.1. Schematic of PWM comparator.

According to the designed digital latching functionality which can be seen in Figure 5.1 created by logic by taking the output of the comparator as feedback, the comparator output trips high and as long as reset signal remains low, the output stacks at a high value. It will require a reset signal to be able to make a low transition when it is required

according to the inputs. To do that, the feedback is taken from the output of the comparator and used to generate the signal called "*clamp*".

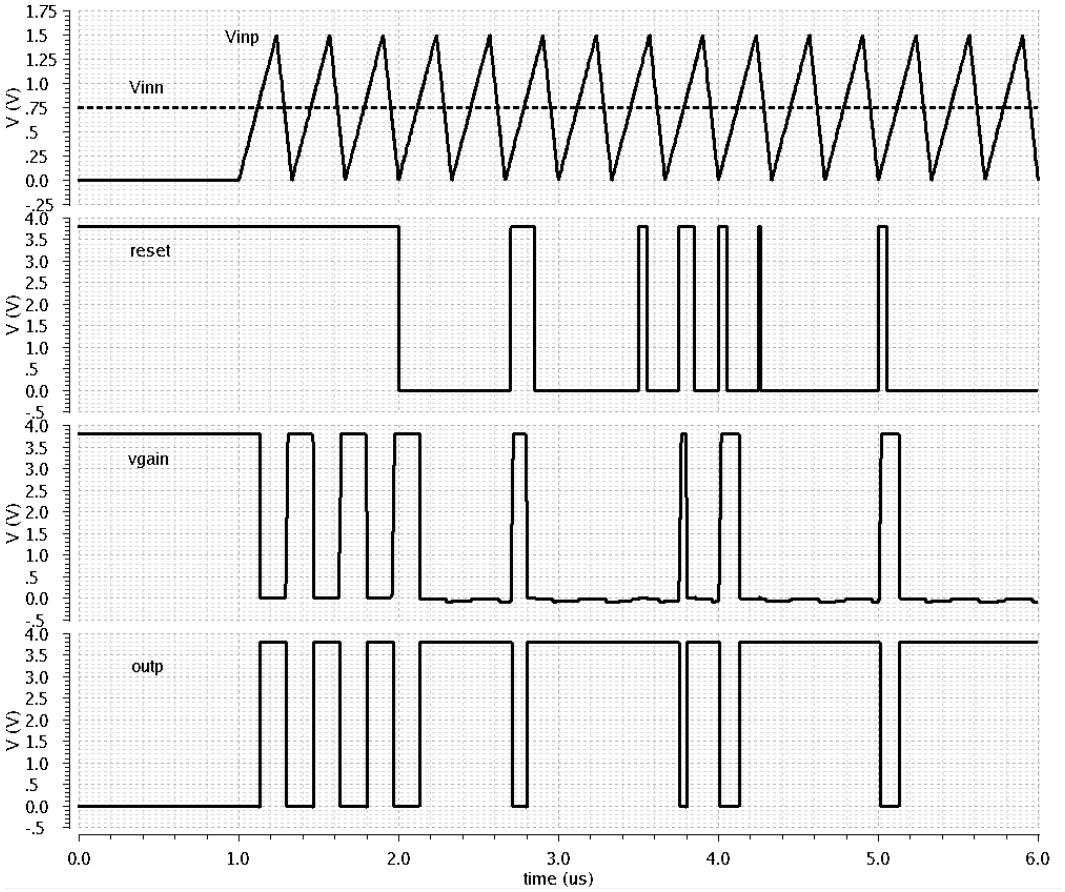

Figure 5.2. Typical transient waveforms of PWM comparator.

The functionality of the design is checked with both transient and DC simulations. To check the latching functionality, speed of the comparator and its quiescent current performances are checked with a transient setup and its input offset performance is checked with a DC setup.

The latching functionality is checked by applying pulses in random time to the reset signal and its effect is checked at the output of the comparator. When the reset signal is high in the beginning of the simulation and the propagation delays and average quiescent currents are measured at that region. Over the PVT, the worst case propagation delay is *20.58ns* and worst case quiescent current is *9.161µA*.

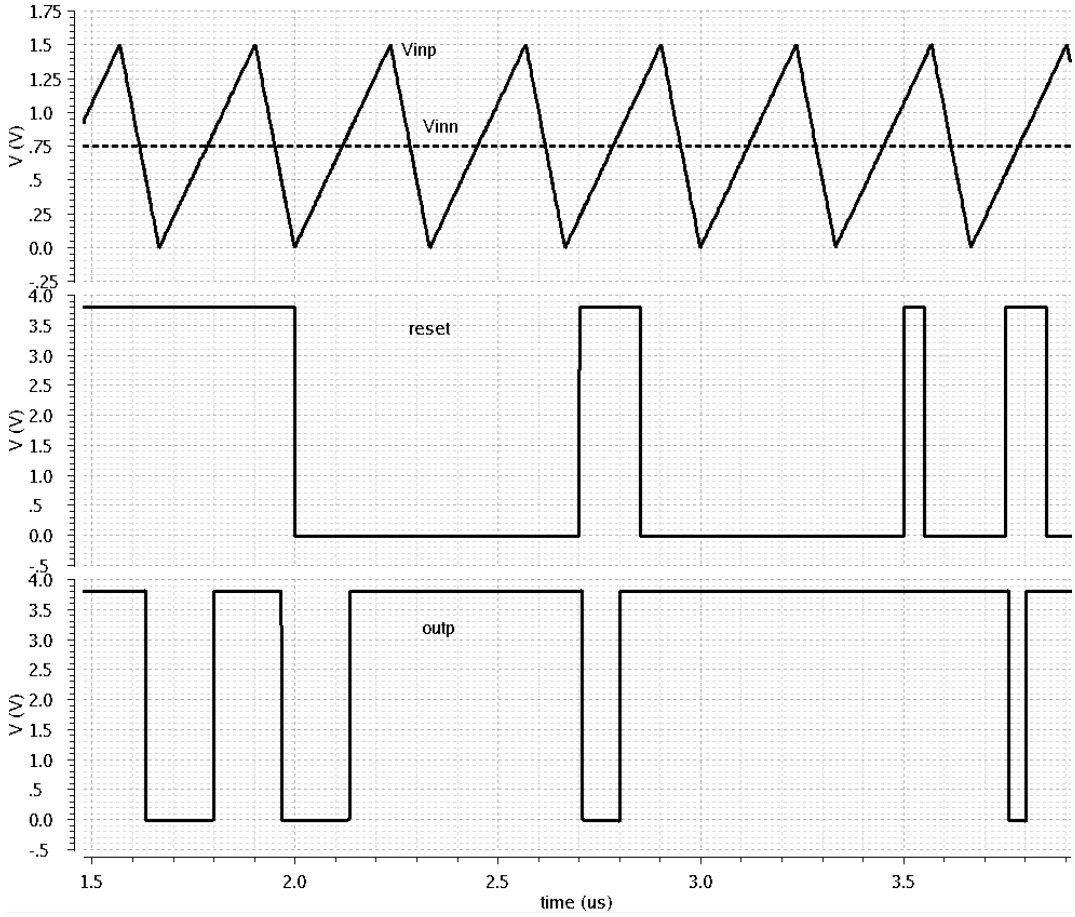

Figure 5.3. Typical transient waveforms -showing the latching functionality.

The input offset of the comparator is checked with a DC simulation. DC input offset is defined as the voltage variation between the crossing points of negative and positive inputs and the point that output makes transition. Monte Carlo simulation to check the mismatch variation is also realized in DC setup. The Monte Carlo (MC) simulation is run in typical corner by choosing mismatch option in simulator.

According to the results of MC simulation which are shown in Figure 5.4, the mean of DC offset value is *-357.5μV* and the *3σ* standard deviation is *11mV*. Its specification was *10mV*. According to the spread shown in MC histogram below, the maximum value of the DC offset is *10.64mV* and the minimum value is *-10.29mV*.

Table 5.1. Summary of PVT simulation results of PWM comparator.

Expressions		Value	Corners			
			Supply Voltage (V)	active	Bias Current (nA)	Temp (°C)
t_{prop_rise} (ns)	max	20.58	4.8	SS	475	70
	min	14.83	2.8	FF	525	0
	typ	17.3	3.8	TT	500	27
t_{prop_fall} (ns)	max	20.29	4.8	SS	475	70
	min	12.38	2.8	SNFP	525	0
	typ	16.18	3.8	TT	500	27
I_{DDQ} (µA)	max	9.161	4.8	FF	525	0
	min	5.1	2.8	SS	475	0
	typ	6.143	3.8	TT	500	27
I_{DDQ_OFF} (pA)	max	166	4.8	FF	525	70
	min	1.772	2.8	FNSP	475	0
	typ	67.53	3.8	TT	500	27
Input DC offset (µV)	max	-637.5	4.8	FF	525	70
	min	-262.5	4.8	SS	475	0
	typ	-437.5	3.8	TT	500	27

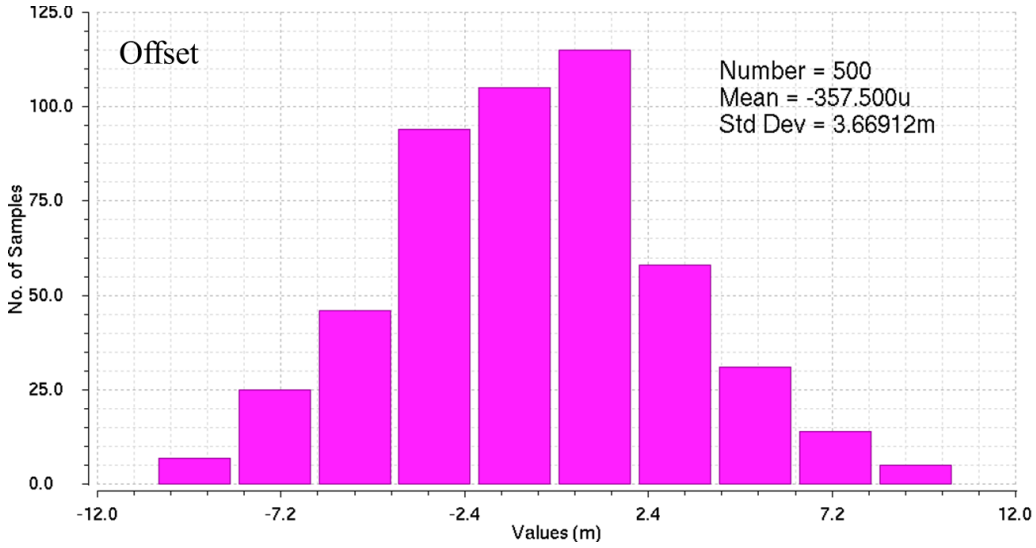

Figure 5.4. MC histogram of the input offset of PWM comparator.

5.2. Ramp Generator

The ramp generator is a circuit specified with a trimmable ramp voltage, switching frequency at *3MHz* and the output ramp voltage range between *100mV* and *1.8V*. For the trimmable ramp voltage implementation, the current which flows through the capacitor is changed with 3-bits trimming. According to the working principle of the circuit, the reset input turns on and off the PMOS switch connected to the voltage node "*cRAMP*". When the switch is on, it conducts and *cRAMP* voltage goes to the supply level since capacitor is discharging. When the switch is off, the current flows through the capacitor, and the voltage in the node ramps down linearly depending on the capacitor size and current amount. The same current is mirrored to the other branch and the voltage on the output "*vRamp*" is defined as a ratio between the resistor in the design and a resistor which is placed to the output of the ramp generator which is *40k*Ω. The schematic design of ramp generator is demonstrated in Figure 5.5.

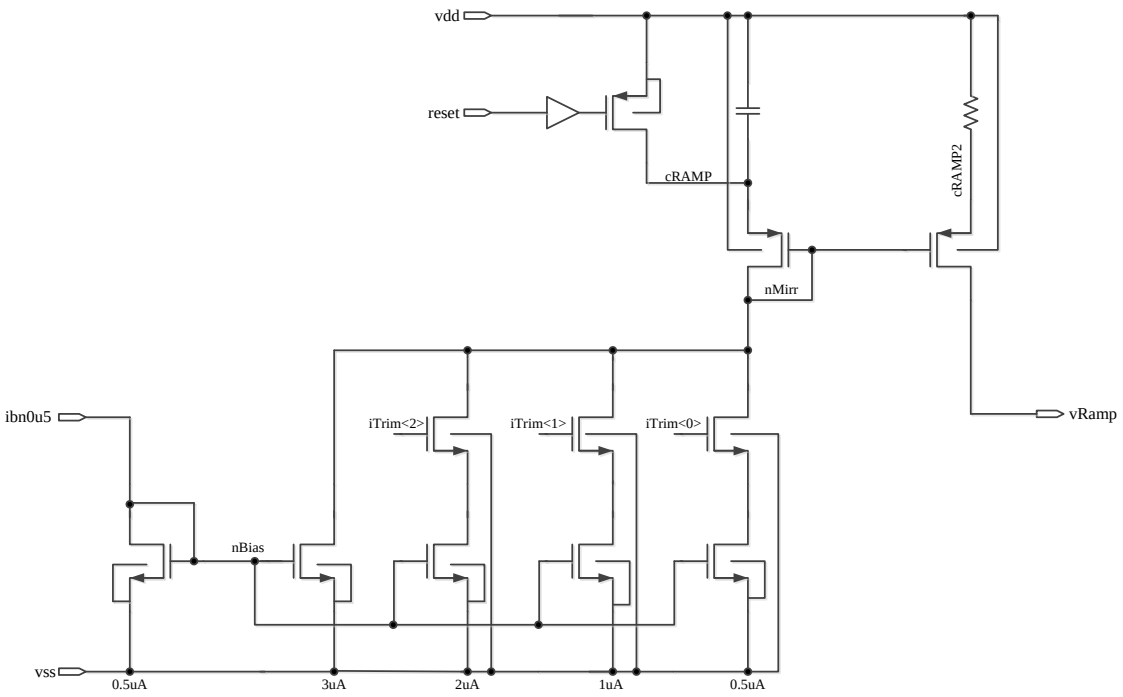

Figure 5.5. Schematic of the ramp generator.

Table 5.2. Transient simulation results of ramp generator over PVT corners.

	TYP		PVT			
iTrim<2:0>	Dip of Voltage Ramp (mV)	Peak of Voltage Ramp (V)	Dip of Voltage Ramp (mV)		Peak of Voltage Ramp (V)	
			Min	Max	Min	Max
000	106	0.747	84	131	0.606	0.877
001	122	0.902	98	151	0.731	1.058
010	138	1.063	111	172	0.867	1.246
011	154	1.213	124	192	0.985	1.421
100	169	1.389	136	213	1.134	1.626
101	185	1.533	149	234	1.237	1.794
110	200	1.691	161	255	1.329	1.979
111	216	1.825	174	277	1.376	2.136

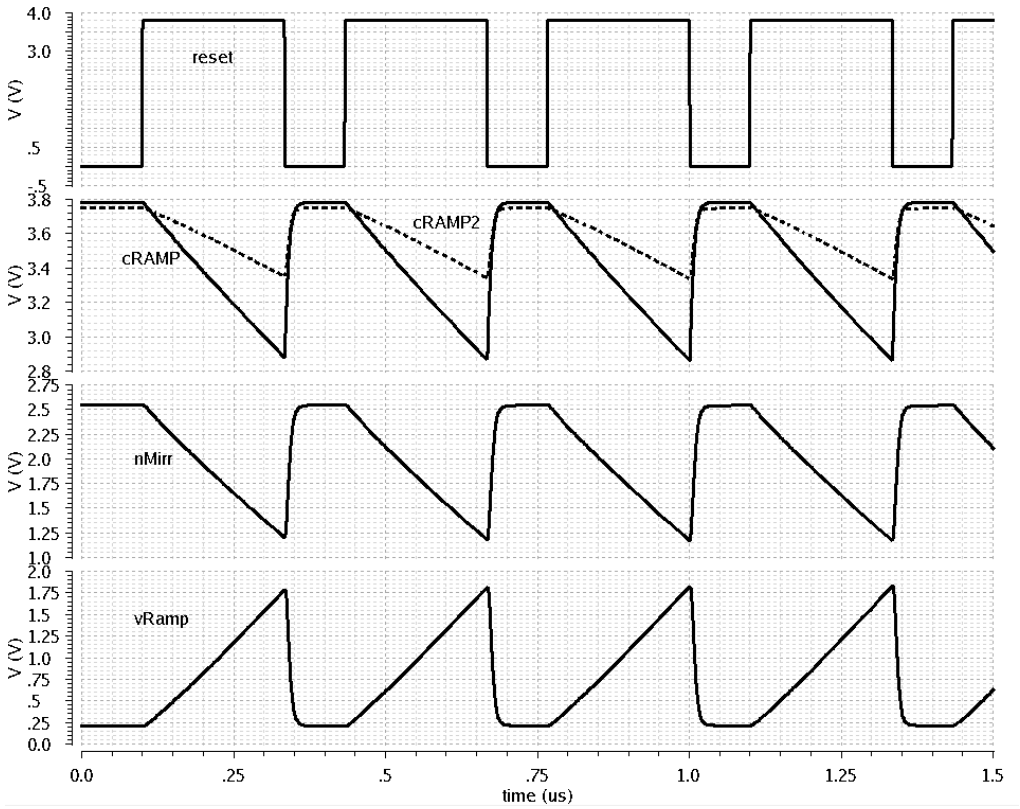

Figure 5.6. Typical transient waveforms of ramp voltage.

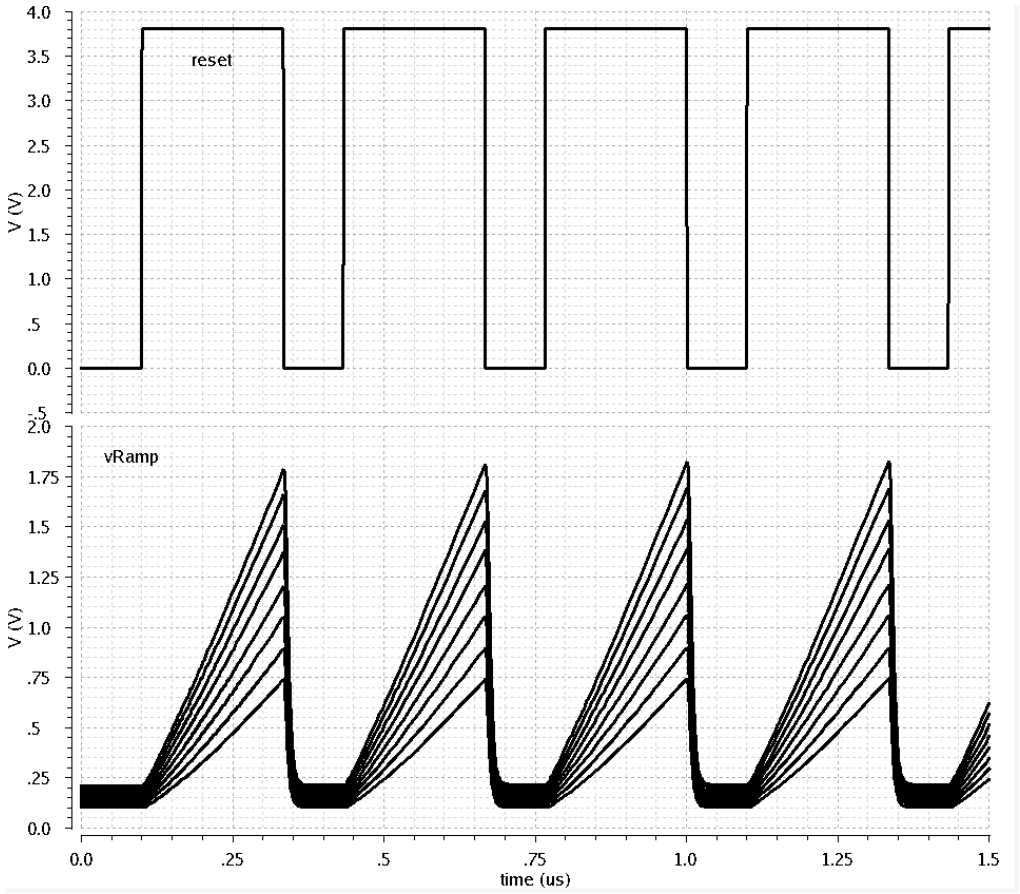

Figure 5.7. Typical transient waveforms of ramp voltage for various trim codes.

5.3. V_{sense} Sample and Hold Circuit

Adaptive resistive g_m block uses the *LX* voltage (the output voltage of buck converter before filtering) and a fixed reference voltage as its inputs. That fixed reference voltage is a ratio of a simple resistive divider from supply to the ground. The other voltage input is the *LX* voltage when the PMOS is on. The main aim is to use the voltage drop on the output stage PMOS. Therefore, the *LX* voltage is used in second negative input and switching supply level is used in the second positive input of the adaptive resistive g_m block. However, the V_{sense} sample & hold circuit is designed to solve a problem emerged in that point. Since the *LX* voltage is changing over the time between *0V* to $(V_{SUPPLY}\text{-}V_{DROP,PMOS})V$, V_{sense} sample & hold block needs to be flat as possible for the sake of adaptive resistive g_m which is a highly linear block but, slow in response time. To be able to do that, the V_{sense}

block is designed to sense the *LX* voltage in correct point, sample it and hold in the sample point for the other cycle which the *LX* goes to zero.

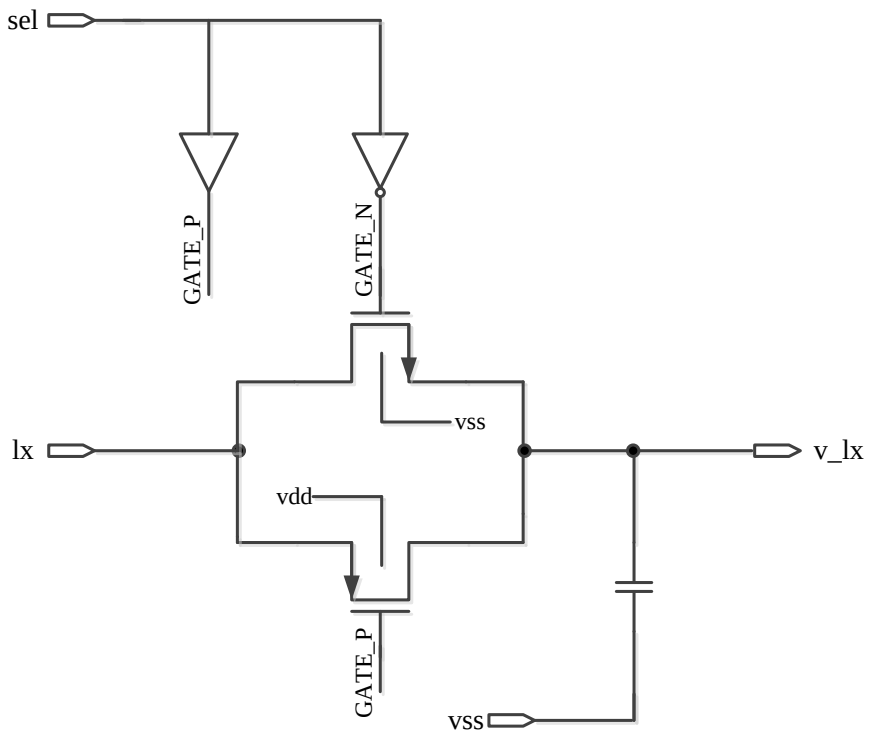

Figure 5.8. Schematic design of V_{sense} sample & hold block.

The design consists of basic NMOS and PMOS switches connected together and a sampling capacitor at the output. The switch sizes are almost minimum size to be able to decrease charge injection to the sampling capacitor as much as possible. Two switches are used as PMOS and NMOS and the switches are driven with inverted signals to minimize charge injection again. Sampling signal which is called "*sel*" in Figure 5.8 comes from the gate voltage of output PMOS.

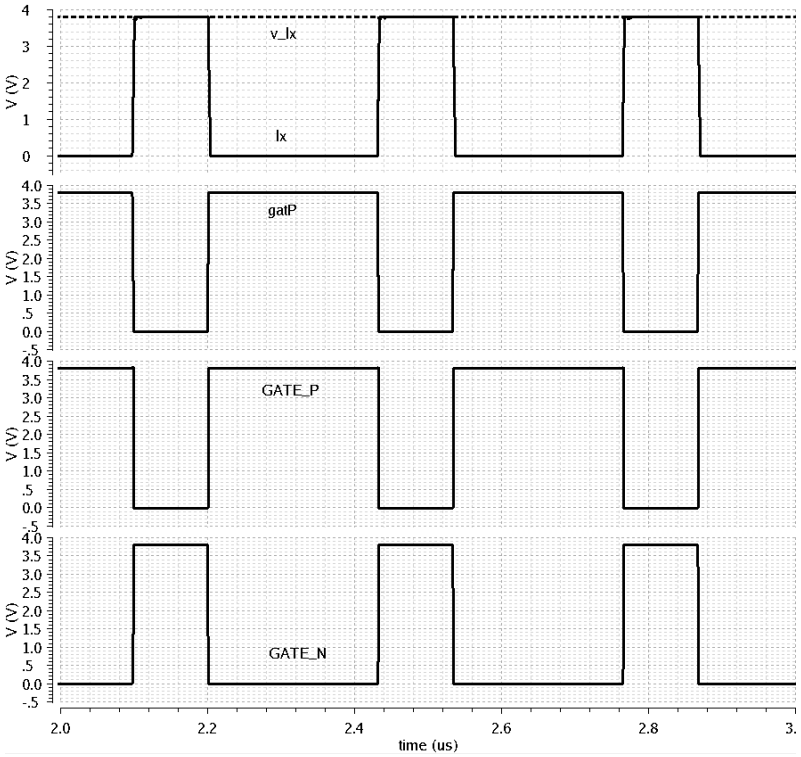

Figure 5.9. Transient waveforms of V_{sense} sample & hold block.

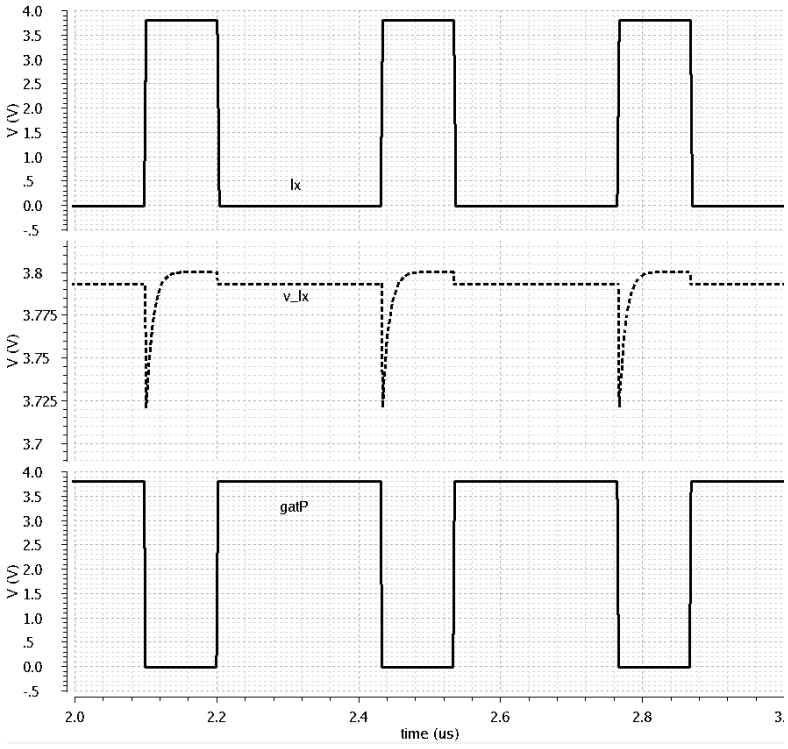

Figure 5.10. Transient waveforms of V_{sense} - zoomed into the output.

It is important to have a sampled voltage which does not vary ideally. Therefore, the voltage drop on the output voltage of V_{sense} sample and hold block is measured. This drop is calculated as a voltage drop between when the selection logic is logic-0 and when it is logic-1. The measurements are done over the PVT and the results are shown in following table:

Table 5.3. Transient simulation results over PVT corners.

	TYP	PVT	
		Min	Max
$V_{SENSE,DROP}$ (mV)	6.85	1.989	15.44

5.4. Pre-driver and Driver

The adaptive pre-driver and driver are among the critical circuit blocks for proposed adaptive buck converter topology since they are the main units to drive various output loads and the efficiency of the buck converter is directly related to their unit sizes. There is a size for PMOS driver transistor which is a result of calculation for optimum efficiency. To be able to size the PMOS driver first the efficiency curves of generic buck converters are analysed. The peak efficiency of buck converter efficiency curves are about the *1/3*rd of the maximum load current. The adaptive buck converter design in this work can provide *5.6A* maximum load current so that, the peak efficiency is around *1.8A* load current. Combining the maximum current of the peak efficiency and the R_{ON} of the PMOS device, size for the PMOS driver is calculated for optimum case. The NMOS driver transistor size is then calculated in compliance with the PMOS driver transistor's size. The small replica of the PMOS driver is put into the design to be able to sense the load current. The transistor chain connected to *LX* and *vssSW* nodes is shown in Figure 5.11.

In zero cross comparator, the *LX* and *vssSW* nodes are needed to be compared. Therefore, the *LX* and *vssSW* nodes are needed to use as outputs from the main drive unit. The series transistors chains are for ESD purposes since the *LX* and *vssSW* nodes are exposed to ESD events as outputs connected to the outside world, there is a need for an

extra circuit between these nodes and the input gates of zero cross comparator. The same amount of transistors which are *16* with the same sizes are implemented between the zero cross comparator inputs and *LX – vssSW* nodes to obtain same amount of variation with the supply ringing.

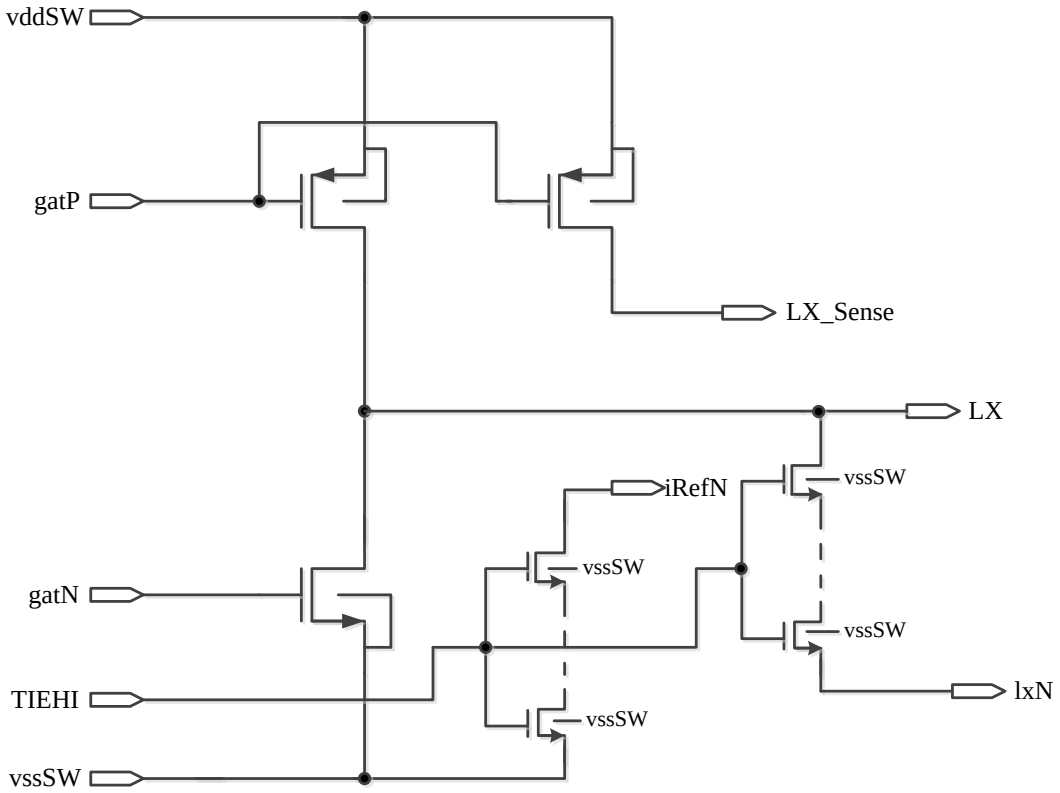

Figure 5.11. Schematic of unit driver/pass device.

Another specification for this block is the non-overlapping circuit implementation since the PMOS and NMOS conducting at the same time creates short circuit current which is an immense issue since it affects efficiency directly. Therefore, a non-overlapping logic is implemented to prevent short circuit current flowing on pass transistors as much as possible. The implementation is done inside the pre-driver shown in Figure 5.12. Gate of the PMOS and gate of the NMOS driver transistors are driven with "*gatP*" and "*gatN*" signals. There is approximately *2ns* delay between those signals thanks to the non-overlapping structure. The unit buffers are different for driving the signals *gatP* and *gatN* according to the different PMOS and NMOS strengths. The adaptive method used in the output stage has a positive impact on the short circuit current as well since the segment size

is smaller. The P_{off} and N_{off} block depicted in Figure 5.12 are designed to compensate a phenomenon called dv/dt induced turn-on phenomenon [77] which is described as follows:

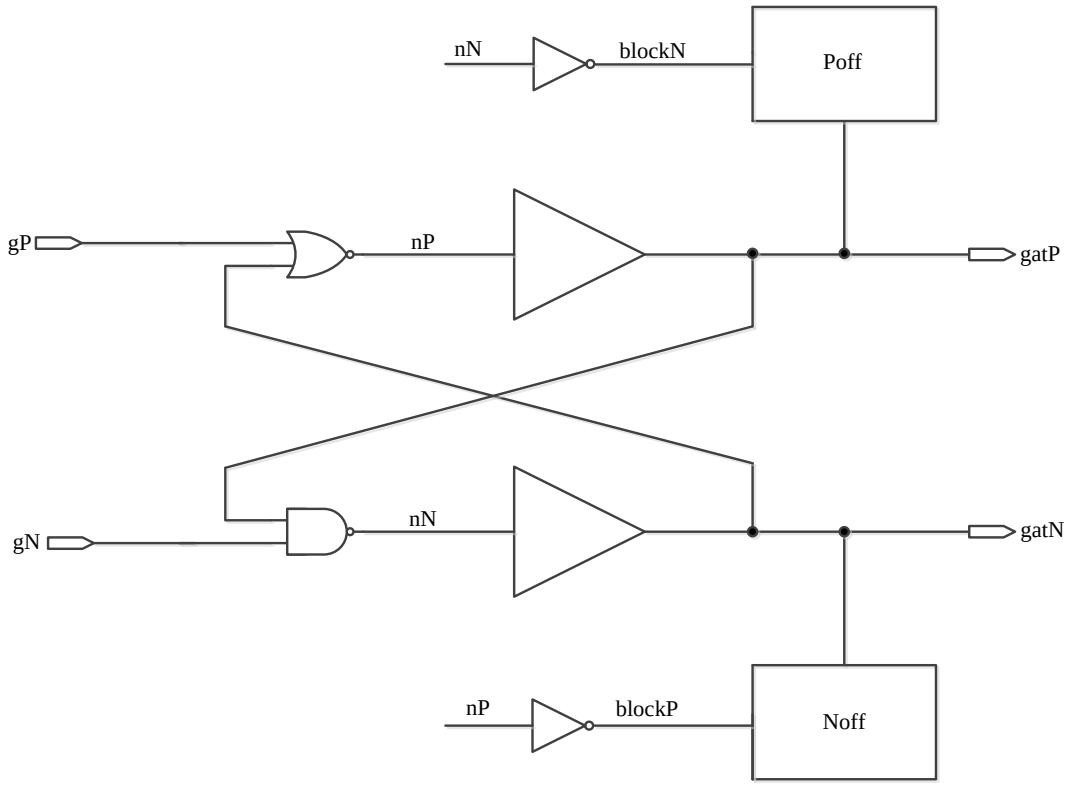

Figure 5.12. Schematic of unit pre-driver.

In Figure 5.13, when V_{gN} signal is decreased to *0V* the V_{gP} signal is still in higher voltage levels due to purposely created dead time with the non-overlapping logic structure. When the V_{gP} decreases due to the current path which is shown in Figure 5.13, the V_{gN} voltage is pushed to go higher voltages thanks to the big parasitic capacitance, C_{gdN}. This situation called dv/dt induced turn-on phenomenon or shoot-through. The same applies to the PMOS transistor in the opposite transition.

For the implementation of S_{aux} transistor shown in Figure 5.13 which is the transistor pulling down the V_{gN} node during transition and the similar replica of it in the PMOS driver side, the following designs are implemented shown in the Figure 5.14 and Figure 5.15.

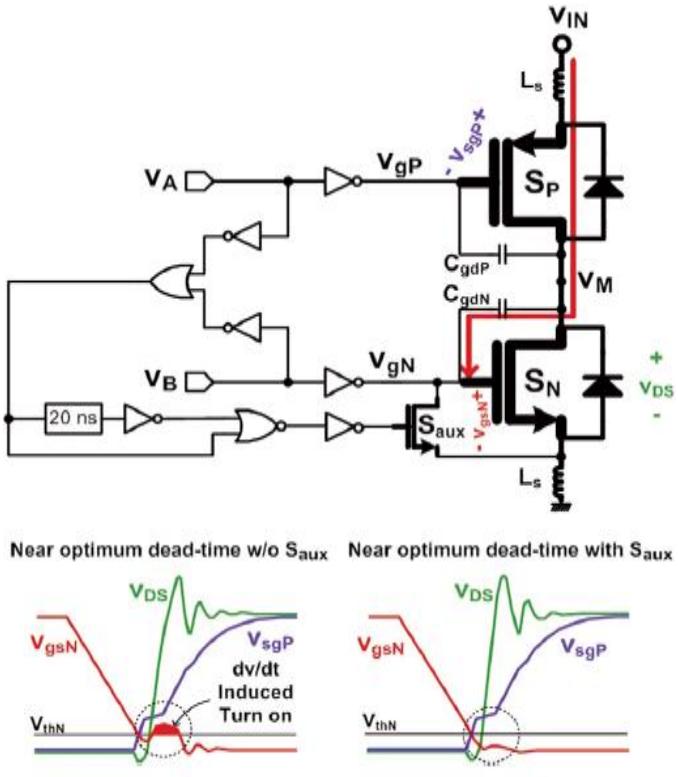

Figure 5.13. dv/dt induced turn-on phenomenon [77].

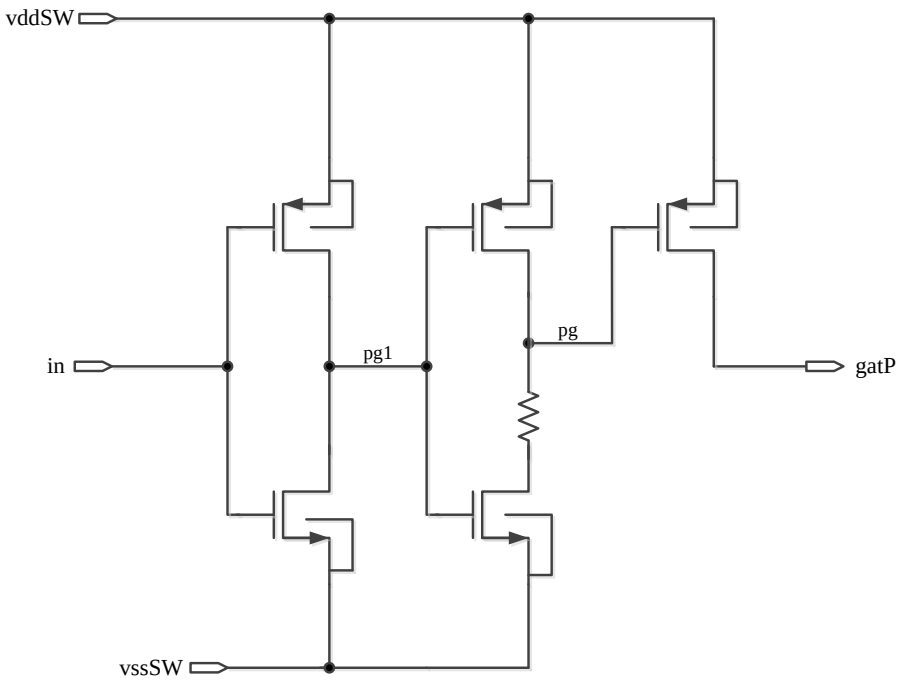

Figure 5.14. Schematic design of P_{off} logic.

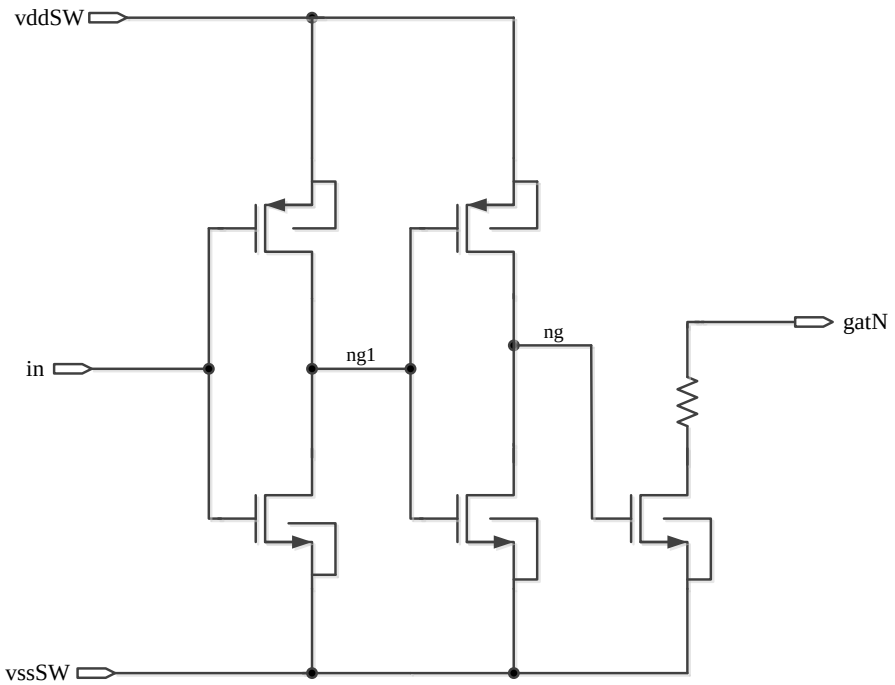

Figure 5.15. Schematic design of N_{off} logic.

The measured parameters for the adaptive pre-driver and driver units are the non-overlapping timing, propagation delays, quiescent and leakage currents. Table 5.4 shows the summary of all calculated parameters.

In Figure 5.16, just before the shoot-through condition appears, *blockP* signal makes a transition from logic-0 to logic-1 to be able to activate the N_{off} block and the N_{off} block tries to pull the gate of N-type pass device to the *0V*. *ng* signal seen in the waveform shows the gate of the NMOS transistor in N_{off} block. Just after the *blockP* signal makes a transition, ng signal also makes the transition from logic-0 to logic-1 to drive NMOS gate in N_{off} block. Thanks to this implementation, the peaking in the *gatN* signal is decreased from *950mV* to *450mV* which is below the threshold of the NMOS driver transistor.

Similarly, in Figure 5.17, just before the shoot-through condition appears, *blockN* signal makes a transition from logic-1 to logic-0 to be able to activate the P_{off} block and the P_{off} block tries to pull the gate of P-type pass device to the high voltage level. *pg* signal shows the gate of the PMOS transistor in P_{off} block. Just after the *blockN* signal makes a

transition, *pg* signal is also making the transition from logic-1 to logic-0 to drive PMOS gate in P_{off} block.

Table 5.4. Summary of PVT simulation results of unit pre-driver & driver.

Expressions		Value	Corners		
			Supply Voltage (V)	active	Temp (°C)
$t_{prop_rise,PMOS}$ (ns)	max	6.319	2.8	SS	70
	min	2.418	4.8	FF	0
	typ	3.428	3.8	TT	27
$t_{prop_fall,PMOS}$ (ns)	max	8.856	2.8	SS	70
	min	4.532	4.8	FF	0
	typ	5.57	3.8	TT	27
$t_{prop_rise,NMOS}$ (ns)	max	11.17	2.8	SS	70
	min	3.978	4.8	FF	0
	typ	5.76	3.8	TT	27
$t_{prop_fall,NMOS}$ (ns)	max	3.257	2.8	SS	70
	min	1.625	4.8	FF	0
	typ	2.03	3.8	TT	27
$I_{sc,PMOS}$ (mA)	max	121.4	4.8	FF	70
	min	11.14	2.8	SS	70
	typ	24	3.8	TT	27
$I_{sc,NMOS}$ (mA)	max	147.5	4.8	FF	70
	min	7.24	2.8	SS	70
	typ	27.5	3.8	TT	27
I_{DDQ} (µA)	max	426.9	4.8	FF	70
	min	121.9	2.8	SS	0
	typ	185.25	3.8	TT	27
I_{DDQ_OFF} (µA)	max	1.44	4.8	FF	70
	min	0.566	2.8	SS	0
	typ	0.8	3.8	TT	27

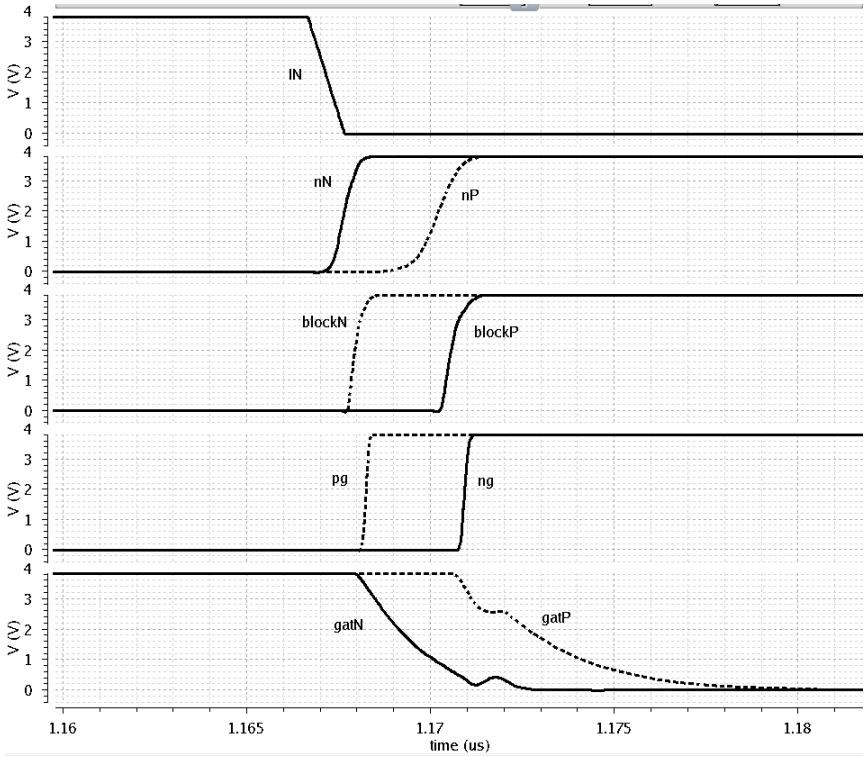

Figure 5.16. Transient waveforms in falling edge of input– showing dead times.

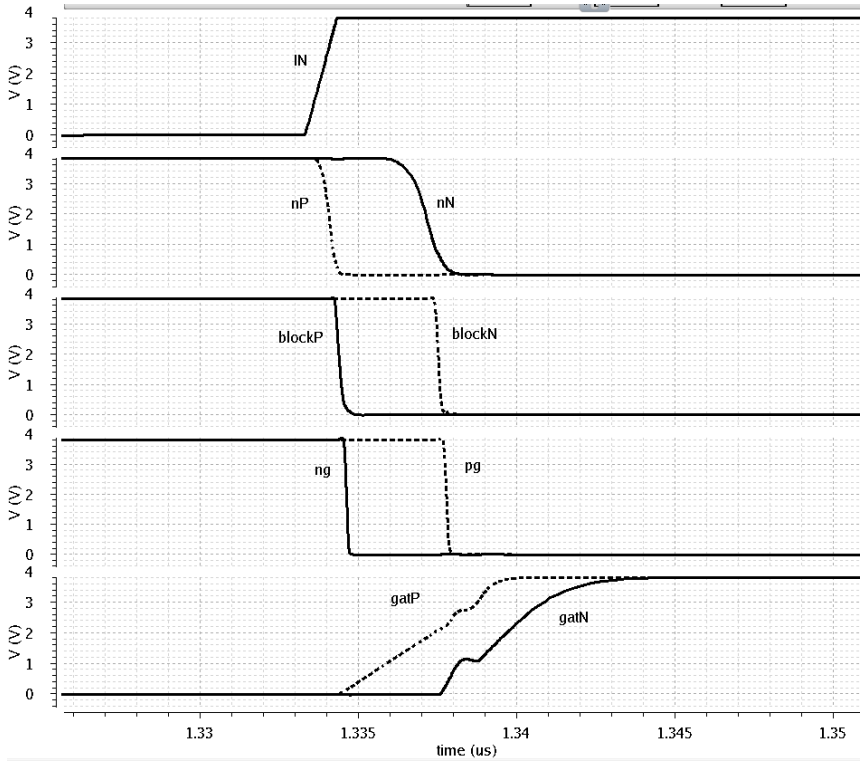

Figure 5.17. Transient waveforms in rising edge of input– showing dead times.

5.5. Current Sense Block

Current sense is one of the blocks which need to be designed together with output stage/pass devices. The basic principle is the following; a small replica of the main PMOS pass device is realized and current sense block senses the current on this small replica which replicates the coil current information. Therefore, it is also important to have matching between the main pass device and its small replica to be able to have a good sense ratio. However, having such big ratios between the replica transistor and the main PMOS transistor causes a significant mismatch in sensing the currents. This is the main trade-off in the design. To be able to design the current sense block itself, it is necessary to add the pass transistor and a small replica to the test bench for the reasons explained above. The sensing ratio between the main PMOS and the replica transistor is *1000*. This *1000* times smaller current than the main pass device current on one segment is an input to the current sense block and it is divided to *40* inside current sense block. The total current sensing ratio is $1/40K$ which means that sensing current is $I_{seg}/40K$ where total segment current is I_{seg}. Those ratios are decided by considering the possible segment current values and the adaptive resistive g_m block input current range since the output of the current sense is the input of adaptive resistive g_m. The adaptive resistive g_m is designed such that it can work very linearly if its input current is in the range *100nA – 1μA*. So, it is necessary to have a sensed current in the output of the current sense block between those ranges. On the other hand, the segment currents can be in the range of *10mA – 40mA* since the segment current is defined by I_{LOAD}/n. The sensed currents for various loads are shown in the Table 5.5.

In the design of the current sense block, the current of the small replica PMOS is taken as an input to the circuit. It is first mirrored to a ten times smaller transistor. This current is mirrored again by a four times smaller PMOS and the output current is obtained. Finally, with the four times mirroring, the output current is taken from the current mirror supplied by another supply domain to eliminate the variations which may occur due to the supply variation in the pass stage [5].

Table 5.5. Current sense variation over load currents.

I_{LOAD} (mA)	n	I_{seg} (mA)	I_{sense} (nA)
10	1	10	250
18	1	18	450
32	3	10.66	266.5
56	5	11.2	280
100	8	12.5	312.5
180	15	12	300
320	26	12.3	307.5
560	32	17.5	437.5
1000	32	31.25	781.5

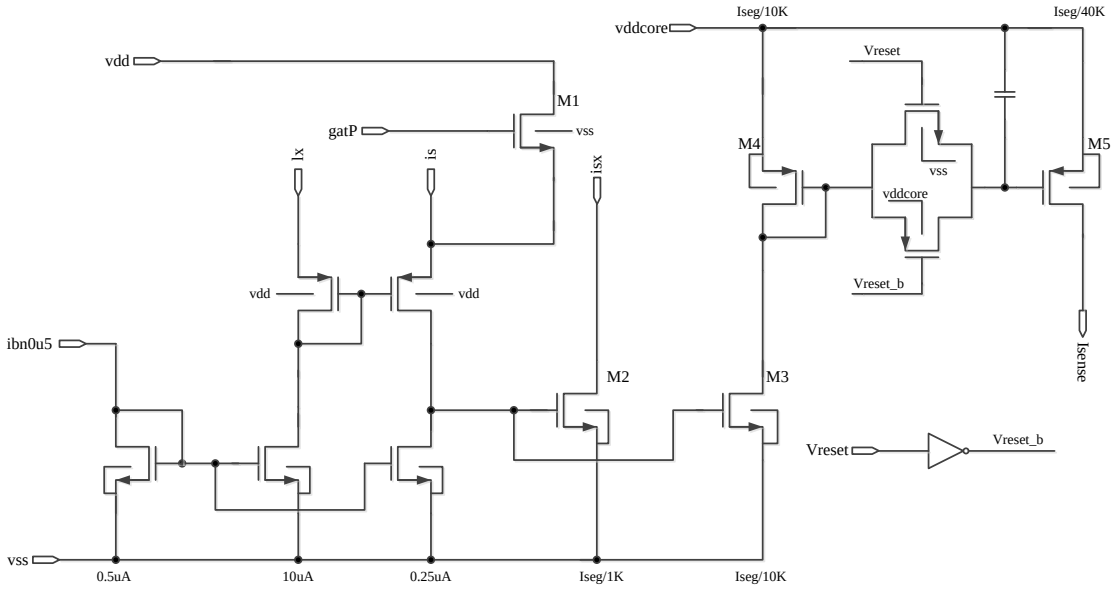

Figure 5.18. Schematic of current sense block.

The current sense is a DC circuit working at but, it needs to work correctly when the driver PMOS turns on and off with buck converter switching frequency which is *3MHz*. Therefore, special attention must be taken care to obtain correct sensing values. To be able to do that, an NMOS bleeding current scheme is applied to the design. When the PMOS turns on and off with the related switching speed, it would require some time to charge the

gates of the mirroring transistors M2 and M3. Since this time is not enough to make M2 conducting, the circuit does not give correct sensed current with fast transitions. To prevent this problem, a NMOS device M1 is added to the circuit which will bleed current when the PMOS is off as well. It holds the gate of M2 at some voltage level so that it does not require much time to turn on in every cycle. This approach works fine and used as a correction scheme to find the correct sensing current at the output.

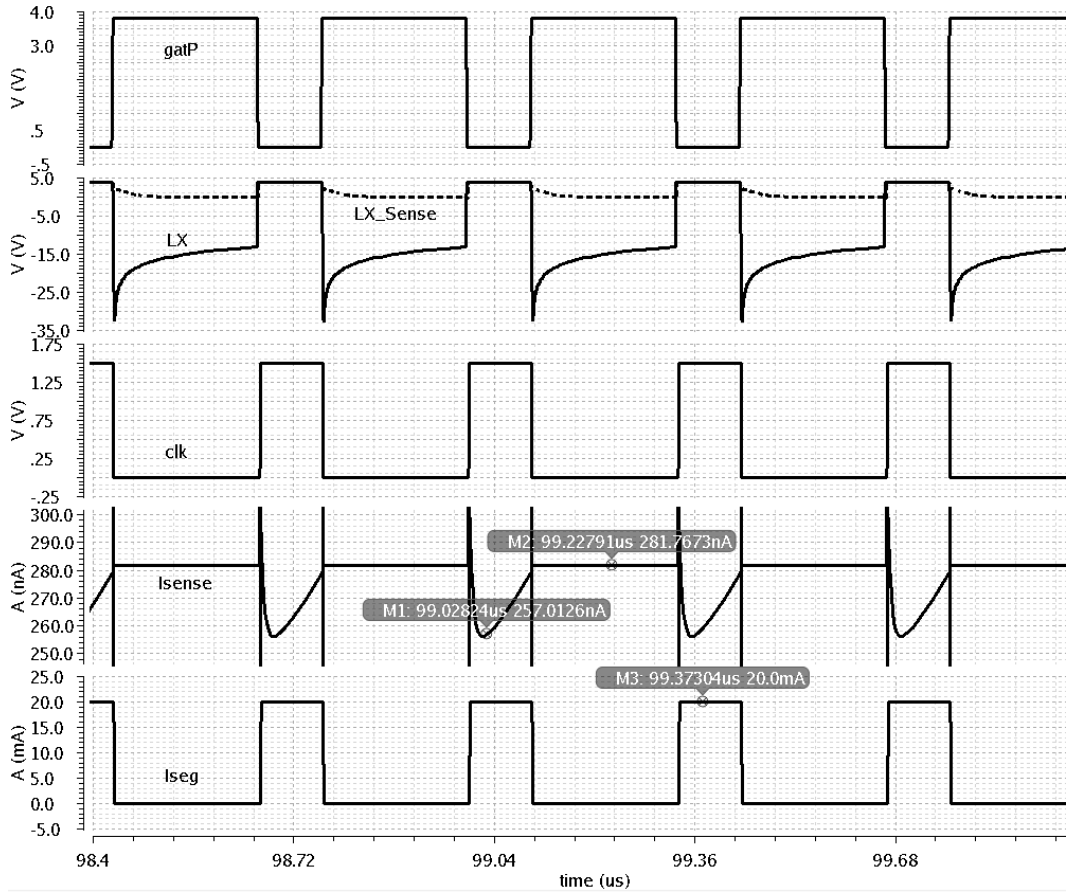

Figure 5.19. Typical transient waveforms of current sensing.

To be able to have a reasonable performance in the switching transient, the output current sense must be as flat as possible which is not the case if the switching segment current is taken as an input current to the circuit. It is needed to sense the current from the output stage when only the PMOS is on. When it is off, the current decreases and the sensed current becomes meaningless in that cycle. It is a real issue since the output of this block is the current input to the adaptive resistive g_m block which is slow in response time

due to its nature and the compensation capacitor. A sample and hold mechanism is implemented to the output mirroring of the current sense block between the transistors M4 and M5 so that when the PMOS is on, the current is sampled and it is held during the off period of the PMOS to keep the inputs of the adaptive resistive g_m block as constant as possible.

During the simulations, the quiescent currents when the circuit is on and off are measured in transient setups together with the pass transistor and the small replica transistor. The DC performance of the circuit is also measured to see the supply and temperature variations of the circuit. The output current of the current sense block is fully dependent on the supply voltage variation and temperature variations since the pass device and its small replica is connected to that supply voltage and the voltage drop on those is the input for the current sense block. Also, the temperature is a huge effect since the pass devices are large transistors and their performance degrades more with temperature. Therefore, the supply voltage and temperature sweeps are done in the typical corner to check the performance of the current sense block.

Table 5.6. Summary of PVT simulation results of current sense design.

Expressions	Conditions		Value	Corners				
				High Supply (V)	Low Supply (V)	active	Bias Current (nA)	Temp (°C)
I_{sense}@TRAN (nA)	I_{seg}=10mA	typ	84.2	3.8	1.5	TT	500	27
	I_{seg}=40mA	typ	476.3	3.8	1.5	TT	500	27
I_{DDQ} (µA)	I_{seg}=40mA	max	18	4.8	1.65	FF	475	0
		min	11.42	2.8	1.35	SNFP	525	0
		typ	12.29	3.8	1.5	TT	500	27
I_{DDQ_OFF} (nA)	I_{seg}=40mA	max	14.56	4.8	1.65	FF	525	70
		min	13.29	2.8	1.35	SS	475	0
		typ	13.79	3.8	1.5	TT	500	27
I_{sense} @ DC (nA)	I_{seg}=12.5mA	typ	365	3.8	1.5	TT	500	27

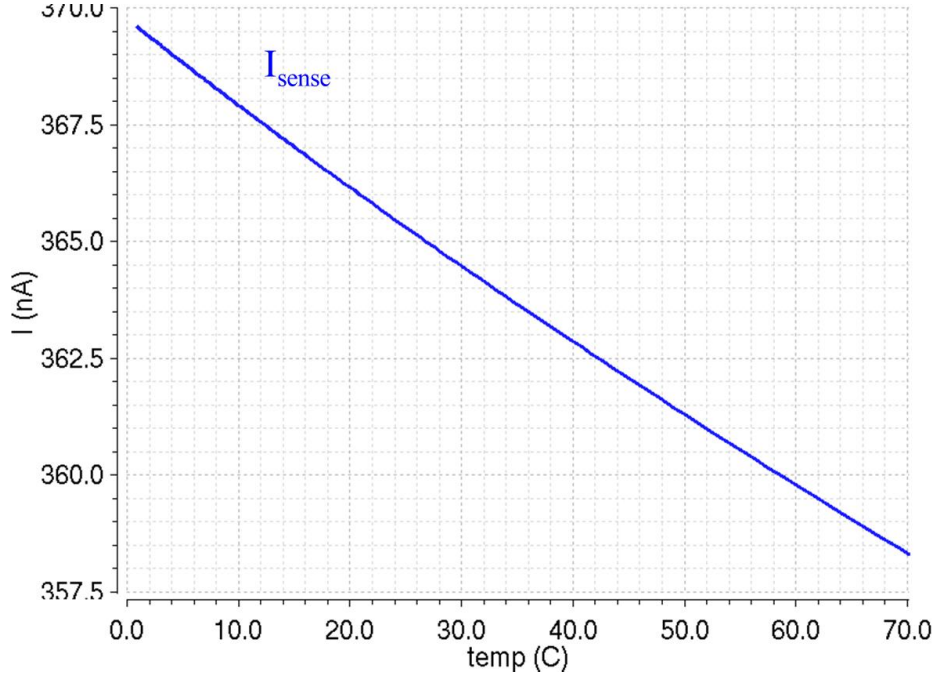

Figure 5.20. Temperature variance of sensed current.

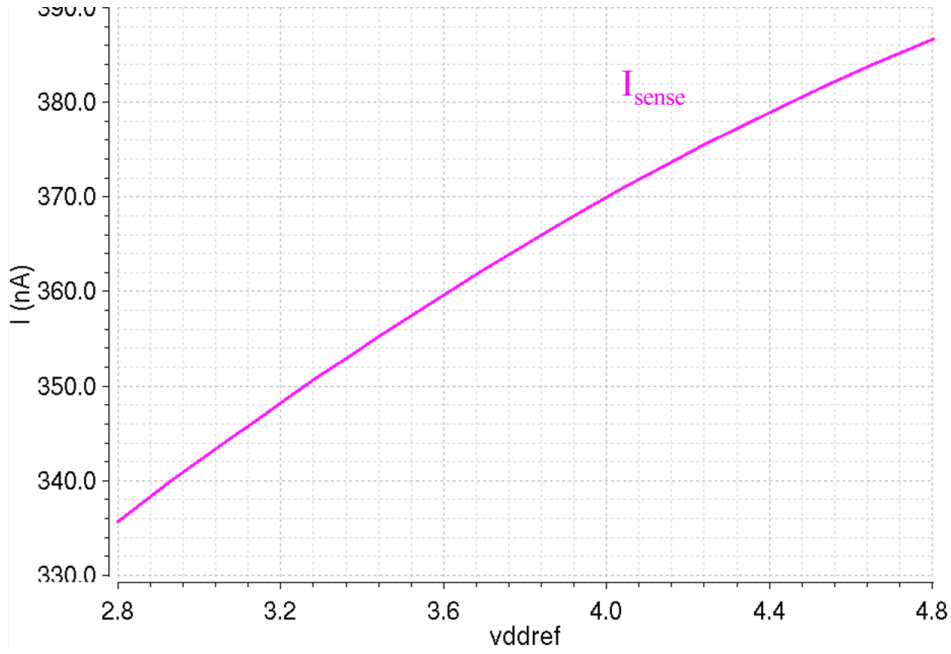

Figure 5.21. Supply voltage dependency of sensed current.

The variance in the sensed output current is in the range of *11nA* within the given temperature range which is *3%* as percentage error. Similarly, the variance in the sensed

output current is in the range of *50nA* within the given supply voltage range which is around *13%* as percentage error.

Monte Carlo simulations are also performed to see the process variation of the circuit. The MC simulation is run at the typical corner by choosing both the process and mismatch options in the simulator. According to the results, the mean of the output current sense is around *362.5nA* and the *3σ* standard deviation is *79nA*. The maximum of the output current sense is *432nA*, and its minimum is *291.6nA*.

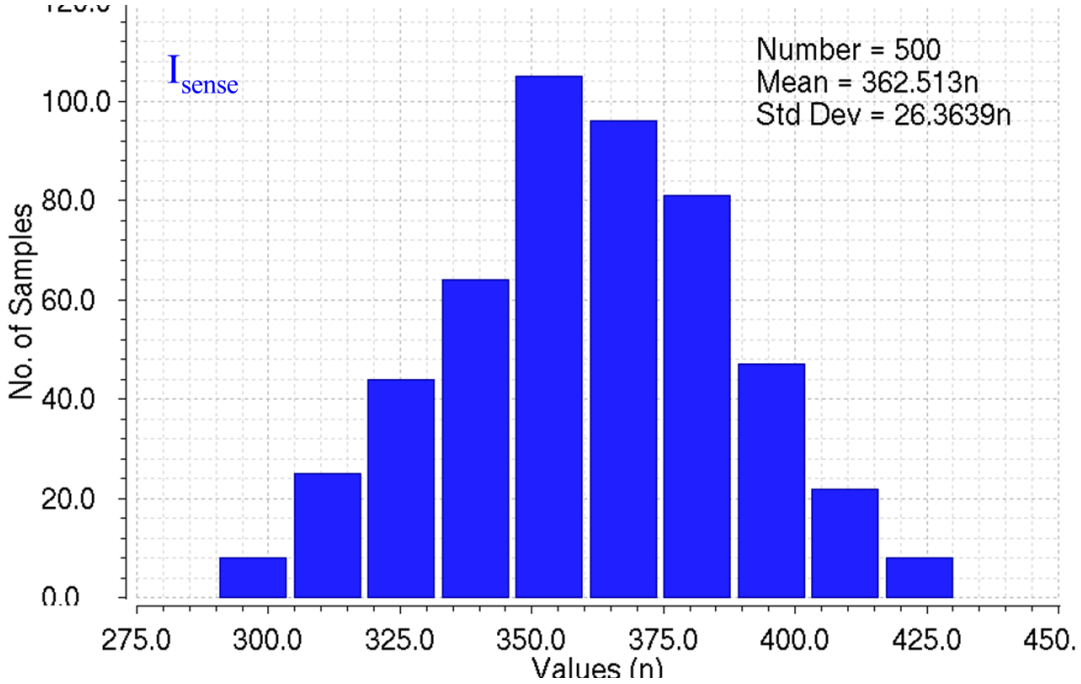

Figure 5.22. Output current of the current sense block – MC histogram.

5.6. Active Diode Comparator

The active diode comparator detects the condition that the inductor current crosses *0A* with the specification of 0V input voltage range, trimmable input offset, typical *20ns* propagation delay, below *8mV 3σ* DC mismatch and below *10µA* quiescent current.

A trimmable input offset specification is given for correcting the input offset mismatches and also more importantly, it is for trimming out the errors resulted due to the

comparator delay. Since the comparator has a delay, it reaches a decision after the coil current crosses zero in real applications. During that time, the coil current enters the negative current region and it decreases efficiency. To prevent this situation, this time is trimmed with input offset trimming so that the coil current never enters the negative current region.

The implementation is shown in Figure 5.23. A resistor string is used in the input stage to implement the trimmability in the input offset. NMOS devices are used as switches to select different values of the resistors to create both positive and negative input offset. The same sized NMOS devices are put to the resistor string as well to compensate the switch resistances. The second stage is for only amplification. The output signal voltage domain is changed from *1.5V* to *5V* to be an input for zero crossing logic.

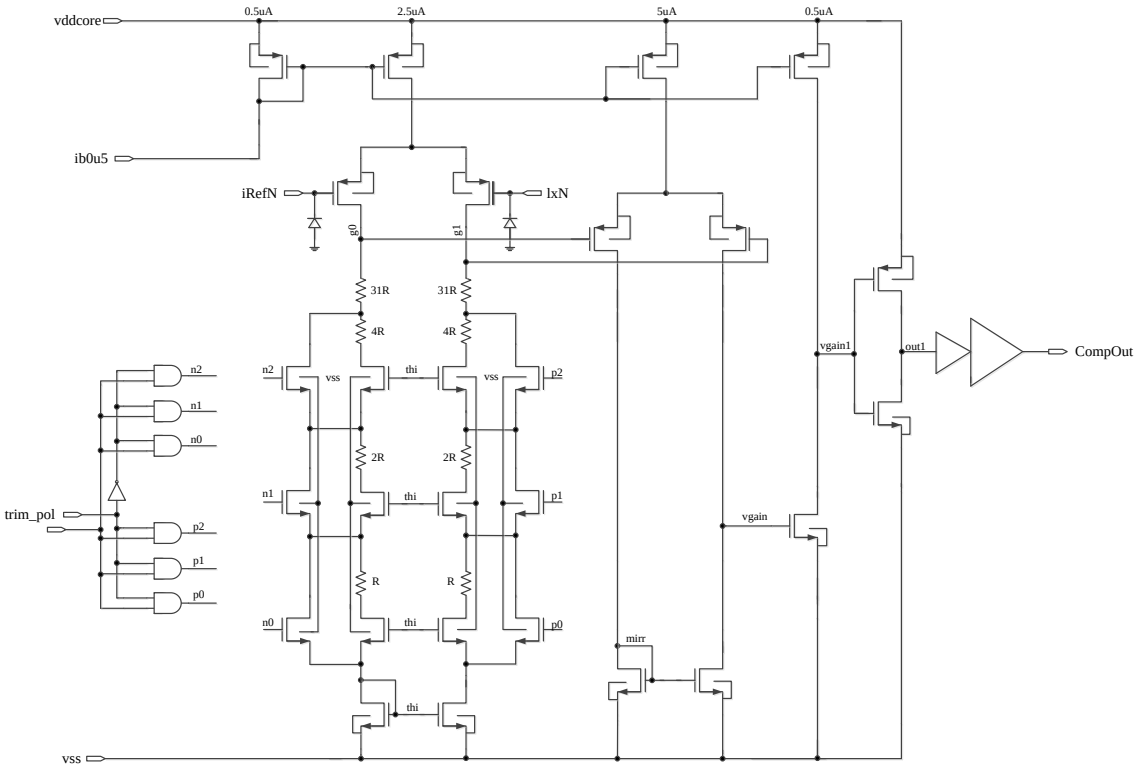

Figure 5.23. Schematic of active diode comparator.

Table 5.7 shows the simulation results of the specification parameters. For the measurement of propagation delays, quiescent and leakage currents, a transient test bench

is used, and for the input offset calculation, a DC test setup is used. As with any comparator, the propagation delay is dependent on the differential input voltage. The results given in Table 5.7 are calculated with *10mV* input difference. However, the *20ns* specification is given for full input range. Therefore, the propagation delay results are worse than the specification since they are only measured in more pessimistic scenario.

Table 5.7. Summary of PVT simulation results of active diode comparator.

Expressions		Value	Corners				
			High Level Supply Voltage (V)	Low Level Supply Voltage (V)	active	Bias Current (nA)	Temp (°C)
t_{prop_rise} (ns)	max	39.5	2.8	1.35	SS	475	0
	min	20.94	2.8	1.65	FF	525	70
	typ	28	3.8	1.5	TT	500	27
t_{prop_fall} (ns)	max	31.46	4.8	1.65	SNFP	475	70
	min	15	2.8	1.35	FNSP	525	0
	typ	20	3.8	1.5	TT	500	27
I_{DDQ} (µA)	max	10.34	4.8	1.65	FF	525	70
	min	8.276	2.8	1.35	SS	475	0
	typ	9.21	3.8	1.5	TT	500	27
I_{DDQ_OFF} (nA)	max	123.7	4.8	1.65	FF	525	70
	min	39.61	2.8	1.35	SS	475	0
	typ	68	3.8	1.5	TT	500	27
Offset (µV)	typ	-720	3.8	1.5	TT	500	27

The trim ranges of the offset are set to cover the MC variation. The *3σ* variation of the offset is *7.97mV* in MC simulations. Therefore, eight *1mV* steps are used for both negative and positive directions. Table 5.8 shows the steps in trim conditions under typical conditions.

Table 5.8. DC Offset under typical condition.

	trim_polarity	
	0	1
off_trim<2:0>	DC Offset under typical conditions	
000	-0.72mV	-0.72mV
001	-1.72mV	0.28mV
010	-2.72mV	1.28mV
011	-3.72mV	2.38mV
100	-4.72mV	3.48mV
101	-5.72mV	4.58mV
110	-6.72mV	5.78mV
111	-7.72mV	6.98mV

Monte Carlo simulation is run to check the possible process and mismatch variations in the offset performance of comparator. The MC simulation is run at the typical corner by choosing the both process and mismatch options in simulator. The resultant histogram of the MC runs can be seen in Figure 5.24. According to the results of MC, the mean of the DC offset is *-0.74mV* and the *3σ* standard deviation is *7.97mV*. The maximum is *6.98mV* and the minimum is *-9.12mV*.

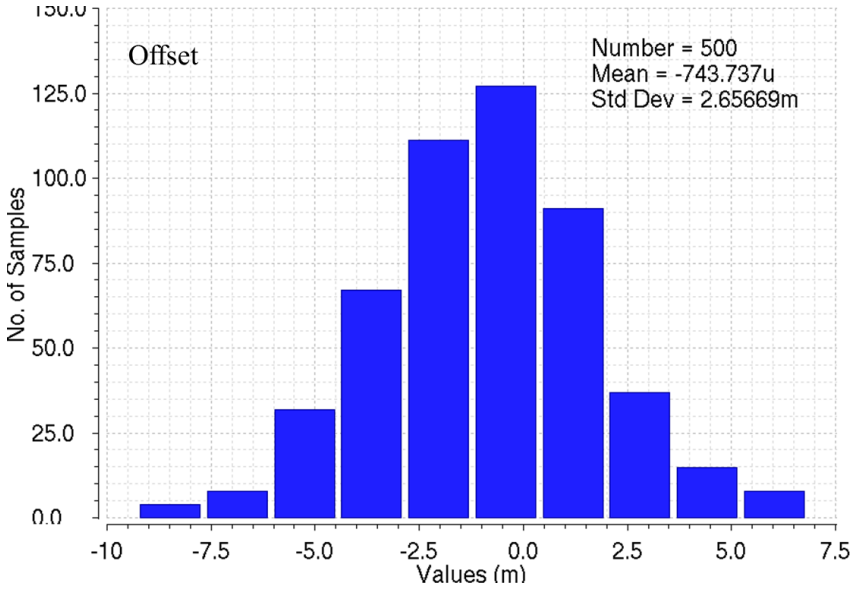

Figure 5.24. MC results of DC offset at typical corner.

6. RESULTS

The main motivation of this work which is improving efficiency in buck converter systems by using adaptive techniques is achieved by doing simulations of the top level design of adaptive output buck converter. The design of buck converter consists of the components described in Section-2. The top level test bench is created to simulate the adaptive output buck design. By starting to build the test bench, it is required to choose the output capacitance and the inductance as a first step since they are put into the test bench as ideal components. A capacitor with *22µF* typical capacitance value is chosen. The actual capacitance is extracted from the datasheet of the capacitor by looking at the DC voltage characteristics of the capacitor that is used as it is shown in Figure 6.1 [78]. At the typical output voltage *1V*, the *22µF* capacitor value degrades to almost *20µF*. Therefore, *20µF* value is chosen as typical capacitance during simulations. On the other hand, the ESR of the capacitor is extracted from the Figure 6.1. At *3MHz* switching frequency which is the switching frequency in this work, the ESR resistance of selected capacitor is about *5m*Ω. This is used as C_{esr} value during the simulations.

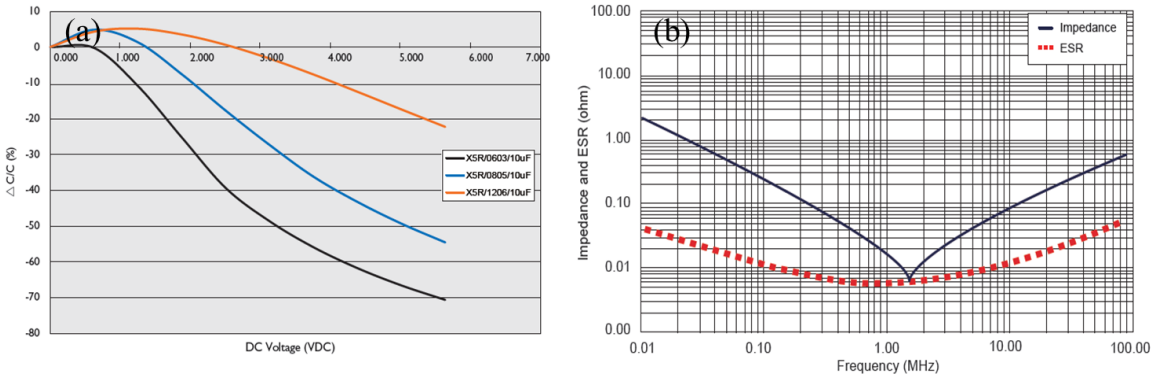

Figure 6.1. C_{out} parameters (a) DC voltage characteristics (b) ESR [78].

The *PIFE25201B* named inductor is chosen among the *1µH* inductor types. Its series resistance is extracted from its datasheet as *50m*Ω. It varies between *45m*Ω and *55m*Ω according to [79]. *1µH* valued inductor is the best choice for *3MHz* switching frequency considering the efficiency [79].

The temperature varies between *0°C* to *70°C* during verifications. After building the test bench, output voltage is verified that buck converter regulates it correctly and the number of the output driver segments should have been increasing accordingly with the optimum efficiency calculations. The number of the segments (*N*) and the corresponding load currents are shown in the Table 6.1.

Table 6.1. Load current vs. segment number.

N	I_{LOAD} (A)
1	1m
1	1.8m
1	3.2m
1	5.6m
1	10m
1	18m
3	32m
5	56m
8	100m
15	180m
26	320m
32	560m
32	1
32	1.8
32	3.2
32	5.6

Figure 6.2 demonstrates a simulation result showing the realization of the implementation. The number of the segments increases while the load current increases. Since everything could not implemented as ideal in the design, the maximum number of segments *(N=32)* is reached when the load current is *536mA* instead of *560mA* as in calculation. The number of segment's decision is made by the current comparator and it makes the decision based upon the capacitive current and resistive current inputs. Figure 6.3 indicates those capacitive and resistive currents and the decision output of the comparator as the number of segments while the load current is increasing.

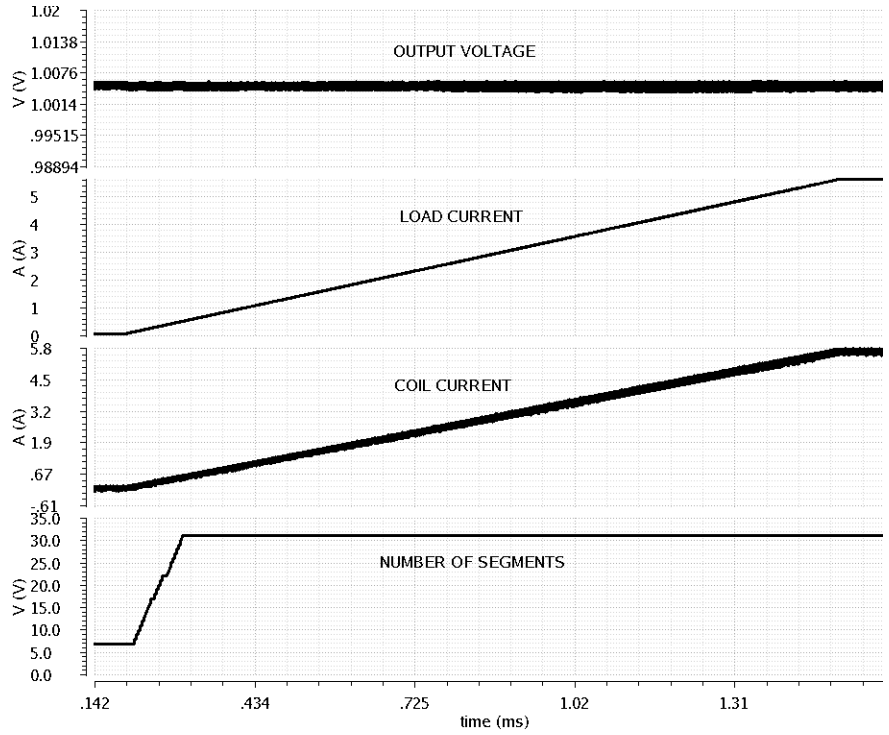

Figure 6.2. Load current ramps from 100mA to 5.6A and N increases.

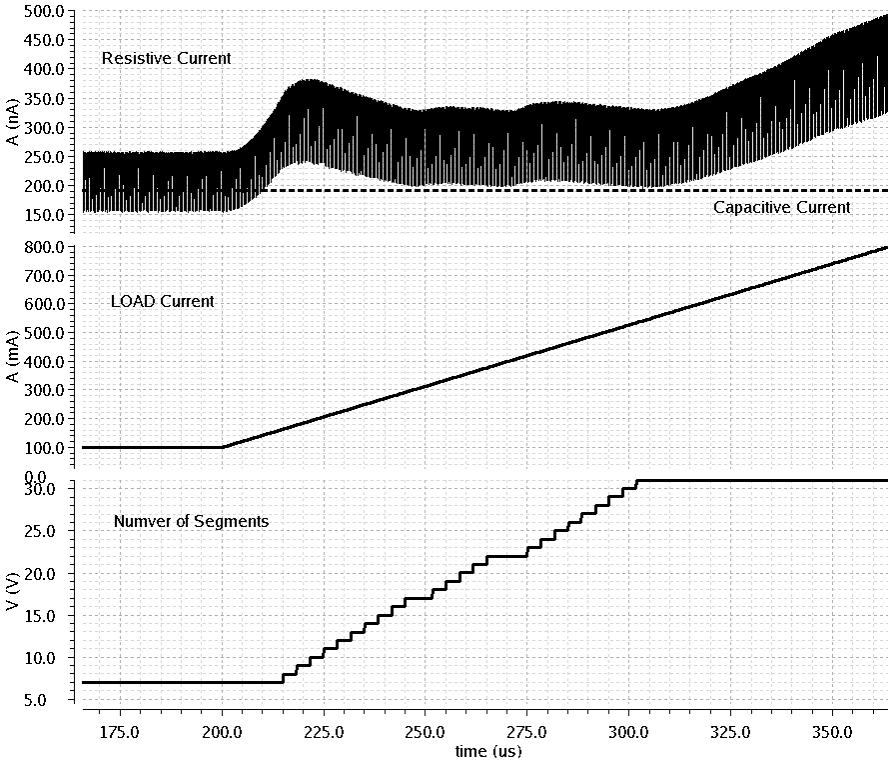

Figure 6.3. N is a result of capacitive and resistive currents comparison.

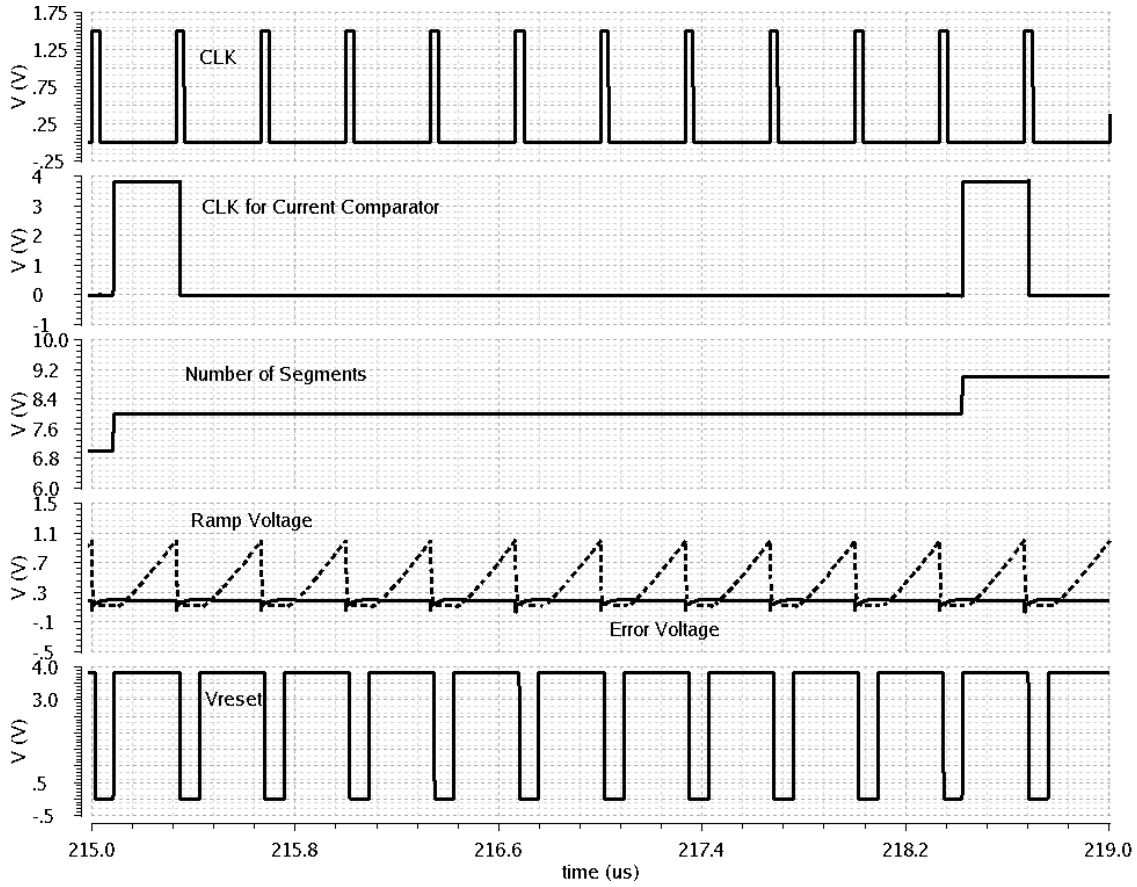

Figure 6.4. Reset signal generation.

The decision of the current comparator is made every ten clock cycles due to the speed concerns of adaptive resistive g_m circuit. It works slower than the switching frequency because of its compensation capacitor inside. Therefore, to be able to make the right decision, the comparator makes that decision with a slower clock which is generated from the switching frequency. Figure 6.4 shows that number of segments *N* increases with every clock cycle of current comparator, not with the clock of buck converter control loop. It also shows the reset signal generation by comparing the ramp voltage and the error voltage.

Active diode circuit is the other implementation in the design which detects the negative current on inductor in falling edge of it, and generates a signal called "*zeroCross*" which is high whenever the inductor current crosses zero. In Figure 6.5, in the falling edge of coil current, when it reaches the zero, the *zeroCross* signal trips high and the gate drive

voltage for the NMOS driver (*gateN*) trips low. The NMOS turns off and during the time of both NMOS and PMOS are off, the circuit is in tristate such that the coil current and *LX* voltage makes oscillatory behaviour. This is a normal behaviour in the tristate region.

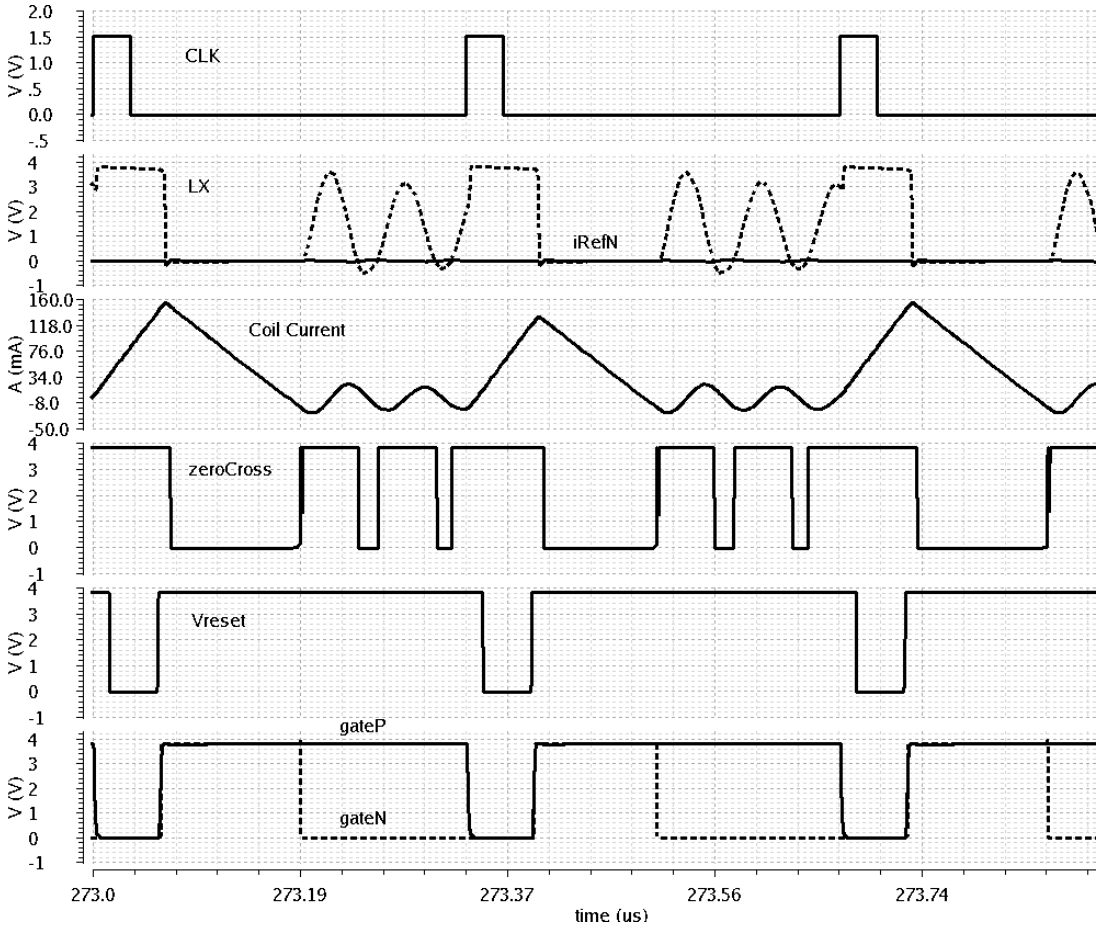

Figure 6.5. Zero cross comparator output in light load condition.

Zero crossing scheme and active diode comparator are crucial for adaptive output buck converter design since this scheme is necessary for increasing efficiency such that there is efficiency loss when NMOS conducts negative currents.

Efficiency (η) can be calculated such that:

$$\eta = \frac{V_{out} I_{LOAD}}{V_{DD} I_{DD}} \tag{6.1}$$

where V_{out} is the output voltage of buck converter, I_{LOAD} is the load current, V_{DD} is the supply voltage and I_{DD} is the total quiescent current of buck converter.

By using the load current values and quiescent current information extracted from the ramping up the load current simulation, the efficiency information is generated over the load currents. Figure 6.6 shows a comparison between adaptive output stage buck converter and a fixed output buck converter whereas Figure 6.7 indicates the efficiency of adaptive output buck converter extracted from simulations.

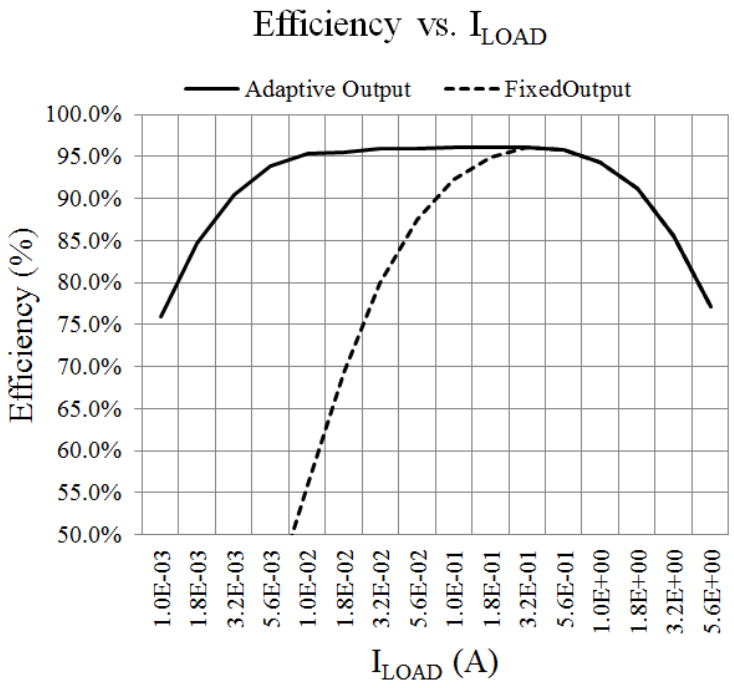

Figure 6.6. Comparison of the efficiencies.

It is seen from the Figure 6.6 and Figure 6.7 that the efficiency plots of adaptive buck converter calculation and simulation differ to each other. In real implementation, efficiencies are a little bit lower compared to the calculation graph. This is a normal situation considering the fact that some non-idealities exist in implementation. Those non-idealities can be resolved in future implementations by improving the circuit more. However, the design is still better in terms of efficiency in light loads compared to every other design in literature. The various designs in literature are investigated thought out this work and as a result a comparison is given in Table 6.2.

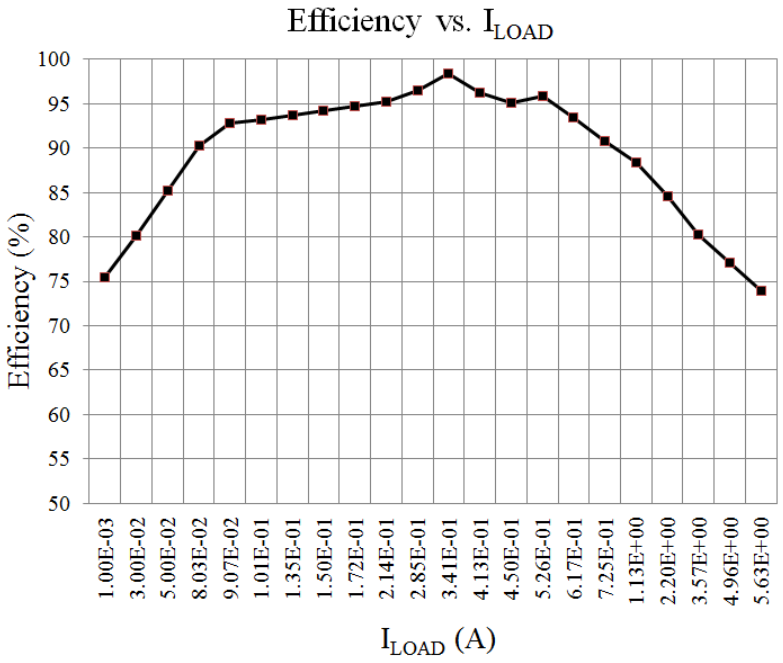

Figure 6.7. Efficiency of designed adaptive buck converter over the loads.

Table 6.2. Comparisons between the proposed method and the prior arts.

	This Work	[23]	[29]	[32]	[53]
Inductor	1μH	10μH	1μH	22μH	N/A
Capacitor	20μF	47μF	4.7μF	22μF	N/A
Input Voltage	2.8V-4.8V	2.8V-5.5V	3V-4.5V	3.3V	5V
Output Voltage	0.9V-1.1V	1V-1.8V	1.8V	1.8V	N/A
Maximum PWM switching frequency	3MHz	1.5MHz	5MHz	1MHz	1MHz
Efficiency at 10mA Load Current	85%	65%	55%	70%	55%

7. CONCLUSION AND FUTURE WORK

7.1. Conclusion

In this study, importance of the efficiency of buck converters in a portable system and methods for increasing efficiency are explained in a switching buck converter. Power loss mechanisms and efficiency increasing methods for light load and heavy load are explained separately and differences between them are discussed. The previous works in the literature to improve efficiency such as Pulse Frequency Modulation (PFM), Pulse Skip (PS), Burst Mode Control (BM), Adaptive Gate Swing (AGS), Resonant Gate Driver, Charge Recycling, Segmented Power Stage (SPS) and Adaptive Dead Time techniques are briefly explained and the advantage of proposed work over all those methods is pointed out. Because all of the other previous methods and mechanisms work on the principle of changing the modulation scheme or frequency basically, the mode of the operation by leaving the Pulse Width Modulation (PWM), this method is a novel one in terms of staying in the PWM mode for light load operation as well. Not to change frequency and modulation scheme over the load currents gives a simplest solution. To be able to stay in PWM mode, the method takes into account the input voltage variation, operating frequency, gate capacitance of the unit driver, the actual R_{ON} information and the load current itself. Optimum output stage size is obtained to produce optimal efficiency in switching buck regulator.

The decision of optimum stage size is given by using adaptive techniques. The capacitive and resistive currents are produced by adaptive g_m cells which can perform multiplication and division. Some circuit tricks are used to have more realistic information in inputs of adaptive g_m circuits since the adaptive g_m blocks are very critical in terms of being calculation mechanisms for capacitive and resistive powers. The optimum number of the segments in the output stage/pass transistors for maximum possible efficiency is decided based upon the current information from adaptive capacitive and adaptive resistive g_m blocks.

The method proved itself according to its results and comparisons to the other prior arts in terms of efficiency in light load regions. The comparison is made at 10mA load current in every work in the literature which is a small load current symbolizing light load condition, and *15%* efficiency improvement is obtained in this work comparing the closest efficiency in prior arts at given light load current.

7.2. Future Work

Although the adaptive output stage buck converter design works in terms of segmentation and finding the optimum number of stages in the output for high efficiency, further optimization of the design can be made. The line and load transient specifications are not given in this work since the adaptive output stage buck converter design is slow against fast load transitions due to its nature. It increases the number of segments against increasing load current. However, circuit does it by increasing the segment number one by one. Therefore, it is slow for a fast load step. Line and load transient performances can be improved in the future by adding another comparator called panic comparator to the design such that in case of a fast load transition, the buck converter does not rely on adaptive resistive and capacitive g_m block's decisions and current comparator response; it relies on panic comparator's decision. Further than that, some more operational modes can be added to the design as well. For instance, there can be an option to be able to enter sleep mode.

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