INTEGRATED ULTRA-WIDEBAND RECEIVER SYSTEM AND ANTENNA DESIGN

by

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INTEGRATED ULTRA-WIDEBAND RECEIVER SYSTEM
AND ANTENNA DESIGN

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ABSTRACT

INTEGRATED ULTRA-WIDEBAND RECEIVER SYSTEM AND ANTENNA DESIGN

Ultra wideband (UWB) is one of the important technologies among the communication types, which is able to reach high data rate in short distances. Wireless personal area networks and wireless sensor networks are the primary of the application areas of this technology. The aim of this thesis is to design a receiver integrated circuit (IC) which is able to work at high data rates, by using UWB technology. The transmitter IC working in collaboration with the receiver IC, is designed by the other members of the project group. The required literature survey is done in order to have a receiver IC to work properly. As an architecture, energy detection type non-coherent impulse radio UWB system is selected because of its relatively smaller complexity. In circuit design phase, the circuit topologies that have proper results in the literature, are determined and among all these topologies, the low noise amplifier (LNA), integrator and comparator circuits are designed with the simulation programs. The layouts of the designed circuits are drawn with UMC's 130 nm complementary metal oxide semiconductor (CMOS) technology for the manufacturing. Moreover, for the measurement purpose of the previously designed IC, a printed circuit board is designed. A research on microstrip line structures is done in order to comply with the properties of the receiver IC and also the theoretical data is supported by the simulation results. As a conclusion, an UWB antenna which maintains the communication between transmitter and the receiver, is designed.

ÖZET

TÜMLEŞİK ULTRA GENİŞBAND ALICI SİSTEM VE ANTEN TASARIMI

Ultra genişband (UGB) kısa mesafede yüksek veri hızlarına ulaşabilen iletişim şekilleri içinde hatırı sayılır teknolojilerden biridir. Kablosuz kişisel alan ağları ve kablosuz algılama sistemleri bu teknolojinin uygulama alanlarının başında gelirler. Bu tezde, UGB teknolojisi kullanılarak yüksek veri hızlarında çalışabilen bir alıcı tümdevre tasarlanması amaçlanmıştır. Alıcı tümdevresinin beraber çalıştığı verici tümdevresi ise proje ekibinin diğer üyeleri tarafından tasarlanmıştır. Alıcı tümdevresinin istenilen şekilde çalışması için gerekli literatür çalışmaları yapılmıştır. Mimari olarak görece daha az kompleks olduğundan, enerji saptamalı bir uyumsuz dürtü radyo UGB sistemi seçilmiştir. Devre tasarım aşamasında daha önce uygun sonuçlar vermiş devre yapıları belirlenmiş ve bu yapılardan düşük gürültülü yükselteç, integral alıcı devre ve karşılaştırıcı devreleri benzetim programlarıyla tasarlanmıştır. Tasarlanan devrelerin serimleri, üretimi için United Microelectronics firmasının 130 nm bütünleyici metal oksit yarıiletken teknolojisi ile çizilmiştir. Buna ek olarak, daha önce üretilen tümdevrenin ölçümü için baskılı devre kartı tasarımı yapılmıştır. Tasarım aşamasında tümdevrenin özelliklerini bozmadan çalışmasına imkan verecek şekilde farklı tip mikroşerit hat yapıları üzerinde araştırma yapılmış ve teorik veriler benzetim sonuçlarıyla desteklenmiştir. Son olarak, alıcı ve verici arasındaki haberleşmeyi sağlayan bir UGB mikroşerit anten tasarlanmış ve üretilmiştir.

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LIST OF SYMBOLS

C_{gs}	Parasitic gate to source capacitance of the transistor
f_H	Upper cutoff frequency
f_L	Lower cutoff frequency
g_m	Transconductance of the transistor
I(z)	Current at node z
L	Length of the transistor
L_g	Series gate inductor
L_{load}	Load inductor
L_s	Source inductor
NF_{min}	Minimum noise figure
R_n	Noise resistance
r_o	Intrinsic output impedance
tanδ	Dielectric constant
V(z)	Voltage at node z
V_{ov}	Overdrive voltage of the transistor
V_t	Threshold voltage of the transistor
W	Width of the transistor
Z_{in}	Input impedance
Z_{out}	Output impedance
Z_s	Source impedance
α	Attenuation constant
α_c	Conductor loss
α_d	Dielectric loss
β	Propagation constant
γ	Complex propagation constant
Γ	Reflection coefficient
ϵ_{eff}	Effective relative permittivity
ϵ_r	Relative permittivity

λ	Wavelength of the wave
ν_p	Phase velocity

LIST OF ACRONYMS/ABBREVATIONS

ADC	Analog to Digital Converter
BPSK	Binary Phase Shift Keying
CDM	Charge Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DFF	D Type Flip Flop
EIRP	Equivalent Isotropically Radiated Power
ESD	Electro Static Discharge
FCC	Federal Communication Commission
HBM	Human Body Model
IQ	In-phase Quadrature-phase
IR	Impulse Radio
LCP	Liquid Crystal Polymer
LNA	Low Noise Amplifier
MB-OFDM	Multi Band – Ortogonal Frequency Division Multiple Access
NF	Noise Figure
PCB	Printed Circuit Board
PTFE	Polytetrafluoroethylene
SNR	Signal to Noise Ratio
SWR	Standing Wave Ratio
UMC	United Microelectronics Corporation
UWB	Ultra Wideband
VGA	Variable Gain Amplifier

1. INTRODUCTION

Ultra Wideband (UWB) is an exciting new wireless technology that promises high data rates over short distances. The UWB system is considered as a system whose bandwidth is in the same order of magnitude as its center frequency and whose power spectral density (PSD) is low. There are several definitions of UWB resulting from the various regulations approved. However, according to the widely known definition, any wireless communication technology that produces signals with a bandwidth which is wider than 500 MHz or with a bandwidth to center frequency ratio (the fractional bandwidth) that is greater than 0.2, can be considered as UWB. The main advantage of UWB is to be an unlicensed system and generally it is used in collaboration with other licensed or unlicensed narrowband systems. Therefore, some power limitations are needed for the UWB system.

The application areas of UWB are mostly in Wireless Personal Area Networks (WPANs), wireless sensor networks and remote telemetric systems. In addition, , the remote monitoring devices and telemedicine solutions are realized on the basis of UWB technology in medical applications. The signal produced within the UWB standard is capable of travelling through many kinds of materials and therefore it allows the design of through-wall imaging and radar imaging systems with high accuracy and resolution. Similarly, accurate ranging capability due to the excellent time resolution property, can be used for vehicular radars such as parking assistant systems in automotive industry.

In recent UWB systems, the designers deal with several specifications such as power, data rate, and accuracy according to the architecture of the transceiver. However, it should be well known which block in a transceiver has the strongest effect over the related specification.

The aim of this thesis is to design long range, high data rate IR-UWB receiver. During the thesis, the main focus is on are Low Noise Amplifier (LNA), integrator and comparator blocks. The circuit topologies with low power and high gain are selected to

form the IR-UWB receiver. In this context, a literature survey is done for all designed blocks.

At the beginning of this thesis, the first consideration was understanding the transmission line behaviour at high frequencies in order to reduce the off-chip effects on the received signal. The material analysis which will be used in the printed circuit board (PCB), is then performed because the appropriate substrate determines the design of the transmission line.

Different types of transmission line structures are analyzed, because of the high sensitivity of RF PCB to the impedance mismatches. Impedance transformers, transition networks and single traces are simulated and the RF PCB was designed according to the attained results.

By following almost the same route as PCB design, the UWB antenna which almost covers the band of interest with its sufficiently well out-of-band rejection, is designed. The results are interpreted including the electromagnetic simulations.

In the analog design phase, the main blocks of the receiver were researched in the literature. Before hand calculations and simulation results, design specifications were selected in order to form a long range, high data rate receiver. The most common topologies were determined for each block and the circuits were designed to satisfy the predetermined requirements.

The simulations for the LNA were performed for both pre-layout and post-layout. According to the amplitude of the incoming signal, the gain of the LNA was made variable. The integrator and comparator are the baseband blocks, thus gain is not considered as much as the RF blocks. The comparator topology was determined to have the hysteresis property in order to increase the accuracy in detection of the received signal.

In section 2, the basic idea of the UWB technology is covered from different angles such as advantages and challenges. In the following section, the selected receiver architecture is briefly explained and some details about the the blocks are presented. In

section 4, the analog blocks which consist of the LNA with two different topologies, integrator and comparator, are analyzed in detail and supported with the simulation results. Various types of transmission lines and PCB substrates are considered to design low loss RF PCB in Section 5. Section 6 includes detailed information about the designed UWB antenna and the comparison between the reference, commercial and off-chip antennas. Finally, Section 7 covers the overall interpretation of the system.

2. ULTRA-WIDEBAND (UWB) TECHNOLOGY

A wireless system is called UWB, if its bandwidth is greater than 500 MHz or its fractional bandwidth is larger then 0.2. Fractional bandwidth is defined as the ratio of the signal bandwidth to the center frequency of the corresponding signal as shown in Equation 2.1 and Figure 2.1.

$$\text{Fractional BW} = \frac{f_H - f_L}{2} \tag{2.1}$$

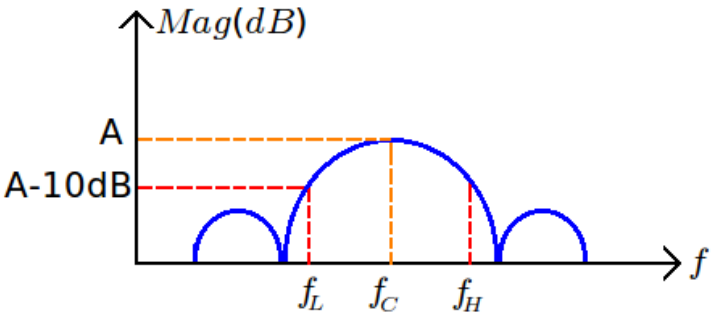


Figure 2.1. Fractional bandwidth.

Frequency bands 0 - 960 MHz, 3.1 - 10.6 GHz and 22 - 29 GHz are allocated as unlicensed bands for UWB with spectrum limitation of equivalent isotropically radiated power (EIRP) which is the product of the power supplied to the antenna and the antenna gain in a given direction relative to anisotropic antenna, (maximum -41.3dBm/MHz) according to Federal Communication Commission (FCC) [1] as shown in Figure 2.2. 0-960 MHz band is allocated for medical imaging and radar related applications such as through wall imaging and ranging. 22 - 29 GHz band is used for automotive radar. 3.1 GHz - 10.6 GHz band is used for multiple purposes including communications, radar, imaging and ranging.

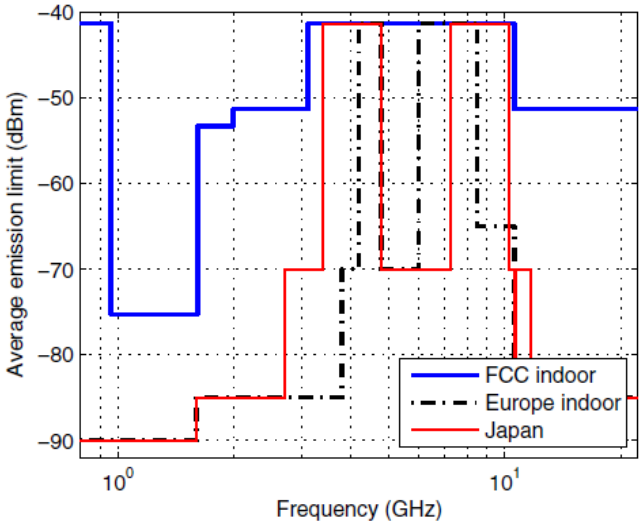


Figure 2.2. Spectrum limitation [1].

Research is focused on the lower section (3.1 GHz-5 GHz) of the 3.1-10.6 GHz band. There are mainly two methods for realizing UWB spectrum. These are called multi-band orthogonal frequency division multiple access (MB-OFDM) and impulse radio (IR) methods.

In MB-OFDM UWB technology the 3.1-5 GHz band is divided in three 528 MHz subbands. There is a hopping structure involved in this architecture such that the signal is transmitted sequentially from these three 528 MHz bands. The 528 MHz band is further divided into 4.125 MHz bands by utilizing the 128 point IFFT/FFT cores in the transceiver. The MB-OFDM method can only be used for communication purposes because of continuous sinusoidal signaling [2].

In IR-UWB method, very short duration (on the order of nanoseconds) pulses are used. These pulses have very large bandwidth in the spectrum, thus becoming UWB signals. IR-UWB system can be used in a variety of applications including communication and radar because of its pulse signaling scheme.

Coherent and non-coherent UWB transceiver systems can be used for IR-UWB. VCO or template based pulse generation methods are used for coherent detection, and it is also necessary to use coherent systems if a BPSK modulation or IQ modulation is selected for the transceiver.

On the other hand, non-coherent systems are less complicated and involve fewer components compared to coherent systems. However, the synchronization part is challenging in non-coherent systems. For reduced complexity and power consumption, it is better to use a non-coherent system. In this thesis, energy detection method which is composed of a mixer (squarer) and integrator is selected for IR-UWB receiver system.

3. UWB RECEIVER ARCHITECTURE

3.1 Non-Coherent IR-UWB Receiver Architecture

Recent designs for UWB systems can be classified into IR-UWB and OFDM based UWB. OFDM based UWB architectures are suitable for high data rate communication; however, IR-UWB is a suitable solution for low rate and low power applications such as wireless sensor networks. For IR-UWB receivers, coherent and non-coherent architectures have been reported in the literature [3]. OFDM needs many timing synchronization circuit blocks, which increases system complexity. On the contrary, IR-UWB architecture provides non-coherent signaling which is employed to reduce power consumption on the receiver along with a simpler architecture without any high frequency clocks except for integration windowing as will be covered later.

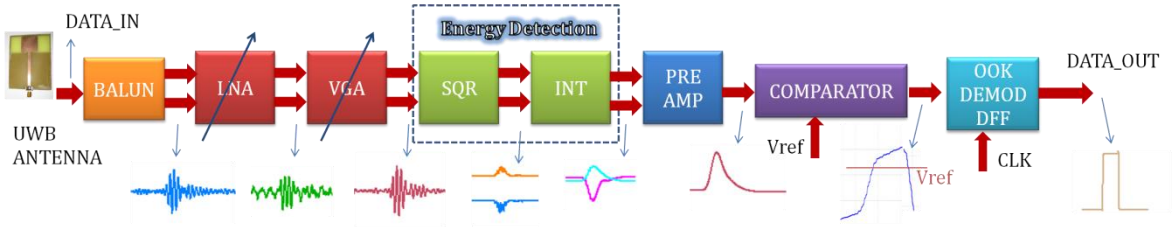


Figure 3.1. Non-coherent IR-UWB Receiver Block Scheme.

The non-coherent IR-UWB receiver architecture is shown in Figure 3.1. Before determining the specifications of the receiver, the operating distance is a key parameter which should be taken into account. Long distances between the transmitter and the receiver mean that RF signal arriving at the antenna will have a comparable noise signal in amplitude.

When the RF front end is integrated on the same chip with the digital logic and baseband analog circuits, the switching noise resulting from the digital circuits and the noise generated by the analog blocks distort the UWB signal. Thus differential circuits are required to minimize these effects. A differential architecture brings some significant advantages in terms of substrate noise and power supply immunity. For instance,

harmonics of low-frequency signals can more easily couple into the other circuitry in single ended architectures and these harmonics cause instability and distortion in the band of interest. By employing a differential architecture, common mode noise signals no longer affect the RF signal with high CMRR amplifier structures. On the other hand, as a drawback of differential structures, power consumption and chip area double. These disadvantages are acceptable because of the many benefits mentioned above. Therefore, all analog blocks are designed in differential form except for the continuous comparator, digital demodulator and off-chip balun.

In the receiver chain, the first passive component is the off-chip balun. The incoming UWB signal has to be converted to differential form in order to be applied to the differential front-end of the receiver. Balun performance plays a significant role in overall system, because the incoming signal having low amplitude and high noise, first comes across the balun. The balun which is a passive device, should have low amount of loss in order to transfer the signal to the following block with minimum attenuation.

The differential signal at the output of the balun, is applied to the Low Noise Amplifier (LNA) in order to reduce the noise contribution of the active device within the band of interest. The LNA is simply an amplifier which has the most significant property of being low noisy. Because of that, it is at the front of the receiver. The noise contributions of the following blocks and the overall system directly depend on the gain of the LNA. In cascaded systems this effect can be explained with (4.4) as will be covered later.

In non-coherent receivers, considerably large gain is required prior to the mixer to obtain a sufficient signal swing. Mixers require input voltages on the order of mV whereas LNA input voltages can be on the order of tens of μV; thus, voltage gain of approximately 40 dB is needed before the mixer. To realize such large gains, noncoherent receivers typically employ gain adjustable multi-stage linear amplifiers called Variable Gain Amplifiers (VGA). Imagine that a wireless projector system is communicating with a laptop as an application of this chip. The distance from the laptop to the projector inside the room is not the same all the time. If the laptop stands far away, the received signal will become weak. To be able to process this signal, the voltage levels must be increased. At

this point, the operation of the VGA becomes meaningful. By adjusting the control voltage of the VGA, the amplitude of the signal is set to a value which enables the signal to be detected by the comparator. In some applications, the control of the VGA is performed automatically. However, this situation needs extra circuitry because the instantaneous power at the output of the VGA is changing as the distance changes. A feedback mechanism helps to keep the power constant at the output of the VGA according to the amplitude of the incoming signal which is adjusted by the control voltage. This mechanism is also known as Automatic Gain Control (AGC).

The front-end of the receiver is followed by the energy detection (ED) part. ED mainly describes the non-coherent receiver architecture [4]. The amplified signal at the output of the VGA is still differential and in order to detect the energy, the signal must be multiplied by itself. Then the resulting waveform must be transferred to an integration phase that basically uses a charging capacitor.

Multiplication of the signal by itself is performed by a mixer. The signal level at the mixer output is quite small because the signal at the input is squared at the output and the resulting output peak-to-peak voltage is on the order of tens of μV. The amplitude of this baseband signal is proportional to the instantaneous received power within the bandwidth of the incoming RF signal. By integrating the baseband signal over a period of time, the receiver forms a signal proportional to the energy received over that period of time which can be demonstrated by a charging capacitor in the integrator.

After the energy detection phase, the next step is detection of the signal by using a comparator. In order to convert the differential signal to single-ended form and increase the sensitivity of the comparator, an additional single-ended differential amplifier is needed. It also acts as a gain block after the mixer.

As a consequence, the D-type Flip Flop (DFF) demodulates the signal with the same clock which is used in generating the modulated signal in the transmitter. At this point, the accuracy of the demodulated data has a strong dependence on the clock frequency. For higher values of the clock frequency, the demodulated signal is closer to the original data.

4. ANALOG DESIGN OF IR-UWB RECEIVER

4.1. Low Noise Amplifier

4.1.1. Basic RF Concepts of a Low Noise Amplifier

Low noise amplifier (LNA) is the most crucial block in the designed receiver and a typical component used regularly in wireless receivers. It takes place most commonly after the antenna, as the first block of the front-end, as shown in Figure 3.1. The basic operation of an LNA is amplification while adding a small amount of noise owing to out-of-band rejection property of itself.

4.1.1.1. Signal-to-Noise Ratio and Noise Figure. The performance of most RF and microwave communication systems strongly depends on the noise because it represents the threshold for the minimum signal which can be reliably detected by the receiver. The noise signal couples into the LNA from the external environment through the antenna at the receiver, as well as being generated internally by the LNA circuitry. The externally introduced noise is amplified within the band of interest. Nevertheless, the in-band noise contribution of the LNA should be minimum. This situation is maintained when the noise figure of the LNA is as low as possible within the operation bandwidth. In order to understand the physical meaning of noise figure we have to define the term signal-to-noise ratio (SNR). SNR gives a measure on the amount of purity of a signal. The definition can be written as,

$$\text{SNR} = \frac{\text{Available Signal Power}}{\text{Available Noise Power in Signal Bandwidth}}. \tag{4.1}$$

When the noise and the data signal are applied to the input port of a noiseless network, the signal and the noise will be amplified or attenuated by the same factor so that the SNR of the output of the network will be unchanged. However, if the network is noisy, the output noise power will be increased more than the output signal power, so that the

output signal-to-noise ratio will be reduced. The noise factor, F, is a measure of this reduction in signal-to-noise ratio, and is defined as

$$F = \frac{S_I/N_I}{S_O/N_O} = \frac{P_{AV,S}/P_{AV,N}}{G.P_{AV,S}/(G.P_{AV,N} + G.P_{AV,EN})} = \frac{P_{AV,N} + P_{AV,EN}}{P_{AV,N}} \geq 1 , \qquad (4.2)$$

where S_I and N_I are the input signal and input noise, respectively. $P_{AV,S}$, $P_{AV,N}$ are the input noise powers. S_O, N_O are the output signal and output noise, respectively. G is the gain of the amplifier. $G.P_{AV,EN}$ is the excess noise power resulting from the amplifier itself. Hence, noise factor can be thought as the total output noise divided by the output noise resulting from the noise power of the input source. In practice, the term “noise figure” is preferred to “noise factor”, because of the fact that the units of the gains and the losses in RF systems are in terms of dB for the most of the cases as given in Equation 4.3 [5].

$$\text{Noise Figure} = 10\log(F) \qquad (4.3)$$

From a wider point of view, the individual effects of the noise figures of each block are not sufficient to represent the overall receiver performance, because all blocks are cascaded to form the receiver itself. Thereby, the relationship between the noise figure and the gain should be stated. In a receiver chain, the noise generated by the final block is referred to the preceeding block by dividing its noise figure by the gain of this block. This yields the overall noise figure of the cascaded blocks as follows

$$F_{TOT} = F_{LNA} + \frac{F_{afterLNA} - 1}{G_{LNA}}. \qquad (4.4)$$

Equation 4.4 covers the noise figure of a cascaded system including LNA and the rest of the receiver. Additionally, it can be observed that the noise figure of the LNA dominates the overall performance and this situation makes the LNA’s noise contribution significant.

4.1.1.1. Scattering Parameters. In RF circuits, especially for wideband applications, , the reflections on the data will cause a distortion and limit the data rate as illustrated in Figure 4.1, because the transmitting data is narrow in time domain. Besides this parameter, there are many other quantities such as power gain, isolation etc. which should be taken into account in the design procedure of an RF circuit. All these parameters are described by the scattering parameters.



Figure 4.1. Reflections on a wideband signal.

A practical problem exists when trying to measure voltages and currents at microwave frequencies because direct measurements usually involve the magnitude (inferred from power) and phase of a wave traveling in a given direction, or of a standing wave. Thus, equivalent voltages and currents, and the related impedance and admittance matrices, become somewhat of an abstraction when dealing with high-frequency networks. A representation more in accordance with direct measurements and with the ideas of incident, reflected, and transmitted waves, is given by the scattering matrix.

The scattering matrix provides a complete description of the network as seen at its N ports and also relates the voltage waves incident on the ports to those reflected from the ports. For the sake of clarity, s-parameters will be covered from the point of view of two port network theory.

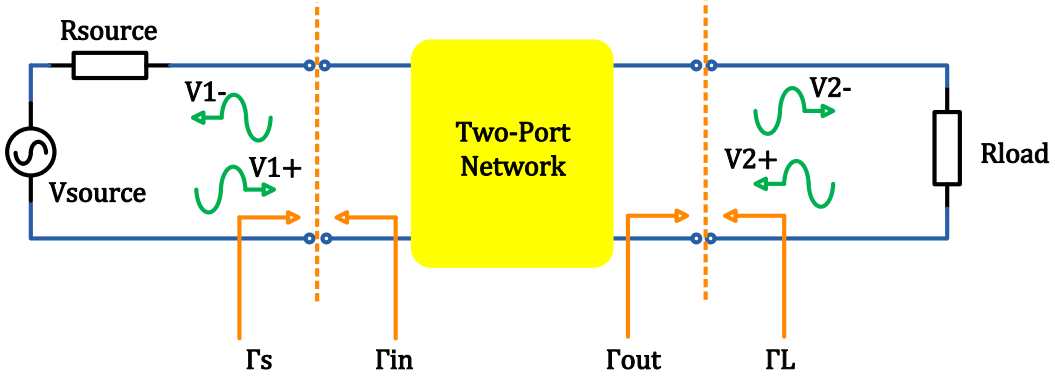


Figure 4.2. Incident and reflected waves on two port network.

In Figure 4.2, a two port network is presented in order to explain the travelling of waves. The green arrows in Figure 4.2 represent the waves while the sign of a wave refers to the directions such that V_n^- is the amplitude of the voltage wave reflected from port n, similarly V_n^+ is the amplitude of the voltage wave incident on port n. The term Γ refers to the reflection coefficient. The s-matrix for a two port network can be written in matrix form in Equation 4.5 and also in terms of incident and reflected waves in Equation 4.6 and 4.7 as follows

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}, \tag{4.5}$$

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ , \tag{4.6}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ . \tag{4.7}$$

Hence, the above two equations, Equation 4.6 and 4.7 allow us to write the s-parameters in terms of reflected and incident waves as in Equation 4.8.

$$S_{11} = \left. \frac{V_1^-}{V_1^+} \right|_{V_2^+=0} \tag{4.8}$$

S_{11} can be equalized to the reflection coefficient seen at port 1 when port 2 is terminated in a matched load ($V_2^+=0$).

$$S_{21}=\left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} \tag{4.9}$$

S_{21} can be found by applying an incident wave at port 1, V_1^+ and measuring the outcoming wave at port 2, V_2^-. This is equal to the transmission coefficient from port 1 to port 2. Additionally, S_{21} corresponds to the power gain for active devices such as amplifiers and insertion loss for passive devices such as baluns etc.

An important point which should not be confused is that these two input port s-parameters correspond to reflection and transmission coefficients as long as the ports are matched. In other words, the reflection coefficient looking into the port 1 is not equal to S_{11}, unless the ports are matched.

For passive networks $S_{11} = S_{22}$ and $S_{21} = S_{12}$ resulting from the bilateral operation. However, in active devices S_{22} and S_{21} show a different behaviour because of the unilateral operation of the amplifiers. In practice, S_{12} is the reverse isolation parameter and S_{22} also represents the amount of reflection which refers to the matching at the output port.

In RFIC design, the reflection parameter S_{11} is most commonly kept less than -10 dB. This is an upper limit for the reflection which can be tolerated. For higher values of S_{11}, the reflections shown in Figure 4.1, become dominant over the data signal and it becomes difficult to distinguish the original data from the reflections.

The reflection coefficients demonstrated with orange arrows in Figure 4.2 refer to impedance mismatches. The physical meanings of these parameters are as follows,

- Γ_{in} = Reflection coefficient looking toward the generator (or the input matching network)
- Γ_s = Reflection coefficient looking toward the input of the amplifier
- Γ_L = Reflection coefficient looking toward the output of the amplifier
- Γ_{out} = Reflection coefficient looking toward the load (or the output matching network)

Γ_x is defined as $\frac{Z_x - Z_0}{Z_x + Z_0}$, where Z_0 is the characteristic impedance of the network and all these parameters can be written in the same manner. However, we can also write Γ_{in} and Γ_{out} in terms of s-parameters in Equation 4.10 and 4.11.

$$\Gamma_{in} = \frac{V_1^-}{V_1^+} = S_{11} - \frac{S_{12}S_{21}\Gamma_L}{1 - S_{21}\Gamma_L} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{4.10}$$

$$\Gamma_{out} = S_{22} - \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \tag{4.11}$$

4.1.2. Design of a Low Noise Amplifier

The design procedure of the LNA is carried out by trying to achieve specifications like low noise figure, flat gain, out-of-band rejection etc. However, bandwidth is the key property to decide the circuit topology for UWB operation. The definition of low noise, intuitively gives an idea on the basic block diagram of the LNA which consists of an amplifying stage and matching network.

For narrowband LNAs, inductive degeneration is widely used based on the fact that the amplifier is terminated using an inductor at the source of the amplifying transistor which yields a narrowband matching at the center frequency [6]. On the other hand, for wideband LNAs, this topology still can be a solution with an additional wideband matching network. However, in wideband applications, distributed amplifiers provide a flatter response for a wider frequency range but relatively high power dissipation and large chip size are drawbacks for the implementation of this topology [7].

4.1.2.1. Matching Network. The input of the LNA should be matched to the output of the filter following the antenna to prevent the incoming signal from reflecting back and forth between the LNA and the antenna. Actually, the filter preceeding the LNA turns out to be a matching network placed between the LNA and the antenna.

The matching network can be defined as a transformer circuit which matches the input and the output impedances by considering the minimum insertion loss. However, the

aim of the matching determines the topology. There are three matching types having their specific targets.

Impedance matching is a term which is mostly used in transmission lines. As will be covered in Section 5, a transmission line is characterized by a characteristic impedance of Z_0 and a termination impedance of Z_L. The reflection of the wave is a function Z_L-Z_0 therefore, for the case $Z_L = Z_0$, no reflection occurs.

The widely preferred type of matching is power matching which is based on power efficiency. Assume that, a voltage source V_S with a source impedance Z_S drives a load of Z_L. For the value of $Z_L = Z_S$*, the maximum power dissipated in the load is as follows

$$P_{MAX} = \frac{V_S}{4Re(Z_S)}. \tag{4.12}$$

Noise matching is completely unrelated both previous matching types. The goal here is low SNR and hence low noise figure. For a given two port network, the noise contribution is controlled by the source impedance which is the impedance seen by looking towards the source from the amplifier. At a certain value of this impedance which is labelled as Z_{opt}, the noise figure is minimized. Therefore, noise matching is achieved when $Z_S = Z_{opt}$.

Any port impedance can be written in terms of the related port reflection coefficient. Hence, we can rewrite Z_{opt} in terms of the characteristic impedance, Z_0 and Γ_{opt} which is the optimum reflection coefficient looking towards the generator (or the input matching network) as given in Equation 4.13.

$$Z_{opt} = Z_0 \frac{(1+\Gamma_{opt})}{(1-\Gamma_{opt})} \tag{4.13}$$

The parameter Z_{opt} is the key factor in defining the noise figure of a two port network. The well known noise factor equation in terms of the two port network noise parameters, is as follows

$$NF = NF_{min} + \frac{R_n / |Z_{opt}|^2}{R_s} |Z_{opt} - Z_s|^2 , \quad (4.14)$$

where NF_{min} is the minimum noise figure of the transistor, attained when $Z_S = Z_{opt}$, R_n is the equivalent noise resistance of the transistor. At first glance, from Equation 4.13 and 4.14, if Γ_{opt} is much smaller than 1, Z_{opt} approaches to Z_0. As the output impedance of the input matching network comes closer to the the source impedance, the term $|Z_{opt} - Z_S|$ becomes zero which results in minimum noise figure, in Equation 4.14. In addition, the parameter R_n should be as low as possible within the band of interest.

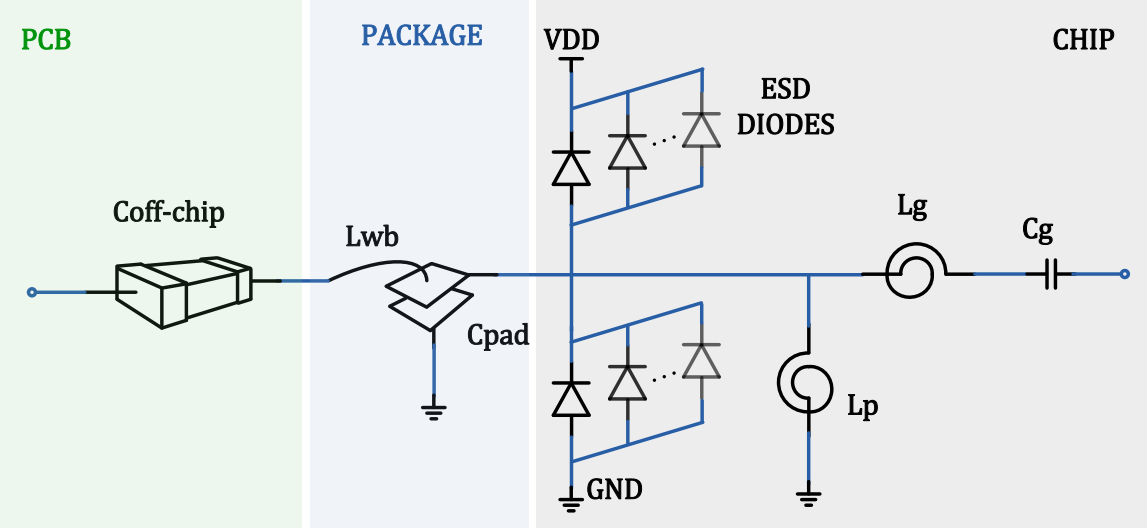


Figure 4.3. Designed matching network including ESD protection and packaging components.

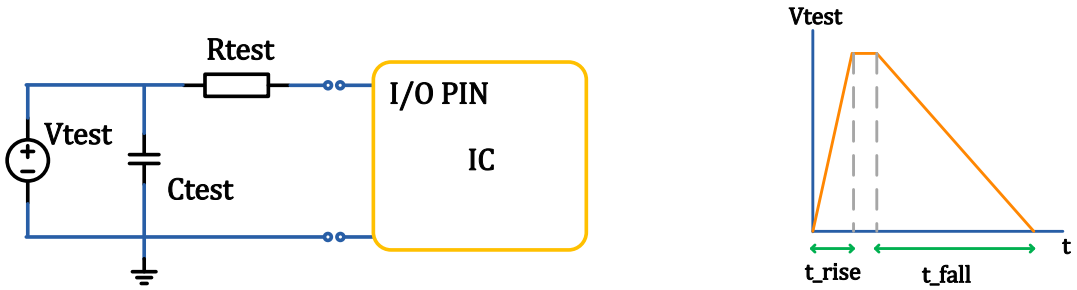
The designed matching network consists of electrostatic discharge (ESD) diodes, input pad, wirebond, and offchip capacitor as illustrated in Figure 4.3.

Electrostatic discharge (ESD), has been a considerable reliability issue in IC industry and especially in nanoscale CMOS technology. With the advances CMOS processes, ESD robustness of CMOS ICs becomes worse as the gate oxide of MOS transistors gets thinner. Since the input of the LNA is usually connected to the external node of an RF receiver chip, off-chip components and on-chip ESD protection circuits are needed for all input pads of the LNA. However, applying ESD protection circuits at the input pads inevitably

affects the RF performance. Hereby, LNA and ESD protection circuits have to be co-designed to simultaneously optimize RF performance and ESD robustness [8].

In general, the ESD protection robustness is proportional to the number of paralel ESD diodes – a higher number of parallel connected diodes provide higher ESD protection. For RF signals, these ESD protection diodes essentially appear as parasitic capacitance. Therefore, implementing more ESD protection devices to achieve higher ESD robustness will result in higher parasitic capacitance. The trade-off here is making a decision between the capacitance and the level of protection.

There are several ways to model the electrostatic discharge such as human body model (HBM), charge device model (CDM), etc. In this design, the HBM is considered and the simulations are performed using HBM test circuitry.



(a) (b)

Figure 4.4. (a) The test setup for ESD diodes. (b) Applied HBM pulse.

The test setup and the applied typical HBM pulse is shown in Figure 4.4a and 4.4b, respectively. The applied pulse has properties of t_{rise} = 2 ns, t_{fall} = 130 ns and V_{test} = 250 V. The resulting peak current is about 0.18 A when the C_{test} is about 600 fF. This result shows that the input of the LNA is protected up to 250V instantaneous peak voltage.

For a higher level protection, C_{test} should be increased, but the bandwidth of LNA is affected negatively in this case and the noise figure becomes worse [9]. Additionally, an increase in C_{test} causes a reduction in S_{11} after a certain width of the amplifying transistor [10].

The rf pad is based on a parameter called “index” which adjusts its capacitive value. The term “index” here corresponds to the minimum metal layer where the top aluminum layer is connected. The number of layers considerably effects the capacitance of the pad.

The wirebond is a piece of thin metal forming the connection between the outside of the chip and the IC as illustrated in Figure 4.5. The length of each wirebond is different from the others in the package except for the vertically and horizontally symmetric counterparts. For this reason, the input ports of the differential receiver have to be symmetric laterally in order to get rid of the mismatches due to the wirebonding process.

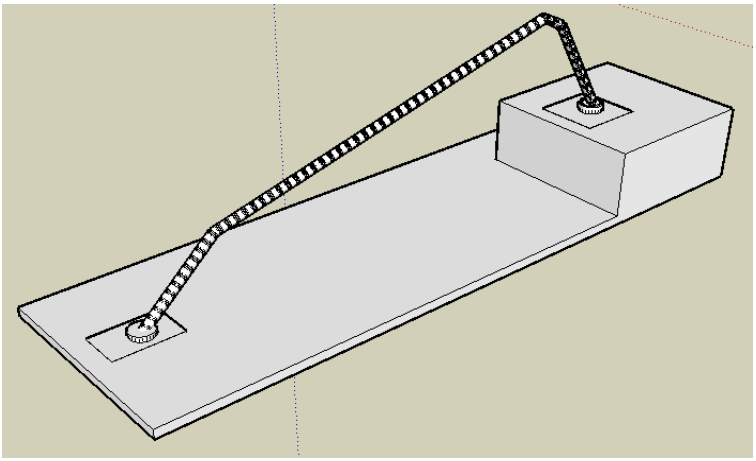


Figure 4.5. 3D illustration of a wirebond.

From Figure 4.5, the inductance of the wirebond is found by measuring the length of each part individually on the microscope. Then the model is simulated and the resulting value is 1.65 nH for a wirebond connected to the LNA (the shortest wirebond in the package).

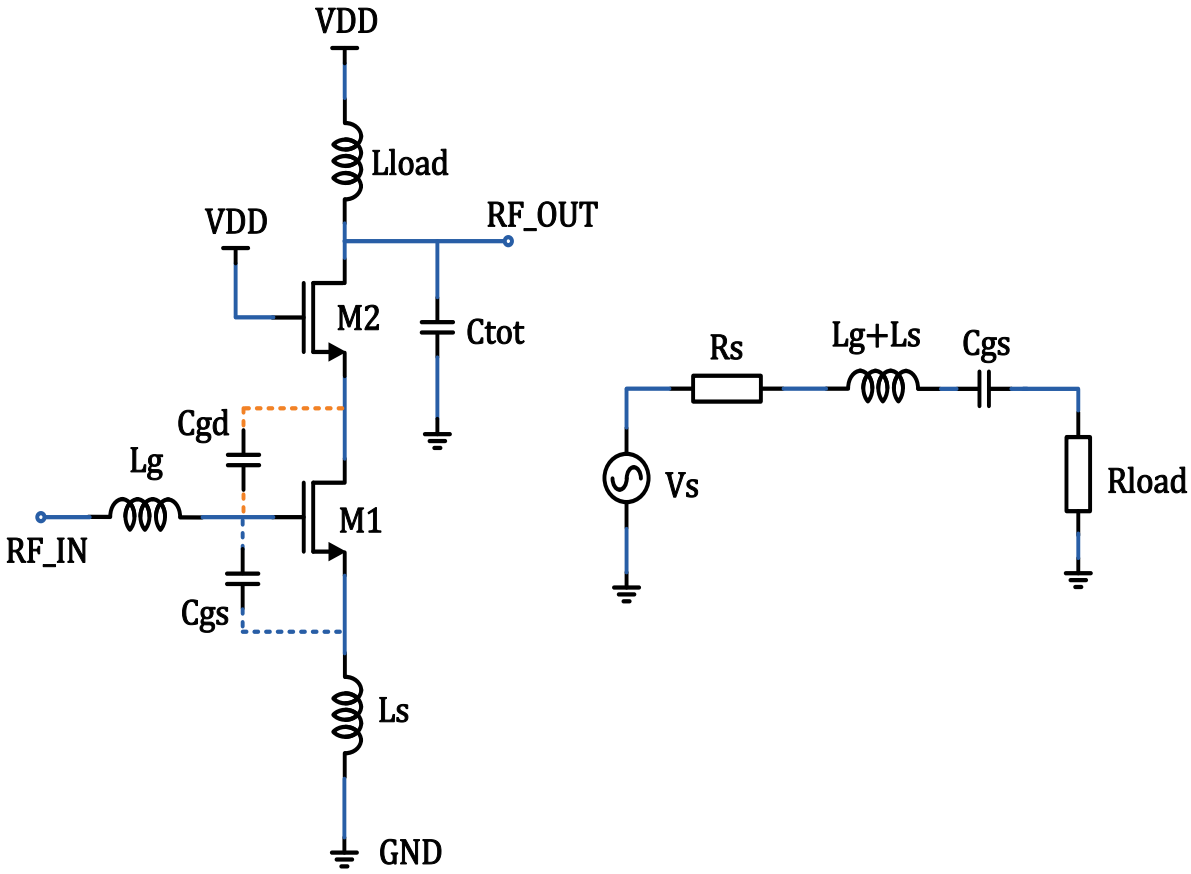
In addition to the ESD diodes, the wirebond and the rf pad, the rest of the matching network is in the form of a Chebyshev bandpass filter. A shunt inductor L_p and a series LC pair are implemented on-chip [11]. The values of these on-chip components are determined according to the designed LNA.

4.1.2.2. The Amplifying Stage of LNA. The topology of the amplifying stage is directly related to the receiver specifications such that high amounts of gain require more power and inductive peaking especially for narrowband LNAs. Moreover, low noise is obtained using less noisy components like inductors. Therefore, these requirements lead the designer to merge all these properties in the same design.

As previously discussed, there are several topologies for wideband LNAs in the literature and the inductive degenerated topology is the most commonly used one among of them, especially for narrow band applications requiring relatively smaller sections of the bandwidth. However, by applying a wideband matching network, this property turns up to be a solution for a wideband LNA. Besides, the design goals can be achieved by applying the proposed techniques with some modifications and adjustments to fit the component values to the predetermined design specifications. Thus, in this thesis, the inductive degenerated topology has been selected to explain in detail and the necessary adjustments are peformed in order to obtain the required operation. However, some substitutions in the circuit may change the topology and therefore the new design needs to be labelled again. The first design is completely the same as the classical inductive degenerated topology and labelled as LNA_1. The second design differs from the first one only in one aspect that L_s is removed in the second one. This second LNA is also labelled as LNA_2. However, some design deficiencies of the following block called as VGA results in some additional arrangements in LNA_2. Therefore, the final design can be considered as a collaborative LNA with the following blocks and this is also called as adapted LNA_2.

Firstly, the basic design principle of the the inductive degenerated LNA is explained. This topology can be clarified using Figure 4.6a.

The inductor at the source is thought as the termination impedance. Normally a single resistor can be used for termination [5]. However the noise contribution of a resistor is relatively large with respect to an inductor. In Figure 4.6b the equivalent circuit model of an inductive degenerated topology is shown. L_g and L_s form a series LC network with gate-to-source parasitic capacitance. When the resonance frequency of this LC network is adjusted to be the center frequency of the band of interest, the impedance of this LC pair becomes zero at the center of the band.



(a) (b)

Figure 4.6. (a) Cascode LNA with source inductive degeneration. (b) equivalent circuit.

The inductor at the source is thought as the termination impedance. Normally a single resistor can be used for termination [5]. However the noise contribution of a resistor is relatively large with respect to an inductor. In Figure 4.6b the equivalent circuit model of an inductive degenerated topology is shown. L_g and L_s form a series LC network with gate-to-source parasitic capacitance. When the resonance frequency of this LC network is adjusted to be the center frequency of the band of interest, the impedance of this LC pair becomes zero at the center of the band.

The termination resistance is a function of L_s and purely resistive, in other words independent of the frequency. For the sake of clarity, the contribution of C_{gd} is neglected and all the statements related to the equivalent circuit model can be written in a mathematical form as in Equation 4.15.

$$Z_{in} = R_S = j\omega_0\left(L_g + L_s\right) + \frac{1}{j\omega_0 C_{gs}} + \frac{g_m L_s}{C_{gs}} + r_{g,NQS} \quad (4.15)$$

In Equation 4.15, when the terms $j\omega_0\left(L_g + L_s\right)$ and $\frac{1}{j\omega_0 C_{gs}}$ are equal, the imaginary part of the input impedance, Z_{in} which is seen at the source looking towards the load, is cancelled. The real part of Z_{in} is just the term $\frac{g_m L_s}{C_{gs}}$ which corresponds to the load impedance, R_{load} in Figure 4.6b. Nevertheless, there are some secondary effects which make Z_{in} different from the ideal case. Due to the classical non-quasi static model of the MOSFET, the parameter non-quasi static gate resistance, $r_{g,NQS}$ appears in series with the gate, which should be taken into account for further accuracy in the calculation of Z_{in}.

The amplifying stage consists of an amplifying transistor M1 and the cascode transistor M2. The design specifications are mostly determined by selecting the appropriate size of M1. As the device size gets larger, the upper cutoff frequency shifts towards the low frequencies and the bandwidth is widened because of the large amount of the gate-to-source parasitic capacitance. On the other hand, large C_{gs} helps to resonate the series LC network at 4 GHz. For instance, C_{gs} = 500 fF resonates at 4 Ghz with the inductor value of 3.16 nH which is applicable. However, for C_{gs} = 100 fF, the series inductor has to be 15.83 nH and this amount of inductance is not supported by the design-kit of UMC 130 nm CMOS Technology. Additionally, a large valued inductor is obtained with large number of nested spirals resulting in a long wire corresponds to high valued resistance. This parasitic resistance is connected in series to the gate and destroys the noise reduction efforts because of its thermal noise [12]. Moreover, the noise figure reduces as the width of the inductor increases and begins to go beyond from the optimum width [12]. Therefore, as a result of trade-off, the optimum width should be selected to satisfy both conditions.

The cascode transistor M2 is basically used to provide isolation from output port to the input port. This isolation can be explained in terms of s parameters. S_{12} is defined as the reverse gain for an amplifier. Reverse isolation ($-S_{12}$) reduces the coupling from output of the LNA to the antenna through the reverse gain of the LNA.

The size of M2 is an another design issue. It is known that increasing the width of the cascode device improves shielding from the output. However, as the width of the cascode stage increases, the generated noise power from the cascode stage also increases. Intuitively, this fact suggests that smaller M2 improves the noise figure by reducing the noise contribution of M2 as well as the capacitance at the intermediate node between M1 and M2 [12]. Due to the Miller effect, however, the required L_s for Z_{in}=50 Ω increases as M2 becomes smaller. Consequently, smaller M2 yields a different noise-match condition as well as larger value of $r_{g,NQS}$. Additionally, the smaller the M2 causes the bandwidth to shift to the right in frequency and small amount of reduction in gain. On the other hand, because of the fact that g_{m2} is proportional to the $\sqrt{W/L}$ of M2, at a given bias current, the g_m of M2 should be large enough in order to reduce the Miller effect. The impedance seen looking towards M2 is $1/g_{m2}$; therefore, the gain seen by C_{gd} of M1 is g_{m1}/g_{m2} which gets smaller as g_{m2} increases.

In general the the gain is obtained by plugging a resistor into the drain of M2. However, in many RF amplifiers, resonant loads consisting of inductors, resistors, and capacitors are used to match impedances, cancel parasitics, and filter out unwanted signals [13] By exploiting resonance of LC networks, it is possible to obtain higher gain at RF than would otherwise be possible with non-resonant (resistor load) circuits [14]. Moreover, the resistor is not a reasonable choice because of its thermal noise at high frequencies. In the presence of a resistor as a load, the voltage drop on the resistor reduces the headroom at the cascoded amplifier.

A single inductor, L_{load} is used to have a peak response at the center frequency. Because of the low quality factor of on-chip inductors, the AC response of the LNA covers the 3.1 GHz - 4.7 GHz bandwidth. The question here is how much load inductance is needed for the desired gain. Manual calculations do not give accurate values because of the parasitic resistance of the on chip inductors. On the other hand, the S_{11} response is directly affected by the variations on the load inductor. As L_{load} decreases, the bandwidth widens, shifts to the right in frequency, and also the gain reduces.

As previously discussed, the source inductor is needed to have a purely resistive and ideally noise-free load impedance for input matching network. The term $(g_m/C_{gs})L_s$ in

Equation 4.15 determines the value of L_s. The noise figure curve has its minima at the optimum value of L_s as can be seen in [10]. For the large L_s, bandwidth shifts towards the low frequencies and gain reduces [15].

It is true that the presence of L_s improves the noise figure of the LNA, however the high gain requirements, matching problems, and large the chip size area are considerable reasons to remove L_s. In the absence of L_s, the termination impedance expressed as $(g_m/C_{gs})L_s$, is no longer purely resistive. Therefore, Z_{in} becomes a complex impedance or in other words, has a dependence on frequency. However, for a certain value of Zin, the matching can be improved.

All the statements and design considerations may comply with the hand calculations for the ideal components. But in reality, the on-chip components effect the overall performance dramatically. [16] verifies this difference between ideal and on chip inductor behaviours over the frequency. The ideal case is about 1 dB more optimistic than the real case. In addition to this, the noise contribution of a single inductor can be almost defined as a linear function of its inductance and frequency.

4.1.2.3. Current Source. While getting started with any analog design, it is assumed that an ideal current source which has an infinite output impedance and constant current vs. V_{ds} curve, exists. However, the implementation of an integrated circuit eventually needs current bias circuitry.

Generally, in integrated circuit design, biasing is based on constant-current sources. The constant DC current is supplied by using several techniques according to the requirement of the circuit. Figure 4.7 shows a basic current mirror which supplies the current bias from the left branch – labelled as I_{out}.

The most important component here is M2 used for a voltage bias for M1. The supply voltage is split into two as the voltage drop over the bias resistor (R_{bias}) and the bias voltage at the gate of both transistors. The output voltage needed to guarantee the transistors to operate in saturation, is the overdrive voltage of M1. The output resistance of this current mirror is r_{o1} which is roughly several kΩ.

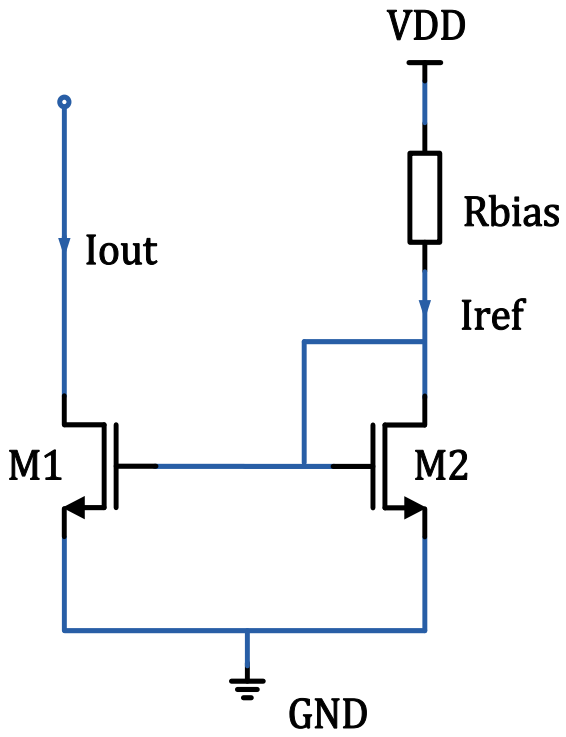


Figure 4.7. Circuit for a basic MOSFET current source.

In the design of the differential LNA, as will be covered later, the process is carried out by assuming that current bias is close to an ideal source. However, a basic current mirror cannot support these specifications. An alternative for larger values of output impedance is cascode topology. In the literature, there are several types of cascode current mirrors [17].

In Figure 4.8, a modified Wilson current mirror is presented. This cascode topology comes from the basic Wilson MOS mirror. Basically, cascode Wilson is constructed in the absence of transistor M4. It exhibits an increase of output impedance by a factor of $g_{m3}.r_{o3}$. An increase in r_o is a result of the negative feedback obtained by connecting the drain of M2 to the gate of M3. But this topology has an immunity on mismatches. Therefore, in order to remove the possibility of current error resulting from the drain-source voltages and to balance the two branches, a diode-connected M4 is included.

The output impedance of this configuration is roughly $R_{out}= g_{m3} \times r_{03} \times r_{02}$ [17] and it is on the order of tens of kΩ.

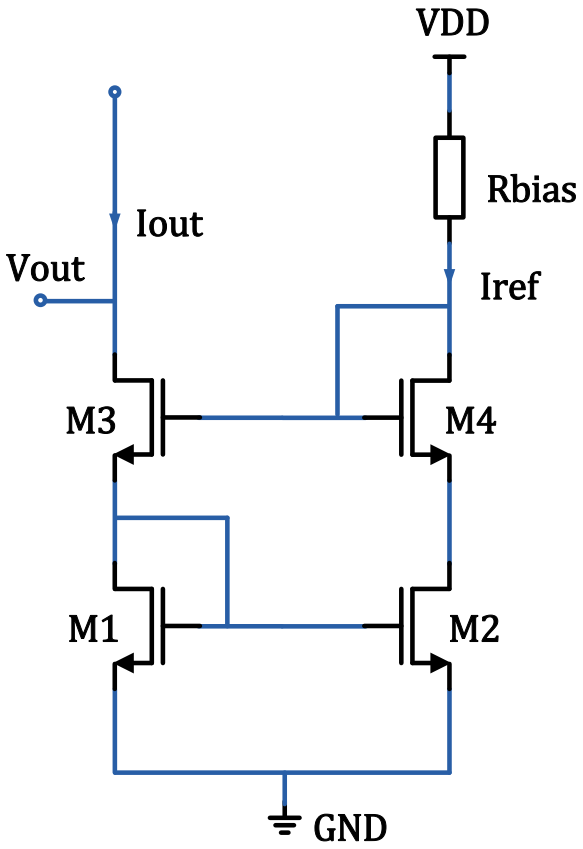


Figure 4.8. Circuit for a Modified Wilson MOSFET current mirror.

One other issue on cascode current mirrors is obtaining a large headroom. For this reason, dc operating points for transistors are selected to make all of them to operate at just above the saturation boundary with a safety margin. Nevertheless, the output voltage limits the dc operating range of the amplifier.

The voltage levels of the transistors can be calculated easily by choosing the bias voltages at a minimum value to keep all of them in saturation. The gates of both M1 and M2 in Figure 4.8, are $V_{ov} + V_t$ where V_{ov} and V_t are overdrive and threshold voltages for all transistor, respectively. V_{ds} of M1 is $V_{ov} + V_t$ and V_{ds} of M2 is V_{ov} for the minimum case. The gates of both cascode devices M3 and M4 are $2V_{ov} + 2V_t$ and V_{ov} is sufficient for the V_{ds} of M3 to stay inside saturation region. Finally, the output voltage is calculated as $2V_{ov} + V_t$. In UMC 130 nm CMOS technology, low-threshold transistors have a threshold voltage of 0.17 V- 0.2 V. Safety margin for overdrive voltage is approximately 100 mV. Hence, the resulting minimum output voltage is roughly between 0.35 V-0.4 V.

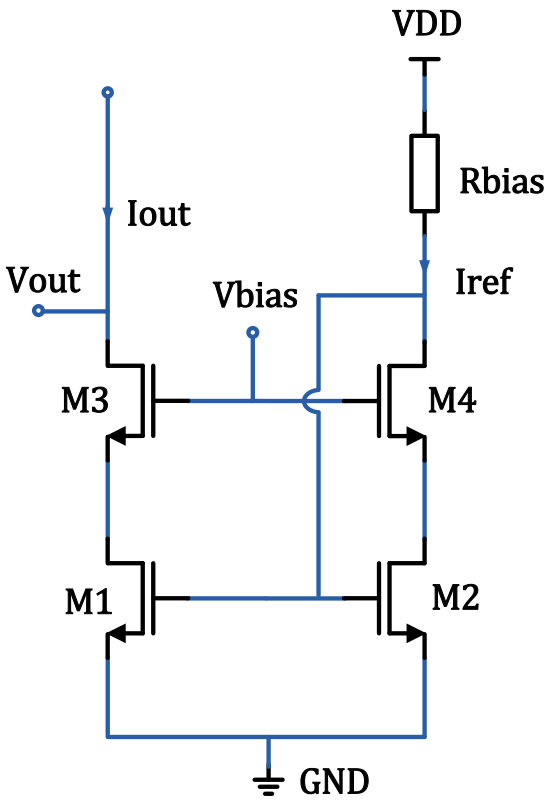


Figure 4.9. Circuit for a low output voltage cascode current mirror.

In some amplifiers which low dc levels are required for input, low voltage current mirrors are preferred as shown in Figure 4.9. As can be observed from this figure, by connecting the gate of M2 to the drain of M4, the gates of both M3 and M4 are forced to be biased at a lower voltage compared to the modified Wilson current mirror, as previously discussed. Thus, low bias voltage yields low output voltage as follows: The gates of M1 and M2 are $V_{ov} + V_t$. V_{ds} voltages of M1 and M2 are V_{ov} for the minimum case. The gates of both cascode devices M3 and M4 are connected to an external bias network and the minimum voltage for saturation is $V_{ov} + 2V_t$. Finally, the output voltage is found as $V_{ov} + V_t$. As a conclusion, the output voltage is improved by V_{ov} with respect to the modified Wilson current mirror and can be reduced further by a factor of 100 mV. On the other hand, the drawback of this current source is an additional bias network and therefore extra power dissipation and chip area.

The equation of the output resistance of this configuration is similar to the previous one, however r_{o1} is replaced by r_{o2} as follows, $R_{out} = g_{m3} \times r_{03} \times r_{01}$.

4.1.2.4. Analysis of Designed LNAs. By considering all the design statements above, the simulation results of LNA_1 are given in Figures 4.10 and 4.11. The voltage gain of this LNA is about 12.3dB and 3dB bandwidth covers the UWB frequency range of 3.1 GHz - 4.7 GHz. The noise figure shows a bandpass characteristic within the band of interest and in the range of 3.27 – 4.27 dB. In Figure 4.11, the undesired peak at 2 GHz stems from simulation mode which takes into account the harmonics.

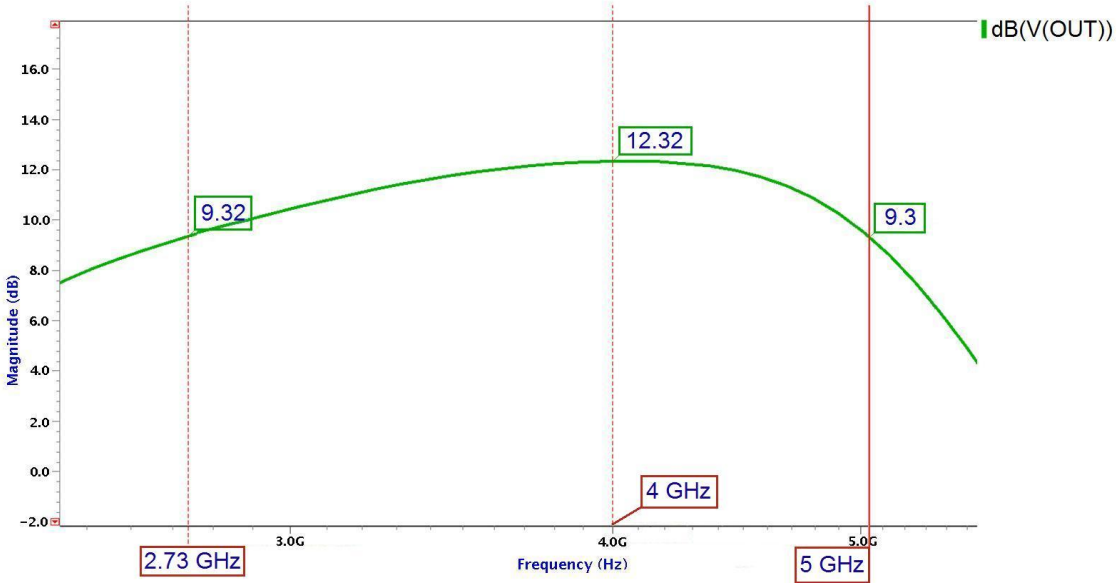


Figure 4.10. AC response of the LNA_1.

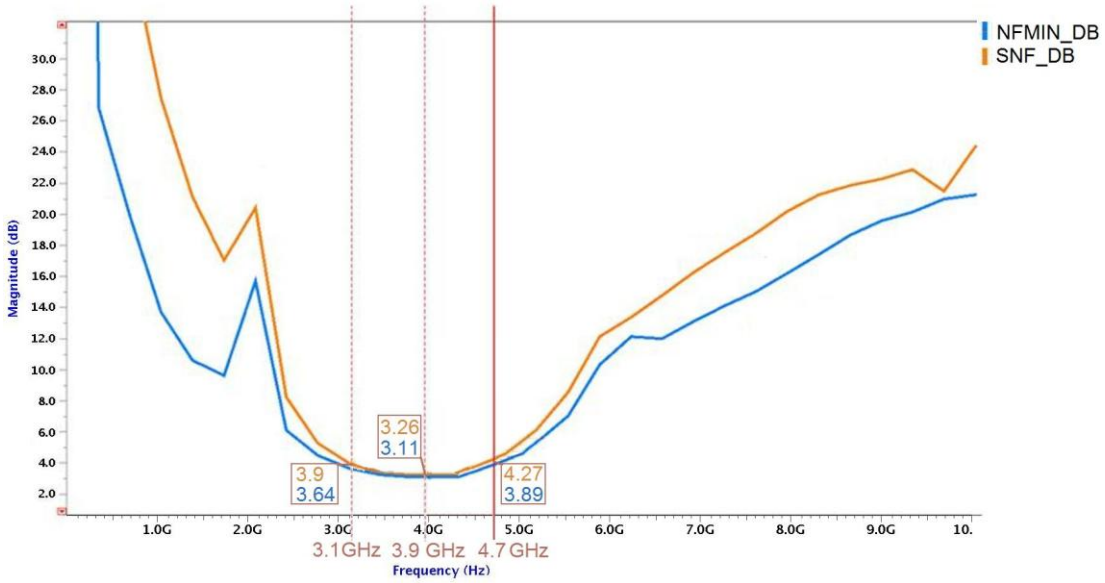


Figure 4.11. Noise figure of the LNA_1.

For the inductive degenerated LNA, the current flowing through the amplifying transistors is 9.1 mA. The total DC power dissipation is 11 mW.

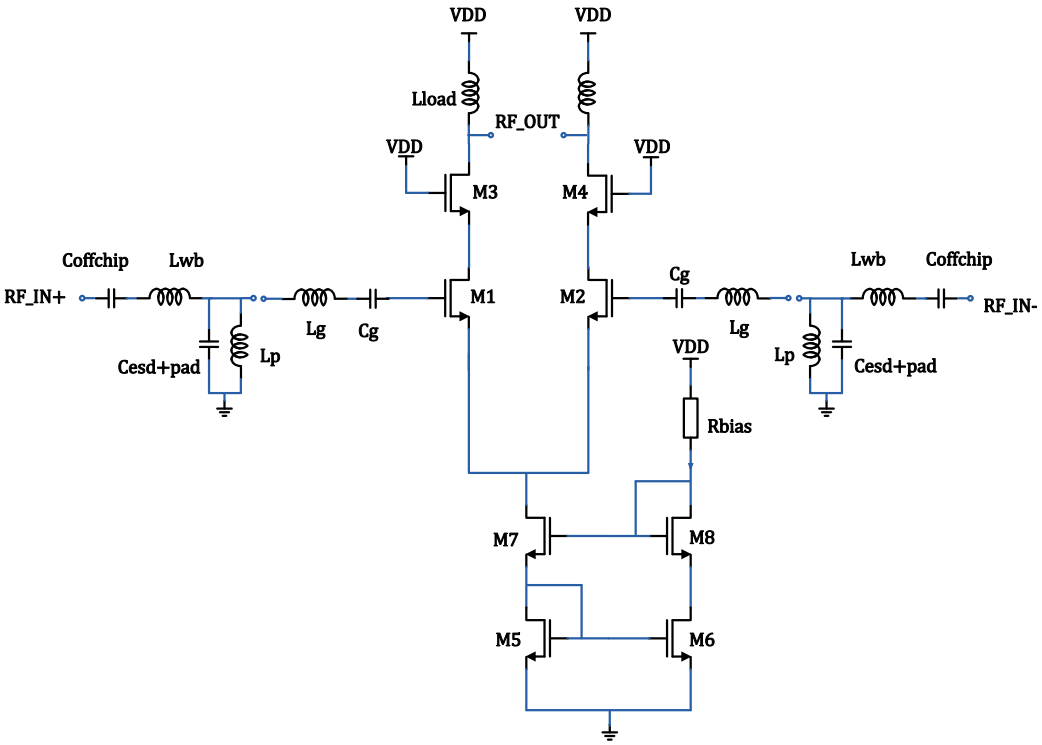


Figure 4.12. The designed LNA and matching network without source inductive degeneration (LNA_2).

As a result, this topology does not seem to be a solution because of the fact that the S_{11} response does not satisfy the bandpass characteristics and causes reflections on the UWB signal as discussed before. Additionally, the voltage gain is not sufficient considering that the receiver should even work from long distances. Hence, gain improvement is needed and the source inductor is removed to achieve this aim. In Figure 4.12, the designed LNA_2 is shown with its matching network.

According to the schematic simulation of LNA_2 in Figure 4.13, the gain is about 21 dB at 0.9 V bias and the S_{11} response satisfies the rule of thumb which is the amount of minimum tolerable reflection correspomding to -10 dB in RF systems, within the lower half of the band. The upper half can cause reflections but they are almost in the tolerable range when the design goals are considered. AC response covers bandwidth perfectly with a sufficient voltage gain.

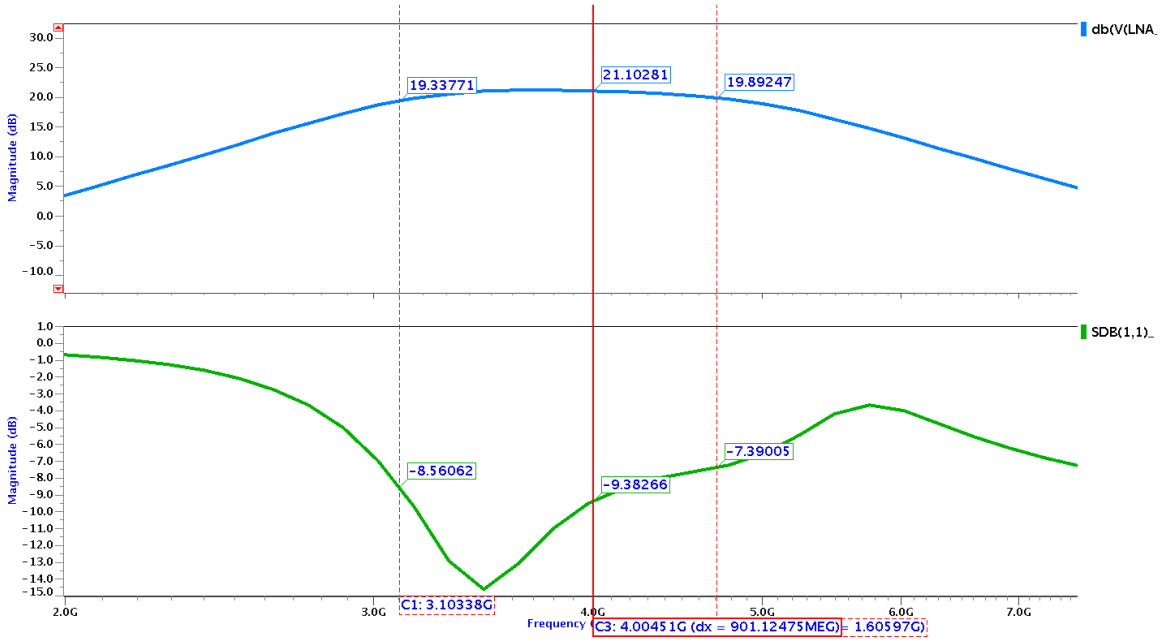


Figure 4.13. The AC (upper plot) and S_{11} (lower plot) response of LNA_2 (schematic).

The noise figure within the band is ranging from 3.7 dB to 4.6 dB (Figure 4.14). The term NF_{min} in the figures, represents the noise figure with ideal matching. At some points the NF_{min} is greater than the NF because of the noise figure simulation of Mentor Graphics-Eldo RF by taking into account the harmonics.

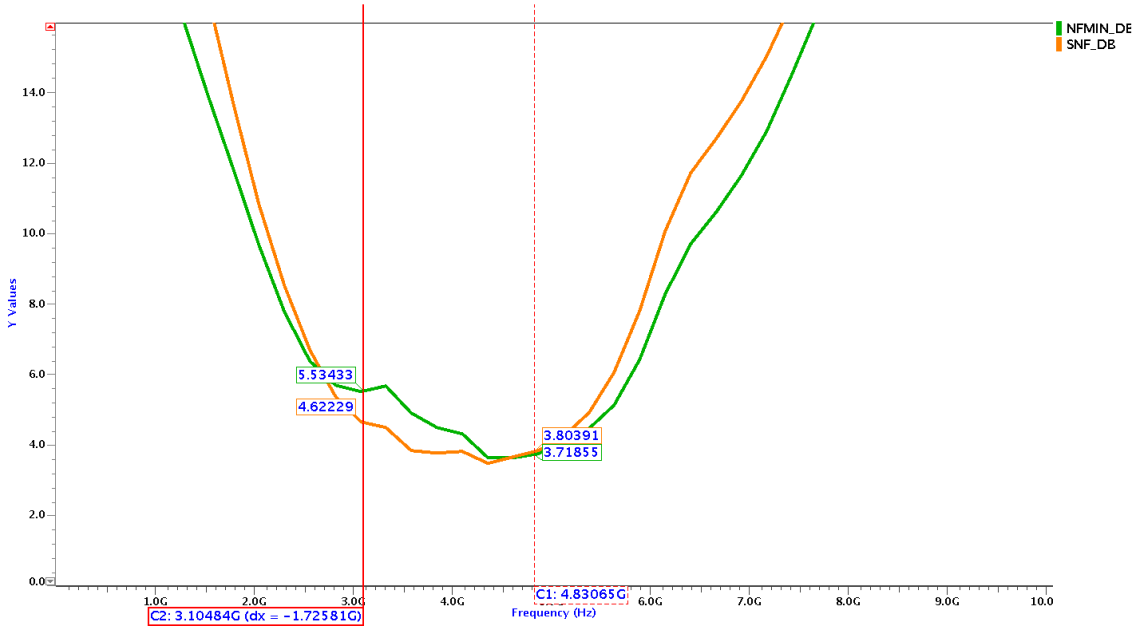


Figure 4.14. Noise figure of the LNA_2 (schematic).

The AC response in Figure 4.13 complies with the design goals but can not work in collaboration with the VGA due to the gain curve of the VGA towards the upper cutoff frequencies. Thus, LNA_2 should be considered with the VGA to discard this problem. What should be done is shifting the bandwidth of LNA_2 towards 5 GHz.

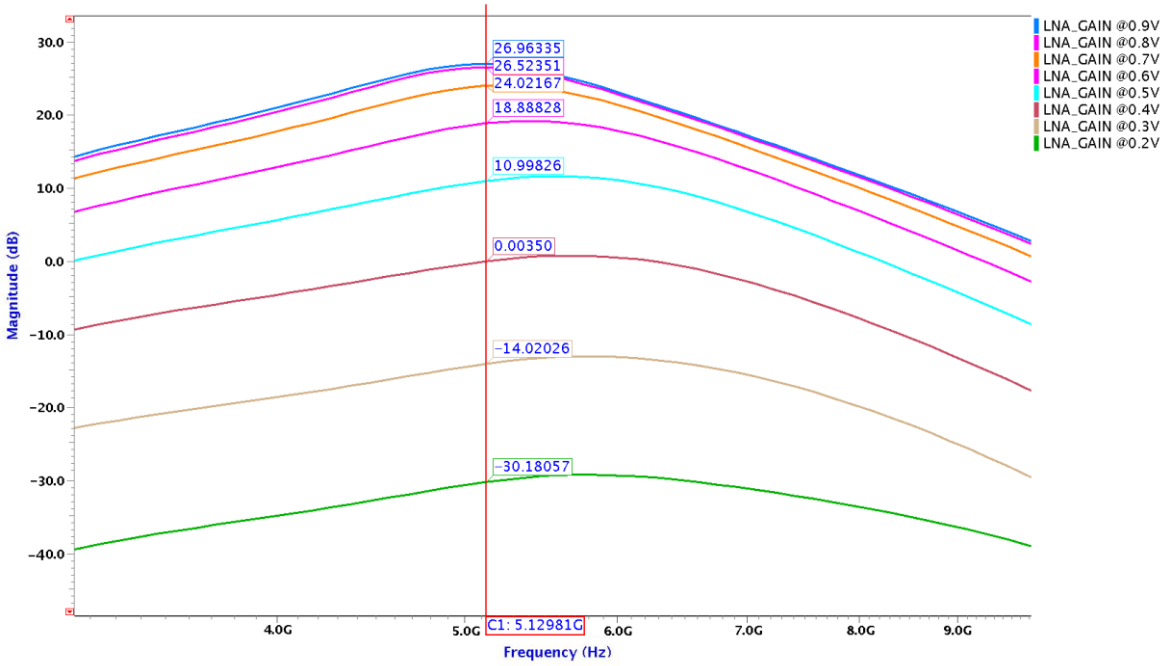


Figure 4.15. The AC response of adapted LNA_2 (schematic).

The schematic simulation of the adapted LNA_2 without source inductive degeneration shows that the gain is about 27 dB at 0.9 V bias as can be observed from Figure 4.15. The bandwidth is shifted to 4.4 GHz – 5.86 GHz because the following stage does not satisfy the upper cutoff frequency, and therefore LNA_2 is designed to get rid of this problem as previously mentioned.

In the post layout simulation (Figure 4.16), the bandwidth is shifted to 3.5 GHz - 4.9 GHz and the gain reduces to 24.3 dB. The variable gain is obtained applying an external bias voltage to the gate of the amplifying transistor. The bias voltage might be applied using a resistive feedback but some stability problems arise in this case. Besides, the variable gain property is one of the design goals and it is obtained with external bias.

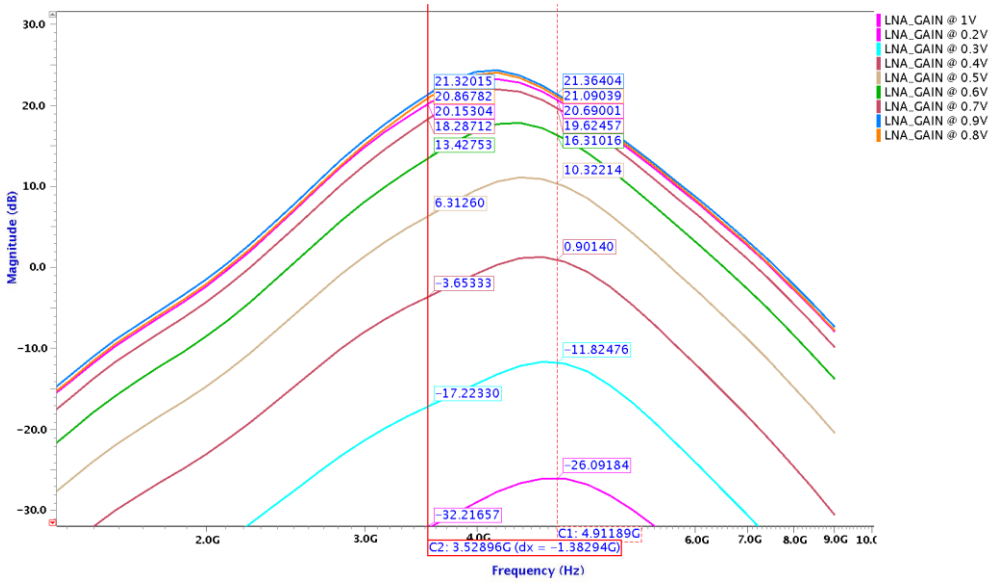


Figure 4.16. The AC response of adapted LNA_2 (layout).

Figure 4.17 shows the AC response after 5 stages cascade VGA. Before the mixer, the bandwidth of the amplified signal is pulled to 3.2 GHz - 5.4 GHz. This is the reason why the adapted LNA_2 is designed with roughly with 1 GHz shifted bandwidth.

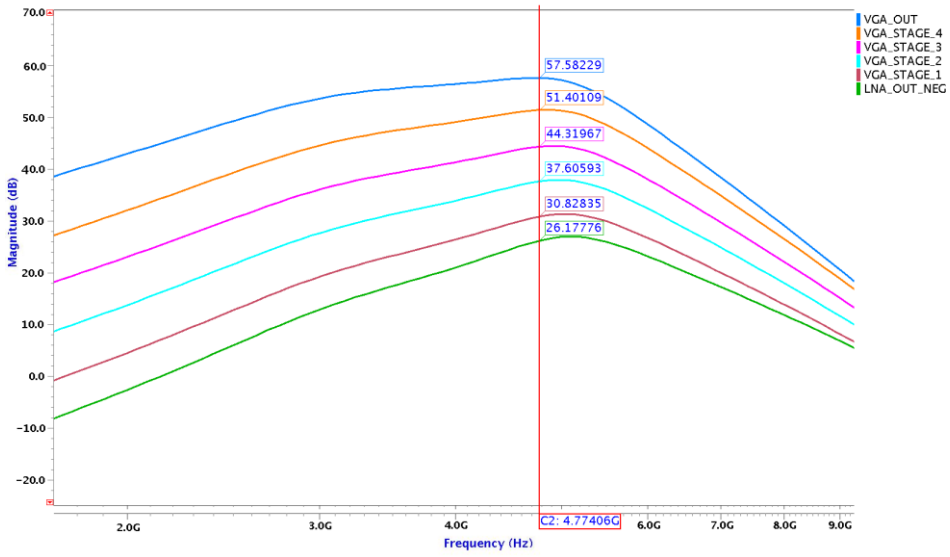


Figure 4.17. The AC response of adapted LNA_2 + 5 stages cascade VGA (schematic).

The noise figure in Figure 4.18 is obtained with the schematic simulation by taking into account the harmonic distortion. Hence, the NF_{min} (minimum noise figure) is greater than the NF at some points in the plot.

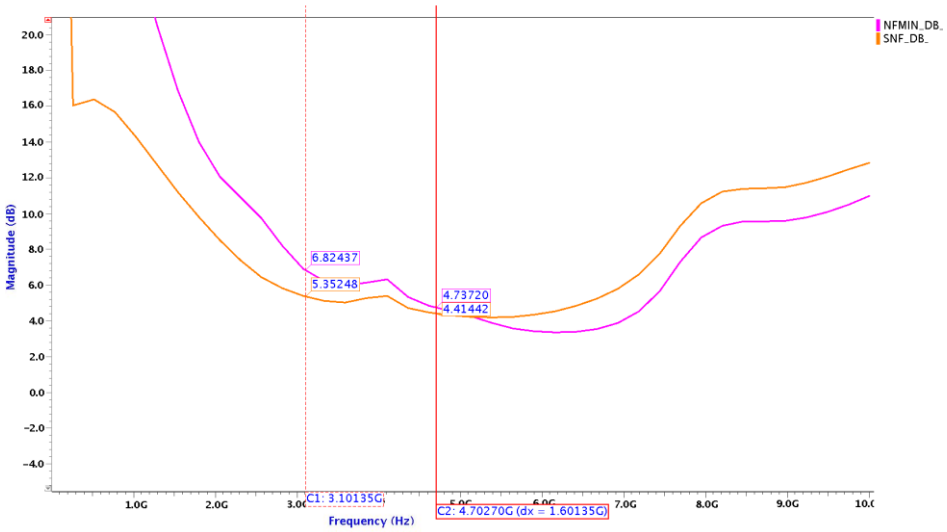


Figure 4.18. Noise figure of the adapted LNA_2 (schematic).

The in-band noise figure is 4.4 dB - 5.35 dB and 4.35 dB - 5.46 dB in pre-layout (Figure 4.18), and in post-layout (Figure 4.21) simulations, respectively. Hence, this small difference in schematic and layout noise figure shows that the parasitic resistance extracted from the layout is not effective.

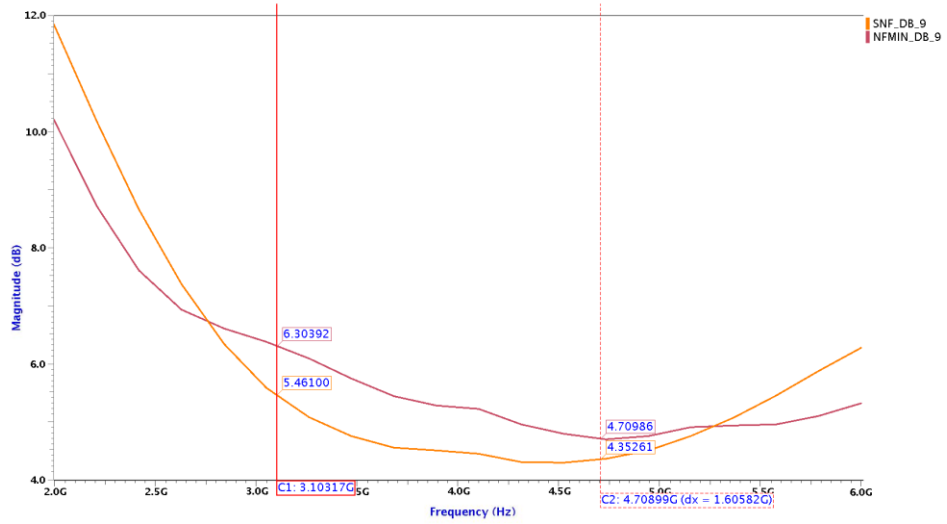


Figure 4.19. Noise figure of the adapted LNA_2 (layout).

Ideally, the noise figure consists of the individual contributions of the matching network, transistors, and passive devices. [18] verifies this contribution sufficiently well. The noise figure is therefore different from the hand calculations or individual noise simulation of these blocks.

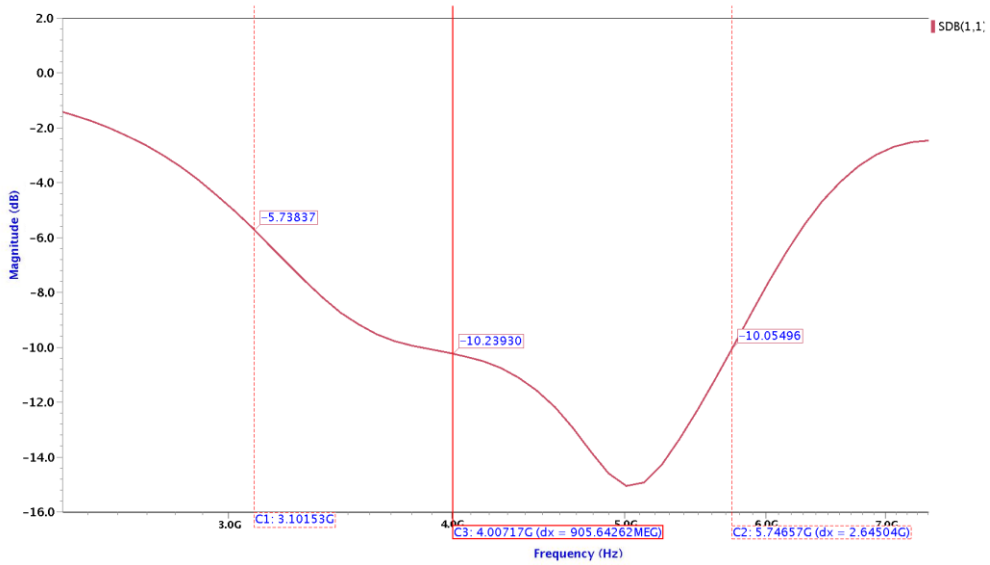


Figure 4.20. S_{11} of the adapted LNA_2 (schematic).

From Figure 4.20, the S_{11} response is mostly less than -10 dB but at the lower cutoff frequency it is about -5 dB. This drawback can be discarded by increasing the L_g, however the noise figure is affected negatively because of the increased parasitic resistance of L_g.

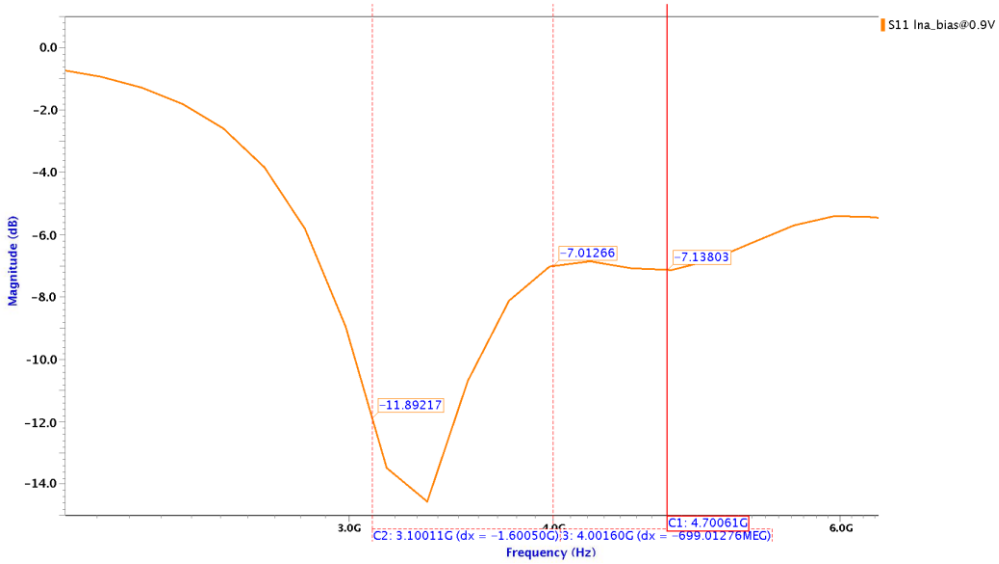
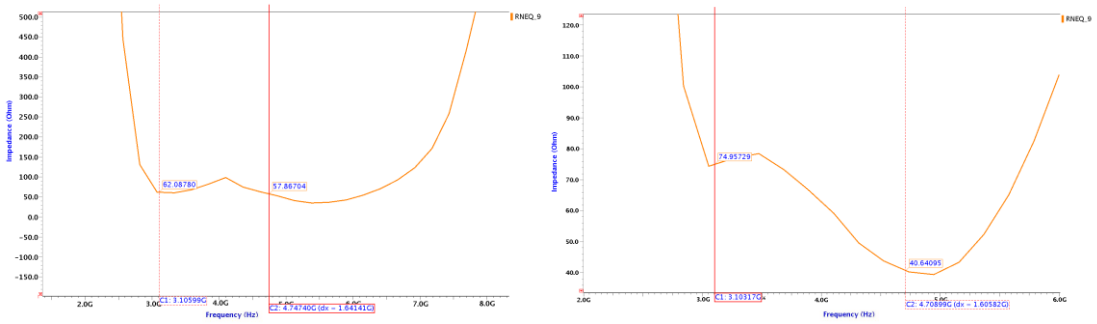


Figure 4.21. S_{11} of the adapted LNA_2 (layout).

On the other hand, the S_{11} turns up to be the curve in Figure 4.21 in the post-layout simulation. The section from 4 GHz to 5 GHz of the frequency band has a tolerable reflection of -7 dB and the rest of the band is less than -10 dB which is a standard in RF design.

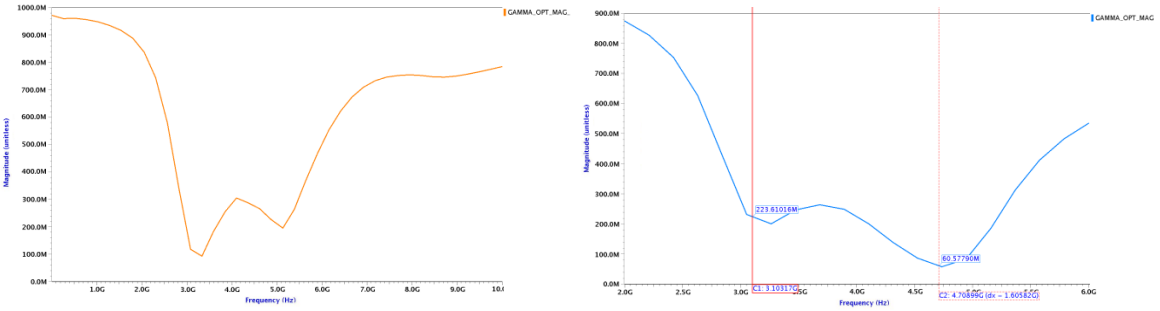
As previously discussed, the noise resistance R_n should be small enough for noise matching. In addition to this, the optimum reflection Γ_{opt} is close to zero where the noise figure is nearly the same as the minimum noise figure. Figure 4.22 and 4.23 illustrate the above statements clearly.



(a) (b)

Figure 4.22. R_n of the adapted LNA_2 (a) Schematic (b) Layout.

The R_n is about 50 Ω - 65 Ω and 40 Ω - 70 Ω for the pre-layout and post-layout simulations, respectively. The noise figure is a function of both R_n and Γ_{opt}, therefore the Γ_{opt} has its minimum within the band of interest (Figure 4.23).



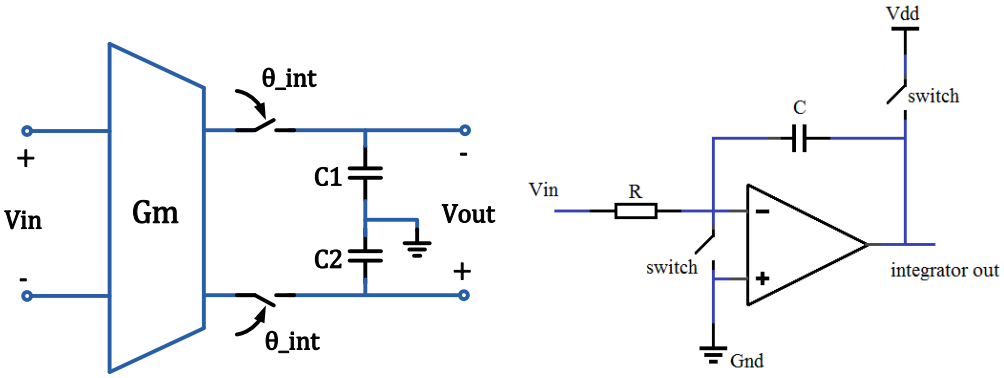
(a) (b)

Figure 4.23. Γ_{opt} of the adapted LNA_2. (a) Schematic (b) Layout.

As a conclusion, the current flowing through the amplifying transistors is 10.37 mA. The total DC power dissipation is 13.96 mW.

4.2. G_m-C Integrator

Integrators can be represented as analog filters which are implemented in two commonly used topologies; switched-capacitor and continuous-time. Switched-capacitor topology is not preferred since the baseband signal bandwidth is about 500 MHz.



(a) (b)

Figure 4.24. Two example circuits implementing a windowed integrator: (a) a transconductor based integrator, and (b) an op amp based integrator.

Another approach is opamp based integrator with capacitive feedback as shown in Figure 4.24b. This feedback forms a virtual ground node at the negative input terminal of the opamp. Feedback capacitor is used to take the integral of the current flowing through it during the pulse duration. The series resistor converts input voltage to current with high linearity. In some cases, this series resistor is replaced by a transconductance amplifier and the overall system is called G_m-C opamp integrator. This topology consumes more power and may not be effective for high frequency baseband analog design.

As illustrated in Figure 4.24a, an alternative way is G_m-C integrator without additional opamp. The transconductor is implemented using a simple differential pair, common source amplifier etc. Low power transconductor based integrator is preferred because of its simplicity.

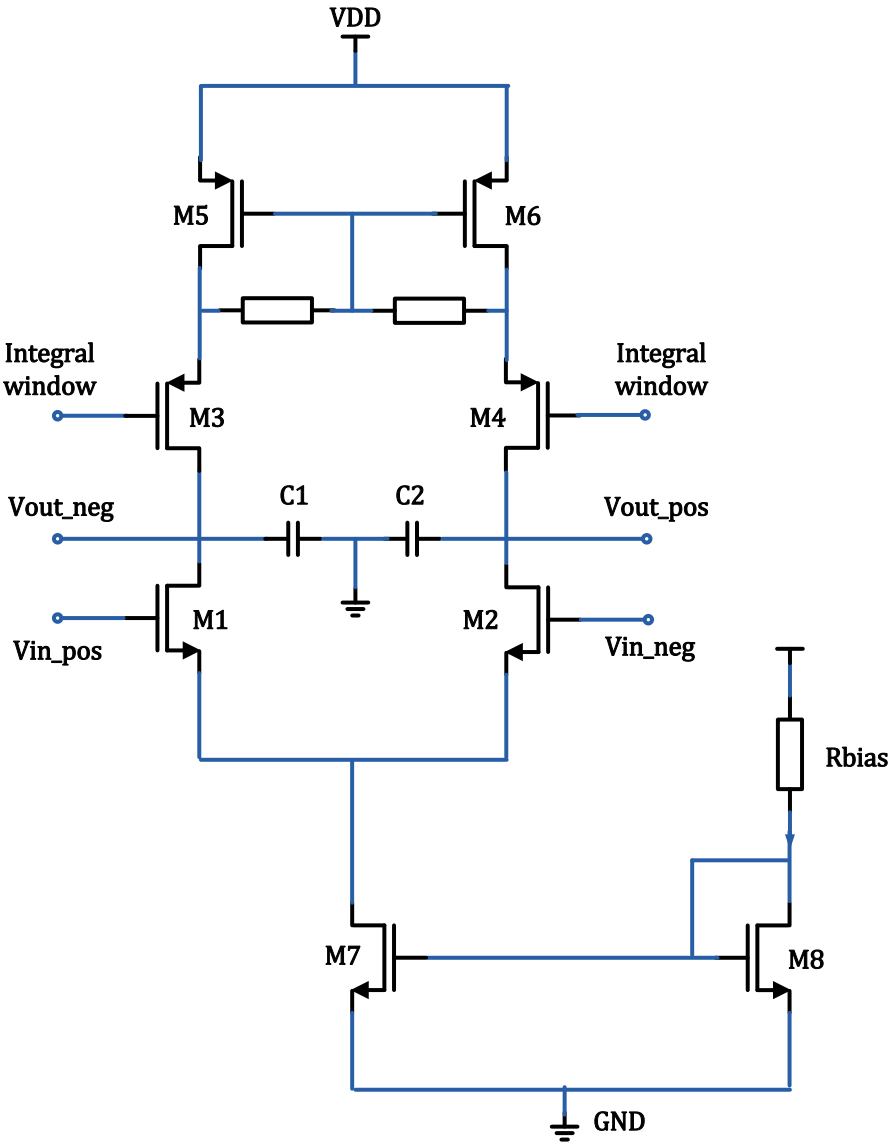


Figure 4.25. Designed G_m-C Integrator circuit.

A simple differential amplifier as the transconductor, integrating capacitors, and basic current mirror circuitry form a G_m-C integrator as shown in Figure 4.25. Firstly, analog design of this circuit can be explained by determining circuit specifications such as dc voltage gain, dc bias point etc.

The baseband signal has a bandwidth about 500 MHz. Therefore, the circuit must have a cutoff frequency of at least 500 MHz. The sizes of the amplifying transistors are selected as width of 2.9 µm, number of fingers of 16 with minimum transistor length of 0.12 µm (same for all transistors), to compensate this requirement.

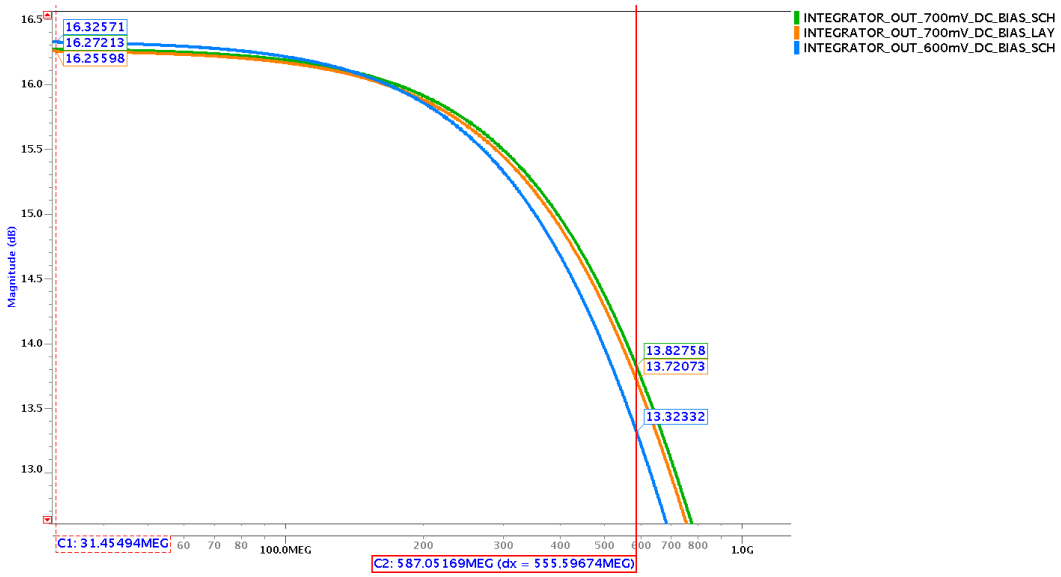


Figure 4.26. AC response of the G_m-C integrator.

The dc voltage gain is calculated by using Equation 4.16 and Equation 4.17 shows the voltage gain in terms of dB.

$$A_V = g_{m8} \times \left[\left[g_{m6} \times r_{06} \times (R_{bias} \parallel r_{03}) \parallel r_{08} \right] \right] \approx 6 \tag{4.16}$$

$$A_V|_{dB} \approx 15.5 \text{ dB} \tag{4.17}$$

As shown in Figure 4.26, dc voltage gain is about 16 dB and the cutoff frequency is 550 MHz. Post-layout and pre-layout results are almost the same because the layout has been drawn by considering the capacitive effects of paths as shown in the integrator layout in Appendix A.

The active loads are used to improve the gain and also the current mirror is self biased through bias resistor, R_{bias}. Typically the current bias is obtained by the basic current mirror. The current flowing through the tail is 1.19 mA. Actually the DC power dissipation should be considered in two ways depending on whether the integration occurs or not.

- When integral window is 0 V (enable), the DC power dissipation is 1.58 mW.
- When integral window is 1.2 V (disable), the DC power dissipation is 132 μW.

- The average power dissipation is calculated as 728 uW for 5 pulses as shown in Figure 4.27.

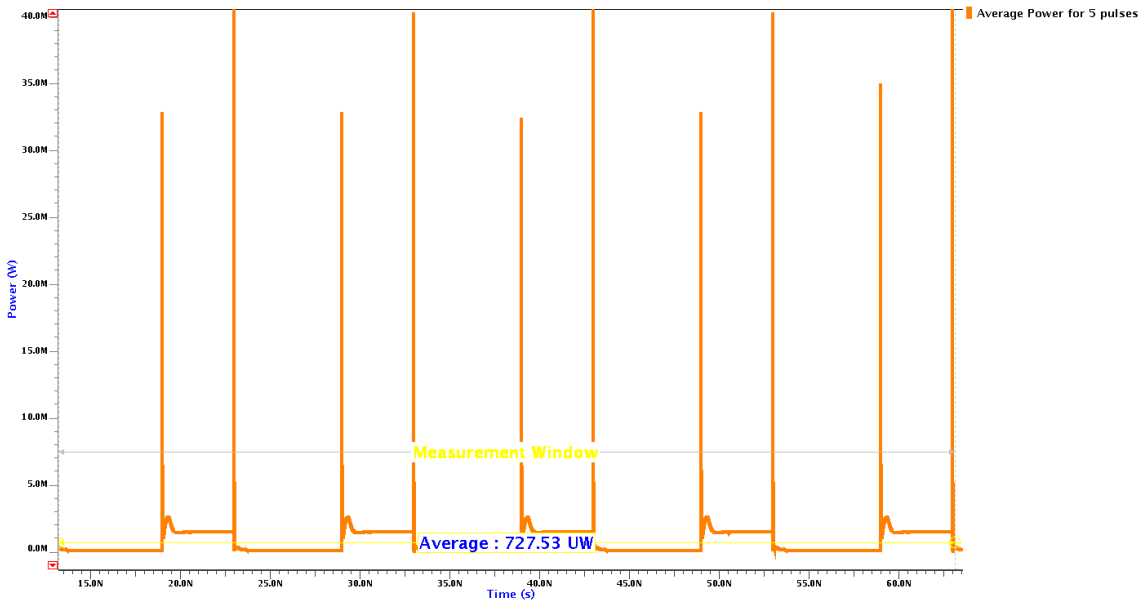


Figure 4.27. Average power calculation for 5 pulses.

In order to control the integration, PMOS transistors labelled as M3 and M4 in Figure 4.25 which are biased by the integral window clock are included as a switch. The operation of the integrator becomes clear with Figure 4.28. When the clock is HIGH or in other words 1.2V is applied (ON state), PMOS enters cutoff region and integration is not performed. On the other hand, when the clock is switched to LOW state or 0 V is applied (OFF state), these integration switches enter saturation and integration occurs within the time interval of ON state. We can say that from the above explanations, enabling of the integration is active low. Another benefit is that during the OFF state, the DC level at the output of the integrator reduces to 0V and this results in a power reduction in the following stage which is pmos preamplifier for comparator which will be covered later.

The input differential signal has a voltage amplitude of 40 mV_{pp} and the amplification increases this difference up to 240 mV_{pp} corresponding to 16 dB as illustrated in Figure 4.26.

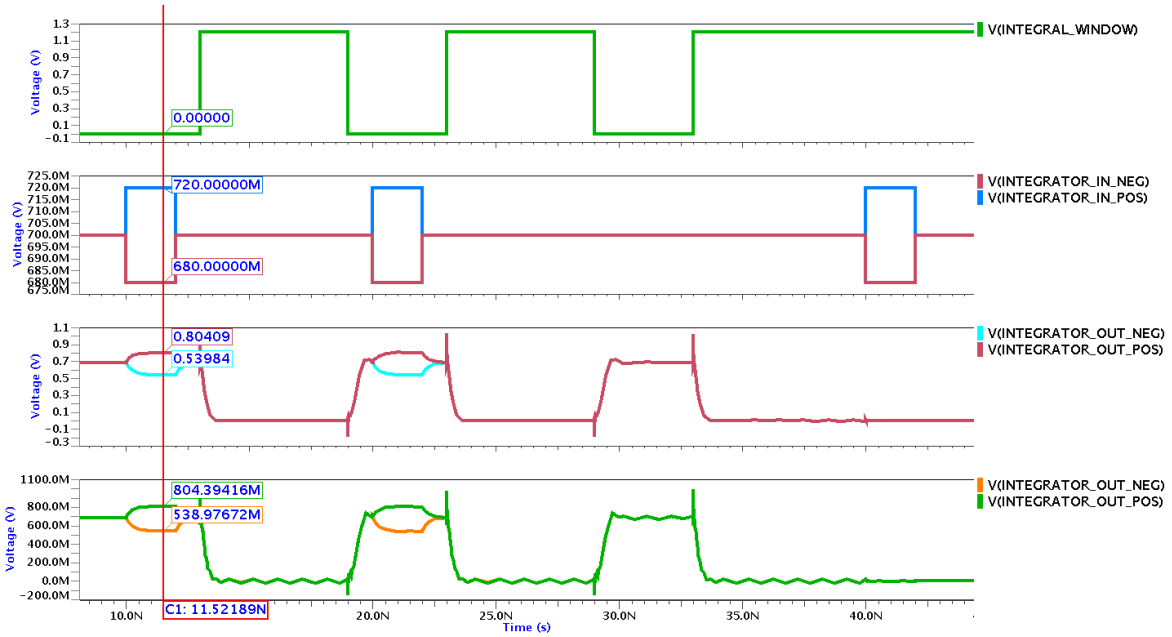


Figure 4.28. Transient analysis of the G_m-C integrator shows the windowing of integration.

The fluctuations at the output waveform result from the wirebond inductors. This can be eliminated by adding bypass capacitors in different values between VDD and GND.

4.3. Continuous -Time Comparator with Hysteresis

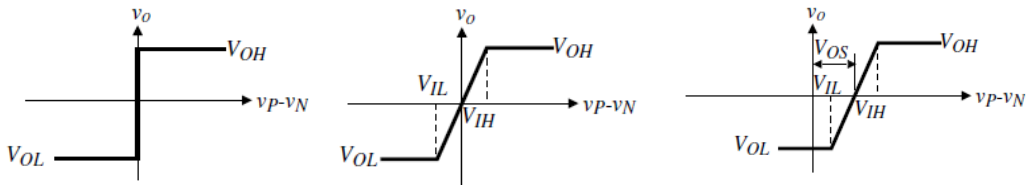
Basically, a comparator is based on an op amp. As in opamps, it has input ports and output ports. On the the contrary, they are generally used in open-loop mode and so it is not necessary to compensate the comparator as opposed to opamp design. Since no compensation is needed, it has the largest bandwidth possible which gives a faster response.

Its basic operation is specifically to compare the voltages between its two inputs. Therefore, it can be said that it operates in a non-linear concept, providing a two-state logic output voltage. These two states represent the sign of the difference between the two inputs (including the effects of the comparator input offset voltage). The sign is equal to logic "1"; if the positive input of the comparator is at a greater potential than the negative input; whereas the sign is equal to logic "0", if the positive input is at a potential less than the negative input.

4.3.1 Characterization of the comparator

Analog design of comparators requires to determine the design specifications as the same for all analog devices. The specifications may divided into two main parts as follows:

- Gain, output high and low states, input offset voltage as static chararacteristics.
- Propagation delay, slew rate as dynamic chararacteristics.



(a) (b) (c)

Figure 4.29. (a) Zero-order (b) First-order and (c) First-order with input offset voltage model for a comparator [19].

The basic operation of comparator can be explained from the ideal case to the more realistic one as shown in Figure 4.29. The voltage levels on the figures are described as:

- V_{OL}= The low level output of the comparator
- V_{OH} = The high output of the comparator.
- V_{IH} = The smallest input voltage at which the output voltage is V_{OH}
- V_{IL} = The largest input voltage at which the output voltage is V_{OL}

The voltage gain of a comparator is the derivative of the DC transfer curve. In the ideal curve, this derivation is infinite, but in reality up to a certain amount of difference between input voltages, the comparator can not make a decision between two possible output states. Based on the above, the higher the voltage gain of the comparator, the smaller the input difference which is the minimum voltage required for the decision and also the closer to the ideal case. The voltage gain is defined as

$$A_{V=}\frac{V_{OH}-V_{OL}}{V_{IH}-V_{IL}}. \qquad (4.18)$$

The sign of the difference between the input voltages is converted to logic levels within the output swing of the comparator. Figure 4.29a is the most idealistic case and does not explain the linear amplification region of comparator. Figure 4.29b shows the amplifier property but in reality designer constantly come across a design challenge called input offset voltage as illustrated in Figure 4.29c which is the input voltage necessary to make the output equal to $\frac{V_{OH}+V_{OL}}{2}$ when the input voltages are the same.

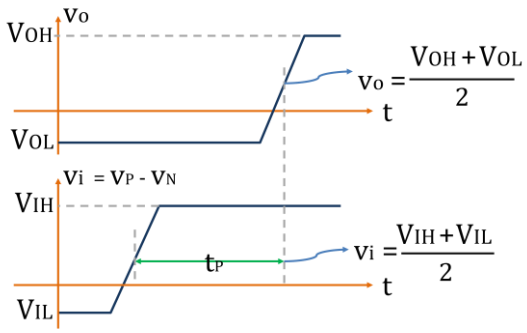


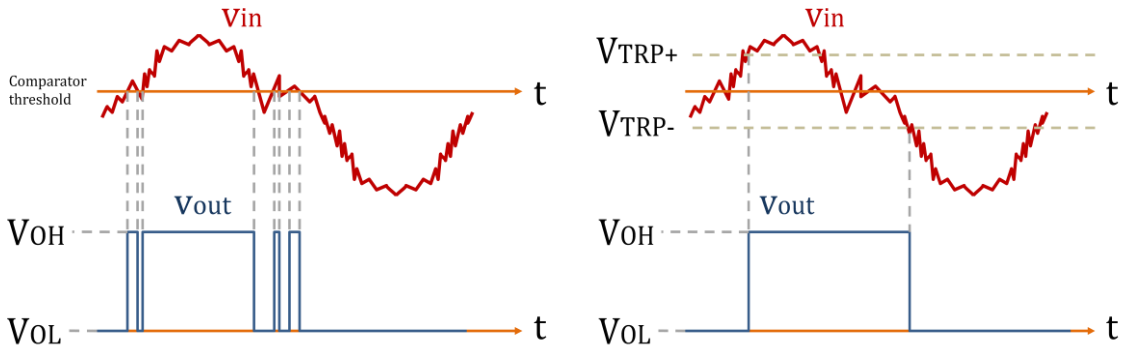
Figure 4.30. Rising propagation delay time.

The time difference between the input crossing the reference voltage and the output changing the logic state is defined as the propagation delay. Rising propagation delay time (t_{LH}) is defined as the delay time between the input and the output transition midpoints when the output is changing from low to high (Figure 4.30). Falling propagation delay time (t_{HL}) is also defined as the The delay time between the input and the output transition midpoints when the output is changing from high to low.

Propagation delay also quantifies the speed of the comparator. In receiver systems, the received data signal is demodulated by using synchronization signal and delays resulting from these digital circuitries may cause wrong data interpretation. This case increases the bit error rate (BER) which is defined as the total number of bit errors divided by the total number of transferred bits during the determined time interval. BER is unitless and often expressed as the percentage.

In noisy environments, one problem that can not be neglected is that the input signal is often corrupted with noise and/or can be fluctuating at high frequencies. Imagine that the

input voltage is so close to the reference voltage, even that small amount of noise can cause the input voltage to vary to values just above or below the reference voltage as shown in Figure 4.31a. This noise can result in incorrect data along with output glitches that consume much more power. In such applications, it may be useful to add hysteresis to the comparator's dc transfer curve. To demonstrate the need for hysteresis, consider the common application of comparators as a zero-crossing detector. Assume the signal to be processed has high frequency interference (noise) superimposed on it. When detecting the zero-crossing points of a signal, we will get errors since the signal may cross the zero axis several times for signals near zero due to the noise signal.



(a) (b)

Figure 4.31. Comparator response to a noisy signal (a) without hysteresis (b) with hysteresis.

Hysteresis is implemented in the comparator by the use of positive feedback applied externally or internally. External positive feedback is simply performed using a resistor connected from the output to the positive input of an opamp. This resistor also helps to determine the amount of hysteresis according to the amplitude of the noise superimposed to the actual data signal.

The amount of hysteresis is defined using the parameters upper trip point (V_{TRP+}) and lower trip point (V_{TRP-}). V_{TRP+} represents transition point when the signal is rising. Therefore, the comparator does not react to the falling actions in the vicinity of this point. V_{TRP-} stands for the opposite case.

4.3.2 Analog design of comparator

In high speed applications, the comparator topology has some additional circuitry to make the comparing action more sensitive. In accordance with this aim, discrete time (latched comparators, switched capacitor comparators) and continuous-time comparators are widely used topologies in the literature. In order to reduce the complexity of the topology and get rid of external switching signals and additional switching noise, continuous-time comparator with preamplifier is preferred. For the sake of clarity, the comparator will be handled as a combination of preamplifier and the decision stage.

4.3.2.1. Preamplifier Design. The basic block diagram of a comparator with preamplifier is given in Figure 4.32. The preamplifier stage improves the comparator sensitivity by increasing input signal amplitude to an acceptable level which the comparator can make a decision and isolates the input of the comparator from switching noise coming from the positive feedback stage. In latched comparators it may be preferred cross coupled topology with differential reference voltage.

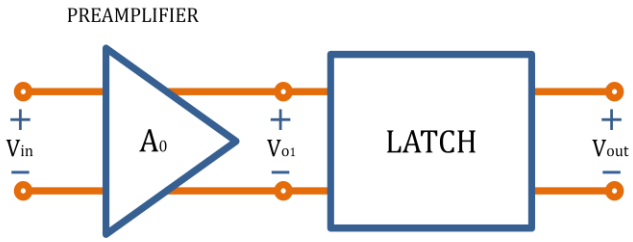


Figure 4.32. Block diagram of high-sensitive voltage comparator.

The schematic of the preamplification stage of the comparator is shown in Figure 4.33. It consists of the differential amplifier with active loads and an additional common source gain stage. The preamplifier was sized so as to meet the speed and gain bandwidth requirements for the comparator. The lengths of the input transistors were kept at minimum so as to obtain the required speed. The widths of the input transistors of the preamplifier were sized in order to obtain a sufficient gain. The type of the input transistors depend on the output waveform of the previous stage. From Figure 4.28, it can be observed that, the dc level of the output of the integrator is zero while the integration window signal is 1.2V. If the input transistors of the preamplifier vare selected as NMOS as circuit view is given in Figure 4.33, these NMOS transistors M1 and M2, turn OFF state because the output is

pulled to V_{DD} during this time interval, resulting in the input signal of the comparator to be inverted. If the signal is sufficiently amplified by the preamplifier, this problem can be solved by adding an extra inverter stage in order to flip the waveform.

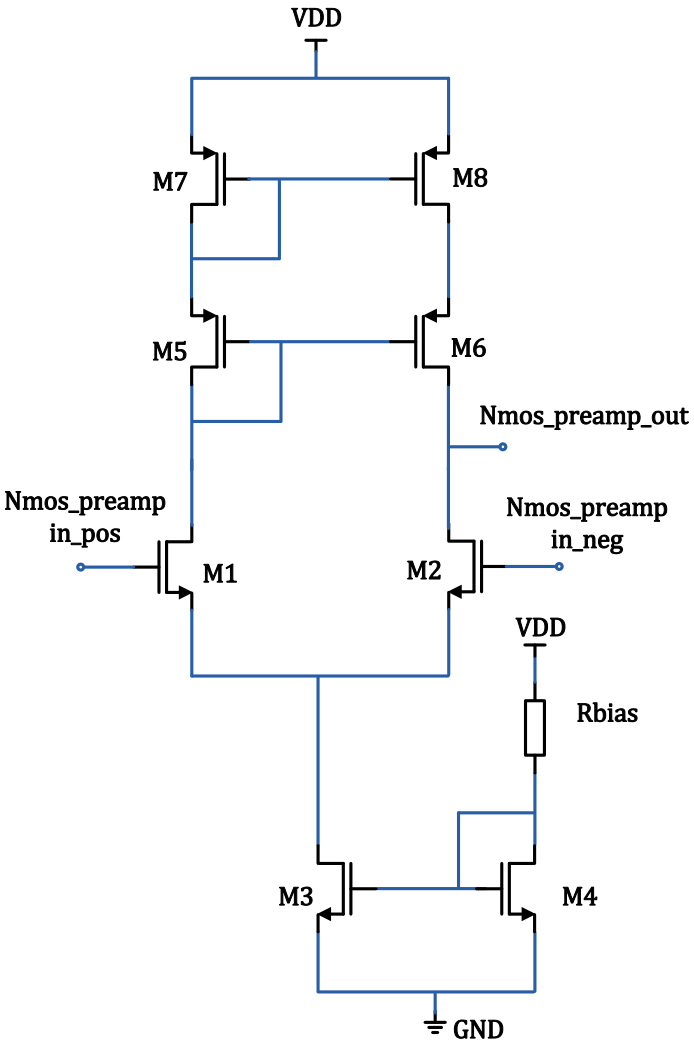


Figure 4.33. Circuit view of the NMOS input preamplifier.

In order to increase the gain, load is selected as cascode PMOS. The current flowing through the amplifying transistors is 120 µA. DC voltage gain is calculated in Equation 4.19 and also in Equation 4.20 in terms of dB.

$$A_V = g_{m2} \times \left[\left(g_{m6} \times r_{06} \times r_{03} \right) \| \, r_{02} \right] \approx 21 \tag{4.19}$$

$$A_V|_{dB} \approx 26.4 \text{ dB} \tag{4.20}$$

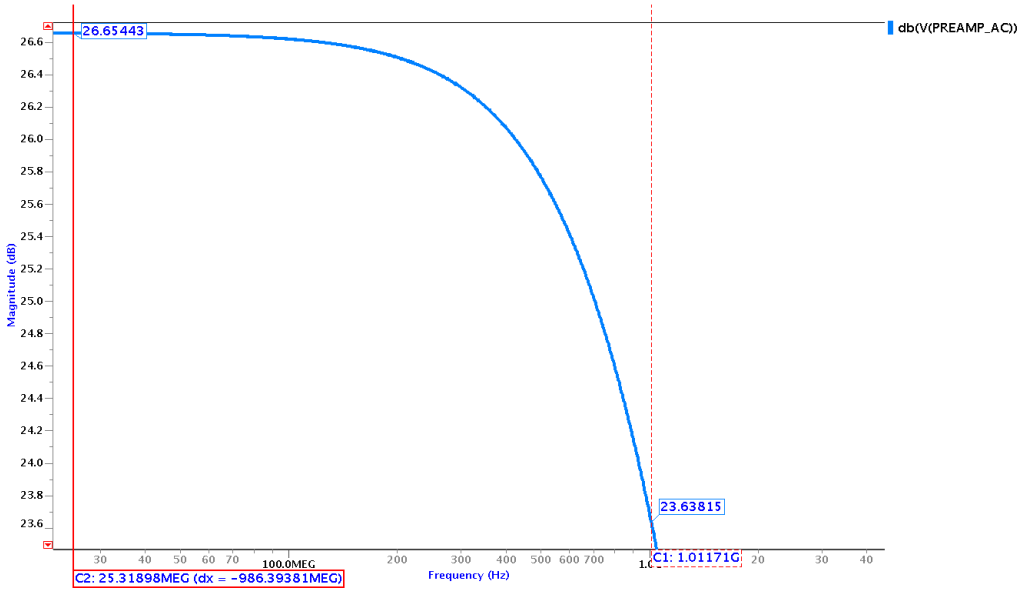


Figure 4.34. AC response NMOS input preamplifier.

The cutoff frequency is about 1 GHz which is sufficient for the baseband signal. The total DC power consumption is 400 µW except for the inverter stage.

In order to reduce the complexity of the topology, the differential signal should be converted to single-ended form for comparator and the integrated signal should be amplified without inverting. Thus, a PMOS input preamplifier is preferred as shown in Figure 4.36.

The PMOS preamplifier is simply a differential amplifier with PMOS input transistors. However, a common source amplifier is added in order to increase the gain.

The current flowing through the amplifying transistors is 692 µA. DC voltage gain is calculated in Equation 4.21 and also in Equation 4.22 in terms of dB. The total dc power dissipation is 2.69 mW.

$$A_V = \left(-g_{m2} \times (r_{02} \| r_{04})\right) \times \left(-g_{m8} \times (r_{08} \| r_{07})\right) \approx 29.5 \tag{4.21}$$

$$A_V|_{dB} \approx 30.4 \text{ dB} \tag{4.22}$$

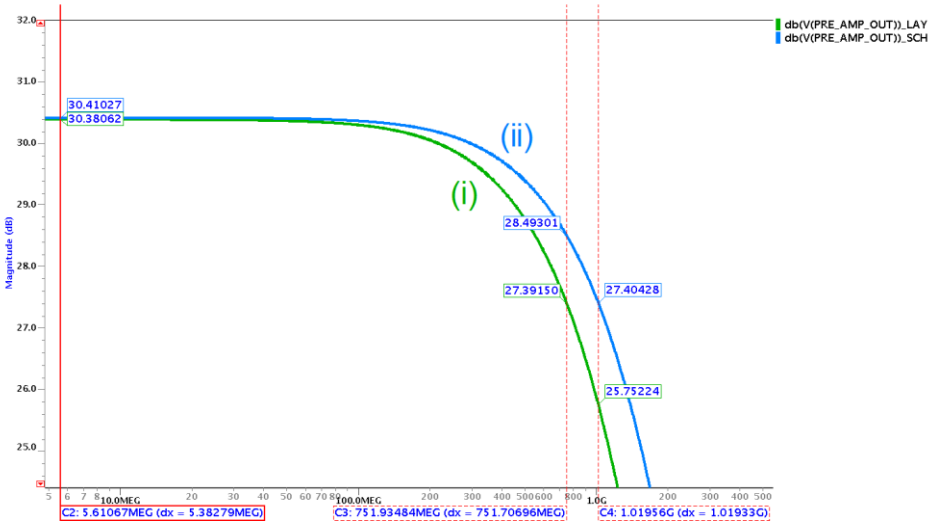


Figure 4.35. AC response of PMOS preamplifier (green curve (i): layout, blue curve (ii): schematic).

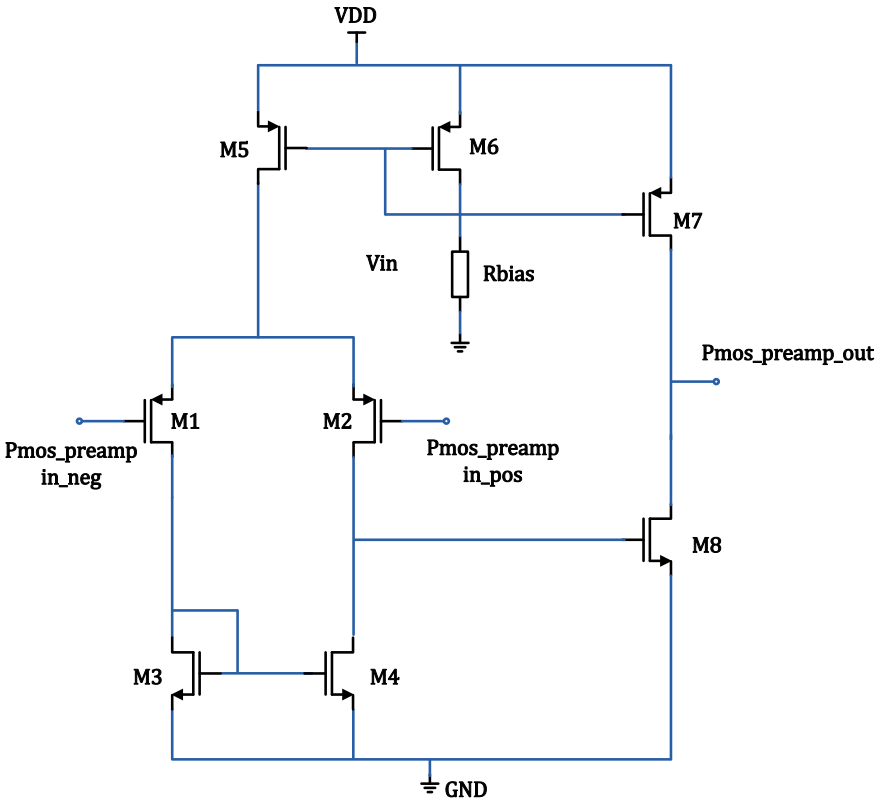


Figure 4.36. Circuit view of the PMOS input preamplifier.

As illustrated in Figure 4.35 the cutoff frequency is 1 GHz for pre-layout and 750 MHz for post-layout. This difference may result from the additional parasitic capacitance in layout. Nevertheless, the DC voltage gain almost verifies the hand calculation.

4.3.2.2. Decision Stage with Hysteresis Design. Decision stage is the heart of the comparing system and its basic functionality is to determine which of the inputs is greater. The circuit topology has a positive feedback provided by cross-gate connected transistors M3 and M4 in Figure 4.37. As will be covered later, the hysteresis is accomplished by these MOS transistors.

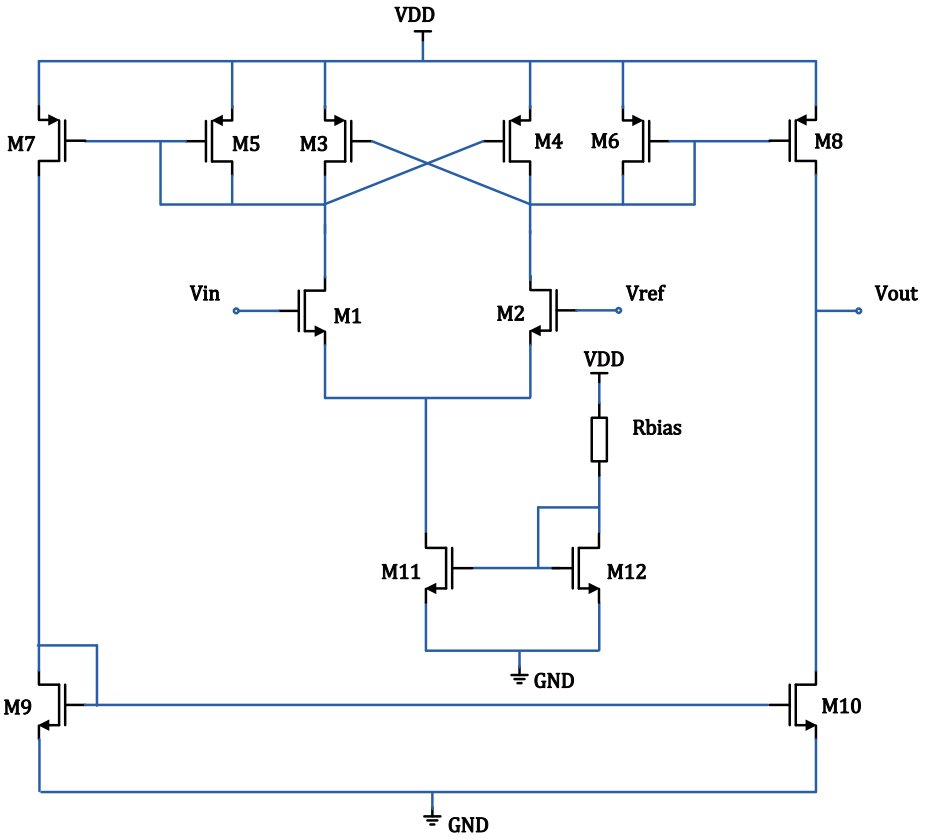


Figure 4.37. Circuit view of decision stage.

The operation principle of the decision stage will be covered by handling two possibilities; signal is larger than the reference voltage or not.

- *CASE 1* : From Figure 4.37, assume that the input signal is smaller than the reference voltage. Initially, under these biasing conditions, input transistors, M1 is OFF and M2 is ON. In parallel, M5 and M4 whose gates are connected to M1, are OFF and similarly M3 and M6 whose gates are connected to M2, are ON.

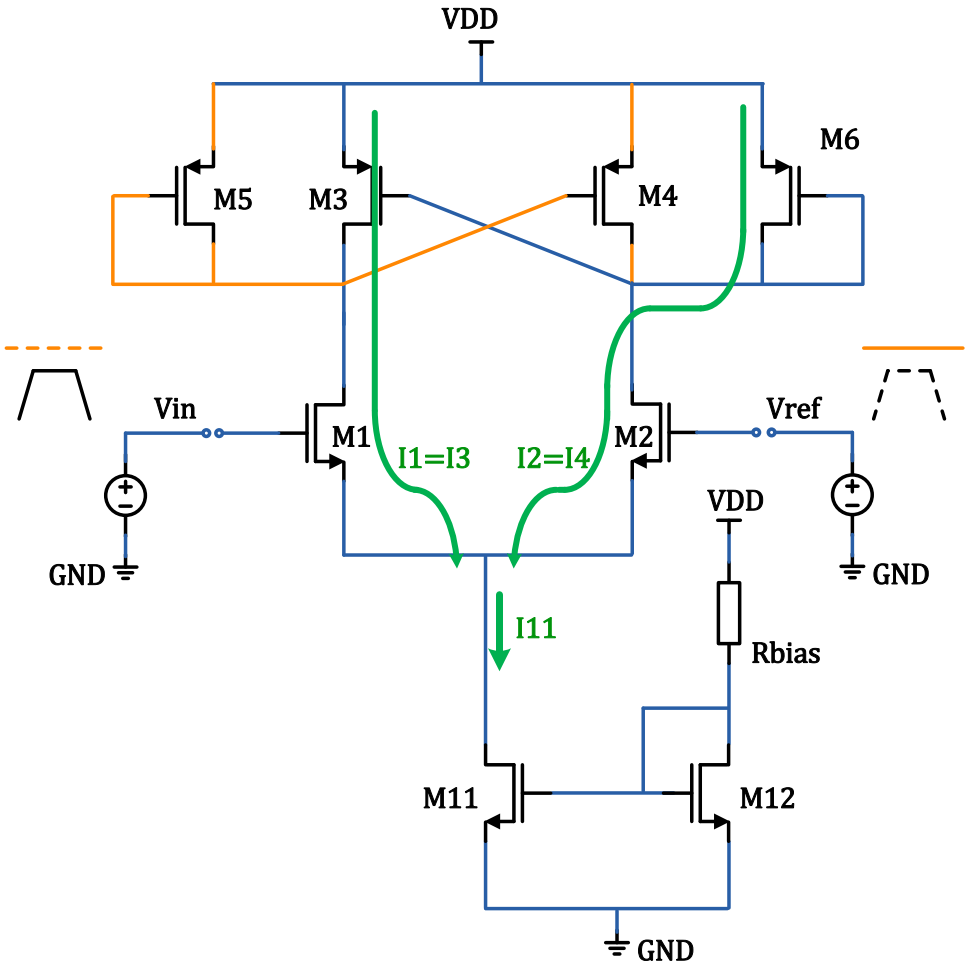


Figure 4.38. Available paths and currents for CASE 1.

M3 and M6 form a current mirror in which M6 is the mirroring transistor. The current flowing through M3 is defined as follows

$$I3 = \frac{(W/L)_3}{(W/L)_6} I6 \,. \tag{4.23}$$

Figure 4.39 illustrates how the currents change related to the input states. As the input signal increases towards the upper trip point, the current flowing through M1 (green arrow in Figure 4.38) becomes to be larger. The point (showed with marker labeled as m7), where I1 (labelled as (i) in Figure 4.39) catches I3 (labelled as (ii) in Figure 4.39), represents the upper limit of the hysteresis range as verified in Figure 4.40 (showed with marker labeled as m3). For both cases, the analysis was performed for input voltage changing from 0.8V to 0.86V when reference is 0.88V.

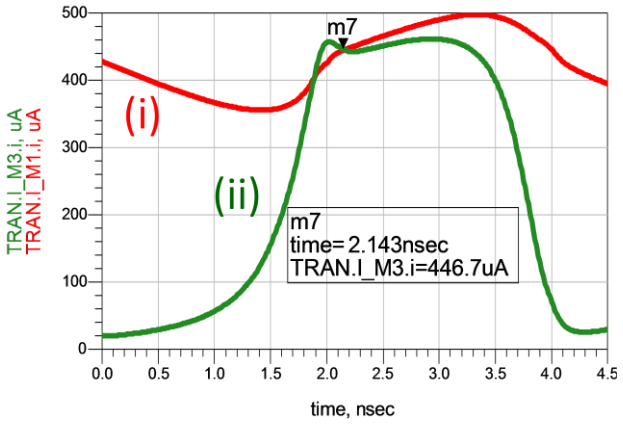


Figure 4.39. Plot of currents for CASE 1.

The current flowing through M11 (green arrow in Figure 4.38) can be written in terms of the current flowing through M6 as given in Equation 4.24.

$$I11 = I1 + I2 = I3 + I6 = \left(1 + \frac{(W/L)_3}{(W/L)_6}\right) I6 \tag{4.24}$$

As long as the values of I1 and I2 are known, the gate-source voltages can be derived from these currents.

$$V_{GS1} = \sqrt{\frac{2 \times I1}{\mu_n C_{ox} (W/L)_1}} + V_{TH1} \tag{4.25}$$

$$V_{GS2} = \sqrt{\frac{2 \times I2}{\mu_n C_{ox} (W/L)_2}} + V_{TH2} \tag{4.26}$$

$$V_{TRP+} = V_{GS1} - V_{GS2} \tag{4.27}$$

In Equation 4.25 and 4.26, μ_n, C_{ox}, V_{TH1} and (W/L) are the well known transistor parameters and can be obtained from the design kit. The gate-to-source voltages are V_{GS1} = 0.284 V and V_{GS2} =0.254 V and from Equation 4.22, V_{TRP+} = 30 mV which can be verified with Figure 4.43.

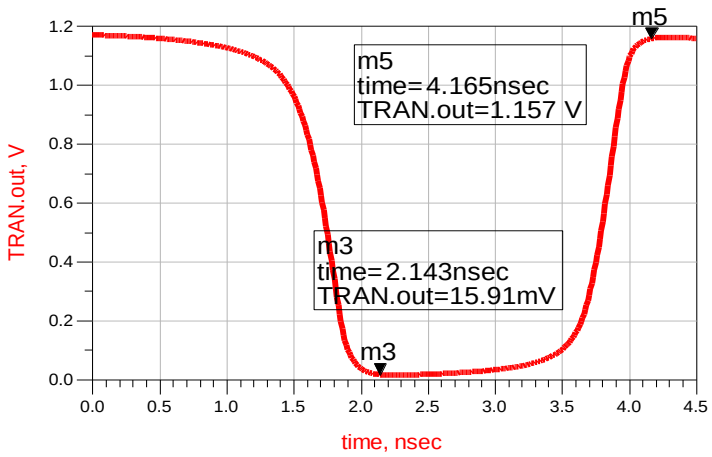


Figure 4.40. Comparator output signal.

- *CASE 2* : From Figure 4.37, assume that the input signal is greater than the reference voltage. Initially, under these biasing conditions, input transistors, M2 is OFF and M1 is ON. In parallel, M5 and M4 whose gates are connected to M1, are ON and similarly M3 and M6 whose gates are connected to M2, are OFF.

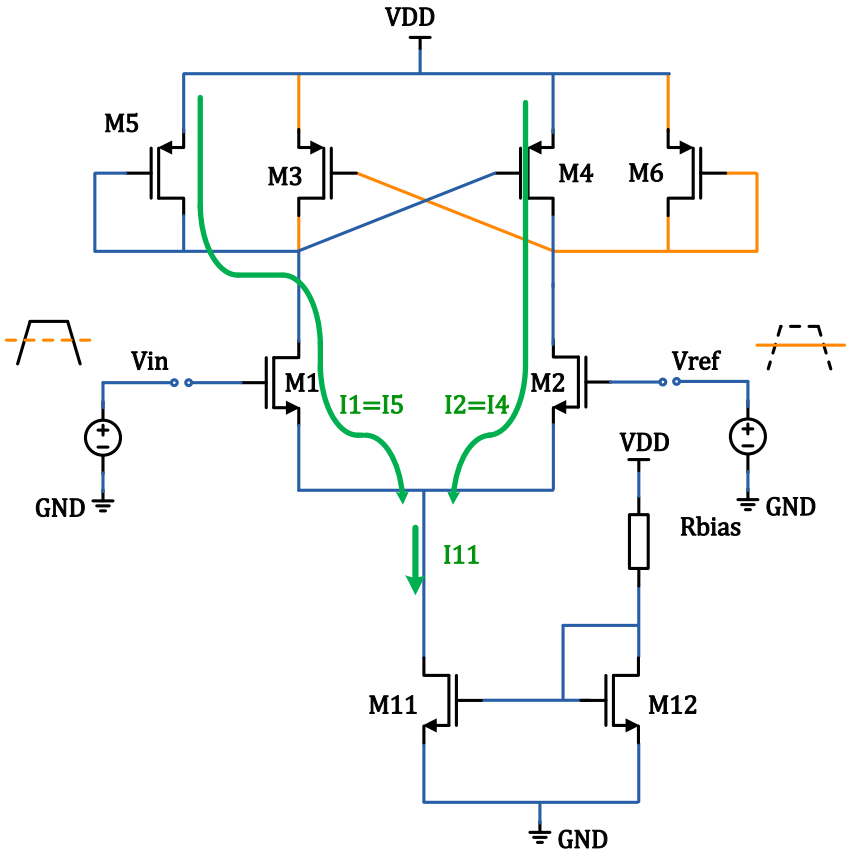


Figure 4.41. Available paths and currents for CASE 2.

M4 and M5 form a current mirror in which M5 is the mirroring transistor. The current flowing through M4 is defined as

$$I4= \frac{(W/L)_4}{(W/L)_5} I5 . \quad (4.28)$$

The variations of currents are shown in Figure 4.42. As the input signal decreases towards the lower trip point, the current flowing through M1 (orange curve in Figure 4.42) becomes smaller. The decision is made when I2 (labelled as (ii) in Figure 4.42), is equal to I4 (labelled as (i) in Figure 4.42), and this point (showed with marker labeled as m4 in Figure 4.42)represents the upper limit of the hysteresis range as verified in Figure 4.40 (showed with marker labeled as m5).

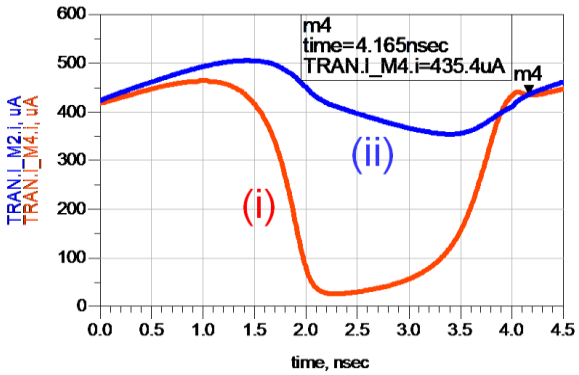


Figure 4.42. Plot of currents for CASE 2.

The current flowing through M11 (green arrow in Figure 4.41) can be written in terms of the current flowing through M5 as given in Equation 4.29.

$$I11= I1+I2= I5+I4= \left(1+\frac{(W/L)_4}{(W/L)_5}\right) I5 \quad (4.29)$$

As long as the values of I1 and I2 are known, the gate-source voltages can be derived from these currents by using Equation 4.24 and 4.25. Finally, V_{TRP-} is given by

$$V_{TRP-}=V_{GS1} - V_{GS2} . \quad (4.30)$$

The gate-to-source voltages are $V_{GS1} = 0.284$ V and $V_{GS2} = 0.254$ V from Equation 4.25 and 4.26, $V_{TRP-} = 30$ mV which can be verified with Figure 4.43.

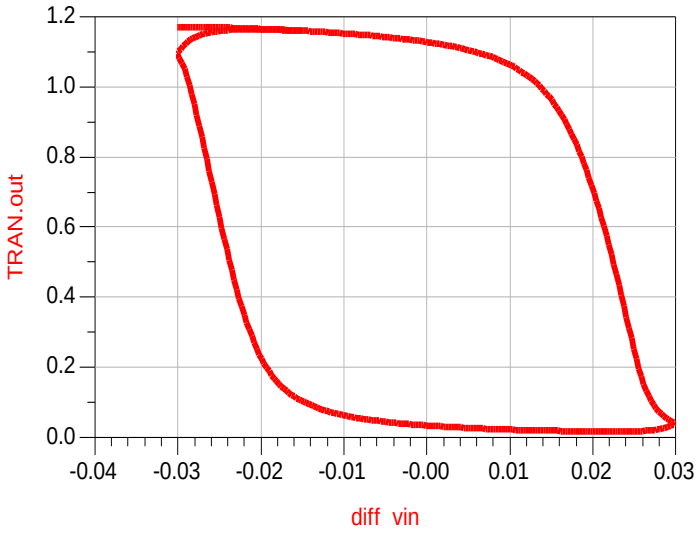


Figure 4.43. Hysteresis curve of designed comparator.

The hysteresis curve illustrated, in Figure 4.43, was observed for the case, input voltage is changing from 0.85 V to 0.91 V when reference is 0.88 V. The hystresis curve is a strong function of bias voltage and transistor sizes. As shown in Figure 4.44, for the large values of bias voltage the V_{OL} and V_{OH} are nearly constant but the width of the hysteresis becomes narrower. Moreover, from the Figure 4.44 as the width of M3 and M4 get larger, the width of the hysteresis increases.

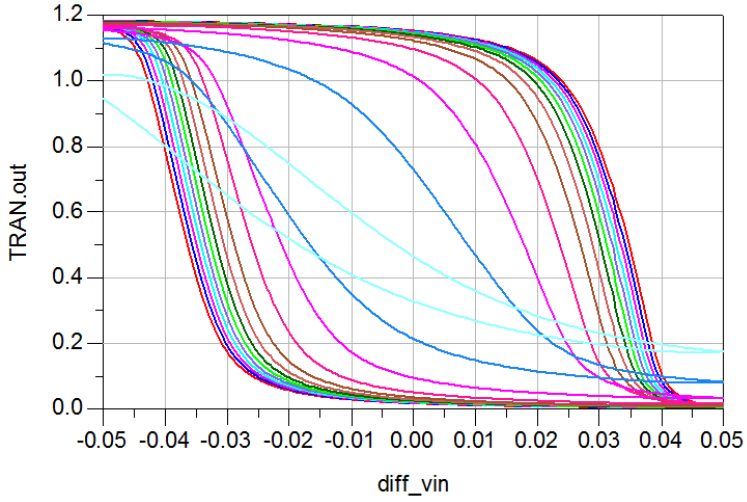


Figure 4.44. Hysteresis curves for different bias voltages.

4.3. Simulation Results of the Overall Receiver

During the design phase, some general considerations are handled and the drawbacks and deficiencies are solved within the theoretical basis. In this context, the overall system simulations demonstrate the basic operation of the receiver as will be analyzed in this section. Related with the distance the receiver works from, two different cases are considered in terms of noise; low noise and low amplitude, high noise and low amplitude.

The figures showing the transient analysis are placed as full page in the following pages without numbering, in order to make the waveforms and labels visible. The labels represent the names of the ports in the receiver. The received signal is converted to differential form by using an off-chip passive balun. The "TRANSMITTED NOISY SIGNAL" refers to one of the outputs of the balun and "CHIP OUTPUT" refers the output of the demodulator. The remaining nodes are specified clearly.

From Figure 4.45, it is easily observed that the received signal can be distinguished from the noise. 15 μV_{pp} UWB signal is applied to the input of the LNA and it amplified roughly to 0.45 mV_{pp} with relatively small in-band noise contribution ("LNA OUTPUT"). At the output node of the 5 - stage cascade RF VGA, the peak to peak signal amplitude is about 10 mV_{pp}. This is an acceptable voltage for the self mixer to multiply the signal by itself while reducing frequency band to the baseband. The mixed baseband signals with opposite signs, have an amplitude of 1.5 mV with roughly 3 mV common mode offset. This undesired offset is cancelled by using a series DC block capacitor. The value of the capacitor should be selected carefully considering the associated pole.

The baseband mixer output is integrated to detect the energy of the signal with the help of the integrator. However, the output of the integrator is not sufficient for the comparating action. Pmos preamplifier amplifies the energy of the received data signal up to 100 mV. Then, the comparator senses the difference between the signal and the applied reference signal in order to settle to one of the possible logic outputs. Finally, the demodulator (DFF) demodulates the signal with the applied synchronization clock. This scenario is simulated in 125 Mbps data rate.

Figure 4.46 shows the transient simulation of the overall receiver for the case of high noise and low signal amplitude. The noisy waveform at the input of the LNA turns up to be a cleaner one in “LNA OUTPUT”. The energy of the signal is detected after the integration phase. The resulting data is seen as “CHIP OUTPUT”. The data rate is 62.5 Mbps this time.

In Figure 4.47, the post-layout simulation results of the overall receiver are shown. The simulation is performed by connecting the individual layout blocks in the top level schematic. The data rate is 125 Mbps and according to the waveform “DFF_OUT”, the data is demodulated succesfully.

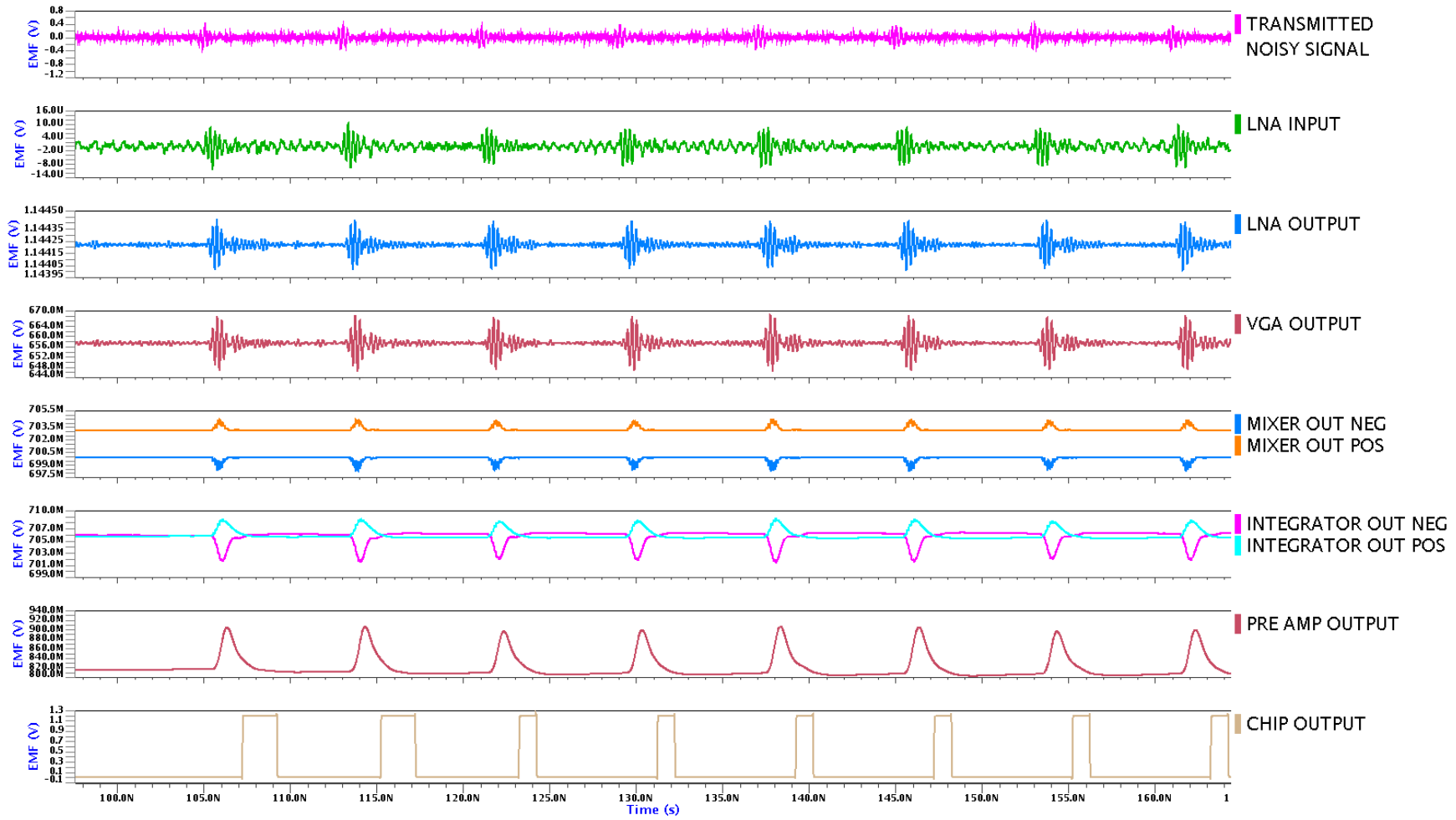


Figure 4.45. Overall transient analysis of the receiver in case of low noise & low signal amplitude (schematic).

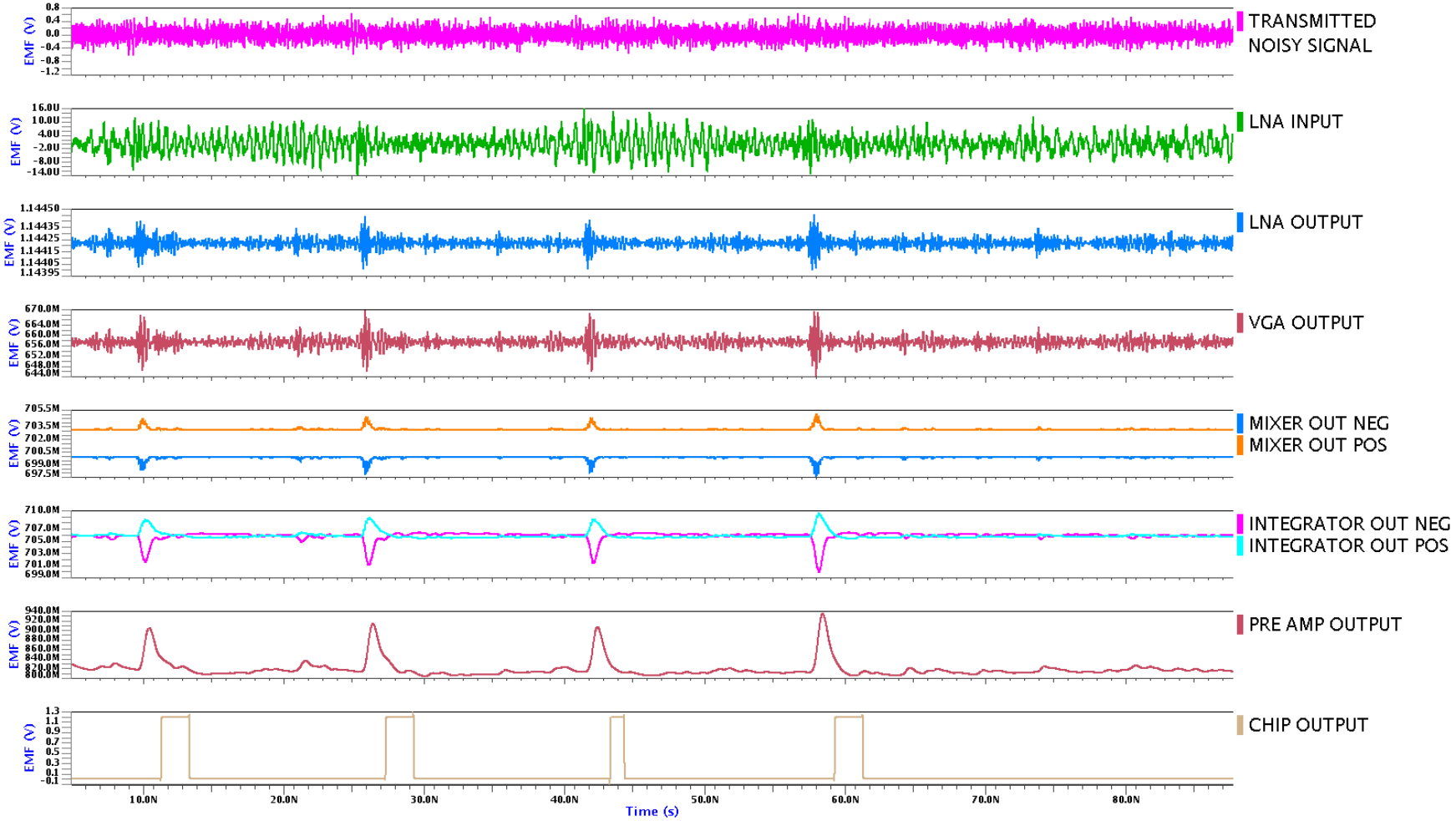


Figure 4.46. Overall transient analysis of the receiver in case of high noise & low signal amplitude (schematic).

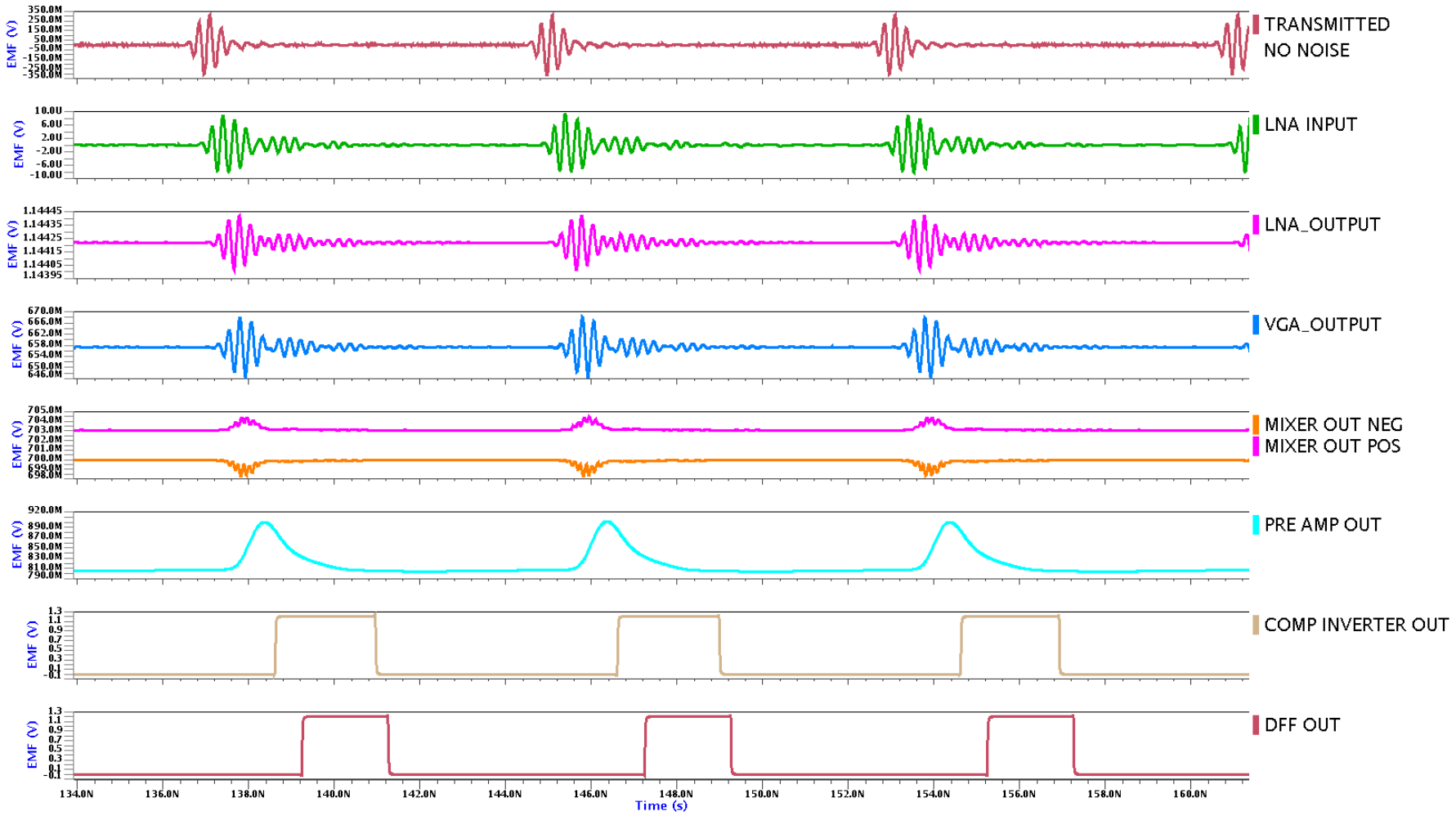


Figure 4.47. Overall transient analysis of the receiver in case of noiseless & low signal amplitude (post-layout).

5. RF PRINTED CIRCUIT BOARD DESIGN

5.1 Basics of Transmission Line Theory

In circuit theory, it is assumed that the physical dimensions of networks are not comparable with the electrical wavelength of the transmission lines. From this point of view, we can say that the voltage drop over a wire is almost zero as Kirschoff`s law tells. On the other hand, transmission lines are a considerable fraction of wavelength, so it is defined as a distributed parameter network, where voltages and currents can vary in magnitude and phase over its length [20].

All types of transmission lines are composed of two conductor and a dielectric material. Therefore, a transmission line can be modeled by using passive lumped components so that each has a physical meaning in reality, as shown in Figure 5.1. In this model, L is the total self inductance of the two conductors, C results from close proximity of the two conductors, R results from finite conductivity of the conductor and G represents dielectric loss of the insulating material.

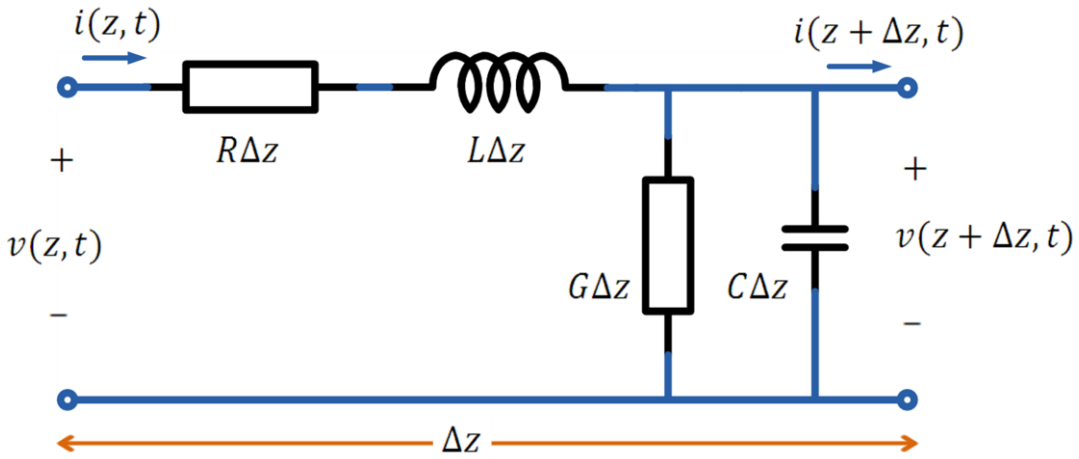


Figure 5.1. Voltage and current definitions and equivalent circuit for an incremental length of transmission line.

From the circuit in Figure 5.1, Kirchoff voltage and current laws can be applied and after some calculations, voltage-current relation is found in Equation 5.1 and 5.2 as follows

$$\frac{dV(z)}{dz} = -(R+j\omega L)\times I(z) \tag{5.1}$$

$$\frac{dI(z)}{dz} = -(G+j\omega C)\times V(z) \tag{5.2}$$

This yields the following where γ is *the complex propagation constant* and has a frequency dependency as shown in Equation 5.3 and 5.4.

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{5.3}$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{5.4}$$

$$\gamma = \alpha + j\beta = \sqrt{(R+j\omega L)(G+j\omega C)} \tag{5.5}$$

where α is called *the attenuation constant* and β is called *the propagation constant*. By using γ, we can derive the propagation of the wave as follows

$$V(z)=V_0^{+}e^{-\gamma z} + V_0^{-}e^{\gamma z}\,, \tag{5.6}$$

$$I(z)=I_0^{+}e^{-\gamma z} + I_0^{-}e^{\gamma z}\,. \tag{5.7}$$

Finally the characteristic impedance of the transmission line is found as

$$Z_0=\frac{V_0^{+}}{I_0^{+}} = -\frac{V_0^{-}}{I_0^{-}} = \sqrt{\frac{R+j\omega L}{G+j\omega C}}\,. \tag{5.8}$$

In addition to this, we can find that the wavelength on the line is

$$\lambda = \frac{2\pi}{\beta}, \tag{5.9}$$

whereas the phase velocity is

$$v_p = \frac{\omega}{\beta} = \lambda f. \tag{5.10}$$

5.2.1. Terminated Lossless Transmission Lines

In the case of terminating a transmission line with an arbitrary load Z_L as shown in Figure 5.2, the reflection from the load can be derived with the help of Equation 5.11 and 5.12.

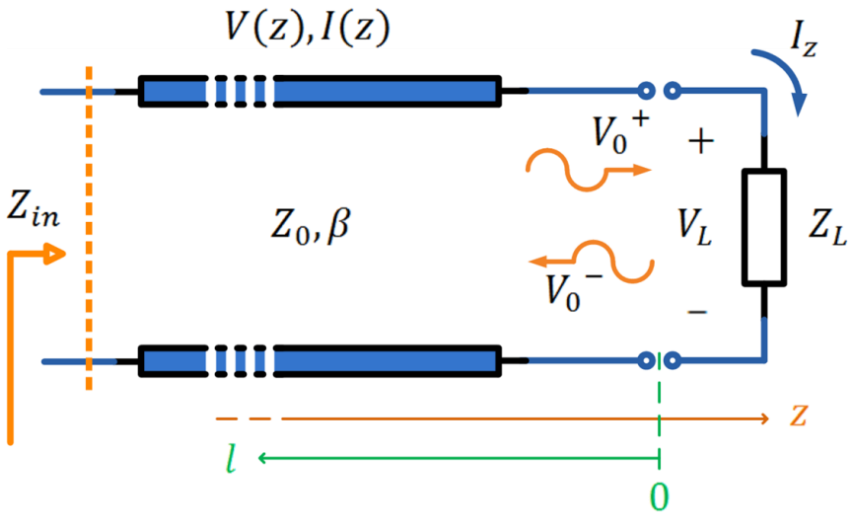


Figure 5.2. A view of a transmission line terminated with load impedance Z_L.

It has been stated above before that the ratio of voltage to current corresponds to Z_0 (characteristic impedance) over the transmission line and Z_L at the load. At point $l = 0$,

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_0^+ + V_0^-}{I_0^+ - I_0^-}, \tag{5.11}$$

$$V_0^- = \frac{Z_L + Z_0}{Z_L - Z_0} V_0^+ . \quad (5.12)$$

Equation 5.12 can be written as the ratio of the amplitude of the reflected voltage wave normalized to the amplitude of the incident wave and this ratio is defined as *voltage reflection coefficient*, Γ:

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} . \quad (5.13)$$

From Equation 5.11 and 5.12, it is seen that the voltage and current over a wire is the superposition of the reflected and incident waves called standing waves. $\Gamma = 0$ means that there is no reflected wave and also the power delivered to the load is maximum. To obtain this condition, Z_L and Z_0 must be equal where Z_L said to be matched to the line.

The case of $Z_L \neq Z_0$ is called mismatch and also means that not all the available power is delivered to the load. This loss is called *return loss* (RL) and defined as

$$RL = -20 \log|\Gamma| \, [dB] . \quad (5.14)$$

For $|\Gamma| = 0$, return loss is ∞ and there is no reflected power. On the other hand, if $|\Gamma| = 1$, return loss will be 0 and all the power will be reflected back which is the worst case for such a transmission line.

At any point on a transmission line, the incident wave and the reflected wave is superimposed. If $|\Gamma| = 0$, there is no reflected wave and the signal at any point only represents the incident wave. Under this condition, the voltage at point z, $|V(z)| = |V_0^+|$. If $|\Gamma| \neq 0$ we have to take into account the reflected wave.

The combination of forward and reverse travelling waves produce a *standing-wave*, which is so-called because the positions of maxima and minima of the signal do not vary

with time. The actual shape of this standing wave is a function of the load impedance. The standing wave ratio can be defined in Equation 5.15.

$$SWR = \frac{|V_{max}|}{|V_{min}|} = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{5.15}$$

The reflection coefficient makes easier to calculate the input impedance at any point. The input impedance looking into the line at a point which is far from the load by length l, is derived in Equation 5.16.

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan\beta l}{Z_0 + jZ_L \tan\beta l} \tag{5.16}$$

This results gives us the input impedance of a transmission line with length l, with an arbitrary load impedance (Notice that $\alpha=0$ is valid for lossless line and the impedance is defined only with β).

The term βl is called the *"electrical length"* of the transmission line. Some special cases to consider are

Table 5.1. Input and output impedances of various types of lines.

	Z_{in}	Z_L	βl
Shorted line	$jZ_0 \tan\beta l$	0	varying
Open Line	$jZ_0 \cot\beta l$	∞	varying
Quarter-Wave Line	Z_0^2 / Z_L	varying	90 °
Half-Wavelength Line	Z_L	varying	180 °

5.2 Synthesis of Transmission Line on PCB

Besides being widely used, printed transmission lines are broadband in frequency. It is easy to produce the overall system on a PCB which is compact and light in weight. They are generally economical to produce since they are readily adaptable to hybrid and monolithic integrated-circuit (IC) fabrication technologies at RF and microwave frequencies.

Physically, transmission lines are realized with two conductors and a dielectric material in a basic manner. Therefore, electrical properties of these elements become crucial at high frequencies. In addition to this, the requirements of the application or the manufactured IC tells which kinds of techniques and transmission lines are needed for the optimum design. For instance, for RF applications, losses due to the PCB are vital and affect directly the basic operation of the system. However, for an analog-to–digital converter IC operating on the order of MHz, the mismatches on the wire may be negligible.

At first glance, what we should consider in depth in designing a printed circuit board working at high frequencies, can be sorted as the following,

- Determining a dielectric material which has a stable frequency response at least within the band of interest.
- Determining the type of the transmission line depending upon the pin thickness of the manufactured IC, the ground plane, and the desired port impedance.
- Determining the dimensions of the dielectric and copper layers in order to have the intended impedance.
- Comparing the transmission lines with the calculated properties and dimensions for different dielectric materials by using an EM simulator by means of s-parameters, characteristic impedance, etc.

5.2.1 Optimum Dielectric Material For High Frequency PCB Design

During the several years prior to the 1990’s many high end laminates were developed for use in RF/Analog circuits, especially for military applications. Most of these materials are expensive and a considerable number of them are not applicable for multilayer boards. On the other hand, most of the RF/Analog circuits developed do not require boards with a high number of layers. During that same period all digital circuits and low frequency analog circuits were tested on FR4 based boards.

Through the 1990's and into this century, improved boards for high frequency and high speed circuitries have become necessary. As the commercial end of the RF/analog industry has dramatically increased in size, attention has been sharply drawn to the need to produce high end RF/Analog laminates without the *"high end"* price tag [21].

RF/Analog circuits usually process precision and/or low level signals. Hence, these circuits require much tighter control of parameters pertaining to signal losses. The two losses of greatest concern are losses caused by signal reflections, due to impedance mismatch or impedance changes and the loss of signal energy into the dielectric of the material. Some critical applications also need to focus on losses due to *"skin effect"*. Impedance variations result from two causes, material parameters that vary with changes in frequency or temperature and variations in the processes at the manufacturer. The amount of signal lost into the dielectric is a function of the material's characteristics. Skin effect can be partially controlled through choice of copper type in or on the PC board. Material choice can have a major impact on all these sources of energy loss. As a result, materials geared to the RF/Analog domain tightly control parameters such as dielectric thickness, dielectric constant, loss tangent and even copper type. Each one of these key parameters has a considerable amount of contribution on the overall high frequency response of the dielectric material. Each contribution can be specified as follows

- *The relative permittivity (ϵ_r)*: The higher the relative permittivity, the slower a signal travels on a trace as mentioned before, the lower the impedance of a given trace geometry and the larger the stray capacitance along a transmission line. Given a choice, lower dielectric constant is nearly always better. Relative permittivity varies with frequency in all materials. In some materials, the variation is small enough so that it can be ignored even in very sensitive applications. Some materials, like FR4, have broad variations in ϵ_r with changes in frequency.

- *Dielectric Thickness and Trace Width*: Both of these parameters play a key role in transmission line impedance. Control of each is necessary during fabrication of the board, with the greatest degree of control needed for high frequency analog circuits.

How much these parameters vary is a function of both process control by the manufacturer and selection of the base material.

Table 5.2. Comparison of mostly used dielectric materials.

	ϵ_r (dielectric constant)	**tan δ (loss tangent)**
***Rogers® RT/duroid 5880* [22]**	***2.2 ± 0.02***	***0.0004 - 0.0009***
Rogers® RT/duroid 5870 [22]	2.33 ± 0.02	0.005 - 0.0012
Rogers® RT/duroid 6202 [22]	2.94 ± 0.04	0.0012
FR4-epoxy [23]	4.2 - 4.9	~0.02
Alumina (Al_2O_3) [23]	8.5 – 10	~0.002
LTCC [23]	5.7 - 9.1	0.0012 - 0.0063
LCP [23]	2.9 - 3.2	0.002 - 0.0045

Table 5.2 shows the comparison between widely used dielectric materials in RF and high frequency applications. FR4 is the most attainable substrate in Turkey, on the other hand, its dielectric constant variations over the frequency is considerably large among all these materials. Alumina has the largest dielectric constant and it is more fragile than the others. Rogers® materials are widely used in designing complex microwave structures which are mechanically reliable and electrically stable but not cost-effective.

The italic row in Table 5.2. shows that Rogers® RT/duroid 5880 has considerably small dielectric constant and loss tangent. As the loss tangent increases, the dielectric loss becomes more important than the others such as conductor loss. Basically, this situation can be explained in terms of electromagnetic (EM) waves. The portion of an electromagnetic wave inside the dielectric substrate is distorted while it travels through the transmission line and this causes a loss on the signal. At this point, one point that should not be ignored is the dielectric constant variations over the frequency, in such a way that

this is actually a huge drawback for wideband applications. The dielectric constant of FR4 fluctuates much more with respect to that of LCP as shown in Figure 5.3 and is not preferred if possible for this reason.

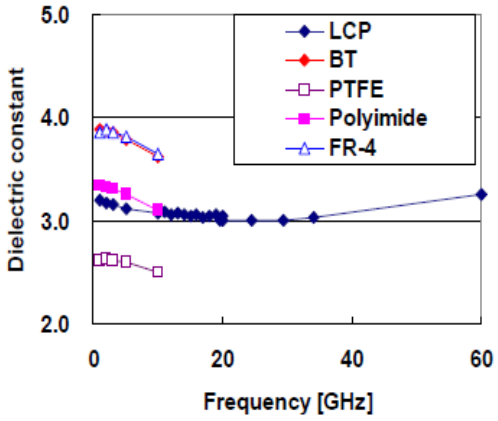


Figure 5.3. Dielectric constant variation over frequency for different materials [24].

In Figure 5.3, it is shown that LCP has the best characteristics with its nearly unchanged dielectric constant variations over frequency. At low frequencies, the dielectric constant tends to go down and it becomes relatively constant as the frequency rises. From this point of view, we can say that each dielectric material has an optimum frequency range where it shows more stable response.

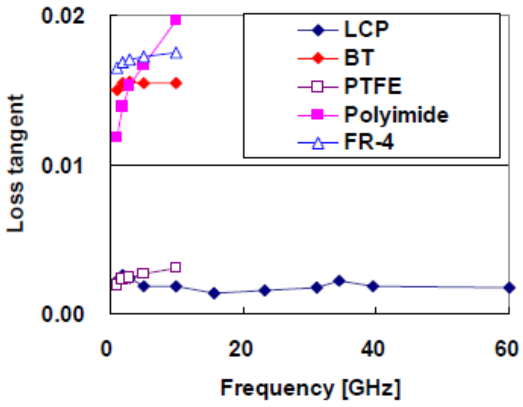


Figure 5.4. Loss tangent variation over frequency for different materials [24].

What has been mentioned for dielectric constant variation over the frequency is almost the same for loss tangent as shown in Figure 5.4. LCP still has the most stable characteristics in terms of loss tangent. FR4 is not as good compared to LCP but almost the

same for the operating frequency band of UWB. Nevertheless, it has high loss tangent which causes relatively higher dielectric loss with respect to the other materials shown in Figure 5.4. In addition to this, Polyimide varies fairly even within the UWB band.

When we zoom into Figure 5.3 and 5.4 up to 10 Ghz in order to do a further analysis on the material within the band of operation, Figure 5.5 and 5.6 can be obtained.

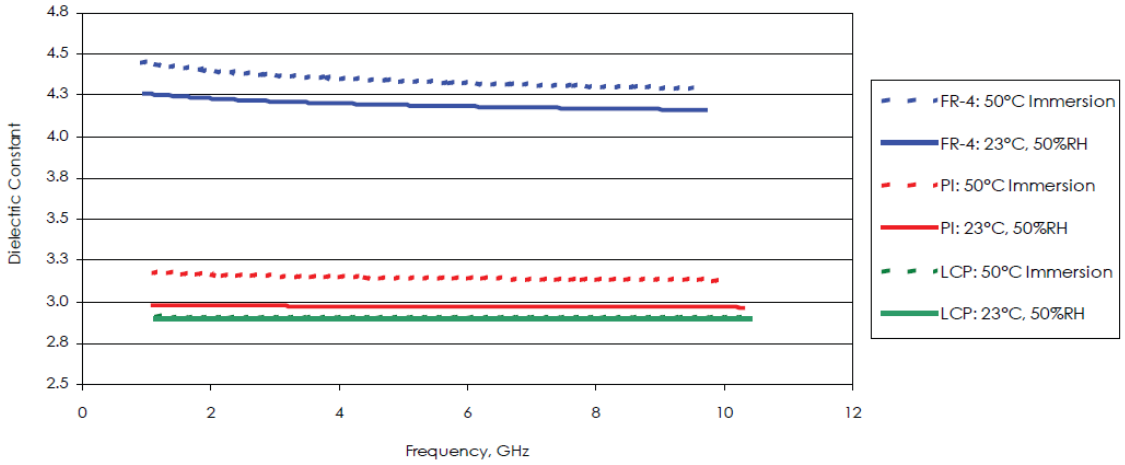


Figure 5.5. Dielectric constant vs frequency for LCP, All Polyimide, and FR-4 laminates [22].

From these figures, it is interpreted that, LCP has the minimum dissipation factor and dielectric constant and the most stable characteristic over UWB frequency band. Additionally, temperature and humidity variations are not crucial for LCP.

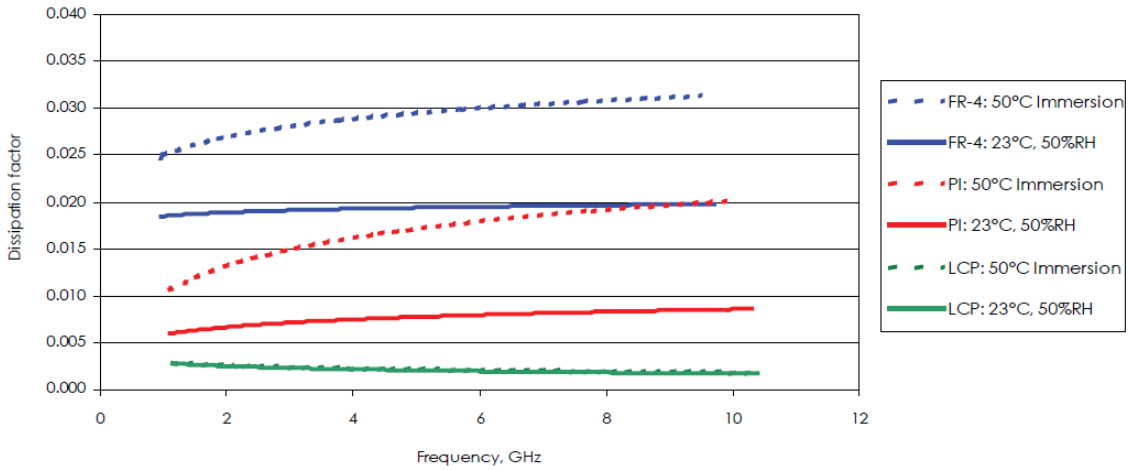


Figure 5.6. Insertion loss vs frequency for a LCP, All Polyimide, and FR-4 laminates [22].

5.2.2 Types of Transmission Lines

The optimum dielectric substrate makes sense if the correct type of the transmission line is used for such an a application.

Table 5.3. A comparison of various transmission-line types [25].

	Q factor	**Radiaton**	**Dispersion**	**Impedance Range**	**Chip Mounting**
Microstrip (dielectric) (GaAs, Si)	250 100 to 150	Low High	Low	20 to 120	Difficult for shunt, easy for series
Stripline	400	Low	None	35 to 250	Poor
Suspended stripline	500	Low	None	40 to 150	Fair
Slotline	100	Medium	High	60 to 200	Easy for shunt, difficult for series
Coplanar waveguide	150	Medium	Low	20 to 250	Easy for series and shunt
Finline	500	None	Low	10 to 400	Fair

The upper and the lower limit of any property listed in Table 5.3 varies between different transmission lines. For instance, 50 Ohm impedance can not be obtained by using the slotline or the useful type of a line may not be attained or fabricated. Therefore, in the next section, some of the mostly preferred and easily fabricated transmission line types are explained.

5.2.2.1. Microstrip Lines. The microstrip line is a transmission line geometry with a single conductor trace on one side of a dielectric substrate and a single ground plane on the opposite side. Since it is an open structure, microstrip line has a major fabrication advantage over stripline. It also features ease of interconnections and adjustments.

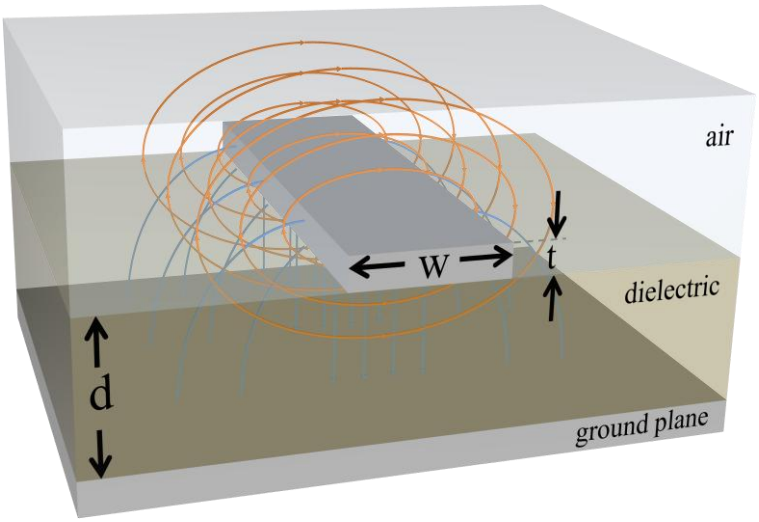


Figure 5.7. A view of a microstrip line with H (orange arrows) and E (blue arrows) fields.

In a microstrip line, the electromagnetic (EM) fields travel partly in the air above the dielectric substrate and partly within the substrate itself as seen in Figure 5.7 [26].

In a microstrip line, the wavelength, λ, is given by

$$\lambda = \frac{c}{f\sqrt{\epsilon_{eff}}} \tag{5.17}$$

where c is the speed of light, f denotes frequency, and the ϵ_{eff}, the effective dielectric constant, which depends on the dielectric constant of the substrate material and the physical dimensions of the microstrip line and can be derived as follows

$$\epsilon_{eff} = \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2} \times \frac{1}{\sqrt{1+12\frac{d}{w}}} \tag{5.18}$$

where, d and w are dielectric thickness and trace width, respectively, as illustrated in Figure 5.7. Intuitively, the effective dielectric constant of the line is expected to be greater than the dielectric constant of air and less than that of the dielectric substrate resulting from the hybrid TEM mode assumption. According to this assumption, the microstrip line is

assumed to extend in one type of medium which has a dielectric constant of ϵ_{eff}. By doing this, the discontinuity at the dielectric-air boundary is neglected.

In order to calculate the characteristic impedance or dimensions of the line, two choices exist. Equation 5.19 gives the value of the characteristic impedance for given line dimensions and Equation 5.20 is a function of characterictic impedance and effective permittivity which leads to width to dielectric thickness ratio as follows

$$Z_0=\begin{cases}\dfrac{60}{\sqrt{\epsilon_{eff}}}\ln\left(\dfrac{8d}{W}+\dfrac{W}{4d}\right), & \text{for } W/d\leq 1\\ \dfrac{120\pi}{\sqrt{\epsilon_{eff}}[W/d+1.393+-0.667\ln(W/d+144)]}, & \text{for } W/d\geq 1\end{cases} \tag{5.19}$$

$$\frac{W}{d}=\begin{cases}\dfrac{8e^{A}}{e^{2A}-2}, & \text{for } W/d<2\\ \dfrac{2}{\pi}\left[B-1-\ln(2B-1)+\dfrac{\epsilon_r-1}{2\epsilon_r}\left\{\ln(B-1)+0.39-\dfrac{0.61}{\epsilon_r}\right\}\right], & \text{for } W/d>2\end{cases} \tag{5.20}$$

where

$$A=\frac{Z_0}{60}\sqrt{\frac{\epsilon_r+1}{2}}+\frac{\epsilon_r-1}{\epsilon_r+1}\left(0.23+\frac{0.11}{\epsilon_r}\right), \tag{5.21}$$

$$B=\frac{377\pi}{2Z_0\sqrt{\epsilon_r}}. \tag{5.22}$$

In addition to this, dielectric and conductor loss can be calculated by using Equation 5.23 and 5.24, respectively.

$$\alpha_d=\frac{k_0\epsilon_r(\epsilon_r-1)\tan\delta}{2\sqrt{\epsilon_{eff}}(\epsilon_r-1)}\left[\frac{Np}{m}\right] \tag{5.23}$$

$$\alpha_c = \frac{R_s}{Z_0 W} \left[\frac{Np}{m}\right] \tag{5.24}$$

One thing that should be added to Equation 5.23 and 5.24 for further accuracy, is to multiply them by the *filling factor* because of the fact that fields around the microstrip line are partly in the air and partly in the dielectric as mentioned above.

$$\text{filling factor} = \frac{\epsilon_{eff}(\epsilon_r - 1)}{\epsilon_r(\epsilon_{eff} - 1)} \tag{5.25}$$

5.2.2.2. Coplanar Waveguides with Ground (CPWG). The coplanar waveguide is another transmission line composed of a signal trace, component side ground planes extending in parallel to the signal trace on one side of a dielectric substrate and a single ground plane connected to the component side ground planes with plated through vias on the opposite side (Figure 5.8). The main advantage of this structure is that it is possible to achieve small trace geometries with 50 Ohm characteristic impedance.

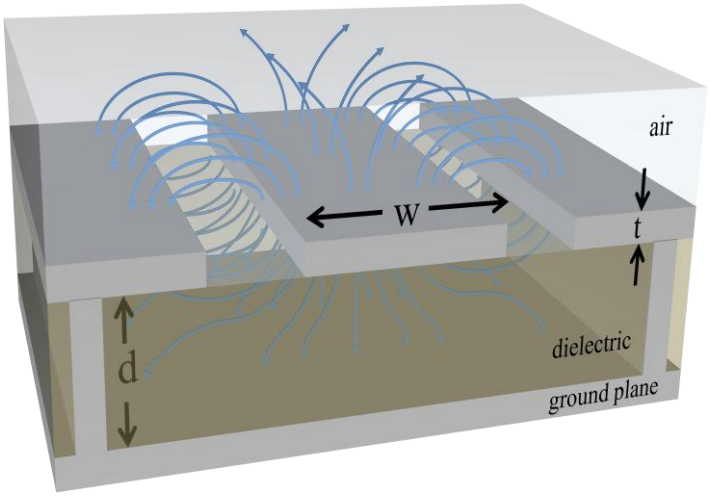


Figure 5.8. A view of a grounded coplanar wave guide with E field distribution.

$$Z_0 = \frac{60 \times \pi}{\sqrt{\epsilon_{eff}}} \frac{1}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}} \tag{5.26}$$

In Equation 5.26, K(k) is the symbol for complete elliptical integral of the first kind which is used to define the characteristic impedance of CPWG. The coefficient k equals to width / (width+2×gap) where width (w) refers the trace width and the gap (g) represents the distance between the ground planes extending on both sides of the trace. Both 'k' and 'k_1' are functions of trace geometries (w, g, h) as given in Equation 5.28 and 5.29 where h is the thickness of the substrate in.

$$\epsilon_{eff}= \frac{1+\varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1+\frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}} \tag{5.27}$$

The parameter, ϵ_{eff} is effective dielectric constant explained in microstrip transmission lines as given Equation 5.27.

$$k'=\sqrt{1-k^2}\ ;\ k_1'=\sqrt{1-k_1^2} \tag{5.28}$$

$$k_1= \frac{\tanh\left(\frac{\pi\times w}{4\times h}\right)}{\tanh\left(\frac{\pi\times g}{4\times h}\right)} \tag{5.29}$$

5.3 Designed PCB Structures

In high frequency applications, microstrip structures such as filters, baluns, passive components, etc are widely used because of their stable response over the frequency. Many passive components can be a solution for off-chip integration of an RF circuit. Nevertheless, especially in the realm of the mm-wave (basically refers to the RF technology where the wavelength is on the order of mm.) technology, packaged passive elements are not preferred because of their high loss.

Besides, the passive components, the PCB routing is crucial issue in terms of loss. In a PCB, there are several considerations which makes transmission line design necessary. The IC lead widths are less than 1 mm. Therefore, it is challenging to connect the leads to

the RF connectors while trying to keep the signal lines away from each other to reduce the coupling effects. On the other hand, thin lines act as an inductor at such frequencies. This additional inductor has a negative effect on the operation of the integrated circuits. Finally, whatever type of the transmission line is used, the length of the line should be kept small because of the fact that the insertion loss of a wire is directly proportional to this parameter.

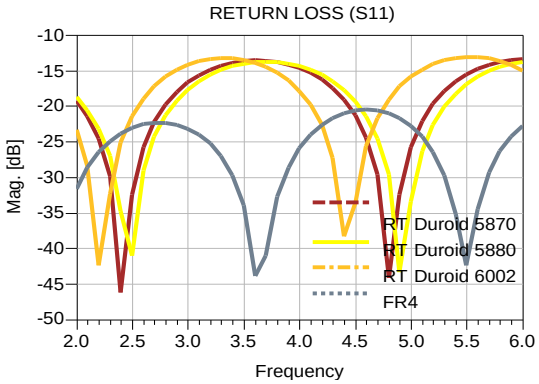


Figure 5.9. Return loss of a microstrip line with RT Duroid 5870, 5880, 6002 and FR4.

The performance of microstrip line structures depends strongly on the property of the substrate. For different substrates, return loss (S_{11}) variations over frequency are plotted in Figure 5.9 and Figure 5.10. The copper thickness is 35 μm and the substrate thickness is 1.6 mm. The rest of the microstrip line properties used in simulations are provided in Table 5.4.

Table 5.4. Microstrip line properties for 50 Ω characteristic impedance.

	Width [mm]	**tanδ**	**ϵ_r**
Alumina	1.49	0.002	10
LCP	3.93	0.003	3
PTFE	4.33	0.004	2.6
RT Duroid 5870	4.65	0.0012	2.33
RT Duroid 5880	4.82	0.0009	2.2
RT Duroid 6002	3.98	0.0012	2.94
FR4	2.94	0.02	4.5

The widths were calculated for 50 Ω characteristic impedance. As can be seen, the width is inversely proportional to the effective permitivity. The return losses are almost the same and less than -12 dB. But for FR4 and Alumina they reach up to -20 dB, according to the analysis of Figure 5.9 and Figure 5.10.

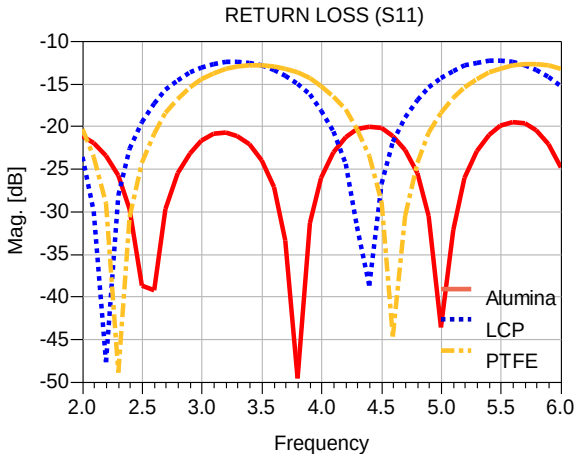


Figure 5.10. Return loss of a microstrip line with Alumina, LCP and PTFE.

Figure 5.11 depicts the insertion loss of microstrip lines with different substrates. From this figure, it can be observed that FR4 has the worst insertion loss despite its relatively good return loss. These results also summarize why FR4 is not preferred in RF applications. However, FR4 is the easiest material to attain in Turkey. Therefore, all measurements are performed on FR4 substrate.

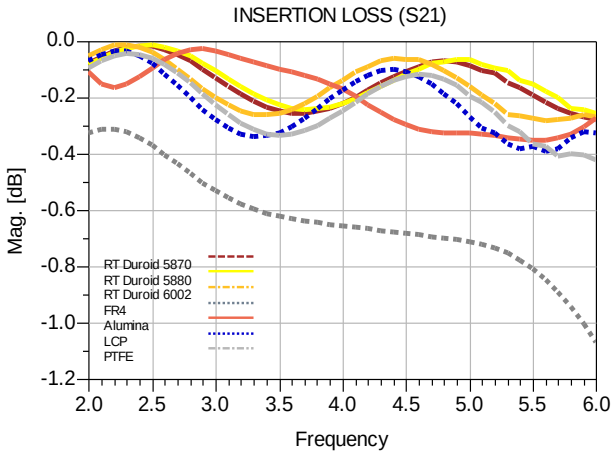


Figure 5.11. Insertion loss of a microstrip line with RT Duroid 5870, 5880, 6002, FR4, Alumina, LCP and PTFE.

In Figure 5.12, the fabricated microstrip line with FR4 substrate is presented. The trace width is calculated as 4 mm for 50 Ω characteristic impedance. The length of the trace is selected to be equal to wavelength at 4 GHz which corresponds to $\lambda = 4.37$ cm.

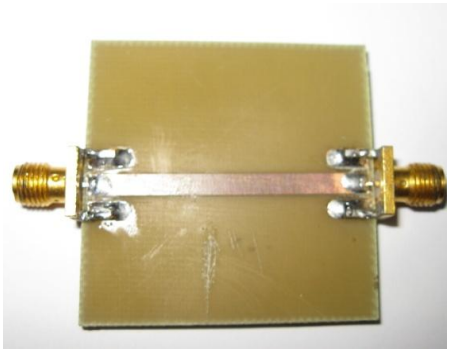
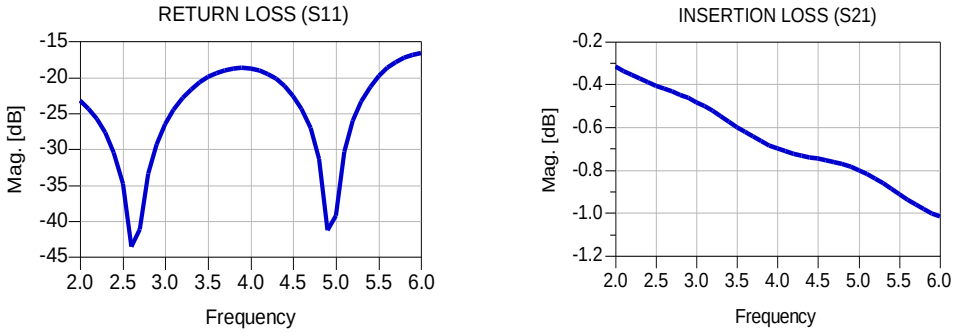


Figure 5.12. The fabricated microstrip line with FR4 substrate.

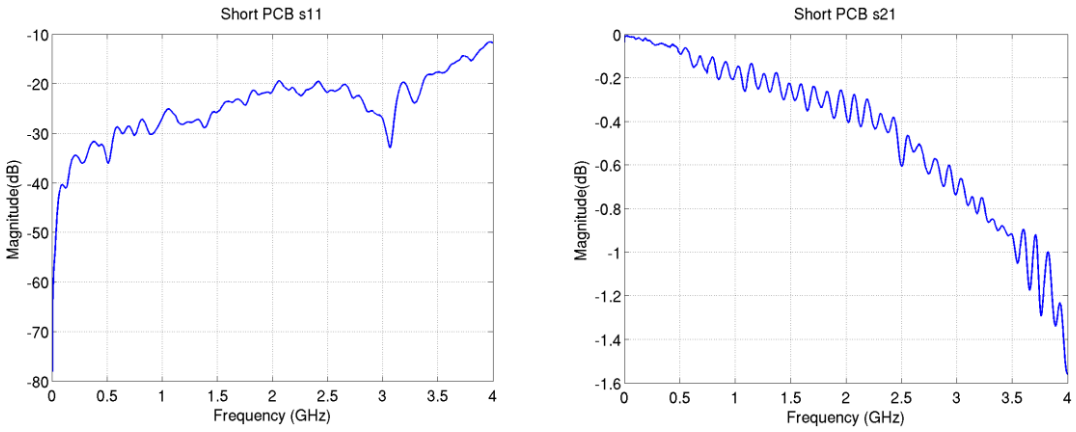
The simulation results of the fabricated microstrip in Figure 5.13, show that reflections on the signal are negligible, and the loss is about 0.7 dB at 4 GHz.



(a) (b)

Figure 5.13. Simulation results of microstrip line with FR4 substrate. (a) Return loss (b) Insertion loss.

The measurement results of the fabricated microstrip are shown in Figure 5.14. The return loss is less than -10 dB (Figure 5.14a) which means that the reflections are tolerable. The insertion loss is about -1.5 dB as shown in Figure 5.14b and does not fit well the simulation result in Figure 5.13b, because of the inevitable loss due to the RF connector. This comment is verified by measuring a RF through connector with calibrated port.



(a) (b)

Figure 5.14. Measurement results of microstrip line with FR4 substrate. (a) Return loss (b) Insertion loss.

In RF IC's, sometimes the port impedances can sometimes be adjusted to be different from the 50 Ω standard. Therefore, transformer circuits are used to match the port with different impedances as shown in Figure 5.15. In microstrip theory, this is achieved by connecting these two ports with a transformer which may have several types of shapes [23]. The basic idea of the transformer shape is to reduce the discontinuity by applying large number of steps in different widths, with intermediate line with a linearly varying width or by directly connecting the two ports.

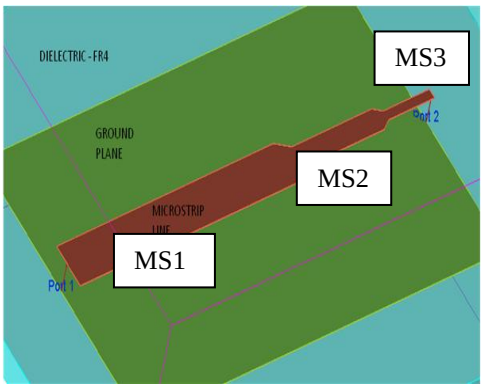


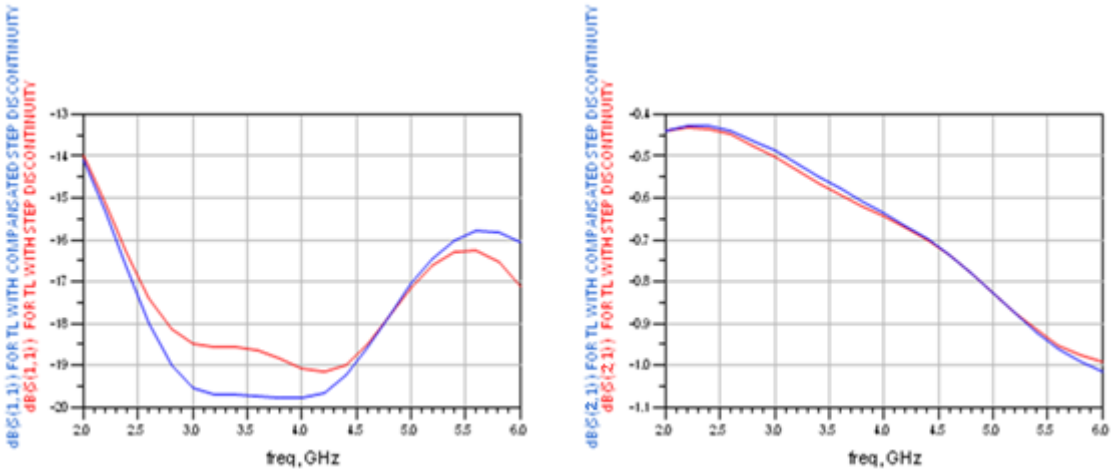
Figure 5.15. Microstrip line with transformer.

The calculated dimensions for the structure in Figure 5.15, are given in Table 5.5.

Table 5.5. Microstrip line dimensions for the sections of the transformer.

	Length	**Width**
MS1	20.6 mm	2.82 mm
MS2	8.27 mm	1.47 (λ / 4) mm
MS3	4.63 mm	0.63 mm

The simulation results in Figure 5.16 show that the return loss covers the entire UWB band and the insertion loss is about 0.65 dB which complies with the previous microstrip sample.



(a) (b)

Figure 5.16. Simulation results of microstrip transformer circuit.

Additionally, Figure 5.16 also illustrates an another design issue such that the blue line in Figure 5.16a is obtained by tapering the discontinuities at the joints of the lines. By doing this, the return loss improves by about 1 dB and the insertion loss is slightly less than the untapered one.

PCB design becomes challenging as the operating frequency increases and the traces on the PCB should be designed by considering the connectors, IC pins and discrete components especially for RF IC's. RF connectors are selected as laterally mounted for the EM wave to travel without any turn. Intuitively, when the receiver has a differential input, it is inevitable that the wiring from IC to the connector or another discrete component

should be in ground-signal-ground (GSG) or multiple combinations of GSG (GSGSG etc.) form. Hence, CPWG takes significant role in RF PCB design. CPWG structures were designed by considering of the basic necessities for the RF PCBs such as connecting the thin IC leads.

The simulation result in Figure 5.17 shows the behavior of a CPWG with characteristic impedance of 50 Ω. The width of the trace is 1 mm and the gap between the trace and the component-side ground plane is 0.197 mm.

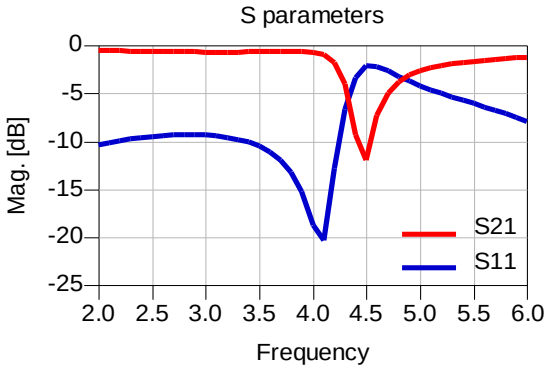


Figure 5.17. The simulation result of a designed CPWG type transmission line.

The S_{11} (return loss) is sufficient for the band from 3 GHz to 4.3 GHz and the insertion loss less than 1 dB up to 4.3 GHz.

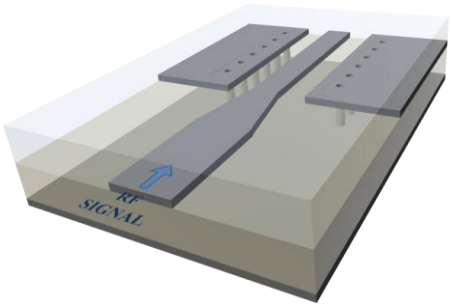
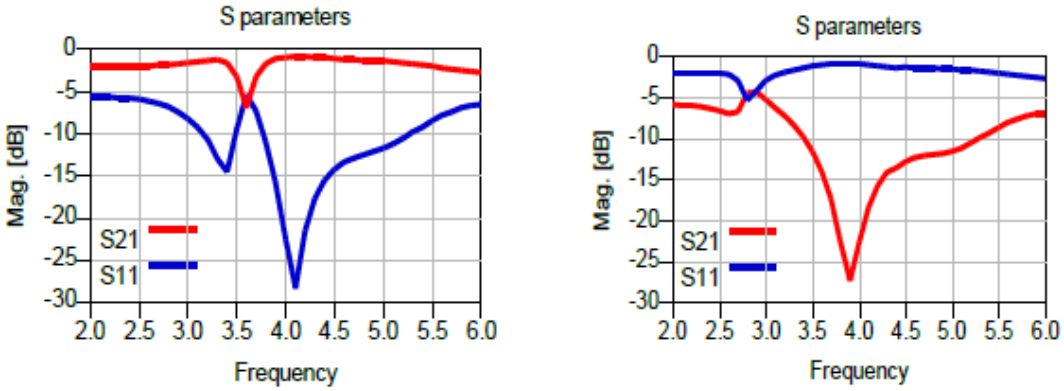


Figure 5.18. The illustration of a designed CPWG to microstrip transformer.

The other structure in CPWG form is the CPWG to microstrip transformer shown in Figure 5.18. This one is used to reduce the inductive effects resulting from the thin signal trace of CPWG. Therefore, apart from the microstrip counterpart, the component side ground planes should be shaped for the transition to be smooth.

The simulation results for the transformer is given in Figure 5.19. The abrupt transition between the two different types of transmission lines does not allow to have a wideband response. However with help of the smooth transition the return loss is acceptable from 3.5 GHz to 5.3 GHz.



(a) (b)

Figure 5.19 S_{11} and S_{21} for CPWG to microstrip transformer. (a) abrupt transition (b) smooth transition.

5.4 Measurement Results of Designed PCB

In Figure 5.20, the designed RF PCB with FR4 substrate is presented. The CPWG type transmission lines which are labelled as TX_data, TX_CLK, RX_OUT, can be seen clearly. The traces labelled as TX are the input ports of the transmitter and the RX is to indicate the receiver.

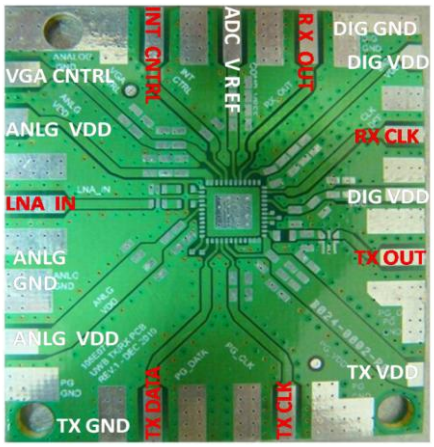


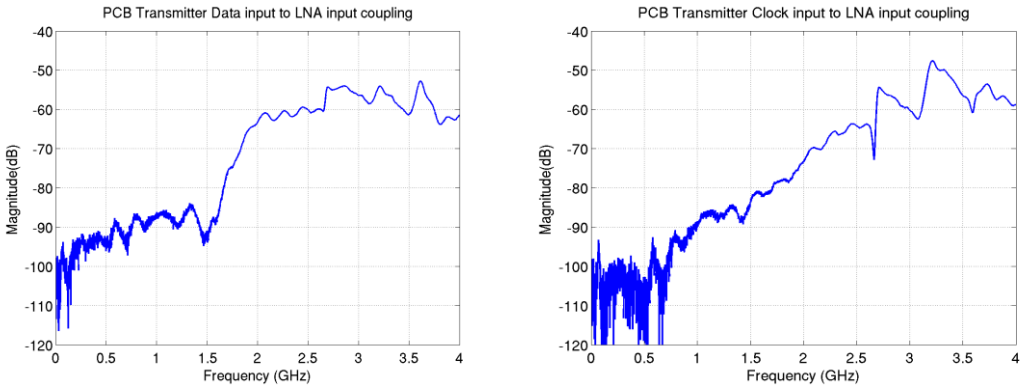
Figure 5.20. The overall view of the designed RF PCB.

The RF PCB is designed by considering the pin diagram of the IC. In order to send away the traces which are close to each other, the thin traces are transformed to thicker one. Thicker traces are needed to reduce the inductive effect of the trace.

The vias connecting the ground plane with component-side ground plane are placed in paralel to the trace with a distance which the manufacturing process allows. The space between the consecutive vias is determined by the wavelength and hence is a function of the signal frequency.

Additionally, the ground plane is divided into three sections as digital ground (for digital blocks), analog ground (for analog blocks) and baseband ground (for baseband blocks) in order to reduce the coupling effects such as switching noise.

The measurement results of the designed RF PCB cover the coupling between the traces and the trace losses. Because coupling causes a distortion on the data signal and reduces the possibility of detection.

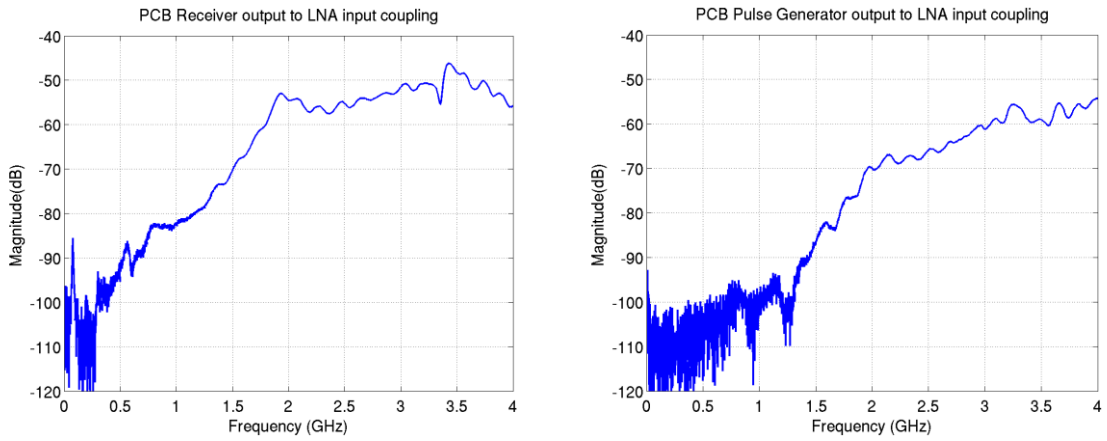


(a) (b)

Figure 5.21. (a) Coupling between TX DATA and LNA IN. (b) Coupling between TX CLK and LNA IN.

The greatest concern during the operation of the IC is coupling between the switching noise resulting from the clock signal and the LNA input. Because the signal received by the antenna is in a single-ended on PCB, coupling can not be tolerated. Figure 5.21a and 5.21b show the coupling between the LNA input and the applied data and clock

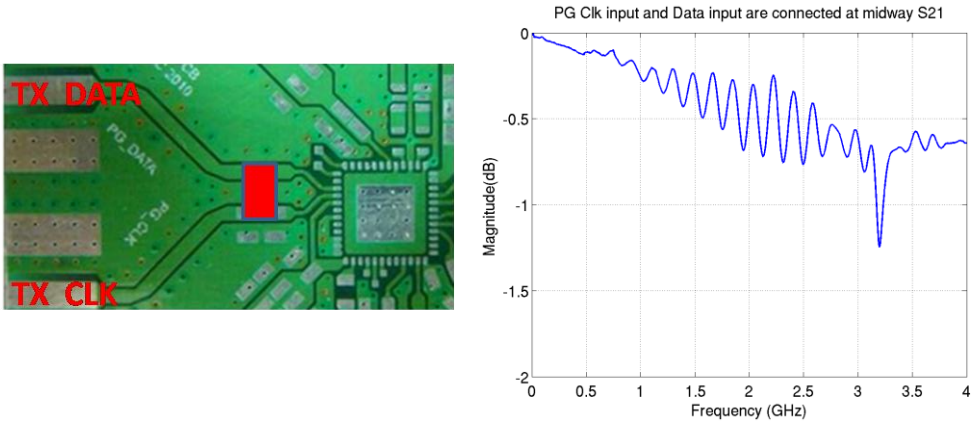
signals, respectively. The coupling is considered up to 1 GHz because of the applied clock frequency and measured to be about -90 dB which is almost negligible.



(a) (b)

Figure 5.22. (a) Coupling between RX OUT and LNA IN. (b) Coupling between TX OUT and LNA IN.

The second issue is the coupling between are the output of the pulse generator which is a block used to generate the UWB pulse, and receiver output. Especially, the receiver output corresponds to the demodulated signal and therefore its causes switching noise. However, Figure 5.22a shows that the coupling is about -80 dB and similarly a better result can be observed from Figure 5.22b.



(a) (b)

Figure 5.23. (a) Test setup of the connected traces with 50 Ω . (b) Total insertion loss of the connected traces.

The measurement result in Figure 5.23b shows the insertion loss of the traces connected to each other with 50 Ω resistor (Figure 5.23a). The total loss measured is less than 1 dB.

6. UWB PATCH ANTENNA DESIGN

6.1 Basics of UWB Antennas

There is a high demand for UWB technology in many communication systems. These systems include radar systems, and communication and imaging systems which have several subsystems. However, the antenna is the common component for all of these communication systems. Furthermore, the antenna is one of the important components in any wireless communication system because it allows the interaction of the electronic device with the outside world. All antennas regardless of whether they are UWB or traditional, are characterized by features such as: operational frequency bandwidth, radiation pattern, efficiency, directivity, gain, polarization, etc.

The design of a UWB antenna, in particular, is more challenging with respect to the other types of antennas because these antennas should work on the entire frequency band of their operation. The pertaining theory has limitations, thus making agreement between the theory and measurements is quite difficult as opposed to other antennas where theoretical results fit measurement much better.

UWB antennas are commonly designed within the frequency range of 3-10 GHz. In this work, the band of operation covers the range 3.1 GHz - 4.7 GHz, hence the first consideration about the UWB antenna is to satisfy the bandwidth entirely.

6.2 Analysis on UWB Patch Antennas

The most common type of a UWB antenna is the patch antenna patterned on PCB. The reason is that the wideband characteristic is more easily maintained with the patch antenna. In addition, they can be easily fabricated with relatively low cost. From this point of view the design process of a UWB antenna is carried out by literature survey, at first glance. From [27], the proposed antenna is selected, fabricated and measured to observe

whether it satisfies the proposed specifications or not. This antenna is referred to as the reference antenna for the rest of the thesis.



Figure 6.1. The fabricated reference antenna.

To achieve an ultrawideband operation for this antenna, first a trapezoid shaped feed line is used in microstrip line form with ground plane on the back side for the purpose of having better impedance matching. Then, the feed line and the main patch is put together with tapered intermediate connection which provides wider impedance bandwidth [27].

The second analysis is on a commercial antenna named In4Tel patented Wisair antenna as shown in Figure 6.2. This antenna has an additional property of including a microstrip bandpass filter different from the others in this thesis as a solution for covering the band [28]. This compact design combining the filter with the radiating patch, shows a considerable performance improvement in terms of band rejection. Furthermore, the substrate on which the the patch is patterned is a special material providing low loss and high efficiency.



Figure 6.2. The commercial antenna.

As a conclusion, the UWB antenna is designed (referred as 1st antenna) in the light of simulation results and the antenna proposed in [29]. The sections of the designed antenna are given in Figure 6.3. The feed line has a length of 4 cm which equals to the wavelength of the received RF signal at 4 GHz. A longer feed line corresponds a higher loss and more attenuation on the signal transmitted or received. In this context, the feed line may be kept short to reduce the attenuation.

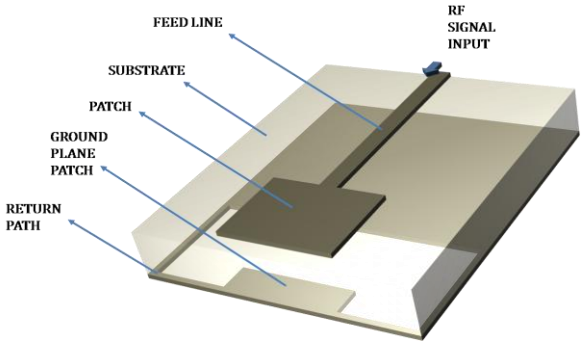


Figure 6.3. Sections of the designed UWB antenna.

The dimensions of the patch, ground plane patch, the distance from the ground plane to the bottom edge of the radiating patch are initially taken from [29]. Then, the optimization process starts by adjusting the position of the feed line in horizontal axis. The ground plane patch is relocated to have the desired response. The return path covering the patch from the back side, connects the ground plane patch to the ground. After a few improvements the S_{11} response turns out to be as shown in Figure 6.4.

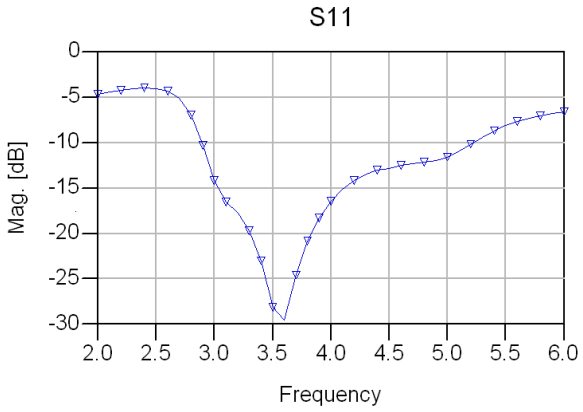


Figure 6.4. Preliminary S_{11} result of the designed UWB antenna.

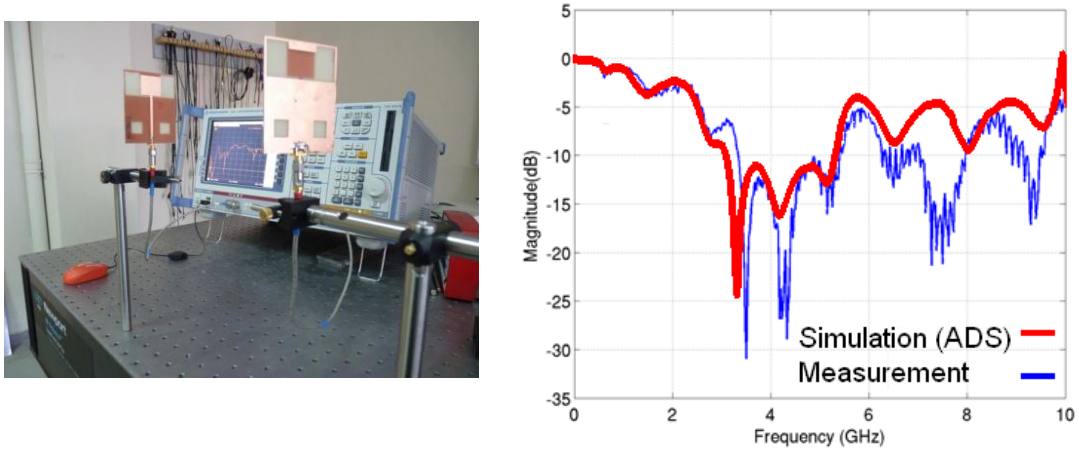
This result shows that the route following the optimization is reasonable. After a certain number of iterations, the ultimate version of the antenna is formed Figure 6.5 shows the picture of the UWB antenna from both sides.



(a) (b)

Figure 6.5. View of designed UWB antenna. (a) top view (b) bottom view.

The measurements are performed using a network analyzer with the established test setup which can be seen in Figure 6.6a. The simulation and the measurement results of the ultimate version of the antenna as given in Figure 6.6b, perfectly complies with the each other and satisfies the UWB bandwidth targeted in this thesis.



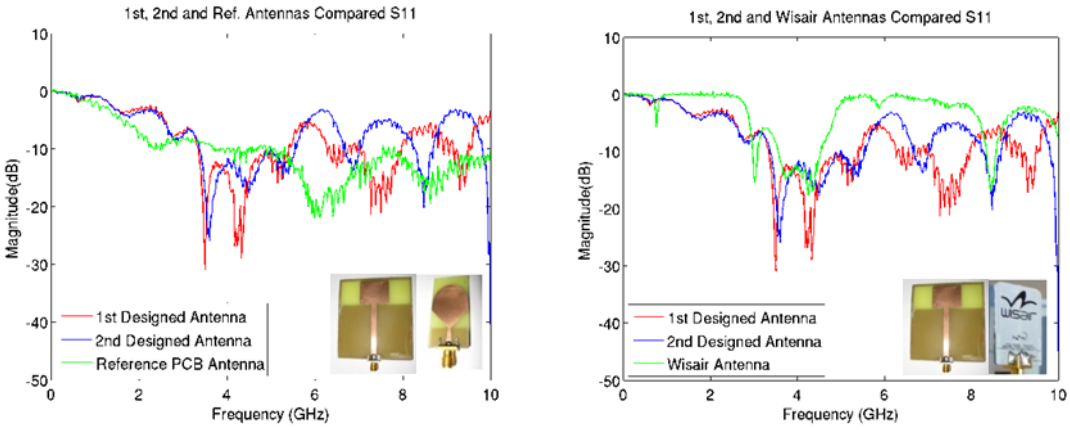
(a) (b)

Figure 6.6. (a) Test setup for antenna measurement (b) Simulation and measurement results of the UWB antenna.

It was also noted that the ground plane shape can effect the overall performance [30]. Hence, in order to observe the behaviour of the antenna when the ground plane is patterned, an additional antenna (referred as 2nd antenna in the plot) is designed. The substrate thickness is half of the 1st antenna. Finally, the performance of these antennas were measured from various distances.

In the next step, the comparison between the designed antennas, reference antenna and the commercial antenna (referred as Wisair antenna in the plots) is performed by measuring each antenna individually and plotting of them on the same axes.

The comparison between the designed antennas and reference antenna is given in Figure 6.7a and similarly designed antennas are compared with the commercial antenna in Figure 6.7b.



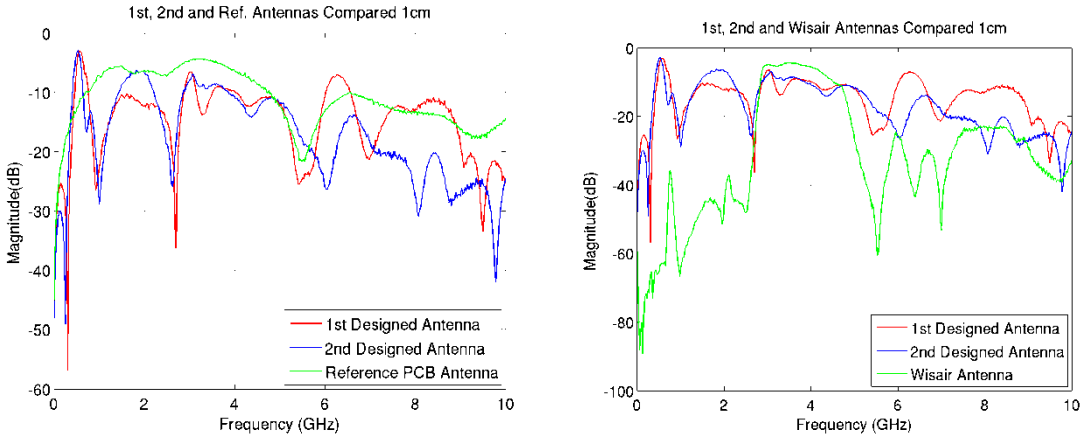
(a) (b)

Figure 6.7. S_{11} comparisons (a) designed antennas vs. reference antenna (b) designed antennas vs. commercial antenna.

From Figure 6.7a, the designed antennas are superior to the reference antenna but not as good as the commercial one, because the bandpass characteristic is clearly observed as a result of the additional microstrip filter as mentioned above.

As a conclusion, the performance of the antennas are measured from various distances. When antennas are close to each other approximately by 1 cm, from Figure 6.8a,

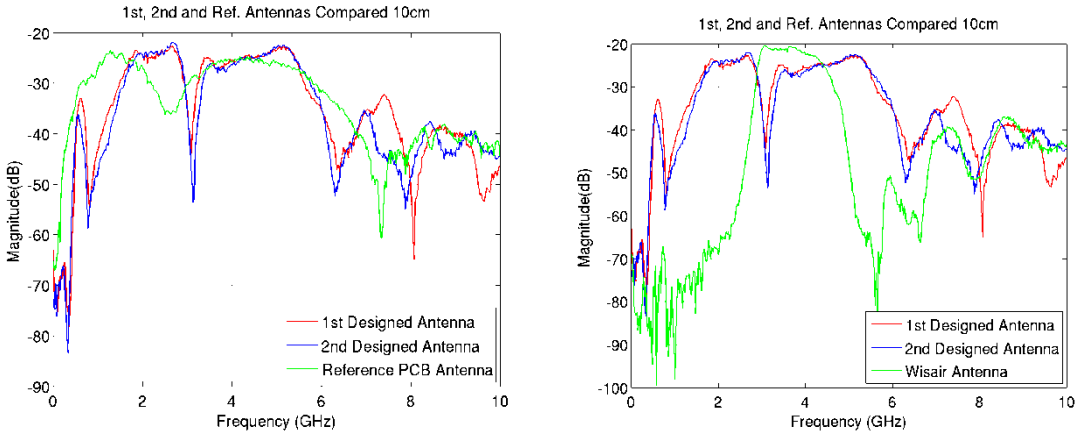
the reference antenna seems to work with less loss but there is no bandpass response. The commercial antenna performs much better during the in-band operation. Nevertheless the designed antennas have the intended bandpass characteristics as observed in Figure 6.8b.



(a) (b)

Figure 6.8. S_{21} comparisons for 1cm distance. (a) designed antennas vs. reference antenna (b) designed antennas vs. commercial antenna.

From a longer distance around 10 cm, the behaviours of all antennas are measured. In the light of the results presented in Figure 6.9, similar interpretations can be performed. The loss of the designed antennas reduces to -25 dB roughly only 5 dB less than the commercial antennas.



(a) (b)

Figure 6.9. S_{21} comparisons for 10 cm distance. (a) designed antennas vs. reference antenna (b) designed antennas vs. commercial antenna.

7. CONCLUSION

In this thesis, some of the basic blocks of a non-coherent IR-UWB receiver are designed by considering the specifications determined according to the overall performance of the receiver.

The first analog block in the receiver is LNA; therefore, the overall system performance strongly depends on this block. Two different LNA topologies were selected for analysis and three different versions were designed. The topology investigated in most detail, is referred to as LNA_2.

According to the predetermined detection range, circuits of both LNAs are modified to comply with design goals which are low noise figure, minimum reflection on the received signal due to the port mismatches, and a considerable amount of gain which can be externally adjusted for the testing purposes. LNA_1 stands out with its relatively low noise figure with respect to LNA_2. However, it has relatively less gain and poor reflection while consuming a DC power of 11 mW.

LNA_2 is designed by considering the 3.1 GHz to 4.7 GHz UWB bandwidth. However, the deficiencies on the following block (VGA) should be eliminated by the adapted LNA_2. Therefore, the third LNA (adapted LNA_2) is designed in the same manner.

According to the s-parameter results of adapted LNA_2, the reflection on the signal is tolerable. The noise figure also shows the noise contribution of the amplifier in the band of interest which allows to detect the data up to 250 Mbps. The total DC power dissipation of the LNA_2 is 13.69 mW.

The integrator which forms the energy detection part of the receiver with mixer, can integrate the squared signal while amplifying it to an applicable voltage level. The dc power dissipation of the integrator is 1.58 mW. The comparator shows a hysteresis behaviour and consumes about 3.1 mW while the pmos preamplifier consumes 2.7 mW.

The remaining part of the thesis consists of the necessary items for the test set-up which are RF PCB board and antenna. RF PCB board is designed by considering the losses due to the mismatches. The RF standard of 50 Ω, is taken into account while calculating the trace dimensions. Besides, some of the commonly used microstrip structures are analyzed.

For the purpose of receiving the transmitted signal, a UWB antenna is designed. According to the comparison results between designed, reference and commercial antennas, the designed antenna helps the receiver to operate up to 10 cm.

After the design phase, layouts of the analog blocks that form the UWB receiver were drawn one by one in Mentor Graphics by using the layout tool. All blocks are simulated to see whether the circuits are still working with the extracted parasitic. As a conclusion, all layouts are put together and the IR-UWB IC is sent to be manufactured.

APPENDIX A: LAYOUT VIEWS OF THE DESIGNED BLOCKS

All the layouts of the designed analog blocks are drawn in Mentor Graphics layout tool and the following figures show the overall view of the each block. The overall receiver layout is shown in Figure A.5.

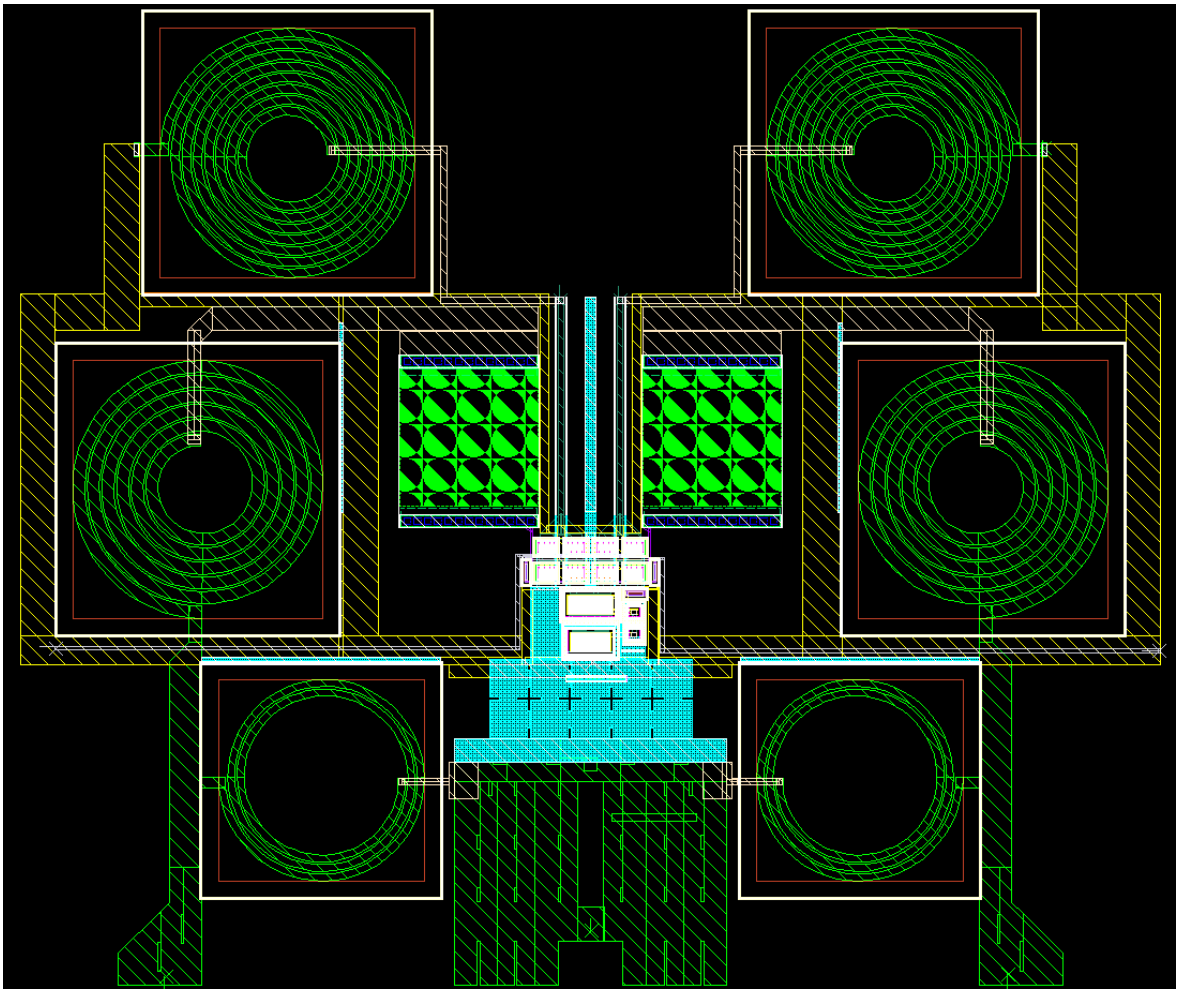


Figure A.1. Low noise amplifier without source inductive degeneration.

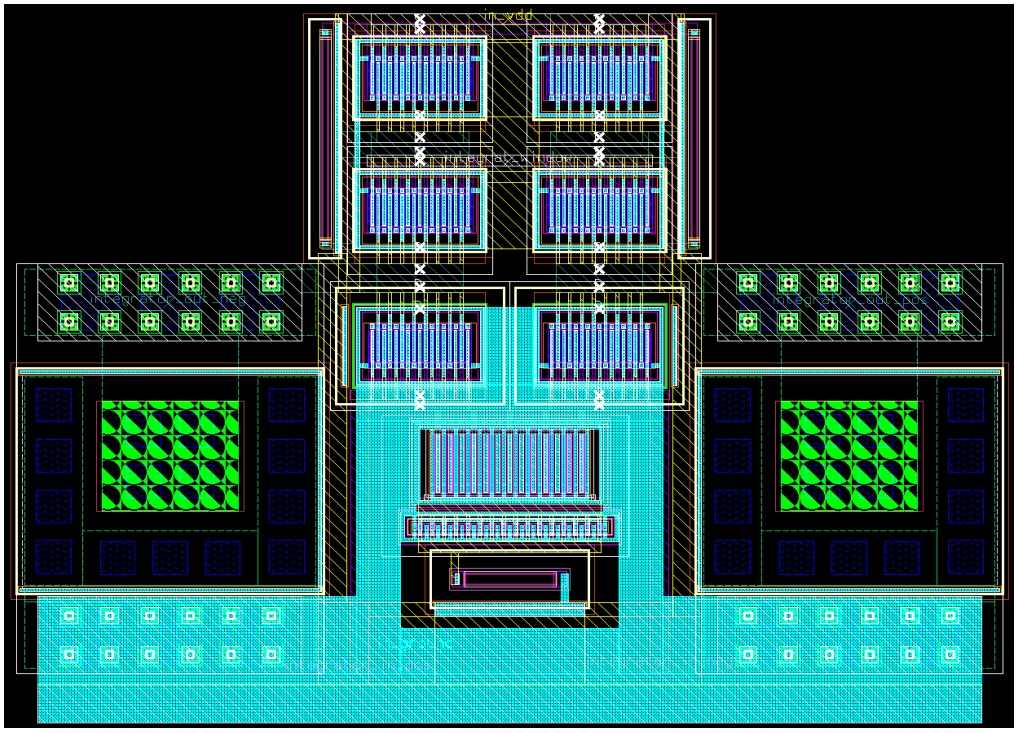


Figure A.2. G_m-C Integrator.

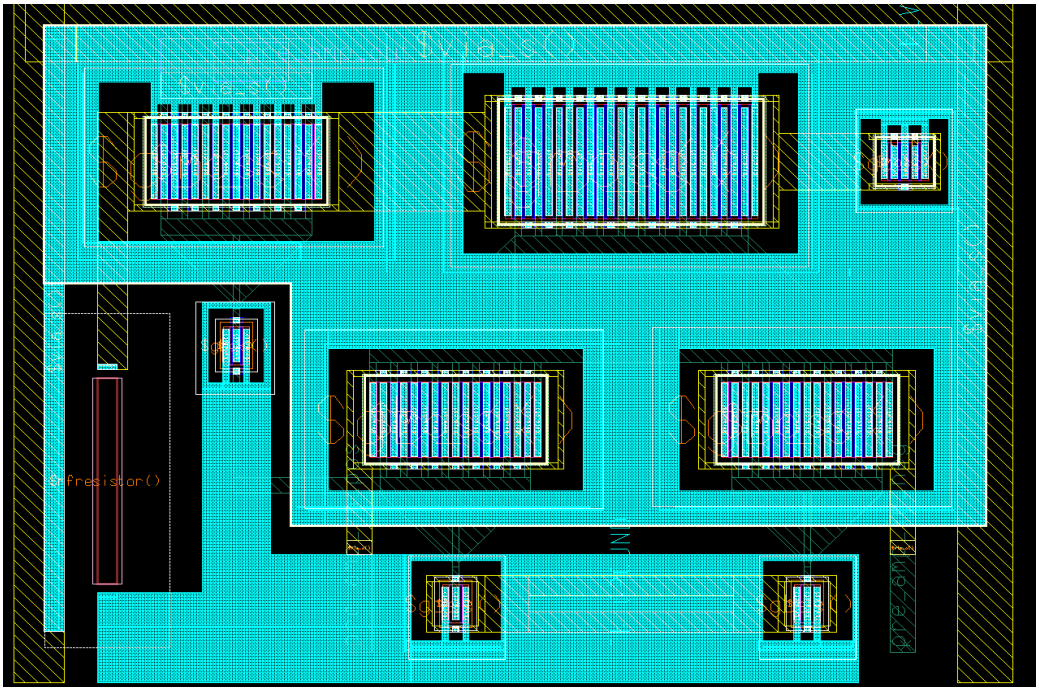


Figure A.3. Pmos input Preamplifier.

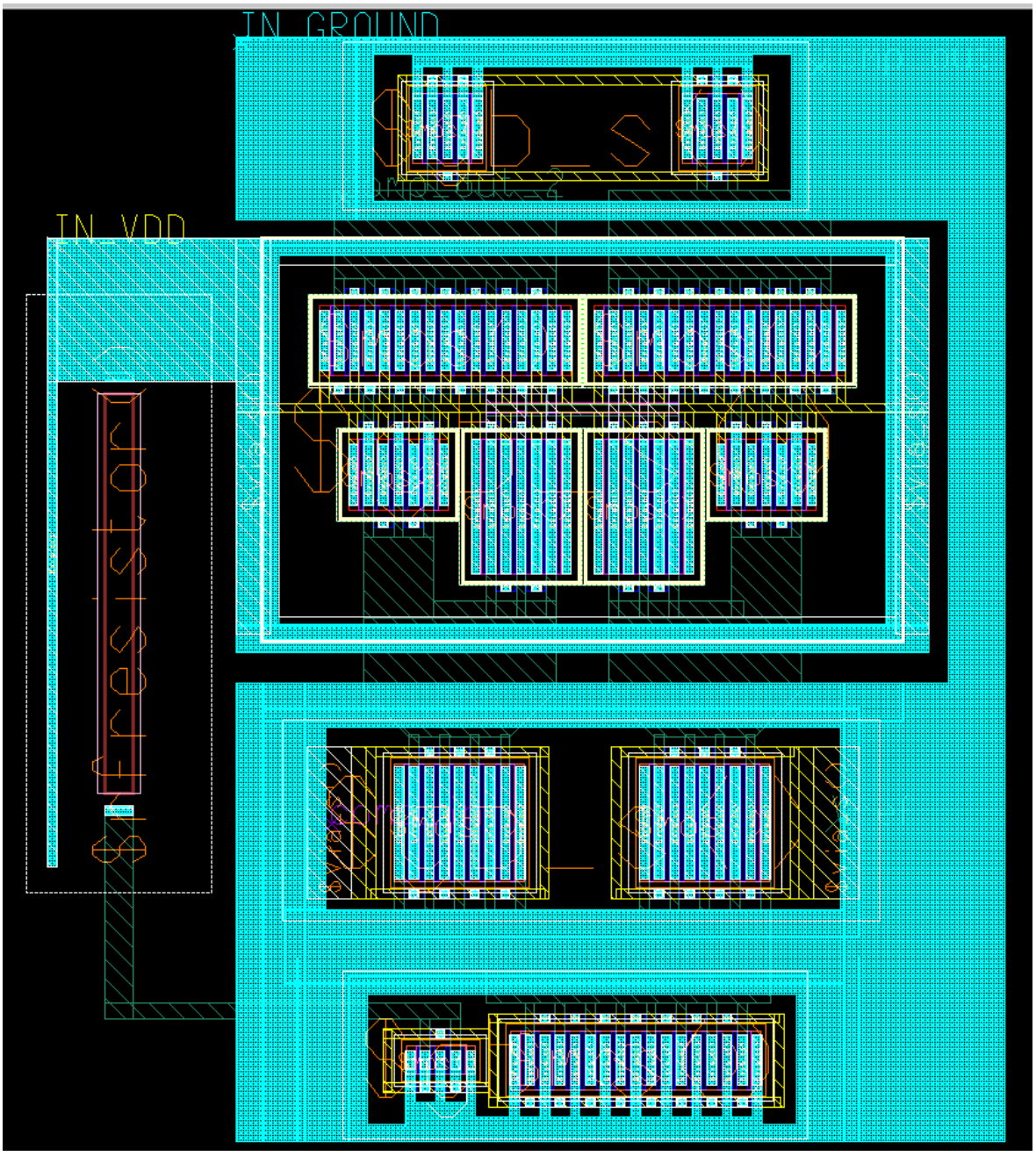


Figure A.4. Comparator with Hysteresis.

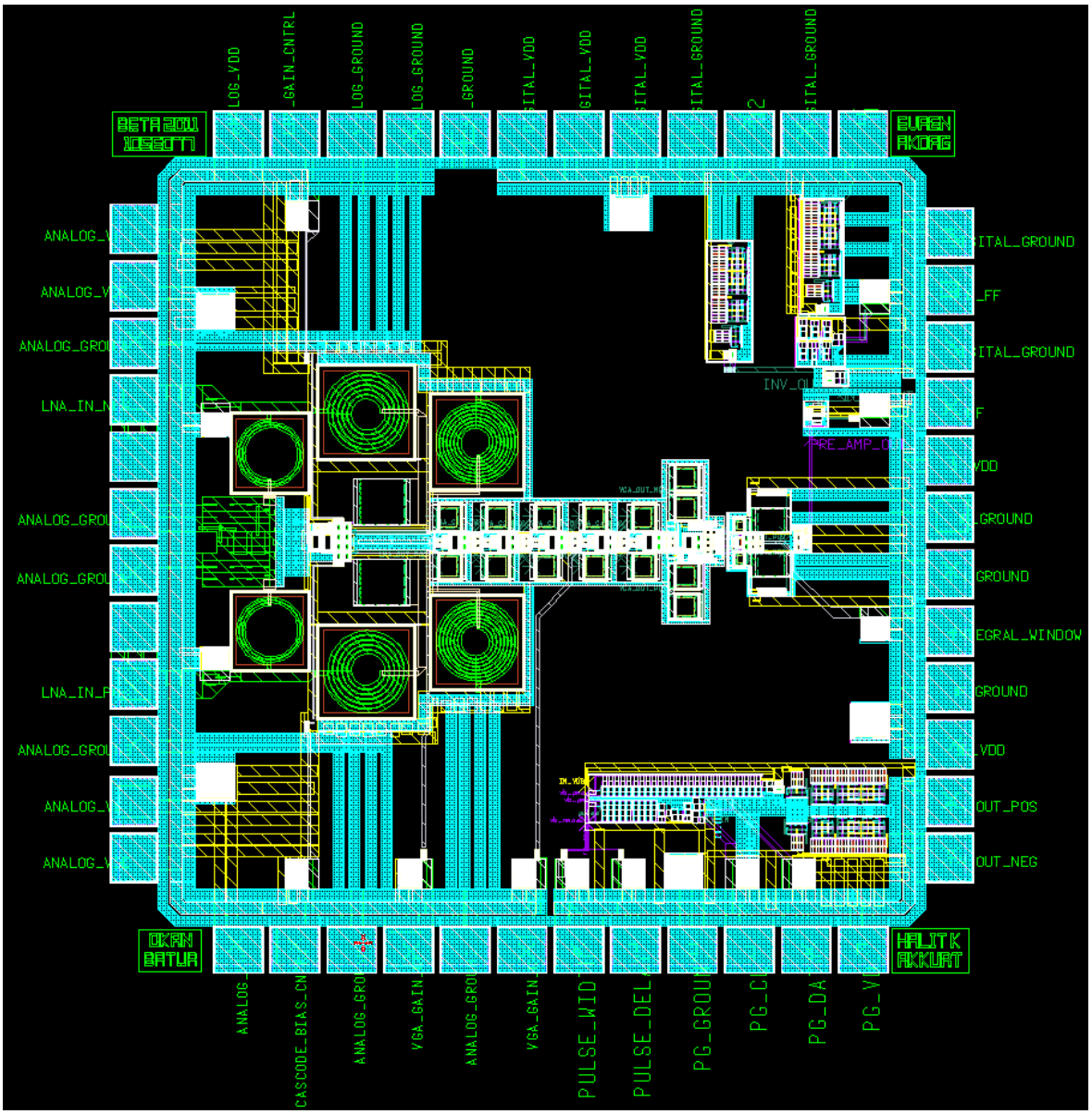


Figure A.5. Overall view of the receiver layout and the placement of the pins.

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