ANALOG DESIGN & OPTIMIZATION OF PWL CIRCUITS USED IN FUZZY LOGIC SOLUTIONS

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ABSTRACT

ANALOG DESIGN & OPTIMIZATION OF PWL CIRCUITS USED IN FUZZY LOGIC SOLUTIONS

Neural networks are widely used in all branches of life such as system identification, decision support and control where systems are designed to be working as human brain and make decisions like the way human beings do. Although neural networks describe much more precise solution surface, fuzzy logic is becoming more popular since complexity, trainability and especially hardware implementation of fuzzy logic is much easier. This work is concerned with the construction of fuzzy logic piecewise linear functions (PWL) that are used for solution surface approximation.

Various combinations of CMOS current mirror circuits are used to realize PWL functions. There are several sources of errors in design of such functions. In order to simplify the optimization of these error calculations, PWL circuits are divided into smaller circuits which are assumed to be current mirrors in this work. Implementation error which is caused by deviation from the real solution surface and mismatch errors between current mirror transistors due to difference between threshold voltages (V_t), oxide capacitance (C_{ox}), width and length of transistor values are considered as the main sources of errors.

This work represents a computer aided tool for calculation of optimized W and L values of current mirror transistors for various values of reference current within a specified error to find the best transistor parameters for possible minimum power dissipation. Results are tested on several applications to verify that the results of the computer aided system presented in this work are matching with the simulation results. It has been seen that instead of designing and calculating PWL circuits manually, introduced optimization tool may well be used in such processes.

ÖZET

BULANIK MANTIK ÇÖZÜMLERİNDE KULLANILAN PARÇALI DOĞRUSAL DEVRELERİN ANALOG TASARIMI VE İYİLEŞTİRİLMESİ

Yapay Sinir Ağ Devreleri, sistem tanımlama, karar verme ve kontrol sistemleri gibi günlük hayatın birçok dalında, insan beyni gibi düşünebilmek ve karar veremebilmek için tasarlanmıştır. Yapay Sinir Ağ Devreleri, her ne kadar daha kesin sonuçlar verse de kıyasla kesinlik oranı daha az olan bulanık mantık devreleri, donanım tasarımlarının kolaylığı, karmaşıklıklarının daha az olması ve eğitilebilirliklerinden dolayı günümüzde daha çok tercih edilmektedirler. Bu çalışma, bulanık mantık devrelerinde çözüm yüzeyinin tahminlenmesinde kullanılan parçalı doğrusal işlemlerinin gerçeklenmesiyle ilgilenmektedir.

Parçalı Doğrusal (PWL) devreleri gerçelleyebilmek için CMOS akım aynaları kullanılmaktadır. Bu devrelerin tasarımında bir takım hata kaynakları bulunmaktadır. Hata iyileştirmesini kolaylaştırmak için PWL devreleri yapı taşları olan akım aynası devrelerine bölünmüştür. Çözüm yüzeyine yakınsama maksadıyla kullanılan algoritmadan ve akım aynası devrelerindeki eşik potansiyeli (V_t), oksit sığası (C_{ox}), tranzistörlerin boy ve en farklılıklarından kaynaklanan hatalar bu çalışmada ana hata kaynakları olarak değerlendirilecek ve hata hesaplamaları bu değerler üzerinden yapılacaktır.

Bu çalışma, belirlenmiş bir güç harcanımı ve hata aralığında çalışacak akım aynası tasarımı ve iyileştirilmesi üzerinedir. Çözüm farklı uygulamalar üzerinde değerlendirilmiş, sonuçlar, benzetim değerleriyle karşılaştırılarak sistemin uygunluğu test edilmiştir. Akım aynası tasarımında elle yapılacak olan işlemler yerine bu çalışmada tanımlanmış olan sistemin kullanılmasının yeterli olacağı sonucuna varılmıştır.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii
ABSTRACT iv
ÖZET v
LIST OF FIGURES viii
LIST OF TABLES xii
LIST OF SYMBOLS / ABBREVATIONS xiii
1. INTRODUCTION 1
2. BACKGROUND OF THE PROBLEM AND DESIGN METHODOLOGY 5
2.1. Background of the Problem 5
2.2. Design Tool for Optimization of Analog Fuzzy Implementation 7
2.2.1. Methodology Used for Design Tool 7
3. DEFINITION OF TRANSISTOR CURRENT 11
3.1. Parameter Calculations 11
3.2. Short Channel Effect 17
4. SOFTWARE 19
4.1. W & L Calculation Algorithm 19
4.2. Linear Approximation Algorithm 22
4.3. Circuit Creation Algorithm 25
5. ANALOG CURRENT MIRROR COMBINATION BLOCKS 27
5.1. Simple NMOS Current Mirror Circuit 27
5.4. Simple PMOS Current Mirror Circuit 29
5.5. NMOS Current Mirror Breakpoint Circuit 31
5.6. PMOS Current Mirror Breakpoint Circuit 32
5.7. NMOS – PMOS Combination of Current Mirrors 34
5.8. PMOS – NMOS Combination of Current Mirrors 36
5.9. Double Break Point Circuit with NMOS Transistors 37
5.10. Double Break Point Circuit with PMOS Transistors 39
5.11. Improved Circuit that Uses Two NMOS Current Mirrors 40
5.12. Improved Circuit That Uses Two PMOS Current Mirrors 42

6. APPLICATION 44
6.2. Sample Two Dimensional Circuit 47
6.3. Fuzzy Logic Applications 52
6.3.1. One Dimensional Fuzzy Solution Surface Realization 53
7. CONCLUSIONS 59
REFERENCES 61

LIST OF FIGURES

Figure 3.1. NMOS current mirror circuit 13

Figure 3.2. Simple Transistor Circuit ($W = L = 1$ μm). 18

Figure 3.3. Short channel effect ($W = L = 1$ μm, $V_{GS} = 0.7, 0.8, 0.9, 1.0$, $V_{DS} = 0\text{-}3$). 18

Figure 4.1. Block diagram of whole design 19

Figure 4.2. Block diagram of *W* & *L* Calculation algorithm 20

Figure 4.3. *W* & *L* Calculation input file 20

Figure 4.4. *W* & *L* Calculation algorithm flowchart 21

Figure 4.5. Block diagram of Linear Approximation algorithm 22

Figure 4.6. Input file of the Linear Approximation algorithm 23

Figure 4.7. Linear Approximation output for two dimensional surface approximation 23

Figure 4.8. Normalization of breakpoints for one dimentional case 23

Figure 4.9. Linear Approximation algorithm flowchart 24

Figure 4.10. Block diagram of Circuit Ceation algorithm 25

Figure 4.11. Circuit Creation algorithm flowchart 26

Figure 5.1. Simple NMOS current mirror circuit 28

Figure 5.2. H-Spice simulation of simple NMOS current mirror 29

Figure 5.3. Simple PMOS Current Mirror 30

Figure 5.4. H-Spice simulation of simple NMOS current mirror 31

Figure 5.5. NMOS current mirror circuit 32

Figure 5.6. H-Spice simulation of NMOS current mirror with a single breakpoint 32

Figure 5.7. PMOS current mirror circuit 33

Figure 5.8. H-Spice simulation of PMOS current mirror with a single breakpoint 34

Figure 5.9. NMOS – PMOS combination of current mirrors 35

Figure 5.10. Simulation of NMOS-PMOS combinational single breakpoint circuit 35

Figure 5.11. PMOS – NMOS combination of current mirrors 36

Figure 5.12. Simulation of PMOS-NMOS combinational single breakpoint circuit 37

Figure 5.13. Double break point circuit with NMOS transistors 38

Figure 5.14. H-Spice simulation of double breakpoint NMOS combinational circuit 38

Figure 5.15. Double breakpoint circuit with PMOS transistors 39

Figure 5.16. H-Spice simulation of the double breakpoint PMOS combinational circuit..40

Figure 5.17. Improved circuit that uses two NMOS current mirrors.....41

Figure 5.18. Simulation of the improved double breakpoint NMOS circuit 41

Figure 5.19. Improved circuit that uses two PMOS current mirrors 42

Figure 5.20. Simulation of the improved double breakpoint PMOS circuit.....43

Figure 6.1. Expected solution surface.....44

Figure 6.2. Breakpoints of sample figure 44

Figure 6.3. Output of the Circuit Creation algorithm, sample circuit H-Spice file 45

Figure 6.4. Circuit schematic of the sample circuit…….. 46

Figure 6.5. H-Spice simulation of the created circuit…….... 47

Figure 6.6. H-Spice simulation of the created circuit at 0.5 MHz.....47

Figure 6.7. Breakpoints of the two dimensional sample circuit 48

Figure 6.8. H-Spice file ouput of the design.....48

Figure 6.9. Sample two dimensional circuit output for 1μA ≤ y ≤8μA.....50

Figure 6.10. Sample two dimensional circuit output for 1μA ≤ y ≤8μA at 50MHz.....50

Figure 6.11. Sample two dimensional circuit output for 8μA ≤ y ≤ 15μA.....50

Figure 6.12. Sample two dimensional circuit output for 8μA ≤ y ≤ 15μA at 50MHz.....51

Figure 6.13. Sample two dimensional circuit two dimensional output graph-1 51

Figure 6.14. Sample two dimensional circuit two dimensional output graph-2 52

Figure 6.15. Fuzzy Solution Surface 53

Figure 6.16. Reconstructed two dimensional fuzzy solution surface 54

Figure 6.17. Normalized reconstructed two dimensional fuzzy solution surface 54

Figure 6.18. H-Spice file of the sample bias circuit 55

Figure 6.19. Bias circuit schematic for two dimensional fuzzy surface function 56

Figure 6.20. H-Spice output of the sample bias circuit 56

Figure 6.21. Surface drawn by the first input breakpoints 57

Figure 6.22. Surface drawn by the second input breakpoints 57

Figure 6.23. Fuzzy solution created by the Circuit Creation algorithm 58

LIST OF TABLES

Table 5.1. Simple NMOS current mirror comparison 28

Table 5.2. Simple PMOS current mirror comparison 30

Table 5.3. NMOS current mirror circuit comparison 31

Table 5.4. PMOS current mirror circuit comparison 33

Table 5.5. NMOS – PMOS combination of current mirrors comparison 35

Table 5.6. PMOS – NMOS combination of current mirrors 37

Table 5.7. Double break point circuit with NMOS transistors comparison 38

Table 5.8. Double break point circuit with PMOS transistors comparison 39

Table 5.9. Improved circuit that uses two NMOS current mirrors comparison 41

Table 5.10. Circuit that uses two PMOS current mirrors comparison 43

Table 6.1. Breakpoints comparison of approximated and expected surface 46

LIST OF SYMBOLS / ABBREVATIONS

C_{OX}	Gate oxide capacitance per unit area
I_{BIAS}	Bias current of the analog block
I_C	Inversion coefficient
I_D	DC current of the analog block
I_F	Forward normalized current
I_R	Reversed normalized current
I_S	Normalized current
L	MOSFET channel length
N	Linearized body effect
Q	Mobile charge per unit area
t_{OX}	Gate oxide thickness of MOSFET channel
U_t	Thermodynamic voltage
V_{ch}	Channel voltage of transistor
V_D	Drain voltage of the transistor
V_G	Gate voltage of the transistor
V_{out}	Output voltage
V_p	Pinch off potential of the transistor
V_S	Source voltage of the transistor
V_{supply}	Supply voltage
V_{TO}, V_T	Threshold voltage of the transistor
W	MOSFET channel width
α	Aspect ratio
ε_{SI}	Permittivity of silicon
μ	Mobility of electrons or holes in the channel
ASIC	Application specific integrated circuit
CAD	Computer aided design
CMOS	Complementary metal oxide field effect transistor
E_{imp}	Implementation error

EKV	Enz, Krummenacher, Vitoz MOS transistor model
Est.	Estimation
MOS	MOSFET transistor
NMOS	N channel MOSFET transistor
P	Total error performance
PMOS	P channel MOSFET transistor
PWL	Piecewise linear
S	Fuzzy surface
Sim.	Simulation

1. INTRODUCTION

In daily life, some problems can not be solved by modeling them mathematically. In fact, the real world itself can not be modeled precisely. Consequently, there is a need for finding a solution to such problems which has not got any specific answer. For example, a problem may have several solutions; however, the effect of each solution on the problem may be different. This need leads to the usage of Neural Networks and Fuzzy Logic systems which help to come out with certain solutions from these problems like human brain does. Neural Network and Fuzzy Logic circuits can be designed as analog or digital. Each has its own advantages and disadvantages. Since the world is an analog environment the usage of digital circuits needs analog to digital and digital to analog conversion. Therefore, usage of analog circuits is more advantageous from this point of view. In addition, analog nonlinear signal processing is known to be faster than digital signal processing, however, the lack of accuracy is the main disadvantage of analog circuits. Therefore, analog circuits are advised to be used in processes where speed is more important than accuracy.

Electronics is becoming a more and more important issue since the beginning of the 21st century. During this century IC technology enroll a big development, now it is in every piece of life to make things simpler. In analog circuit design the most popular technology is the CMOS (Complementary Metal Oxide Semiconductor) technology, since they present low cost high performance circuits. Based on this technology with low cost and high performance they supply, it is important to implement neural networks and fuzzy logic on CMOS design circuits which will lead to low voltage, low current circuits and application specific integrated circuits. However, design of analog circuits is more complex than the other design methods such as digital design. Analog design requires creativity and expert man power since the dependency to environment is very high which makes modeling analog functions is very hard. These handicaps make the analog design harder to develop. Benefits of analog design is improved speed and low power dissipation.

When compared to fuzzy logic, neural networks, presents more precise solution surfaces. Although neural networks describe much more precise surface, fuzzy logic is becoming more popular since complexity, trainability and especially hardware implementation of fuzzy logic is much easier. This work is concerned with the construction of fuzzy logic piecewise linear functions (PWL) that are used for surface approximation.

Usage of piecewise circuits is a known method but diode-resistor networks are difficult to be implemented in CMOS integrated circuits. Some methods are proposed for the solution of this problem. One of them is the use of current mirrors to obtain diode like curves where slopes are defined by the *W/L* ratios. In this work, the optimization of low power, current mode CMOS circuits for synthesis of arbitrary nonlinear functions [1], are observed.

Various combinations of CMOS current mirror circuits are used to realize PWL functions. There are several sources of errors in design of such functions. In order to simplify the optimization of these error calculations, PWL circuits are divided into smaller circuits which are assumed to be current mirrors in this work. Implementation error which is caused by deviation from the real solution surface and mismatch errors between current mirror transistors due to difference between threshold voltages (V_{TO}), oxide capacitance (C_{OX}), width and length of transistor values are considered as the main sources of errors in this work. These error sources can be summarized as follows.

- Deviation from the original solution surface
- Difference in the drain voltages
- Difference in the threshold voltages
- Difference in the C_{OX} values
- Difference in the *W* and *L* values

In this work each of these errors is calculated independent of the other errors and in the end all of the calculated errors are added. This final error is regarded as the total error and the *W* and *L* values are calculated according to this total value.

Design duration is also getting an important issue in the new world order. Sometimes time is much more important than scope, that is, what is done or what is needed to be done. At least, when time to market concept is considered, lots of work must be accomplished in limited time periods. Here in this work, the main purpose is to develop a computer aided design tool to adjust the current mirror transistor values of PWL circuits used in fuzzy logic surface approximation. This will make the overall design easier for developer to pass by this stage faster with better assumptions, when several constraints which are mentioned above and going to be mentioned briefly in the on going chapters, to design the overall circuit are taken into consideration. This purpose can also be clarified as follows; this work represents a design tool for calculation of optimized W and L values of current mirror transistors for various values of reference current within a specified error to find the best transistor parameters for possible minimum power dissipation.

Results are tested on several applications to verify that the results of the design tool presented in this work are perfectly matching with the simulation results. EKV analytic models are used in both calculations and simulations.

EKV model claims to satisfy most of criteria required for a good MOSFET model, suitable for analog applications. In addition, the EKV model is hierarchically structured, offering several coherent hierarchical levels, from simple analytical expressions to support creative synthesis, to more detailed expressions for precise computer simulation. The simplicity and intuitiveness of the EKV model helps the circuit designer to understand the operation of the MOS transistor and to correctly exploit and master its various characteristics in order to develop new high performance circuits.

From the overall extractions of this work, it has been seen that instead of designing and calculating PWL circuits manually, introduced optimization tool may well be used in such processes.

The organization of this thesis is as follows; Chapter 2 will introduce the background of the problem, why there is a need for such design tool and the method used in this work to reach the desired purpose is determined. In Chapter 3, heart of the design

tool, EKV analytical modeling of transistor currents will be explained. In Chapter 4, software flow will be examined and the input and output format of the design tool will be introduced. In Chapter 5, analog circuits that are used to verify the design tool are introduced and results are presented. In Chapter 6, a brief summary and conclusion is made, possible future works are mentioned.

2. BACKGROUND OF THE PROBLEM AND DESIGN METHODOLOGY

2.1. Background of the Problem

There are several possible inputs for current mirror design of PWL circuits in surface approximation of fuzzy logic solutions. In this work these wide range of inputs are limited according to some constraints and assumptions. It is assumed that the most effective errors in calculation of current mirror transistor parameters are V_T, C_{OX}, $W\backslash L$ and V_D differences and the best and the easiest way to model these errors is the usage of EKV models. The constraint is to hold the error with in a specified range in addition with the implementation error occurred during the surface approximation of PWL circuits. Sustaining the specified power dissipation is another important issue in design.

For the following calculations, P is used for total error performance while S and E_{imp} represent fuzzy surface and implementation error.

$$S \cong f_1(x) \tag{2.1}$$

$f_1(x)$ is the approximated surface and it is more or less the same as the fuzzy surface. In fact, there is a difference between these surfaces. Therefore, surface estimation of fuzzy logic solution with PWL has the following error:

$$E_{imp} = S - f_1(x) \tag{2.2}$$

Error due to the surface approximation of fuzzy logic solution with PWL

$$P = E_{imp} + E\left(\Delta C_{OX}, \Delta V_T, \Delta V_D, \Delta \frac{W}{L}\right) \tag{2.3}$$

The problem is to find the optimum W (width) and L (length) values of current mirror transistors, with the P (performance) value with in the specified power dissipation. There exist several solutions for different values of I_D. It is also considered that, it is better to minimize the design area for power optimization. Therefore, the optimum W and L values are the possible minimum values required to satisfy the power constraint with in the specified error range.

EKV MOSFET parameters are preferred to be used in such designs. The main reason for EKV model usage is that in this formulation MOSFET current characteristic is continuous in all regions. Therefore, this characteristic supplies an important simplicity in calculation of transistor parameters [2].

Another issue that is examined in this work is interpolation. Several interpolation techniques are observed but since the point of interest on this work is not interpolation linear interpolations used as the basic interpolation technique. This technique is used to approximate the fuzzy solution surfaces which are going to be realized by PWL circuits whose transistor parameters are calculated by the optimization software explained and designed in this work.

Several optimization techniques are observed in early works [3]. One of them is OAC [4] which is a two stage optimizer similar to the one mentioned in this thesis. In the first stage a circuit topology is defined and then in the second stage, circuit elements parameters or circuit sizing is done.

Another approach to circuit optimization in building the concept in this work is genetic algorithms. Genetic algorithms are also used in design optimization [5-6].

Piecewise Linear (PWL) circuits are not a new concept in approximating surfaces as it is defined in this work. PWL circuits are commonly used in networks where diode characteristics are needed. They are known to be diode like circuits with several breakpoints adjusted by the design. PWL circuits especially introduce a good solution to diode-resistor characteristic circuit elements which can be implemented to integrated

circuits with the current CMOS technologies. Slopes of this circuits are controlled by the current mirrors *W/L* ratios [7].

On this point of view Prof. Wilamowski's PWL logic circuits are examined, which are going to be observed briefly in all aspects on going chapters. System that is introduces in thesis is built on the concept of these designs.

Many application fields are observed during the survey of this work. Fuzzy networks are found to be the best matching application field for PWL circuit design because of the characteristic of these circuits.

2.2. Design Tool for Optimization of Analog Fuzzy Implementation

Performance estimator tools are mainly used for increasing the design speed as well as preventing the man made errors. This tool is used to automize and increasing the speed of the approximation and optimization of fuzzy logic circuit designs by optimizing several values defined in the circuit. The accuracy of approximation and optimization are in great importance to the designer since designer will construct the following design on these estimations. Calculation is made depending on some assumptions and some constraints. With in these constraints results are determined to be precise. System has several inputs and outputs depending on the expected output which makes the system much more sensitive to inputs. Dependency to inputs are designed to maximize the freedom of the designer on adjusting its design parameters, making decision trees and working over the trade offs analog design.

2.2.1. Methodology Used for Design Tool

In this work, power dissipation in defined error limits and best approximation to the expected solution surface are the main design constrain. Power optimization leads to a dependency on C_{OX}, V_T, *W/L* ratios and input current of the system. Other parameters considered to be fixed. Here the point is to discover the error caused by these differences

mentioned, which are going to be called as design errors, and adjusting this error to a defined value while minimizing the power dissipation. Proper *W* and *L* values will be defined for the possible best optimized design for the output of this process.

Surface approximation error will be considered as the implementation error. In approximation to solution surface some breakpoints are selected according to some constraints defined by the user. This constraint defines the amount of breakpoints to be selected and implementation error. For example, defining more breakpoints will increase the accuracy of the approximation while increasing the transistor numbers which means increase in the power dissipation. This trade off must be defined and determined by the designer. In this work MATLAB libraries and compiler is used for algorithmic calculation of this process. Input and output of this process are defined as text files so that these files can be used as a source for different development environments.

After surface approximation and circuit design with the help of approximation output with the power optimization algorithm, there will be deviation from expected results. As it is told above there will be two main sources for that deviation. First one is the approximation error which is also defined as implementation error and the design error caused because of the mismatches of current mirror transistors of PWL circuits.

In order to limit the error range user will define a total error limit. Then the difference between the total error and the implementation error will give the design error limit for designer. From this point, design tool will define possible *W* and *L* values in the given range of input current. With the definition of input current and optimized *W* and *L* values, the minimum size to supply the given circuit will be defined, by this way power dissipation will also be minimized.

Transistor behaviors are modeled by the EKV equations. However, in defining large analog circuits with this method is a time consuming and complex process. Therefore in this work, PWL circuits are divided into its molecules which are current mirror. From this point of view, several sub PWL circuits are examined and design criteria for these circuits are defined. These circuits are referenced from the works defined in [1].

Afterwards with the help of these circuits, one and two dimensional two sample circuits are designed and outputs of these circuits for several input values are calculated with the help of previously defined circuits' results. Calculated values are compared with the simulation results to display the accuracy.

The whole process can be summarized as; approximating a solution surface with in the defined precision. In this work fuzzy solution surface is used as an example but in need not to be a fuzzy surface; it is just an application field used in this work. Then after, with the help of this approximation and breakpoints obtained from this approximation, a circuit will be designed to give the approximated surface as output. The transistor parameters will be calculated by the power optimization tool. And outputs will be examined by H-Spice and MATLAB simulations.

Finally a fuzzy logic surface is selected as an application field to show that the approximated and power optimization, with in the defined error limit and input current variation range by defining optimum W and L values, method can be used in the real world solutions. Circuits examined in this work can be summarized as follows:

- Simple NMOS Current Mirror
- Simple PMOS Current Mirror
- NMOS – PMOS Combination of Current Mirrors
- PMOS – NMOS Combination of Current Mirrors
- Double Breakpoint NMOS Circuit
- Double Breakpoint PMOS Circuit
- Improved NMOS Current Mirror Circuit
- Improved NMOS Current Mirror Circuit
- Sample Current Mirror Combination Circuit
- Sample One Dimensional Circuit
- Sample Two Dimensional Circuit
- One Dimensional Fuzzy Logic Example Approximation (Inverse Kinematics)
- Two Dimensional Fuzzy Logic Example Approximation (Inverse Kinematics)

Design tool explained in this work can be used in all designs where the current mirrors are the molecule or it can be said that, heart of the design. Therefore, it can be said that the solution explained in this work is independent of the application field, fuzzy networks, mentioned in this work.

In the following chapter analytic EKV MOSFET model used in this work is introduced.

3. DEFINITION OF TRANSISTOR CURRENT

3.1. Parameter Calculations

In this work, EKV model for MOS transistors is used to define mathematical solutions of the circuits. This model is an analytical analysis model for low-voltage, low-current analog circuits [2].

Large and small signal parameters are all continuous in the EKV MOSFET Model. This model is based on the $V_p - V_{ch}$ which is defined to be the inversion charge Q. V_p is the pinch-off voltage and V_{ch} is the channel voltage.

Since the EKV model is continuous in all regions of the transistor, it allows the designer to use the same I_D equation in all regions. I_D in the EKV MOSFET Model is expressed as the difference between the forward current I_F and the reverse current I_R. EKV MOSFET model is derived from the charge-sheet formulation [3].

$$I_D = 2 \cdot N \cdot \mu \ \cdot C_{ox} \cdot \frac{W}{L} \cdot (U_t)^2 \cdot \left[\ln^2 \left(1 + e^{\frac{\frac{V_G - V_T}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_T}{N} - V_D}{2 \cdot U_t}} \right) \right] \tag{3.1}$$

$$V_P = \frac{V_G - V_{TO}}{N} \tag{3.2}$$

$$I_S = 2 \cdot N \cdot u \cdot C_{ox} \cdot \frac{W}{L} (U_t)^2 \tag{3.3}$$

$$Kp = u \cdot C_{ox} \tag{3.4}$$

For EKV model used in this work; N is 1.8, C_{OX} is 3.45 x 10^{-3}, Kp_n is 150.10^{-6}, Kp_p is 300.10^{-6}, U_t is 25.8 x 10^{-3}, V_{TO} is 0.55 for NMOS transistors and V_{TO} is -0.55 for PMOS transistors.

$$V_T = |V_{TO}| \tag{3.5}$$

$$V_G = |V_{GO} - V_{BULK}| \tag{3.6}$$

$$V_S = |V_{SO} - V_{BULK}| \tag{3.7}$$

$$V_D = |V_{DO} - V_{BULK}| \tag{3.8}$$

$$I_S = 2.N.K_P.\frac{W}{L}(U_t)^2 \tag{3.9}$$

$$V_G = |V_{GO} - V_{BULK}| \tag{3.10}$$

Taking this formula as the reference point, errors can be calculated mathematically. W/L will be decided by software.

The first error to be calculated is the current error due to the difference between the drain voltages of the each transistor of the current mirror. This calculation is done for several I_D values (start, stop, and step size of I_D current range is defined in the CAD input file.) and for a range of W/L values (from 10 to 1/10).

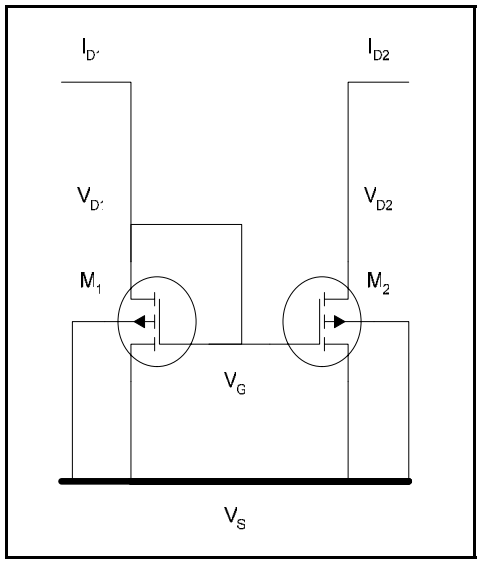

Figure 3.1. NMOS current mirror circuit

$$I_{D1} = 2 \cdot N \cdot u \cdot C_{ox} \cdot \frac{W}{L} \cdot (U_t)^2 \cdot \left[\ln^2 \left(1 + e^{\frac{\frac{V_G - V_T}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_T}{N} - V_{D1}}{2 \cdot U_t}} \right) \right] \tag{3.11}$$

$$V_{D1} = V_G \tag{3.12}$$

$$I_{D2} = 2 \cdot N \cdot u \cdot C_{ox} \cdot \frac{W}{L} \cdot (U_t)^2 \cdot \left[\ln^2 \left(1 + e^{\frac{\frac{V_G - V_T}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_T}{N} - V_{D2}}{2 \cdot U_t}} \right) \right] \tag{3.13}$$

$$\Delta I_D = I_{D1} - I_{D2} \tag{3.14}$$

$$error = \frac{\Delta I_D}{I_{D1}} \tag{3.15}$$

$$error1 = \frac{\ln^2\left(1+e^{\frac{\frac{V_G-V_{TO}}{N}-V_{D2}}{2\cdot U_t}}\right)-\ln^2\left(1+e^{\frac{\frac{V_G-V_{TO}}{N}-V_{D1}}{2\cdot U_t}}\right)}{\ln^2\left(1+e^{\frac{\frac{V_G-V_{TO}}{N}-V_S}{2\cdot U_t}}\right)-\ln^2\left(1+e^{\frac{\frac{V_G-V_{TO}}{N}-V_{D2}}{2\cdot U_t}}\right)} \tag{3.16}$$

In this error calculation, C_{ox}, V_{TO} (threshold voltage) and the W/L ratios are thought to be the same which means I_{S1} is equal to I_{S2}. Drain voltage of the second transistor V_{D2}, is defined to be 1.65V, since the supply voltage is defined as 3.3V and the aim is to supply the maximum swing and the symmetry in the circuit. Drain voltage of the first transistor V_{D1} is calculated for different values of the reference current I_{D1}. Due to the cancellation of I_S values of W/L ratio does not effect the result.

The second source of error is the difference in the C_{OX} values. The difference in the C_{OX} values of each transistor may also lead to an error.

$$C_{OX} = \frac{t_{OX}}{\varepsilon_{Si}} \tag{3.17}$$

$$I_{D1} = 2\cdot N\cdot u\cdot C_{ox1}\cdot\frac{W}{L}\cdot(U_t)^2\cdot\left[\ln^2\left(1+e^{\frac{\frac{V_G-V_T}{N}-V_S}{2\cdot U_t}}\right)-\ln^2\left(1+e^{\frac{\frac{V_G-V_T}{N}-V_{D1}}{2\cdot U_t}}\right)\right] \tag{3.18}$$

$$I_{D2} = 2\cdot N\cdot u\cdot C_{ox2}\cdot\frac{W}{L}\cdot(U_t)^2\cdot\left[\ln^2\left(1+e^{\frac{\frac{V_G-V_T}{N}-V_S}{2\cdot U_t}}\right)-\ln^2\left(1+e^{\frac{\frac{V_G-V_T}{N}-V_{D1}}{2\cdot U_t}}\right)\right] \tag{3.19}$$

From Equation 4.15,

$$error2 = \frac{\Delta C_{ox}}{C_{ox1}} \tag{3.20}$$

$$\Delta C_{ox} = C_{ox1} - C_{ox2} \tag{3.21}$$

ΔC_{OX}, which is defined in Equation 4.21 is determined by the model and technology used, in the input file.

The third source of error is difference in the threshold voltages, V_{TO}. This will affect the pinch-off voltages.

$$I_{D1} = 2 \cdot N \cdot u \cdot C_{ox} \cdot \frac{W}{L} \cdot (U_t)^2 \cdot \left[\ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_{D1}}{2 \cdot U_t}} \right) \right] \tag{3.22}$$

$$I_{D2} = 2 \cdot N \cdot u \cdot C_{ox} \cdot \frac{W}{L} \cdot (U_t)^2 \cdot \left[\ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_{D1}}{2 \cdot U_t}} \right) \right] \tag{3.23}$$

From Equation 4.15,

$$error3 = \frac{\left[\ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_{D1}}{2 \cdot U_t}} \right) \right] - \left[\ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_{D1}}{2 \cdot U_t}} \right) \right]}{\ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_S}{2 \cdot U_t}} \right) - \ln^2 \left(1 + e^{\frac{\frac{V_G - V_{TO}}{N} - V_{D1}}{2 \cdot U_t}} \right)} \tag{3.24}$$

After these error calculations, all the errors are added and subtracted from the total design error which is defined previously by the designer according to the sensitivity and the tolerance of the circuit, total error expected from the solution and the implementation error. The result gives the error limit for the final source of error which is the variation between the *W/L* ratios of the current mirror transistors. In more complex designs where more than one current mirror is used worst case, which is the longest path, that means the maximum current mirror amount from input to output node, is calculated and remaining error is divided to the number of current mirrors found in the worst case so that the error limit for each current mirror on such circuits is determined.

From Equation 4.15,

$$error4 = \frac{\Delta I_D}{I_D} = \frac{\Delta W/L}{W/L} \tag{3.25}$$

$$\Delta\left(\frac{W}{L}\right) = error4 \cdot \left(\frac{W}{L}\right) \tag{3.26}$$

$$\frac{W}{L} = \alpha \tag{3.27}$$

α is the constant ratio of *W* and *L* given by the designer. It ranges from 10 to 1/10 and all the solutions for each ratio are noted to find the best ratio which gives the best *W* and *L* values when power dissipation, error and technology limits are taken into consideration (In this work *ΔW* and *ΔL* are thought to be close to each other, otherwise a more detailed calculation method for *W*, *L* calculation than the one defined in Equation 3.28 must be used.).

$$\Delta\left(\frac{W}{L}\right) = \frac{\left(W + \Delta W\right)}{\left(L - \Delta L\right)} - \frac{W}{L} \tag{3.28}$$

$$W = L \cdot \alpha \tag{3.29}$$

$$L = \frac{\Delta W - \left(\Delta\left(\frac{W}{L}\right) + \frac{W}{L} \right) \cdot \Delta L}{\Delta\left(\frac{W}{L}\right)} \tag{3.30}$$

$$\Delta\left(\frac{W}{L}\right) = \begin{cases} \Delta\left(\frac{W}{L}\right) \Leftarrow 0 < \frac{W}{L} < 1 \\ -\Delta\left(\frac{W}{L}\right) \Leftarrow \frac{W}{L} > 1 \end{cases} \tag{3.31}$$

W/L, ΔW and ΔL values are defined in the technology file and Δ*(W/L)* value is obtained from the error calculation process. After the calculation of *W* and *L* values, it is verified whether they are in the range of the technology which is taken as 0.35µm AMS technology in this work. In this technology, *L* can be 0.35µm and *W* can be 0.45µm for minimum sized transistors.

3.2. Short Channel Effect

When short channel effect is taken into consideration technology minimums are not seem to be the best size to be taken. Short channel effect representation on a simple NMOS circuit is shown on the Figure 3.2.

It is better to take 1µm as the minimum size for both *W* and *L* values. Therefore, in the rest of this work 1µm will be taken as the minimum size and calculations will be done up to these values.

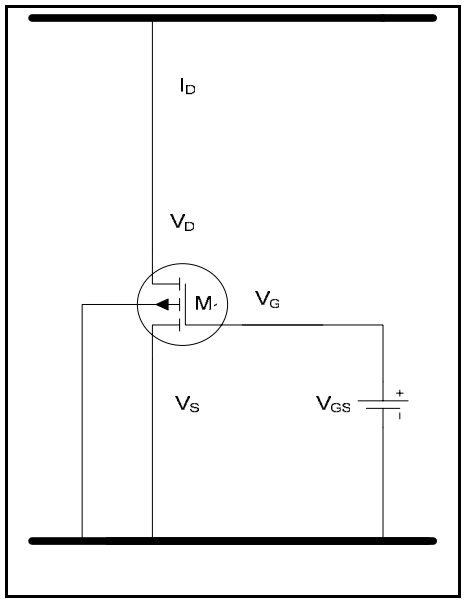

Figure 3.2. Simple Transistor Circuit ($W = L = 1$ µm).

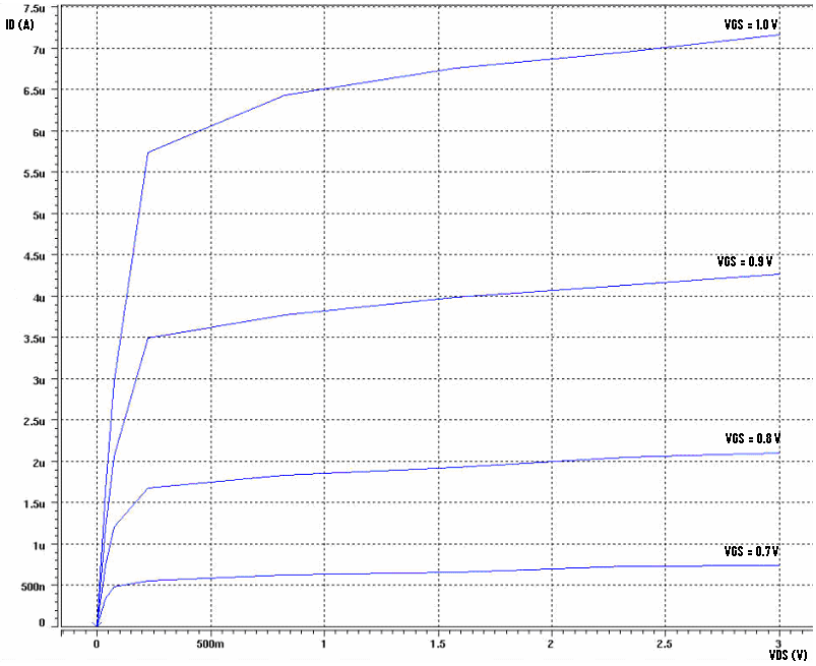

Figure 3.03. Short channel effect (W = L = 1 µm, VGS = 0.7, 0.8, 0.9, 1.0, VDS = 0-3).

4. SOFTWARE

System which is created in this work based on a computer aided design. This design is composition of several blocks which are shown in Figure 4.1.

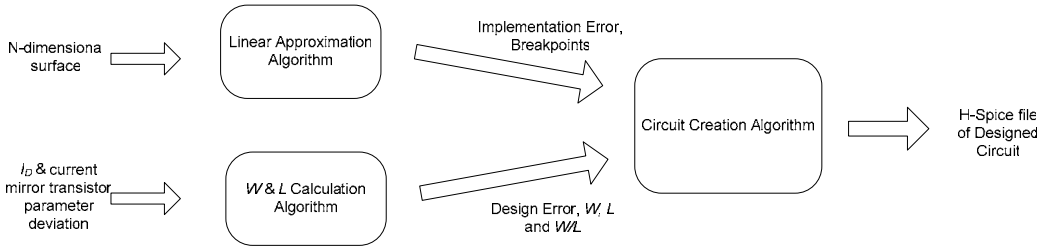

Figure 4.1. Block diagram of whole design

Circuit Creation algorithm is the core of this design, while Linear Approximation algorithm supplies the breakpoints for PWL design and *W* & *L* Calculation algorithm supplies the transistor parameters of PWL circuits. Blocks in Figure 4.1 will briefly be explained in the following sections.

4.1. *W & L* Calculation Algorithm

The main algorithm of the program is as described in Figure 4.2. User defined specifications can be read from a file or they can be entered simultaneously from the command prompt. Block diagram of the *W* & *L* Calculation is shown in Figure 4.2.

Outputs are written to a text file so that it can be followed easily. This process is repeated for the current values that are defined by the user. In addition, for every current value, *W* and *L* values are calculated for *W/L* ratios ranging from 1/10 to 10.

In Figure 4.3, “n” refers to the type of the MOSFET. If it is “1”, type is PMOS; if it is “0”, type is NMOS. “Vsupply” refers to the supply voltage of the overall circuit. “Vs1”

is the source potential of the first transistor where “Vs2” is the supply potential of the second transistor. “deltaCox” is the expected difference between C_{OX} values of current mirror transistors. “deltaVt” is the expected difference between V_{TO} values of current mirror transistors. “I_D” refers to the input current of the circuit. First parameter of the I_D is the initial voltage, second parameter is the final voltage and the final parameter is the step size used to reach from initial parameter to final parameter. “W/L” is the optimum aspect ratio. “Cox” is the model value of the C_{OX} (for EKV model in this work). “Ut” is the thermodynamic voltage. “Vt” is the model value of the V_{TO} (for EKV model in this work). “N” is Linearized body effect. “u” is the electron mobility μ. “deltaW” and “deltaL” are the expected variations of *W* and *L* values between current mirror transistors. “totalerror” is the remaining error range when the implementation error is subtracted from the total error expected by the designer. These parameters changes from design to design as well as from type PMOS to NMOS. Designer first set these values and then design tool will make calculations according to these assumptions.

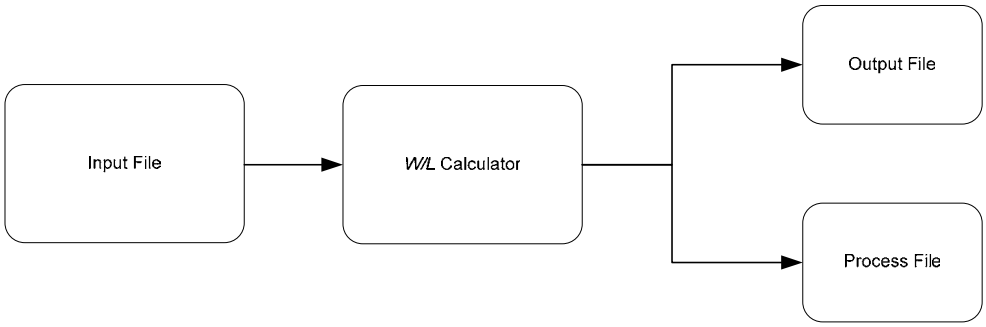

Figure 4.2. Block diagram of W & L Calculation algorithm

```
n = 0
Vsupply = 3.3
Vs1 = 3.3
Vs2 = 3.3
deltaCox = 3.45E-5
deltaVt = -0.0055
ID = 10e-6 100e-6 10e-6
W/L = 1
Cox = 3.45E-3
Ut = 25.8e-3
Vt = -0.55
N = 1.8
u = 10e-3
deltaW = 0.01e-6
deltaL = 0.01e-6
totalerror = 0.2
```

Figure 4.3. W & L Calculation input file

Software flowchart is shown in Figure 4.4.

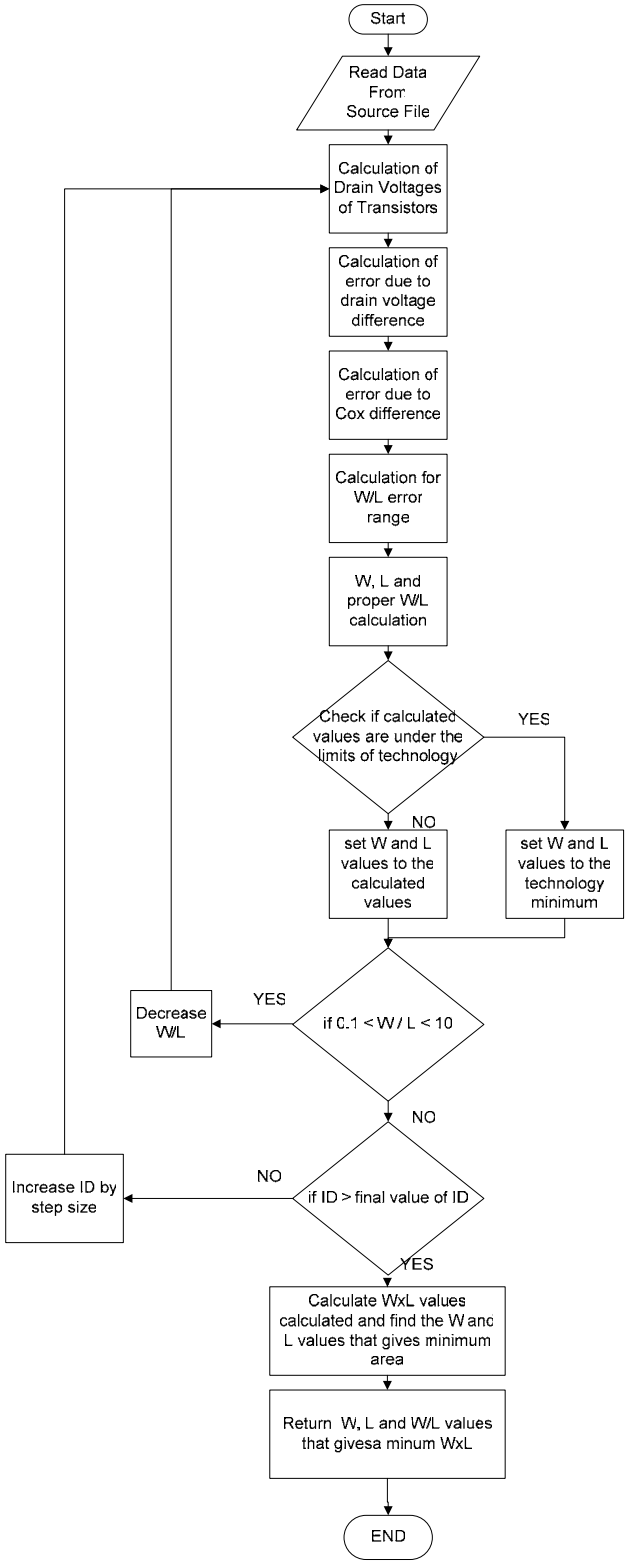

Figure 4.4. W & L Calculation algorithm flowchart

4.2. Linear Approximation Algorithm

Approximation algorithm is designed for approximating the real solution surface with possible minimum points. These points are regarded as the breakpoints and written to a file where they are going to be read to create a spice file. Block diagram of the software is shown in Figure 4.5.

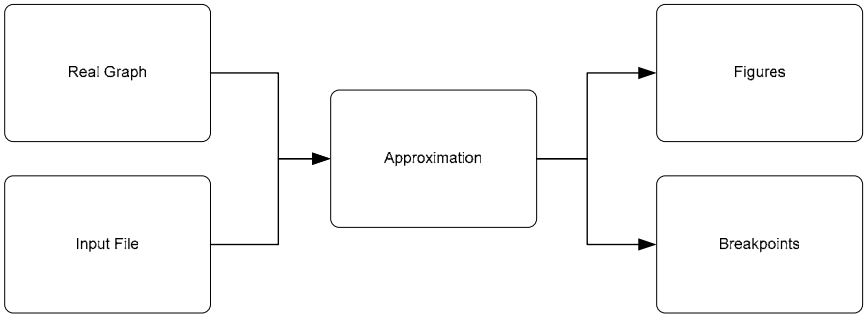

Figure 4.5. Block diagram of Linear Approximation algorithm

As you can see from the block diagram Real Graph is the input of the approximation algorithm. Another input is the Input file where some criteria are defined by the user. A sample input file is shown in Figure 4.6.

In Figure 4.6 “invkine1” is the name of the input file. Dimension of the input surface is specified by the user in the second column above. İn this sample it is defined to be “2”. If it is going to be one dimensional solution it will be assigned as “1”. Threshold constant defined in the third column is going to be used in defining the threshold of the breakpoint selection. In breakpoint selection variance of the output points is defined. Then the output points whose second derivative exceeds the variance multiplied by the threshold constant defined in the third column of the input file are selected as the breakpoints. Forth column determines the total error range of the overall design. And the last column represents the error occurred due to the approximation algorithm defined here. This input file is also going to be an input for the spice file creation algorithm.

Output of this algorithm will be the actual graph which is approximated and the breakpoint which are written to a file. Breakpoint file will be a text file and the format will be as shown in Figure 4.7.

Input current range of the circuit creation algorithm is defined to be larger than zero so that the output breakpoints of approximation algorithm must be normalized if there are values under zero. In normalization initial value of each input is added to all input values of the same dimension. A sample is shown in Figure 4.8.

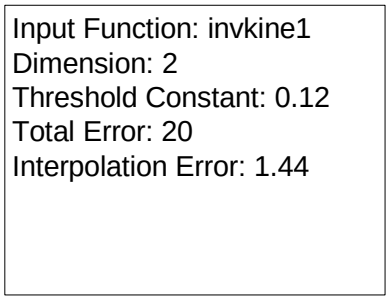

Figure 4.6. Input file of the Linear Approximation algorithm

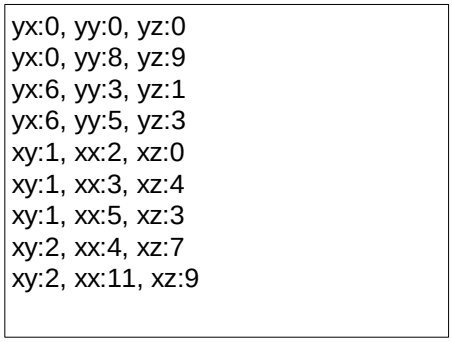

Figure 4.7. Linear Approximation output for two dimensional surface approximation

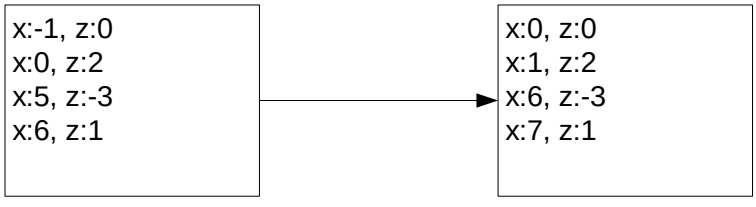

Figure 4.8. Normalization of breakpoints for one dimentional case

Software flowchart of the algorithm will be as shown in Figure 4.9.

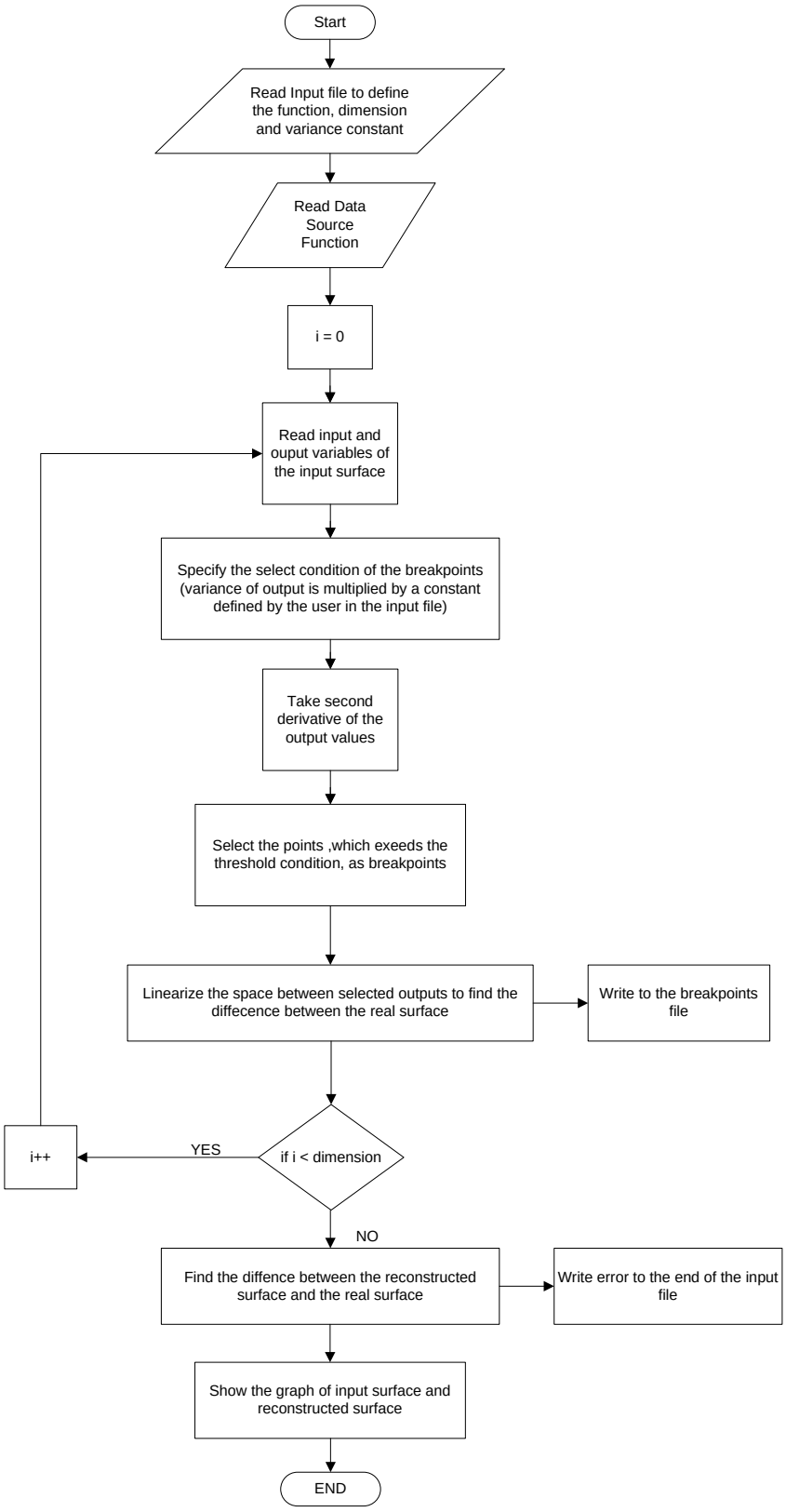

Figure 4.9. Linear Approximation algorithm flowchart

4.3. Circuit Creation Algorithm

This algorithm is used for the creation of the spice output file in order to establish a circuit whose output will be the approximated surface. In creation of this surface *W* and *L* values used in this design will be determined by the *W* and *L* calculation value. Therefore created circuit will be a power optimized circuit which supplies the defined input solution surface. Here in this work a fuzzy solution surface is used as an input to this algorithm but any kind of surface may be an input.

Circuit creation is done in one and two dimension modes. To show that it is a working system and it can easily be enlarged to multi-dimensional input, optimized surface approximation designs. A rough block diagram of the algorithm is shown in the Figure 4.10.

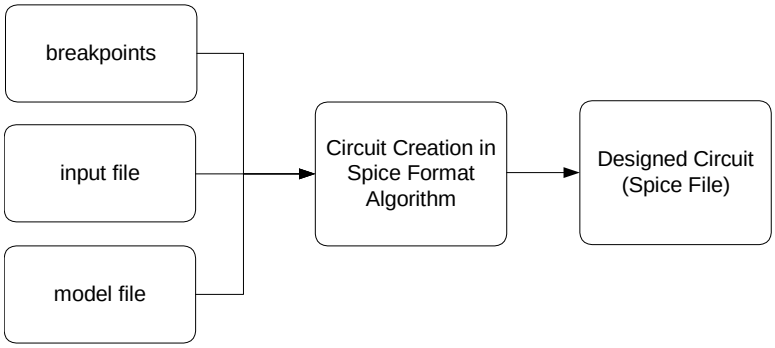

Figure 4.10. Block diagram of Circuit Ceation algorithm

Model file is the text file where the model which is going to be used is written. In this work EKV model is used.

Input file is shown in the figure 5.5. Approximation error in the last column of the input file, calculated by the approximation function, is subtracted from the total error defined in the third column of the input file. Then the worst path which is also the longest path from input node to output node is calculated. That is the maximum current mirror number from input node to output node. Then the remaining error is divided to worst case number and the remaining error range for each current mirror is defined.

Software flowchart of the Circuit Creation Algorithm is shown in Figure 4.11.

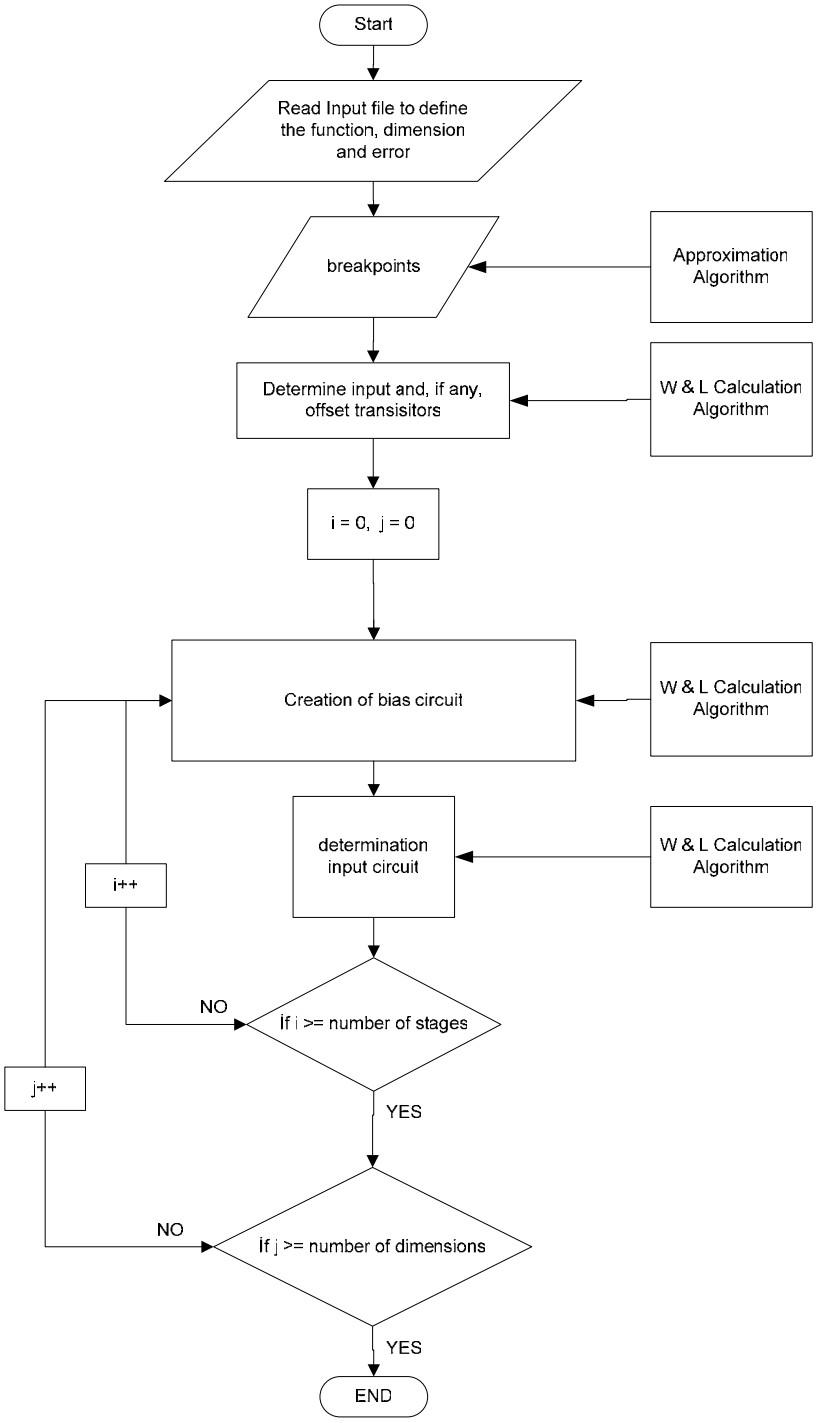

Figure 4.11. Circuit Creation algorithm flowchart

Next chapter is going to deal with the application of developed design process on the selected circuits.

5. ANALOG CURRENT MIRROR COMBINATION BLOCKS

Formuls derived in Chapter 3 are used on the following circuits which are used as the main stones of PWL circuits to approximate fuzzy logic solution surfaces. The aim is to find the optimum *W* and *L* values that lead to the minimum error and minimum power consumption.

5.1. Simple NMOS Current Mirror Circuit

This is a simple NMOS current mirror circuit. Current mirror is fed by a current source I_{IN} and output node is fixed to the half of the V_{SUPPLY}. The same current that flows on the M1 transistor is expected to be seen on the M2 transistor as I_{OUT}.

V_D is calculated as $7.75 \cdot 10^{-1} V$, *error1* is calculated as $1.808 \cdot 10^{-12}$, *error2* is calculated as 0.01 and *error3* is calculated as $4.661 \cdot 10^{-2}$. Since the total error is defined to be 0.2, the remaining error is used to calculate the *W* and *L* values.

$$error4 = totalerror - (error1 + error2 + error3) \tag{6.1}$$

From Equation 6.1, remaining error *error4* is calculated as 0.14339. From this calculation and from Equation 3.29 and Equation 3.30, *W* and *L* are calculated as $1 \cdot 10^{-8} m$.

The calculated total error is simply the sum of all errors. However, the simulation results are different which shows that some errors tend to cancel each other. In reality, the errors may be in such a fashion that they may add up or cancel each other. For the following NMOS transistors these values are going to be used.

In Table 5.1, I_{out} (V_{d2} is 1.65V) refers to output current of the circuit while the drain voltage of the output transistor is connected to 1.65V to obtain the maximum symmetry in the circuit, I_{out} (C_{OX} error) refers to output current of the circuit while the C_{OX} values of each transistors of the current mirrors are different from each other by the ratio of 1%, I_{out} (V_t error) refers to output current of the circuit while the V_t values of each transistors of the current mirrors are different from each other by the ratio of 1%, I_{out} (All errors) refers to output current of the circuit while all the causes of errors are taken into consideration, V_{drain} refers to the drain voltage of the first transistor from which reference current passes through.

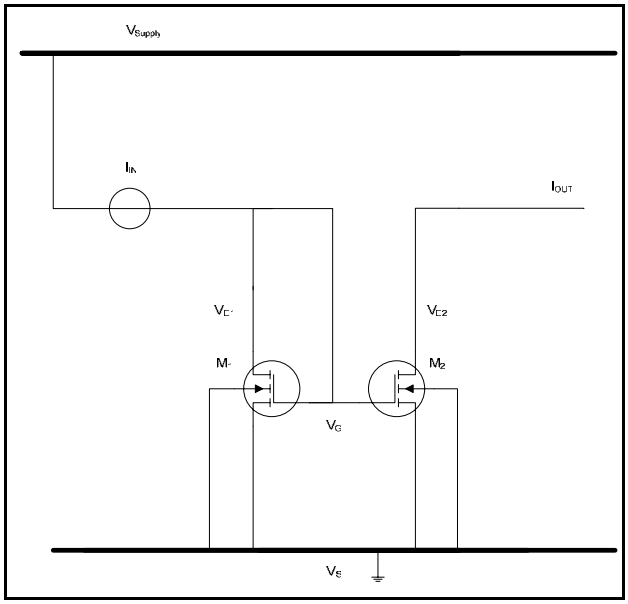

Figure 5.1. Simple NMOS current mirror circuit

Table 5.1. Simple NMOS current mirror comparison

Values	Calculated	Simulation
I_{out} (V_{d2} = 1.65V)	1.00 µA	1.04 µA
I_{out} (C_{OX} error)	1.02 µA	1.01 µA
I_{out} (V_t error)	0.95 µA	0.942 µA
I_{out} (All errors)	0.80 µA	0.94 µA

For the input range of 0 to 10µA the output characteristic of the circuit is as shown in Figure 5.2.

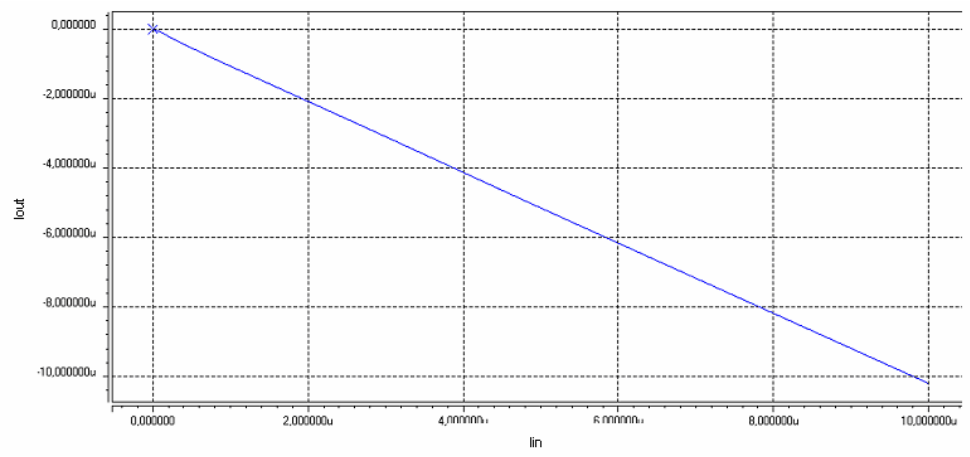

Figure 5.2. H-Spice simulation of simple NMOS current mirror

5.4. Simple PMOS Current Mirror Circuit

This is a simple PMOS current mirror circuit. Current mirror is fed by a current source I_{IN} and output node is fixed to the half of the V_{SUPPLY}. The same current that flows on the M1 transistor is expected to be seen on the M2 transistor as I_{OUT}.

V_D is calculated as 2.43V, error1 is calculated as $1.83806 \cdot 10^{-13}$, error2 is calculated as 0.01 and error3 is calculated as $3.27 \cdot 10^{-2}$. Since the total error is defined to be 0.2, the remaining error is used to calculate the *W* and *L* values.

From Equation 6.1, *error4* is calculated as 0.1573. From this calculation and from Equation 5.29 and Equation 5.30, *W* and *L* are calculated as $9 \cdot 10^{-9} m$. Since this value is less then the technology limits these parameters are set to technology minimum $1 \cdot 10^{-8} m$. For the following PMOS transistors, these values are going to be used.

Again, since these lengths are under the limits of the 0.35µm technology, 1µm is used for both the *L* and *W* values for *W/L* ratio is equal to one. The reason for not using the minimum allowable length 0.45µm is to avoid short channel effect which is shown in this work in the following pages.

With these *W* and *L* ratios the following results are gained. Simulation results and calculated values are compared in the Table 5.2.

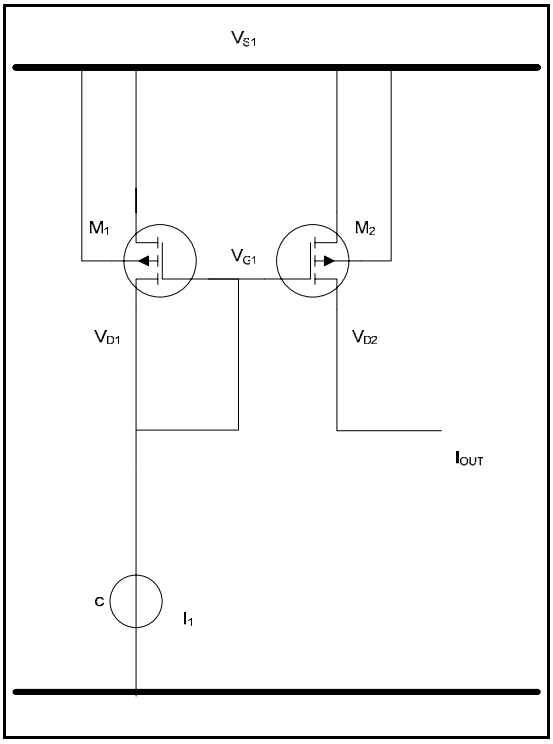

Figure 5.3. Simple PMOS Current Mirror

Table 5.2. Simple PMOS current mirror comparison

Values	Calculated	Simulation
$I_{out}(V_{d2} = 1.65V)$	1.00 µA	1.05 µA
$I_{out}(C_{OX}$ error)	1.01 µA	1.00 µA
I_{out} (V_t error)	0.96 µA	0.97 µA
I_{out} (all errors)	0.80 µA	0.97 µA

For the input range of 0 to 10µA the output characteristic of the circuit is shown in Figure 5.4.

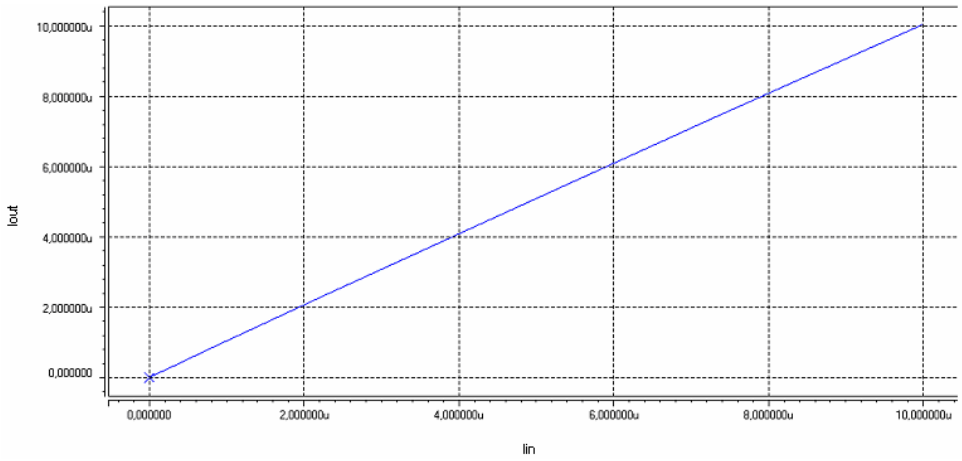

Figure 5.4. H-Spice simulation of simple NMOS current mirror

5.5. NMOS Current Mirror Breakpoint Circuit

This is a simple current mirror circuit that acts as a diode with one break point. Current mirror will not work until the input current passes the current value pulled down by the I_1 current. And output current will be set to the I_2 while the current mirror is off.

For $I_{IN} = 2\mu A$, $I_1 = 1\mu A$ and $I_2 = -1\mu A$ values on Table 5.3 are gained.

For the input range of 0 to 10µA the output characteristic of the circuit is as shown in Figure 5.6. I_1 and I_2 are set to 1µA while transistors aspect ratios are "1".

Table 5.3. NMOS current mirror circuit comparison

Values	Calculated (µA)	Simulation (µA)
$I_{out}(V_{d2} = 1.65V)$	2.00	2.00
$I_{out}(C_{OX}$ error)	2.02	2.01
I_{out} (V_t error)	1.95	1.94
I_{out} (all errors)	1.80	1.94

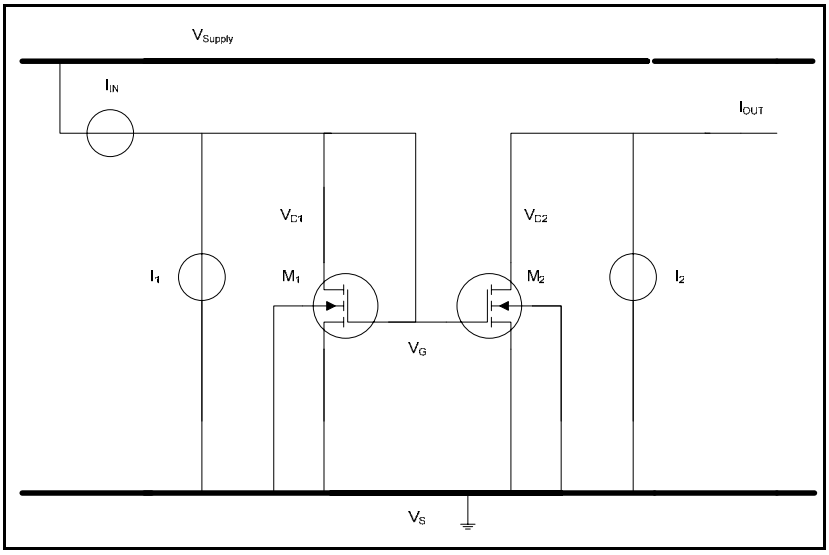

Figure 5.5. NMOS current mirror circuit

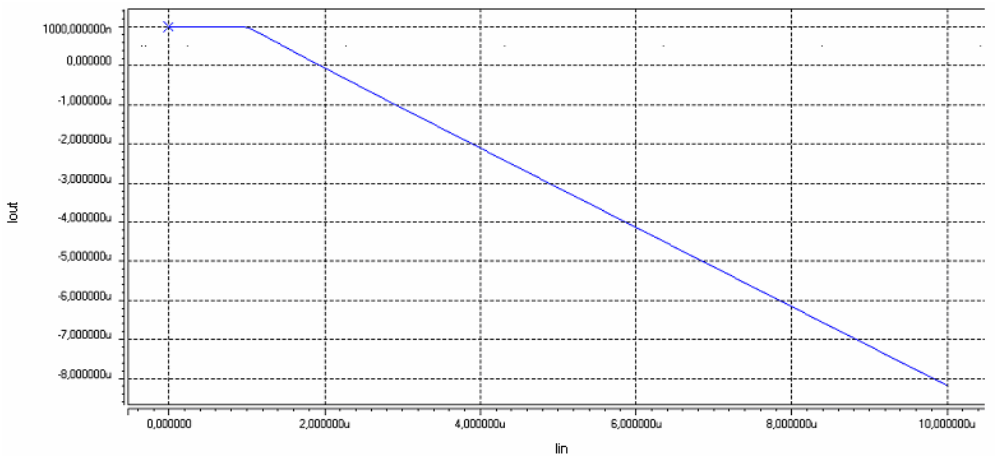

Figure 5.6. H-Spice simulation of NMOS current mirror with a single breakpoint

5.6. PMOS Current Mirror Breakpoint Circuit

This is a simple current mirror circuit that acts as a diode with one breakpoint. Current mirror will not work until the input current passes the current value pulled down by the I_1 current. And output current will be set to the I_2 while the current mirror is off.

For $I_{IN} = 0.5\mu A$, $I_1 = 0.5\mu A$ and $I_2 = 0.5\mu A$ values on Table 5.4 are gained.

For the input range of 0 to 10μA the output characteristic of the circuit is as shown in Figure 5.8. I_1 and I_2 are set to 1μA while transistors aspect ratios are "1".

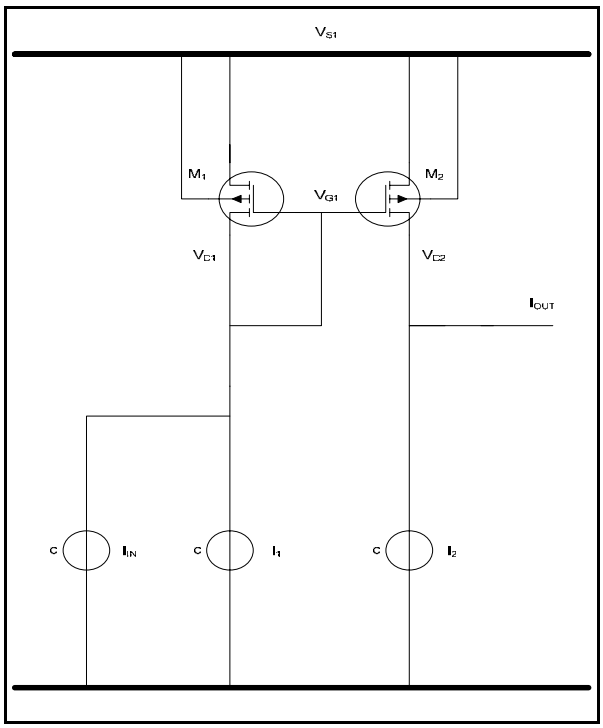

Figure 5.7. PMOS current mirror circuit

Table 5.4. PMOS current mirror circuit comparison

Values	**Calculated (μA)**	**Simulation (μA)**
$I_{out}(V_{d2} = 1.65\text{V})$	0.50	0.49
$I_{out}(C_{OX}$ error)	0.51	0.49
I_{out} (V_t error)	0.47	0.49
I_{out} (all errors)	0.30	0.49

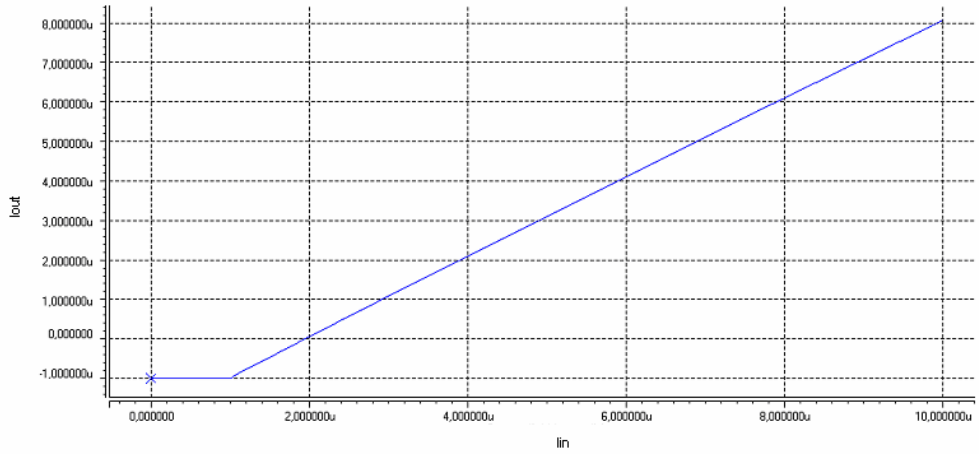

Figure 5.8. H-Spice simulation of PMOS current mirror with a single breakpoint

5.7. NMOS – PMOS Combination of Current Mirrors

In this circuit until the input current passes the value of I_1 system will be off. During that time output will be set to the value of I_2. While the system is on PMOS current mirror pulls up the output current that is transferred by the NMOS current mirror.

Due to the biasing in this circuit *W/L* ratio of the PMOS transistors is taken to be "2.5" while the NMOS transistor's *W/L* ratio is still "1". Errors of a PMOS transistor with *W/L* ratio"2.5" are; $2.06 \cdot 10^{-12}$ for *error1*, $1.00 \cdot 10^{-02}$ for *error2* and $4.34 \cdot 10^{-02}$ for *error3*.

The total expected error in this circuit is the addition of the error coming from the first current mirror with the error coming from the second current mirror.

For $I_{IN} = 2\mu A$, $I_1 = -1\mu A$ and $I_2 = 1\mu A$ values on Table 5.5 are gained.

For the input range of 0 to 10μA the output characteristic of the circuit is as shown in Figure 5.10. I_1 and I_2 are set to 1μA while transistors aspect ratios are "1".

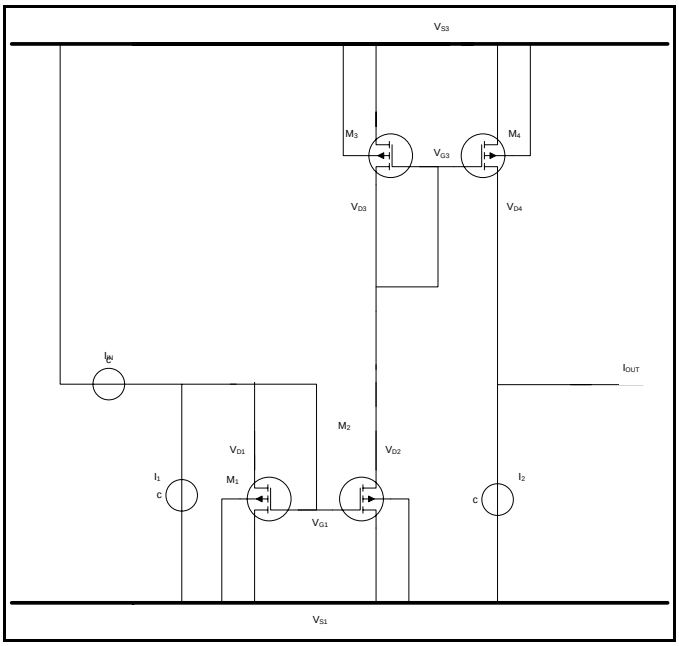

Figure 5.9. NMOS – PMOS combination of current mirrors

Table 5.5. NMOS – PMOS combination of current mirrors comparison

Values	Calculated (µA)	Simulation (µA)
$I_{out}(V_d = 1.65V)$	2.00	2.09
$I_{out}(C_{OX}$ error)	2.02	2.10
I_{out} (V_t error)	1.91	1.98
I_{out} (all errors)	1.60	1.98

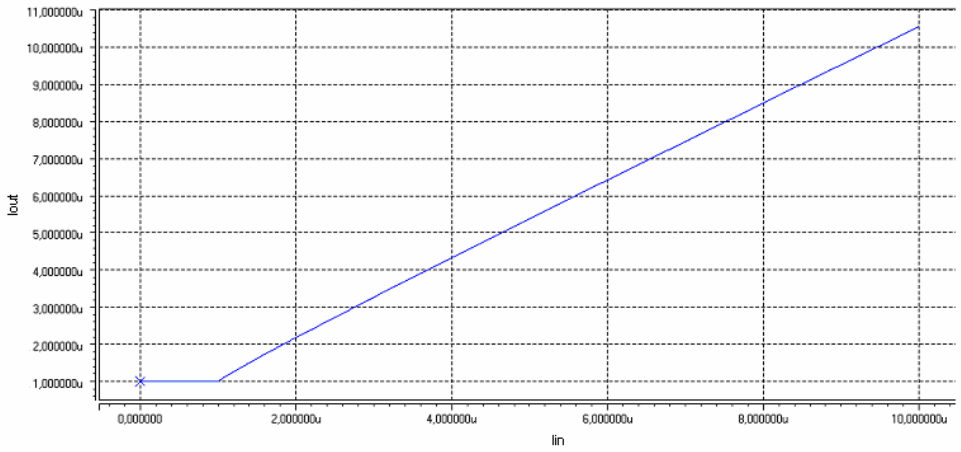

Figure 5.10. Simulation of NMOS-PMOS combinational single breakpoint circuit

5.8. PMOS – NMOS Combination of Current Mirrors

Here in this circuit until the input current passes the value of I_1 system will be off. During that time output will be set to the value of I_2. While the system is on NMOS current mirror pulls down the output current that is transferred by the PMOS current mirror.

Due to the biasing, in this circuit *W/L* ratio of the PMOS transistors is taken to be 2.5 times of the NMOS transistor's *W/L* ratio. Errors are; $2.06 \cdot 10^{-12}$ for *error1*, $1.00 \cdot 10^{-02}$ for *error2* and $4.34 \cdot 10^{-02}$ for *error3*.

The total expected error in this circuit is the addition of the error coming from the first current mirror with the error coming from the second current mirror. For $I_{IN} = 0.5\mu A$, $I_1 = 0.5\mu A$, and $I_2 = 0.5\mu A$ following values are gained.

For the input range of 0 to 10μA the output characteristic of the circuit is shown in Figure 5.12. I_1 and I_2 are set to 1μA while transistors aspect ratios are "1".

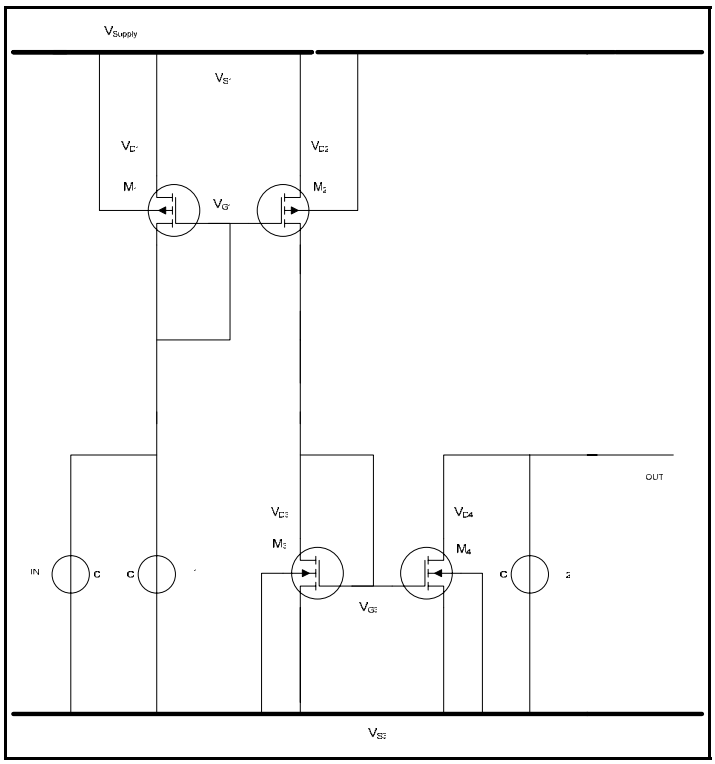

Figure 5.11. PMOS – NMOS combination of current mirrors

Table 5.6. PMOS – NMOS combination of current mirrors

Values	Calculated (µA)	Simulation (µA)
$I_{out}(V_d = 1.65V)$	0.50	0.69
$I_{out}(C_{OX}$ error)	0.52	0.65
I_{out} (V_t error)	0.41	0.52
I_{out} (all errors)	0.30	0.53

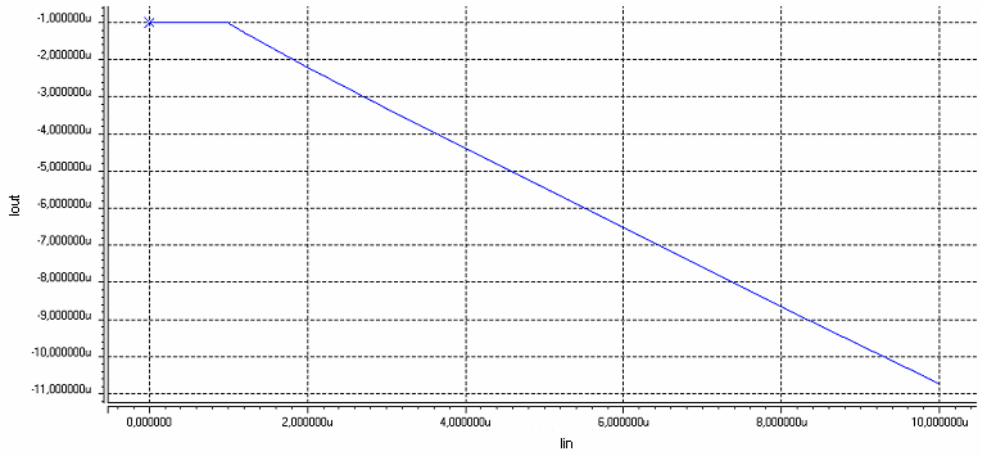

Figure 5.12. Simulation of PMOS-NMOS combinational single breakpoint circuit

5.9. Double Break Point Circuit with NMOS Transistors

In this network until input current passes the value of I_1 system will be off. During that time output is limited by the current I_2 transferred from M_3 to M_4. While the system is on, output current will be limited by the addition of M_2 and M_3 drain currents. System will not let I_2 current source to pass the value of this addition over the value of I_2. So that output will be off when the value of drain voltage of M_2 exceeds I_2 value.

For $I_{IN} = 2\mu A$, $I_1 = 1\mu A$ and $I_2 = 2\mu A$ values on Table 5.7 are gained. The total expected error in this circuit is the addition of the error coming from the first current mirror with the error coming from the second current mirror. For the input range of 0 to 10µA the output characteristic of the circuit is as shown in Figure 5.14. I_1 is set 1µA and I_2 is set to 4µA while transistors aspect ratios are "1".

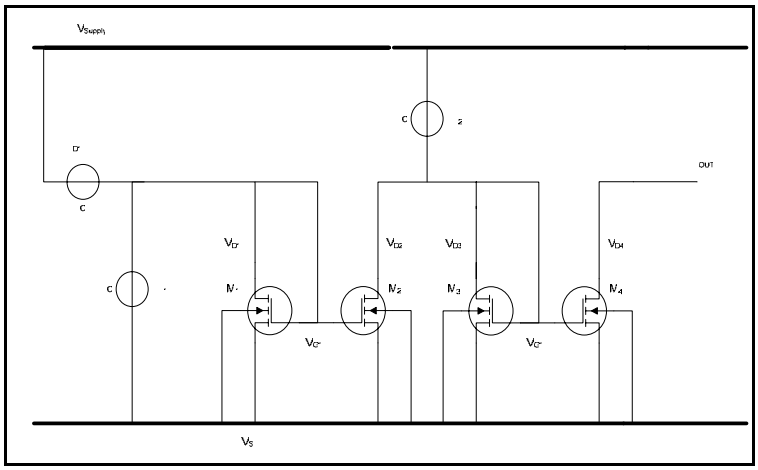

Figure 5.13. Double break point circuit with NMOS transistors

Table 5.7. Double break point circuit with NMOS transistors comparison

Values	Calculated (µA)	Simulation (µA)
$I_{out}(V_d = 1.65\text{V})$	1.00	0.99
$I_{out}(C_{OX}$ error)	1.02	1.00
I_{out} (V_t error)	0.91	0.99
I_{out} (all errors)	0.60	1.00

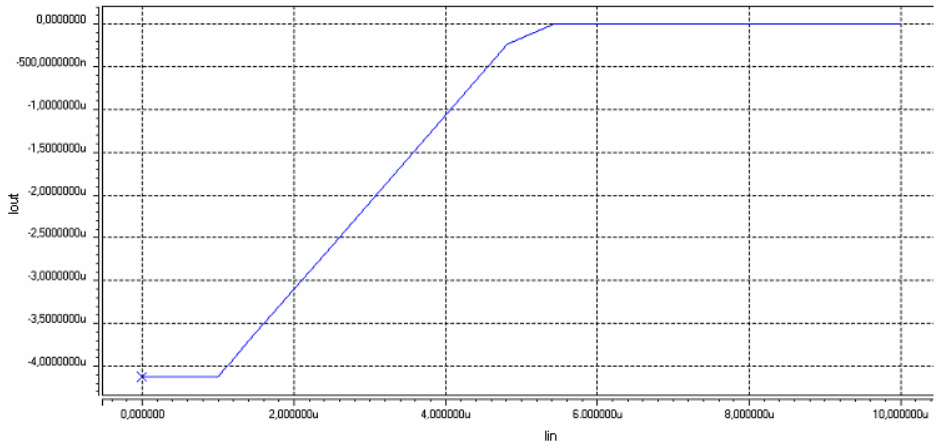

Figure 5.14. H-Spice simulation of double breakpoint NMOS combinational circuit

5.10. Double Break Point Circuit with PMOS Transistors

In this network until input current passes the value of I_1 system will be off. During that time output is limited by the current I_2 transferred from M_3 to M_4. While the system is on, output current will be limited by the addition of M_2 and M_3 drain currents. System will not let I_2 current source to pass the value of this addition over the value of I_2. So that output will be off when the value of drain voltage off M_2 exceeds I_2 value.

For $I_{IN} = 0.5\mu A$, $I_1 = 0.5\mu A$ and $I_2 = 2\mu A$ values on Table 5.8 are gained. The total expected error in this circuit is the addition of the error coming from the first current mirror with the error coming from the second current mirror.

Table 5.8. Double break point circuit with PMOS transistors comparison

Values	Calculated (µA)	Simulation (µA)
$I_{out}(V_d = 1.65V)$	1.00	1.05
$I_{out}(C_{OX}$ error)	1.02	1.00
I_{out} (V_t error)	0.93	0.99
I_{out} (all errors)	0.60	0.99

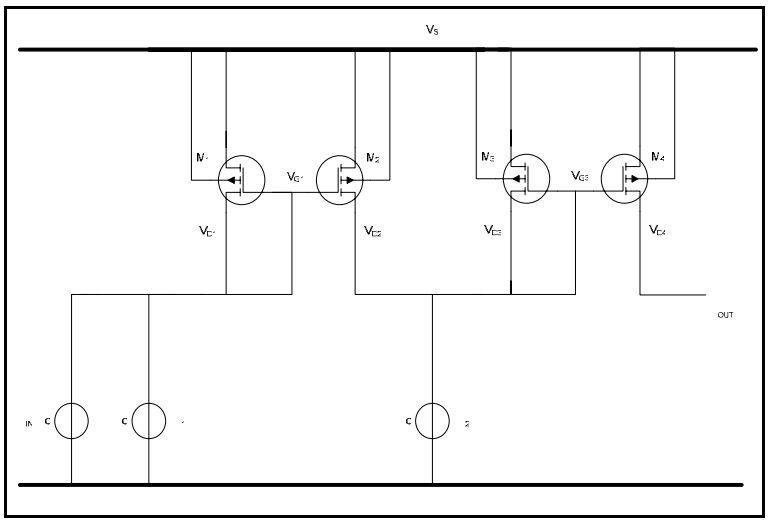

Figure 5.15. Double breakpoint circuit with PMOS transistors

For the input range of 0 to 10µA the output characteristic of the circuit is as shown in Figure 5.16.. I_1 is set 1µA and I_2 is set to 4µA while transistors aspect ratios are "1".

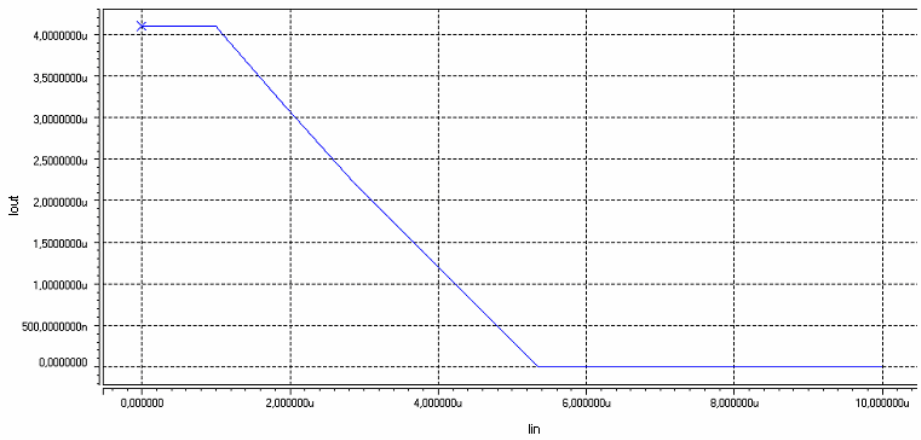

Figure 5.16. H-Spice simulation of the double breakpoint PMOS combinational circuit

5.11. Improved Circuit that Uses Two NMOS Current Mirrors

The last circuit is an improved version of the double break point NMOS current mirror circuits. In this network system is off until the input current passes the value of I_1. Then after, the total current that can be passed over M_1 and M_2 is limited by the current pulled down by the I_2 current source via M_3 drain current. This gives a two breakpoint circuit.

For $I_{IN} = 2\mu A$, $I_1 = 1\mu A$, $I_2 = 2\mu A$ values on Table 5.9 are gained. 2 µA is passing through the second transistor. Calculated errors for this current value are; $1.57 \cdot 10^{-13}$ for *error1,* $1.00 \cdot 10^{-02}$ for *error2*, $3.50 \cdot 10^{-02}$ for *error3*. The total expected error in this circuit is the addition of the error coming from the first current mirror with the error coming from the second current mirror.

For the input range of 0 to 10µA the output characteristic of the circuit is as shown in Figure 5.18. I_1 is set 1µA and I_2 is set to 10µA while transistors aspect ratios are "1". Graph is deviates from the expected values. Output is expected to settle on 5µA, but it is not as it can be seen in the Figure 5.18. This problem can be solved by adding a buffer current mirror after the input current source.

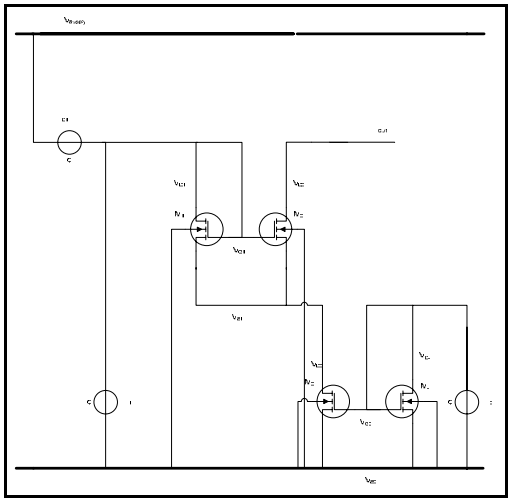

Figure 5.17. Improved circuit that uses two NMOS current mirrors

Table 5.9. Improved circuit that uses two NMOS current mirrors comparison

Values	Calculated (µA)	Simulation (µA)
$I_{out}(V_{d2} = 1.65V)$	1.00	0.97
$I_{out}(C_{OX}$ error)	1.02	0.96
I_{out} (V_t error)	0.92	0.93
I_{out} (all errors)	0.60	0.93

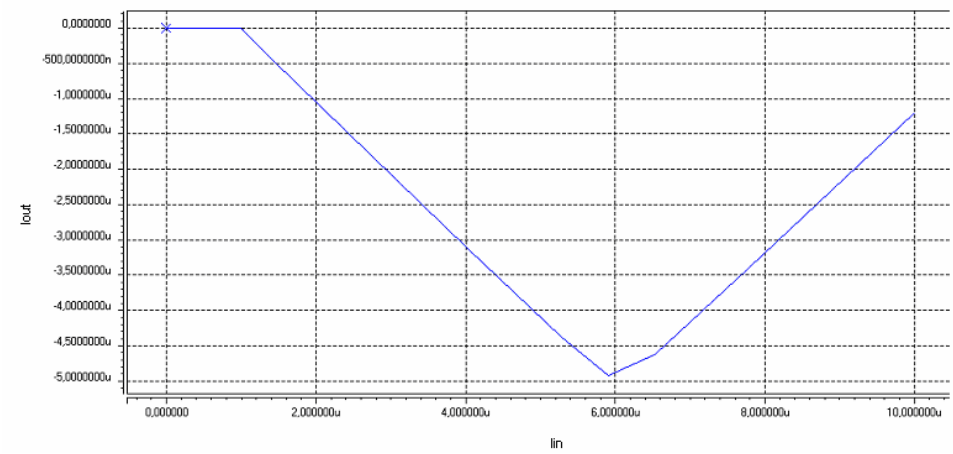

Figure 5.18. Simulation of the improved double breakpoint NMOS circuit

5.12. Improved Circuit That Uses Two PMOS Current Mirrors

The last circuit is an improved version of the double break point PMOS current mirror circuits. In this network system is off until the input current passes the value of I_1. Then after, the total current that can be passed over M_1 and M_2 is limited by the current pulled up by the I_2 current source via M_3 drain current. This gives a two breakpoint circuit.

For $I_{IN} = -2\mu A$, $I_1 = 1\mu A$ and $I_2 = 2\mu A$ values on Table 5.10 are gained.. 2 µA is passing through the second transistor. Calculated errors for this current value are; $8.89 \cdot 10^{-15}$ for *error1,* $1.00 \cdot 10^{-02}$ for *error2*, $2.38 \cdot 10^{-02}$ for *error3*.

The total expected error in this circuit is the addition of the error coming from the first current mirror with the error coming from the second current mirror.

For the input range of 0 to 10µA the output characteristic of the circuit is as shown Figure 5.20. I_1 is set 1µA and I_2 is set to 10µA while transistors aspect ratios are "1". Graph is deviates from the expected values. Output is expected to settle on 5µA, but it is not as it can be seen in the Figure 5.20. This problem can be solved by adding a buffer current mirror after the input current source.

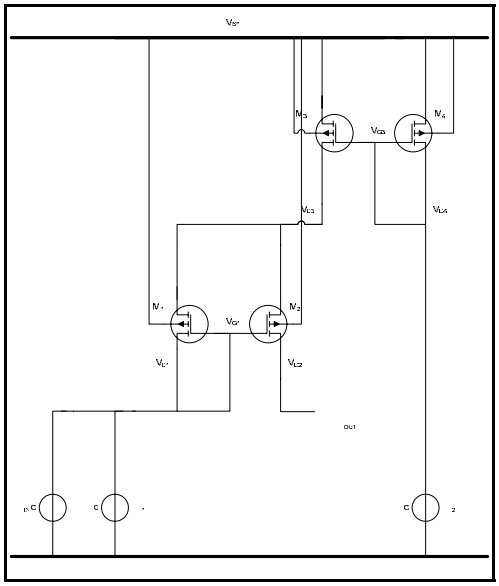

Figure 5.19. Improved circuit that uses two PMOS current mirrors

Table 5.10. Circuit that uses two PMOS current mirrors comparison

Values	Calculated (µA)	Simulation (µA)
$I_{out}(V_{d2} = 1.65V)$	1.05	0.98
$I_{out}(C_{OX}$ error)	1.02	0.99
I_{out} (V_t error)	0.94	0.99
I_{out} (all errors)	0.60	0.99

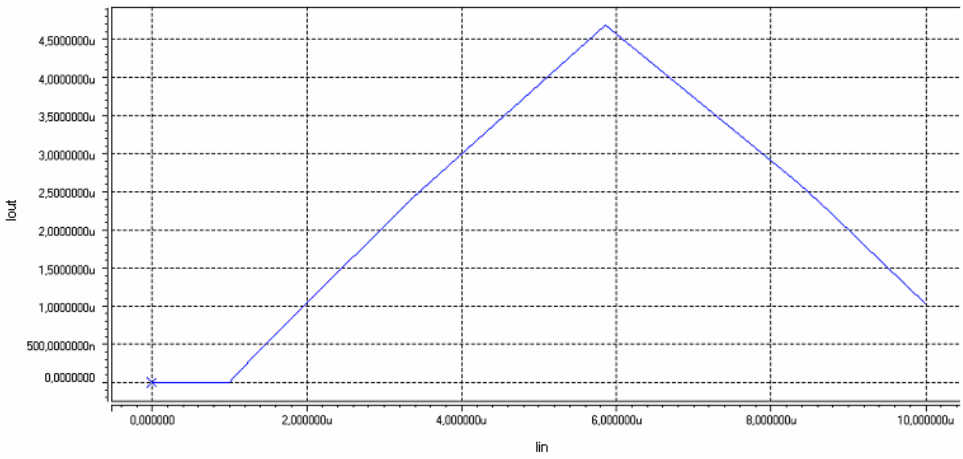

Figure 5.20. Simulation of the improved double breakpoint PMOS circuit

6. APPLICATION

6.1. Sample One Dimensional Circuit Design

A combination of circuits defined in the Chapter 5 is used to approximate a surface. Surface that is planned to be approximated is shown in Figure 6.1. Breakpoint values are converted to actual current values by multiplying them with 10^{-5}. With this breakpoints ouput spice file created by the circuit creation function is shown Figure 6.3.. Breakpoints calculation in Figure 6.2 is going to be used as breakpoints in circuit design.

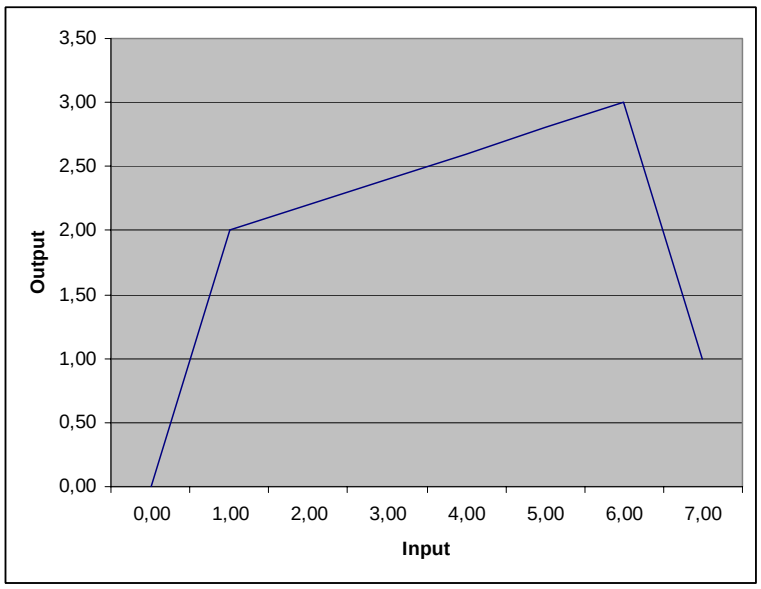

Figure 6.1. Expected solution surface

```
x:0, z:0
x:1, z:2
x:6, z:3
x:7, z:1
```

Figure 6.2. Breakpoints of sample figure

```
*****Sample Circuit Circuit Schemtic*****

.options post
.op
.tran 1ms 20ms
.probe

**********************************************************
***************One Dimensional Circuit***************
**********************************************************

***Voltage Sources***
Vsupply 1 0 3.3
Vout 2 0 1.65

***Current Sources***
Iin 100 0 pulse(0 0.000105 0 20ms 0 1ms 21ms)

Vinv 3 100 0

**Bias Current Source**
IBias 0 4 1e-005


***Transistors***

*Input Transistors (maximum current to be pass: 7e-005) *
M1 3 3 1 1 PMOS l=1e-006 w=2.5e-006

**Bias Transistors  (fix current passing: 1e-005) *
M2 4 4 0 0 NMOS l=1e-006 w=1e-006

**Subcircuit #1: Pull_Up Network**
* Input Transistors (maximum current to be pass: 7e-005) *
M3 5 3 1 1 PMOS l=1e-006 w=2.5e-006
*No Start Break Point Transistor*
* Stop Breakpoint Transistors (current passing: 3e-005, aspect ratio to bias transistor: 3) *
M4 6 4 0 0 NMOS l=1e-006 w=3e-006
* Current Mirror #1*
*(maximum current to be passed: 1e-005) *
M5 5 5 6 0 NMOS l=1e-006 w=1e-006
M6 7 5 6 0 NMOS l=1e-006 w=2e-006
* Current Mirror #2*
*(maximum current to be passed: 2e-005) *
M7 7 7 1 1 PMOS l=1e-006 w=5e-006
M8 2 7 1 1 PMOS l=1e-006 w=5e-006

**Subcircuit #2: Pull_Up Network**
* Input Transistors (maximum current to be pass: 7e-005) *
M9 8 3 1 1 PMOS l=1e-006 w=2.5e-006
* Start Breakpoint Transistors (current passing: 1e-005, aspect ratio to bias transistor: 1) *
M10 8 4 0 0 NMOS l=1e-006 w=1e-006
* Stop Breakpoint Transistors (current passing: 6e-005, aspect ratio to bias transistor: 6) *
M11 9 4 0 0 NMOS l=1e-006 w=6e-006
* Current Mirror #1*
*(maximum current to be passed: 5e-005) *
M12 8 8 9 0 NMOS l=1e-006 w=5e-006
M13 10 8 9 0 NMOS l=1e-006 w=1e-006
* Current Mirror #2*
*(maximum current to be passed: 1e-005) *
M14 10 10 1 1 PMOS l=1e-005 w=2.5e-005
M15 2 10 1 1 PMOS l=1e-005 w=2.5e-005

**Subcircuit #3: Pull_Down Network**
* Input Transistors (maximum current to be pass: 7e-005) *
M16 11 3 1 1 PMOS l=1e-006 w=2.5e-006
* Start Breakpoint Transistors (current passing: 6e-005, aspect ratio to bias transistor: 6) *
M17 11 4 0 0 NMOS l=1e-006 w=6e-006
* Stop Breakpoint Transistors (current passing: 3e-005, aspect ratio to bias transistor: 3) *
M18 12 4 0 0 NMOS l=1e-006 w=3e-006
* Current Mirror #1*
*(maximum current to be passed: 1e-005) *
M19 11 11 12 0 NMOS l=1e-006 w=1e-006
M20 2 11 12 0 NMOS l=1e-006 w=2e-006
```

Figure 6.3. Output of the Circuit Creation algorithm, sample circuit H-Spice file

Circuit schematic of the spice file is shown in Figure 6.4. This schematic is created by the circuit creation algorithm. *W* and *L* values of each transistor are calculated by the *W* & *L* Calculation algorithm. Calculated values can be examined on the spice file in Figure 6.3.

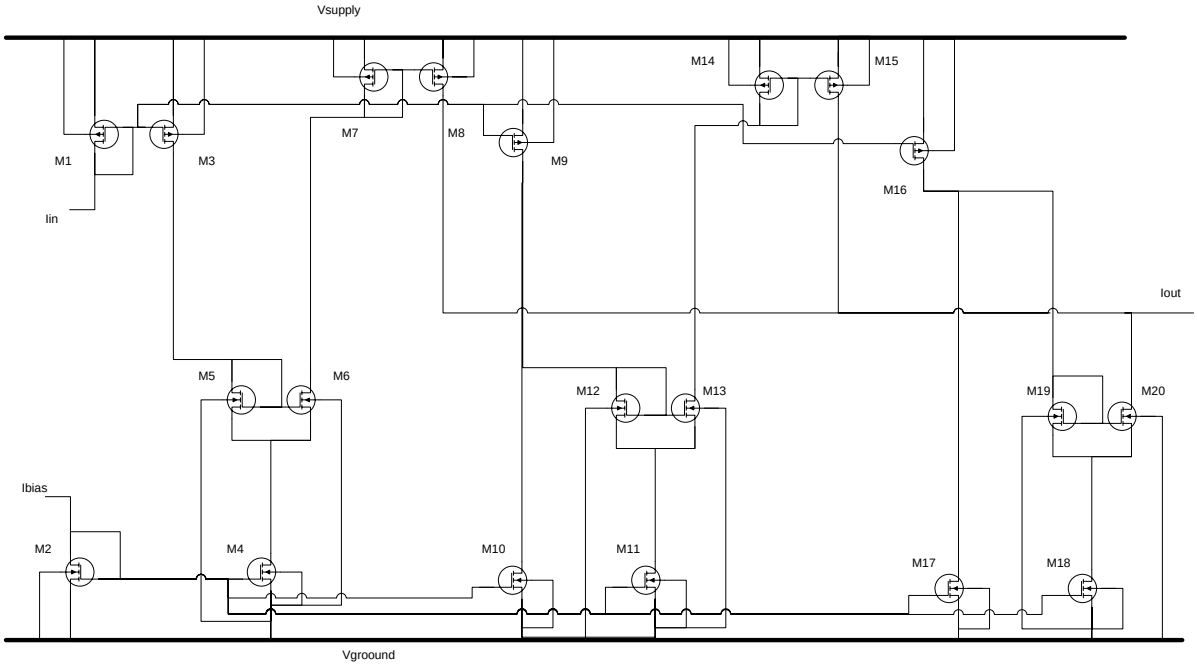

Figure 6.4. Circuit schematic of the sample circuit

Deviation from the expected values is shown on Table 6.1.

Table 6.1. Breakpoints comparison of approximated and expected surface

Breakpoints	x_1	z_1	x_2	z_2	x_3	z_3	x_4	z_4	x_5	z_5
Expected (10^{-5}A)	0.00	0.00	1.00	2.00	6.00	3.00	7.00	1.00	7.00	1.00
Approximated (10^{-5}A)	0.00	0.00	1.09	2.11	6.12	2.98	7.49	1.34	8.13	1.10

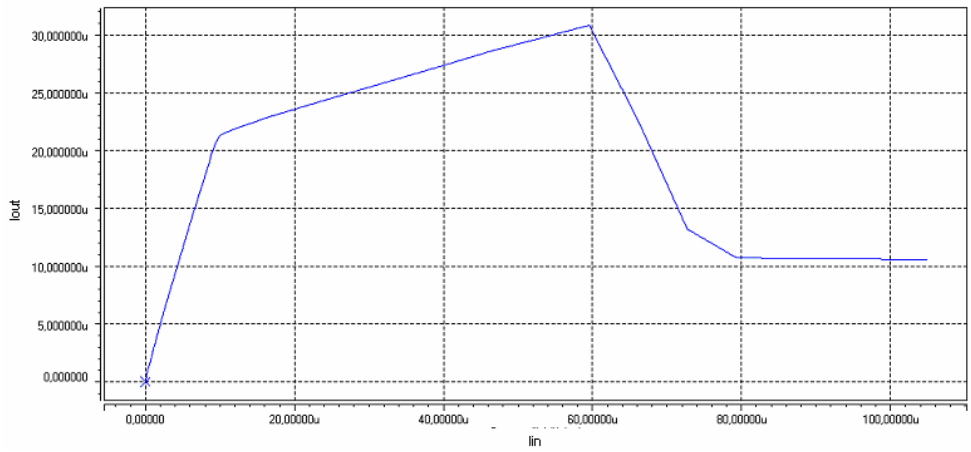

Figure 6.5. H-Spice simulation of the created circuit

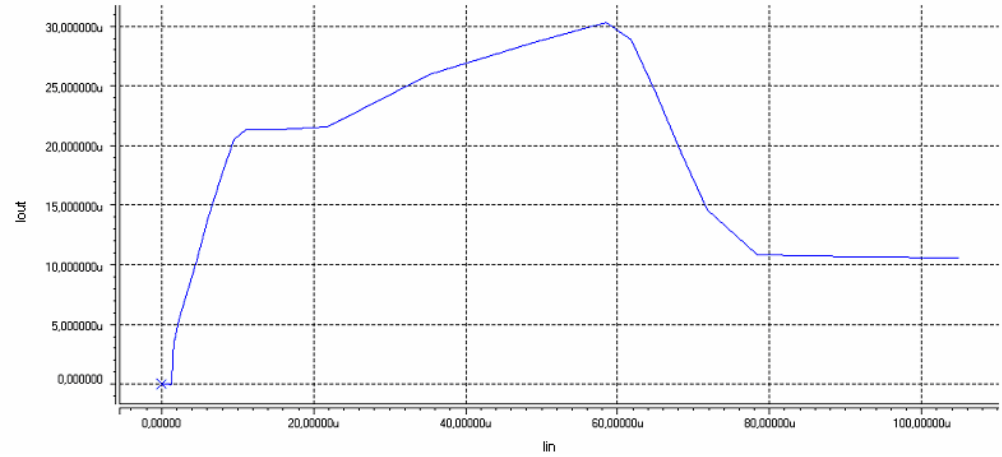

Figure 6.6. H-Spice simulation of the created circuit at 0.5 MHz

As it is adjusted from the transient analysis it is seen that for frequencies larger than 0.5 MHz output looses its proper shape.

6.2. Sample Two Dimensional Circuit

The purpose of this example is to identify the two dimension ability of the program. Breakpoints extracted from a sample circuit are shown in Figure 6.7.

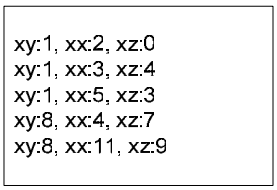

Figure 6.7. Breakpoints of the two dimensional sample circuit

First variable “xy” refers to the second input, “xx” refers to the first input “xz” is the output. H-Spice file for this circuit is shown Figure 6.8.

```
*******************************************************
****************Two Dimensional Circuit****************
*******************************************************
***Voltage Sources***
Vsupply 1 0 3.3V
Vout 2 0 1.65

*************First Input Circuit Schematic*************
*******************************************************
Ibias_1 0 5 1e-005mA


***Transistors***

**input transistor (maximum current to be pass: 0.00022) **
M1 3 3 1 1 PMOS 1e-006 2.5e-006
**bias circuit input transistor (maximum current to be pass: 0.00015) **
M2 4 4 1 1 PMOS 1e-006 2.5e-006
**bias circuit bias transistor (fix current passing: 1e-005) **
M3 5 5 0 0 NMOS 1e-006 1e-006
**bias circuit error transistor (fix current passing: 3u) **
M5 9 9 0 0 NMOS 1e-006 1e-006

*********************************************
**Bias Circuit #1**
*input transistors (maximum current to be pass: 0.00015) *
M6 10 4 1 1 PMOS 1e-006 2.5e-006
M13 13 4 1 1 PMOS 1e-006 2.5e-006
*first start breakpoint transistor (current passing: 1e-005, aspect ratio to bias transistor: 1) *
M7 10 5 0 0 NMOS 1e-006 1e-006
*first stop breakpoint transistor (current passing: 2.7e-005, aspect ratio to bias transistor: 2.7) *
M8 11 5 0 0 NMOS 1e-006 2.7e-006
*second start breakpoint transistor (current passing: 8e-005, aspect ratio to bias transistor: 8) *
M14 13 5 0 0 NMOS 1e-006 8e-006
*second stop breakpoint transistor (current passing: 2.7e-005, aspect ratio to bias transistor: 2.7) *
M15 14 5 0 0 NMOS 1e-006 2.7e-006
*function1 transistors (maximum current to be passed: 7e-006) *
M9 10 10 11 0 NMOS 1e-006 1e-006
*(maximum current to be passed: 2e-005) *
M10 12 10 11 0 NMOS 1e-006 2.85714e-006
*function1 pull_up transistors (maximum current to be passed: 2e-005) *
M11 12 12 1 1 PMOS 1e-006 7.14286e-006
M12 15 12 1 1 PMOS 1e-006 7.14286e-006
*functio2 transistor (maximum current to be passed: 7e-006) *
M16 13 13 14 0 NMOS 1e-006 1e-006
*function2 transistor (maximum current to be passed: 2e-005) *
M17 16 13 14 0 NMOS 1e-006 2.85714e-006
*buffer pull_up transistors (maximum current to be passed: 2e-005) *
M18 16 16 1 1 PMOS 1e-006 7.14286e-006
M19 17 16 1 1 PMOS 1e-006 7.14286e-006
*buffer pull_down transistors (maximum current to be passed: 2e-005) *
M20 17 17 0 0 NMOS 1e-006 2.85714e-006
M21 15 17 0 0 NMOS 1e-006 2.85714e-006
*error transistor (maximum current to be passed: 3u) *
M22 15 9 0 0 NMOS 1e-006 1e-006
*bias transistor for first input circuit (current paassing: 2e-005)*
M23 15 15 0 0 NMOS 1e-006 1e-006
```

Figure 6.8. H-Spice file ouput of the design

```
*Input Circuit #1*
*input transistor (maximum current to be pass: 0.00022) *
M24 18 3 1 1 PMOS 1e-006 2.5e-006
*start breakpoint transistor (current passing: 2e-005, aspect ratio to bias transistor: 1) *
M25 18 15 0 0 NMOS 1e-006 1e-006
*stop breakpoint transistor (current passing: 5e-005, aspect ratio to bias transistor: 2.5) *
M26 19 15 0 0 NMOS 1e-006 2.5e-006
*function1 transistors (maximum current to be passed: 1e-005) *
M27 18 18 19 0 NMOS 1e-006 1e-006
*(maximum current to be passed: 4e-005) *
M28 20 18 19 0 NMOS 1e-006 4e-006
*function2 transistors, pull_up transistors*
*(maximum current to be passed: 4e-005) *
M29 20 20 1 1 PMOS 1e-006 1e-005
M30 2 20 1 1 PMOS 1e-006 1e-005

*Input Circuit #2*
*input transistor (maximum current to be pass: 0.00022) *
M31 21 3 1 1 PMOS 1e-006 2.5e-006
*start breakpoint transistor (current passing: 3e-005, aspect ratio to bias transistor: 1.5) *
M32 21 15 0 0 NMOS 1e-006 1.5e-006
*stop breakpoint transistor (current passing: 3e-005, aspect ratio to bias transistor: 1.5) *
M33 22 15 0 0 NMOS 1e-006 1.5e-006
*function1 transistors (maximum current to be passed: 2e-005) *
M34 21 21 22 0 NMOS 1e-006 2e-006
*pull_down transistor (maximum current to be passed: 1e-005) *
M35 23 21 22 0 NMOS 1e-006 1e-006
*buffer pull_up transistors (maximum current to be passed: 1e-005) *
M36 23 23 1 1 PMOS 1e-006 2.5e-006
M37 24 23 1 1 PMOS 1e-006 2.5e-006
*buffer pull_down transistors (maximum current to be passed: 1e-005) *
M38 24 24 0 0 NMOS 1e-006 1e-006
M39 2 24 0 0 NMOS 1e-006 1e-006

*********************************************
**Bias Circuit #2**
*input transistors (maximum current to be pass: 0.00015) *
M40 25 4 1 1 PMOS 1e-006 2.5e-006
M47 28 4 1 1 PMOS 1e-006 2.5e-006
*first start breakpoint transistor (current passing: 8e-005, aspect ratio to bias transistor: 8) *
M41 25 5 0 0 NMOS 1e-006 8e-006
*first stop breakpoint transistor (current passing: 2.7e-005, aspect ratio to bias transistor: 2.7) *
M42 26 5 0 0 NMOS 1e-006 2.7e-006
*second start breakpoint transistor (current passing: 0.00015, aspect ratio to bias transistor: 15) *
M48 28 5 0 0 NMOS 1e-006 1.5e-005
*second stop breakpoint transistor (current passing: 2.7e-005, aspect ratio to bias transistor: 2.7) *
M49 29 5 0 0 NMOS 1e-006 2.7e-006
*function1 transistors (maximum current to be passed: 7e-006) *
M43 25 25 26 0 NMOS 1e-006 1e-006
*(maximum current to be passed: 2e-005) *
M44 27 25 26 0 NMOS 1e-006 2.85714e-006
*function1 pull_up transistors (maximum current to be passed: 2e-005) *
M45 27 27 1 1 PMOS 1e-006 7.14286e-006
M46 30 27 1 1 PMOS 1e-006 7.14286e-006
*functic2 transistor (maximum current to be passed: 7e-006) *
M50 28 28 29 0 NMOS 1e-006 1e-006
*function2 transistor (maximum current to be passed: 2e-005) *
M51 31 28 29 0 NMOS 1e-006 2.85714e-006
*buffer pull_up transistors (maximum current to be passed: 2e-005) *
M52 31 31 1 1 PMOS 1e-006 7.14286e-006
M53 32 31 1 1 PMOS 1e-006 7.14286e-006
*buffer pull_down transistors (maximum current to be passed: 2e-005) *
M54 32 32 0 0 NMOS 1e-006 2.85714e-006
M55 30 32 0 0 NMOS 1e-006 2.85714e-006
*error transistor (maximum current to be passed: 3u) *
M56 30 9 0 0 NMOS 1e-006 1e-006
*bias transistor for first input circuit (current paassing: 2e-005)*
M57 30 30 0 0 NMOS 1e-006 1e-006

*Input Circuit #1*
*input transistor (maximum current to be pass: 0.00022) *
M58 33 3 1 1 PMOS 1e-006 2.5e-006
*start breakpoint transistor (current passing: 4e-005, aspect ratio to bias transistor: 2) *
M59 33 30 0 0 NMOS 1e-006 2e-006
*stop breakpoint transistor (current passing: 9e-005, aspect ratio to bias transistor: 4.5) *
M60 34 30 0 0 NMOS 1e-006 4.5e-006
*function1 transistors (maximum current to be passed: 7e-005) *
M61 33 33 34 0 NMOS 1e-006 3.5e-006
*(maximum current to be passed: 2e-005) *
M62 35 33 34 0 NMOS 1e-006 1e-006
*function2 transistors, pull_up transistors*
*(maximum current to be passed: 2e-005) *
M63 35 35 1 1 PMOS 1e-006 2.5e-006
M64 2 35 1 1 PMOS 1e-006 2.5e-006
*offset transistor (current pulled up: 7e-005, aspect ratio to bias transistor of the input stage: 3.5) *
M65 36 30 0 0 NMOS 1e-006 3.5e-006
M66 36 36 1 1 PMOS 1e-006 8.75e-006
M67 2 36 1 1 PMOS 1e-006 8.75e-006
```

Figure 6.8. (Cont.) H-Spice file ouput of the design

One dimensional output is shown in Figure 6.9.

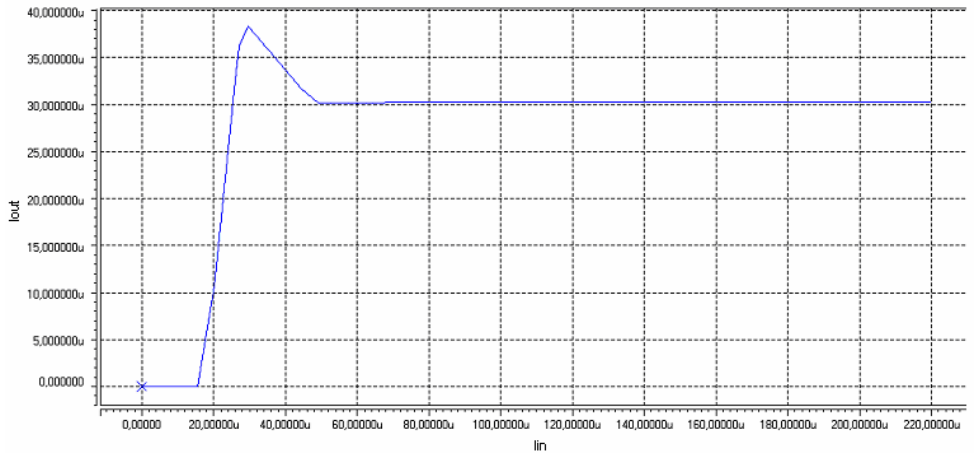

Figure 6.9. Sample two dimensional circuit output for 1μA ≤ y ≤8μA

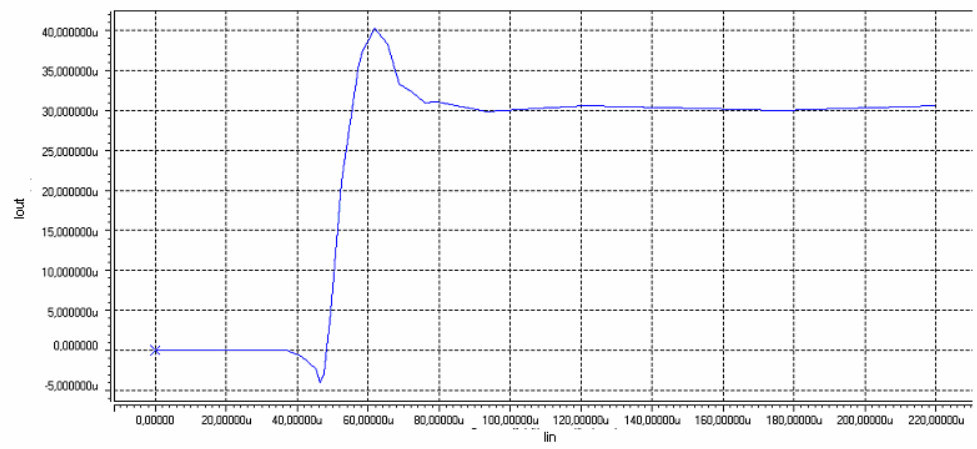

Figure 6.10. Sample two dimensional circuit output for 1μA ≤ y ≤8μA at 50MHz

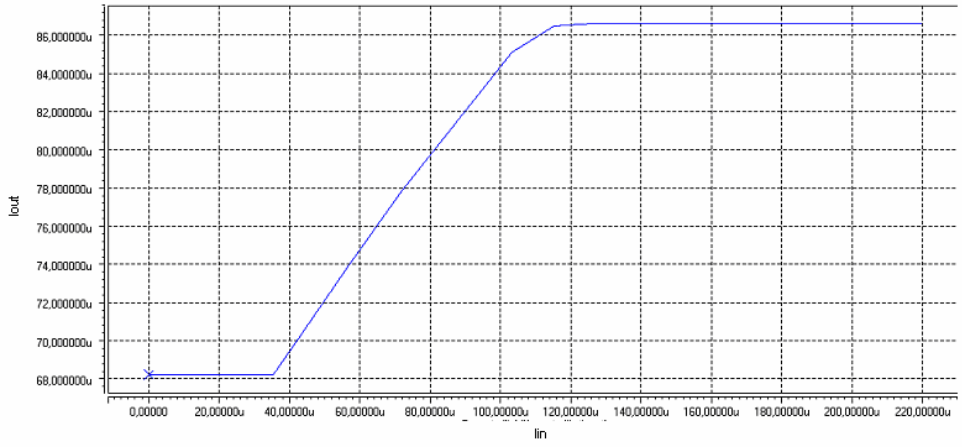

Figure 6.11. Sample two dimensional circuit output for 8μA ≤ y ≤ 15μA

This is the surface of first input while second input is between “8µA” and “15µA”. Output will be set to “0” outside the range of 1µA -15µA. Figure 6.12 it is shown that after 50MHz signal in Figure 6.11 looses its proper shape.

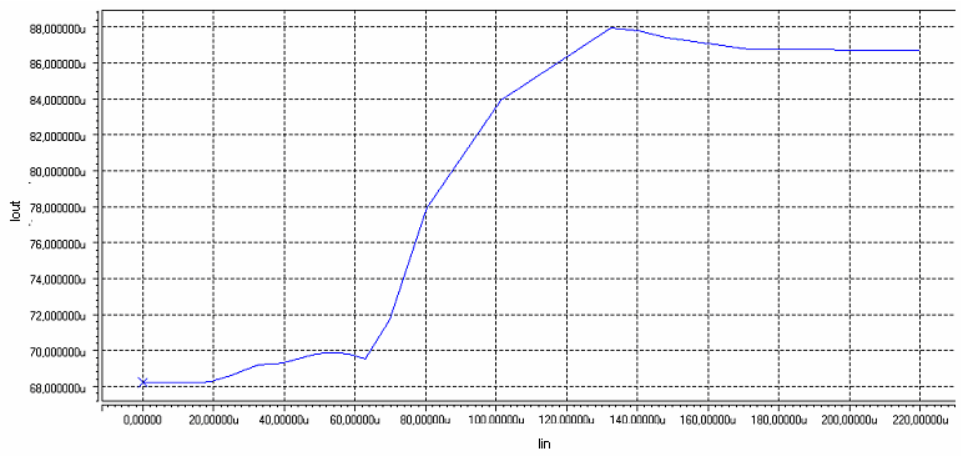

Figure 6.12. Sample two dimensional circuit output for 8µA ≤ y ≤ 15µA at 50MHz

Two dimensional output of the above design is shown in Figure 6.13:

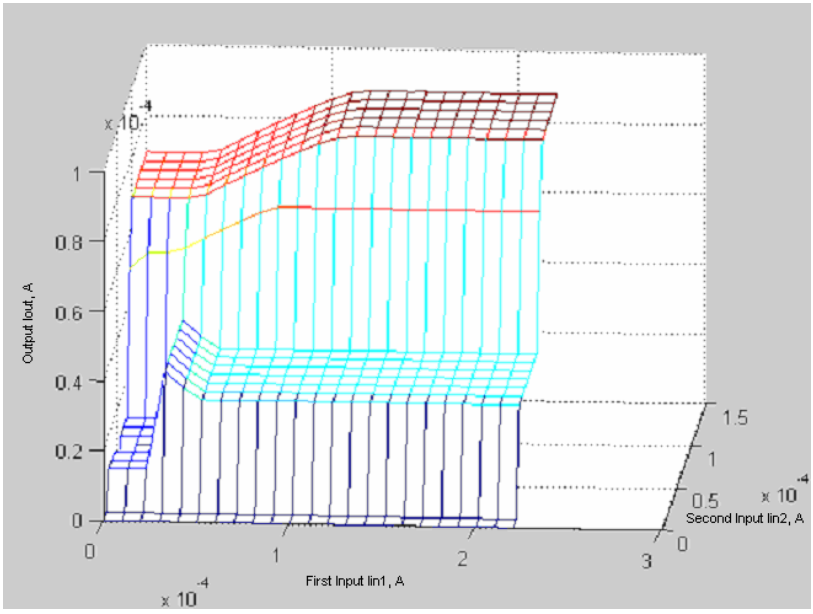

Figure 6.13. Sample two dimensional circuit two dimensional output graph-1

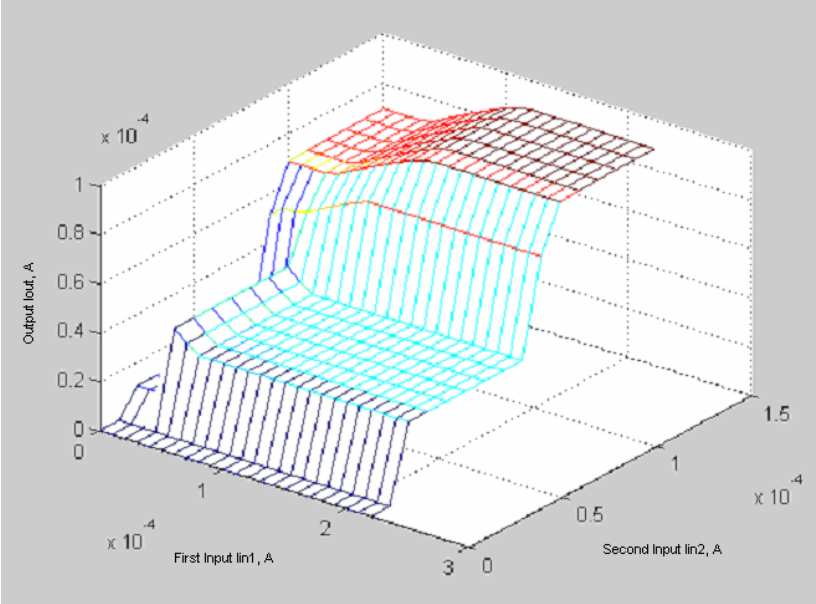

Figure 6.14. Sample two dimensional circuit two dimensional output graph-2

As it can easily be seen from the above graphs algorithm's H-Spice output is perfectly matching with the expected surface.

6.3. Fuzzy Logic Applications

In this work one of the two dimensional fuzzy logic demos implemented in MATLAB R2006a is selected as the application field. Following design will be constructed on the "Modeling Inverse Kinematics in a Robotic Arm" application. Kinematics is the science of motion. In a two-joint robotic arm, given the angles of the joints, the kinematics equations give the location of the tip of the arm. Inverse kinematics refers to the reverse process. Given a desired location for the tip of the robotic arm, what should the angles of the joints be so as to locate the tip of the arm at the desired location.

Since the scope of this work is not "Inverse Kinematics", it is not going to be explained in this work. For more information on this topic, MATLAB demo file will be a good start point.

Surface that is going to be approximated in Modeling Inverse Kinematics in a Robotic Arm is shown in Figure 6.15.

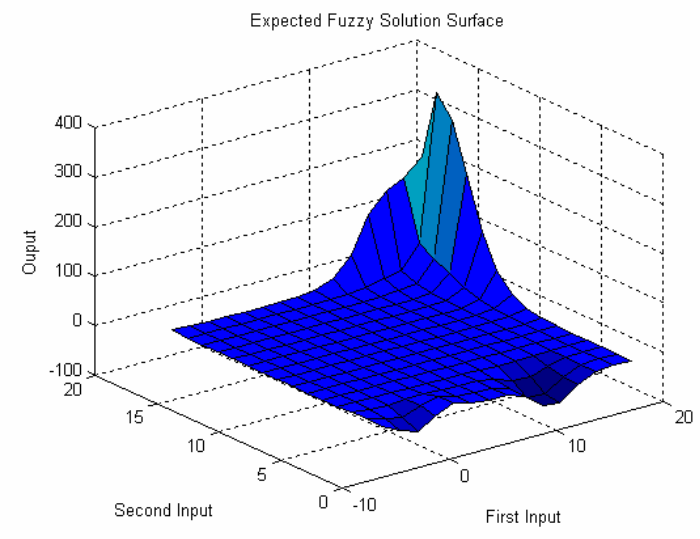

Figure 6.15. Fuzzy Solution Surface

6.3.1. One Dimensional Fuzzy Solution Surface Realization

The process of two dimensional surface approximations is the same as the process defined in the one dimensional mode. The only difference is, second input is not defined to be fixed in this case. Solution surface defined in Figure 6.5 is the expected surface. Reconstructed surface created by the breakpoints calculated is shown in Figure 6.16. This circuit is normalized and the final output surface is shown in Figure 6.17**.**

Approximation error is defined to be 18% which is quit a small amount for fuzzy calculations.

With the breakpoints calculated the remaining error for *W* and *L* calculations, will be the inputs of the circuit creation algorithm. In creation of two dimensional circuits, there are two parts for each input case. If the one dimension sample mentioned in Section 7.1 is considered to be the input case for a constant value of second input, this input case will be considered as same for all values between the arbitrary two values of second input. Second

input will be considered as the bias current of input sequence for that specific input case and input case will be continues between two arbitrary second input values by pulling down the bias current off and consequently output of the input case to zero beyond the range. Bias circuit which feeds the circuit up to the second input sequence is shown in Figure 6.19.

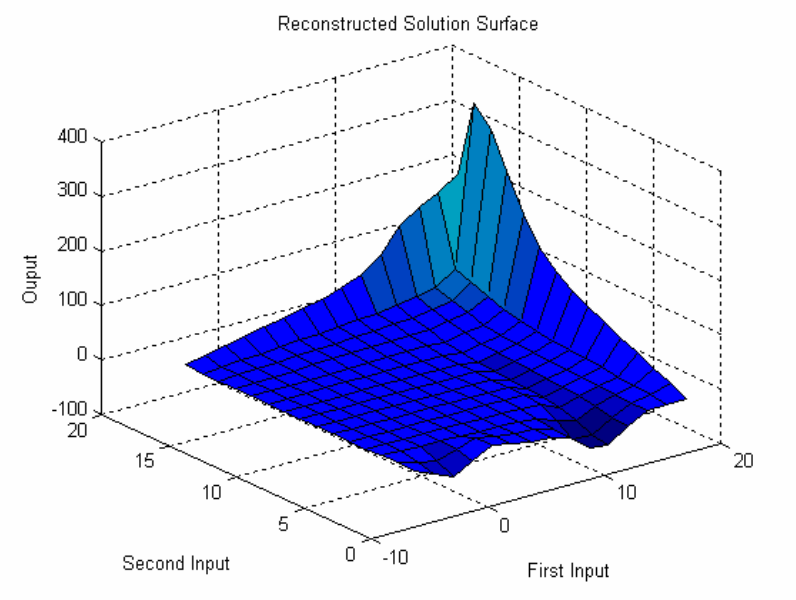

Figure 6.16. Reconstructed two dimensional fuzzy solution surface

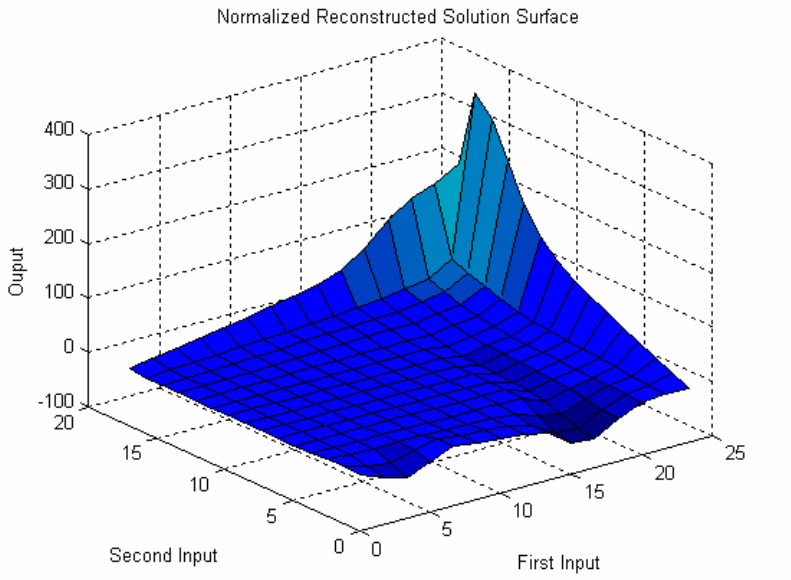

Figure 6.17. Normalized reconstructed two dimensional fuzzy solution surface

```
***Voltage Sources***
Vsupply 1 0 3.3V
Vout 14 0 1.65

***Current Sources***
*Iinput1 7 C PULSE(0 C.00012 0 2Cms 0 1ms 21ms)
Iinput2 8 0 PULSE(0 1Ce-005 0 20ms 0 1ms 21ms)
Vcontrolsecondinput 4 8 C

*************First Input Circuit Schematic*************
*****************************************************
Ibias_1 0 5 1e-005mA


***Transistors***

**bias circuit input transistor (maximum current to be pass: 3e-005) **
M2 4 4 1 1 PMOS 1e-006 2.5e-006
**bias circuit bias transistor (fix current passing: 1e-005) **
M3 5 5 0 C NMOS 1e-006 1e-006

*********************************************
**Bias Circuit #1**
*input transistors (maximum current to be pass: 3e-005) *
M5 9 4 1 1 PMOS 1e-006 2.5e-006
M12 12 4 1 1 PMOS 1e-006 2.5e-006
*first start breakpoint transistor (current passing: 1e-005, aspect ratio to bias transistor: 1) *
M6 9 5 0 0 NMOS 1e-006 1e-006
*first stop breakpoint transistor (current passing: 2.1e-005, aspect ratio to bias transistor: 2.1) *
M7 10 5 0 C NMOS 1e-006 2.1e-006
*second start breakpoint transistor (current passing: 2e-005, aspect ratio to bias transistor: 2) *
M13 12 5 0 C NMOS 1e-006 2e-006
*second stop breakpoint transistor (current passing: 2.1e-005, aspect ratio to bias transistor: 2.1) *
M14 13 5 0 C NMOS 1e-006 2.1e-006
*function1 transistors (maximum current to be passed: 1e-006) *
M8 9 9 10 C NMOS 1e-006 1e-006
*(maximum current to be passed: 2e-005) *
M9 11 9 10 C NMOS 1e-006 2e-005
*function1 pull_up transistors (maximum current to be passed: 2e-005) *
M10 11 11 1 1 PMOS 1e-006 5e-005
M11 14 11 1 1 PMOS 1e-006 5e-005
*functic2 transistor (maximum current to be passed: 1e-006) *
M15 12 12 13 C NMOS 1e-006 1e-006
*function2 transistor (maximum current to be passed: 2e-005) *
M16 15 12 13 C NMOS 1e-006 2e-005
*function2 pull_up transistors (maximum current to be passed: 2e-005) *
M17 15 15 1 1 PMOS 1e-006 5e-005
M18 16 15 1 1 PMOS 1e-006 5e-005
*function2 pull_down transistors (maximum current to be passed: 2e-005) *
M19 16 16 0 C NMOS 1e-006 2e-005
M20 14 16 0 0 NMOS 1e-006 2e-005
```

Figure 6.18. H-Spice file of the sample bias circuit

To give an idea, the H-Spice output for the bias circuit shown in Figure 6.18 is shown in the Figure 6.20.

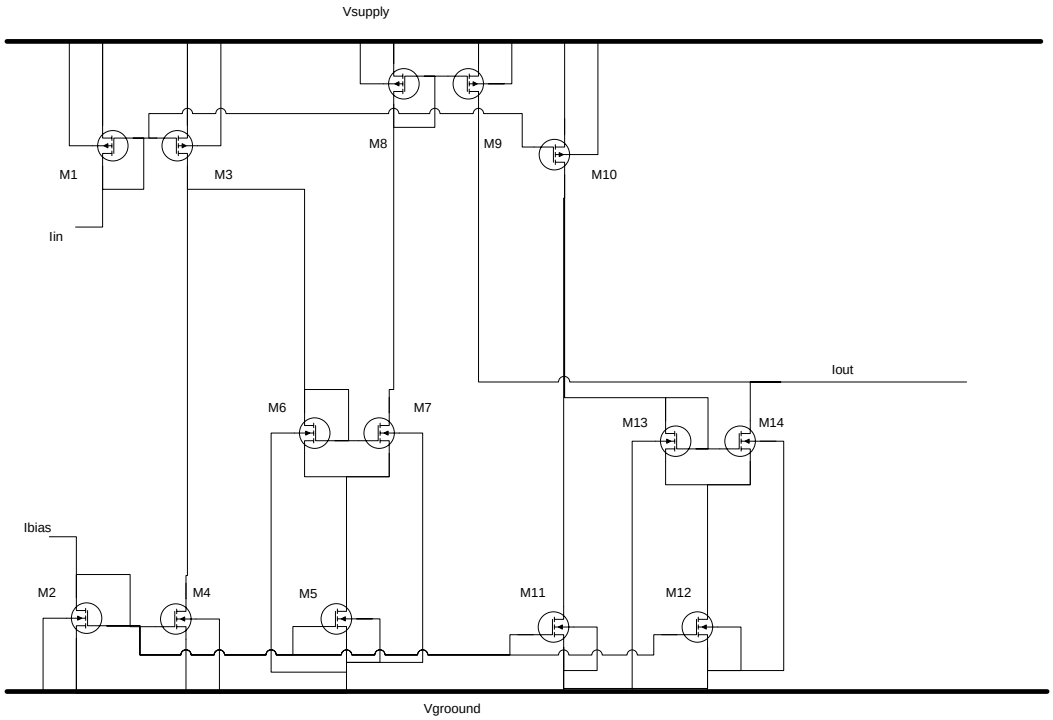

Figure 6.19. Bias circuit schematic for two dimensional fuzzy surface function

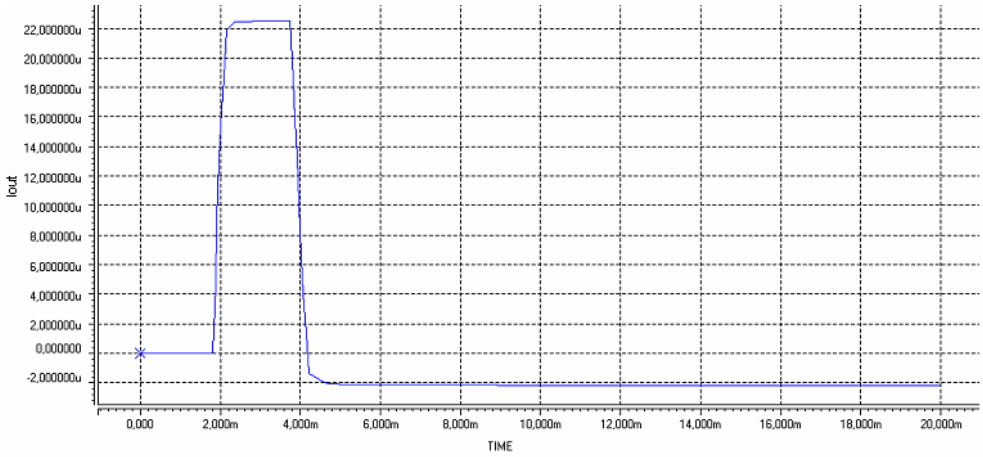

Figure 6.20. H-Spice output of the sample bias circuit

While the output value is “0” and less than zero input circuit will not work.

Output of this circuit will be the input of bias current of input circuits such as the bias current of the circuit mentioned in Figure 6.4.

The H-Spice output of the circuit created by circuit creation algorithm is shown in Figure 6.23.

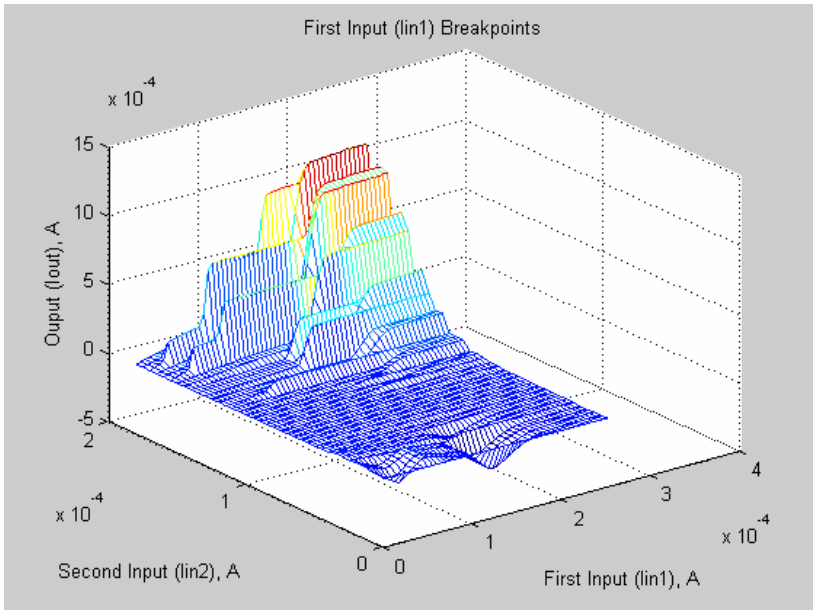

Figure 6.21. Surface drawn by the first input breakpoints

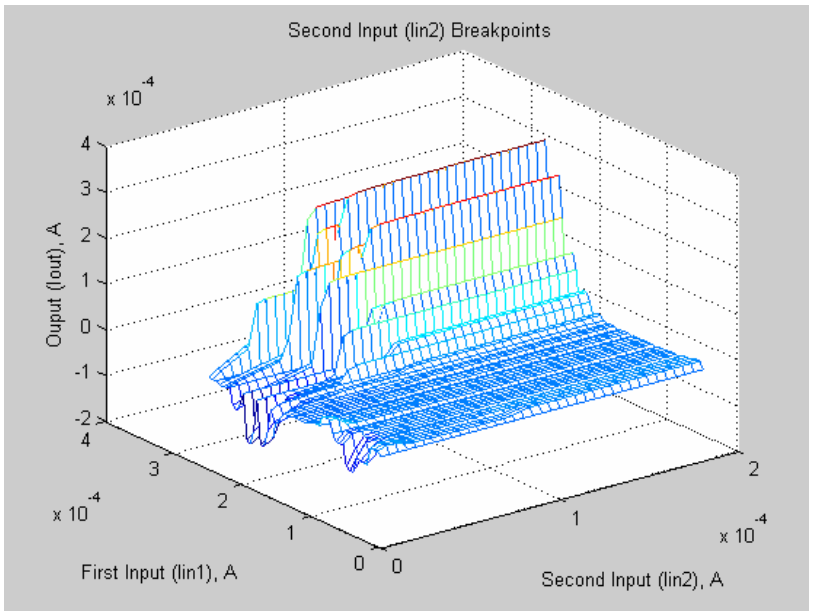

Figure 6.22. Surface drawn by the second input breakpoints

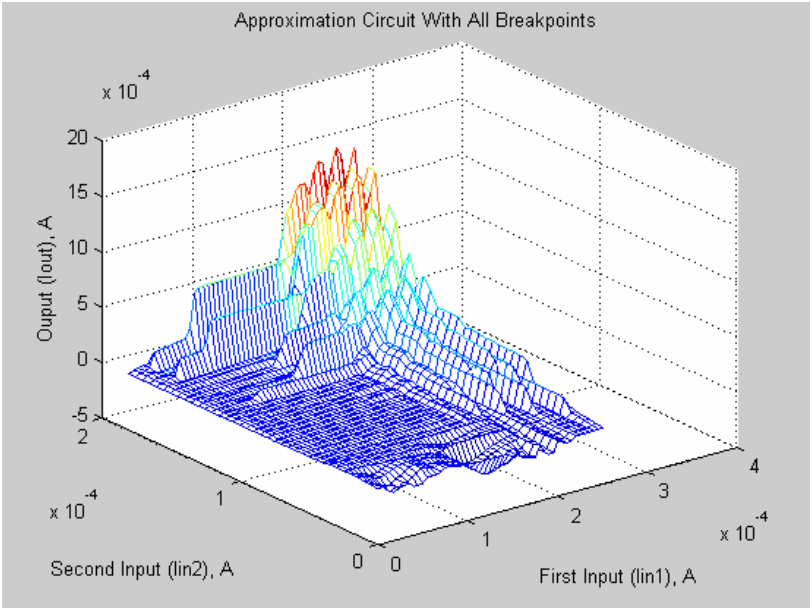

Figure 6.23. Fuzzy solution created by the Circuit Creation algorithm

7. CONCLUSIONS

A design automation tool which is used to increase the design speed with an acceptable accuracy is defined with in this work. Performance specifications and constraints coming from the designer and with the assumptions coming from the model used in this design tool to make accurate calculation suitable for the purpose of the design.

Entire work consists of different levels of approximation and design. First of all a given solution surface is approximated with possible minimum breakpoints with in a range of approximation accuracy. Then these breakpoints are used to design a circuit, whose blocks are made up of current mirrors, to create the proper shape of the input surface. And finally current mirror transistors' parameters are optimized while keeping the mismatch errors with in a defined error range. The main purpose is to satisfy the DC operating points. Some analyses are also made on the bandwidth of the outputs, just to given an idea to the designer.

Analog blocks defined in this work are combination of current mirrors, which are main blocks of PWL circuits used in fuzzy logic circuits. These blocks are modeled by analytic EKV models. The design tool, based on this background, is tested on several circuits and results are listed in the work with comparison to the spice simulation results. Results are so convincing that they are more or less close to simulation results.

The method proposed in this work is not specific to application field. Therefore, it can be used to approximate any kind of surface. Fuzzy solution approximation examined in this work is used just to give an idea. The core of the circuit design mentioned in the thesis is PWL circuits and these circuits are used in designing fuzzy solutions. This is also another reason why a fuzzy application is preferred as an example.

The future work will process in several directions. One direction will be the usage of this method in other blocks rather than current mirrors. Second direction is to take in to

consideration the gain bandwidth performance criteria in design of PWL circuits. And another possible direction is the integration of the tool defined in this work to other design tools to introduce a complete solution for fuzzy logics. This work introduces solution for two dimensional surfaces to show that n-dimensional solutions are possible. Converting this solution for n-dimensional surfaces may be another future work if there is a demand.

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