VLSI IMPLEMENTATION OF A SECURE COMMUNICATION SYSTEM USING CURRENT-MODE CHAOTIC CIRCUITS

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by

Sedat Nişancı

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T.C. YÜKSE
DOKÜM

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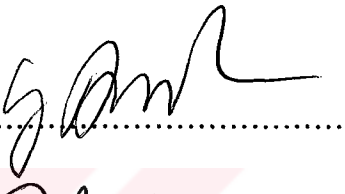
APPROVED BY:

Assoc. Prof. Günhan Dündar ..... 
(Thesis supervisor)

Assoc. Prof. Yağmur Denizhan ..... 

Assoc. Prof. Levent Akın .....

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ABSTRACT

Analogue IC(Integrated Circuit) design is historically seen as a voltage dominated form of signal processing. In fact, the analogue devices that are often used (e.g. transistors) are current output devices, so we can utilize them up to their limits in bandwidth which is one of the important issues in analogue circuits.

Current mode design has recently started appearing in the literature. The advantages are very important in IC design. The most important issues are low power consumption and less space which are the key considerations in VLSI(Very Large Scale Integration). Because of working with quite low currents the power consumption is impressively low. Low current also means small W/L ratios so that less space is needed.

Security is obtained by chaotic behavior of circuits that the communication is based on synchronizing two chaotic circuits. Such a system brings security to analog communication like a scramble type processing. The VLSI implementation can make this type of communication systems smaller. The advantages and design parameters of current mode circuits will be examined with the basic building blocks and it will be applied on a chaotic current mode communication system. This means that even portable devices for analog communication like pocket phones can be possible in the marketplace.

ÖZET

Analog devre tasarımında genelde gerilim domeni işaret işleme yöntemleri kullanılmıştır. Ancak analog devrelerde sıkça kullanılan tranzistör benzeri elemanlar aslında akım çıkışlı elemanlardır ve bunları akım modunda kullandığımızda, analog devreler için önemli olan bant genişliğini verimli bir şekilde kullanabilmekteyiz.

Ayrıca tümleşik devre tasarımında dikkate alınan temel unsur olan güç harcama ve yer açısından akım modu büyük avantajlar getirmektedir. Düşük akımlarla işaret işleme olanağı olduğu için güç harcama da o ölçüde az olacaktır. Az akım gerektirmesi daha küçük W/L oranı yani daha az yer demektir.

Güvenlik, devrelerin kaotik darvanıslarıyla elde edilmektedir ve haberleşme kaotik davranan iki devrenin birbiri ile senkronize olmasi ile gerçeklenmektedir. Kaotik haberleşme işaretin karıştırılarak anlaşılmamasına benzer bir tarzda güvenlik sağlamaktadır. Bu tarz bir sistemin VLSI tasarımı olarak gerçeklenmesi, akım ya da voltaj modunda benzer haberleşme sistemlerinin daha ufak gerçeklenebilirliği sonucunu getirmektedir. Akım modunda çalışan devrelerin avantajları ve tasarımda dikkat edilmesi gereken parametreler temel bloklar anlatılırken incelenecek ve kaotik akım modu haberleşme sisteminde örneklendirilecektir. Bu sayede taşınabilir analog haberleşme cihazları örneğin cep telefonu mümkün olabilecektir.

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LIST OF SYMBOLS

b	Third constant for Lorenz equations
C_{ox}	Gate oxide capacitance per unit area
DELL	Length reduction of source drain diffusion(SPICE parameter)
g_m	Small signal transconductance of MOS transistor
L	The channel length of the MOS transistor
L_D	Lateral diffusion
r	Second constant for Lorenz equations
V_{FB}	Flat-Band voltage of the MOS transistor
V_{SB}	Voltage difference of source terminal and substrate (Body effect)
V_T	MOS threshold voltage
W	The channel width of MOS transistor
γ	Body effect parameter
δ	Width effect on threshold voltage
λ	Channel Length modulation parameter
μ	Mobility of charge carriers
σ	First constant for Lorenz equations
Φ_F	Surface inversion potential

1. INTRODUCTION

A new design approach to implement analog circuits has appeared in the literature since the last 10 years: Current mode [1,2,3]. In this method the input and output signals are currents instead of voltage. It is easy to design circuits that are working in current mode because when considering the current to implement the circuits some basic functions are easily implemented, e.g. summing and subtracting. Also, the current flows through a path. This is a similar case to that of dataflow design in digital technology.

The two significant advantages are power and area. These two items are the most important constraints in VLSI design. Because currents as low as μA or nA can be obtained, it is easy to design circuits consuming low power. Small currents let us implement MOS transistors even in minimum size so that less area is consumed. Also, the frequency response of current mode circuits is much better than voltage mode circuits because the transfer function of a current mode circuit has a pole and also a zero very close to the pole.

The traditional design considerations may not always work because designers are used to dealing with the problem with voltage mode approach. Because of this, the design methodology for a current mode circuit will be stated and wherever possible the differences and advantages from voltage mode will be mentioned. Although the design style is different, it does not bring much complexity, it can even be argued that current mode is more easily designed than voltage mode circuits.

The current mode approach brings advantages to analogue IC design. It is introduced as a design concept for analogue circuits but it will clearly be seen that it can be extended to digital circuitry and this point of view will be stated as one of the future works of this thesis.

Using current as a direct output can bring some problems. The loading conditions are more effective than voltage mode circuits so this is the most important subject in current mode circuits to be concentrated on and also related to this, the measurement of currents is difficult. The interface to the current mode circuits will also be mentioned.

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Voltage mode IC's are usually modeled by a transfer function with a pole, instead the current mode circuits generally have a transfer function with a pole and also a zero which is very close to the pole. This makes the current mode circuits to have better frequency responses. Transistors are used in voltage mode circuits but they are current output devices. Wide bandwidth is the key performance feature of current mode circuits where the transistors can be used up to its maximum operating frequencies. In this thesis, frequency response of current mode circuits will be mentioned.

The communication in a secure media is a big problem in analogue domain. The chaotic behavior of the signals brings security to such communication systems. In this system two identical chaotic circuit is synchronized to each other to achieve communication with a signal from transmitter with a message added on it. In this work a secure communication system based on chaotic behavior is implemented as an integrated circuit working in current mode. This system consumes low power and less chip area.

The flow of the thesis will be as follows. First an introduction to current mode circuits will be made and then basic building blocks will be presented and implementation will be shown. Then, some of these basic building blocks will be used in the project for the realization of a chaotic communication system in current mode [4]. The basic blocks that will be used in the project are multiplier, filter and integrator. These blocks will be used to realize the state equations of chaotic transmitter and receiver system. Each of the blocks will be designed first and then the chaotic system will be constructed. In this project the circuit will be implemented as a VLSI circuit in coordination with Europractice. The technology will be Alcatel Mietec 0.7 μm CMOS technology. We are using Mentor Graphics ICstation tool and Hspice program.

At last, the obtained results of the project will be stated and the advantages of current mode circuits and some applications will be mentioned again. recently

2. CURRENT MODE CIRCUITS

In analogue IC design a new design approach is appearing in the literature recently. Since this method is not well-known, the concept -what is current mode, how can we design a current mode circuit, what is its advantages- will first be described in this chapter.

2.1. Translinear Viewpoint to Current Mode Circuits

In 1975 classification of the circuits is proposed [5] for a specific purpose to realize such circuits –that consist of BJTs- based on the fact that "the transconductance of a BJT is linearly proportional to its collector current, hence the term trans-linear" [1].

In these type of circuits the voltage is not considered to design or to analyze the circuits which are constructed with the BJTs, whose function depends on primarily currents as signals or function variables. This type of circuits is called current mode circuits recently.

This principle will be briefly stated in this section because it is based on the BJTs pn junctions –between base and collector or base and emitter- in one or more closed loops. In this thesis our work is to realize the circuits in CMOS technology.

The translinear principle is stated as "In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise-facing and counterclockwise-facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction" [1].

2.2. Current Mode Concept

In the current mode design approach, the transfer function is a function of input and output currents of the circuit. Since the circuit processes the current. The current mode system is shown in Figure 2.1. If the input and output signals are in terms of voltage, it is needed to convert the voltage to current at the input and the current to voltage at the output. It is seen that if the input from real world is current and the output is current (e.g. signal to loudspeaker), the transconductor and transresistor is not needed. But to maintain compatibility to voltage mode circuits a current mode IC must be considered like this.

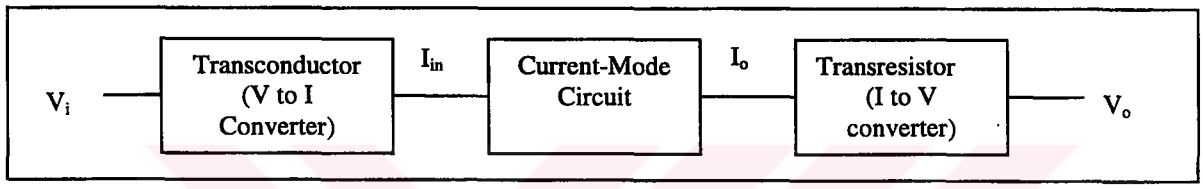

FIGURE 2.1 Current Mode System

In this thesis the IC is designed for voice band and we can convert human sound to current by microphones so we do not need the transconductor and transresistor blocks for our design, although such circuits will be briefly described in the following chapters.

The current mode concept will be clearly understood while the differences from the voltage mode are given. In the following section the advantages of current mode circuits will be stated and it shows us that the design concept is mostly preferred because of those issues.

2.2.1. Comparison of Current mode and Voltage Mode Circuits

Let us consider circuits in Figure 2.2 and 2.3 [6]. The amplifier and current mirror implementation in Figure 2.3 is called as supply–current–sensing on a voltage op-amp [7].

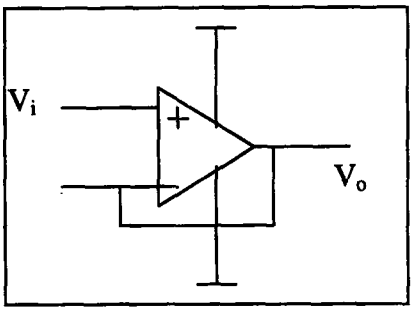

FIGURE 2.2 Voltage Follower

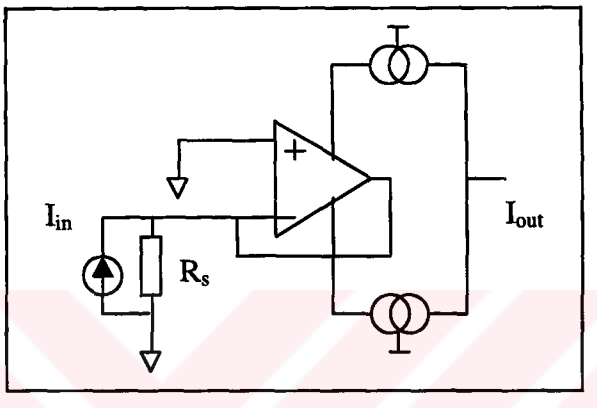

FIGURE 2.3 Current Follower

The R_S in Figure 2.3 is the output resistance of the current source. Generally the open-loop gain of the op-amp is

$$\frac{V_o}{V_{in}} = \frac{A_o}{1 + j\frac{f}{f_0}} \tag{2.1}$$

where A_o is open-loop DC gain and f_o is open-loop 3dB bandwidth. The transfer function of the voltage follower can be written as

$$\frac{V_o}{V_{in}} = \frac{1}{1 + j\frac{f}{GB}} \tag{2.2}$$

by assuming $A_o >> 1$ and the GB (gainbandwith product) is equal to $A_o f_o$. It can be seen that the 3 dB bandwidth of the closed-loop voltage follower is equal to the open-loop GB of the opamp.

For the circuit in the Figure 2.3 the following formula can be written [6]:

$$\frac{I_{out}}{I_{in}} = \lambda \frac{1 + j\frac{f}{GB}}{1 + j\frac{f}{kGB}} \tag{2.3}$$

Here, λ is the current transfer ratio of the current mirrors and

$$k = \frac{R_s + r_o / A_o}{R_s + r_o} \tag{2.4}$$

where r_o is the output resistance of the opamp. The value of $k \approx 1$ while $A_o >> R_s >> r_o$ so it is clear that the pole and zero in Equation 2.3 are canceled.

Thus, the current mode circuit operates above the GB product of the opamp and high frequency parasitic poles of the current mirrors determine the 3 dB cut-off frequency. In this application the usage of the opamp is not the same as in voltage mode. Input terminals of the opamp are at virtual ground. One disadvantage of the circuit is that the term λ limits the transfer accuracy, but the overall performance is determined by the application rather than the device [6].

The next issue to be discussed is the power consumption. One of the basic building blocks is the current mirror that will be described and analyzed later. The power consumption of the circuit is no more than a few hundred of mW. Let us consider an integrator implemented with an opamp. Typical circuitry supplied by 5 V will consume power not less than hundreds of mW in a typical application. If the supply voltage is reduced, the voltage mode circuit may not work properly or will work in a limited range.

This is because the inputs and outputs can be represented by currents less than mA. However, the voltages for voltage mode circuits can reach up to supply voltage so that the current for these values can reach tens of mAs. If the biasing current is added to this current, during operation the current sinked from the supply increases and this increases

the power consumption. But even the biasing current and supply voltage of the circuit can be small in current mode compared to Voltage mode and the power consumption is considerably less.

The statements made for power also lead us to area consideration. The power consumption is less so the total current sinked is less. This means that the transistors in the chip are not so large. Flow of the current on a transistor is proportional to W/L ratio of a MOS transistor. If large currents are not needed, the W/L ratio will be accordingly less.

This allows the implementation of more than one circuit on one chip because the area is small for most of the basic building blocks. The small IC means that the money to manufacture will be less. This is a subject that must be considered.

By reducing the size of the circuits, the recent target to implement systems on chip can be realized in analogue circuits by the current mode design techniques.

2.3. Basic Building Blocks

There are some circuits that are used commonly in current mode systems. We will concentrate on the circuits used in this work.

2.3.1. Current Mirror

Current mirror is the basic block of current mode signal processing because duplicating or scaling of a current is needed in every circuit and it can be implemented easily with a current mirror.

The performance characteristics about current mirror that are important for our specific application are accuracy, input and output resistance and bandwidth.

First we will analyze a classical current mirror then we will describe the current mirror that we used in our design so that the difference and improvement to the circuit can be seen.

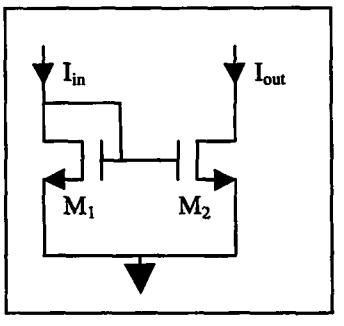

FIGURE 2.4 Simple Current Mirror

In Figure 2.4. the simple current mirror is shown. This circuit operates as the current flows trough drain of M_1 causes V_{GS} so that M_2 is forced to flow the drain current I_{out}. Assuming that all transistors are in saturation we can write the current equations as

$$I_{out} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2 \tag{2.5}$$

$$I_{in} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS} - V_T)^2 \tag{2.6}$$

where μ is the mobility of charge carriers, C_{ox} is the oxide capacitance per unit area. The transfer function can be written as

$$\frac{I_{out}}{I_{in}} = \frac{(W/L)_2}{(W/L)_1} \tag{2.7}$$

if the transistors are matched [8]. The mirroring is done when the W/L ratios of two transistors are the same neglecting the process mismatches. If the current wanted to be scaled –constant multiplication- the ratio of W/Ls of the transistors must be selected so that it is equal to scale factor.

The output resistance of simple current mirror is

$$R_o = \frac{1}{\lambda I_{out}} \tag{2.8}$$

where λ is equal to channel length modulation. We see that if the current increases the output resistance decreases. Even in lower currents the output resistance may not be high enough.

There are classical methods to improve the output resistance but the following structure is very interesting and suitable for our design to obtain higher output resistance and good frequency response.

This circuit is called Accurate Compact Cascode Current Mirror, shortly ACCCM [9]. It is given in Figure 2.5.

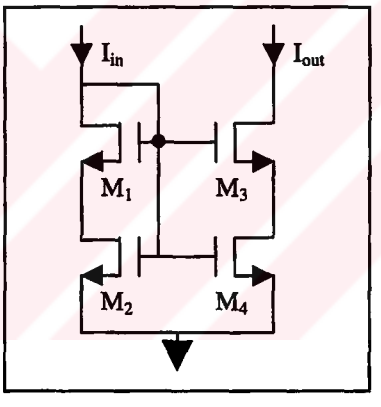

FIGURE 2.5 Accurate Compact Cascode Current Mirror (ACCCM).

The triode region current of a MOS transistor is expressed as [10,11]

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}(1+\delta)V_{DS}^2\right] \tag{2.9}$$

where δ is body effect in triode region and given as

$$\delta = \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_F}} \,. \tag{2.10}$$

Here γ is called body effect factor. The Equation 2.9 is obtained by expanding the '3/2 power' triode region expression into Taylor series. The equation shows that,

$$V_{DSsat} = \frac{V_{GS} - V_T}{1+\delta} \tag{2.11}$$

so the saturation current is given by [11]

$$I_D = \frac{\mu C_{ox} W (V_{GS} - V_T)^2}{2L(1+\delta)} . \tag{2.12}$$

We can understand by Equation 2.11 that the transistors still operate in saturation even below V_{GS}-V_T down to $(V_{GS}$-$V_T)/(1+\delta)$. For M_3 to operate at onset of saturation for widest output voltage swing, V_{DS4}=V_{GS4}-V_{GS3} should be equal to V_{Dsat4}=$(V_{GS4}$-$V_T)/(1+\delta)$. So we can write the following formula :

$$V_{GS3} - V_T = \frac{\delta}{1+\delta}(V_{GS4} - V_T) \tag{2.13}$$

With the current expression I_{D3}=I_{D4} and Equation 2.13 we can obtain the following equation :

$$\left(\frac{W}{L}\right)_3 = \frac{(1+\delta)^2}{\delta^2}\left(\frac{W}{L}\right)_4 \tag{2.14}$$

For Mietec 0.7 μm technology δ=1.6 for NMOS. Although it is sufficient to obtain W/L ratios equal to three from Equation 2.14, to keep M_4 and M_2 in saturation it is suggested to select W/Ls ratio as 15.

This current mirror achieves high accuracy and high output resistance and low input resistance at the same time. The output and input resistance is similar to that of classical cascode current mirror but because of all gates connected to each other output and input resistance is 10 per cent higher [9].

The frequency response to achieve an integrator is adequate for our needs which will be shown detailed in Section 2.3.2. This is because of connecting gates together. If the transistors will be replaced with its low frequency small signal equivalent circuit it is seen that the C_{GS4} will bring a zero because it can be considered series connected capacity. This zero is near to the pole because the capacitance values are not so different from each other. The bandwidth of the ACCCM is high enough, goes up to MHz.

But one disadvantage of the circuit as shown in Equations 2.9 and 2.10 is the body effect is a critical point on the transistors M_1 and M_3.

2.3.2. Current Integrator

The chaotic system which will be discussed in Chapter 3 includes integrator. We tried to achieve an integrator with a characteristic very close to ideal one. This means a transfer function which has a pole very close to zero (1/s). The classical current mirror was not satisfactory for us to get a good frequency response and the novel current mode block ACCCM is used. The circuit of the integrator is shown in Figure 2.6.

With classical Current mirror we could not get a transfer function having a pole not small than tens of kHz. But the circuit with the second current mirror has a transfer function obtained with an input of 1 μA shown in Figure 2.7. We discussed bandwidth of ACCCM on previous section that there is a zero close to the pole to get flat bandwidth. The effect of this is seen at the integrator's frequency response.

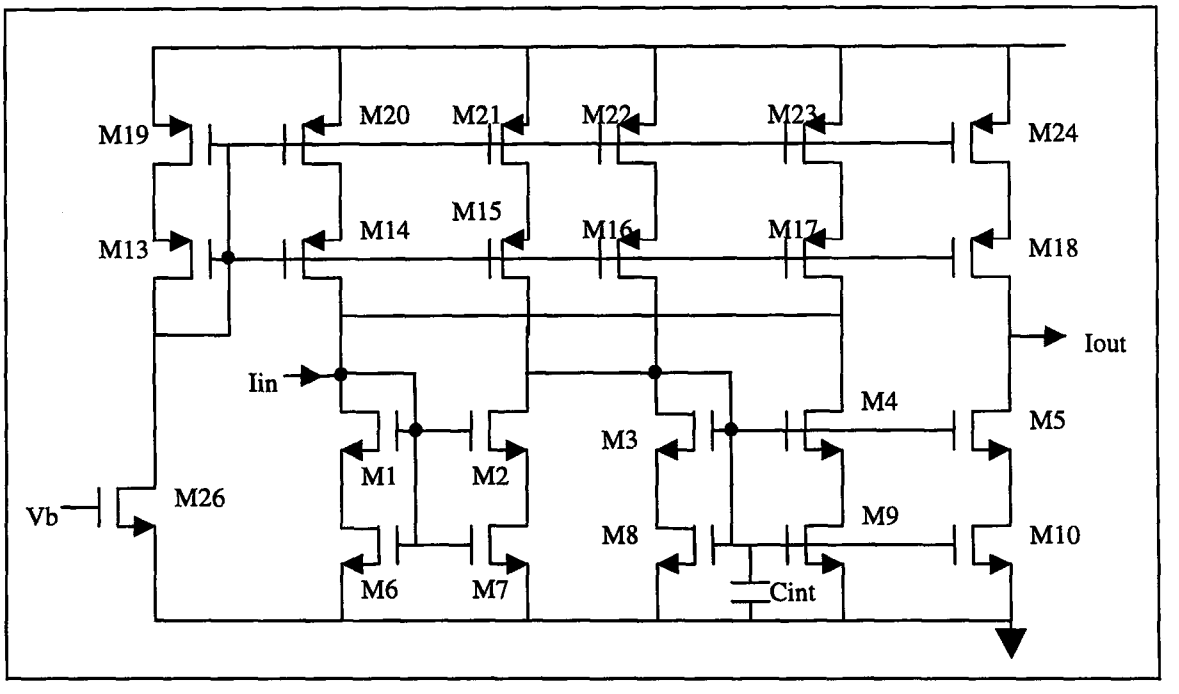

FIGURE 2.6 Current Mode Integrator

This circuit topology is obtained by changing the classical current mirrors with ACCCM from [12]. The first current mirror sources the second current mirror which charges the capacitiy as an integral of the current. The charge voltage on the capacitiy changes the output of the current mirror. This output is fed to the input of the first current mirror to achieve the integration. The capacitor is in the closed loop to achieve the transfer function similar to an integrator.

The ACCCM has high output resistance so this makes the transistor matching problem more important. Layout step is critical for this circuit so the layout techniques – will be described in Section 3.2.2 – will be considered seriously.

The chaotic system will work in frequency range 20 Hz to 20 kHz that is hearable sound band. The phase response of integrator must be remained close to ideal in this frequency band. The measurements show that even, frequencies up to Mhz the phase shift of the integrator is close to 90 degrees. The phase of the circuit is shown in Figure 2.8.

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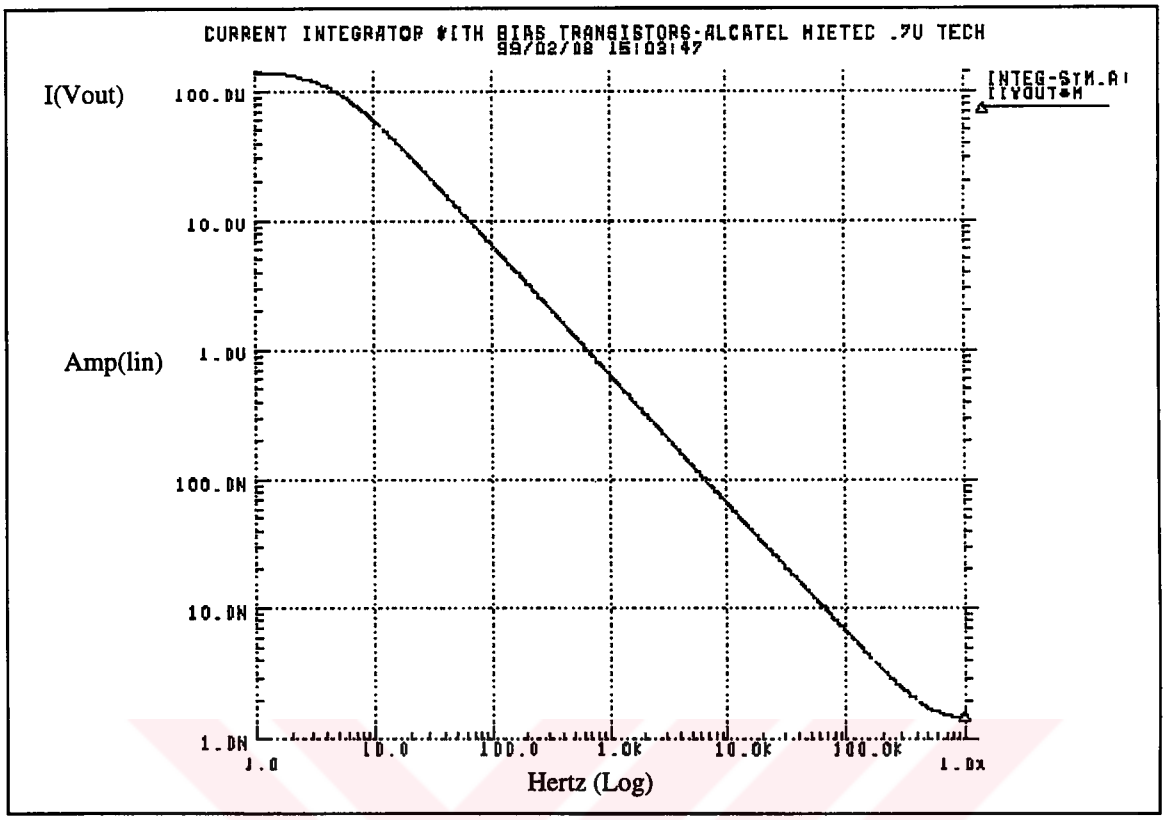

FIGURE 2.7 Frequency Response of Integrator

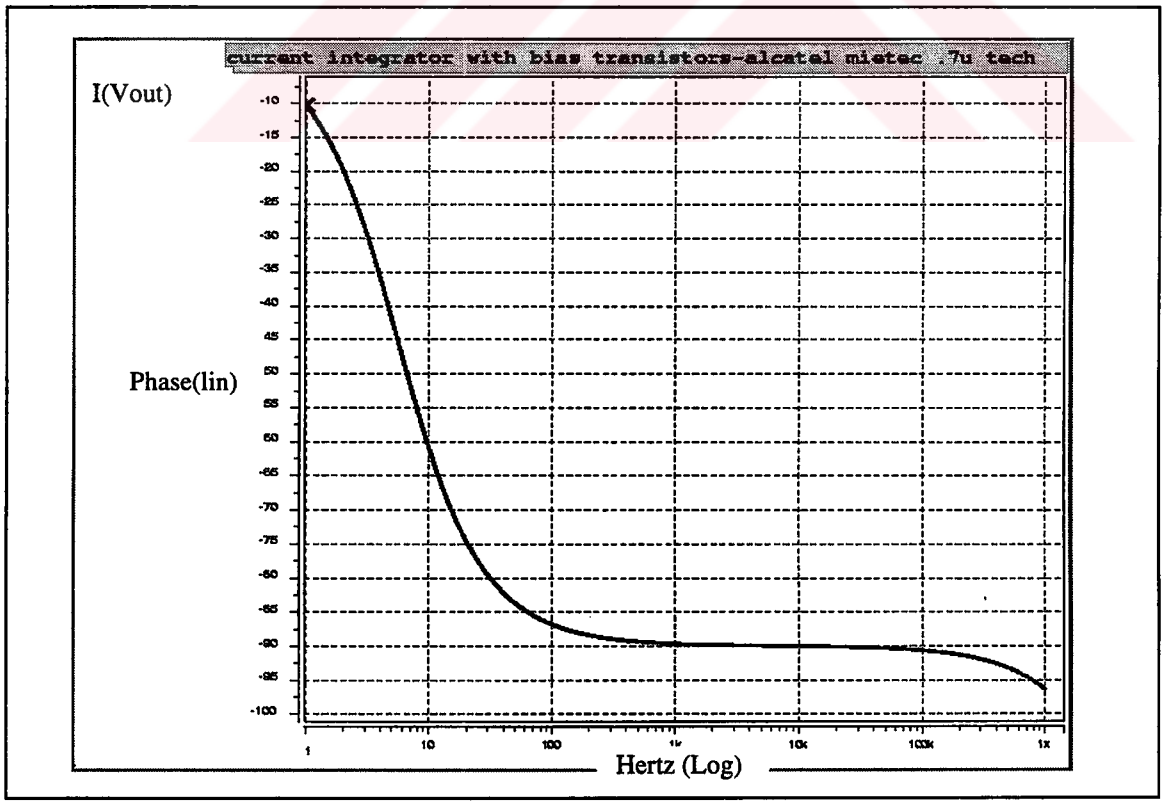

FIGURE 2.8 Phase Response of Integrator

To have symmetric signals at input and output, the voltages are adjusted to be in the middle of the supply voltage range. The supply voltage for the system is 5 volts and integrator has input and output voltages of approximately 2.5 volts. If not, the combination of the blocks would not work as expected because the intermediate nodes of the blocks would float.

2.3.3. Current Multiplier

The next building block is the current multiplier. The performance characteristics for this block are the linearity and low offset because the linearity will effect the quality of the communication. This block will be in a feedback loop as will be shown in Section 3, little offset will become higher and cause the circuit to stuck in either supply voltage or ground depending on the type of the offset.

This circuit is shown in Figure 2.10 [13]. This is the basic idea to implement current multiplication and the operation of the block is simple. The transistors N1,N2,N3,N4 is the standard voltage multiplier and in front there is I to V converter so the current input is converted to voltage and multiplied and then the output is obtained as current.

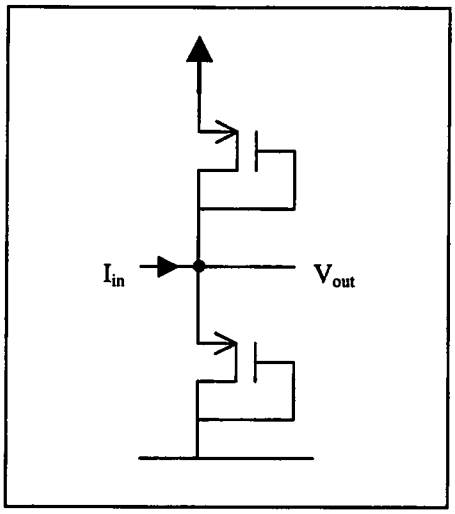

FIGURE 2.9 Basic I-V Conversion Circuit

The I-V converter used in the circuit is shown in Figure 2.9. The transfer function of this circuit can be expressed as [13]

$$V_A = \frac{I_{in}}{K_A} \tag{2.15}$$

where $K_A=2\beta_v(V_{dd}-|V_T|)$.

Considering currents of the transistors N1, N2, N3 and N4 the following function can be written :

$$I_O = I_{N1} + I_{N2} - I_{N3} - I_{N4} \tag{2.16}$$

Here the currents I_{N1}, I_{N2}, I_{N3} and I_{N4} are the standard MOS current equations. If we replace the V_{gs} term with the corresponding current value at the output of I-V converter, the main multiplication expression can be obtained as

$$I_O = \beta \frac{I_1 I_2}{K_A^2}. \tag{2.17}$$

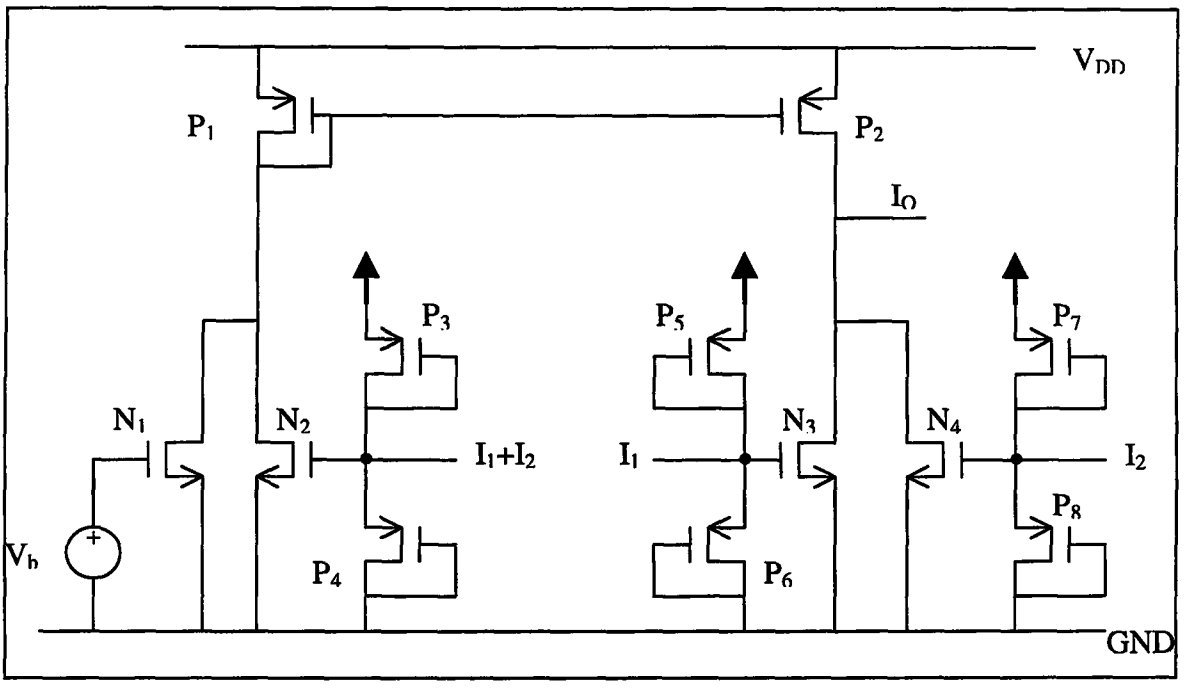

FIGURE 2.10 The Current Mode Multiplier Circuit.

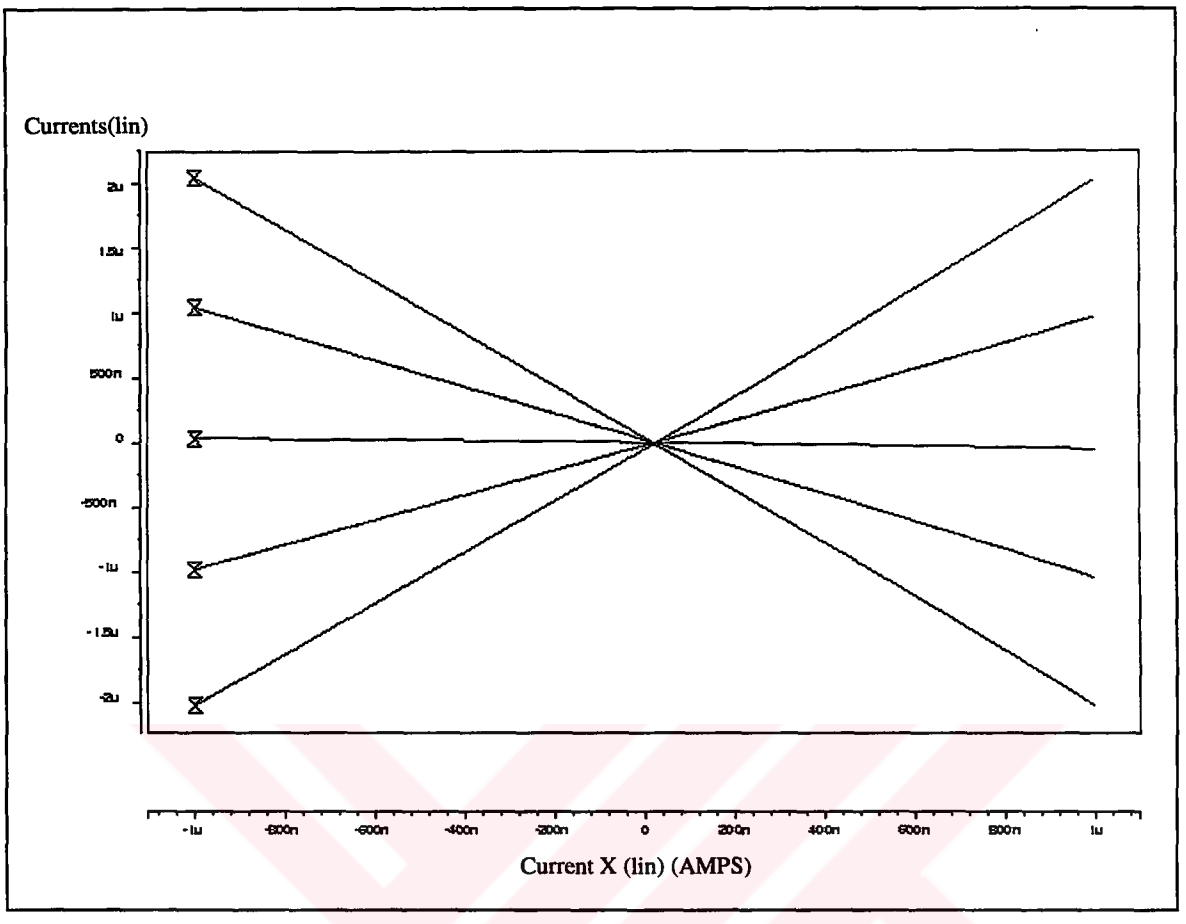

FIGURE 2.11 DC Transfer Characteristics of Multiplier

The non-linearity and offset is present for the circuit that can be observed from Figure 2.11. The circuit is highly linear but the addition circuit at the input can affect the linearity. The adder is presented in the next section.

Cancellation of the offset is very easy for current mode circuits. By sourcing or sinking current same as offset value cancels the offset. Even making the offset zero is possible.

The transient response of the multiplier is shown in Figure 2.12. The plot below is the ideal multiplication scaled from MATLAB simulation results –see Section 3- and the above one is the output of the implemented circuit. There are extra blocks at input and output of the multiplier for scaling, to fit the dynamic range and to achieve unit multiplication at order of μA.

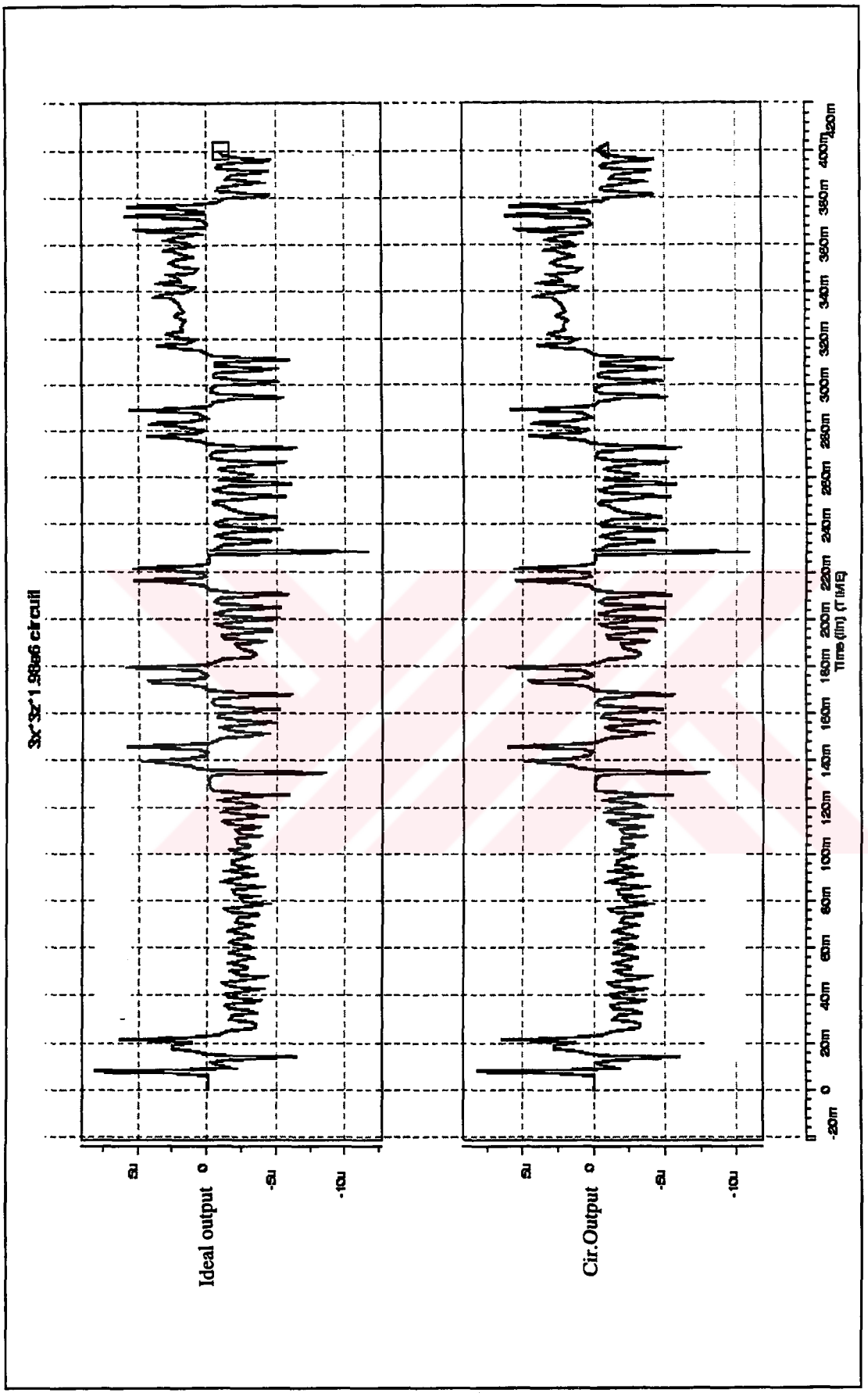

FIGURE 2.12 Comparison of Transient Responses of Current Multiplier

2.3.4. Current Adder and Subtractor

From the Figure 2.10 it is observed that for the multiplier there is a requirement for a block to add the inputs. The subtractor is also used in the chaotic system. For this purpose a simple circuit to acive addition and subtraction at the same time is designed shown in Figure 2.12.

Here we used the classical current mirrors to duplicate and to change its direction – that means changing its sign. The p type current mirror is used because to have various blocks to understand their behavior within a system.

The maximum available output value of the circuit is 10 μA so the inputs must be kept in the range not to force the output more than this value. For example the both inputs of the adder must not exceed 5 μA.

The transistors M_9, M_{10}, M_{11} and M_{12} are used to achieve the circuit's output sign positive. The outputs of the current mirrors are negative so we must use a current mirror to make the sign positive both for addition and subtraction. Here, V_b is the bias source that is selected as 2 V.

Addition is only used at the input of the multiplier and for the rest of the circuit subtraction part is used –will be described in Section 3. To reduce the number of transistors, adder and subtractor can be separated but in this work the area consumption was not so critical problem.

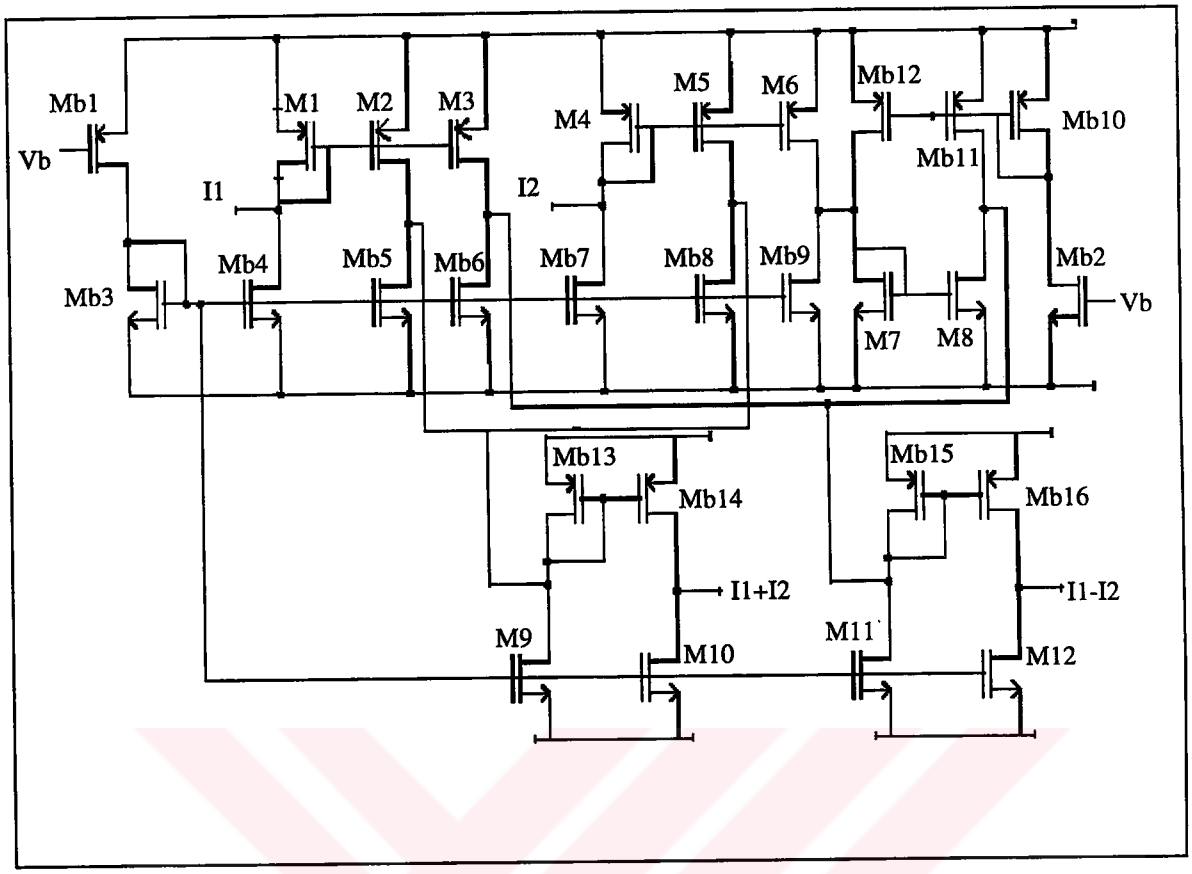

FIGURE 2.13 Adder Subtractor Circuit

3. CHAOTIC COMMUNICATION IC

In this section, a chaotic system with the current mode building blocks -described in above section- will be presented. Problems or design constraints about current mode circuits may only be seen by realizing such a circuit.

An analog communication system is not preferred nowadays considering the security issues. The classical security implementations for analogue communication are not as many as in digital. For example there are different ways of encrypting and processing the digital data but for analogue signals there is only frequency hopping technique.

The security is achieved by chaotic behavior of Lorenz based chaotic circuits. These type of signals are similar to noise so hard to predict.

The communication is based on synchronizing two such Lorenz based circuits by transmitting a state variable. Even adding a message to this variable the synchronizing occurs. All this concepts and the implementation will be detailed in the following subsection.

3.1. Chaotic System

A chaotic system is a dynamic non-linear system that has strange attractors. Even infinitesimally close initial points give rise to totally different trajectories, i.e. chaotic systems have high sensitivity to initial condition. Because of this property such systems have long term unpredictability.

Privacy and security are important issues in communication. In digital domain, the security can be obtained mathematically by coding etc. But it is not that easy in analogue design. In analogue communication masking can provide a solution to the security problem.

The signals obtained from a chaotic system exhibit noise-like behavior, i.e. noise-like spectral characteristics. This makes such signals good candidate for masking.

Under certain conditions chaotic systems have a synchronizing behavior [14], if an appropriate chaotic signal is used as a mask at the transmitter end, the same signal can be regenerated at the receiver end using the transmitted signal and a chaotic signal identical to the one at the transmitter, without needing additional synchronization signal [15].

This approach first presented in [15], will be explained below in further details, using the Lorenz system as the chaotic signal generator.

The communication system consists of two identical (or almost identical) chaotic systems, one for the transmitter and the other is the receiver as shown in Figure 3.1, as the chaotic systems we have chosen the one given by the Lorenz equations, shown in Equation 3.1.

$$\begin{aligned} \dot{x} &= \sigma(y - x) \\ \dot{y} &= rx - y - xz \\ \dot{z} &= xy - bz \end{aligned} \tag{3.1}$$

The variables x, y, z are the states of the system and σ, r, b are constant values. If the constants are chosen appropriately, the system exhibits chaotic behavior. We have used the following values: σ=10, r=30, b=6.6/3. With these values the system simulated in Matlab and it has been observed that the Lorenz system shows chaotic behavior.

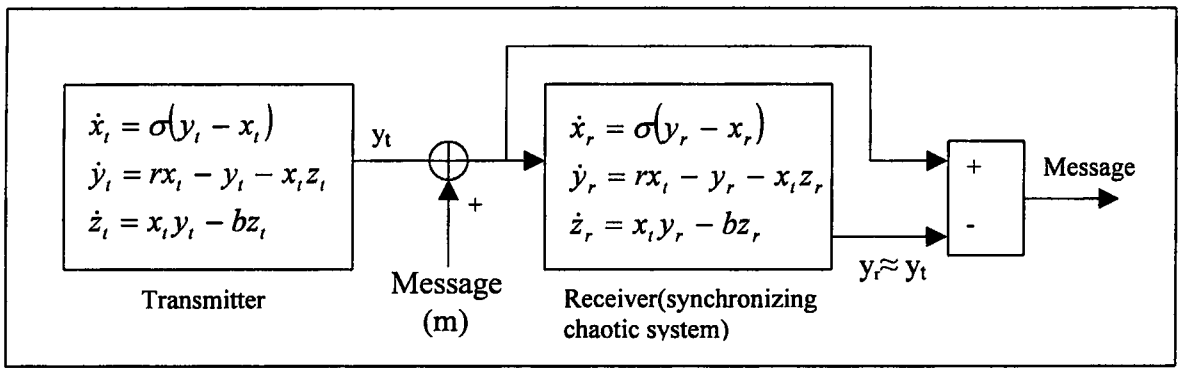

FIGURE 3.1 Chaotic Communication System

The communication is based on the synchronization of two chaotic systems – transmitter and receiver- that can be achieved by transmitting an appropriate state variable to the synchronizing chaotic system (receiver).

How the appropriate state variable to be transmitted can be determined is explained in [15]. In this specific case y(t) has been used as transmitted state variable.

Synchronization is the converging of the receiver's trajectories to the same values as the transmitter. The mathematical proof or this behavior is done in [14].

In the literature the transmitted state variable is called as chaotic masking signal. The message is added to this signal to achieve communication. The constraint about adding the message to masking signal is that the power spectrum should have a signal to masking ratio approximately –20dB that the original masking signal can be recovered as shown in [15].

From here onwards the sum of the masking signal and the message will be referred to as the transmitted signal. The transmitted signal, in spite of the additional message, is still able to synchronize the receiver so the masking signal is obtained. Clearly, if we subtract the recovered masking signal from the transmitted signal the message can be recovered. Usually, in order to eliminate the noise effects came from media the message should be filtered appropriately.

This block diagram –shown in Figure 3.2- is realized by using current–mode circuits using the building blocks described in Section 2. For this purpose several scaling operations are necessary to satisfy the constraints of the current-mode circuits utilized, such as the operation range, bias current, etc. In the Equations 3.2 and 3.3 the frequency response of the integrator is modified as to obtain close to ideal response.

The one in front of the multiplier is to unitize multiplication to microamperes. It means that all the blocks in real world work in the ranges of microamperes so the multiplier has to multiply 10 μA and 10 μA as unit inputs.

$$H(s) = \frac{K}{s+a} \tag{3.2}$$

$$H'(s) = \frac{H(s)}{a} = \frac{\frac{K}{a}}{\frac{s}{a}+\frac{a}{a}} = \frac{K'}{s'+1} \tag{3.3}$$

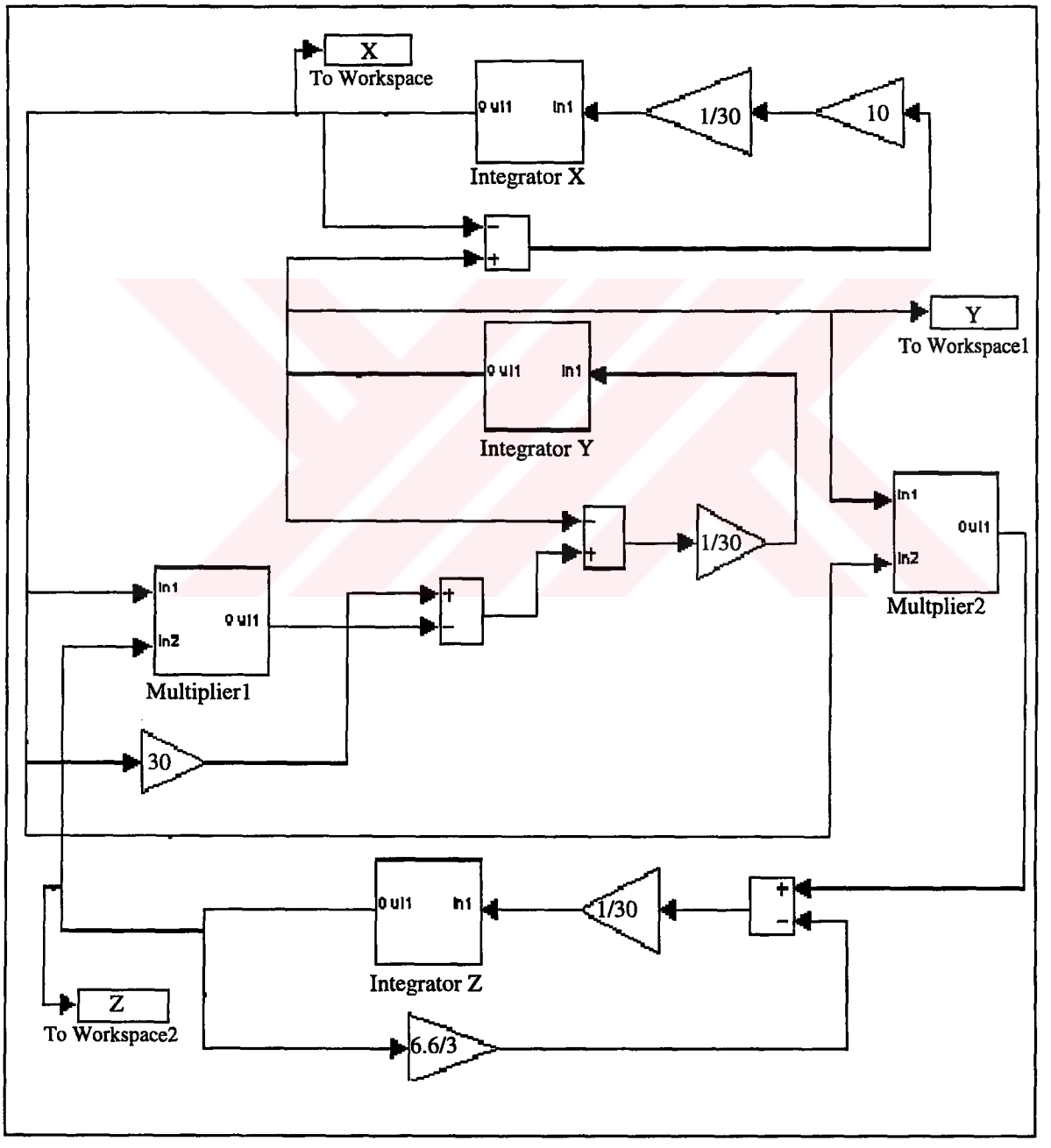

FIGURE 3.2 The Matlab Block Diagram of the Chaotic System

In Figure 3.3 the obtained chaotic signals from the implemented Lorenz-based chaotic system in Matlab are shown. These are the state variables x(t), y(t) and z(t) of the Lorenz equations respectively. The chaotic behavior can be observed by the attractors – trajectories in phase space - of the system. The xy and xz projections of the attractors are presented in Figure 3.4. It is not that smooth as the ideal mathematical simulations because of the difference of the circuit implementation.

In the Figure 3.5 the transmitted state variable and the recovered one at the receiver end is shown. The $y_t(t)$ synchronizes the receiver and at the receiver this $y_t(t)$ does not fed to the second equation which generates $y_r(t)$. The transmitted variable is inputted to the first and third equations and the recovered state variable $y_r(t)$ is achieved as shown in the figure. This is because of the time constants of the integral loops –not the integrators- of the circuit. If the pole of the integrator inside this loop is shifted to the right –in Bode plot- the obtained signal at the receiver is better. A lossy integrator is more suitable for such a system as shown in [16].

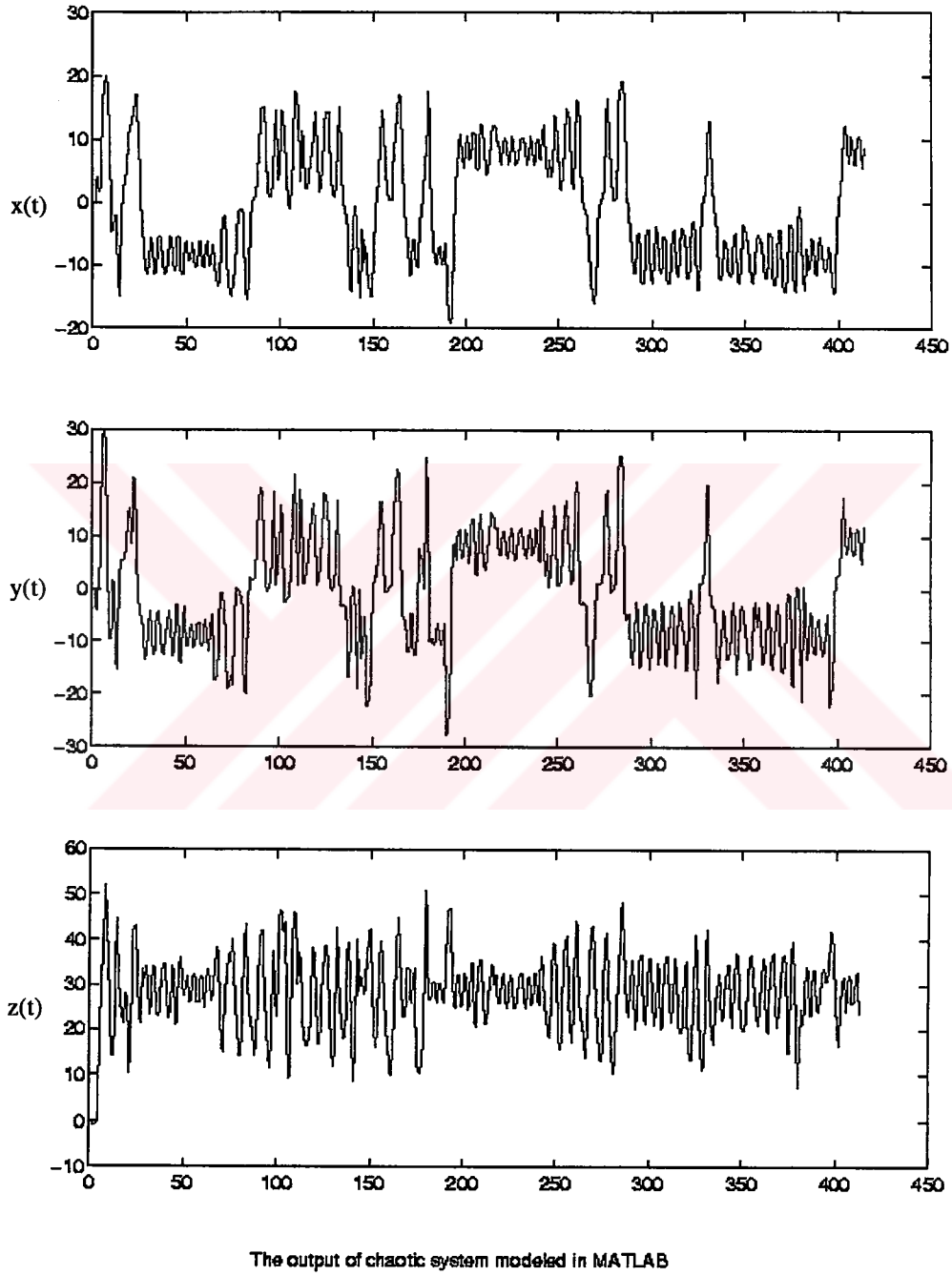

FIGURE 3.3 The Chaotic Signals of State Variables (x, y and z)

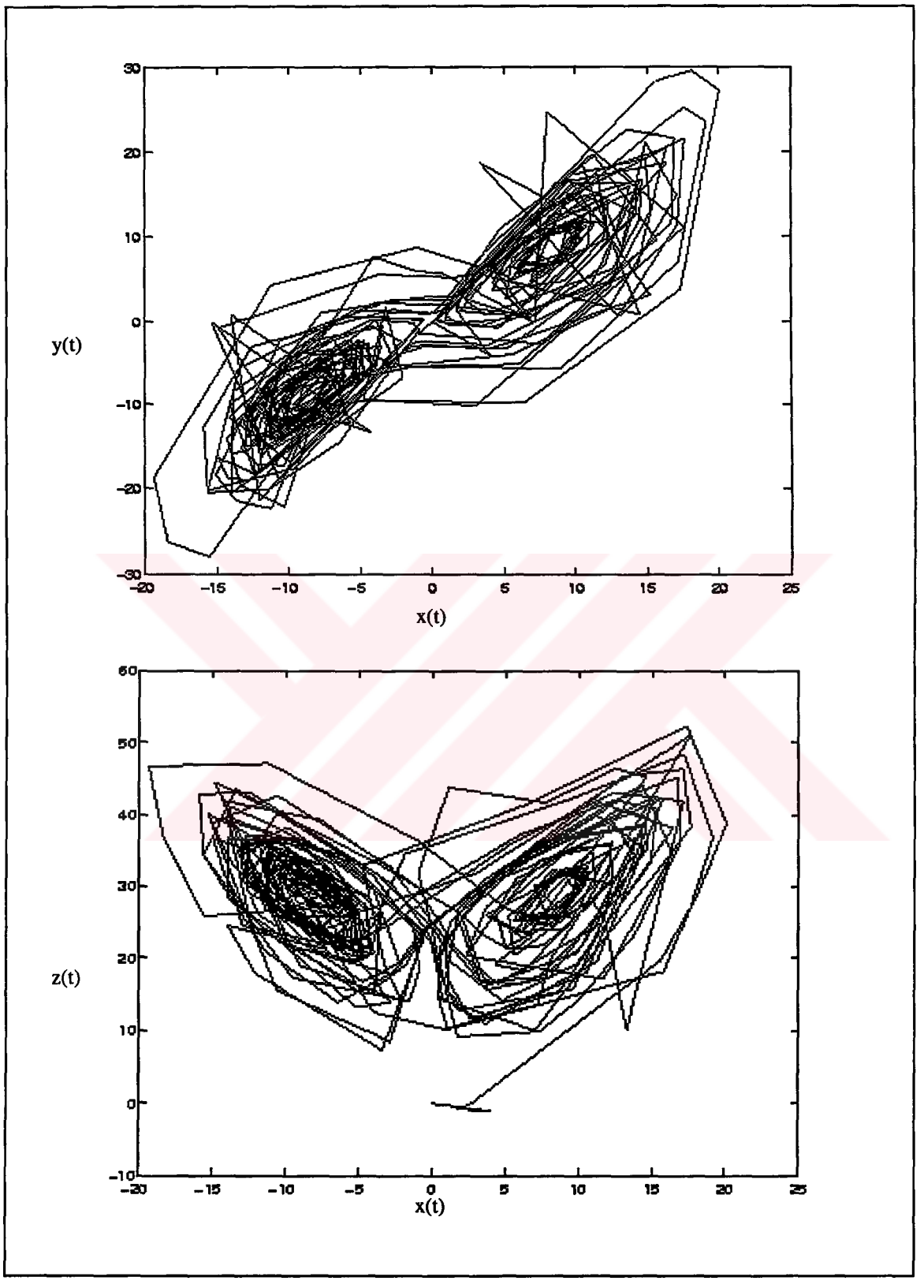

FIGURE 3.4 Attractors of the Lorenz System with σ=10, r=30, b=6.6/3 as Simulated in Matlab(xy and xz projection respectively)

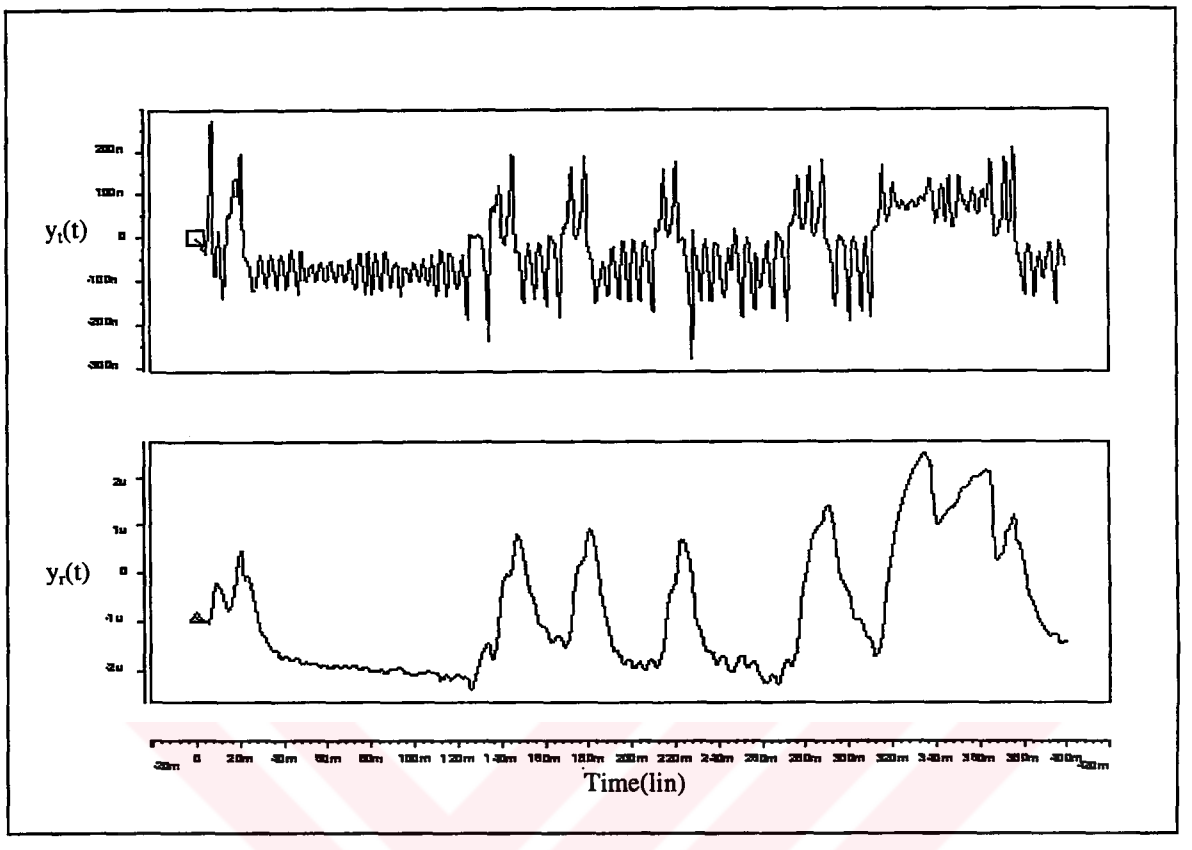

FIGURE 3.5 Transmitted State Variable and Recovered One at Receiver

3.2. Design Considerations

3.2.1. Simulation

One of important points for current mode design is the input and output voltages. Let us consider two cascade current mirrors as in Figure 3.6. To transport the current from one block to another, the voltage at the input of the second block must be the same as the output of the first one. If it is not, the symmetry of the intermediate signal is lost because the equivalent voltage will be at a value determined by equivalent resistance. Also the current value changes because the input resistance of the current mirror remains the same so that the voltage difference effects the current.

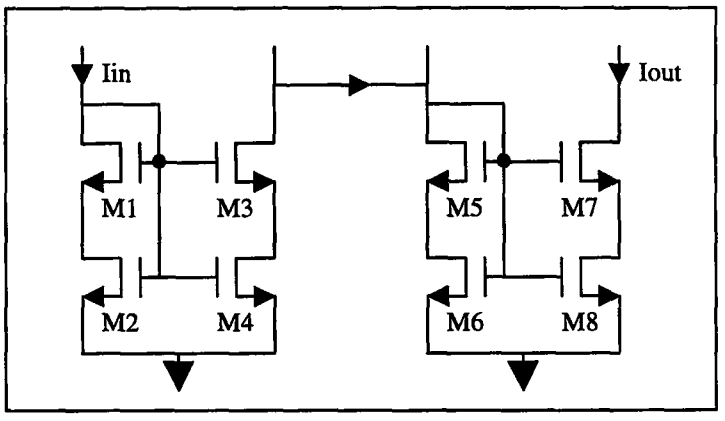

FIGURE 3.6 Cascade Current Mirrors

Let us consider the Figure 3.6 again. Especially for adder and subtractor circuit, the output current is not higher than the bias current. For realized adder the bias current is 10 μA and the output that the circuit maximum operates as an adder-subtractor is again 10 μA. While constructing the system we must consider how much current is needed for the next block.

The next point to take into consideration about chaotic communication system is the frequency and the phase response of the integrator. The ideal integrator has a frequency response which has a pole at s=0 and the phase response is 90 degrees. In real world this is not the case. The frequency response of the integrator has a pole at the point s=a. The problem is to make this pole closer to zero. This can be done by –for the integrator topology presented here- to increase the capacity and to decrease the biasing current. If you increase the capacity the required goal could not be achieved. That was to realize every thing on a chip.

If the bias current is decreased then there is a problem about the output resistance of the current mirrors as stated in Section 2.3.1.

The other design issue for integrator is the phase response. The frequency range that the phase is 90 degrees with a desired error must cover the frequency range of which the circuit is designed for. If it is not then some frequency compensation techniques would be applied.

The measuring is the key point of the analysis of the current mode circuits. Every block drives an input consist of current mirrors, so classical current mirror which has same voltage at the input –as the voltage at the output of main circuit- is used as the load for the main circuit. Obtained circuit output values are similar to normal operating values. This is shown in Figure 3.7.

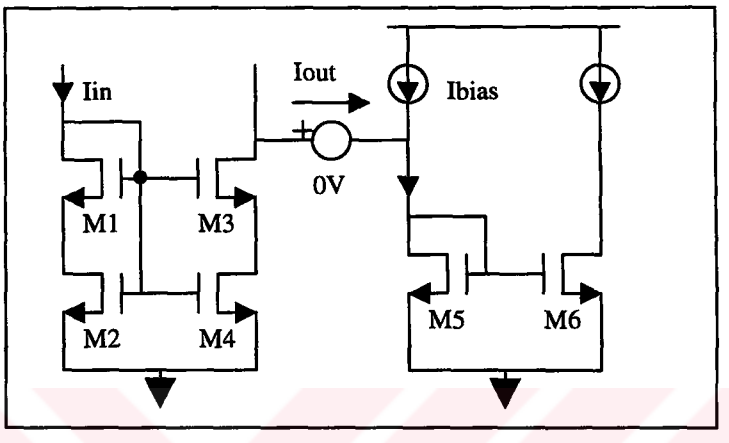

FIGURE 3.7 The Load to Measure the Output Current

The voltage source at the output is to read the output current in Hspice program easily. There is no other way found for Hspice to read the current because, as it is seen, it is the same node. This violates the tradition of the spice program. For current mode circuits there can be a new program for observing such currents easily. This point will be stated also in Section 5 as a future work.

$$\lambda = 85.10^{-4}\frac{3.10^{-6} - 2L_D + DELL}{L - 2L_D + DELL} \tag{3.4}$$

$$\lambda = 10^{-3}\frac{3.10^{-6} - 2L_D + DELL}{L - 2L_D + DELL} \tag{3.5}$$

3.2.2. Layout

The technology used to implement the system is Alcatel 0.7μm CMOS technology. There are some points to take into consideration. In this technology λ varies with the length of the transistor as shown in Equation 3.4 for NMOS and in Equation 3.5 for PMOS.

Here L is the length of the transistor, L_D is the lateral diffusion and DELL is the length reduction of source and drain diffusion. The depletion region between source and bulk reduces the effective channel length. This parameter is not important for large feature sizes because typical value of this parameter is less than 0.1 μm but for 0.7 μm technology we must consider it. In the Appendix B the model card used in this work is listed.

It can be seen that if the transistors have different L values the λ must be recalculated and a new model must be assigned. Not to calculate many λ values, all of the transistors have the same L value, e.g. 1 μm or 10 μm.

One important issue for the layout is the matching of the transistors, e.g. in current mirrors. This constraint is about all analogue layouts. Because of the doping density and the other effects of the fabrication process such as etching, parasitics, etc., it is hard to achieve two identical transistors. Generally we can make the following statement: The process parameters will affect the circuit but we must draw the layout such a way that the effects on each transistor will be same.

To achieve this property, the transistors to be matched, i.e. must placed near to each other such that the structure is identical for both. There are different layout techniques like interdigitated, common-centroid, fully stacked, etc [17,18]. The fully stacked technique is based on splitting the transistors into smaller transistors. The common-centroid technique is a structure to divide the transistor into subsections along orthogonal axis. These layouts are shown in Figure 3.8 and 3.9 [17].

Another thing done in the layout is to add dummy elements into the circuit to achieve the symmetry for the main transistors. This will make the area a bit larger but the main goal is to operate the circuit.

In this thesis all layout techniques are tried to be implemented in the design. In fact it is important to use them at the proper part of the system. Merging means to take the advantages of all techniques at the same time.

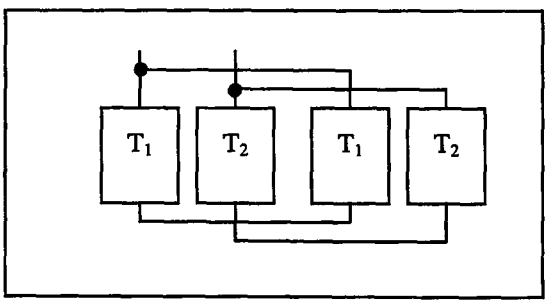

FIGURE 3.8 Interdigitated Layout

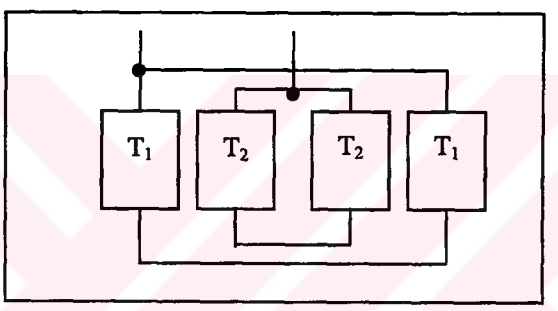

FIGURE 3.9 Common-Centroid Layout

4. INTERFACE WITH CURRENT MODE CIRCUITS

Current mode design is not a familiar design technique nowadays and we must use voltage mode circuits with current mode circuits, so there is a compatibility problem with voltage mode circuits. But if the input and output variables are currents then there is no need to deal with the interfacing.

There are not standard current mode circuits as much as in voltage mode. For example the corresponding ones of simple transistor amplifier, oscillators, etc. in current mode are not that popular or realized.

Blocks adequate for our needs to realize large systems can not be found as easy as in voltage mode, so merging these two types of circuits is the only way to solve the problem. In this section the blocks designed for this purpose will be stated briefly.

Interfacing current mode circuits with voltage mode circuits means voltage to current or current to voltage conversion. For the conversion, the loading conditions are must be taken into consideration. Input resistance must be high enough and output resistance must be as low as possible for V-I conversion, for I-V conversion vice versa. Because the current input means lower resistance.

The frequency range of the converter must be larger than the circuits operation range not to affect the AC behavior. The poles and parasitic frequencies of the converter must be kept far away from the frequency range that the circuit will operate.

The transfer accuracy is the first point to deal with. If current to voltage or voltage to current conversion could not be done with minimum error then the other performance parameters as loading and frequency response lose their importance. But the V-I conversion is less complex because a MOS transistor itself can be considered as a simple transconductor. There is very low current flows into the gate so input resistance is as high as MΩ. But the technology and device geometry effects the transfer accuracy for a MOS transconductance. It is not preferred to use alone as a transconductance.

I-V conversion can be easily done with a resistor. The current on the resistor creates a voltage on it. As stated above the key point is the low input resistance because the inputting signal is current. Again MOS can be used for this purpose with the reverse behavior. In fact the voltage between gate and the source terminals of the transistor creates a drain current but also by flow of the drain current it is possible to obtain a voltage difference between gate to source terminals as done in current mirrors. Again the technology parameters and device geometry is the effects of the conversion.

This interface circuits can be considered as analog VLSI design technique. The importance is given to the transconductors. In this thesis these circuits are not implemented and the theory of these type of circuits –transconductors- with MOS transistors will be stated in the below section briefly.

4.1. Transconductors

The block that converts voltage to current is called a transconductor. We can classify transconductors into three groups, differential pair transconductors, adaptively biased transconductors and triode region transconductors. In this section, the widely used differential pair transconductors will be described. The circuit of the differential pair transconductor is given in Figure 4.1.

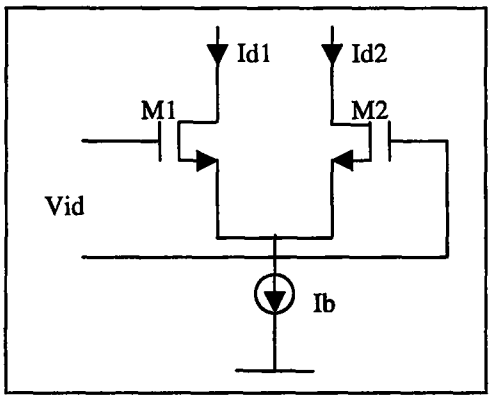

FIGURE 4.1 Differential Pair Transconductor

With the saturation current and assuming the transistors are matched we can write the following formula :

$$I_O = I_{D1} - I_{D2} = \begin{cases} \sqrt{2KI_b}V_{id}\sqrt{1-\frac{K}{I_b}V_{id}^2} & , \ |V_{id}| \le \sqrt{\frac{I_b}{K}} \\ I_b \operatorname{sgn}(V_{id}) & , \ |V_{id}| \ge \sqrt{\frac{I_b}{K}} \end{cases} \quad (4.1)$$

where V_{id} is the differential input voltage and K is given as

$$K = \frac{\mu C_{ox} W}{2L}. \quad (4.2)$$

The Equation 4.1 shows that the output is linear in a specific range. This nonlinearity is a disadvantage of differential pair transconductors. This problem can be solved by cross-coupling two differential pairs [19].

The Equation 4.1 also shows that the nonlinearity increases when the input signal increases. For large signal performance nonlinearity can be defined as the per cent deviation of the output current from the ideal value $g_m V_{id}$ (g_m is the small signal transconductance). To obtain nonlinearity less than 1 per cent from the Equation 4.1 we can describe the range of linear dynamic operation as

$$-0.20\sqrt{\frac{I_b}{K}} \le V_{id} \le 0.20\sqrt{\frac{I_b}{K}}. \quad (4.3)$$

By substituting the small signal equivalent of the transistors we can find the frequency response of the transconductor. The transconductance can be given by

$$\frac{I_0(s)}{V_{id}(s)} = \frac{g_m\left(1 - s\frac{C_{gd}}{g_m}\right)}{sR_S\left(C_{gd} + C_{gd}\right)+1}. \quad (4.4)$$

Here R_S is the output resistance of the source. This response is made by assuming the load of the transconductor is zero because the transconductor drives a current mode system. A current mode circuit's input resistance must be very low and the output resistance must be high as mentioned before.

5. CONCLUSION AND FUTURE WORK

Digital design techniques are preferred by most engineers today because of the simplicity of the concept. There are many things to implement by digital circuits. Considering that the real world is analog, the conversion of signals is required and also the size of the digital circuit increases with the complexity of the function.

Today the systems became larger and consume high power. This leads engineers to reconsider analog techniques again. But from the voltage mode perspective the analog circuits are not advantageous considering implementation.

Recently this has been changing. The current mode design technique is being more popular day by day. For VLSI design, the two important problems in front of the designers are area and power. These problems can be solved by current mode design techniques.

In this thesis, the concept is described and some circuits used commonly in these type of circuits are analyzed as building blocks. With this circuits a chaotic communication system based on synchronization of two chaotic circuits is implemented.

Chaotic behavior is very interesting behavior from communication security point of view. Analog communication does not bring so much chances for the system to be secure. As mentioned in the relevant sections the signals can be mistaken for noise by the person who tries to listen the communication. This concept can not be implemented in digital circuitry.

An important work done in this thesis is to implement such a communication system on a chip. Previously, there are monolithic chaotic circuits but the current mode implementation is the main goal of this work.

Possible future works of this thesis will be in current mode applications. The improvement of the quality of the communication system because of process variations can be a subject for a Ph.D. dissertation.

Current mode circuits make the adding and subtracting functions very easy. The implementation of digital circuits with current mode techniques is very interesting projection to digital circuitry considering the low power and low area specifications. There are implementations in the multivalued logic systems but a system entirely working in current mode performing logic functions must be taken into consideration.

Observing intermediate currents with Hspice is not easy. If we consider the Figure 3.5 the voltage source at the output of the ACCCM only connected like this to observe the current. If there were no voltage source the nodes will be connected together and at one node we can not measure the current. If the currents wanted to be observed is very much then there will be many voltage sources and it is easy to confuse and make mistake. Special CAD tools that makes current observation of this type will be useful for current mode design.

APPENDIX A

The triode region current expression will be explained here. Let's assume a MOS transistor shown in Figure A.1 has long channel relative to the feature size (L≥5μm and V_{DS}≤5V), operating in strong inversion the drain current can be expressed as

$$I_D = 2K\left\{(V_{GS} - V_{FB} - \phi_B)V_{DS} - \frac{1}{2}V_{DS}^2 - \frac{2}{3}\gamma\left[(V_{DS} - V_{SB} + \phi_B)^{\frac{3}{2}} - (V_{SB} + \phi_B)^{\frac{3}{2}}\right]\right\}. \quad (A.1)$$

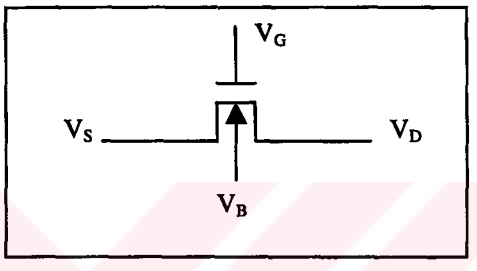

FIGURE A.1 MOS Terminals

Equation A.1 is too complex to use in hand calculations because of the 3/2 power terms. The nonlinear change in depletion charge along the channel causes these terms but this variation is only weakly nonlinear. Under this condition linear approximation gives us the following formula:

$$I_D = 2K\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}(1+\delta)V_{DS}^2\right] \quad (A.2)$$

This equation is true if V_{DS}<$V_{DS(sat)}$ where

$$V_T = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + V_{SB}} = V_{TO} + \gamma\sqrt{\phi_B + V_{SB}} - \sqrt{\phi_B} \quad (A.3)$$

$$\delta \approx \frac{\gamma}{2\sqrt{1+\phi_B+V_{SB}}} \quad (A.4)$$

$$V_{DS(sat)} = \frac{V_{GS} - V_T}{1+\delta} \quad (A.5)$$

and

$$K = \frac{\mu C_{ox} W}{2L} . \qquad \text{(A.6)}$$

APPENDIX B

The Alcatel Mietec 0.7 μm CMOS technology model cards used in Hspice analysis are as follows. TNA is the NMOS model TPHA is the PMOS model. These are the typical model values. The slow and fast models are also available.

This is a two metal layer process and maximum supply voltage (the maximum channel voltage) for this model is 5.5Volts. The minimum design grid for poly, Metal1 and Metal2 layers is 0.05 μm and 0.1 μm for others.

```
* MODEL CARDS CO7M NMOS - TYPICAL MODELS

.MODEL TNA NMOS LEVEL=2
+ TOX=170E-10 XJ=0.05U NFS=1.2E11 VTO=0.75 NSUB=7.0E16 DELTA=1.7
+ U0=470 UCRIT=1.08E5 UEXP=0.124 RSH=520 LD=0.1U DELL=0.2U WD=0.05U
+ JS=1E-3 CJ=5.0E-4 MJ=0.32 CJSW=2.8E-10 MJSW=0.23
+ PB=0.68 FC=0.5 CGSO=4E-10 CGDO=4E-10 KF=3E-28 AF=1

* SCALABLE MODEL
*+ LAMBDA=0.0085*(3E-6-2*LD+DELL)/(L-2*LD+DELL)
+ LAMBDA=1.16e-3
* FOLLOWING PARAMETERS ARE FOR HSPICE
*+ XL=O.2U XW=0U NLEW=0.0

* MODEL CARDS CO7M PMOS - TYPICAL MODELS

.MODEL TPHA PMOS LEVEL=2
+ TOX=170E-10 XJ=0.05U NFS=0.5E11 VTO=-0.95 NSUB=3.5E16 DELTA=1.6
+ U0=158 UCRIT=1.15E5 UEXP=0.265 RSH=870 LD=0.06U DELL=0.15U WD=0.1U
+ JS=1E-3 CJ=6.0E-4 MJ=0.51 CJSW=3.6E-10 MJSW=0.35
+ PB=0.90 FC=0.5 CGSO=1E-10 CGDO=1E-10 KF=5E-30 AF=1

* SCALABLE MODEL
```

+ LAMBDA=0.010(3E-6-2*LD+DELL)/(L-2*LD+DELL)

+ LAMBDA=4.29e-3

* FOLLOWING PARAMETERS ARE FOR HSPICE

*+ XL=O.15U XW=0U NLEW=0.0

APPENDIX C

The layouts of the system and the blocks are presented here. The layout techniques used can be observed clearly. The number of transistors is 300.

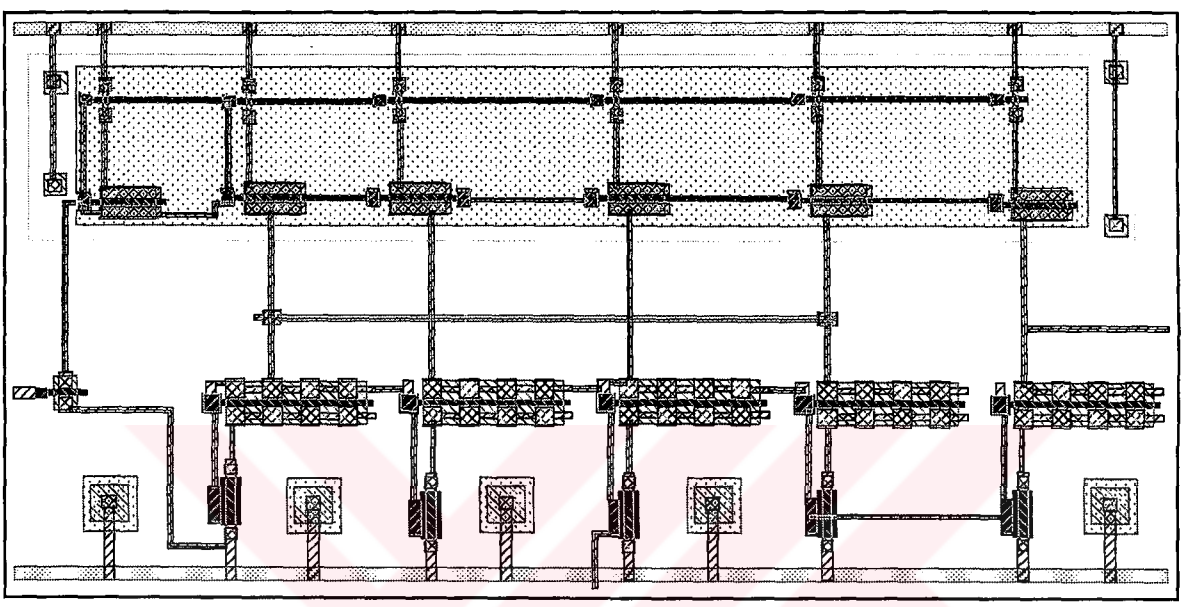

FIGURE C.1 Layout of the Integrator

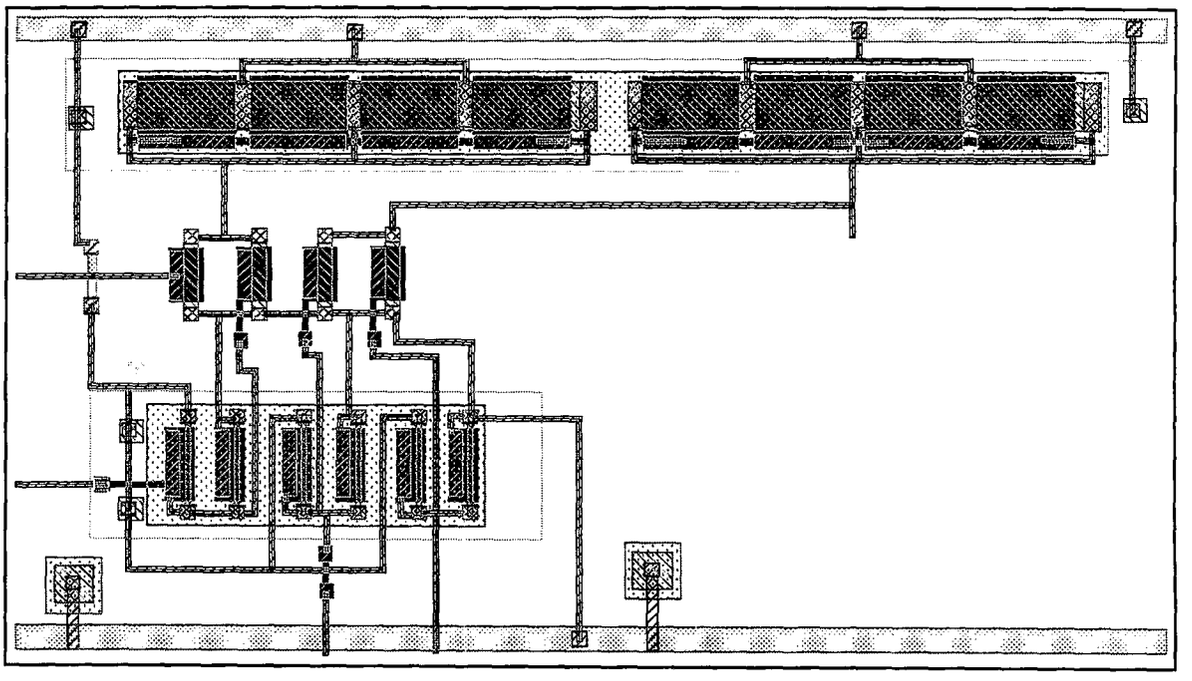

FIGURE C.2 The Layout of the Multiplier

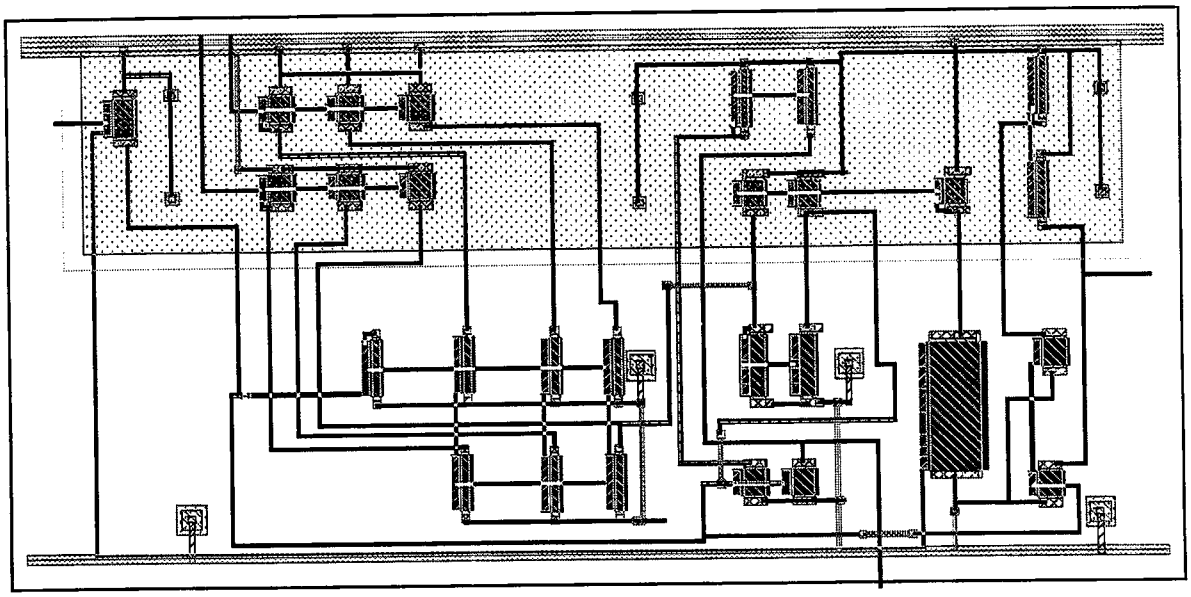

FIGURE C.3 Layout of the Adder-Subtractor

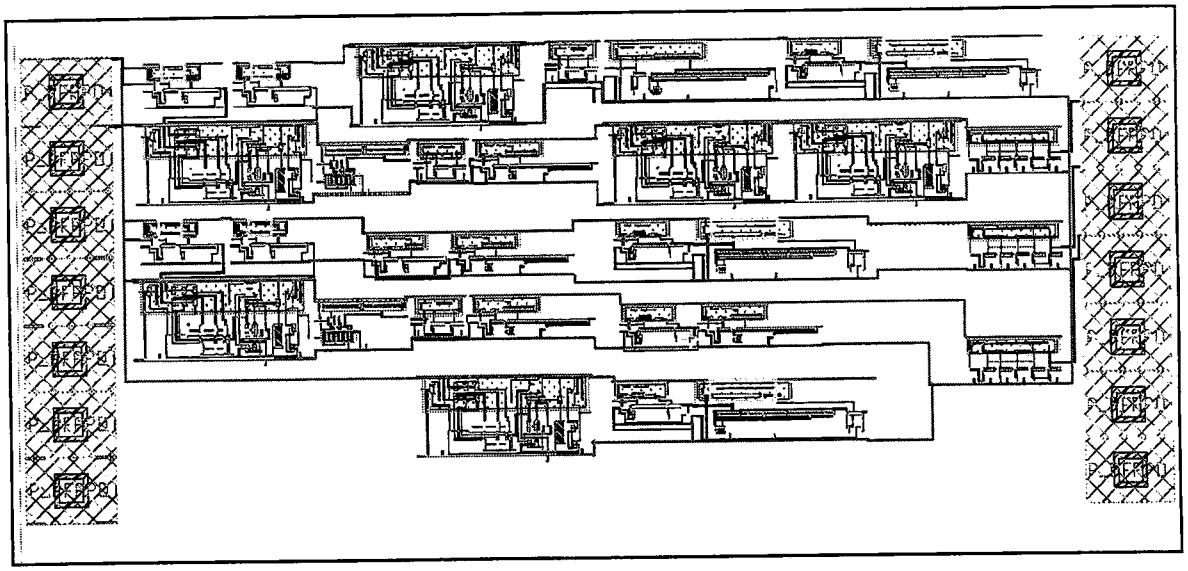

FIGURE C.4 Layout of the Complete System

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T.C. YÜK[illegible]URULU
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