ON OFF KEYING MODULATION/DEMODULATION AND ITS APPLICATIONS

by

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ABSTRACT

ON OFF KEYING MODULATION/DEMODULATION AND ITS APPLICATIONS

OOK based communication is getting more and more popular to reduce the power consumption of portable systems. Although OOK based communication requires less circuit complexity, high performance structures are needed. Most common methods used for OOK demodulation are envelope detection and production of the signal with itself. Envelope detection is simple with minimal power consumption meanwhile production usually requires mixers which requires much more power. This work provides design steps for various blocks in OOK communication based systems, especially demodulators. This work introduces two demodulator structures, one for 60 GHz pulse communication and the other for RFID tag chips. In addition, this work provides information about the systems as a whole as well as block based sections. Simulation and measurement results are provided when available.

ÖZET

AÇMA KAPAMA ANAHTARLAMA MODÜLASYON/DEMODÜLASYON VE UYGULAMALARI

OOK tabanlı iletişim sistemleri daha düşük güç tüketimi sundukları için gittikçe yaygınlaşmaktadır. Daha basit devreler ile gerçeklenebilmesine rağmen, yüksek performanslı yeni yapılara ihtiyaç duyulmaktadır. En yaygın demodülasyon türü olarak zarf süzgeci ve işaretin kendisi ile çarpılmasına dayanan yöntemler kullanılır. Zarf süzgeci son derece basit bir tasarım olup, güç harcaması da oldukça düşüktür. Buna karşın işaretin çarpımına dayanan sistemlerde ise karıştırıcıya ihtiyaç duyduğu için daha yüksek güç harcamasına sahiptir. Bu çalışma OOK tabanlı iletişim sistemlerinde kullanılabilecek bloklar için tasarım sürecini anlatmaktadır. Bu çalışmada biri RFID etiket diğeri 60 GHz bandında darbe haberleşmesine uygun iki adet demodulatör tanıtılmıştır. Blok bazında tasarımlara ek olarak sistem hakkında bilgiler sunulmuştur. Mevcut ölçüm ve benzetim sonuçları da paylaşılmıştır.

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LIST OF ACRONYMS/ABBREVIATIONS

ASK	Amplitude Shift Keying
EPC	Electronic Product Code
FSK	Frequency Shift Keying
LDO	Low-DropOut
MESFET	Metal Semiconductor Field Effect Transistor
MIIM	Metal Double Insulator Metal
MIM	Metal Insulator Metal
OOK	On Off Keying
PLL	Phase Locked Loop
POR	Power On Reset
PSTN	Public Switched Telephone Network
PTAT	Proportional to Absolute Temperature
RFID	Radio Frequency Identification
RTcal	Receiver to Transmitter Calibration
TRcal	Transmitter to Receiver Calibration
UWB	Ultra Wide Band

1. INTRODUCTION

Short range wireless communication is a growing need for household application and to be able to make each device communicate with each other easily and safely without the risk of data theft. 60 GHz band offers a great prospect in means of security and speed. As 60 GHz band offers a wide bandwidth as well as oxygen attenuation, there is a growing attention over 60 Ghz band over last decade.

In this study, a low power multi Gb/s pulse receiver is going to be implemented using 90 nm process for wireless communication. The aim is to produce designed chip and reach required specs for USB 3.0, blu-ray players etc. Another section of this work provides information about UHF RFID Class 1 Generation 2 tag chip. The chip will be designed in 180 nm process. This work will provide guidelines for several analog front-end circuits of tag chips.

Both systems will use OOK modulation which is a special type of ASK modulation. ASK is a form of modulation that represents digital data as variations in the amplitude of a carrier wave.

Any digital modulation scheme uses a finite number of distinct signals to represent digital data. ASK uses a finite number of amplitudes, each assigned a unique pattern of binary digits. Usually, each amplitude encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular amplitude. The demodulator, which is designed specifically for the symbol-set used by the modulator, determines the amplitude of the received signal and maps it back to the symbol it represents, thus recovering the original data. Frequency and phase of the carrier are kept constant.

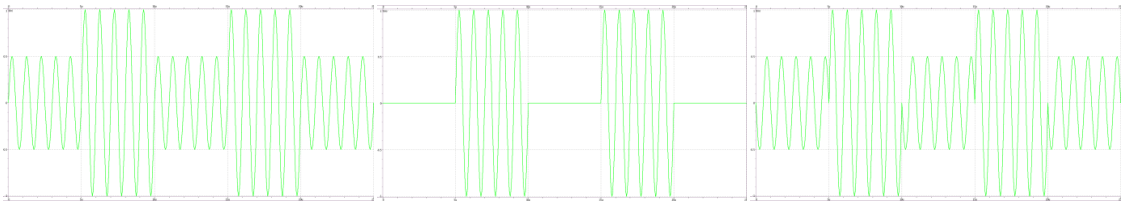
Like AM, ASK is also linear and sensitive to atmospheric noise, distortions, propagation conditions on different routes in PSTN, etc. Both ASK modulation and demodulation processes are relatively inexpensive. The ASK technique is also commonly used to transmit digital data over optical fiber. For LED transmitters, binary 1 is

represented by a short pulse of light and binary 0 by the absence of light. Laser transmitters normally have a fixed "bias" current that causes the device to emit a low light level. This low level represents binary 0, while a higher-amplitude lightwave represents binary 1.

ASK modulation, which is a digitalized version of AM, is a form of modulation that represents digital data as a variation of amplitude of a carrier wave. Main advantage of ASK modulation is, it provides simple demodulation schemes such as envelope detector which consists of a diode and an RC network. For more complex system there is also the product detector which has improved performance at the cost of additional circuit complexity and power consumption.

AM modulation is commonly used in radio communications where a carrier wave which is a sinusoidal has its amplitude varied by message signal. The message signal modifies the amplitude of the carrier wave and determines the envelope of the transmitted signal. In the frequency domain, amplitude modulation produces a signal with power concentrated at the carrier frequency and two adjacent sidebands. Each sideband is equal in bandwidth to that of the modulating signal, and is a mirror image of the other. This type of amplitude modulation is inefficient in power usage; at least two-thirds of the power is concentrated in the carrier signal, which carries no useful information.

The modulation index is defined as the change of amplitude in percentage to carrier amplitude. For example, 1V sinusoidal with 50% modulation index will vary between 1V and 0.5V while 100% modulation index will vary between 1V and 0V. Modulation index can exceed 100% which will cause a phase reversal at the signal which can be detected during demodulation.



%50 modulation index %100 modulation index %150 modulation index

Figure 1.1. Modulation Index.

The OOK modulation is a special form of ASK in which modulation index is 100% [1]. OOK is more spectrally efficient than FSK. Also the modulator simplicity of OOK modulator can surpass any other modulator. Furthermore, OOK modulator consumes less power compared to FSK as modulator does not transmit any wave during "0"s. Also on the demodulator side, OOK provides simple solutions for detection with much less power consumption and circuit complexity compared to FSK, as PLL structures are needed for FSK. On the other hand, OOK receiver sensitivity is equal to or better compared to coherent and non-coherent FSK.

Both for coherent FSK and OOK:

$$\mathrm{E} = \frac{\mathrm{A}^2 \mathrm{T_b}}{2} \tag{1.1}$$

where A is the amplitude while T_b is one bit interval. The average energy per bit divided by twice the channel noise density N_0 is:

$$\varepsilon = \frac{A^2 T_b}{4N_0} \tag{1.2}$$

Thus, for coherent FSK and OOK, the probability of bit errors P_e is:

$$P_e = \frac{erfc(\sqrt{\frac{\varepsilon}{2}})}{2} \tag{1.3}$$

while the probability of bit errors in non-coherent FSK is:

$$P_e = \frac{e^{\frac{-\varepsilon}{2}}}{2} \tag{1.4}$$

which is 1 dB poorer than coherent FSK and OOK [2].

To sum it up, probability of bit errors is comparable with FSK when using OOK based communication. However, OOK based communication can be achieved with much less power consumption. Therefore, pulse communications especially OOK systems are getting more and more popular in literature.

In this work, pulse communication systems are studied. Two different pulse communication systems are designed to prove the low-power suitability of OOK based systems. First one is a 60 GHz multi Gbps pulse receiver which uses a novel demodulator. The demodulator is studied both theoretically and in simulation environment and implemented in 90 nm technology. Measurement results are provided. The other system is RFID tag chip which will satisfy UHF RFID Class 1 Generation 2 standards. Block level design guidelines are provided for several blocks inside RFID tag chip.

2. 60-GHz MULTI GB/S PULSE RECEIVER

2.1. Introduction

Short range multi Gb/s wireless communication systems has been attracting attention. Because of the low-power nature of the pulse communication and 7.5 GHz-wide bandwidth available, the UWB pulse communication is suitable for realizing multi Gb/s wireless short-range data transfer applications such as downloading a DVD from a kiosk to a portable data storage device. Not only UWB but also 60 GHz band is also attracting much interest for realizing the multi Gb/s pulse communication. The 60 GHz band has a potential to provide higher throughput than UWB, because the 60 GHz band has approximately the same bandwidth but with a higher transmission power and less unwanted interference due to oxygen attenuation.

Receiver systems are core elements of wireless communication and there is a wide range of research about receivers at literature. Receiver structures are formed by several stages. First stage is usually a preamplifier or a front end filter with gain which is followed by the detector and then a driver or a digital buffer depending on the type of information received.

A 60 GHz pulse detector is an essential receiver building block of an impulse radio. There are several well-known conventional methods to build a pulse detector such as MIIM diode detector [3] or Schottky diode detector [4]. However, MESFET occupies a large area and Schottky diodes are not available in most of the standard design rules. In order to overcome these issues, CMOS compatible detectors are needed. In this work, the nonlinear detection property of a 60 GHz band multi-Gbps CMOS pulse detectors are studied and to analyze its millimeter-wave detector performance a complete millimeter-wave pulse receiver test circuit is implemented using 90 nm CMOS process technology.

2.2. Receiver Structure

The receiver will consist of five main parts: antenna, low-noise preamplifier, detector, limiting amplifier and digital buffer.

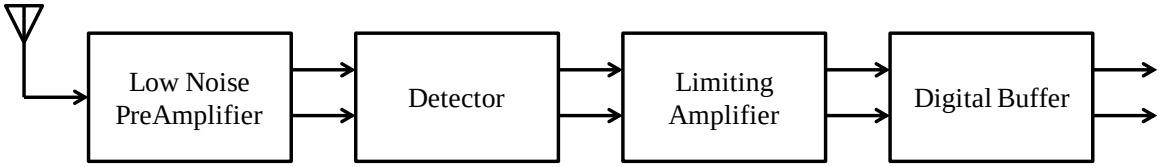


Figure 2.1. Receiver Structure Block Diagram.

The system will receive single ended signals with antenna. The signals will be at 60 GHz band for several reasons. 60 GHz band is license free and is highly secure because of O_2 absorption. As a result, 60 GHz band is a popular topic for research for short range wireless communication.

Antenna is followed by and low noise preamplifier stage with balun to generate differential signals from single ended antenna. Preamplifier stage is important to achieve enough range on wireless communication.

Preamplifier's output will then be given to detector in order to generate a small voltage difference at detectors output to be able to identify 1s and 0s. There are several ways to realise 60 GHz pulse detectors. However, the single-ended MESFET detector cannot be integrated on the silicon substrate with the receiver CMOS digital circuitry. The complete receiver system with MESFET occupies a large area. Instead of using an MESFET detector, the diode detector circuit which consists of a MIIM capacitor and Schottky diode. Since Schottky diode is unavailable in general design rules, using a non-linear amplifier as a detector would be both area and cost effective way.

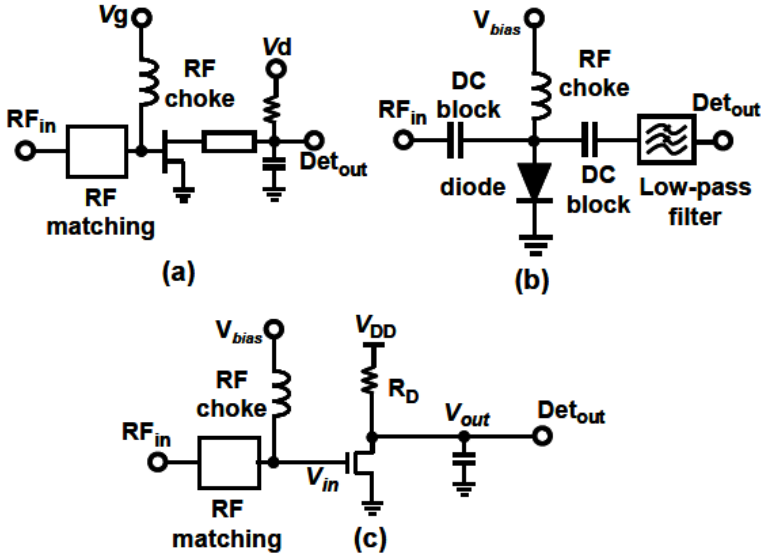


Figure 2.2. Detector Structures [5].

To convert small voltage difference generated by detector to a rail-to-rail signal to make it compatible with digital circuitry, limiting amplifier is used. Limiting amplifier is a cascade amplifier stage with high gain.

Then signals are digitized with a digital buffer to make system compatible with digital signal processing units. In the system designed there is no low-noise preamplifier to reduce power consumption.

2.3. Design of Receiver

The CMOS detector is the core of the multi-Gbps CMOS pulse receiver. The complete receiver requires impedance matching network, detector, limiting amplifier and a buffer. The block diagram of the system is given in Figure 2.3. The system receives 60 GHz millimeter-wave signals via antenna and applies to the input. The matching network, nonlinear MOSFET detector, a 60 dB limiting amplifier and a buffer is designed using 90 nm CMOS technology. While designing the layout, to reduce the parasitic components all building blocks are merged together. The detector provides a voltage difference at its output which is amplified further by the limiting amplifier and the digital buffer drives the high-speed off-chip loads.

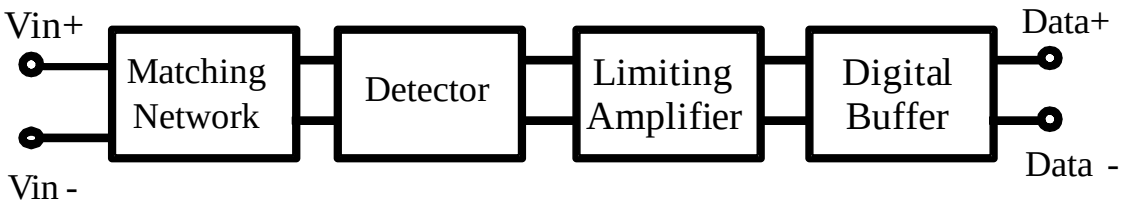


Figure 2.3. Block Diagram of the Receiver System.

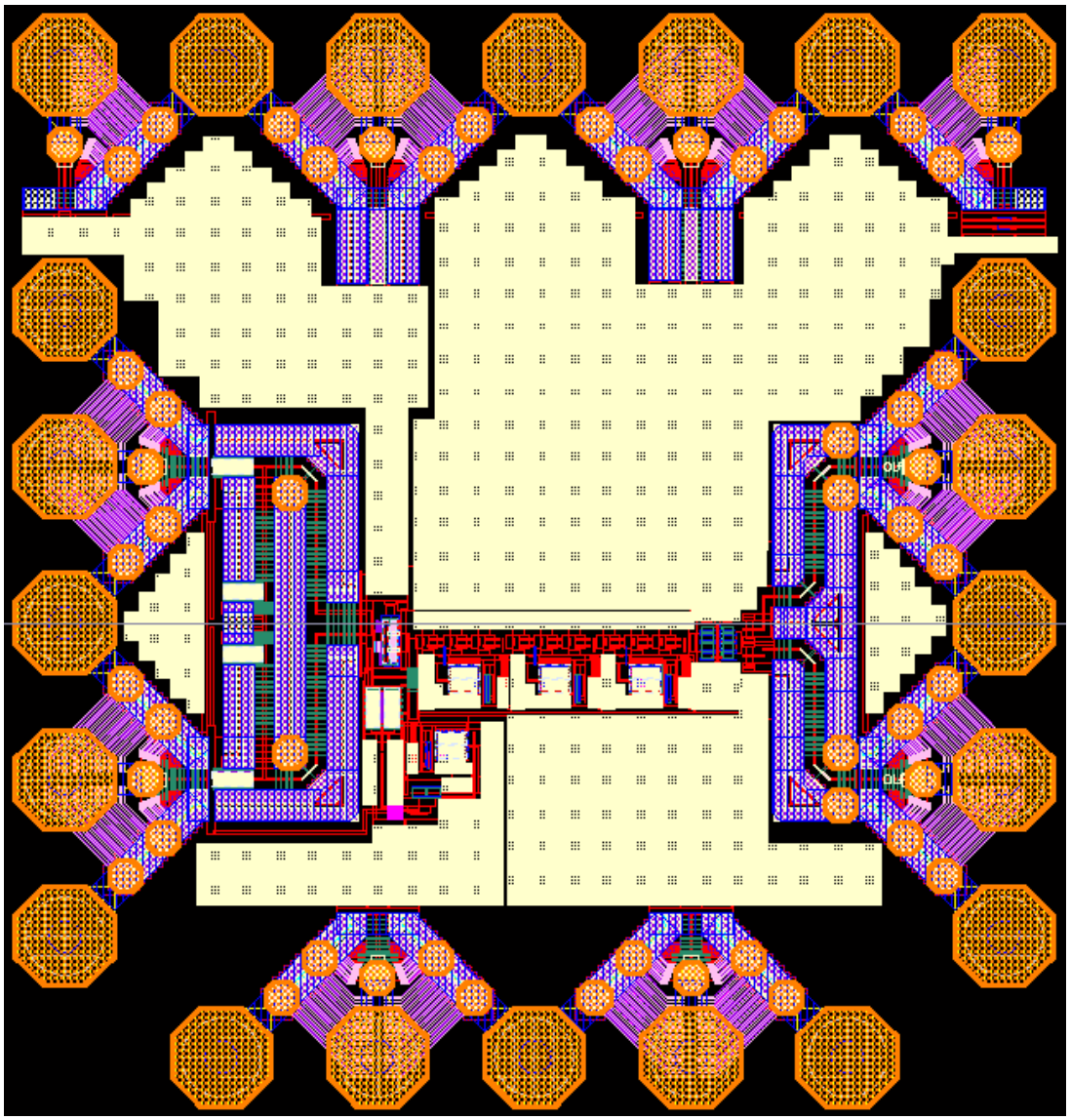


Figure 2.4. Chip Layout.

2.3.1. Matching Network

The matching network provides the impedance matching between the antenna and detector. A 50 Ω impedance matching network is designed using L type single shorted shunt-stub impedance matching method for M1 and M2 as shown in Figure 2.5. The node n shown in Figure 2.5 is a virtual ground for differential signals. Additionally the two shunt capacitors are reducing the node impedance. The matching network also provides DC bias to detector MOSFETs and isolates the biasing voltage from the front-end circuitry. A dummy matching network is not designed for M3-M4, not to increase chip area. The common mode noise is more effective at the baseband rather than millimeter-wave band. Therefore bias capacitances for M1-M2 and M3-M4 pairs are designed to be equal to 2C.

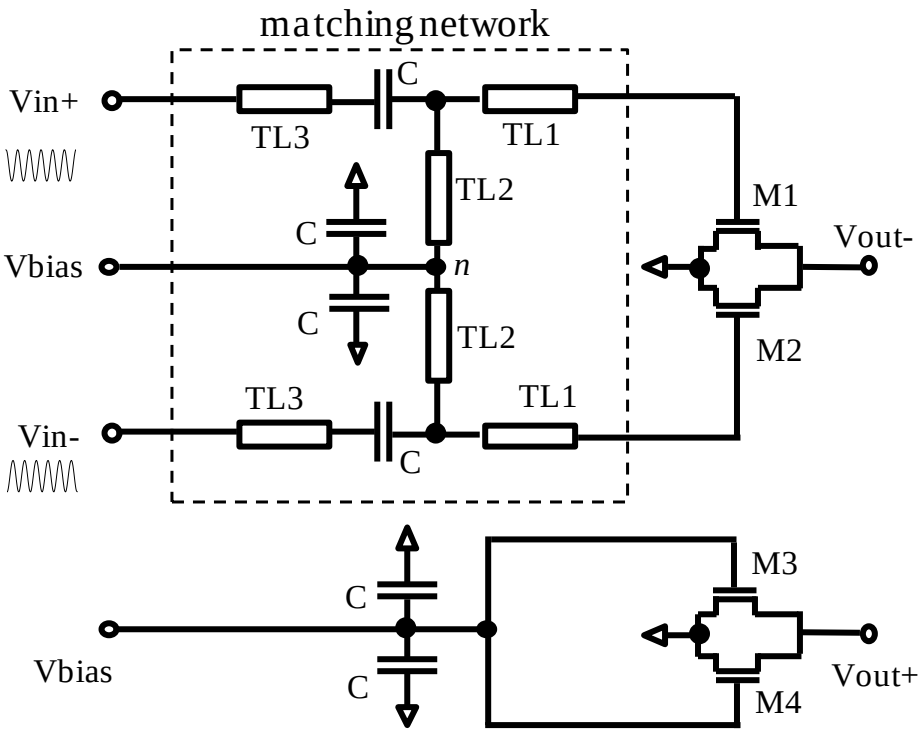


Figure 2.5. Matching Network.

The matching network is simulated using Cadence Spectre simulation tool. The lengths of TL1 and TL2 are 247 μm and 120 μm, respectively. The on-chip MIM capacitance C is equal to 311 fF. The S-parameter response is shown in Figure 2.6. A

61.5 GHz center frequency and 7 GHz bandwidth are obtained. As a result, the matching network can provide a 50 Ω input impedance for a wide bandwidth as desired.

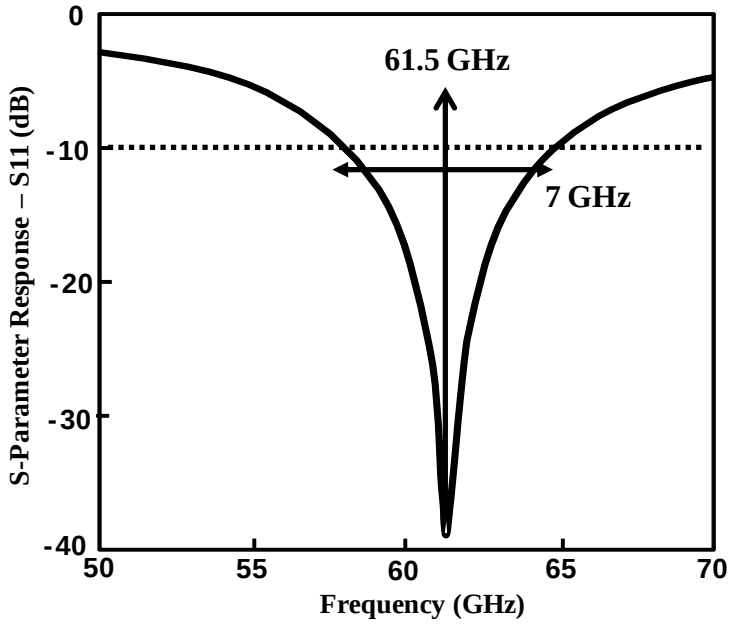


Figure 2.6. Simulated Return Loss of the Designed Impedance Matching Network.

2.3.2. Detector

The schematic of the studied CMOS pulse detector in [5], that is similar to a common-source amplifier, is shown in Fig 2.7. In many cases, nonlinear characteristics of MOSFET devices are undesired and attempted to be avoided using biasing. However, in this work the nonlinear characteristics of the MOSFETs are utilized to obtain a low-power multi-Gbps detector at 60 GHz millimeter-wave band.

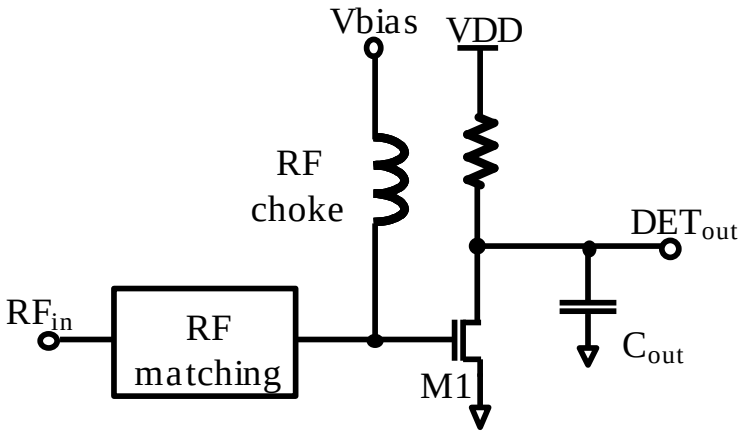


Figure 2.7. Schematic of Studied NMOSFET Millimeter-wave Pulse Detector [5].

As stated in [5], a drain shift current can be obtained which is proportional to derivative of g_m which is referred as g_{m2} and square of input voltage.

$$\Delta i_D = \frac{1}{4} g_{m2} A^2. \tag{2.1}$$

As a result, the drain current shift is proportional to g_{m2} and A^2. Based on this evidence, drain current, g_{m1} and g_{m2} characteristics of NMOSFET are analyzed and its results are shown in Figure 2.8. Nonlinearity caused by g_{m2} is predominant at low-gate voltages. This is an expected outcome due to sub-threshold and weak inversion regions of I_{DS}-V_{GS} relationship.

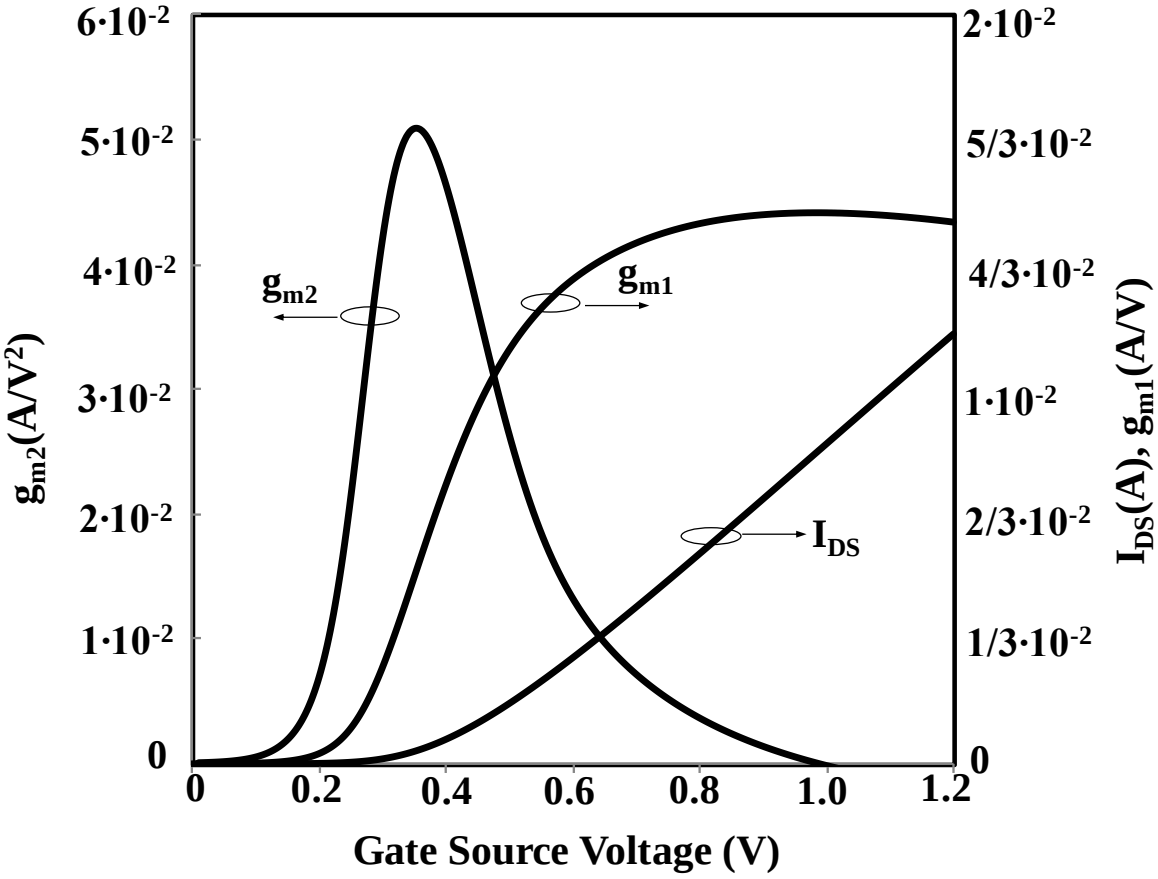
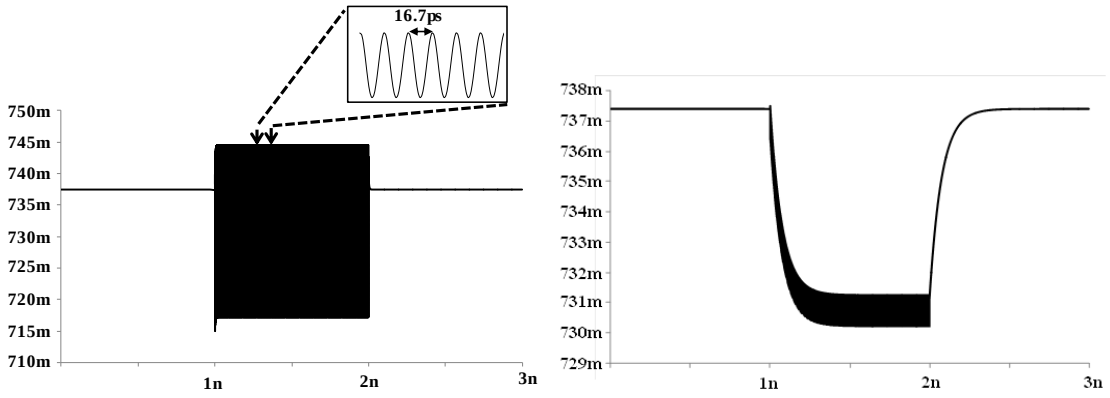


Figure 2.8. I_{DS}, g_{m1} and g_{m2} Characteristics with respect to V_{GS}.

In order to analyze the time domain response of the proposed detector, transient simulations are conducted. During simulations, the detector provided a shift in DC to prove its detection characteristics shown in Figure 2.9a. If the output capacitance of the detector is considered, it comprises a low-pass filter. The capacitance filters out high frequency components such as the fundamental and 2nd harmonic terms, as a result only the envelope signal appears at the output shown in Figure 2.9b. In the following section the design and CMOS implementation of the proposed detector is discussed.



(a) (b)

Figure 2.9. The Simulated Output of the Detector (a) without (b) with Output Capacitor.

The schematic of the detector is given in Figure 2.10. M1-M2 pair provides a nonlinear detection characteristic while M3-M4 pair is a dummy circuitry and M5-M6 pair with R1 and R2 resistors operate as an active balun.

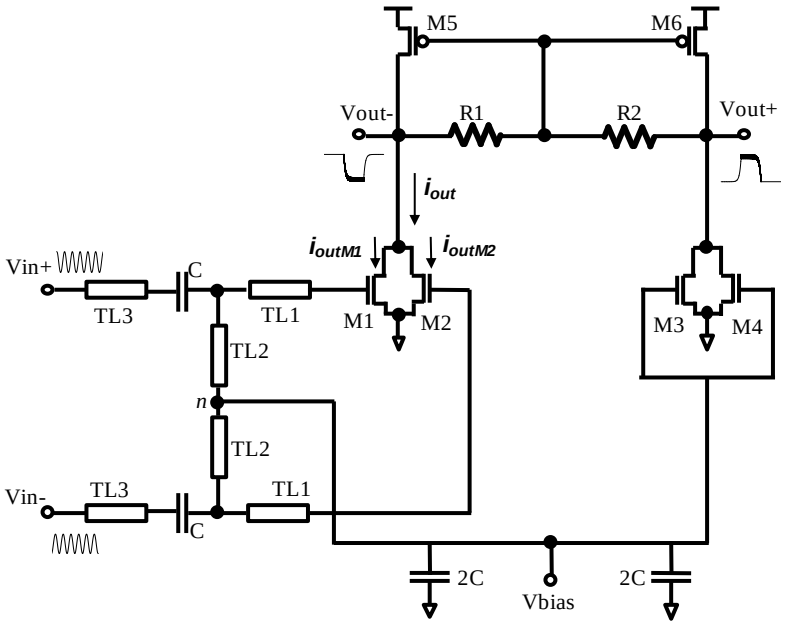


Figure 2.10. The Schematic of the Designed 60 GHz CMOS Detector with Matching Network.

When a differential RF signal is applied to the M1-M2 pairs, such that $Vin_{+}=A\cos(\omega t)$ and $Vin_{-}= -A\cos(\omega t)$, and g_{m1} and g_{m2} values for M1 and M2 transistors are identical due to the symmetric design, then the output current shift will be

$$i_{outM1} = g_{m1} A\cos(\omega t) + \frac{1}{2} g_{m2} (A\cos(\omega t))^2 \tag{2.2}$$

$$i_{outM1} = g_{m1} A\cos(\omega t) + \frac{1}{4} g_{m2} A^2 + \frac{1}{4} g_{m2} A^2 \cos(2\omega t) \tag{2.3}$$

$$i_{outM2} = -g_{m1} A\cos(\omega t) + \frac{1}{2} g_{m2} (-A\cos(\omega t))^2 \tag{2.4}$$

$$i_{outM2} = -g_{m1} A\cos(\omega t) + \frac{1}{4} g_{m2} A^2 + \frac{1}{4} g_{m2} A^2 \cos(2\omega t). \tag{2.5}$$

As the drains of the M1-M2 pair are connected together, the fundamental and odd components of the currents will be canceled out and only baseband and even harmonics are amplified. The combination of i_{outM1} and i_{outM2} will be

$$i_{out} = \frac{1}{2} g_{m2} A^2 + \frac{1}{2} g_{m2} A^2 \cos(2\omega t). \tag{2.6}$$

Because of the capacitances at the output node, 120 GHz terms will be heavily attenuated at the output and only the baseband term remains.

M3-M4 pair provides the same quiescent current with M1-M2 pair to prevent offsets while the active balun makes the baseband signal differential. All M1-M2-M3-M4 transistors are designed to have a common centroid layout. The CMOS detector is designed as compact as possible with the active balun, not only to minimize the detector area but also to reduce the common mode noise coming from the silicon substrate where all active circuit elements are fabricated [6].

As it can be seen from equation 2.6, the CMOS nonlinear amplifier discussed in [5] is further improved with this structure not only in terms of detection capabilities but also mismatch immunity. The shift in drain current is now doubled compared to previous work. On the other hand, circuit is now less susceptible to mismatch because of differential pair input, the dummies and active balun introduced in this work.

Detector designed is a differential input envelope detector with an active balun to generate differential output and has dummy circuitry to not cause systematic offsets. In order to reduce offsets further, an active feedback loop is designed to eliminate offsets.

After finishing schematic based simulations, layout of the given circuit is made. The loop amplifier and bias generator layouts are given below. Layout was made in 90 nm process using Cadence Virtuoso XL.

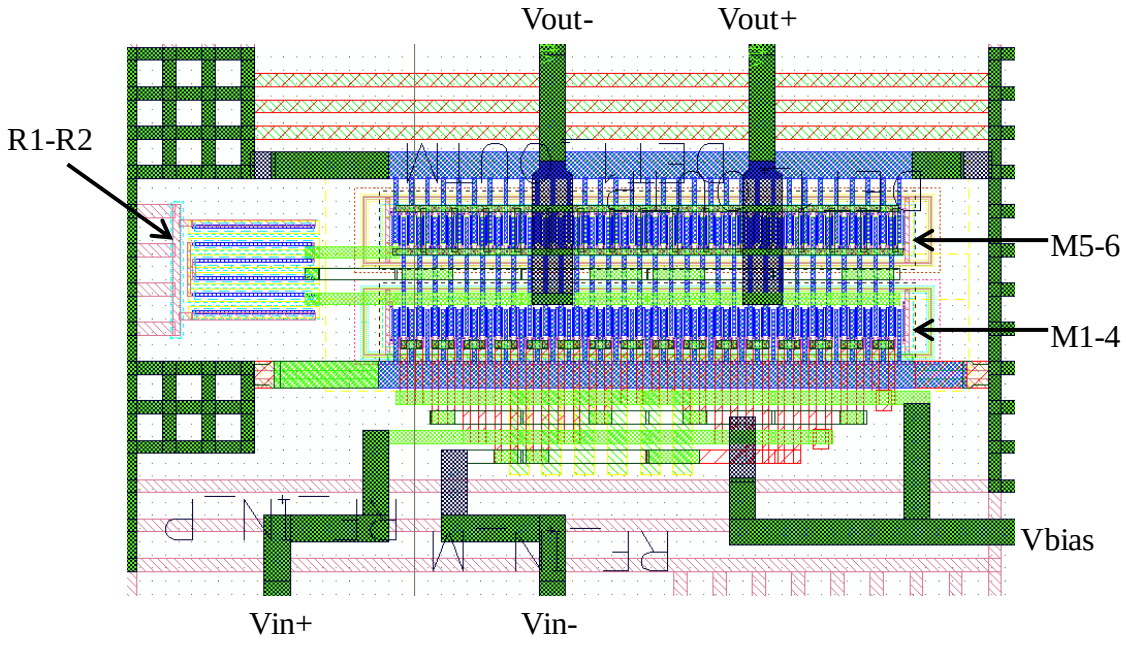


Figure 2.11. Detector Layout.

2.3.3. Limiting Amplifier

The 60 GHz fully differential limiting amplifier is a prior design for millimeter-wave wireless communication. As shown in Figure 2.12, limiting amplifier a chain of amplifiers with feedback loops to avoid saturation from DC mismatches which can be caused by offsets and low frequency noise factors.

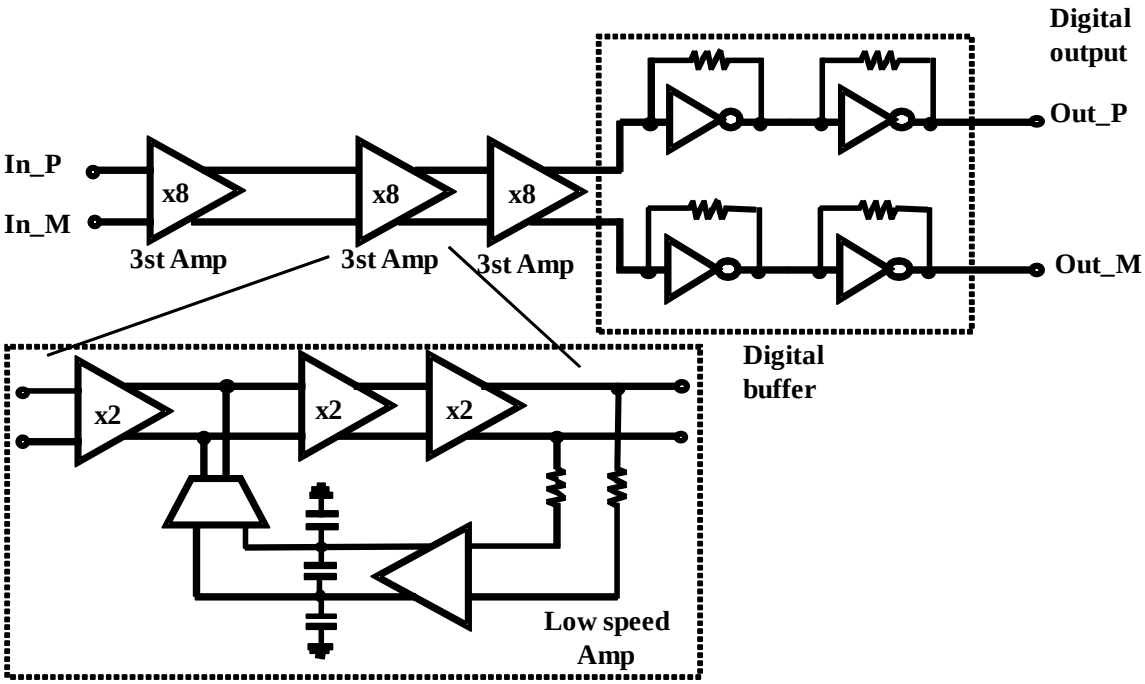


Figure 2.12. Limiting Amplifier System Diagram.

The gain unit is three stage amplifiers with a feedback loop. Feedback loop provides stable DC operating points for high gain amplifier stages. Then gain units are cascaded to provide a gain of 60 dB for baseband frequency range which is between several MHz and several GHz as shown in Figure 2.13.

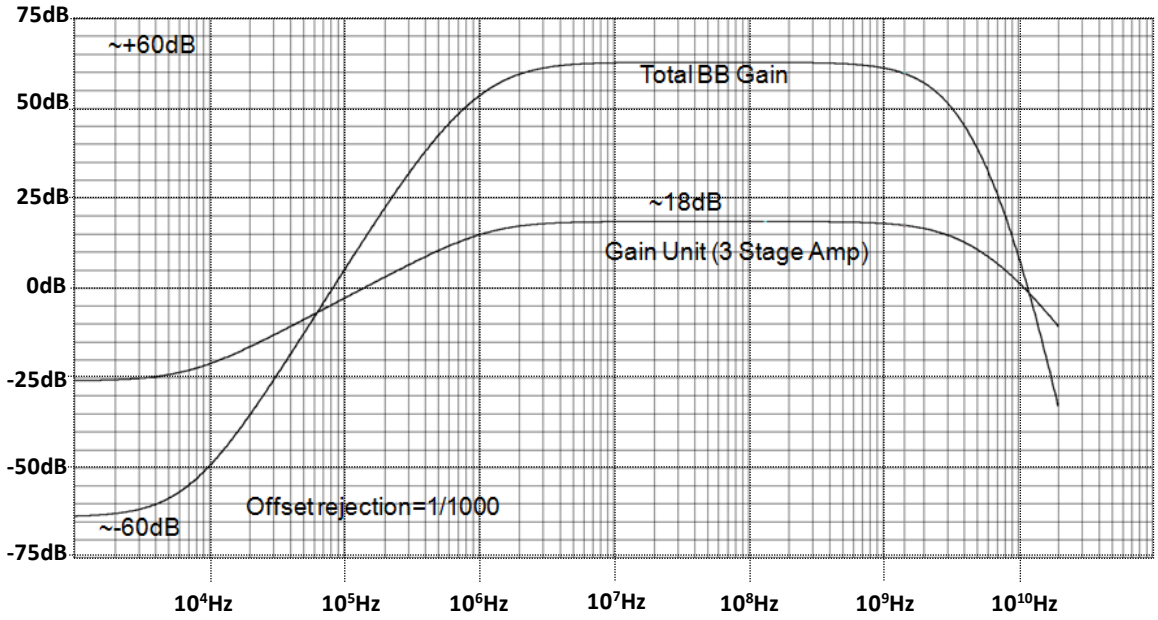


Figure 2.13. Limiting Amplifier Frequency Response.

2.4. Simulations

Simulations are run on Virtuoso Analog Design Environment. In order to characterize the circuitry, several simulations are to be made. To measure input sensitivity for different level of input power, output voltages of the differential output detector are measured.

For this purpose, for an input power level transient simulations are run for a long enough time and then parametric sweeps are made to provide more data points for input power versus output voltage graph.

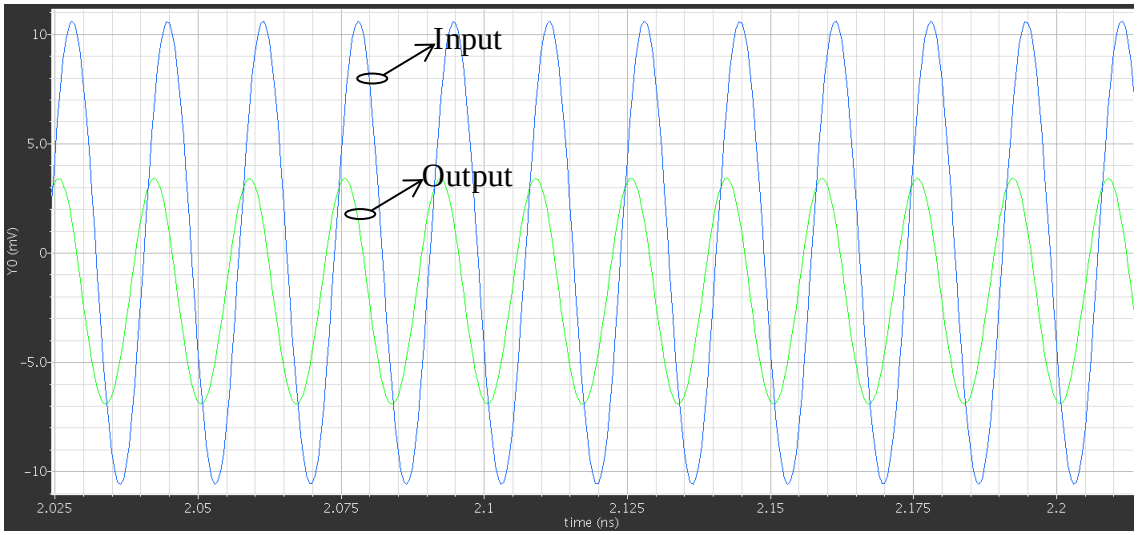


Figure 2.14. Detector Input and Output.

Figure 2.14 represents the output of detector in green while the input power is -30 dBm which is in blue. As it can be seen detector can cover 60 GHz signals.

The coverage of 60 GHz by detector is important however as detector is an envelope detector, it generates an envelope at its output and this envelope must be observed.

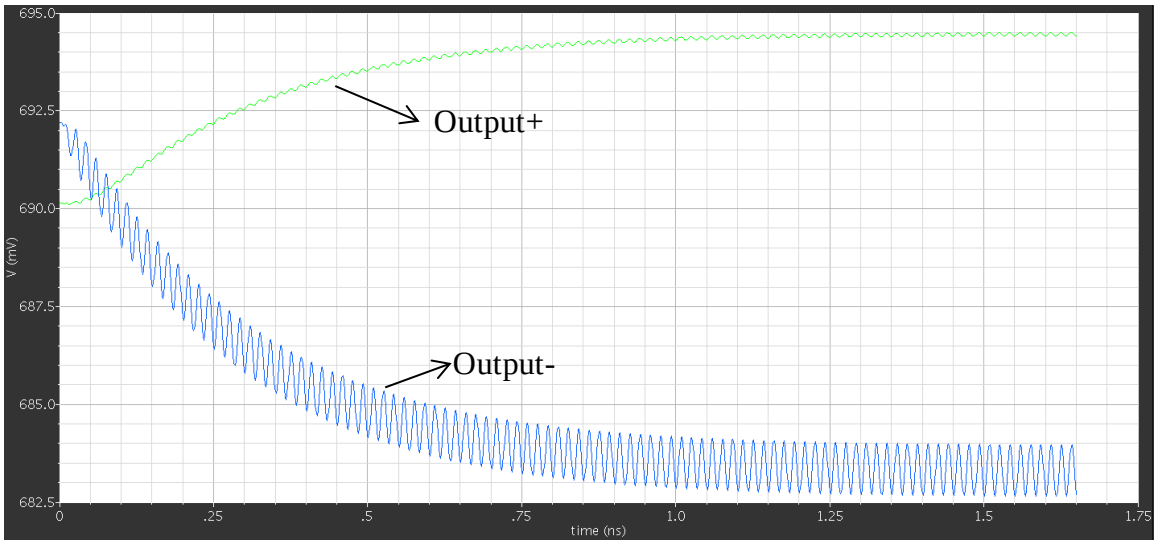


Figure 2.15. Envelope Generated by Detector.

Figure 2.15 represents the envelope generated by detector when logic “1” with input power of -30 dBm is received. As it can be seen the voltage difference between positive and negative output is around 10mV. This 10mV difference at the output is then made rail to rail using limiting amplifier.

The voltage difference between envelopes can be acquired by running simulation for a long time and then taking the average of outputs. To provide this information parametric sweeps are made which had run for several hours.

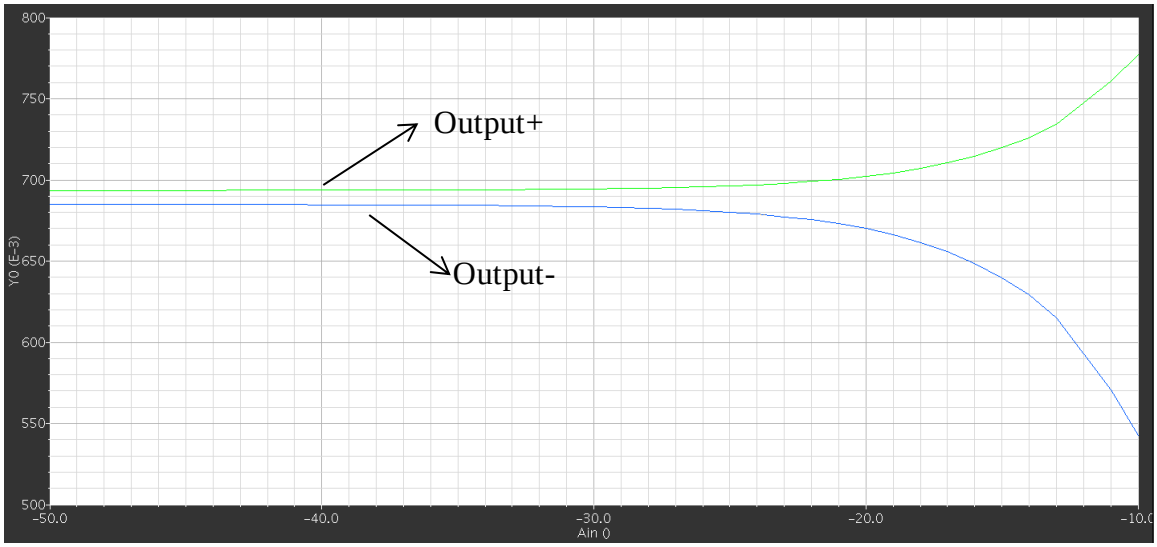


Figure 2.16. Output Voltages of Detector versus Input Power.

As it can be seen from Figure 2.16, the envelopes are getting larger with increasing input power which is in terms of dBm. For inputs with low power, the output of detector is almost flat and then increases rapidly. As there is a quadratic relationship between the envelope and input voltage, this result was expected.

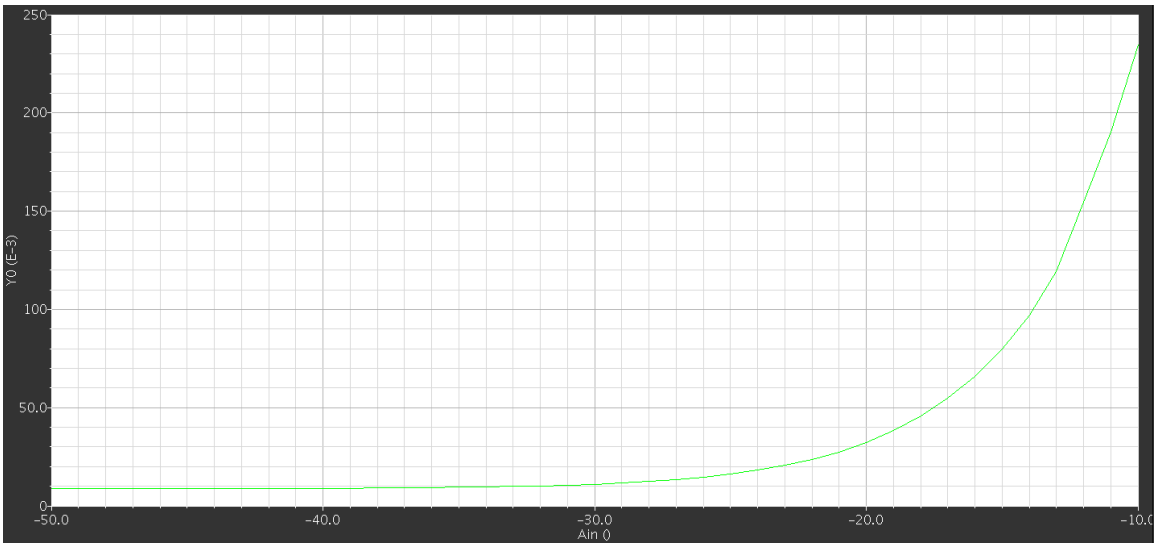


Figure 2.17. Difference between Output Voltages of Detector versus Input Power.

Figure 2.17 is a natural result of Figure 2.16. This difference between outputs will be amplified by limiting amplifier, generating logic output.

2.5. Measurement and Discussion

The chip is fabricated using a 90 nm CMOS process technology. The active circuit area of the chip occupies 250 µm × 450 µm. Figure 2.18 shows the micrograph of the fabricated chip. The fabricated chip was tested using on-chip probe station. Limiting amplifier and CMOS Buffer in the circuit is supplied with a 1.2 V power supply and total 21.4 mA supply current is measured.

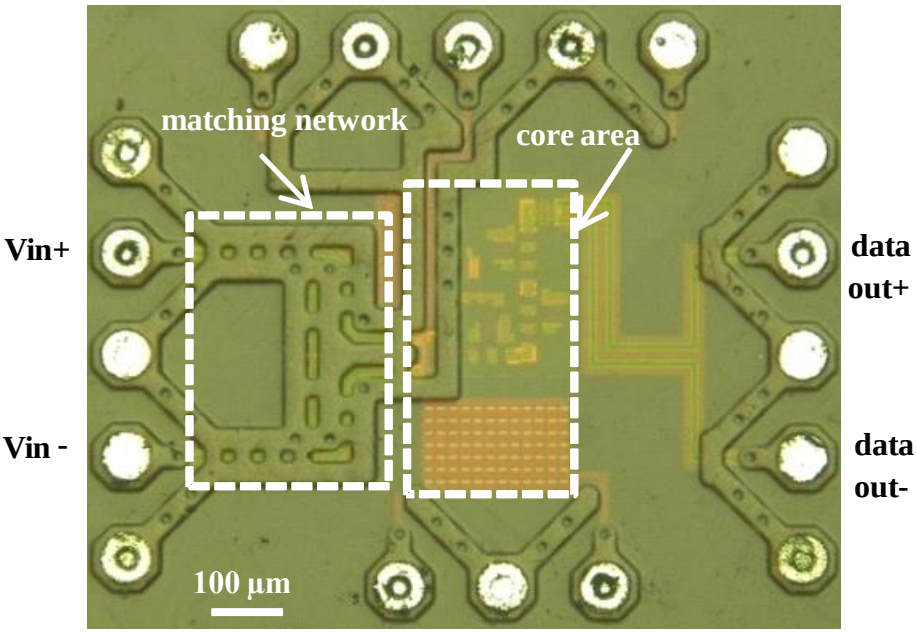


Figure 2.18. Fabricated Chip Micrograph.

A $2^{31}-1$ bits long pseudo random 60 GHz band millimeter-wave on-off keying pulses are applied to the input of the receiver. While applying the multi-Gbps millimeter-wave pulses, the digital output waveform and eye diagram are measured using a sampling oscilloscope, and bit-error rate performance is measured using a bit-error-rate tester. Clear eye diagrams are observed up to a data-rate of 3 Gbps that is shown in Figure 2.19.

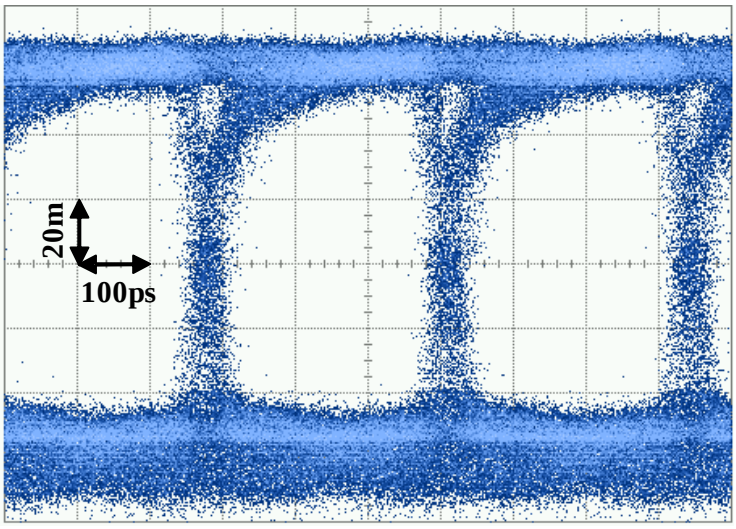


Figure 2.19. Eye Diagrams of Receiver for 3 Gbps Data Rate.

Input sensitivity for 2 and 3 Gbps are determined by measuring bit-error-rate performance with respect to input RF power. The input sensitivity of the fabricated circuit is −26 dBm for 2 Gbps and −22 dBm for 3 Gbps with a BER of 10^{-6} which could be seen in Figure 2.20. The total power dissipation of the entire chip is measured to be 29 mW while only 1.6 mW of this is consumed by active pair of detector, another 1.6mW consumed by dummies and rest being consumed by limiting amplifier and CMOS buffer.

It is seen that 60 GHz pulse communication is promising for low-power, short-range multi-Gbps wireless communication. While designing the proposed receiver, a fully differential architecture and common centroid layout techniques are adopted to reduce common mode noise. Additionally, an on-chip 60 GHz band matching circuitry has been implemented to reduce the reflection loss due to mismatching. As a result, this work shows better sensitivity performance than similar kind of low-power receivers [7-10].

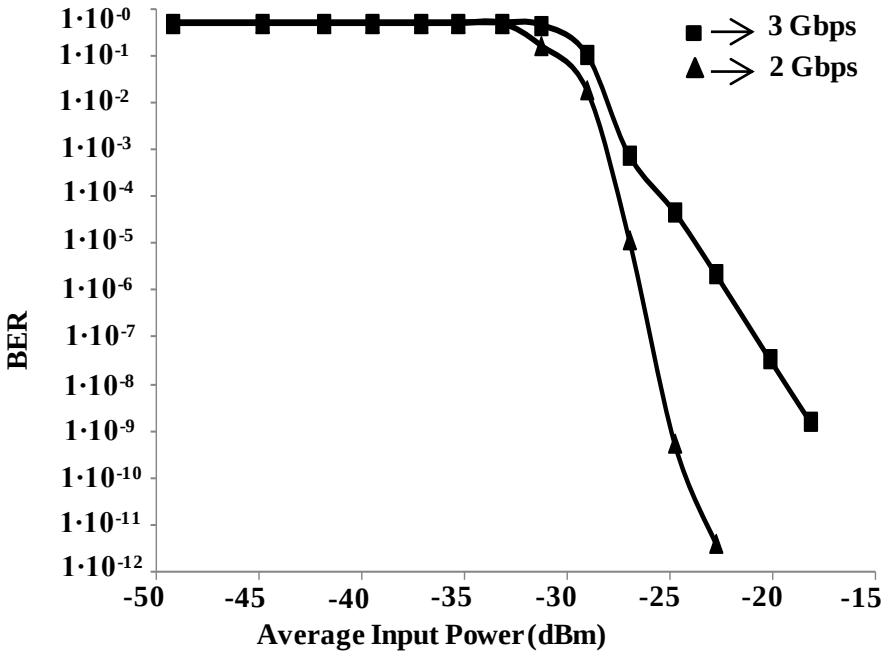


Figure 2.20. BER versus Average Input Power.

According to measured data-rate and sensitivity, we expect that this receiver circuit can provide 3 Gbps data-rate up to 4 cm wireless communication distance with the power consumption of 29 mW. In this scenario, it is assumed that the transmitter can provide

0 dBm RF pulses, total a 3 dB interconnection loss exists and 10 dBi antenna gains are available in both transmitter and receiver parts. If longer transmission distance is required, the proposed detector can be connected to the differential ended millimeter-wave front-end circuits such as differential ended low-noise amplifier to improve the sensitivity [11-13] or more powerful RF pulses can be transmitted from the transmitter.

If this receiver circuit was supplied by a typical 2900 mAh capacity AA size battery, it could receive 3 Gbps wireless data up to 120 hours. The energy per bit consumed during data transmission is as low as 9.6pJ/bit. We expect that this millimeter-wave pulse receiver circuit is promising for high-speed and short-range data transfer applications such as wireless digital kiosks.

3. RFID TAG

3.1. Introduction

RFID is using radio frequency electromagnetic fields to communicate with a tag which is attached to an object to either track or identify the object. RFID tags are specific to application in order to provide better performance. The most commonly used RFID tags, shown in Figure 3.1, have no battery and harvest energy from RF waves sent by the interrogator. Unlike barcodes, RF tags do not depend on line of sight communication and can be implemented in the object to identify. These features enable RFID to be used in various different applications [14, 15].



Figure 3.1. RFID Tag.

The designed tag will satisfy the Class 1 Generation 2 UHF RFID tag standards. The project is carried out in Gate Electronics with codename Melisa and consists of three main blocks. These three main blocks are analog part, digital block and nonvolatile memory. The analog part is designed in firm meanwhile the digital circuitry is synthesized by contractors. The memory is AEON/MTP RFID which is licensed from Synopsys. This section will mainly cover blocks designed by the author.

3.2. Structure of RFID Tag

RFID tag is a transponder which receives commands from interrogator, executes them and then provides a reply. In addition to all these, tag itself harvests its own energy from RF waves. Tag needs all these functional units collected to satisfy standards.

Rectifier has three stages two of which provides supply for analog circuitry meanwhile the final third supplies memory which requires a higher supply voltage. The demodulator provides interrogator to tag data for the baseband processor meanwhile modulator uses backscattering to enable tag to interrogator communication. Bandgap and LDO provide a stable voltage for baseband processor and oscillator such that logic delays are kept in range.

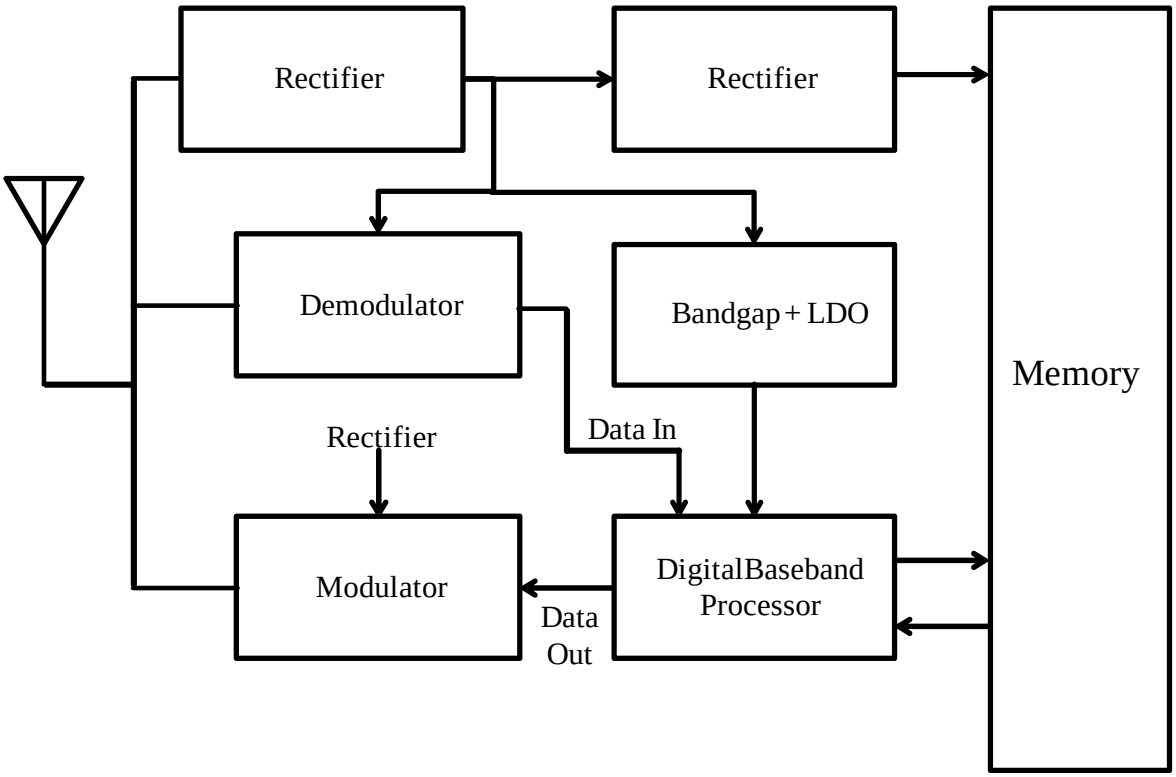


Figure 3.2. Structure of RFID Tag.

The main purpose of tag is to provide its EPC to interrogator. The main differences between tag chips are their minimum read and write sensitivities. To have a higher sensitivity, tag needs a higher power convergence efficiency and lower power consumption. Therefore, main design consideration in all analog blocks is to have simple circuitry with low power consumption.

3.3. Design and Simulations of RFID Tag

3.3.1. Demodulator

The demodulator is the circuitry that extracts data from RF waves. There are two main demodulation approaches for ASK modulated signals which are multiplication based and envelope detection based [16-18]. The prior project 60 GHz pulse receiver uses a multiplication based detector, mainly because of the high data rate and high frequency carrier. The RFID tag uses an envelope detection based demodulator, because of the low power nature of passive elements and need of less complex circuitry.

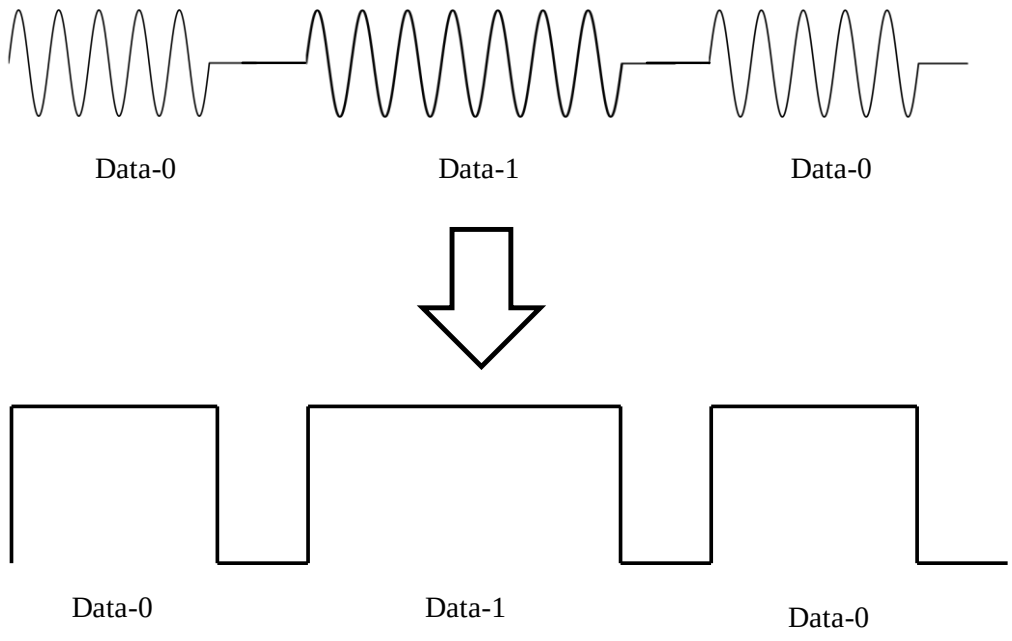


Figure 3.3. Function of demodulator.

The demodulator consists of an envelope detector, a low pass filter and a comparator. The envelope detector is formed from a diode connected NMOS and a parallel RC network that extracts the envelope of the input RF waves. The output of envelope detector is then applied to low pass filter to obtain a delayed version of the envelope. The comparator compares these two outputs and detects the rising and falling edges of RF waveform, therefore demodulates the input data.

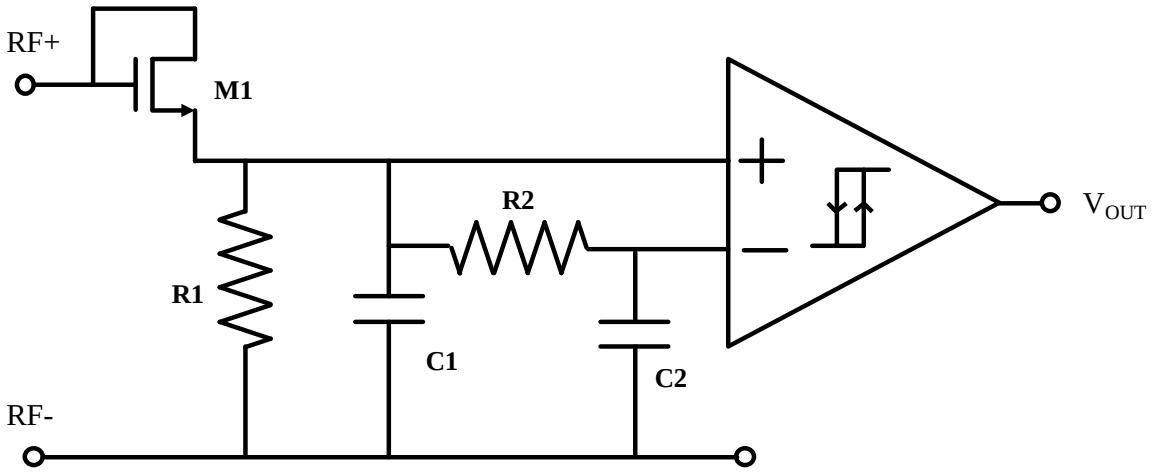


Figure 3.4. Schematic of Demodulator.

The realization of envelope detector is done with M1, R1 and C1 which has a time constant of 76nS. The highest message band of RFID signal is 160 kHz and its period is 6.25µs. This relatively low time constant allows envelope detector to track the changes in the RF envelope simultaneously. The low pass filter is realized by R2 and C2 and their time constant is 920ns which is more than a decade larger than the envelope detector's. Because of this difference, the low pass filter provides a delayed version of the envelope as mentioned before. The RF input and blocks respective outputs are given below in Figure 3.5.

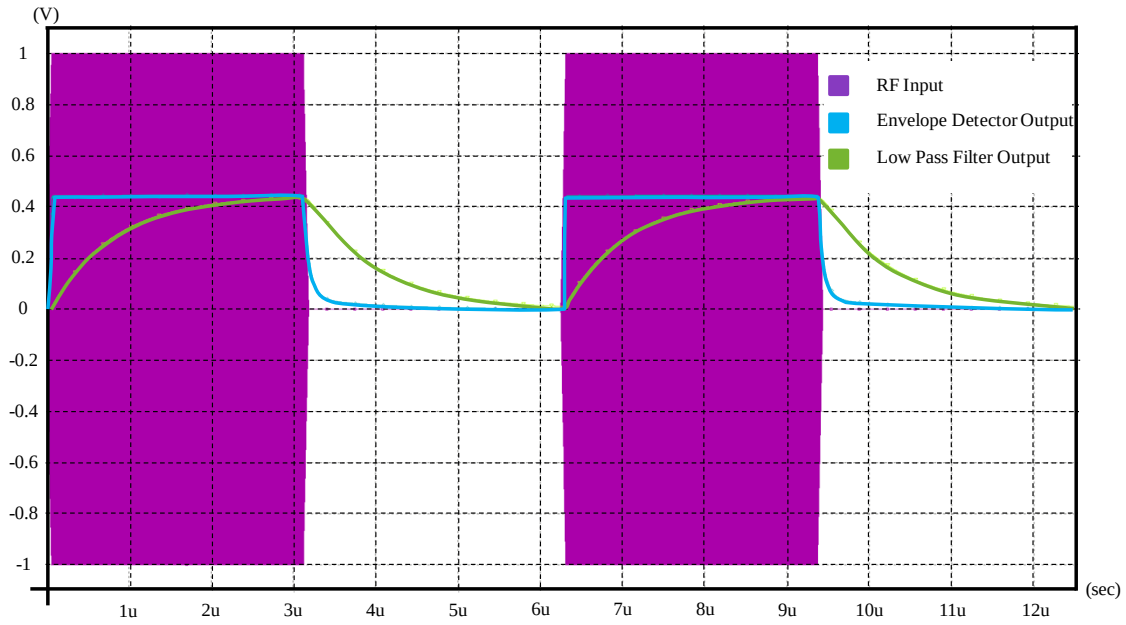


Figure 3.5. RF Input, Envelope Detector and Low Pass Filter Output.

The time interval which envelope detector output and low pass filter become inseparable, the comparator is more susceptible to noise. To avoid an oscillation at comparator output and provide stable comparator output, a hysteresis property is needed at comparator.

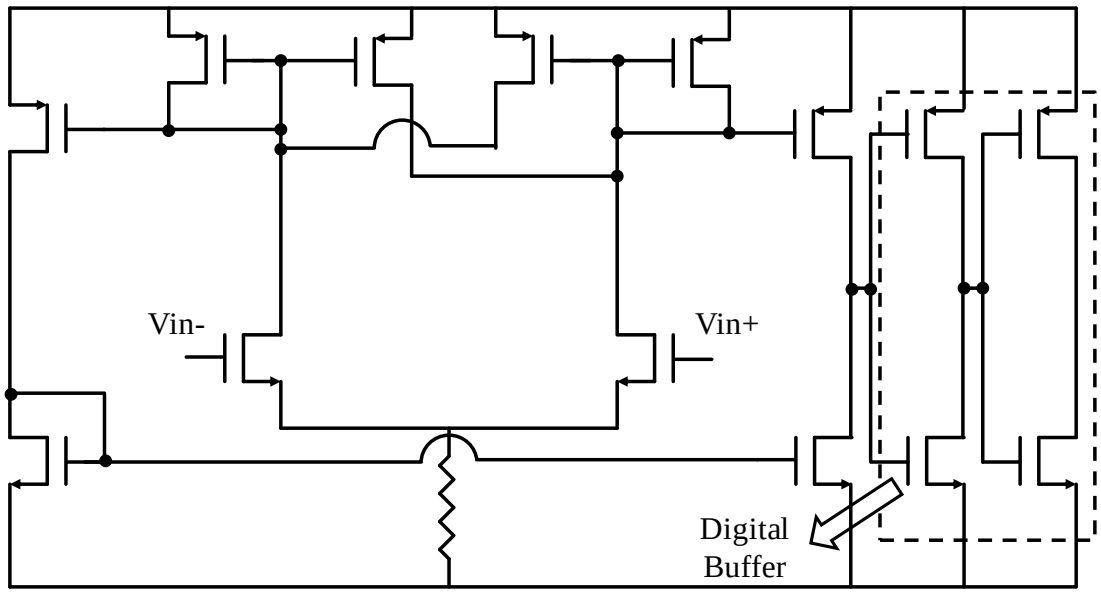


Figure 3.6. Comparator with Hysteresis.

The schematic of comparator with hysteresis is given in Figure 3.6. The cross coupled transistors provide a positive reaction for the circuit, which prevents output changing its state for small voltage differences at input. In order to change the output of the comparator, the voltage difference must exceed a certain threshold which is defined as:

$$V_{th} = \sqrt{\frac{2I_{tail}}{\mu_p C_{OX}(W/L)_{M1,2}(1+\alpha)}}\left(1-\sqrt{\alpha}\right) \tag{3.1}$$

The UHF RFID Class 1 Generation 2 standards have chip power-up sequence of 2ms, followed by several well-defined signals such as delimiter, RTcal and TRcal. The delimiter is sent as a low signal which forces demodulator output to be at logic "1" state to change its state from high to low and then low to high in order to let baseband processor count delimiter.

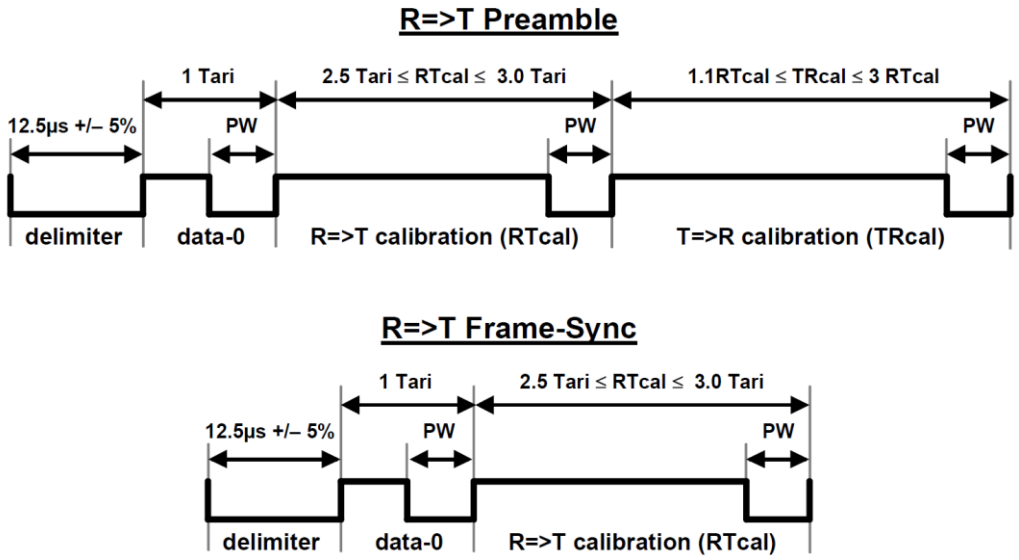


Figure 3.7. R=>T Preamble and Frame-sync.

Although for typical cases of power-up demodulator output can be assumed to set at "1", it is not true for low power cases due to the fact of low supply voltage. At lower power inputs, it usually takes up a long time before the supply is high enough to enable

comparator work properly. However, inputs of comparator can settle much faster and are equal to each other when supply becomes available which results in an uncertainty about the demodulator output. In order to solve this issue, POR signal is used to set demodulator output at "1" when supplies become stable.

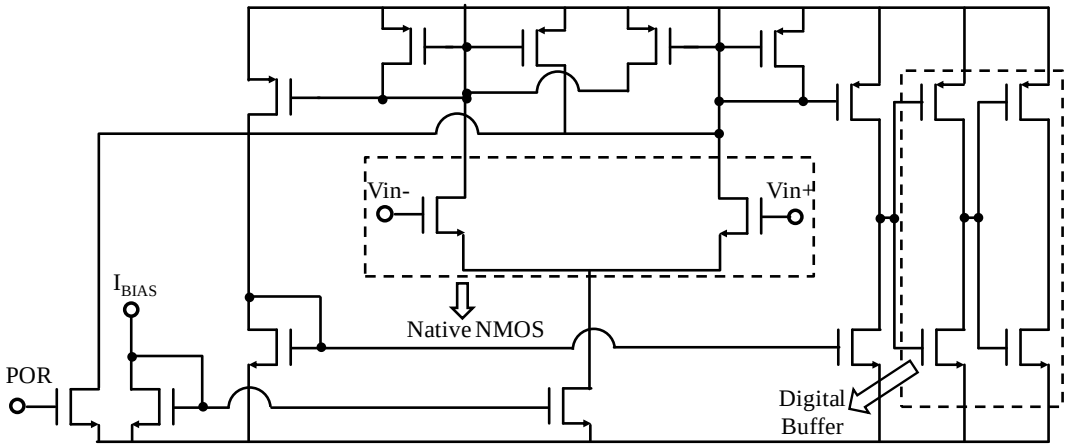


Figure 3.8. Schematic of Proposed Comparator.

Using a single NMOS transistor with high threshold voltage, the inner node is pulled down. Positive feedback inside comparator holds the node pulled down, which assures the demodulator output stays at logic "1" till the delimiter signal is received.

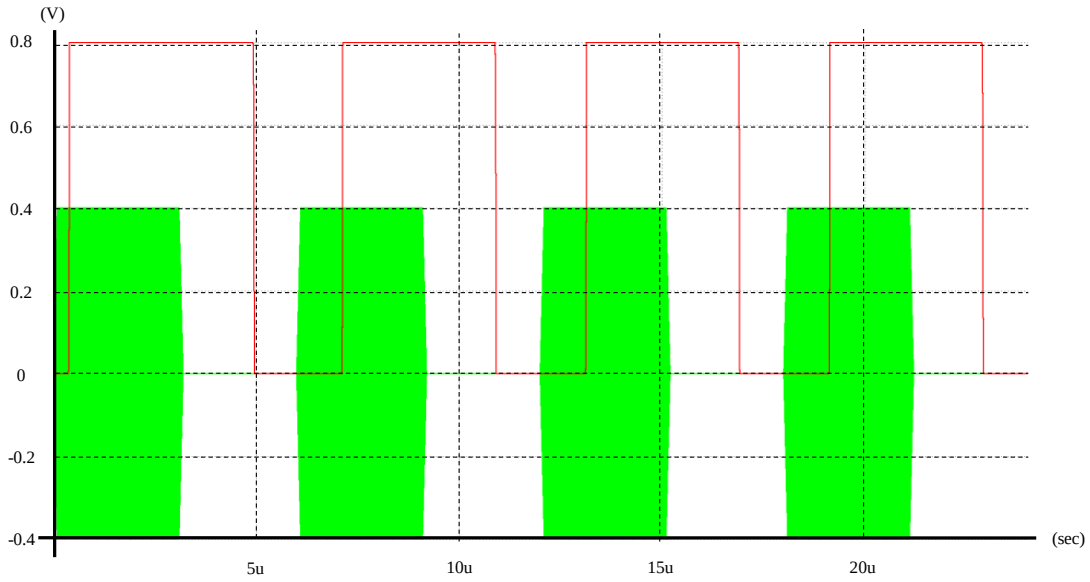


Figure 3.9. RF Input versus Demodulator Output.

The demodulator has a static power consumption of 600nA from 900mV supply meanwhile simulated dynamic power consumption is around 600nW.

3.3.2. Bandgap

Voltage reference is required for power supply voltage regulation in IC. Due to low-power nature of RFID, the bandgap voltage reference must consume low power while providing a constant voltage. Most conventional bandgap voltage references make use of an op-amp to equalize gate-source voltages of MOSFETs with different area [19]. In order to decrease the power consumption of bandgap circuit, MOSFETs are used in subthreshold region and a bandgap voltage reference without op-amp is selected. The schematic of the circuit is given in Figure 3.10.

The current mirrors at top provide the same drain current for M1, M2 and M3. The VGS difference is applied on R1 to generate a PTAT current. Then this current is fed into M3 and R2 to provide a zero temperature coefficient voltage reference.

$$I_{D1} = I_{D2} = I_{D3} = I_D \tag{3.2}$$

$$V_{GS1} = V_{GS2} + I_D R_1 \tag{3.3}$$

The subthreshold voltage-current relationship of a MOSFET can be expressed as $I_D = I_S e^{\frac{V_{GS}}{nV_T}}$. If it is applied to equation 3.3 and simplified the result will be

$$I_D = \frac{nV_T \ln(A)}{R_1} \tag{3.4}$$

where A is the ratio of device areas and n is subthreshold slope. This PTAT current is fed into R2 and M3 to generate a voltage.

$$V_{BG} = I_D R_2 + V_{GS3} \tag{3.5}$$

Gate to source voltage of a diode connected NMOS device is complementary to absolute temperature which makes it possible to obtain a zero temperature coefficient for a specific R2 value. Temperature coefficients of I_D and V_{GS} are 1.35 nA/K and -950µV/K at room temperature respectively.

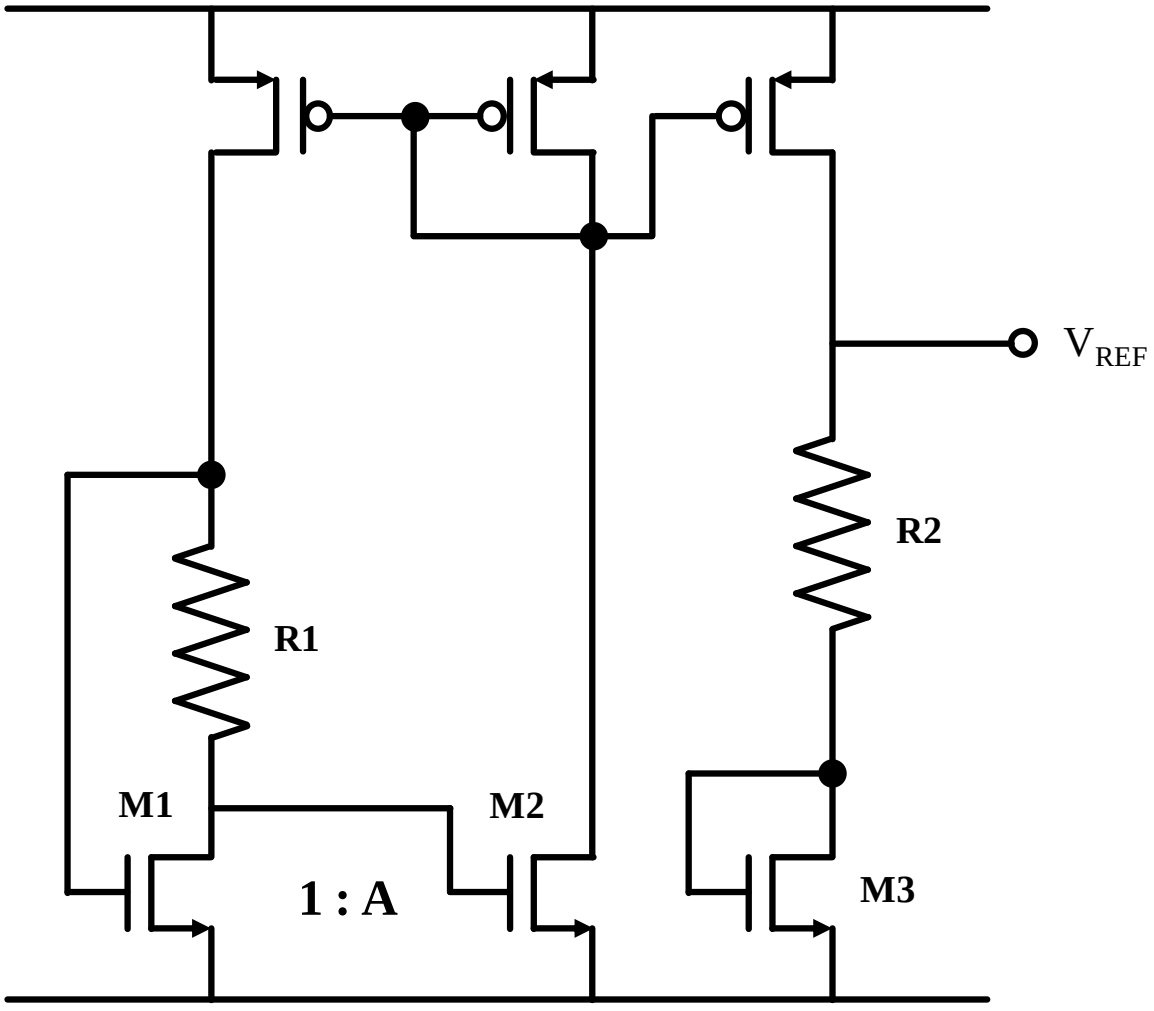


Figure 3.10. Schematic of Bandgap.

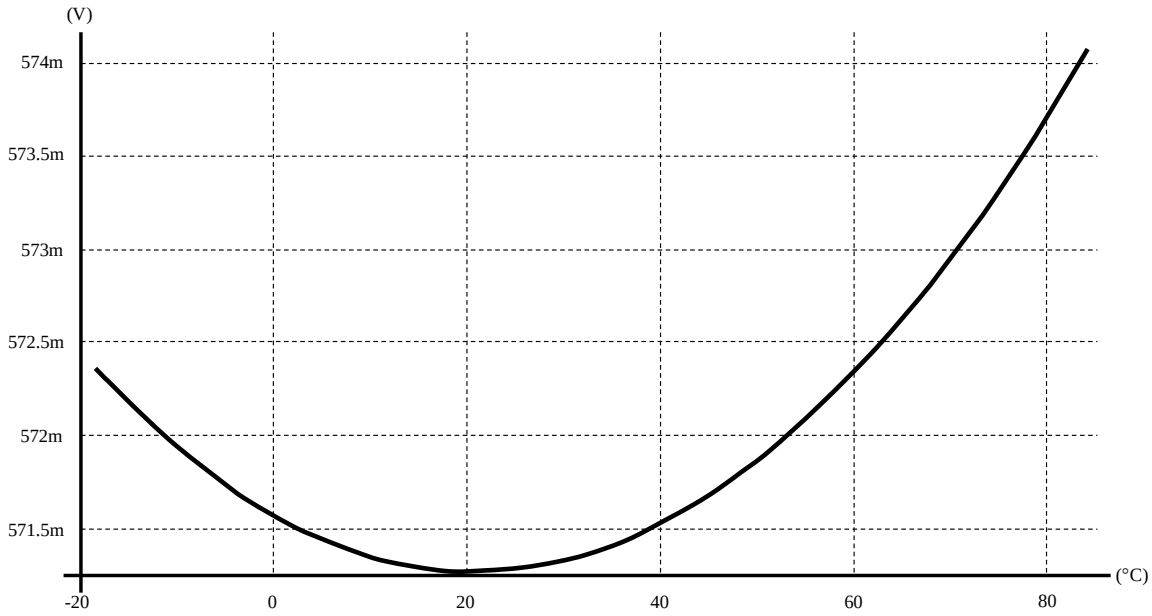


Figure 3.11. Bandgap Voltage versus Temperature.

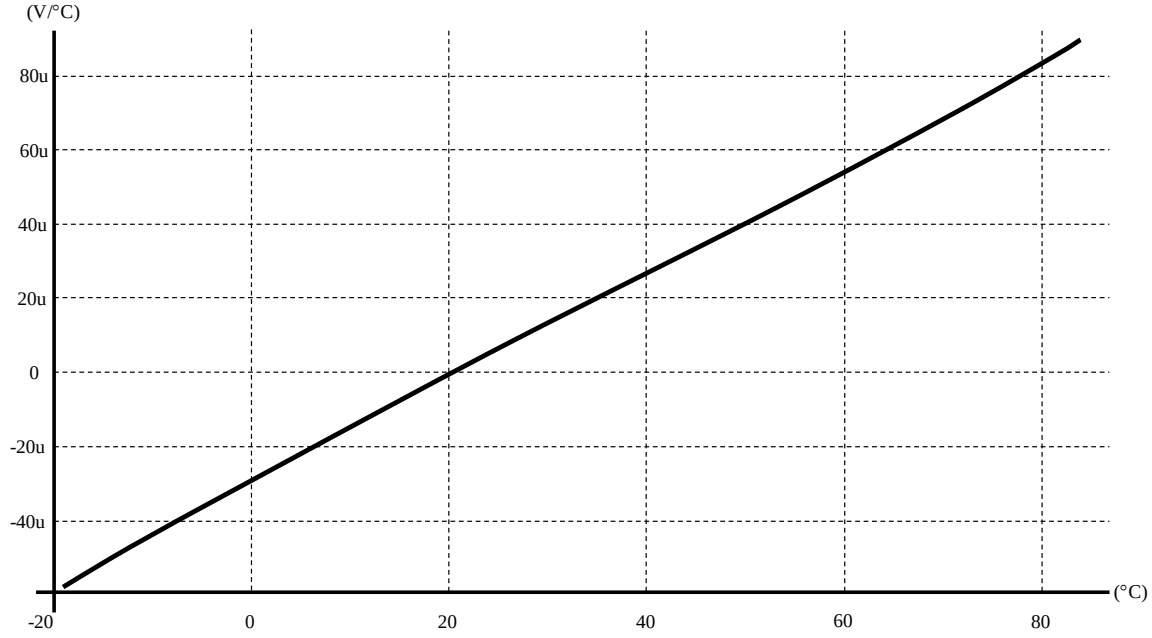


Figure 3.12. Temperature Coefficient of Bandgap Voltage versus Temperature.

The bandgap has a current consumption of 2uA from 900mV supply while providing 300nA bias current for 3 blocks in the RFID tag.

3.3.3. LDO

Low-dropout regulator is a linear voltage regulator which uses a feedback loop to provide a stable voltage at its output. The main advantage of the low-dropout regulator is the low input-output voltage difference which also increases the efficiency of power usage is the key factor for being used in our RFID tag. Due to the low power nature of RFID tag, an op-amp with decent bandwidth was enough to suppress voltage variations at output. To further reduce the variations at output, a decoupling resistor is added.

The operating principle of LDO is simple. As the op-amp provides same node voltages at its plus and minus input terminals, V_{REF} is generated over R2 resistor. As the same current is flowing through R1 and R2, the output voltage will be:

$$V_{OUT} = V_{REF} \frac{R_1 + R_2}{R_2} \tag{3.6}$$

V_{REF} is the bandgap voltage which is around 570mV and desired output voltage is 670mV. R1 must be 0.17 times R2 to get such an output from the LDO with given specs. One of the most important design criteria of LDO is its quiescence current that is bias current of op-amp and output branch current which is determined by V_{REF}/R2. For output quiescence current of 500nA R2 will be around 1.1MΩ and R1 will be around 200kΩ. The OTA used inside LDO consumes 300nA from 900mV supply that makes the quiescence current of LDO 800nA from 900mV supply. As a result, LDO has a total power consumption of 720nW which is promising for low power applications.

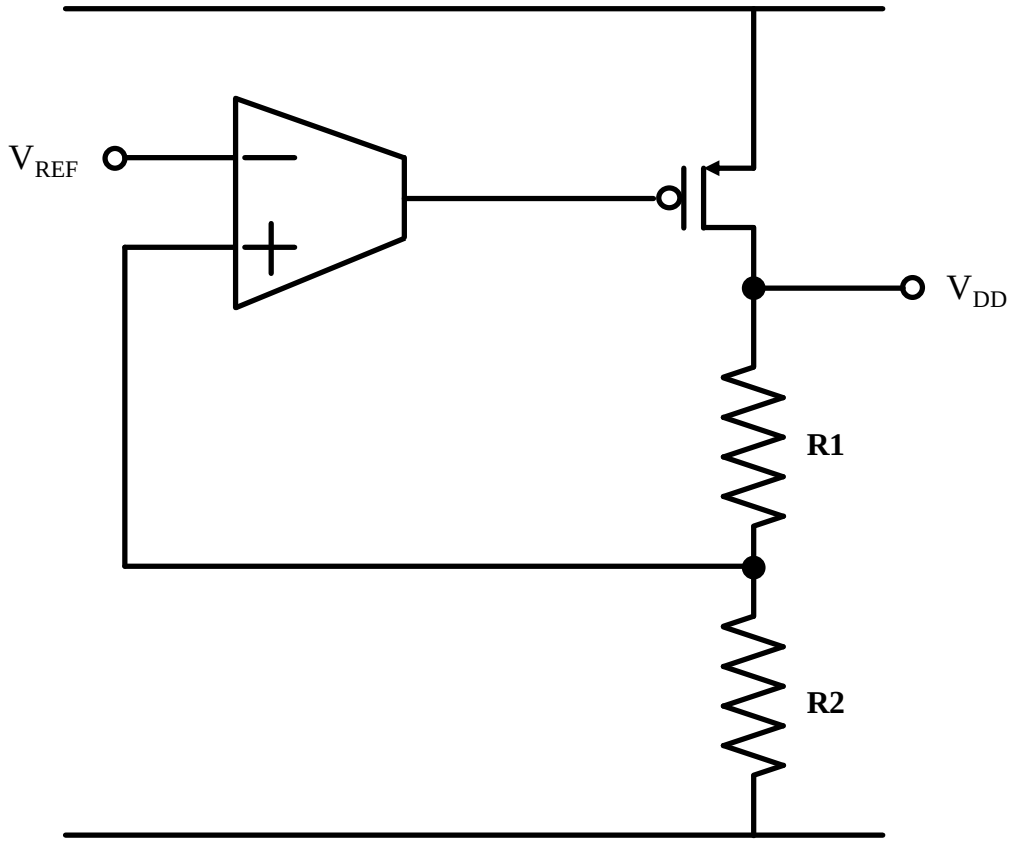


Figure 3.13. Schematic of LDO.



Figure 3.14. PSRR of LDO.

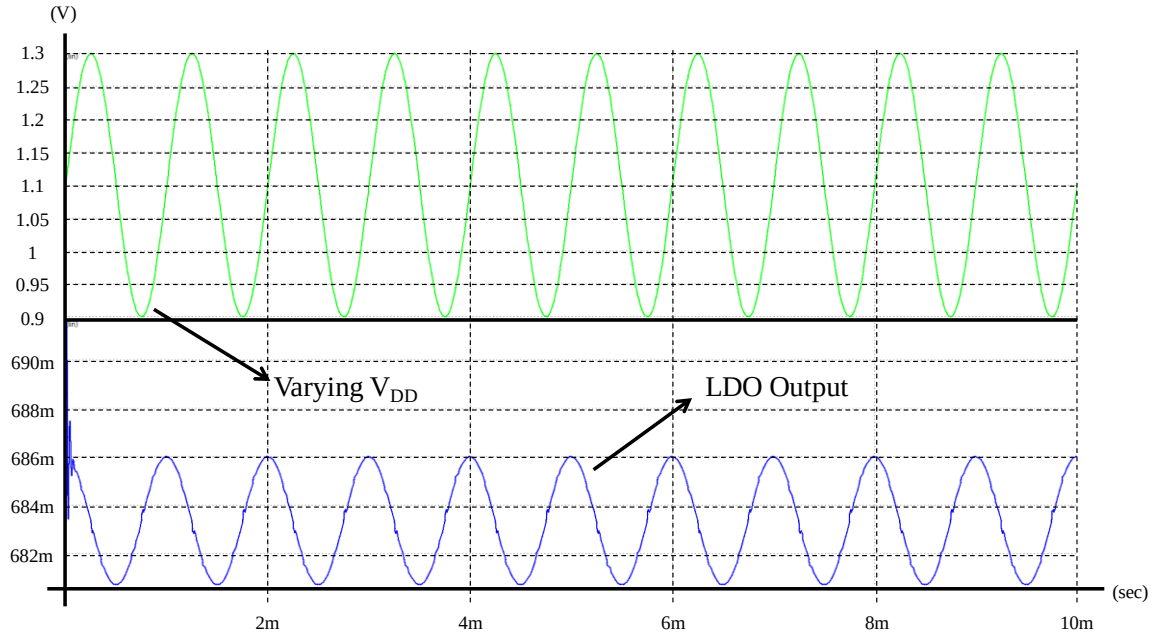


Figure 3.15. Varying V_{DD} and LDO Output Transient Result.

3.3.4. POR

POR is a wake-up signal for the digital baseband and nonvolatile memory. It assures that all voltage supplies are stable and above a certain threshold before generating a one-shot reset pulse [20]. The operating principle of POR circuitry can be seen on Figure 3.16.

Once the voltage on supply rail exceeds the threshold of the switch, it charges up a capacitor which feeds cross-coupled inverters. The outputs of these cross-coupled inverters are then applied to OR gate to generate logic “1”. Using XOR gate, signal is compared with its delayed version which generates a one-shot at POR output. The schematic of POR is given in Figure 3.17.

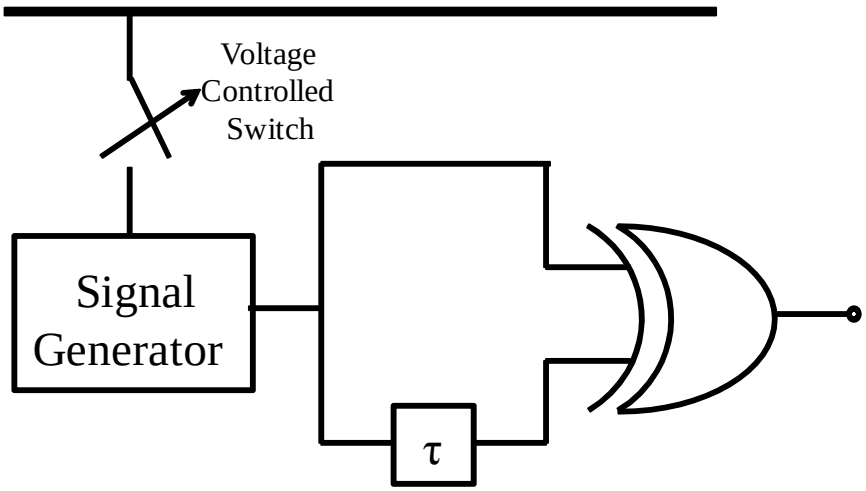


Figure 3.16. Operating Principle of POR.

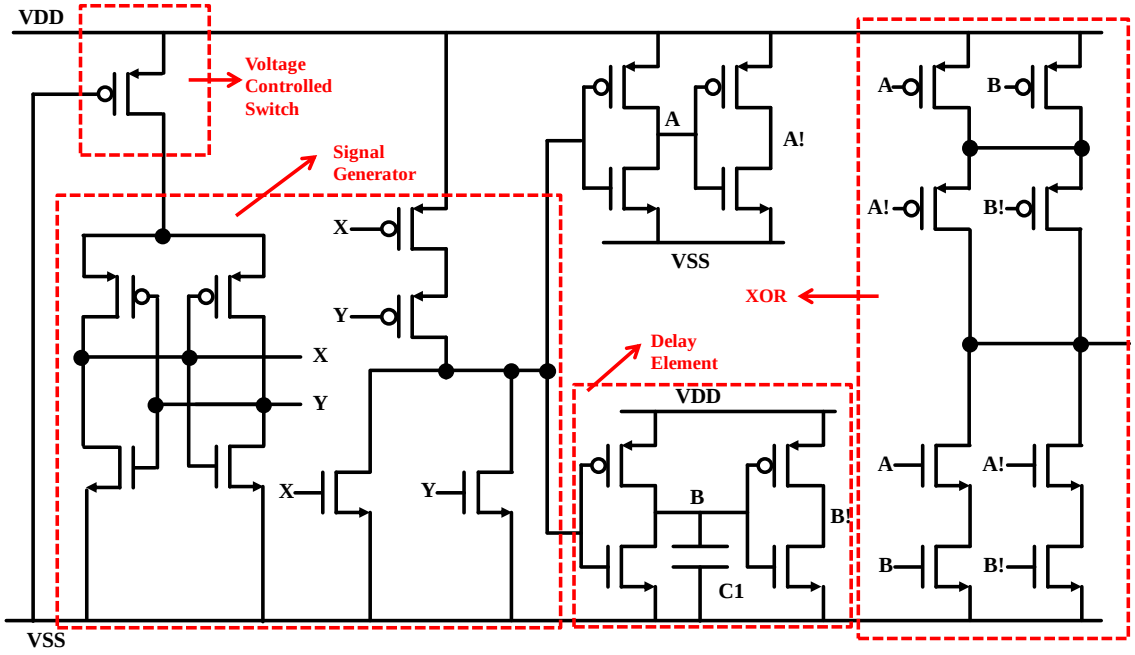


Figure 3.17. Schematic of POR.

Simulations are run to test POR circuit under several test conditions to determine the pulse width of one-shot reset pulse. As the system clock is around 2.5MHz, the pulse is expected to be around 4 or 5 clock cycles which is around 2μs to ensure reset operation. Result of PVT analysis is given in Table 3.1.

Table 3.1. PVT of POR One-Shot.

Cases	Pulse Width
Typical Case Nominal VDD,Typical device corner, 25°C	1.79us
Slowest Case Lowest VDD,Slow device corner, -20°C	3.71us
Fastest Case Highest VDD,Fast device corner, 85°C	1.57us

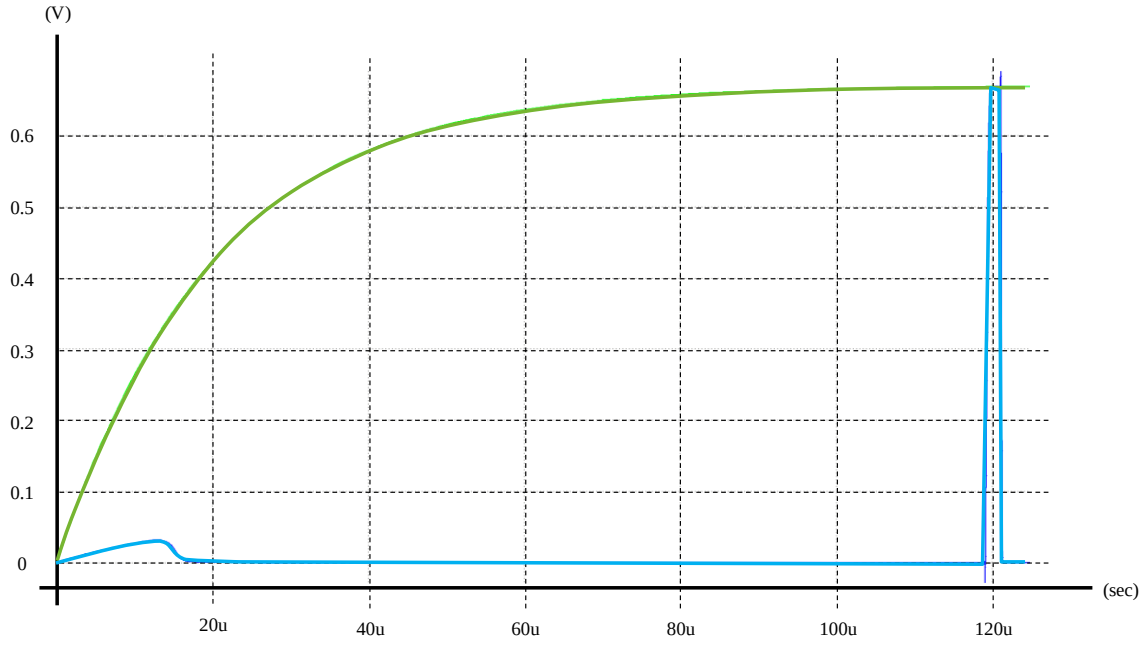


Figure 3.18. Transient analysis of POR.

On typical cases, the LDO output versus POR in transient analysis is like in Figure 3.18. POR requires a long time to produce a one-shot compared to LDO output, which provides a safe operation.

POR is designed with CMOS digital circuits to eliminate static power consumption. This property of POR is vital for energy dependant RFID tag chip.

3.4. Discussion

RFID applications are getting more attention because of their advantages over barcodes. Barcodes require being in line-of-sight to communicate and are not programmable. However, RFID tags do not depend on line-of-sight communication, are programmable and provide several functions to increase its security. RFID has a good market potential both in Turkey and all around the world. For instance, the new HGS system used in highways and bridges is an RFID based system which stores data about the route of the vehicle and associated bank account to charge customers.

UHF RFID Class 1 Generation 2 protocol uses PIE modulation scheme with % 100 modulation index. Therefore, the RF signals are much like OOK modulated signals. This feature enables to use low power circuitry which increases the maximum distance tag can power up itself with harvested energy. As the protocol provides a basis for RFID tag standards, the most important feature that separates products are their minimum read and write sensitivities. In order to have a better read and write sensitivity, the tag needs a higher rectifying efficiency and lower power consumption.

To prove the concept of OOK modulation being suitable for low power applications, RFID tag is studied both in system and block level. Non-coherent and asynchronous communication eliminates the need for power consuming PLL structures. In addition, when using direct conversion techniques, the system does not have an IF level which reduces the power consumption. Therefore, non-coherent direct conversion techniques for OOK modulation are promising for low power applications.

Nanopower structures for RFID tags are studied. Design guidelines for several blocks are provided. It is shown that blocks with ultra low power consumption can be designed for UHF RFID tag. Problems encountered during system level simulations are discussed. The initialization problem of demodulator could prevent the RFID tag from satisfying tag standards. In order to solve this issue, a novel approach had been used. This

technique has minimal power consumption and silicon area. Using an already existing signal as a trigger, the demodulator output is set at logic “1” to be able to receive the delimiter signal from the interrogator.

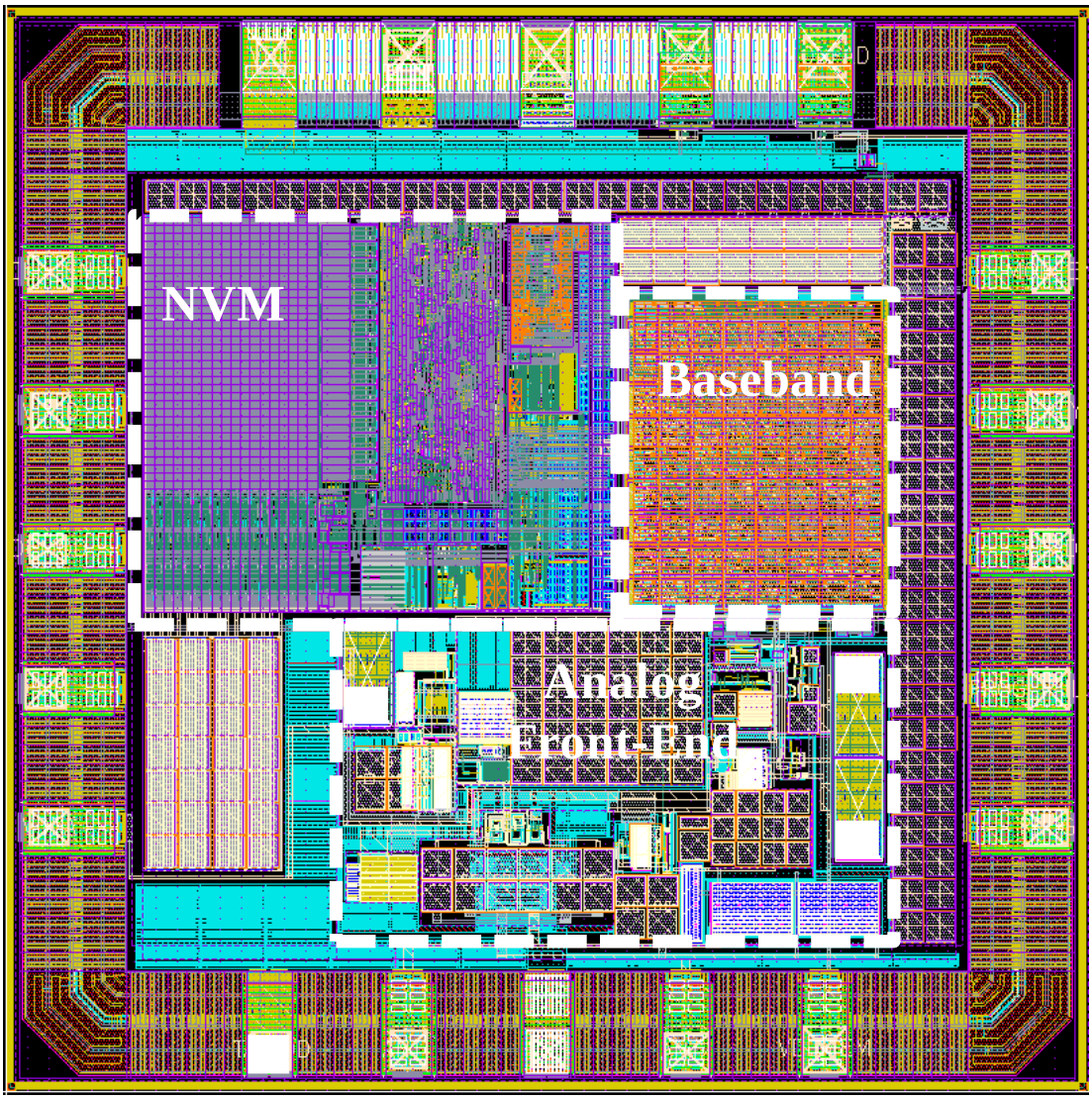


Figure 3.19. RFID Tag Chip Layout.

The RFID tag chip is simulated to verify its functionality and determine minimum read and write sensitivities. Simulated read and write sensitivities of RFID tag chip are -13 dBm and -7 dBm respectively. This is a promising result for low-power applications based on pulse communication. The required energy per bit for data transfer is as low as 312pJ/bit. Although it may seem more consuming compared to the previous 60 GHz pulse

receiver system, RFID tag powers up itself with the RF waves. Therefore, this higher energy per bit ratio is acceptable.

4. CONCLUSION

OOK based communication systems are studied in this work. OOK based communication is suitable for low power applications because it does not require local oscillator or PLL structures which are power hungry blocks. The battery lives of portable products are becoming a major property with evolving technology. In order to present the low power nature of OOK modulation, two different demodulation schemes are used for two different frequency bands. Their respective block diagrams, circuit schematics, theoretical and simulation based analysis are provided where relevant.

To begin with, 60 GHz pulse receiver designed is an improved version of the prior work. The demodulator used in system is based on multiplying the signal with itself. Multiplication usually requires use of active mixers which becomes a power hungry block with increasing carrier frequencies. The studied detection method in this thesis gets rid of the power hungry active mixers, reducing the power consumption of the system further. Direct conversion systems usually suffer from even-order distortion. However this detection scheme takes advantage of it explicitly. Therefore, the overall power consumption of the system is reduced.

The prior design suffered from mismatch and common mode noise due to its single-ended topology. In order to improve these properties of circuitry, a fully differential version of the detector is designed. Theoretical analysis is done to maximize the detection property. The detection property had been doubled with recent modifications and the circuit is now more immune to common noise and mismatch effects. Proposed detector is much more suitable for low-power short-range data communication.

Designed 60 GHz multi-Gbps pulse receiver is fabricated in 90 nm technology. Input sensitivity for 2 Gbps and 3 Gbps are -26 dBm and -23 dBm respectively for BER of 10^{-6}. The receiver consumes 29 mW while only 1.6 mW of this is consumed by the detector. This is promising evidence for OOK is suitable for low-power data communication.

Another pulse communication based popular communication system is the RFID. RFID tags have no battery, they harvest energy from waves sent from the interrogator. RFID has many fields of application which encourages researchers to still study the subject. The RFID tag for UHF Class 1 Generation 2 protocol is designed at Gate Elektronik, Ankara.

RFID uses PIE signals to transmit data. The major difference between PIE encoded signals and OOK is both data “0” and data “1” are represented with pulses, but their duration changes. In terms of demodulator structure however, this feature has no effect as the digital signal processor compares the pulse interval with a reference to decide if the data is “0” or “1”. The tag uses an envelope detection based demodulator to enable interrogator to tag communication. The passive envelope detector has no power consumption from supplies which makes it suitable for low-power applications. Followed by a low-power low-voltage comparator, the demodulator is complete.

The demodulator had an initialization problem because it is powered up by RF power harvested from the interrogator. The demodulator output had to be set at logic “1” before the interrogator starts sending baseband data. In order to solve this issue, an already system generated signal is used to not only to simplify the analog front-end but also to do not cause any additional power dissipation for the system.

The RFID system is implemented in 180nm process technology. The licensed NVM, synthesized baseband and designed analog front-end are placed and routed all together inside a square of 920µm x 920 µm. Moreover, an additional test chip is designed with additional output pads to probe several critical nodes to check blocks separately.

System level simulations are done to verify RFID tag performance. The expected read and write sensitivities of the RFID tag are -13 dBm and -7 dBm respectively. Simulation results verify the UHF RFID Class 1 Generation 2 standards. Pulse communication lets designers use low-power structures which make systems portable and battery-efficient. In RFID example, the system gets rid of the need for battery which increases its mobility and field of application by doing energy harvesting. It is shown that

pulse communication is suitable for low-power applications which are very much needed in today's technology.

In this work, pulse communication based communication systems are studied. In order to prove the low power nature of OOK based communication systems, two different pulse communication applications are chosen. System level information as well as block level design guidelines are provided for each system. To reduce overall system power consumption, main design consideration was to reduce branch currents. Overall system performance results are provided.

All in all, it is shown that pulse communication is promising for low-power applications in order to increase battery life and portability. Pulse communication can negate the need of power hungry blocks like PLLs, mixers or local oscillators. Thus, overall power consumption can be reduced significantly. Two different systems studied inside this work support this idea. For example, 802.11n MIMO3 has an energy per bit efficiency around 5nJ/bit at data rate of 400Mb/s [21]. However in our work, even batteryless RFID tag chip has 312pJ/bit which makes at least one order of magnitude difference compared to 802.11n MIMO3. Moreover, the 60 GHz pulse receiver consumes 9.6pJ/bit which is more than 500 times lower compared to 802.11n MIMO3. This feature proves the fact that pulse communication is suitable for low-power, portable and battery efficient applications.

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