IMPULSE RADIO ULTRA-WIDEBAND TRANSCEIVER DESIGN

by

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M.S., Electrical and Computer Engineering, University of California, Santa Barbara

2014

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Doctor of Philosophy

Graduate Program in Electrical and Electronics Engineering

Boğaziçi University

2024

ACKNOWLEDGEMENTS

This dissertation marks the end of a long and challenging journey, one that has been filled with numerous ups and downs. I owe a debt of gratitude to many individuals who have supported me along the way.

Firstly, I would like to express my deepest appreciation to my supervisor, Prof. Günhan Dündar, who helped and supported me during this dissertation process. Additionally, I appreciate Assist. Prof. Okan Zafer Batur's help and contributions.

My academic journey has begun at Boğaziçi University, and I am deeply thankful for the education and opportunities I received there. Boğaziçi has become an integral part of who I am, providing the foundation for my academic and professional growth. I would also like to honor the memory of Frederick Kerem Harmancı, one of the most gentle and inspiring professors I had the privilege of knowing at Boğaziçi, whose life was taken from us too soon. His memory will always be with us and continue to guide us.

I would also like to thank my project partner Semih Ramazanoğlu for his technical support and friendship during this process. I'd like to thank other project partners, Atakan Aydoğdu and Muhammed Salih İnneci, who helped me through this process.

I would also like to thank ADI Turkey for their support during the measurements. This support has been of great importance in completing this work. I would also like to thank all my friends and colleagues who have given their support and companionship along the way. The existence of all of you in my life has made this path easier and more enjoyable.

Finally, I am profoundly grateful to my family, who have been my rock throughout this journey. Without their unwavering support, love, and encouragement, I would not have been able to achieve so much. Special thanks to my mother, Nesrin, for her

patience and care during this time. My heartfelt thanks also go to my sisters, Rabia and İrem, who have brought joy and laughter into my life, lightening the load when things got tough.

ABSTRACT

IMPULSE RADIO ULTRA-WIDEBAND TRANSCEIVER DESIGN

This thesis presents a novel, digitally configurable, switching oscillator-based impulse radio ultra-wideband (IR-UWB) transmitter that is robust to process variations. The pulse width and pulse position properties of the output waveform are configurable to ensure operation for the desired bandwidth and output pulse energy values. The architecture is based on a cross-coupled LC voltage-controlled oscillator (LC VCO) implemented with a custom-designed on-chip balun at a center frequency of 2.4 GHz. The presented IR-UWB transmitter that occupies a total area of 0.35 mm^2 is fabricated in the United Microelectronics Corporation (UMC) 180-nm mixed-mode/radio frequency (MM/RF) CMOS process. The measured output voltage swing of the fabricated transmitter is 0.812 Volts on a 50-Ω antenna load for the 200 Mb/s data rate. The fabricated transmitter can drive 50 Ω, 75 Ω and 100 Ω loads with measured efficiency values 4.16%, 5.76%, and 4.05%, respectively. Compared to other works in the literature, this design achieves a higher output pulse energy at a higher data rate while maintaining low power consumption and, thus, high efficiency.

For the IR-UWB receiver side, a differential common-source (CS) cascode LNA with inductive source degeneration is implemented for the RF front-end. Additionally, the subsequent variable gain amplifier (VGA) and mixer blocks are designed for potential future applications in coherent and non-coherent architectures. The fabricated components include an IR-UWB receiver front-end with a cascode CS LNA and a source follower buffer stage for LNA measurements. The fabricated RX occupies a total area of 1.47 mm^2 and the transmitted UWB signal from the proposed transmitter was successfully measured on the receiver side during the chip testing procedure.

ÖZET

DARBE TABANLI RADYO ULTRA GENİŞBANT VERİCİ-ALICI TASARIMI

Bu tez, işlem varyasyonlarına karşı dirençli olan, sayısal olarak yapılandırılabilir, anahtarlanabilir osilatör tabanlı bir darbe tabanlı radyo ultra-genişbant (UGB) verici sunmaktadır. Çıkış dalga formunun dar bant genişliği ve çıkış darbe enerji değerlerinin hedeflenen seviyelerde olması için yapılandırılabilir darbe genişliği ve darbe pozisyonu özelliklerine sahiptir. Mimari, özel tasarlanmış bir entegre balun ile 2.4 GHz merkez frekansında bir çapraz bağlı LC gerilim kontrollü osilatöre dayanmaktadır. Toplam 0.35 mm^2 alan kaplayan darbe tabanlı UGB verici, United Microelectronics Corporation (UMC) 180 nm karışık modlu/radyo frekansı (MM/RF) CMOS işleminde üretilmiştir. Üretilen verici devresinin ölçülen çıkış voltaj salınımı, 200 Mb/s veri hızı için 50-Ω anten yükünde 0.812 Volt'tur. Üretilen verici, sırasıyla %4.16, %5.76 ve %4.05 verimlilik değerleri ile 50 Ω, 75 Ω ve 100 Ω yükleri sürme kapasitesine sahiptir. Literatürdeki diğer çalışmalarla karşılaştırıldığında, bu tasarım düşük güç tüketimini korurken daha yüksek bir veri hızında daha yüksek bir çıkış darbe enerjisi elde eder ve bu nedenle yüksek verimliliği sağlar.

Darbe tabanlı UGB alıcı tarafı için RF ön uçta indüktif kaynak bozmalı ortak kaynak kaskodu tasarlanmıştır. Değişken kazançlı amplifikatör ve karıştırıcı bloklar ise koheran ve koheran olmayan alıcı mimarilerinde potansiyel gelecekteki uygulamalar için tasarlanmıştır. Üretilen bileşenler, düşük gürültülü kuvvetlendiricinin çıkışında yer alan kaynak takipçi tampon aşaması ile birlikte kaskod ortak kaynak düşük gürültülü amplifikatörden oluşan bir darbe tabanlı UGB alıcı ön ucunu içermektedir. Alıcı toplam 1.47 mm^2 alan kaplamakta ve üretilen verici tarafından iletilen UGB sinyali, çip test prosedürü sırasında alıcı tarafında başarıyla ölçülmüştür.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS . . . iii
ABSTRACT . . . v
ÖZET . . . vi
LIST OF FIGURES . . . viii
LIST OF TABLES . . . xiv
LIST OF SYMBOLS . . . xv
LIST OF ACRONYMS/ABBREVIATIONS . . . xviii
1. INTRODUCTION . . . 1
1.1. Background and Literature Survey . . . 4
1.2. Contributions and Organization of the Thesis . . . 8
2. IMPULSE RADIO ULTRA-WIDEBAND TRANSCEIVER DESIGN . . . 10
2.1. Transmitter Architecture . . . 10
2.1.1. Configurable Digital Pulse Generator . . . 11
2.1.2. Digitally Controlled LC Oscillator . . . 20
2.1.3. Custom Designed On-chip Balun . . . 25
2.1.4. PCB Design . . . 31
2.2. Receiver Architecture . . . 35
2.2.1. Low Noise Amplifier . . . 36
2.2.2. Variable Gain Amplifier . . . 43
2.2.3. Mixer . . . 46
2.2.4. PCB Design . . . 48
2.3. Transceiver Post Layout Simulations . . . 51
3. MEASUREMENT RESULTS . . . 54
3.1. Transmitter Measurement Results . . . 54
3.2. Receiver Measurement Results . . . 61
3.3. Transceiver Measurement Results . . . 65
4. CONCLUSION AND FUTURE WORK . . . 68
5. PUBLICATIONS . . . 70
REFERENCES . . . 71

LIST OF FIGURES

Figure 1.1. Block diagram of a conventional UWB transceiver. 4

Figure 2.1. Proposed transmitter architecture. 10

Figure 2.2. Desired output pulses for the digital pulse generator. 12

Figure 2.3. (a) Block diagram of the proposed digital pulse generator (b) Block diagram of the unified transmitter. 14

Figure 2.4. Two sets of data and clock inputs with OOK modulation output waveforms. 15

Figure 2.5. (a) Input and output waveforms of the configurable delay unit (b) Output waveforms of the digital pulse generator (c) TX output waveform at the antenna. 16

Figure 2.6. Schematic of the digitally controlled delay line. 17

Figure 2.7. Tail_ON/OFF waveform with OscPair_ON and OscPair_OFF signals which are generated with different configuration of control bits. (a) The least delayed and min width, (b) the max width, and (c) the most delayed and min width cases. 18

Figure 2.8. Layout view of the Digital Pulse Generator. 19

Figure 2.9. Input and output waveforms of pulse generator for 200 Mb/s data rate. 19

Figure 2.10. Schematic view of the proposed transmitter based on a cross-coupled LC oscillator. 21

Figure 2.11. Switching clock input and the oscillator output waveforms and zoomed view of a single UWB output pulse. 23

Figure 2.12. Layout of the proposed TX excluding the custom designed balun. 24

Figure 2.13. Frequency vs V_{bias} for different configuration of <CTRL3, CTRL2, CTRL1, CTRL0> bits. 25

Figure 2.14. Simulation results for the custom-designed balun including both the lumped model and EM data: (a,b) Forward transmission loss for inverting and non-inverting output ports, (c,d) Phase and angle imbalance between inverting and non-inverting outputs, (e) Output reflection coefficient, (f,g) Inductance seen from antenna output and oscillator connected input ports. 26

Figure 2.15. Schematic illustration of the designed balun. 26

Figure 2.16. Layout of the custom-designed balun. 27

Figure 2.17. Balun Turns Ratio vs. (a) Voltage swing at Oscillator and Antenna Outputs, (b) Generated pulse energy, (c) Total Power, (d) Efficiency. 28

Figure 2.18. LC Oscillator control pulses and their corresponding oscillator and balun outputs. 28

Figure 2.19. Zoomed view of the output pulses at 50 Ω load. 29

Figure 2.20. ANTENOUT waveforms for different configurations of control bits. 29

Figure 2.21. ANTENOUT waveforms in time and frequency domains with different configurations of OscPair_ON/OFF control signals. 30

Figure 2.22. BW calculation details for ANTENOUT output waveforms in frequency domain. 30

Figure 2.23. (a) Pin-out diagram of the chip (b) 48-pin QFN package. 31

Figure 2.24. Top level schematic view of the PCB. 32

Figure 2.25. Cross-section of a coplanar waveguide. 33

Figure 2.26. (a) Layout and (b) 3D views of the PCB. 34

Figure 2.27. (a) TX Gerber files output and (b) Soldered PCB board with connectors. 35

Figure 2.28. (a) Template pulse based coherent receiver (b) Energy detection non-coherent receiver. 36

Figure 2.29. Schematic view of the proposed differential common source cascode LNA architecture. 37

Figure 2.30. (a) Half circuit schematic view of the proposed LNA (b) the small-signal model of the input transistor. 38

Figure 2.31. Layout view of the differential common source cascode LNA. . . . 40

Figure 2.32. Testbench for AC analysis. 41

Figure 2.33. Post-layout AC simulation results. 41

Figure 2.34. Testbench for s parameter analysis. 42

Figure 2.35. Post-layout simulation results for the s-parameters. 42

Figure 2.36. LNA noise figure for the post-layout design. 43

Figure 2.37. Active loaded VGA schematic. 43

Figure 2.38. AC response of the design VGA stage. 44

Figure 2.39. Reconfigurable VGA with varying feedback resistors. 45

Figure 2.40. Reconfigurable VGA with varying bias current. 45

Figure 2.41. Cascaded VGAs with multiplexer architecture. 46

Figure 2.42. Proposed Gilbert Mixer architecture. 47

Figure 2.43. Proposed Gilbert Mixer input and output waveforms. 48

Figure 2.44. Top level schematic view of the LNA PCB. 49

Figure 2.45. (a) Layout and (b) 3D views of the Receiver PCB. 50

Figure 2.46. (a) RX Gerber files output and (b) Soldered PCB board with connectors. 50

Figure 2.47. Transceiver simulation setup including the pi-network. 51

Figure 2.48. Time domain waveforms at the transmitter output and the LNA input respectively. 52

Figure 2.49. Time domain waveforms at the LNA differential outputs. 52

Figure 2.50. Differential waveform observed at the LNA output. 53

Figure 3.1. Microphotograph of the final silicon. 54

Figure 3.2. Layout of the proposed TX architecture. 55

Figure 3.3. Microphotograph of the fabricated transmitter. 55

Figure 3.4. Measurement setup. 56

Figure 3.5. Measured output waveforms on 50, 75, and 100 Ω loads at 200 Mb/s. 56

Figure 3.6. Measured output waveforms for different configuration of control bits. 57

Figure 3.7. Output spectrum of the UWB pulse, center frequency 2.4GHz, 1 MHz PRF. 58

Figure 3.8. Measured frequency values for the specific configurations of <CTRL3, CTRL2, CTRL1, CTRL0> bit set and V_{bias} value (a) 2.14 GHz (b) 2.40 GHz (c) 2.81 GHz (d) 3.05 GHz. 58

Figure 3.9. Microphotograph of the fabricated receiver. 62

Figure 3.10. Measurement Setup. 63

Figure 3.11. S parameters measurements. 63

Figure 3.12. Frequency domain single tone measurement of the LNA output. . 64

Figure 3.13. Measured time domain response of the receiver front-end (a) output pair (b) differential output. 65

Figure 3.14. Measurement Setup. 65

Figure 3.15. Spectrum waveform in (a) transmitter output, (b) LNA input, and (c) LNA output respectively. 66

Figure 3.16. Output waveform measured at the LNA output 67

LIST OF TABLES

Table 2.1. Parameters for Digital Pulse Generator Output Pulses. 12

Table 2.2. Selection bits with corresponding total delay for process corners. . 13

Table 2.3. Pin List for the Configurable Digital Pulse Generator. 13

Table 2.4. Pulse position and width values for OscPair_ON and OscPair_OFF signals with different configurations of control bits. 18

Table 2.5. Register map for the control bits. 30

Table 3.1. TX Performance Summary and Comparison. 60

LIST OF SYMBOLS

$A0$	Digital configuration bit 1
$A1$	Digital configuration bit 2
$A2$	Digital configuration bit 3
$B0$	Digital configuration bit 4
$B1$	Digital configuration bit 5
$B2$	Digital configuration bit 6
$C0$	Digital configuration bit 7
$C1$	Digital configuration bit 8
$C2$	Digital configuration bit 9
C_d	Drain capacitance
C_{gs}	Gate to source capacitance
C_{par}	Parasitics capacitance
C_{tot}	Total capacitance of the binary weighted capacitor array
C_{var}	Tunable varactor capacitance
$D0$	Digital configuration bit 10
$D1$	Digital configuration bit 11
$D2$	Digital configuration bit 12
dB	Decibel-watts, logarithmic unit
dBm	Decibel-milliwatts, logarithmic unit
E_p	Total pulse energy of the output signal
fF	Femtofarads, capacitor unit
GHz	Gigahertz, frequency unit
GSa/s	Gigasamples per second, sampling rate unit
I_{BIAS1}	Bias current 1
I_{BIAS2}	Bias current 2
L_{balun}	Balun inductance
L_d	Drain inductance
L_g	Gate inductance

L_s	Source inductance
$Mbps$	Mega bits per seconds, data rate
MHz	Megahertz, frequency unit
mA	Milliamperes, current unit
mm	Millimeters, metric unit
mm^2	Area of the chip in metric system
mV	Millivolts, voltage unit
mW	Milliwatts, power unit
nF	Nanofarads, capacitor unit
nH	Nanohenries, inductance unit
nm	Nanometers, metric unit
ns	Nanoseconds, time unit
P_{avg}	Average power
pJ	Picojoules, energy unit
$pJ/pulse$	Pico-joules per pulse, figure of merit
PW	Pulse width
Q	Quality factor
R_{load}	Load resistance
R_d	Parasitic resistance of Ld
$S0$	Digital configuration bit 13
$S1$	Digital configuration bit 14
s	Seconds, time unit
V_{bias}	Bias voltage
V_{DD}	Supply voltage
V_{gate}	Gate voltage
V_{out}	Output voltage
V_{pp}	Peak-to-peak voltage amplitude
η	Efficiency
μF	Microfarads, capacitor unit
μm	Micrometers, metric unit

ω_o	Oscillation frequency
Ω	Ohms, resistance unit

LIST OF ACRONYMS/ABBREVIATIONS

ADS	Advanced Design System
BPSK	Binary Phase-shift Keying
BW	Bandwidth
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
DATA	Input Data
DUT	Device Under Test
EM	Electromagnetic
EPP	Energy per Pulse
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
INV	Inverter
IoT	Internet of Things
IR	Impulse Radio
IR-UWB	Impulse Radio Ultra-wideband
LNA	Low Noise Amplifier
MB-OFDM	Multi-band Orthogonal Frequency Division Multiplexing
MIM	Metal-Insulator-Metal
MM	Mixed-Mode
NBI	NarrowBand Interference
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PPM	Pulse Position Modulation
PRF	Pulse Repetition Frequency
PVT	Process, Voltage, and Temperature

Q	Quality Factor
QFN	Quad Flat No-lead
RF	Radio Frequency
SMT	Surface Mount Technology
TX	Transmitter
UMC	United Microelectronics Corporation
UWB	Ultra-wideband
VCO	Voltage-Controlled Oscillator
VGA	Variable Gain Amplifier
VIA	Vertical Interconnect Access
WPAN	Wireless Personal Area Network

1. INTRODUCTION

The high data rate and low power consumption properties in short-range communication have made ultra-wideband (UWB) technology a good candidate for a wide range of applications such as wireless telemetry, telemedicine, WPAN, and wireless sensor networks in recent years. Transmission of very high data rate signals, in some cases reaching 100 Mb/s, is necessary for many Internet of Things (IoT) applications including wireless connectivity between PCs and projectors, synchronization and data transfer of media files between mobile devices and the cloud, and wireless streaming of high-definition video content in multimedia apps [1]. Precision localization is also a recent and interesting application of UWB technology. In these applications, short-pulse waveforms are used to accurately determine the precise time of arrival and, as a result, the precise time of flight of a burst broadcast from a short-pulse transmitter to a corresponding receiver [2].

Biomedical wireless applications are another area where UWB technology is extensively studied, particularly in short-range data communication systems within wireless body area networks and radar sensors that remotely detect vital signs such as heartbeat and respiration [3]. In wireless medical applications, secure, lossless connections and noninvasive transmission are essential. Portable medical devices like ultrasound transducers demand high data rates with energy efficiency to reduce coding complexity and extend battery life. Unlike conventional narrowband systems, UWB technology provides seamless, low-latency communication with enhanced security, supporting additional backchannel data through Bluetooth or WiFi. While limited transmission distance can be a drawback, the short range allows for frequency reuse in nearby operating rooms, making UWB's available channels sufficient. Additionally, bit-level duty cycling enhances energy efficiency and offers flexible data rate control [4].

In 2002, the U.S. Federal Communications Commission (FCC) allocated the 3.1-10.6 GHz frequency band, with a spectral limit of -41.3 dBm/MHz, for unlicensed ultra-wideband technologies. According to FCC regulations, a signal is called ultra-wideband

if its bandwidth is greater than 500 MHz or its fractional bandwidth is greater than 0.2 [5]. Numerous advantages come with the use of large transmission bandwidths in UWB technology, such as precise range, robustness against propagation fading, superior obstacle penetration, covert operation, resistance to jamming, interference rejection, and coexistence with narrow bandwidth systems [6].

There are numerous methods of modulating an UWB signal for high-rate systems; the most often used ones are IR-UWB, also referred as pulsed UWB and orthogonal frequency-division multiplexing (OFDM). The position, amplitude, and/or polarity of a brief pulse are modulated to encode data in IR-UWB. In OFDM systems, synchronized orthogonal carriers are used to send a set of bits for each symbol [7]. In comparison to conventional OFDM-based UWB systems, the IR-UWB technique can deliver high data rates while consuming extremely low power [8]. Multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB transceivers can deliver high data rates, but the peak-to-average power ratio necessitates a linear power amplifier (PA), leading to reduced power efficiency. Moreover, MB-OFDM receivers are sensitive to carrier frequency variations, and the use of coherent receivers with complex OFDM demodulation makes achieving good energy efficiency challenging, thereby making them less suitable for portable applications [4]. This thesis focuses on the IR-UWB transceiver architecture.

The impulse radio UWB (IR-UWB) approach utilizes very short nanosecond duration baseband-modulated pulses and such that the synchronized transmitter and receiver parts can power down their radio frequency (RF) subsystems for long periods of time between consecutive pulses. This characteristic allows ultralow-power communication that is orders of magnitude lower in power consumption than continuous-wave approaches to be accomplished [9].

Numerous studies have explored the use of IR-UWB with various pulse modulation techniques. The most commonly employed methods include on-off keying (OOK), pulse position modulation (PPM), and binary phase-shift keying (BPSK). However, each modulation method presents its own challenges. For instance, PPM has a limita-

tion on the number of bits that can be transmitted in one period due to inter-symbol interference (ISI). Consequently, simply changing the modulation scheme does not effectively enhance the data rate. To achieve a higher data rate, it is essential to increase the clock speed. Thus, the IR-UWB communication data modulation techniques developed so far must focus on increasing the pulse repetition frequency (PRF) for high-data-rate communication, as the data rate is directly proportional to the PRF [10]. BPSK offers excellent noise immunity and is easier to synchronize than PPM. However, the circuit design for phase-modulated signals is more complex, leading to higher hardware costs. In contrast, OOK is commonly used in the literature due to its simpler circuit design compared to other methods [11].

In high data rate applications, increasing energy efficiency by reducing power consumption is critical. For example, in brain-computer interface systems, multiple channels (> 100) are used to record and transmit data. As the number of channels or the sampling rate increases, the data rate increases proportionally, leading to higher power consumption [12]. In biomedical devices, particularly brain implants, the limited power budget is a major challenge. These devices typically rely on lightweight, low-capacity batteries or wireless power links. Additionally, the heat dissipation requirements of miniaturized implants impose further constraints [13, 14]. Consequently, the available power, often limited to a few milliwatts per square centimeter, is insufficient for most conventional transmitters (TXs) to achieve the necessary data rates [15]. Therefore, designing energy-efficient systems is essential for these applications.

The IR-UWB transmitter is operated in a brief amount of time with short-duration pulses, and thus consumes low power and has a very wide spectrum. On the receiver side, non-coherent detection is commonly utilized in IR-UWB receivers to simplify operations and save power. To achieve a longer battery life, low-power IR-UWB architectures with reduced circuit complexity are proposed in the literature and will be discussed in the next section.

1.1. Background and Literature Survey

The diagram depicting a typical UWB transceiver system in Figure 1.1 shows the proposed transmitter/receiver blocks within the system architecture. Energy efficiency is the most critical design aspect in such a battery-powered UWB transceiver system. Recent advances to enhance high-speed data transmission capabilities in challenging environments for energy-efficiency further emphasize the significance of high data rates, low power consumption, and energy efficiency in modern communication systems [16–19].

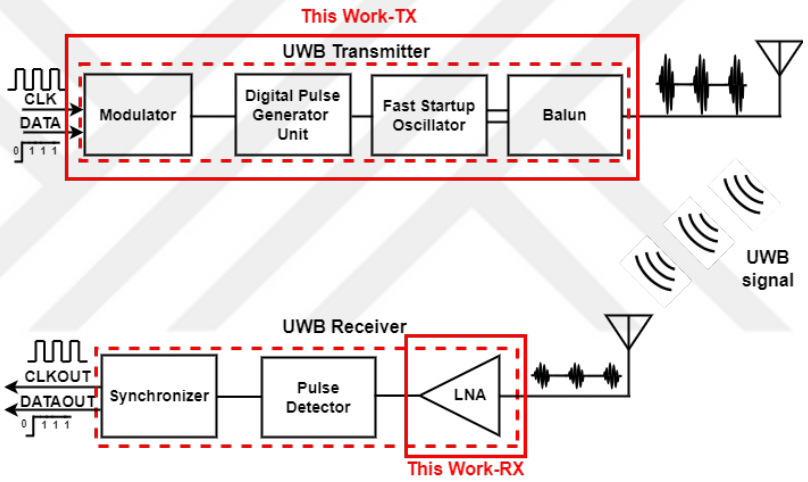


Figure 1.1. Block diagram of a conventional UWB transceiver.

With the evolution of UWB technology, novel IR-UWB transceiver architectures have been introduced to the literature to address the needs of modern communication systems. The primary focus in the battery-powered designs still remains on maximizing the energy efficiency of the transmitter block [20]. To achieve a longer battery life, low-power IR-UWB transmitter architectures with reduced circuit complexity are proposed in the literature, and can be classified on the basis of the pulse generation technique utilized in their architecture.

The primary approaches encompass LC oscillator [21–25], ring oscillator [26–28], pulse combination [29, 30], pulse shaping [31–33] and up-conversion [34, 35] methods. Although digital architectures often achieve low power consumption, only a fraction of the total energy is converted to the transmitted pulse. However, in designs based

on LC oscillators, most of the energy is converted to the transmitted pulse, and high-efficiency figures are possible as in [36]. In addition, a digital pulse generator has fast on/off characteristics, but channel selection is also more difficult compared to the LC-VCO-based transmitter, where the frequency can easily be tuned by adjusting the varactor values in the capacitor bank [37, 38]. The active current of the digital pulse generators is also directly proportional to the operating frequency, which limits the high-speed applications for this structure [39].

Although digital pulse generation architectures consume power only when they are active, which results in negligible static power consumption, the static power consumption of LC-VCO based transmitters can also be reduced to similar levels by using an on-off switching scheme. In [40], a switched cross-coupled LC VCO is implemented with very low static power. Using the capacitor mismatch technique, this design achieves a fast build-up of the oscillation. However, the output voltage swing is 400 mV, resulting in a very short-range communication. The tail transistor is used directly as a switch in [41] to power (on or off) the VCO so that a high peak output power is achieved with the 3 V peak-to-peak output voltage. On the other hand, the data rate is limited to 10 Mbps in this design. In [37], LC-VCO is quickly turned on/off with a differential output swing of 2 V and a power consumption of 1.8 mW, but the achieved data rate is only 1 Mbps. High data rates are important, especially in medical applications, to obtain more accurate diagnosis. The trade-off between high data rate and low power is still an issue for such demanding systems [41], [42].

In this thesis, we propose a switchable and configurable LC-VCO based UWB transmitter architecture that is robust to process variations and is designed for low power and high data rate applications. Although many proposed architectures are based on LC-VCO in the literature, the proposed design uses a tail switching architecture together with the charge injection and charge removal techniques to ensure fast start-up and wide-band operation. The implemented transmitter (TX) also features an on-chip balun as an output antenna driver circuit after the comprehensive investigation for the proper turns ratio to achieve high data rate and high efficiency simultaneously.

Within IR-UWB systems, two primary types of receiver architectures are utilized: coherent and non-coherent detection. The coherent receiver not only offers improved sensitivity but also enhances immunity to Narrow Band Interference (NBI). However, it necessitates a synchronized LO signal, which relies on a high-performance Phase-Locked Loop (PLL). Due to the PLL's settling time issue, implementing a duty-cycled operation for the coherent receiver becomes challenging [43]. The non-coherent detection eliminates the need for a PLL that consumes a lot of power and is difficult to implement with duty-cycle. This is achieved by utilizing techniques such as self-mixing, threshold crossing, or peak detection technique [44]. Compared to the coherent receiver, the non-coherent IR-UWB receiver has a simpler architecture and lower power consumption, but it may require more complex demodulation and additional timing synchronization circuitry due to the absence of phase information [45–47].

Coherent IR-UWB receivers are regarded as optimal for achieving robust performance in multipath channels. The conventional coherent IR-UWB rake receiver consists of a series of matched filters, referred to as correlators, with each correlator precisely aligned to a delayed version of the transmitted signal. The output from these correlators effectively combines the multipath energy from each path, thereby maximizing the utilization of multipath diversity. However, this methodology introduces increased system complexity, necessitating the use of correlators, accurate channel estimation, and perfect synchronization [48]. The non-coherent approach provides the advantage of eliminating the need for a bank of correlators and template generators, making it easier to implement. However, its drawback is that noise is amplified along with the signal at the receiver [49].

Non-coherent detection is frequently employed in IR-UWB receivers to reduce complexity and conserve power [4, 7, 8, 10, 47, 50]. Among various architectures, energy detectors based on super-regenerative designs or self-mixing coupled with integrators demonstrate good sensitivity performance [51]. In this architecture, the received UWB pulse is typically first amplified by a low noise amplifier (LNA) before undergoing processing for pulse energy or peak detection, where the received signal is squared and integrated to obtain a representation of the received energy. Detection over meter-

range links demands a considerable LNA gain, and as a result, the power consumption of the non-coherent IR-UWB receiver is largely dominated by the LNA [7, 52].

The low noise amplifier (LNA) is one of the most important blocks in the receiver part. As the first block of the RF signal's receiving path, the amplifier's noise has a considerable effect on the overall noise figure (NF) of the receiver, making it essential for the LNA to have a low NF. Additionally, to prevent gain compression, cross-modulation, and intermodulation, LNA must be highly linear. However, there is a significant trade-off between these characteristics and the amplifier's power gain, power consumption, and input/output impedance matching [53].

Common source (CS) and common gate (CG) architectures are the two commonly used LNA topologies used at the receiver front-end. Compared to the CG configuration, CS offers higher gain and better noise performance. However, the CG configuration is capable of achieving wideband input matching. To further enhance the performance of CS architectures, the cascode common source configuration is often used. This architecture combines two transistors in a way that significantly increases the overall voltage gain while simultaneously improving bandwidth by reducing the Miller effect. The cascode structure effectively reduces voltage variations that can affect linearity, resulting in lower distortion and more reliable signal amplification. It also provides higher output resistance, enabling larger output voltage swings and effective impedance matching. These attributes make the cascode CS configuration very suitable for RF front-end applications where stability, gain, and bandwidth are crucial [54].

In this thesis, a differential common-source cascode LNA with inductive source degeneration is employed in the RF front-end, and while the following variable gain amplifier (VGA) and mixer blocks are designed for future use in coherent/non-coherent receiver architectures, they have not been fabricated. Instead, the fabricated components include an IR-UWB transmitter and the receiver front-end, which consists of a cascode CS LNA plus a source follower buffer stage at the output of the LNA, used specifically to facilitate the measurement of the LNA. The transmitted UWB signal from the proposed transmitter is measured on the receiver side during the chip's test

procedure.

1.2. Contributions and Organization of the Thesis

The contributions made within the framework of this thesis can be summarized as follows:

- IR-UWB transmitter that features configurable pulse width, pulse position, and center frequency settings, designed to withstand PVT variations.
- A custom-designed balun designed for maximum efficiency, eliminating the necessity for an output stage to drive a 50 ohm, 75 ohm, or 100 ohm loads.
- Achieving high efficiency through the combination of high data rate and large output voltage swing while maintaining low power consumption.
- Fast start-up and shutdown using configurable charge injection and charge removal from the output of the oscillator circuit.
- Design of many digital circuits including delay blocks, muxes, configurable delay units, and digital pulse generators to be used in the UWB transmitter.
- Design of many low power amplifiers, baluns, and digital circuits to be used in the UWB transceiver.
- Preparation of layouts for the designed UWB transmitter and receiver blocks and post-layout simulations.
- Design and characterization of two integrated circuits containing UWB transmitter and receiver architectures in 180nm CMOS technology and lab measurements of the fabricated chip.

The organization of the thesis is as follows:

In Chapter 2, the transmitter and receiver design blocks are discussed, including their PCB details. Post-layout simulation results are also presented. Additionally, unified TX and RX simulations are provided in Section 2.3.

Measurement results of the fabricated chip, including TX, RX, and combined TX+RX performance, are presented in Chapter 3. The thesis concludes with final remarks and a discussion of potential future work in Chapter 4.

2. IMPULSE RADIO ULTRA-WIDEBAND TRANSCEIVER DESIGN

2.1. Transmitter Architecture

The transmitter (TX) is composed of two main stages; a configurable digital pulse generator and a digitally controlled LC oscillator including active circuit elements, capacitor bank, and a custom-designed on-chip balun as shown in Figure 2.1. All parts are designed for UWB operation at a high data rate with low power consumption.

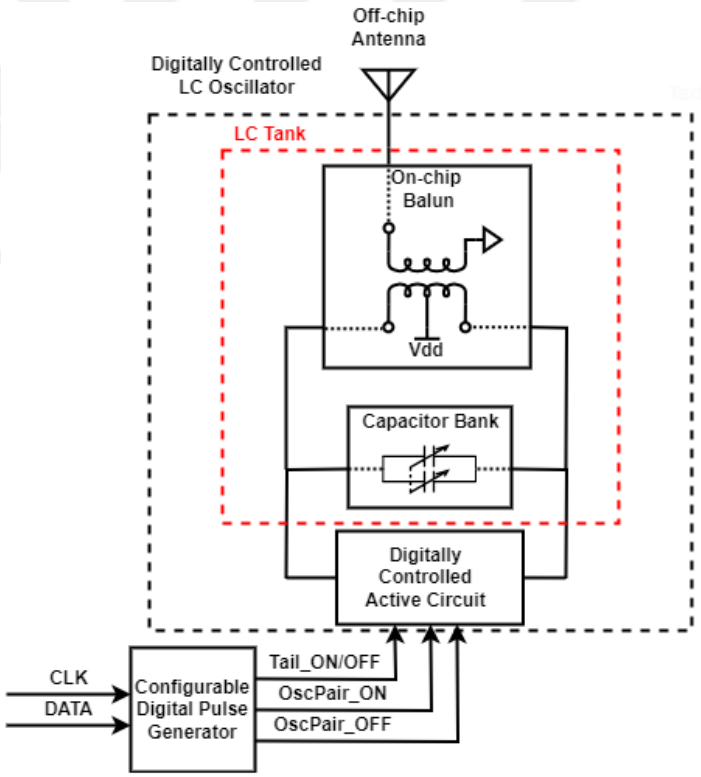


Figure 2.1. Proposed transmitter architecture.

The LC oscillator part operating at 2.4 GHz oscillation frequency is controlled by a MOS switch mechanism placed in the tail current mirroring and current-supplying transistors. Tail_ON/OFF signal turns on and off the active circuitry for low-power operation. Because fast startup is crucial for high data rate and wide bandwidth operation, an additional charge injection transistor controlled by the OscPair_ON signal

is introduced into the cross-coupled pair transistors. Also, OscPair_OFF controlled PMOS switches are used to ensure fast shutdown and, therefore, wideband operation. These switch control pulses are generated by a configurable digital pulse generator that uses clock (CLK) and input data (DATA) signals as input pulses.

The integrated balun operating at the 2.4 GHz center frequency isolates the LC oscillator core stage from the low impedance antenna and removes the need for a buffer stage to drive 50 Ω antenna. Additionally, a capacitor bank is used to achieve the desired frequency tuning range.

All the properties of TX are configurable, and the switching mechanism ensures a very low static power consumption when the pulse transmission does not occur. The proposed TX also operates at a high data rate with high peak output power, which ultimately leads to improved overall efficiency.

2.1.1. Configurable Digital Pulse Generator

The digital control signals, Tail_ON/OFF, OscPair_ON, and OscPair_OFF are obtained by a configurable digital pulse generator in the TX architecture. Optimum values are recorded for each pulse after completing recursive simulations and the desired signal outputs of this block are plotted in Figure 2.2.

Each signal has a duration of 5 nanoseconds, and the pulse positions are determined in relation to the reference Tail_ON/OFF signal. T1 refers to the delay of the OscPair_ON signal with respect to the reference pulse, while T2 indicates the delay of the OscPair_OFF signal. These values are listed in Table 2.1.

The input DATA and CLK signals are used to generate three output signals, Tail_ON/OFF, OscPair_OFF, and OscPair_ON to digitally control the LC oscillator. No additional input signal is required for this generation. Tail_ON/OFF signal switches the tail current for low power consumption. OscPair_OFF and OscPair_ON signals adjust the pulse position and pulse shape to achieve a high-power and wideband signal

output.

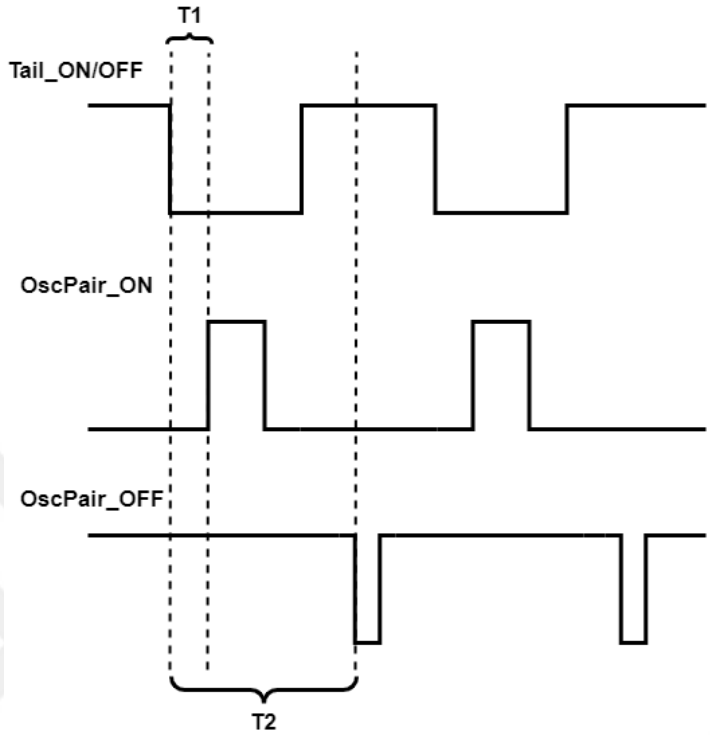


Figure 2.2. Desired output pulses for the digital pulse generator.

A set of configuration bits, <A2,A1,A0>, <B2,B1,B0>, <C2,C1,C0> and <D2,D1, D0> is used to control the pulse positions and pulse widths of the generated OscPair_OFF and OscPair_ON signals in the digital pulse generator. In addition, the configurable delay unit suppresses the process, voltage, and temperature (PVT) variations with a suitable configuration of S0 and S1 selection bits as given in Table 2.2.

Table 2.1. Parameters for Digital Pulse Generator Output Pulses.

Variable	**Tail_ON/OFF**	**OscPair_ON**	**OscPair_OFF**
Pulse width	2.5ns	0.9ns	0.3ns
Delay	-	0.8ns	3.4ns
Period (T)	5ns	5ns	5ns

Pin list for the configurable digital pulse generator block is also summarized in Table 2.3. A standard cell library including NAND2, NOR2, AND3, PASSGATE,

INVERTER (INV) and MUX2x1 designs is created to be used in the design of the subblocks of the digital signal generator.

Table 2.2. Selection bits with corresponding total delay for process corners.

Select bits <S1,S0>	**Number of Delay Cells**	**Process Corners**	**Total Delay (ns)**
00	2	P1:slow-slow	0.178
01	5	P2:typical-typical	0.380
10	9	P3:fast-fast	0.603
11	-	-	-

Table 2.3. Pin List for the Configurable Digital Pulse Generator.

Pin Name	**Pin Direction**	**Pin Description**
CLK	IN	input clock signal
DATA	IN	input data
<A2,A1,A0>	IN	configuration bit sequence for delay line #1
<B2,B1,B0>	IN	configuration bit sequence for delay line #2
<C2,C1,C0>	IN	configuration bit sequence for delay line #3
<D2,D1,D0>	IN	configuration bit sequence for delay line #4
<S1,S0>	IN	selection bit sequence for PVT supress
OSCPAIR_ON	OUT	OSCPAIR_ON control signal for LC oscillator
OSCPAIR_OFF	OUT	OSCPAIR_OFF control signal for LC oscillator
TAIL_ON/OFF	OUT	TAIL_ON/OFF control signal for LC oscillator
VDD	IN	Supply voltage signal
GND	IN	Ground signal

As shown in Figure 2.3 (a), the DATA and CLK signals enter into the On-Off Keying Modulator (OOK) block. Tail_ON/OFF signal is generated at the output of this block, and the buffered OOK output signal is also used to generate the OscPair_ON and OscPair_OFF control signals in the digital pulse generator.

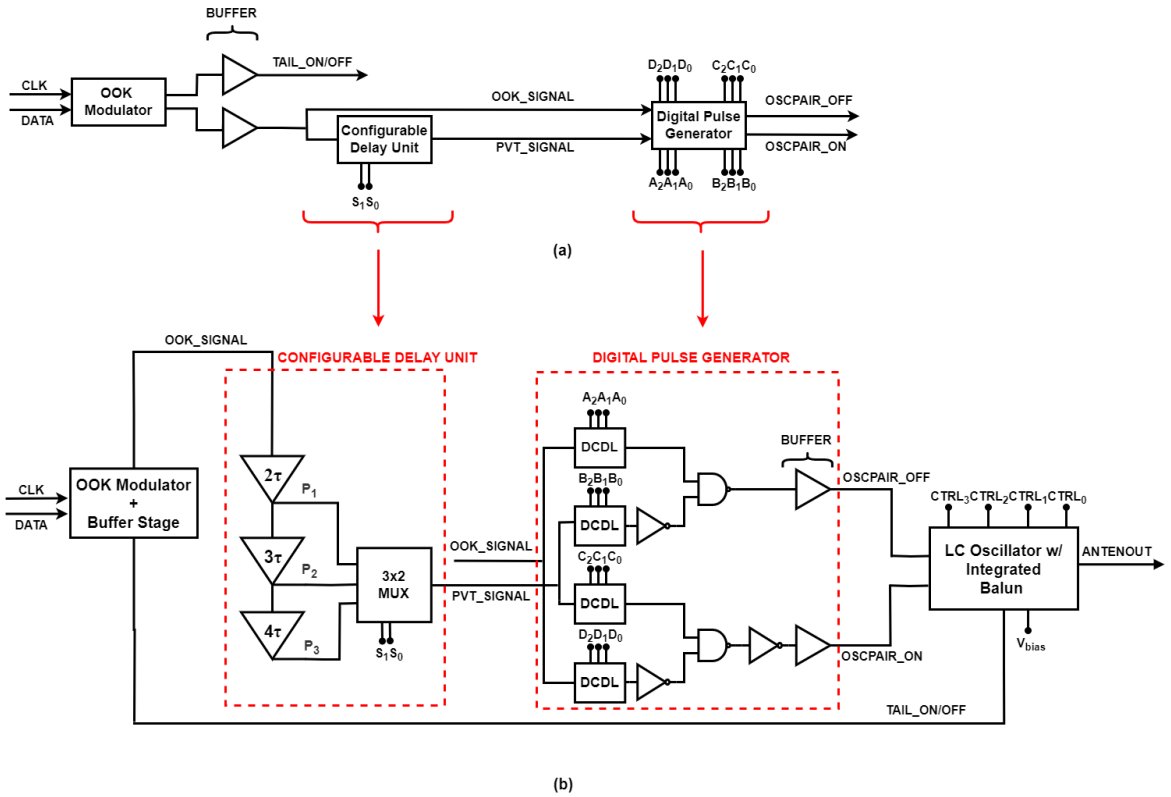


Figure 2.3. (a) Block diagram of the proposed digital pulse generator (b) Block diagram of the unified transmitter.

The adopted modulation scheme is On-Off Keying and the modulator output waveforms are plotted for the data rate of 200 Mb/s in Figure 2.4 for 010101 and 011111 input data sequences respectively where binary 1 is represented by a short pulse and binary 0 is represented by no pulse transmission [8].

The configurable delay unit consists of delay elements and a 3x2 multiplexer as shown in Figure 2.3 (b). Its function is to provide the required number of delay blocks for the process corners P1, P2, and P3, as listed in Table 2.2.

Four digitally controlled delay line (DCDL) blocks are used to generate OscPair_ON and OscPair_OFF control signals in the digital pulse generator unit. Each delay line block is controlled by a set of configuration bits <A2,A1,A0>, <B2,B1,B0>, <C2,C1,C0>, and <D2,D1,D0> respectively as shown in Figure 2.3 (b). While the set of <D2,D1,D0> is controlling the rising edge position of OscPair_ON signal, <C2,C1,C0>

set controls the falling edge of this pulse. In the same way, <B2,B1,B0> set determines the rising edge position of the OscPair_OFF signal, while <A2,A1,A0> is controlling the falling edge.

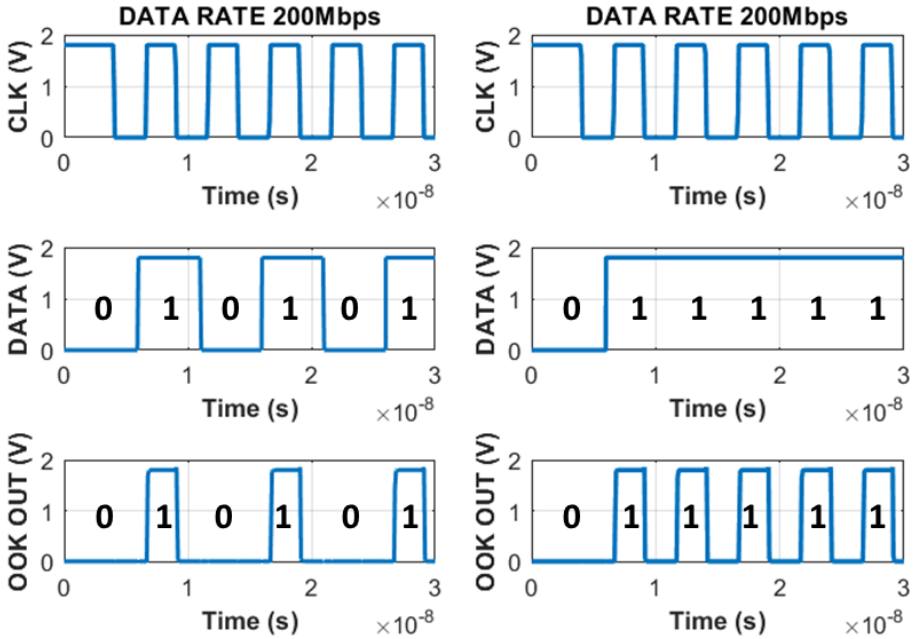


Figure 2.4. Two sets of data and clock inputs with OOK modulation output waveforms.

Rising and falling edge positions, and thus, the pulse width of these control signals are configured. A NAND gate is used to combine the rising and falling edges of each signal to form the final pulse.

The different PVT_SIGNAL outputs composed according to the process corner selections are plotted in Figure 2.5 (a). The generated OscPair_ON and OscPair_OFF control signals are also plotted in Figure 2.5 (b). The three signals, Tail_ON/OFF, OscPair_ON and OscPair_OFF which are generated by the digital pulse generator block, are fed to the oscillator-based TX as in Figure 2.3 (b), and the UWB output signal shown in Figure 2.5 (c) is obtained at the antenna output.

Digitally controlled delay lines play an important role in the configuration and signal generation of the transmitter. As given in the circuit diagram in Figure 2.6, a 3x8 decoder is used to generate control bits for each PMOS transistor. Each PMOS

transistor acts as a resistor and is turned on/off with the control bits <O7:O1>. One-cold coding (all bits are 1 except one 0) is employed to reduce the impact of parasitics on the step size of the delay line. According to the total equivalent resistance value, the voltage V_{gate} changes in a range. This part works as a digital-to-analog converter, which receives 3 digital inputs, <A2,A1,A0>, and generates an analog output, V_{gate}.

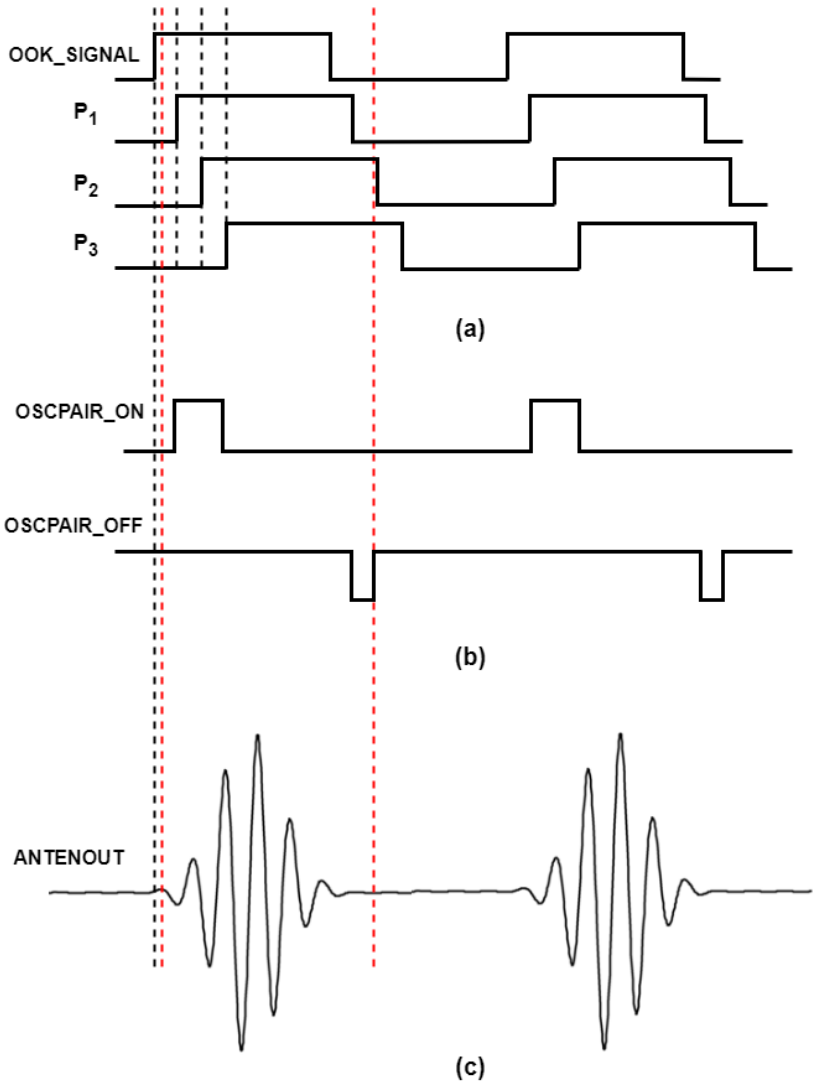


Figure 2.5. (a) Input and output waveforms of the configurable delay unit (b) Output waveforms of the digital pulse generator (c) TX output waveform at the antenna.

The remaining circuit is a current-starved voltage-controlled delay line implementation. The current passing through the NMOS transistors at the tail, and thus the delay of the inverters, is controlled by V_{gate}.

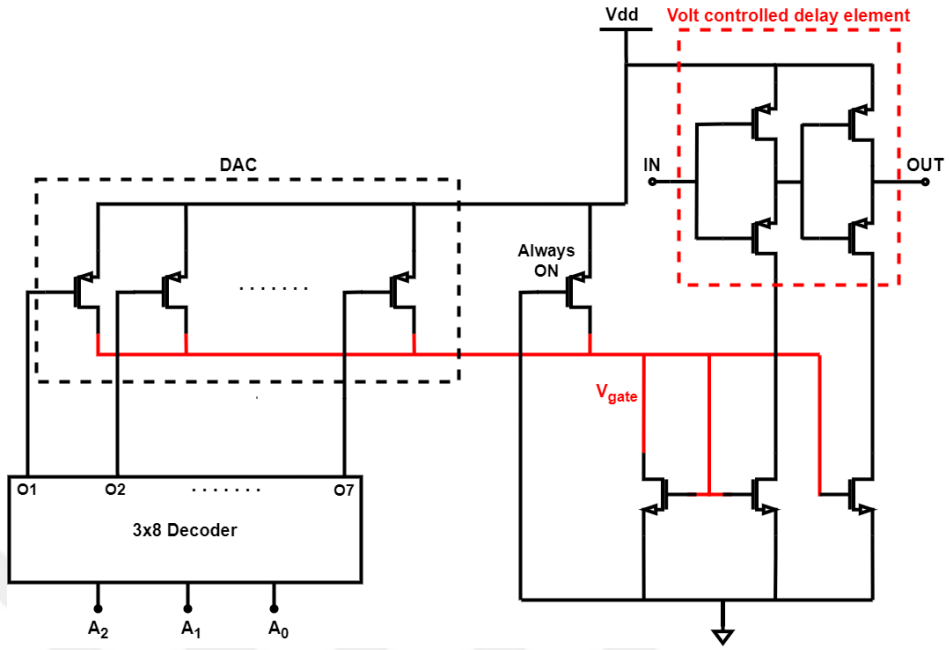


Figure 2.6. Schematic of the digitally controlled delay line.

Digitally controlled delay lines ensure different positions and widths of the OscPair_ON and OscPair_OFF control pulses of TX, and hence tunable output pulse position and width in the transmitter circuit.

For specific values of <A2,A1,A0>, <B2,B1,B0>, <C2,C1,C0> and <D2, D1,D0> control bits, the digitally configurable pulse generator outputs the OscPair_ON and OscPair_OFF signals with minimum and maximum widths. The starting point of the pulses is also configured with these sets of bits, and the related results of the post-layout simulation are shown in Figure 2.7.

The pulse positions and pulse widths of the generated signals are listed in Table 2.4. Tail_ON/OFF signal output is taken as a reference and the pulse start values are recorded according to this reference. When all control bits are 1, the OscPair_ON and OscPair_OFF signals have a minimum width. In the second configuration of the control bits, pulses with maximum widths are generated. The most delayed and minimum width versions of the pulses of OscPair_ON and OscPair_OFF are listed in the third row of Table 2.4.

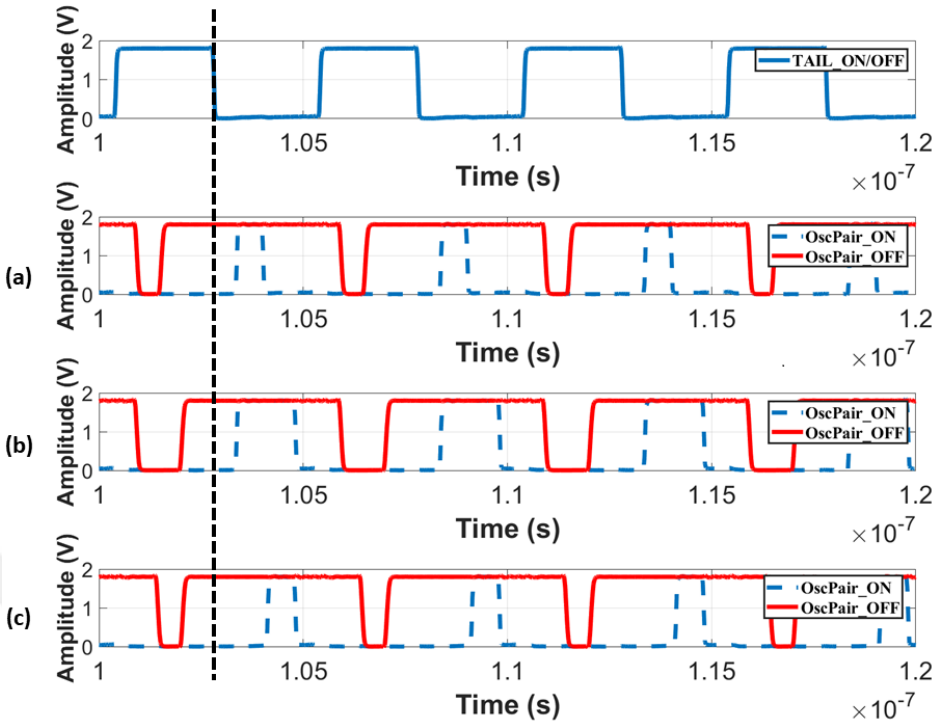


Figure 2.7. Tail_ON/OFF waveform with OscPair_ON and OscPair_OFF signals which are generated with different configuration of control bits. (a) The least delayed and min width, (b) the max width, and (c) the most delayed and min width cases.

Table 2.4. Pulse position and width values for OscPair_ON and OscPair_OFF signals with different configurations of control bits.

	<A2,A1,A0>	<B2,B1,B0>	<C2,C1,C0>	<D2,D1,D0>	OscPair_ON		OscPair_OFF	
					pulse start	pulse width	pulse start	pulse width
(a)	<1,1,1>	<1,1,1>	<1,1,1>	<1,1,1>	0.39 ns	0.82 ns	2.64 ns	0.76 ns
(b)	<1,1,1>	<0,0,0>	<0,0,0>	<1,1,1>	0.39 ns	1.55 ns	2.61 ns	1.42 ns
(c)	<0,0,0>	<0,0,0>	<0,0,0>	<0,0,0>	1.12 ns	0.78 ns	3.21 ns	0.78 ns

The layout view of the configurable digital pulse generator block is given in Figure 2.8.

For 200 Mb/s data rate and desired TX UWB operation region, the required control pulses are generated by the configurable digital pulse generator as shown in Figure 2.9. The input DATA and CLK signals are plotted with the generated Tail_ON/OFF, OscPair_ON, and OscPair_OFF signals for this block.

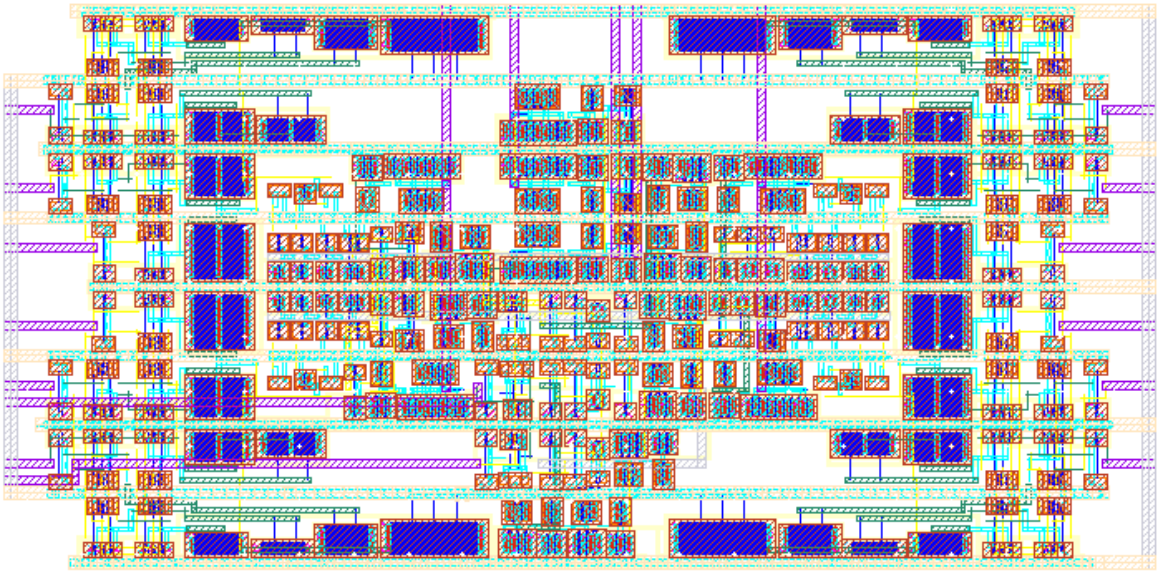


Figure 2.8. Layout view of the Digital Pulse Generator.

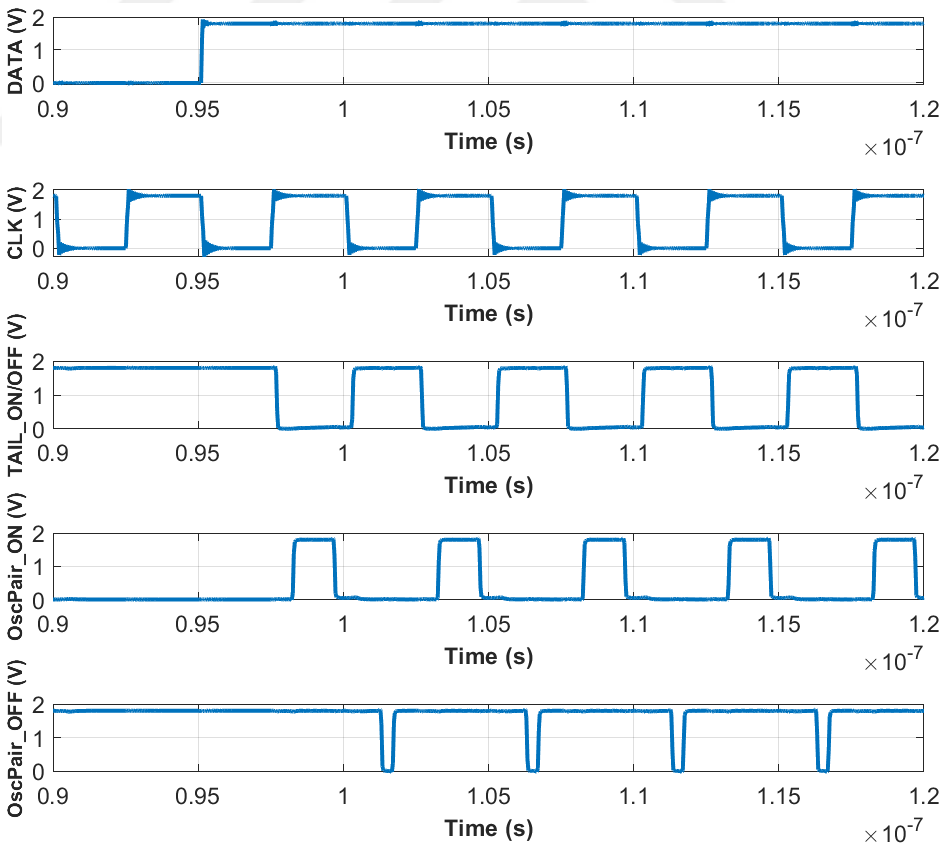


Figure 2.9. Input and output waveforms of pulse generator for 200 Mb/s data rate.

2.1.2. Digitally Controlled LC Oscillator

The implemented oscillator consists of cross-coupled NMOS pair transistors and an LC tank, which is a combination of a 5 nH on-chip balun and a switched capacitor array plus a MOS varactor structure, namely the frequency tuning block as shown in Figure 2.10.

The pulse-controlled cross-coupled LC oscillator architecture is designed with a fast startup and discharging mechanism for high data rate and wide bandwidth operation and many features of the TX can be reconfigured with the digital control signals generated by the digital pulse generator discussed in Section 2.1.1. The tail current source transistor, M3, is turned on and off by using an NMOS switch, M_SW1, controlled by Tail_ON/OFF signal to limit static power consumption. During periods of no data transmission, M_SW1 forces the gate voltage of M3 tail transistor to zero, effectively halting the current flow through the circuit. Only a small amount of current is dissipated by the digital pulse generator block, which is responsible for generating the digital configuration signals, Tail_ON/OFF, OscPair_ON, and OscPair_OFF. As the width of the cross-coupled transistors increases, the start-up time decreases for the transmitter. Yet, the parasitic effects increase at the same time [55]. Considering parasitic capacitance limitations, the cross-coupled pair transistors, M1 and M2, are sized as 10*10 μm/0.18 μm.

The setup time for the oscillation can be defined as the combination of the off time and the time taken for the output voltage to reach 1% of the peak-to-peak output voltage [36]. Some significant amount of power is consumed by the turned-on LC oscillator during setup time and does not contribute to the output waveform. For a symmetric LC VCO architecture, it is possible to reduce the setup time by decreasing the tank Q value, but it requires increased biasing current, thus leading to higher power dissipation [40]. Without increasing the power consumption, a charge injection MOS transistor, M_SW2 is introduced into the cross-coupled transistors to reduce the setup time and obtain the maximum output pulse energy.

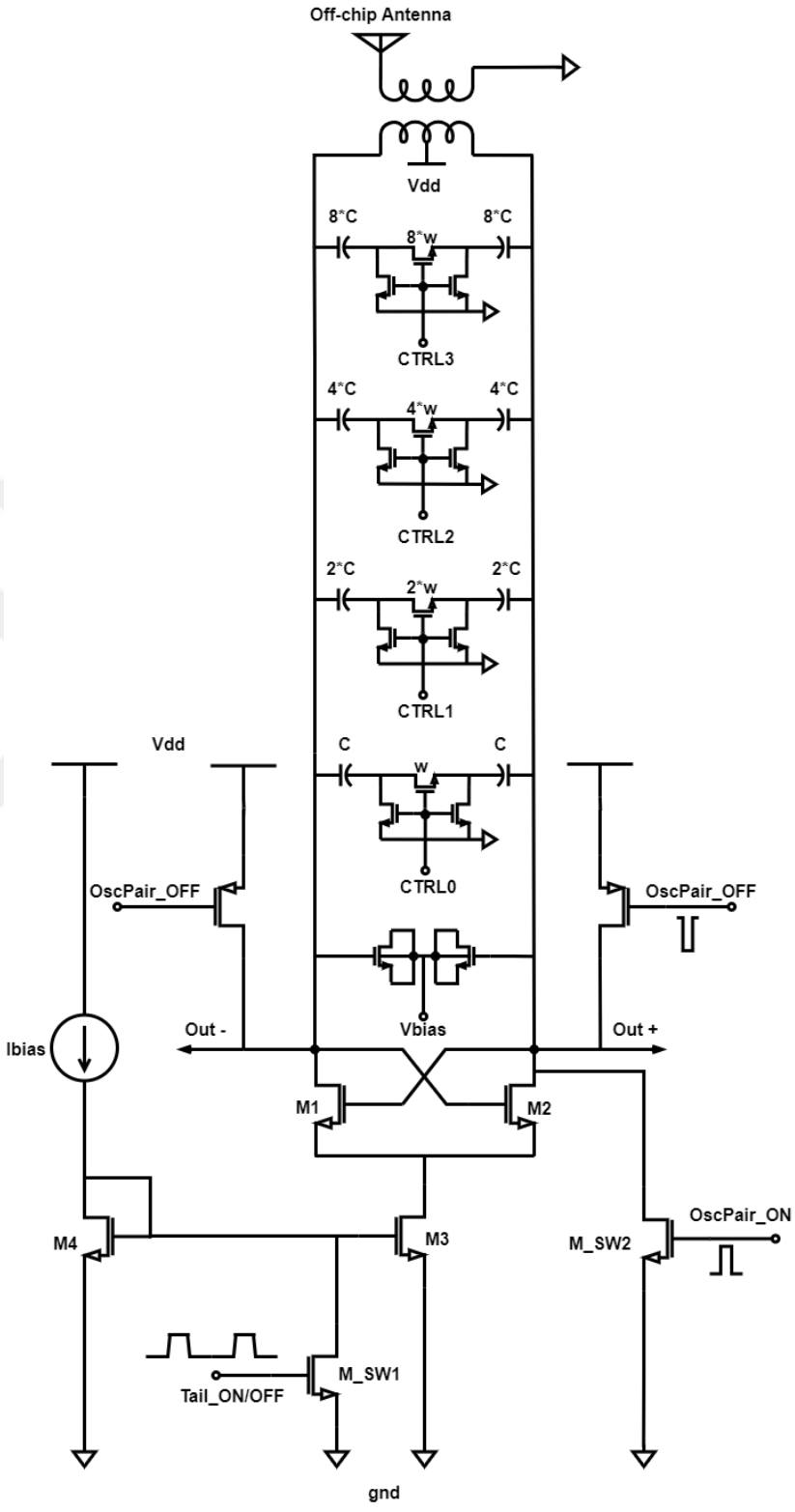


Figure 2.10. Schematic view of the proposed transmitter based on a cross-coupled LC oscillator.

OscPair_ON signal controlling the switch, M_SW2 connected to the drain of the pair transistor, M2 turns on this transistor with the incoming pulse and ensures fast start-up. OscPair_OFF signal controls the upper PMOS switches, M5 and M6, connected to the drain of both pair transistors. It provides faster discharging after the output signal reaches the peak value, thus enables higher bandwidth with less power.

The center frequency determined by the LC resonator is chosen as 2.4 GHz, where the oscillation frequency is given by

$$\omega_o = \frac{1}{\sqrt{L_{\text{balun}} \times (C_{\text{tot}} + C_{\text{var}} + C_{\text{par}})}} \tag{2.1}$$

where C_{tot} is the binary weighted total of the switched capacitor array, C_{var} is the tunable varactor capacitance, and C_{par} to include parasitics associated with the transistors and the layout.

The LC oscillator output waveform recorded before the balun stage is shown in Figure 2.11. This oscillating output waveform is given with the input CLK signal to show the on/off switching regions. As the tail transistor is activated by the pulse signal, the oscillation starts to build up and the output swing of the LC oscillator stage reaches its maximum value. The output swing is recorded as 3.2 V at a data rate of 200 Mb/s.

The LC tank employs a switched capacitor array and a small NMOS varactor combined architecture to achieve frequency tuning. As proposed in [56], a 4-bit binary weighted array of switched metal-insulator-metal (MIM) capacitors is used to divide the desired frequency region into 16 sub-bands with the configuration of differential switches, controlled by <CTRL3,CTRL2,CTRL1,CTRL0> bit set.

One important factor to consider is the size of the switched transistors as it directly impacts how the system operates. One potential drawback is the slow turn-on and turn-off time of the switched transistors, particularly when using transistors with large widths to handle high capacitance values. This slow switching speed can affect

the responsiveness of the system and may lead to inefficiencies in frequency tuning. Conversely, using small-sized transistors can introduce additional losses to the tank due to their finite resistance. The sizing of the switched transistors are chosen properly to minimize the losses due to their finite resistance while maintaining adequate switching speed. CTRL0 bit turns on/off the switch transistor with 1 μm width, connected to 50 fF capacitors. CTRL1, CTRL2, and CTRL3 bits are connected to switches with 2 μm, 4 μm, and 8 μm width respectively and they control 100 fF, 200 fF, and 400 fF capacitors.

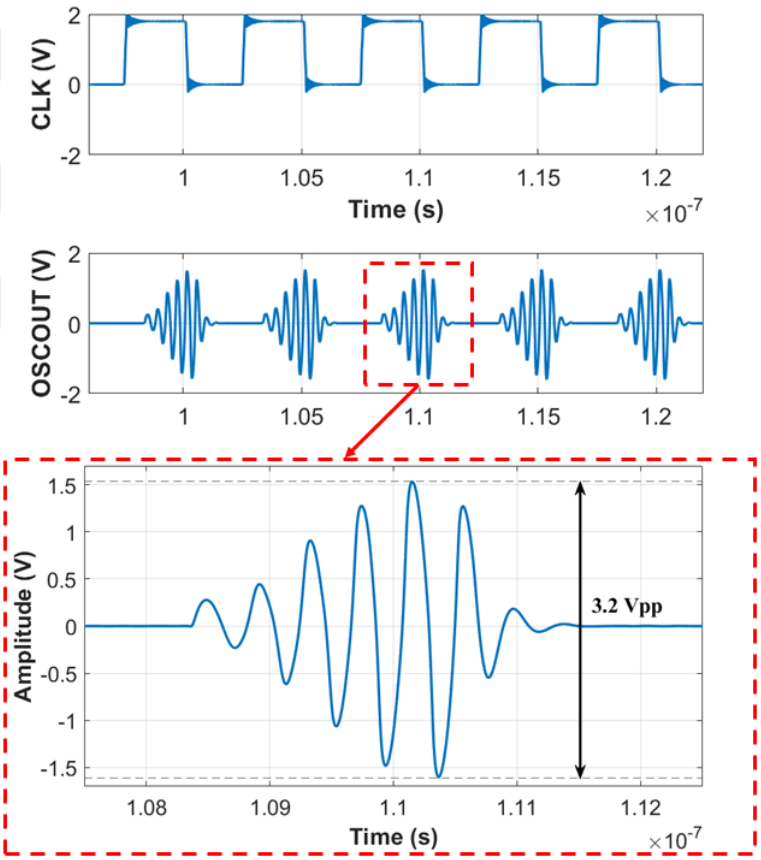


Figure 2.11. Switching clock input and the oscillator output waveforms and zoomed view of a single UWB output pulse.

Long thin NMOS transistors, M9-M16, (l=1μm, w=0.24μm) are also connected to the source and drain of each switch to provide the DC reference points in the ON state. The accumulation mode varactors, M7 and M8, of 5 μm width with a gate length of 5 μm are tuned with V_{bias} voltage to ensure continuous frequency tuning, while the switched capacitor array is responsible for coarse tuning.

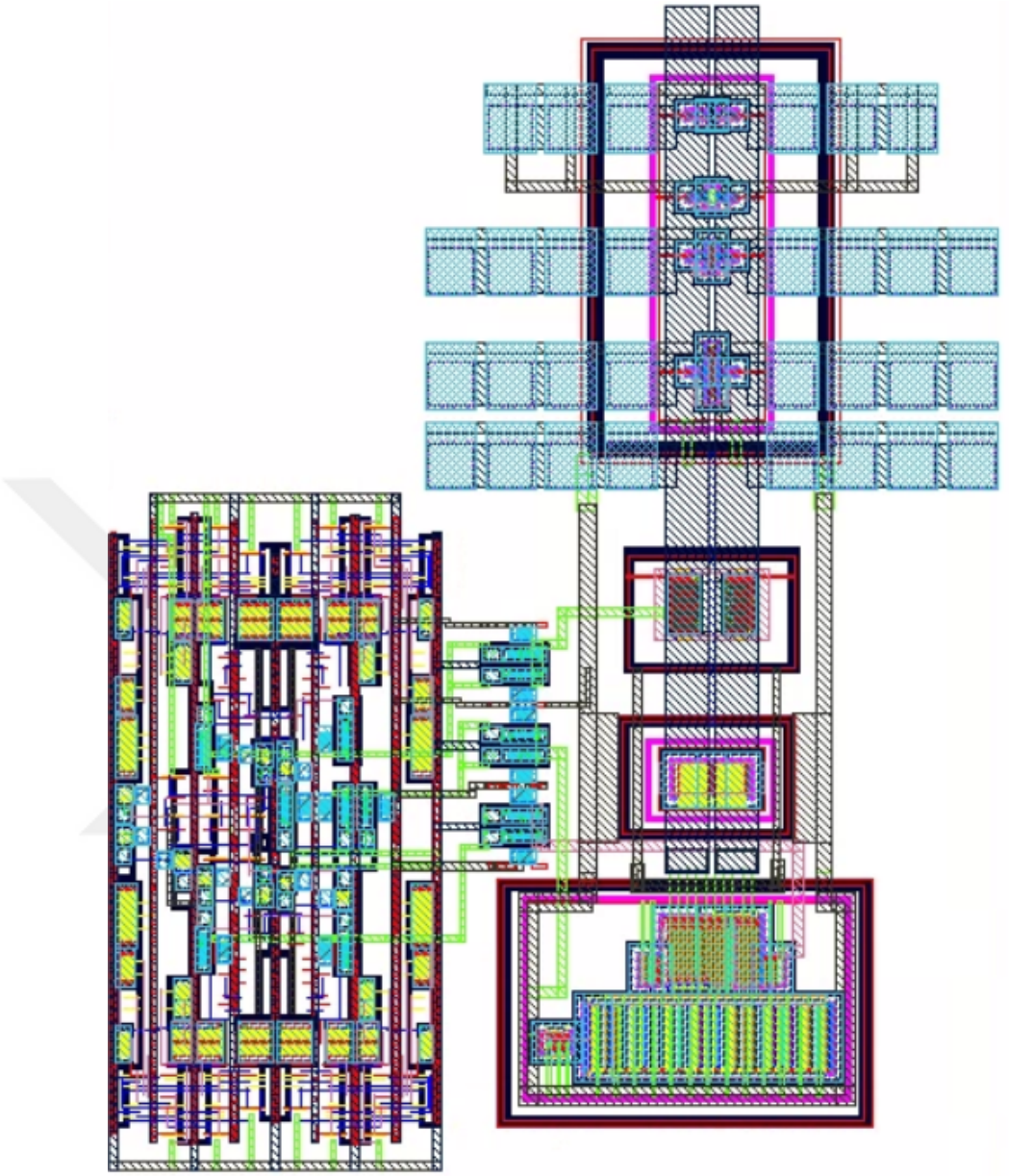


Figure 2.12. Layout of the proposed TX excluding the custom designed balun.

The layout of the overall design is given in Figure 2.12 and the post-layout simulation results depicted in Figure 2.13 indicate that the proposed TX architecture is capable of achieving frequency tuning within the range of 2.25 to 3.25 GHz.

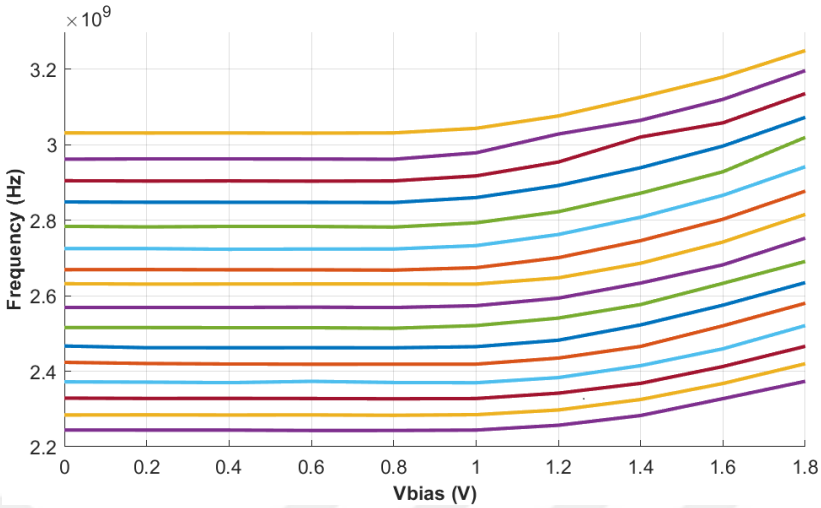


Figure 2.13. Frequency vs V_{bias} for different configuration of <CTRL3, CTRL2, CTRL1, CTRL0> bits.

2.1.3. Custom Designed On-chip Balun

In the transmitter architecture, a center-tapped transformer-based balun is employed to mitigate power dissipation in an additional output buffer stage. This configuration allows direct connection of the transformer output to a 50 Ω load, facilitating differential to single-ended signal conversion from LC oscillator outputs to the antenna load. The balun effectively matches the impedance between the transmitter circuitry and the antenna, minimizing signal reflections and ensuring maximum power transfer.

The integrated balun is specially designed based on the lumped model adapted from [57] and characterized through electromagnetic (EM) simulations using Advanced Design System (ADS) Momentum considering the physical aspects of the geometry.

The results of the lumped model simulation are plotted alongside the EM data in Figure 2.14, and the design parameters are verified at the center frequency of 2.4 GHz. Forward transmission losses from the input to the non-inverting and inverting output ports are shown in Figure 2.14(a,b). The forward insertion loss difference between the non-inverting and inverting ports of the balun is expected to be 0 dB in amplitude and 180° in phase for differential operation. Both the lumped model and

EM data simulation results in Figure 2.14(c,d) demonstrate that the phase difference is very close to 180° for the 0-5 GHz band. Additionally, the difference of insertion loss between the two output ports is below 0.5 dB for both datasets. In Figure 2.14(e), the output reflection coefficient is given for 50 Ω antenna load connection. The mutual inductance values are recorded for both sides, the antenna and the oscillator ports, as illustrated in Figure 2.14(f) and (g), respectively.

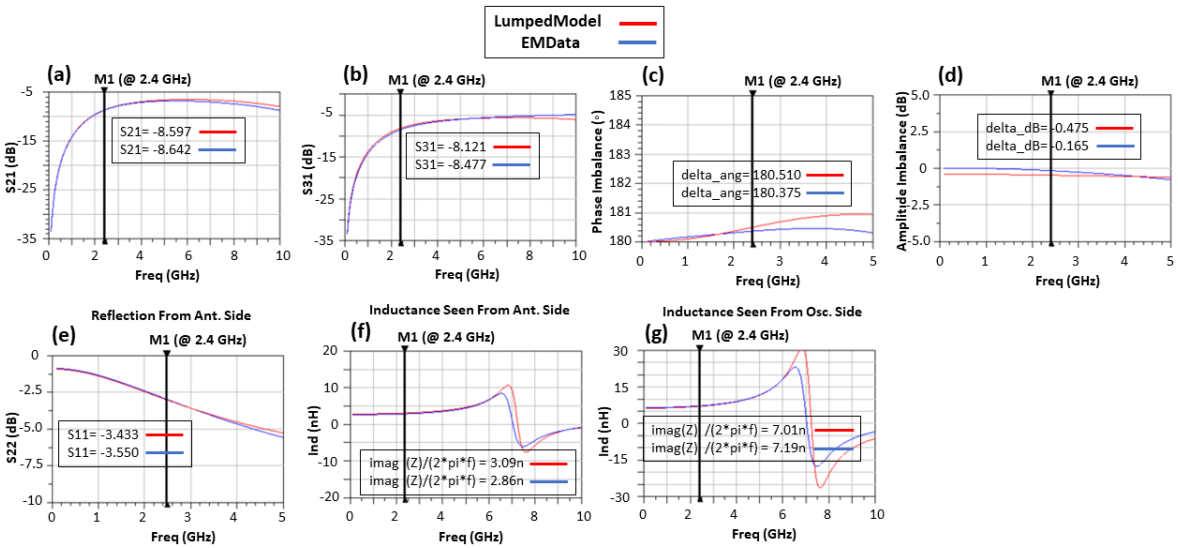


Figure 2.14. Simulation results for the custom-designed balun including both the lumped model and EM data: (a,b) Forward transmission loss for inverting and non-inverting output ports, (c,d) Phase and angle imbalance between inverting and non-inverting outputs, (e) Output reflection coefficient, (f,g) Inductance seen from antenna output and oscillator connected input ports.

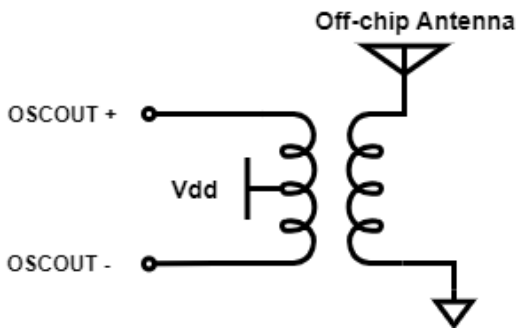


Figure 2.15. Schematic illustration of the designed balun.

The center tap is connected to the DC supply source, Vdd, while the remaining inputs are directly connected to the differential outputs of the LC oscillator. The

antenna load is connected to the output of the transformer balun to observe the transmitted pulse as illustrated in the schematic diagram of the designed balun in Figure 2.15.

The layout of the designed planar interleaved balun, along with the use case connections, is also provided in Figure 2.16. It has a width of 400 μm, with a spacing of 9 μm applied between windings. The turns ratio from primary to secondary windings is 2 to 1, and thus the impedance ratio from the oscillator output to the antenna load is 4:1. This impedance reflection relieves the matching criteria in the oscillator design.

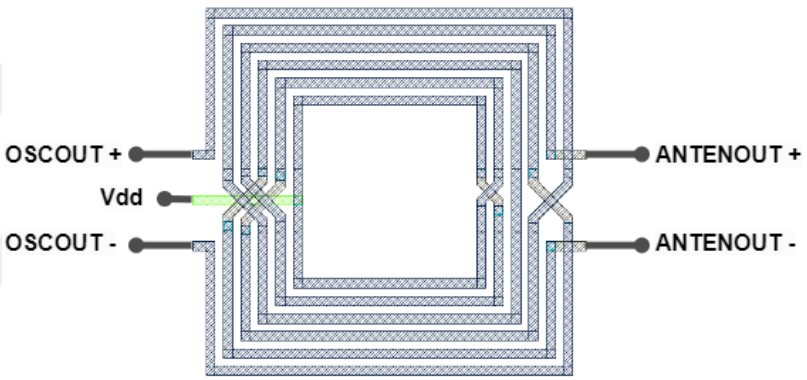


Figure 2.16. Layout of the custom-designed balun.

The 2:1 turns ratio is the optimal design decision for the proposed TX architecture. If the turns ratio was 1:1, this design would not be able to drive the 50 Ω antenna load. Similarly, with a larger ratio, such as 3:1, the output swing would be lower, resulting in a lower efficiency value. The output swings for both the oscillator and the antenna outputs versus the turns ratio plots are shown in Figure 2.17(a) with an ideal transformer balun having variable turns ratio values:1, 1.5, 2, 2.5, 3, and 3.5. Although the total average power consumed remains nearly constant across different sample turns ratio values, the maximum values for output pulse energy and efficiency are obtained with a 2:1 ratio, as revealed in Figure 2.17(b,c,d).

The need for a buffer stage is eliminated with the usage of custom-designed balun, resulting in a higher peak-to-peak output voltage achieved with reduced power consumption. As a result, the transmit power of the proposed design increases without

additional power consumption.

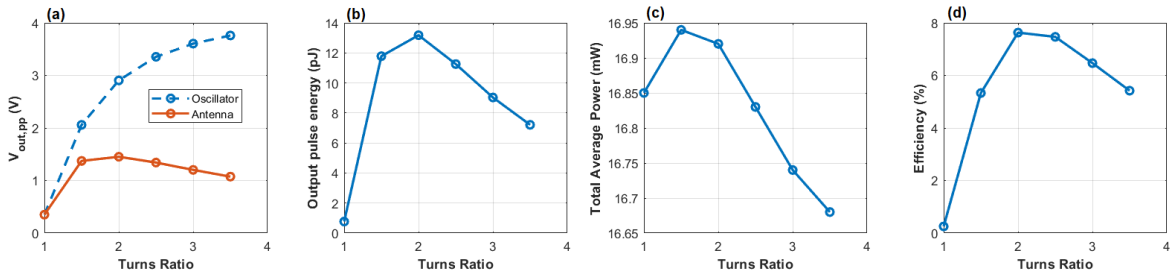


Figure 2.17. Balun Turns Ratio vs. (a) Voltage swing at Oscillator and Antenna Outputs, (b) Generated pulse energy, (c) Total Power, (d) Efficiency.

For the given input DATA and CLK signals, the final generated Tail_ON/OFF, OscPair_ON, and OscPair_OFF signals along with the oscillator and antenna output waveforms, OSCOUT and ANTENOUT, are presented in Figure 2.18. According to post-layout simulations, the recorded peak-to-peak output voltage in the antenna load is 1.2 Volts, as shown in Figure 2.19.

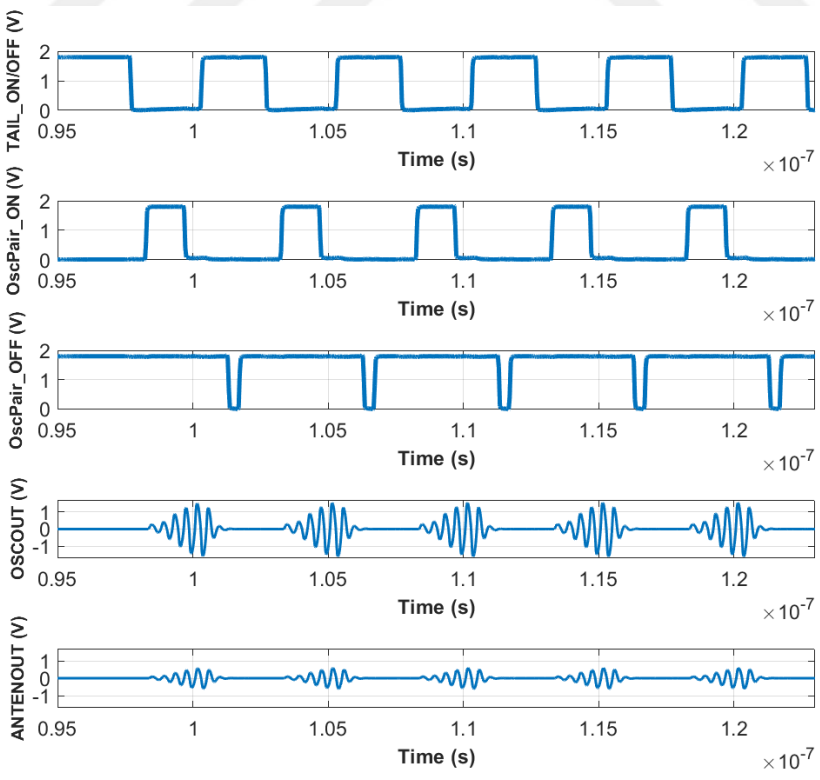


Figure 2.18. LC Oscillator control pulses and their corresponding oscillator and balun outputs.

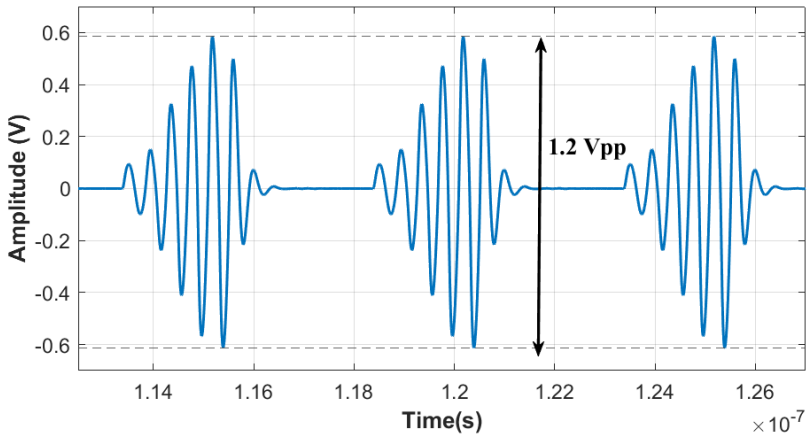


Figure 2.19. Zoomed view of the output pulses at 50 Ω load.

Changes in pulse position and pulse width of the output waveform, ANTENOUT, for different configurations of OscPair_ON and OscPair_OFF signals, are illustrated in Figure 2.20.

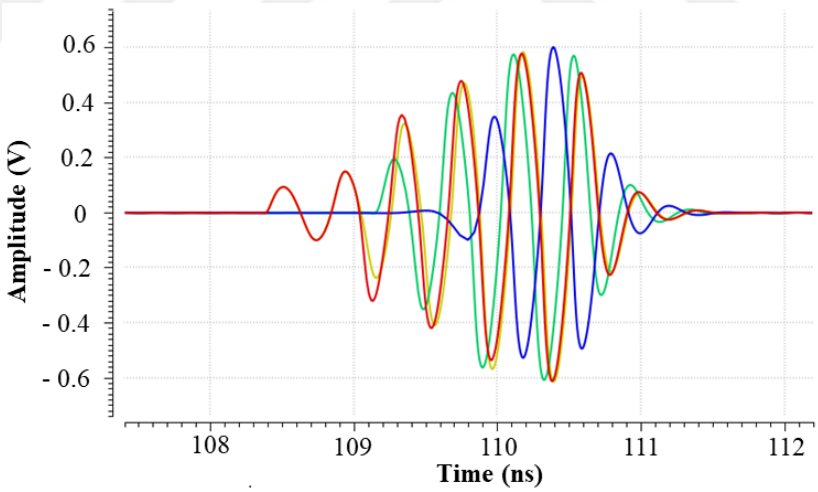


Figure 2.20. ANTENOUT waveforms for different configurations of control bits.

Both the time domain and frequency domain representations of the waveforms are presented in detail for each output pulse in Figure 2.21. The register map used to identify the different configurations is given in Table 2.5.

The center frequency of each output pulse is 2.4 GHz, with recorded bandwidth values of 1.13 GHz, 1.65 GHz, 1.04 GHz, and 995 MHz for C1, C2, C3, and C4 configurations, respectively, thus confirming the UWB operation.

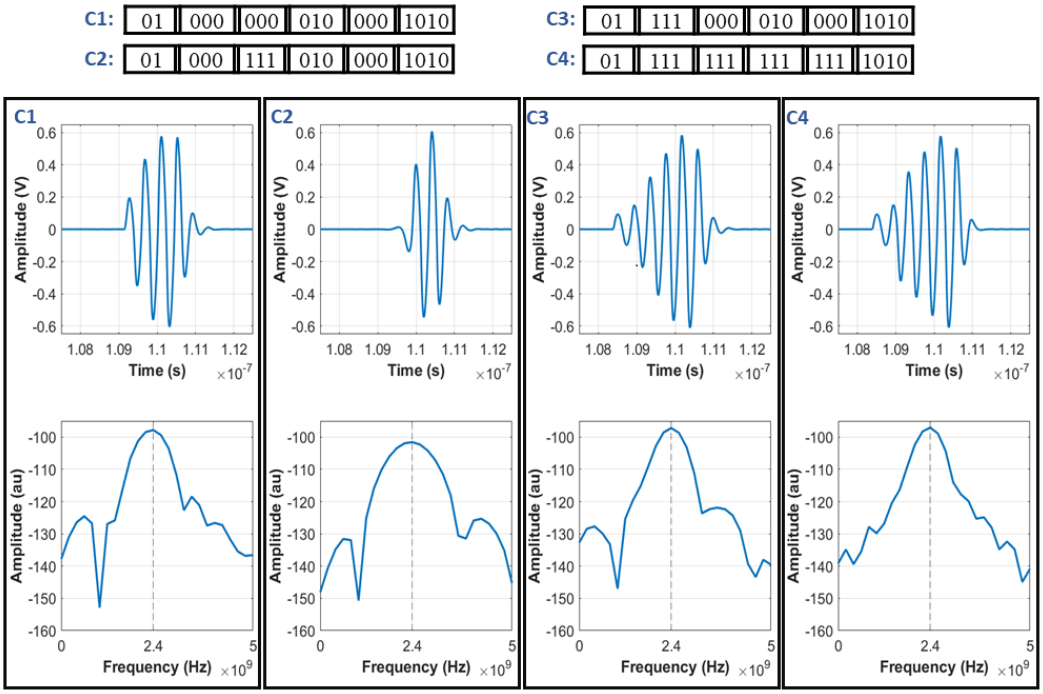


Figure 2.21. ANTENOUT waveforms in time and frequency domains with different configurations of OscPair_ON/OFF control signals.

Table 2.5. Register map for the control bits.

PVT variation control bits	OscPair_ON signal rising edge control bits	OscPair_ON signal falling edge control bits	OscPair_OFF signal rising edge control bits	OscPair_OFF signal falling edge control bits	Frequency tuning range control bits
S1 S0	D2 D1 D0	C2 C1 C0	B2 B1 B0	A2 A1 A0	CTRL3 CTRL2 CTRL1 CTRL0

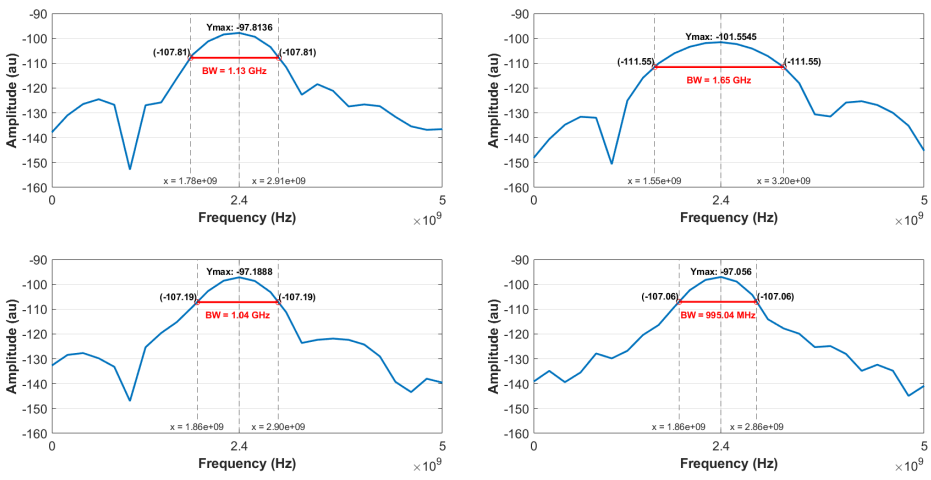
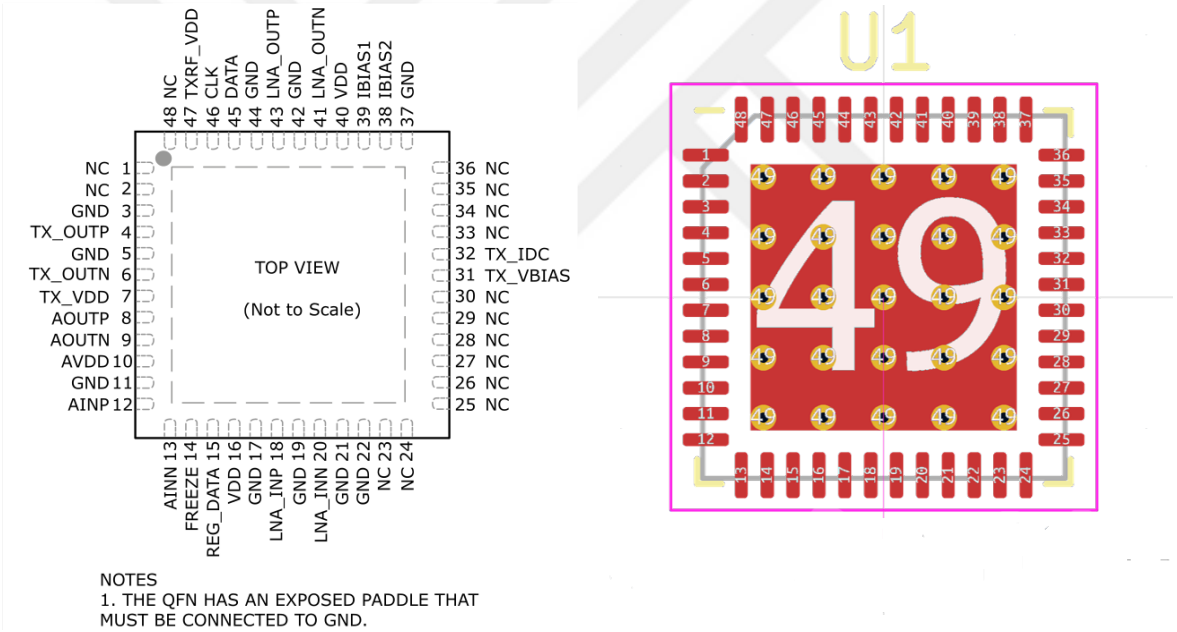


Figure 2.22. BW calculation details for ANTENOUT output waveforms in frequency domain.

2.1.4. PCB Design

A printed circuit board is designed to expose the chip's pins and connect them to necessary supplies and measurement equipment. KiCad is used as EDA/electronic CAD software to design the component libraries, schematic, and layout of the PCB. Firstly, a component library is created for the chip. The component library consists of two parts. One is the symbol that is used in the schematic to help with the wiring and the other one is the footprint which includes the dimensions of the physical package for soldering and assembly. The symbol is created based on the pin-out diagram of the chip. The pin-out diagram is given in the below Figure 2.23(a).



(a) (b)

Figure 2.23. (a) Pin-out diagram of the chip (b) 48-pin QFN package.

The package of the chip is a 7x7mm 48 Pin Quad Flat No-lead (QFN) package. The footprint was created using the package outline dimensions of the 48-pin QFN package. The designed footprint is given in Figure 2.23(b).

The next step of designing a PCB is schematic capture. Schematic capture provides a visual representation of the electrical connections between parts. In the schematic capture stage, decoupling capacitors, test points, and SMA connections are

placed and an electrical connection to the chip is realized. Various decoupling capacitors are placed on supply lines to reduce the external noise and emission on the supply. An RF Bead is placed on to supply line in series to suppress the RF emissions coming from supply lines. 100nF capacitors are placed to dampen high-frequency ripples and higher value, 10uF, capacitors are placed to reduce low-frequency noise contribution.

SMA connectors are placed onto high-frequency RF lines to create an easy interface between DUT and measurement equipment. Additionally, sensitive high-frequency digital inputs are connected to SMA connectors to eliminate external noise contribution from the environment. For power supplies, a male header with a 2.54 mm pitch is used to be able to connect external supplies via Dupont cables. After completing the schematic capture, the next step is layout design. The completed schematic capture can be seen in the Figure 2.24.

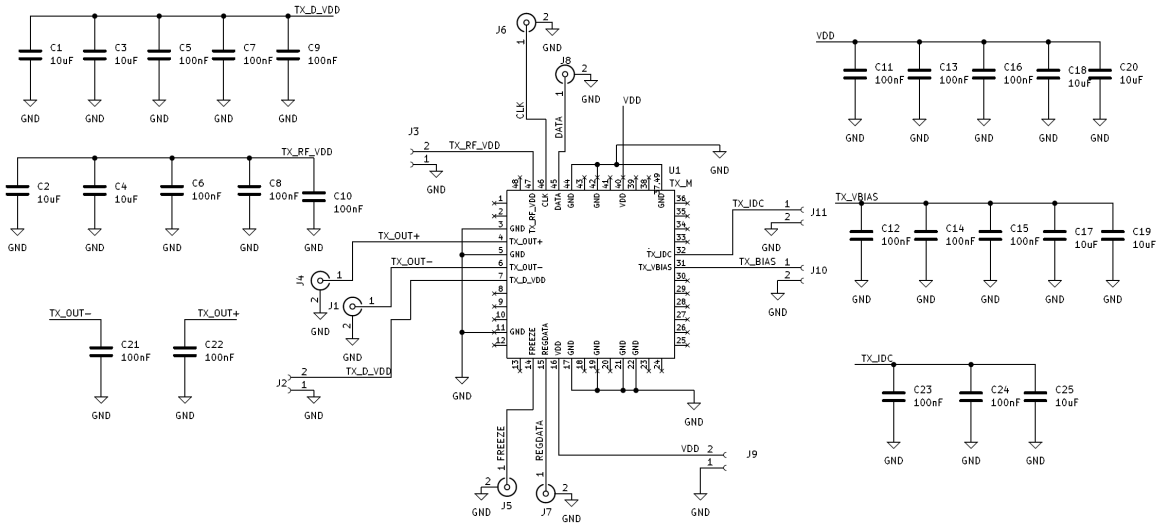


Figure 2.24. Top level schematic view of the PCB.

In the layout design, components are placed on the actual circuit board and copper traces for electrical connections are routed. The layout consists of multiple layers of conductive copper and substrates. These layers are called stack-up. This design can be realized using a 2-layer stack-up. There are top and bottom copper plates and in between them, there are dielectric substrates called FR4. There are certain good engineering practices at the layout design stage. The good engineering practices followed in this design are given below.

- In the schematic capture, decoupling capacitors with different values are connected in order to reduce supply noise contributions. In the layout design, these decoupling capacitors are placed carefully as close to the supply input of the chip as possible. As stated in [58], the location of an SMT decoupling capacitor relative to an IC can impact the noise performance of the DC power bus for certain PCB stackup configurations. Local decoupling can effectively reduce high-frequency power bus noise.
- High-frequency transmitter output and sensitive digital inputs are routed using a grounded coplanar waveguide. Grounded coplanar waveguide is a type of microstrip transmission line. Unlike microstrip transmission line, the coplanar waveguide has ground traces near the transmission line and VIAs to the bottom ground plane to guide the electromagnetic wave transmission [59]. The below figure gives a cross-section of a coplanar waveguide, 2.25. In the PCB stackup, the thickness of the copper layer (T) is 35 um. The thickness of the PCB substrate (H) is 1.6mm. These numbers are manufacturing parameters supplied by the manufacturer. Various PCB manufacturers can provide different copper and substrate thicknesses. The grounded coplanar waveguide is matched to 50 ohm impedance. The dielectric constant of the FR4 substrate is 4.6. Using these numbers, the width (W) of the trace is calculated as 1 mm and the separation (S) between the ground and the trace is calculated as 0.2 mm.

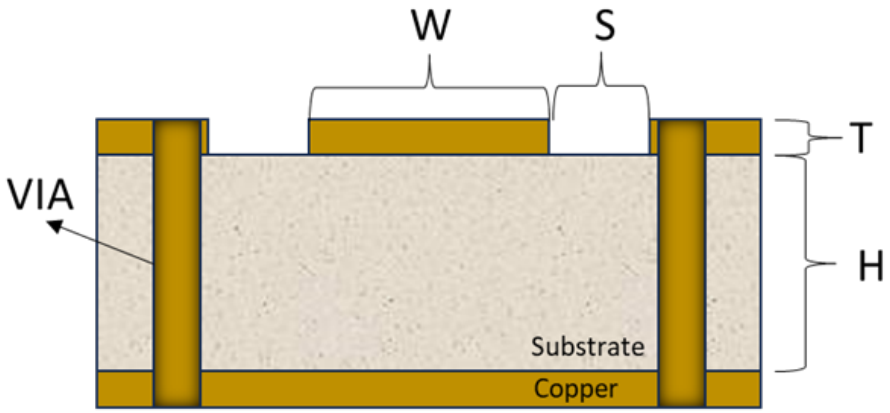
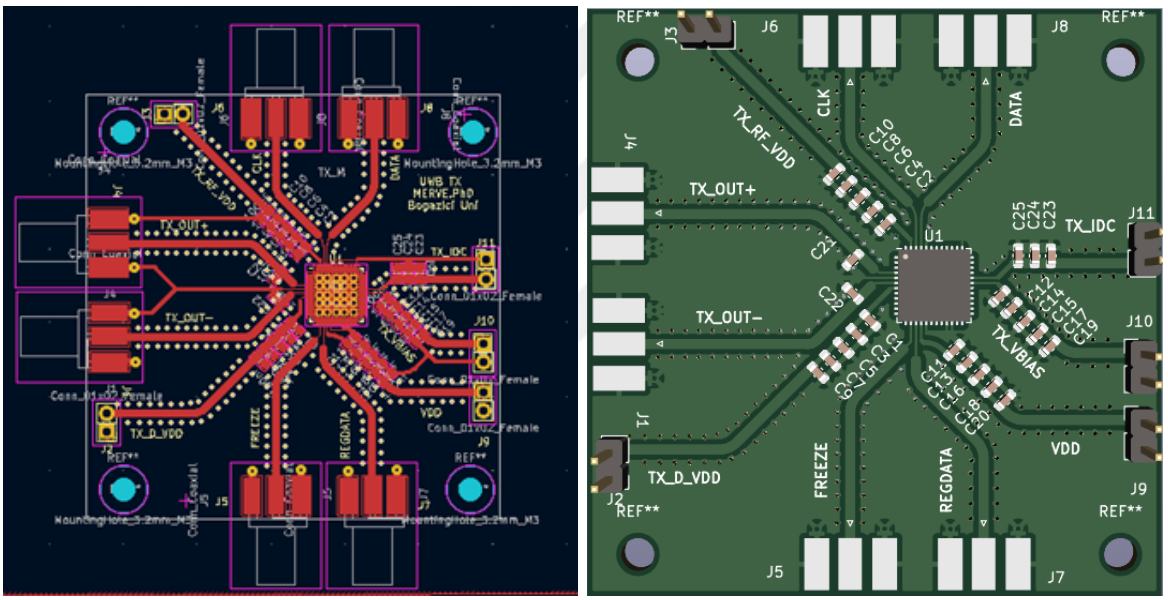


Figure 2.25. Cross-section of a coplanar waveguide.

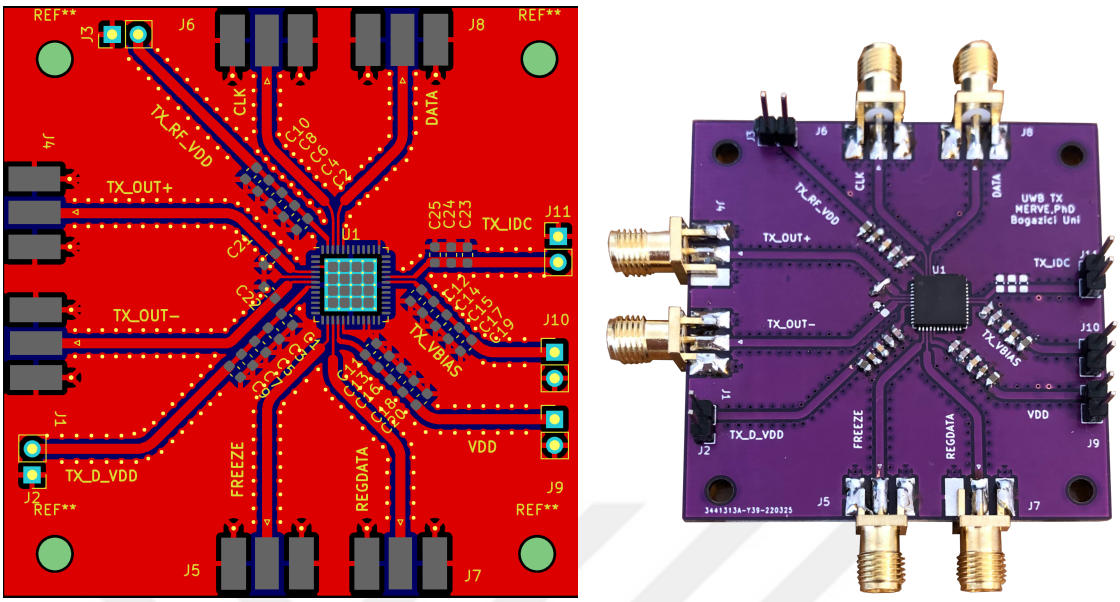
- To provide adequate grounding throughout the PCB, ground VIAs are placed along the PCB surface to connect the top and bottom layers. The unpopulated areas of the PCB are poured with ground copper. Pouring ground into unpopulated areas improves the PCB's noise susceptibility.
- Pouring ground into unpopulated areas also increases the thermal mass of the PCB. Because this PCB will be exposed to soldering rework for test purposes, thermal reliefs are placed on the passive component's ground pins in order to reduce the heat exposure time and ease the rework.



(a) (b)

Figure 2.26. (a) Layout and (b) 3D views of the PCB.

After placing components and routing the traces between components, Electrical Rule Check (ERC) and Desing Rule Check (DRC) procedures are followed. EDA Tools like KiCad provide a good interface to set the electrical and design rules. These rules mostly consist of minimum trace thickness, clearance between different traces and components, and minimum and maximum drill hole widths. After clearing the ERC and DRC errors, PCB can be exported to manufacturing files also known as Gerber files. These Gerber files are the files that are understandable by the PCB manufacturing machines. The routed layout, 3D view, gerber files output and manufactured and assembled PCB are given in Figure 2.26 and 2.27 respectively.



(a) (b)

Figure 2.27. (a) TX Gerber files output and (b) Soldered PCB board with connectors.

2.2. Receiver Architecture

Both coherent or non-coherent architectures can be used to implement IR-UWB receivers as discussed in section 1.1. The most commonly employed configurations are shown for both in Figure 2.28.

A copy of the transmitted pulse shape is used at the mixer in the template-based coherent receiver design. The coherent architecture requires precise synchronization between the transmitter and receiver, which typically results in more complex circuit design and higher power consumption. Nonetheless, it is advantageous where there is a need for high data rates with very few bit errors. On the other hand, in the energy detection non-coherent configuration, the receiver does not require a synchronized template of the transmitted signal. Instead, the received signal is squared and then integrated to obtain a representation of the signal energy. Although non-coherent receivers are typically more energy-efficient and simpler to design, they can struggle with reduced sensitivity in noisy environments.

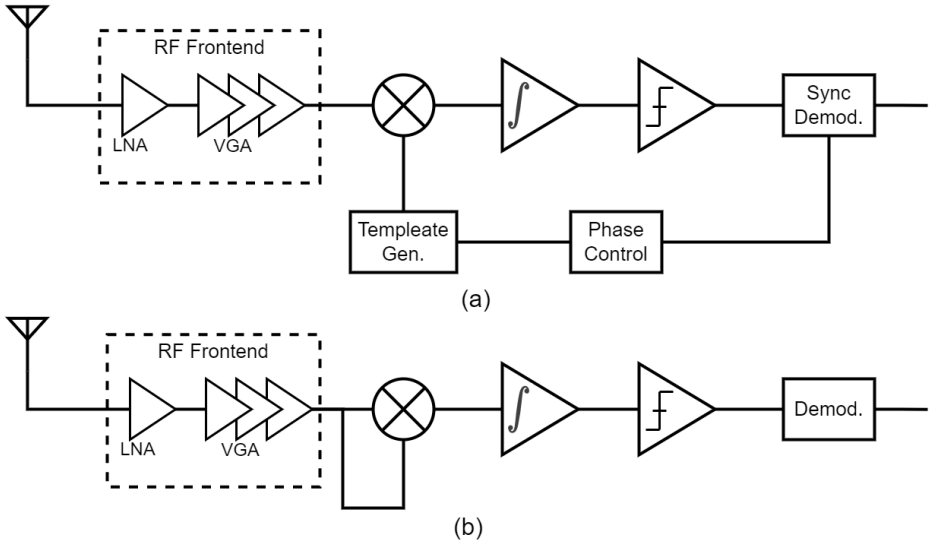


Figure 2.28. (a) Template pulse based coherent receiver (b) Energy detection non-coherent receiver.

In both coherent and non-coherent receivers, the received UWB signal is first amplified by the RF front-end, which consists of the LNA and VGA blocks. In the coherent receiver, the amplified signal is then multiplied with a locally generated template signal using a Gilbert-based multiplier, followed by integration to detect the transmitted signal. On the other hand, in the non-coherent receiver, instead of using a template, the signal is squared and integrated for energy detection [49].

The proposed LNA, VGA, and Gilbert-based mixer blocks for potential future applications in coherent or non-coherent receiver architectures are discussed in the following sections.

2.2.1. Low Noise Amplifier

As the first stage, LNA is one of the most important blocks of a typical receiver. It should provide sufficient gain to overcome the noise from the subsequent stages while minimizing its own noise contribution. In addition to this low noise figure specification, high power gain (s21), effective wide impedance matching for both input and output, high reverse isolation, and low DC power consumption is required for the LNA. The trade-off between gain, input impedance, noise figure and power consumption is the

main design issue here [60–62].

A differential common-source cascode LNA with source degeneration is implemented, as shown in Figure 2.29. The cascode LNA is preferred due to its high gain, low noise, and low power characteristics. The cascode transistor suppresses the Miller capacitance of the input device thereby enhancing the reverse isolation [63]. Additionally, a differential architecture is employed because it offers a higher common-mode rejection ratio and is less sensitive to ground inductance variation L_s compared to its single-ended counterpart. Another advantage of this architecture, it can achieve both input and noise matching using identical components close to the targeted frequency [64]. Therefore, optimal performance can always be achieved with high gain and low noise figures.

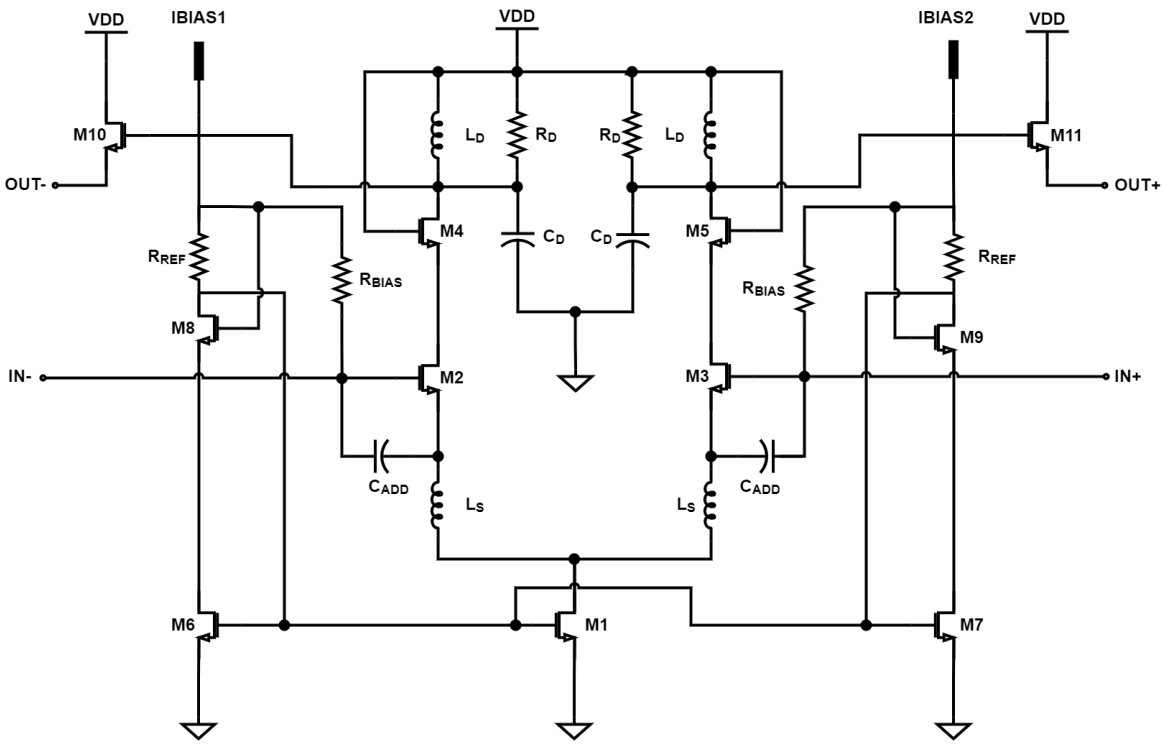


Figure 2.29. Schematic view of the proposed differential common source cascode LNA architecture.

A current mirror bias architecture is used to supply the differential amplifier with I_{BIAS1} and I_{BIAS2} supply currents. The R_{BIAS} resistor is chosen large enough such that

its equivalent noise current is negligible [65]. The M2-M4 and M3-M5 pairs form the cascode stages on both sides of the differential amplifier. The input matching network consists of L_g, an off-chip gate inductor, L_s, a source degeneration inductor, and C_{ADD}, an additional capacitor connected between the gate and source terminals of the input transistors. The C_{gs} value of the input transistors, M2 and M3, is insufficient for the noise and impedance matching requirements, so C_{ADD} is added to increase the total gate to source capacitance.

L_D and C_D, connected to the drain of the cascode transistors, function as the load for the amplifier and are used to tune the amplifier frequency. R_D load resistance is also added to reduce the loading effects at low frequencies, thus enabling a wider bandwidth. All inductive components are selected from the available circular spiral inductors in the UMC 180-nm design library, using their given measured characteristics and geometry parameters.

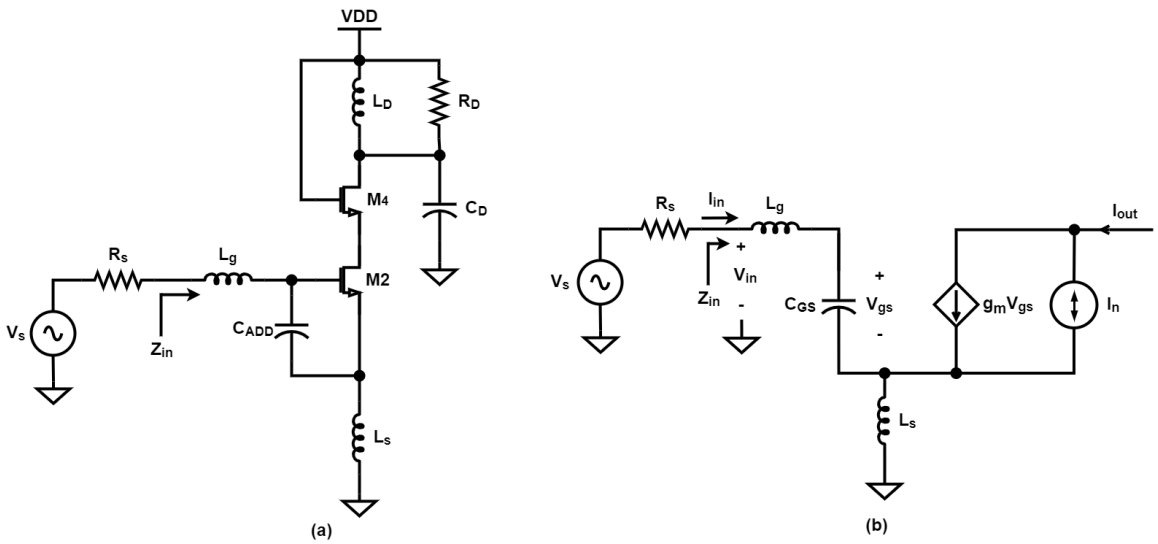


Figure 2.30. (a) Half circuit schematic view of the proposed LNA (b) the small-signal model of the input transistor.

The half circuit shown in Figure 2.30 (a) is used for the small signal analysis of the design due to the fully differential architecture. The input impedance, Z_{in} is determined using the equivalent transistor model given in Figure 2.30 (b), as discussed in [66]:

$$V_{in} = jwL_gI_{in} + \frac{I_{in}}{jwC_{GS}} + jwL_s(I_{in} + g_mV_{gs}) \tag{2.2}$$

where

$$V_{gs} = I_{in}\frac{g_m}{jwC_{GS}}. \tag{2.3}$$

Thus, the input impedance is given by

$$Z_{in} = \frac{V_{in}}{I_{in}} = jw(L_g + L_s) + \frac{1}{jwC_{GS}} + \frac{g_mL_s}{C_{GS}} \tag{2.4}$$

where

$$C_{GS} = C_{gs} + C_{ADD}. \tag{2.5}$$

For maximum power transfer, Z_{in} should be equal to the complex conjugate of the source impedance, R_s. Thus, from equation 2.4:

$$jw_0(L_g + L_s) + \frac{1}{jw_0C_{GS}} = 0 \tag{2.6}$$

$$Rs = \frac{g_mL_s}{C_{GS}} = 50\,\Omega. \tag{2.7}$$

The resulting operating frequency formula is

$$\omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{GS}}}. \tag{2.8}$$

The value of the source degeneration resistance is determined by the maximum allowable inductance size based on the process technology [61]. For our design, an L_s inductor with a value of 1.2 nH was selected from the UMC 180-nm design library. Using the optimal quality factor of the inductor, the L_g value was also determined. Based on equation 2.8, C_{GS} was calculated, followed by the design parameters, including the transistor width, g_m, and tail current, all optimized for the center frequency of 2.4 GHz.

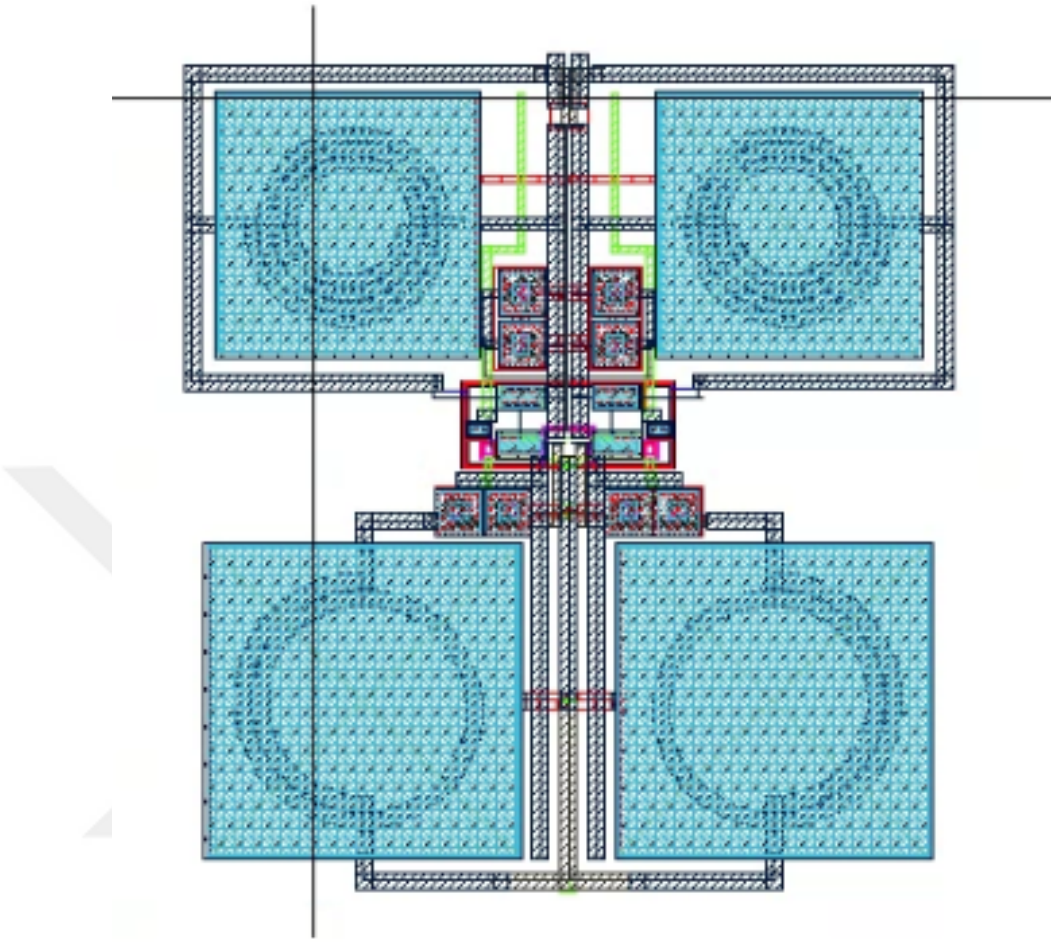


Figure 2.31. Layout view of the differential common source cascode LNA.

The layout of the proposed design is given in Figure 2.31. ESD protection is also placed in the gate inputs of the chip due to the high input impedance and low gate breakdown voltage.

For the post-layout simulation and measurements, a DC blocking capacitor, C_{DC} is placed at both the input to prevent upsetting the gate-to-source bias of M2-M3 input transistors and at the output [65]. Additionally, the parasitic inductor from the bond wire lengths and package pad capacitance are considered. The bond wire length, following standard technological design rules for the die and 48-pin QFN package, is approximately 2 mm, resulting in an inductance value of about 2 nH for L_{wire} [67].

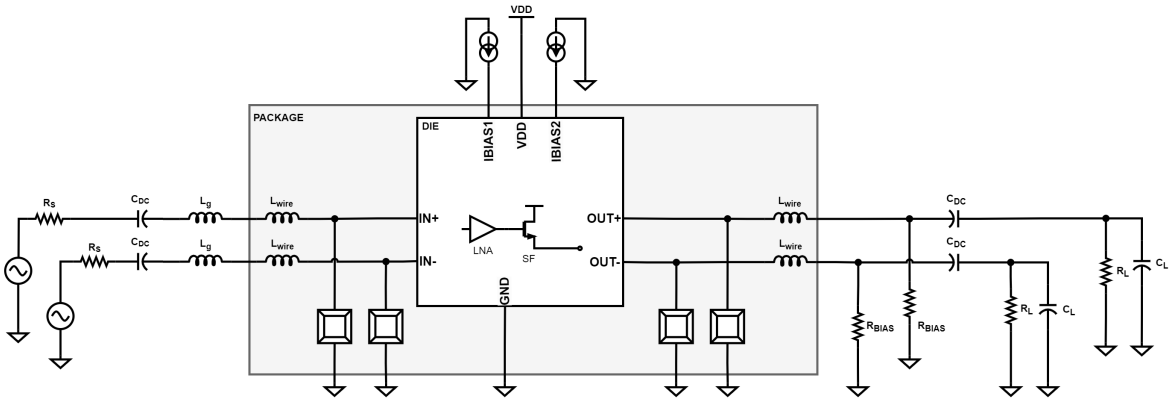


Figure 2.32. Testbench for AC analysis.

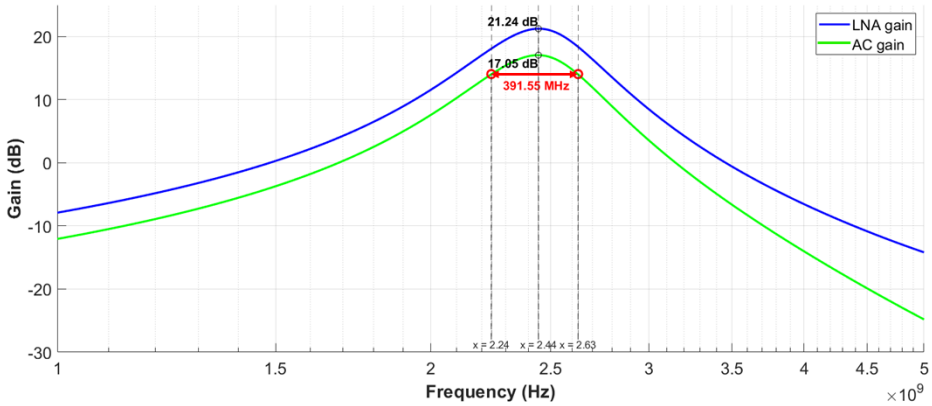


Figure 2.33. Post-layout AC simulation results.

The LNA is designed to drive the input capacitance of a subsequent VGA, but the output impedance and S-parameters cannot be simulated directly. To facilitate design simulation and measurements, a source follower buffer stage with a 50-ohm output impedance is designed at the LNA output [68]. R_{BIAS} resistor is used to bias this source follower stage. The testbench for the AC anaysis is given in Figure 2.32. The AC simulation results show that the voltage gain of the proposed common-source LNA with source degeneration is 17 dB at the center frequency. However, the 3 dB bandwidth of approximately 400 MHz does not meet the requirement for UWB signals, which need a bandwidth greater than 500 MHz. To achieve a wider bandwidth, a lower gain design will be necessary. This reduction in gain is acceptable because this block will be followed by a variable gain amplifier in the RF front-end. Due to time limitations, a new design could not be completed and the tests are performed with this fabricated

chip.

S parameter simulation results given in Figure 2.35 show that a nice s11 match is obtained over a wide band, with the center frequency being the desired frequency. The input and output reflection coefficients, s11 and s22 are less than -10 dB as aimed. The s21 gain is recorded as 9.44 dB for the post-layout simulations of the proposed LNA plus source follower architecture.

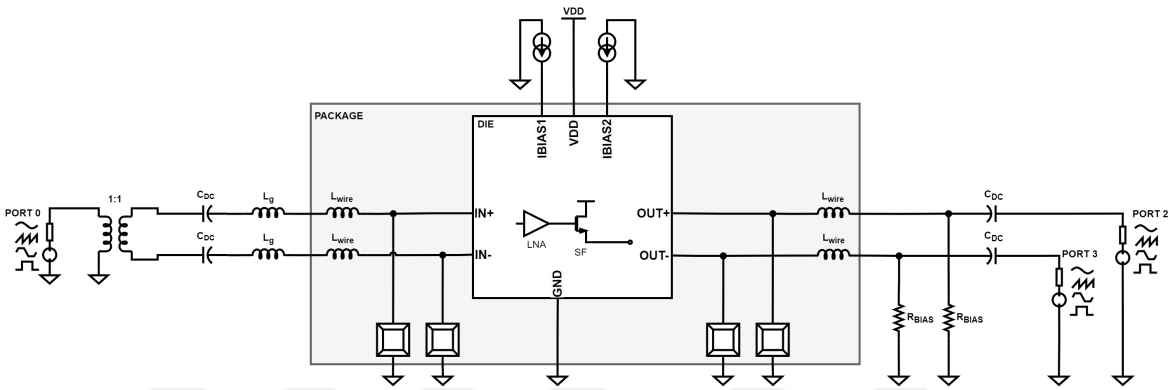


Figure 2.34. Testbench for s parameter analysis.

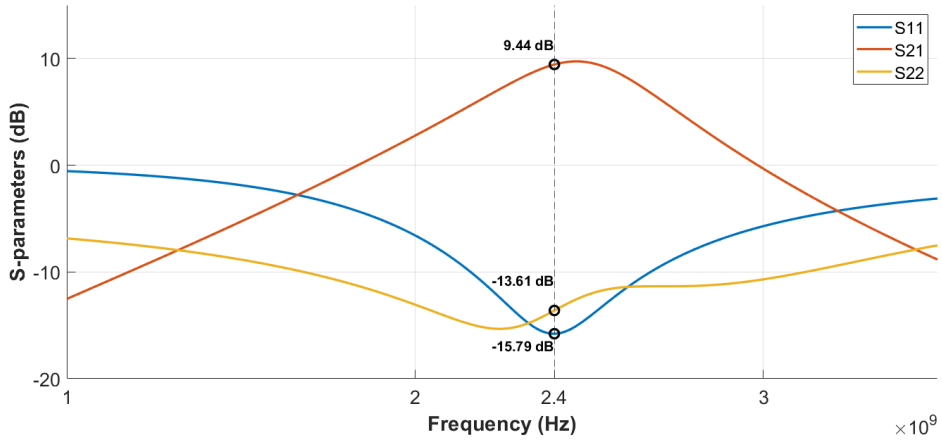


Figure 2.35. Post-layout simulation results for the s-parameters.

The noise figure is approximately 5 dB at 2.4 GHz and remains relatively stable over a wide bandwidth. It closely aligns with the graph of the calculated minimum NF value as shown in Figure 2.36.

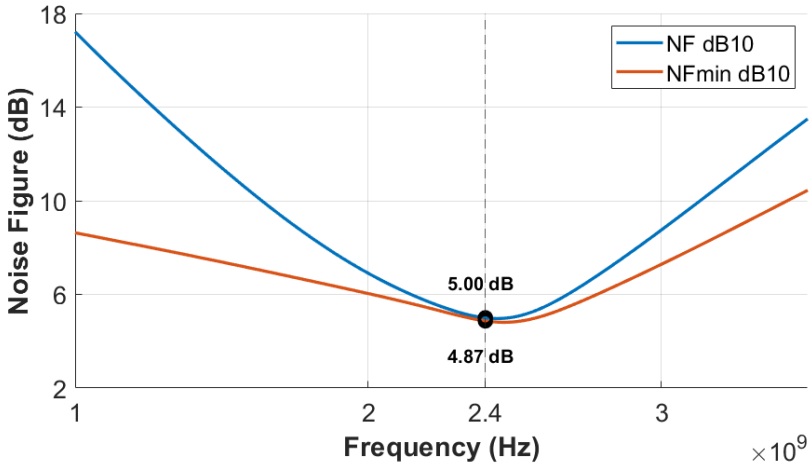


Figure 2.36. LNA noise figure for the post-layout design.

2.2.2. Variable Gain Amplifier

The LNA block is followed by a variable gain amplifer (VGA) in the receiver front-end. The schematic diagram of the implemented active loaded VGA configuration is shown in Figure 2.37.

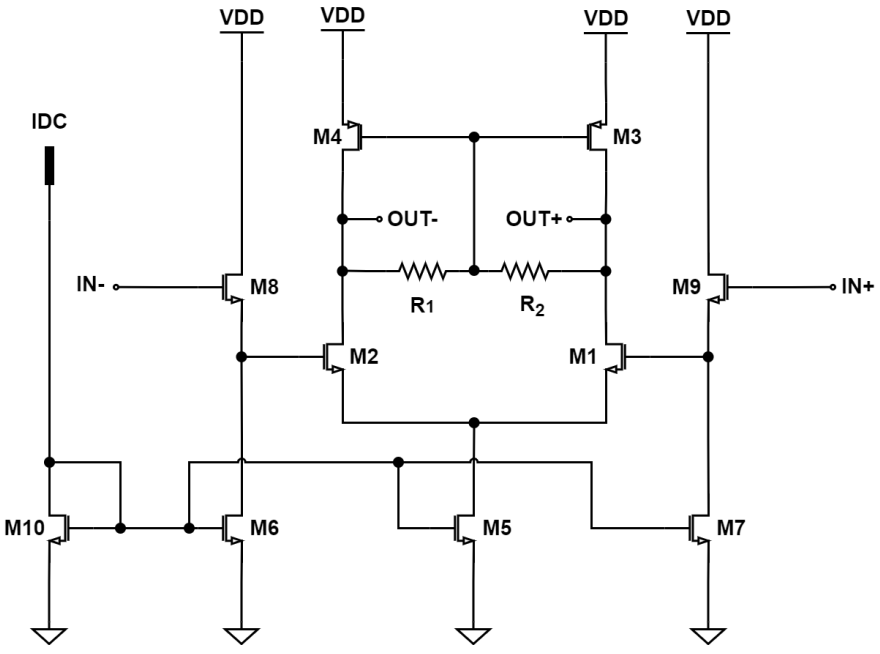


Figure 2.37. Active loaded VGA schematic.

Resistors R1 and R2 are placed at the output of the fully-differential active load amplifier to provide common-mode feedback to the active load and stabilize the out-

put common-mode voltage, while the source follower stages at the input reduce the common-mode voltage to allow sufficient margin for proper operation [69].

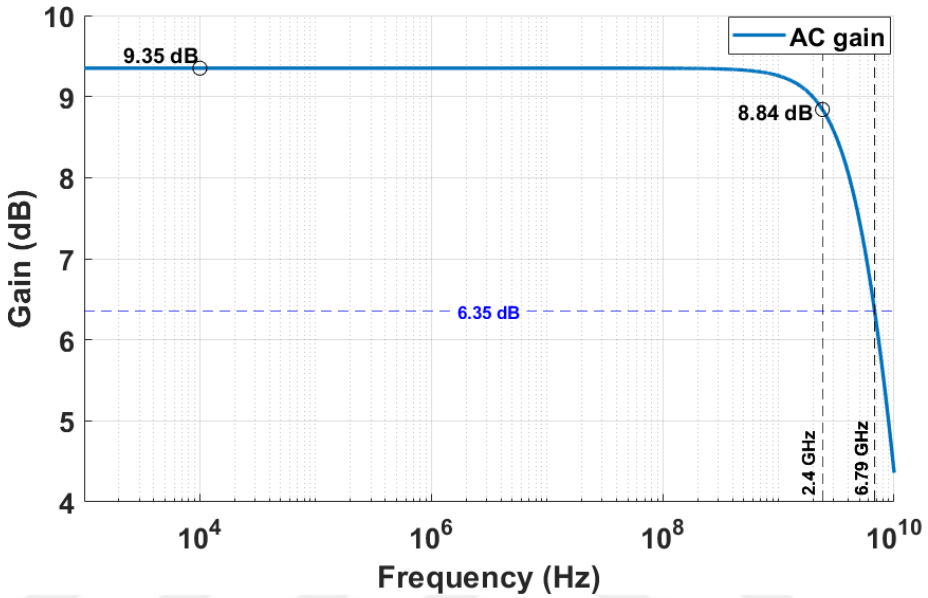


Figure 2.38. AC response of the design VGA stage.

The gain of 9.35 dB is observed with a 6.79 GHz bandwidth in the schematic simulation results depicted in Figure 2.38. At the frequency of interest, 2.4 GHz, the gain of the amplifier is 8.84 dB.

For a reconfigurable VGA design, various architectures have been implemented. As a first alternative, the feedback resistance is digitally controlled and changed as shown in Figure 2.39. To get rid of parasitic capacitances introduced by MOS switches, the bias current is varied as an alternative to this method as shown in Figure 2.40.

Additionally, cascaded VGA's are utilized with 2x1 multiplexer (MUX) to enable gain switching according to the design adjustments. While the methods employed in the architectures given in Figure 2.39 and 2.40 allow for continuous tuning, the number of stages determines the coarse tuning of the gain.

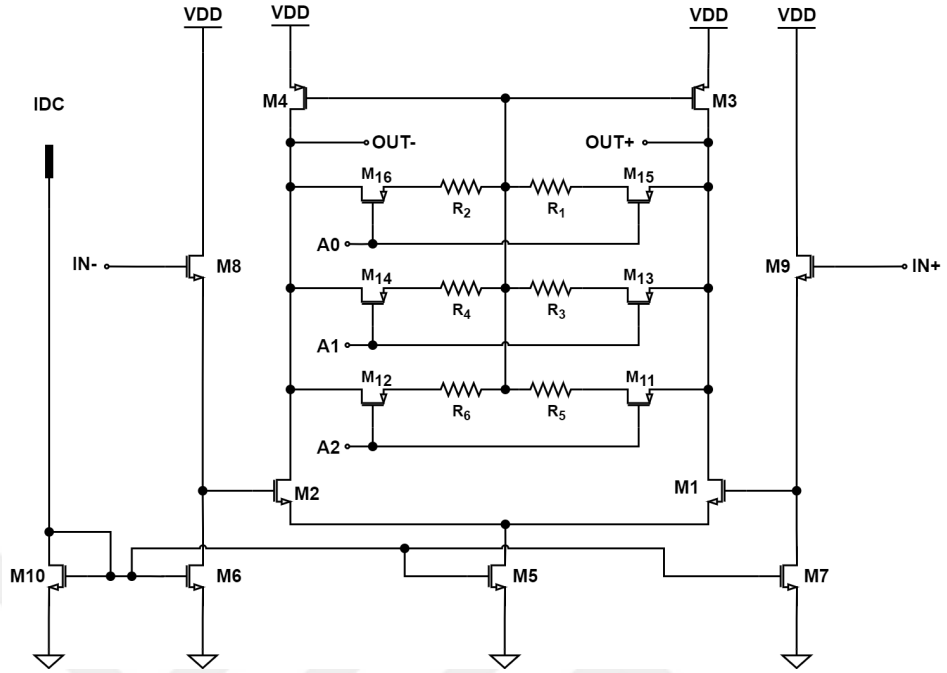


Figure 2.39. Reconfigurable VGA with varying feedback resistors.

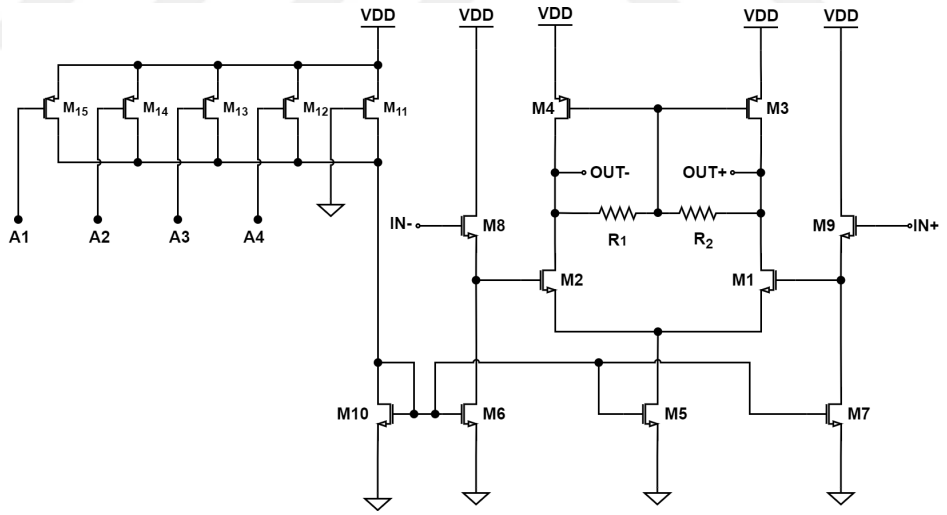


Figure 2.40. Reconfigurable VGA with varying bias current.

The total bandwidth of the N-stage cascaded VGA can be estimated using the following formula, as stated in [70]:

$$f_t = f_s\sqrt{2^{1/N} - 1} \tag{2.9}$$

where f_s represents the identical bandwidth of the single-stage amplifiers and f_t represents the total bandwidth of the cascaded chain VGA.

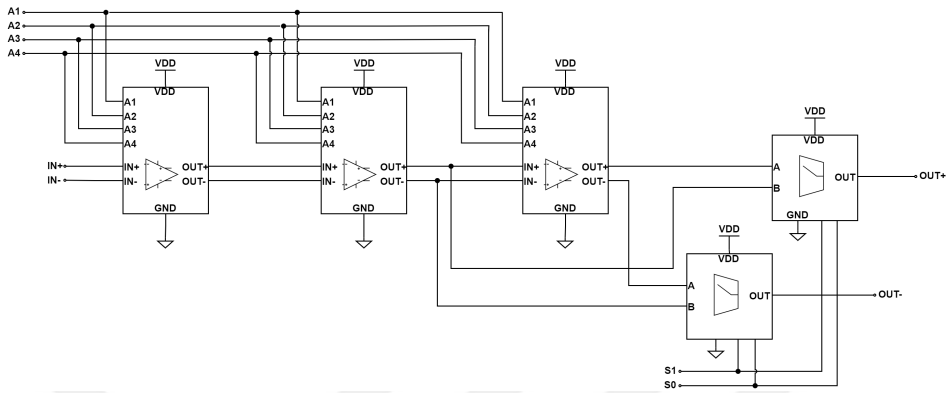


Figure 2.41. Cascaded VGAs with multiplexer architecture.

Different VGA designs have been implemented but further analysis should be done to decide on the optimal architecture. To maximize the receiver's performance, design trade-offs between bandwidth, linearity, and power consumption must be properly taken into account. [71].

2.2.3. Mixer

In the template based coherent receiver, a double-balanced Gilbert cell is used as the signal and template mixer. The differential signal outputs of the RF front-end are fed to gates of transistors M1 and M2 transistors which perform the voltage to current conversion in Gilbert cell as shown in Figure 2.42. The amplitude of the local oscillator (LO) signal in this topology must be sufficiently large to effectively switch the M3 and M6 transistors on and off. Transistors M3 to M6 multiply the RF signal currents from M1 and M2 with the differential LO currents applied by template pulse generator [72, 73]. The multiplication results are transferred to the two load resistors R_1 and R_2 to perform the current to voltage transformation providing the differential output IF signals [74].

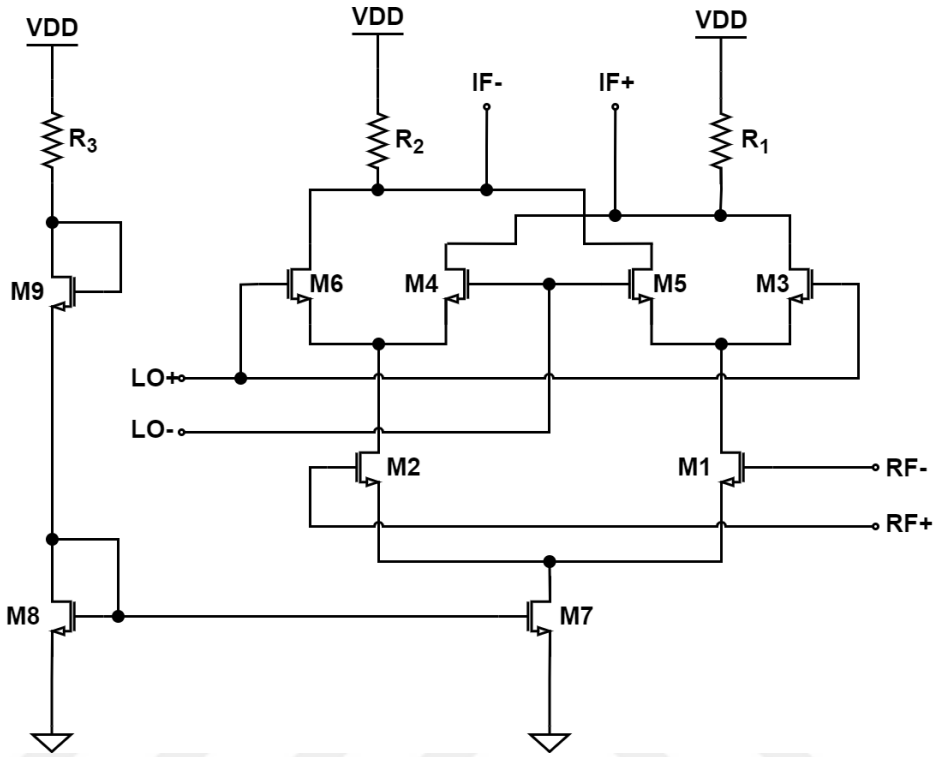


Figure 2.42. Proposed Gilbert Mixer architecture.

The voltage conversion gain, defined as the ratio of the desired IF output to the RF input, is given by the following equation, as stated in [72]:

$$G_v = g_m \frac{2}{\pi} R_L \cdot \tag{2.10}$$

A sinuosial input signal of 300 mV peak to peak amplitude is given to each RF input of the mixer at 2.4 GHz. The template signal is given as a bit smaller than these inputs but at the same frequency. The output waveforms OUT1 and OUT2 are shown in Figure 2.43 with given inputs.

Further analysis is needed to see the conversion gain, 1 dB compression and IIP3 results of the designed mixer.

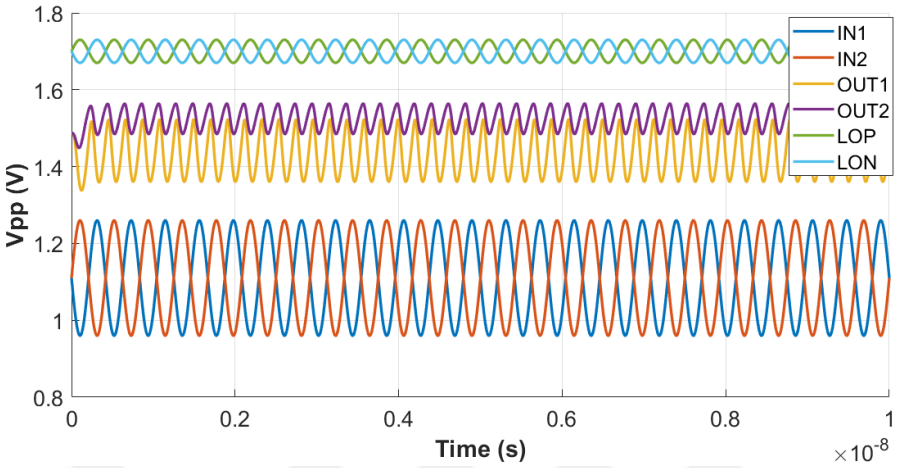


Figure 2.43. Proposed Gilbert Mixer input and output waveforms.

2.2.4. PCB Design

A separate PCB was designed for the LNA using the component library created during the TX PCB design process. The purpose of designing a separate PCB was to isolate the LNA from the TX section. The completed schematic capture can be seen in the Figure 2.44

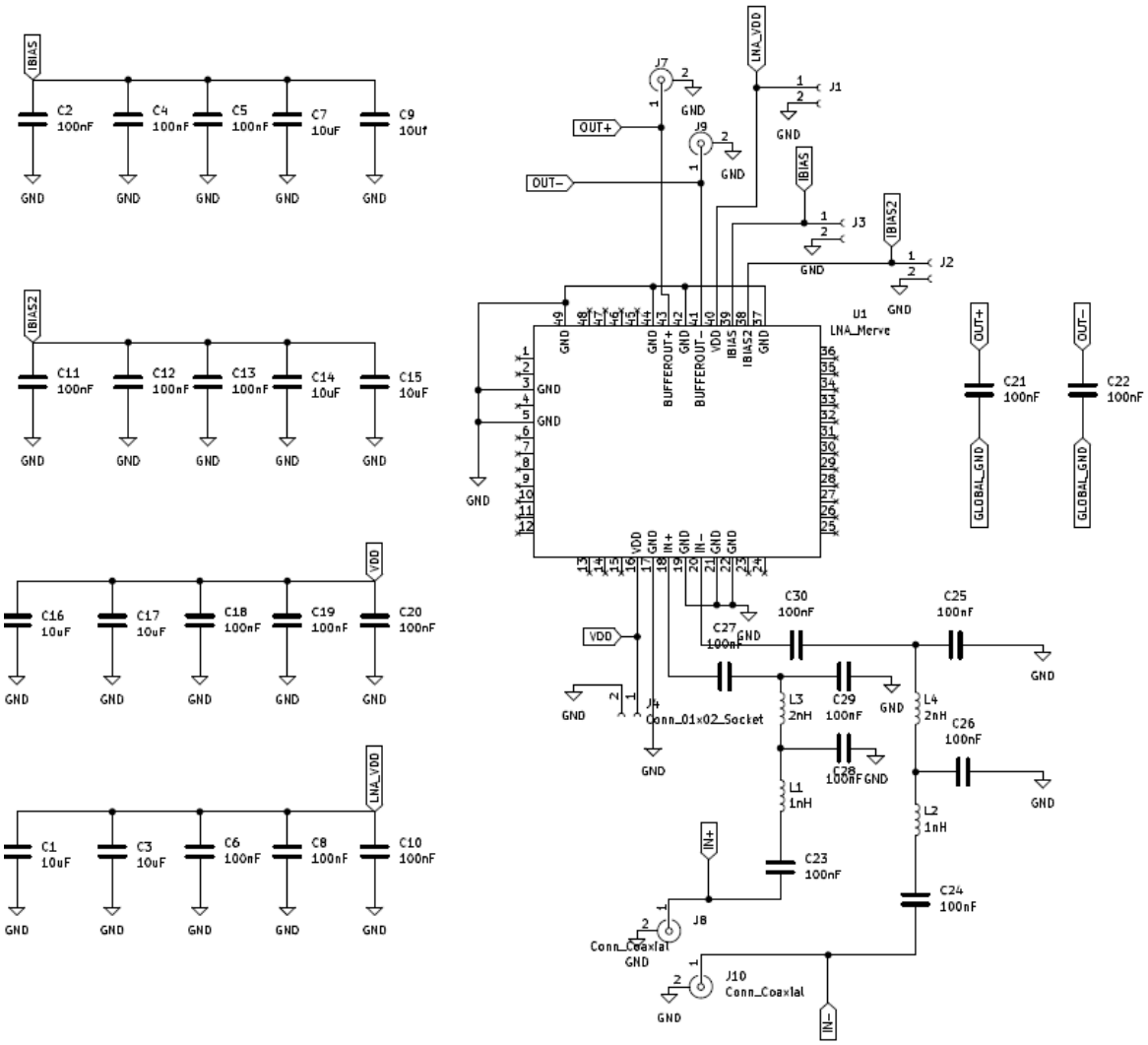
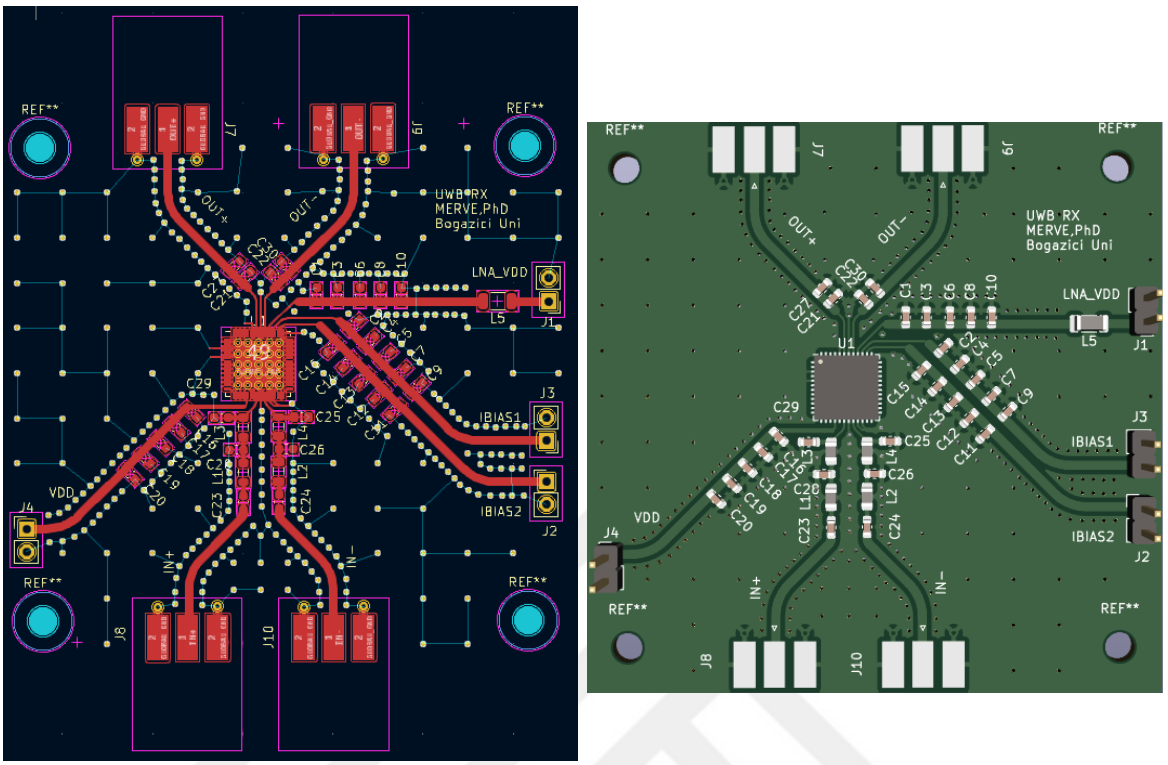


Figure 2.44. Top level schematic view of the LNA PCB.

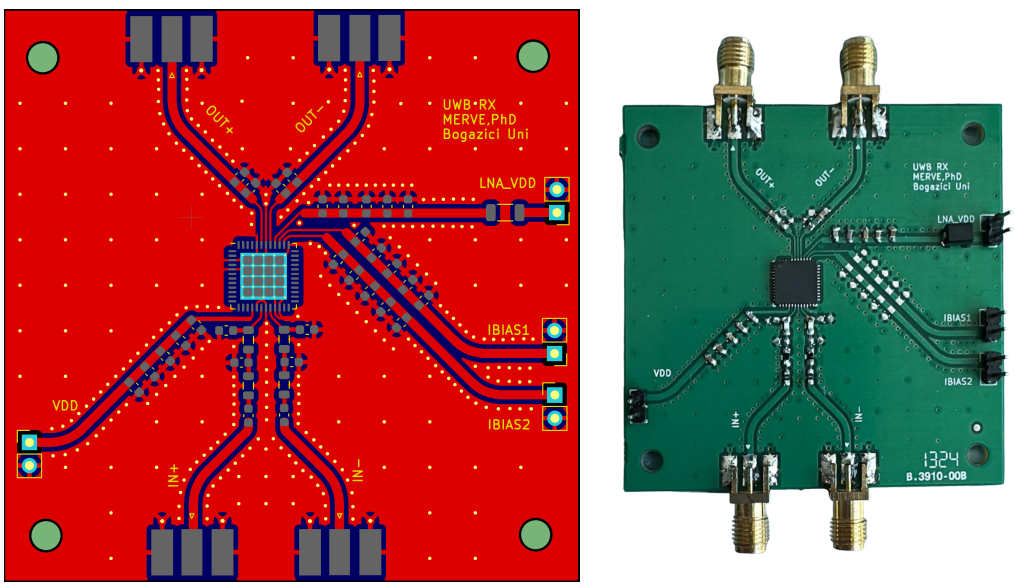
Using the same engineering practices followed in the TX PCB design section 2.1.4, the routed layout and 3D view given in Figure 2.45 were obtained.



(a) (b)

Figure 2.45. (a) Layout and (b) 3D views of the Receiver PCB.

The Gerber file outputs, along with the manufactured and assembled PCB, are shown in Figure 2.46 with the main design points summarized below.



(a) (b)

Figure 2.46. (a) RX Gerber files output and (b) Soldered PCB board with connectors.

High-frequency receiver outputs and sensitive RF inputs are routed using a grounded coplanar waveguide. To provide adequate grounding throughout the PCB, ground VIAs are placed along the PCB surface to connect the top and bottom layers. The unpopulated areas of the PCB are poured with ground copper to improve the PCB's noise susceptibility. Thermal reliefs are placed on the passive component's ground pins in order to reduce the heat exposure time and ease the rework.

2.3. Transceiver Post Layout Simulations

The TX output signal which has a 1.446 V peak to peak amplitude, is attenuated with a 50 ohm matching pi network to have an input signal of 10 mV at the LNA input as shown in Figure 2.47.

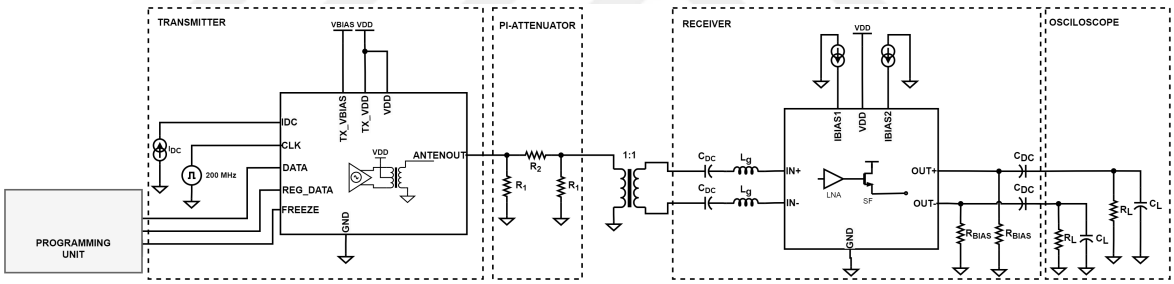


Figure 2.47. Transceiver simulation setup including the pi-network.

The time domain simulations are conducted for the post-layout transceiver architecture, in which the receiver consists of the proposed LNA and source follower implemented in the fabricated chip. The transmitter output, ANTENOUT and the LNA input, LNAIN waveforms are illustrated in Figure 2.48.

Due to the limited bandwidth of the LNA, the high-frequency components of the input pulse are attenuated, resulting in a decreased pulse width at the output. The sinusoidal envelope can be observed in the differential LNA output waveforms shown in Figure 2.49.

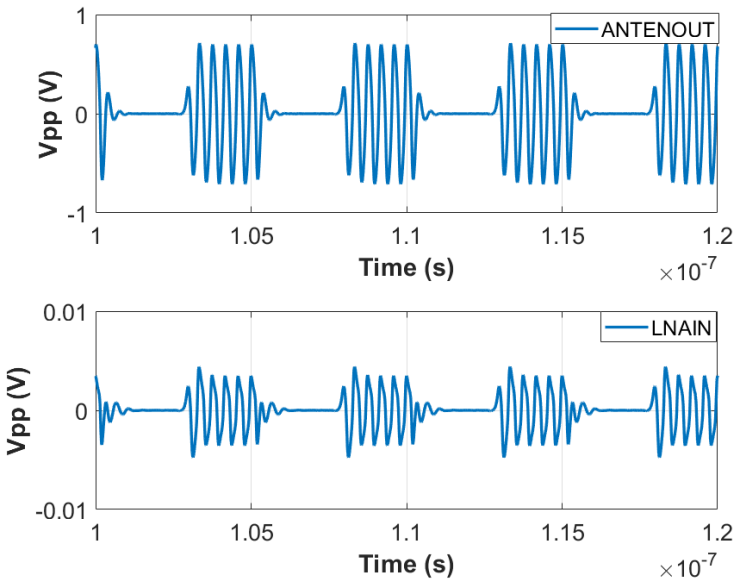


Figure 2.48. Time domain waveforms at the transmitter output and the LNA input respectively.

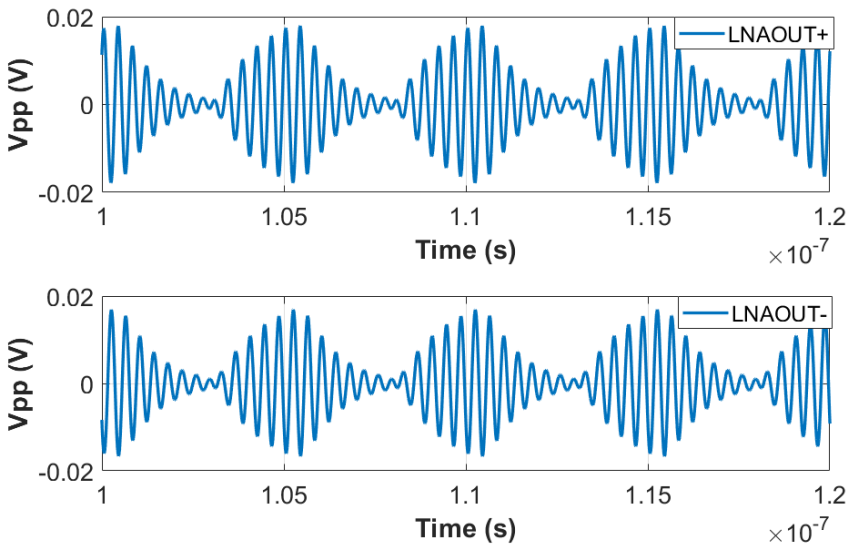


Figure 2.49. Time domain waveforms at the LNA differential outputs.

The differential output amplitude of the receiver, shown in Figure 2.50, has a peak-to-peak amplitude of 76 mV. The LNA gain on the receiver side is calculated to be approximately 17 dB, consistent with the LNA AC simulation results.

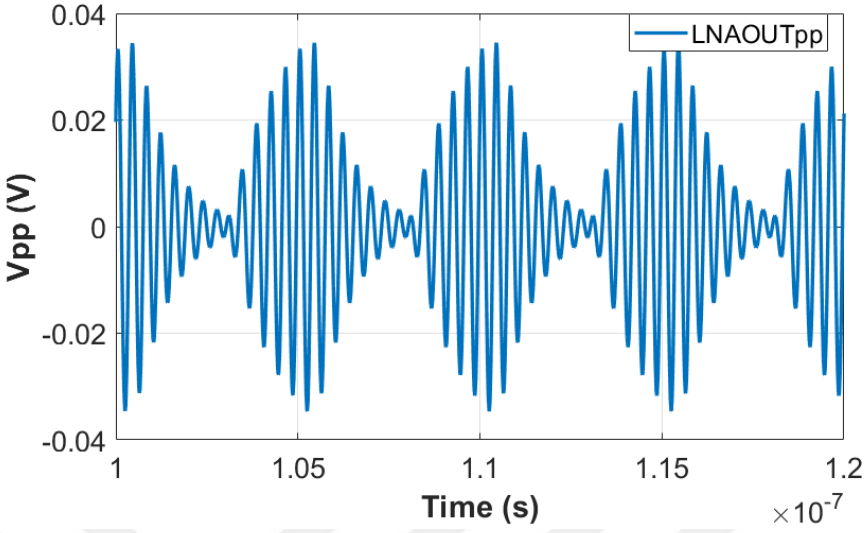


Figure 2.50. Differential waveform observed at the LNA output.

3. MEASUREMENT RESULTS

The microphotograph of the final silicon is shown in Figure 3.1, and the measurement results are discussed in the subsequent sections.

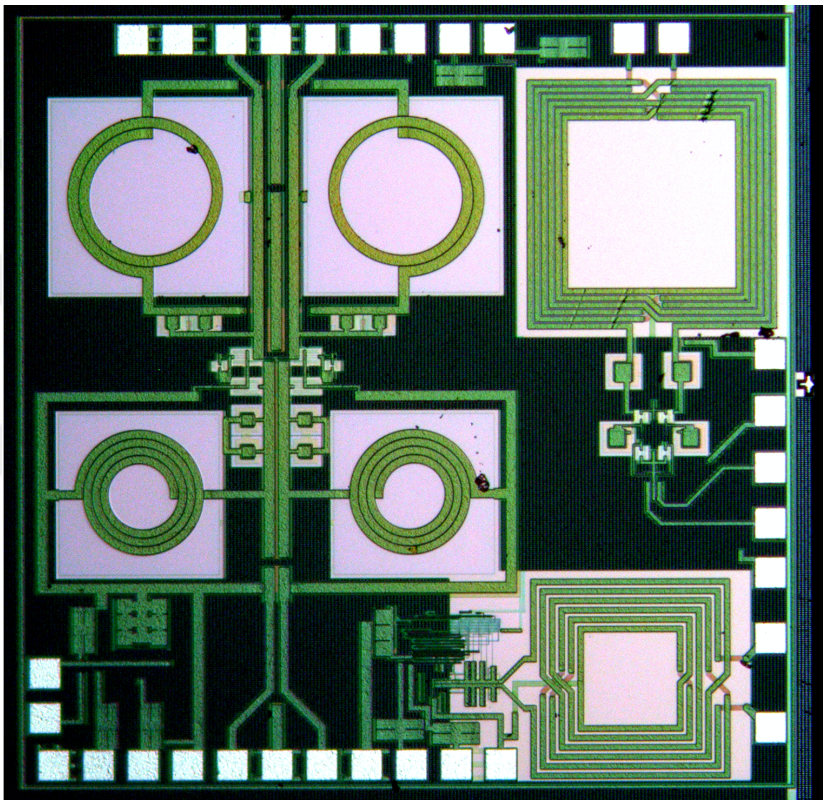


Figure 3.1. Microphotograph of the final silicon.

3.1. Transmitter Measurement Results

The presented IR-UWB transmitter is designed and simulated using Cadence Virtuoso tools with the PDK for the United Microelectronics Corporation (UMC) 180 nm CMOS technology, and fabricated in UMC 180-nm mixed-mode/radio-frequency (MM/RF) CMOS process. The fabricated TX covers a total area of 0.35 mm^2, while the transmitter section, excluding the balun, occupies only 0.017 mm^2. The layout and die photographs of the chip are shown in Figure 3.2 and Figure 3.3.

The measurement setup is given in Figure 3.4. The input CLK signal with a frequency of 200 MHz is provided by the RF signal generator, and DC power supplies are used for the DC biasing of the circuit, including the varactor elements. The configuration bits are sent to the chip via a microcontroller, and the output waveform is observed on a Keysight Infinium DSA80000B oscilloscope which has a 3 GHz bandwidth and sample rate of 40 GSa/s.

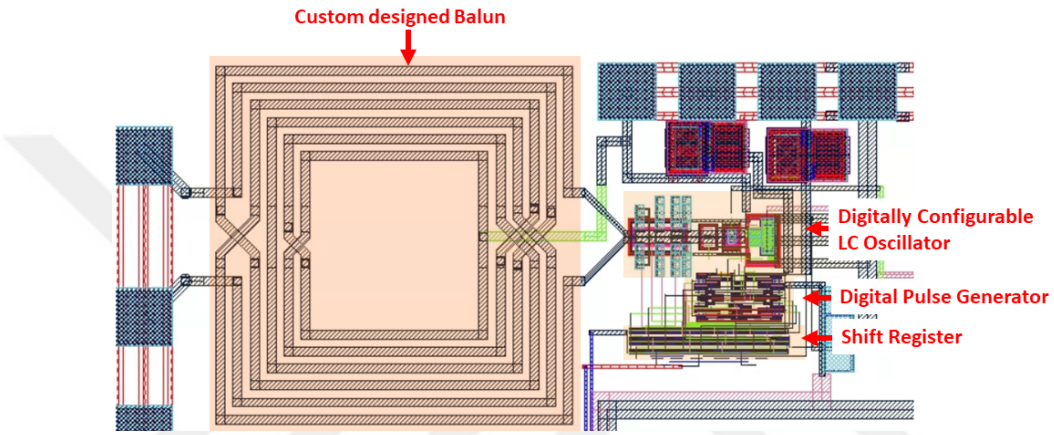


Figure 3.2. Layout of the proposed TX architecture.

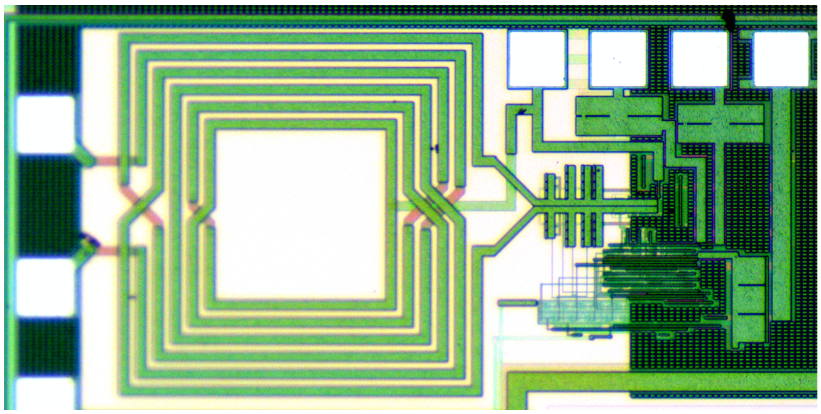


Figure 3.3. Microphotograph of the fabricated transmitter.

The implemented TX architecture is initially designed to work with the standard 50 Ω antenna, but it is also capable of supporting 75 Ω and 100 Ω load configurations. The output waveforms with a peak-to-peak voltage amplitude (V_{pp}) of 812 mV, 1,142 mV, and 1,132 mV are measured at 50 Ω, 75 Ω, and 100 Ω antenna loads, respectively, as shown in Figure 3.5. The pulse duration of one UWB pulse is measured as 2.5 ns for each pulse.

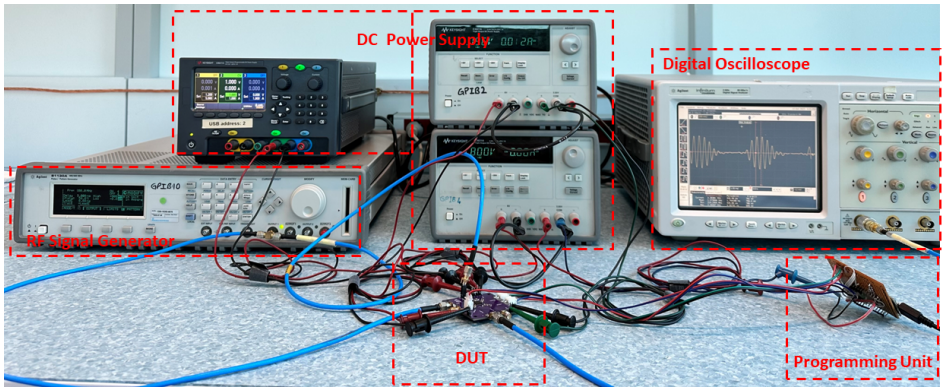


Figure 3.4. Measurement setup.

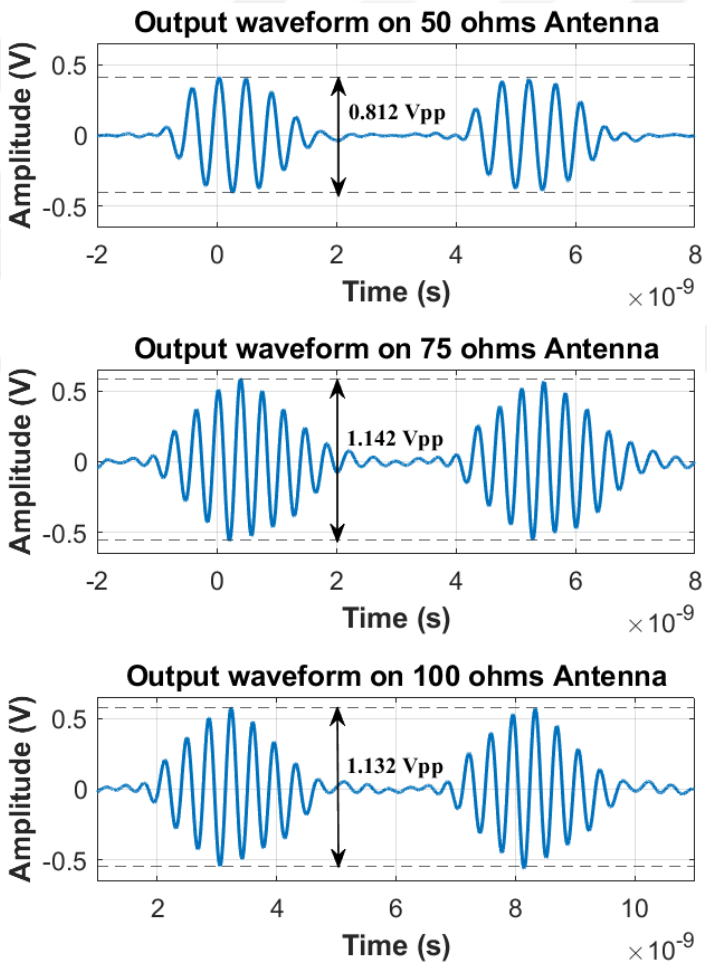


Figure 3.5. Measured output waveforms on 50, 75, and 100 Ω loads at 200 Mb/s.

The overall power consumption of the proposed design is measured as 19.8 mW on the 50 Ω load for 200 Mbps operation, while the static power consumption is recorded as 0.52 mW. The measured value includes all losses, counting the power consumed during the generation of digital control pulses.

Measured output waveforms with different configurations of OscPair_ON and OscPair_OFF signals are also recorded, as shown in Figure 3.6. The register map given in Table 2.5 is used to display the configuration details for each pulse.

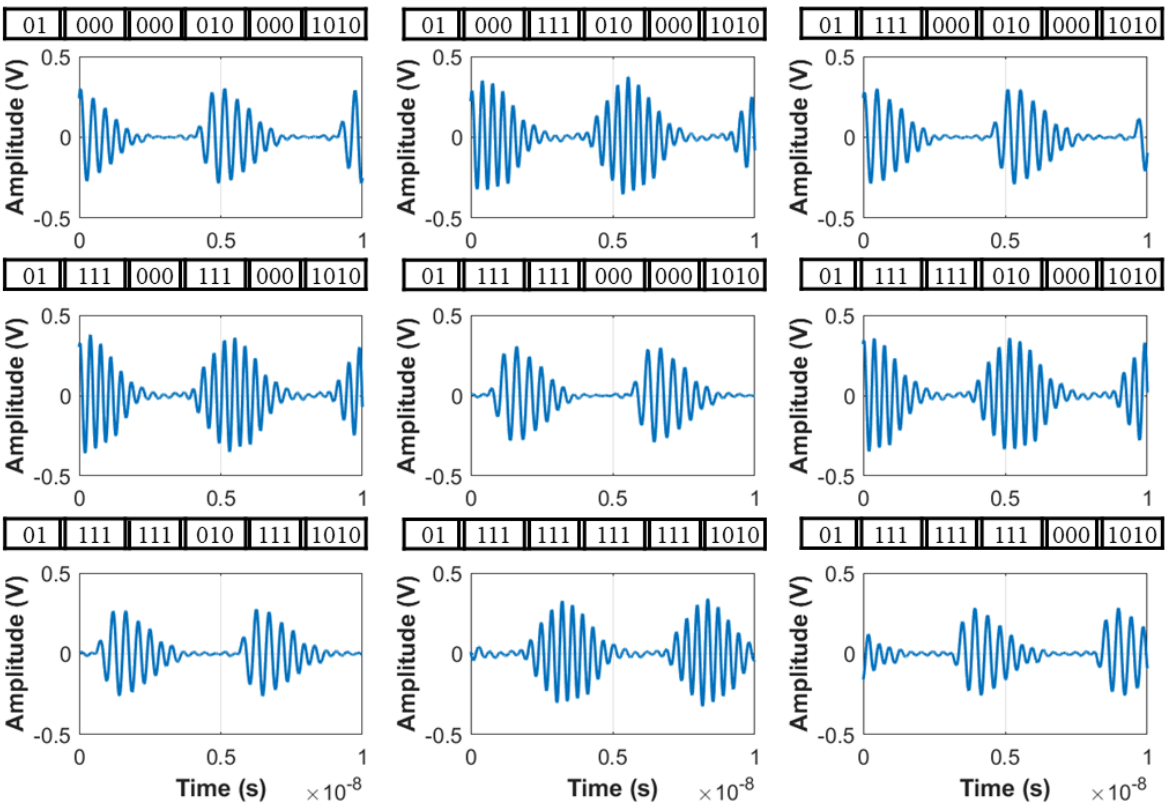


Figure 3.6. Measured output waveforms for different configuration of control bits.

The results of the frequency domain measurements taken using a spectrum analyzer are shown in Figure 3.7. 2.4 GHz center frequency can be observed from the measurement results. Because of the 200 MHz pulse repetition rate, the energy is concentrated at separate peaks. The measured transmission bandwidth is 902 MHz, confirming the UWB operation.

Time domain measurement results with different operating frequencies are also shown in Figure 3.8.

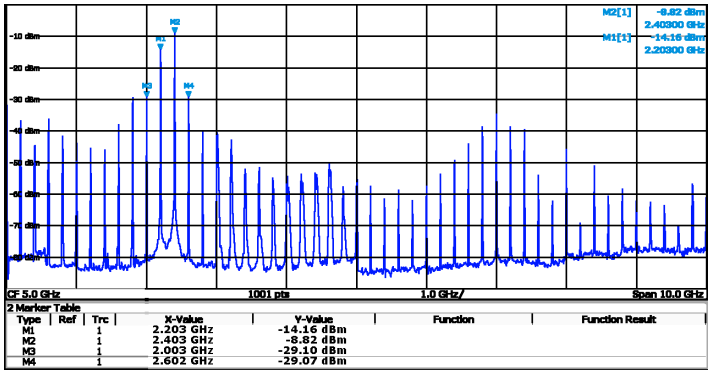
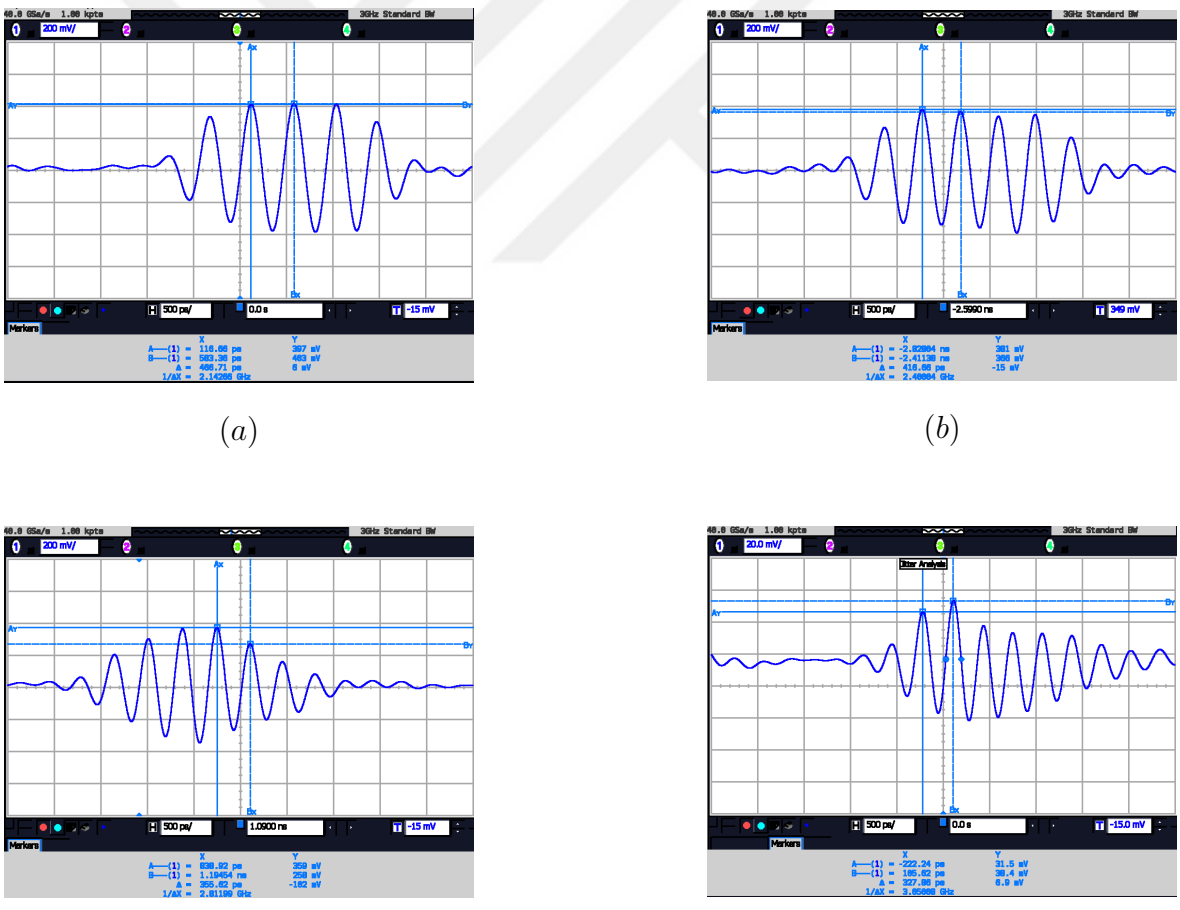


Figure 3.7. Output spectrum of the UWB pulse, center frequency 2.4GHz, 1 MHz PRF.



(a) (b)

(c) (d)

Figure 3.8. Measured frequency values for the specific configurations of <CTRL3, CTRL2, CTRL1, CTRL0> bit set and V_{bias} value (a) 2.14 GHz (b) 2.40 GHz (c) 2.81 GHz (d) 3.05 GHz.

The main design merits used to compare UWB transmitter designs with different data rates and output pulse energy values are the efficiency and energy per pulse (EPP) parameters given in [36] and [75]:

$$\eta = \frac{E_p}{EPP} \tag{3.1}$$

where E_p is the total pulse energy of the output signal and

$$EPP = \frac{P_{avg}}{PRF} \tag{3.2}$$

where P_{avg} represents the total average power consumed in the circuit and PRF is the pulse repetition frequency, set at 200 Mb/s in the proposed design.

There are two methods used to calculate the output pulse energy, E_p,

$$E_p = \frac{(\frac{V_{pp}}{2})^2 \times PW}{2 \times R_{Load}} \tag{3.3}$$

$$E_p = \int_{t_1}^{t_2} \frac{V_{out}^2}{R_{Load}}\, dt \tag{3.4}$$

where PW is the pulse width of the output waveform, which is recorded as 2.5 ns for each ANTENOUT pulse. While Equation 3.3, named as Method#1 is based on analytical calculations conducted with V_{pp} value, the Method#2 given in Equation 3.4 relies on the waveform data, which is processed with the integral operation. Although Method#2 is the more accurate way to calculate the total peak power of the output signal, Method#1 is the approximate one that is commonly used in the literature. Measurement data are processed with both methods. While the efficiency parameter η based on Method#1 is calculated as 4.16%, 5.76%, and 4.05% for 50 Ω, 75 Ω, and 100 Ω loads respectively, it is calculated as 2.31%, 3.26%, and 2.1% with Method#2.

Table 3.1. TX Performance Summary and Comparison.

	Tech (nm)	**Supply Voltage (V)**	**Data Rate (Mb/s)**	V_{pp} **(V)**	**Pulse Width (ns)**	E_p **(pJ)**	**EPP (pJ/pulse)**	**Efficiency** (η) **(%)**
This Work 50 Ω	180	1.8	200	0.812	2.5	4.12	99	4.16
This Work 75 Ω	180	1.8	200	1.142	2.5	5.44	94.4	5.76
This Work 100 Ω	180	1.8	200	1.132	2.5	4	99	4.05
[22]	180	1.5	100	0.16	3.5	0.224	16.8†	1.33
[24]	180	1.8	200	0.26	1	0.169	20	0.84
[55]	110	1.2	40	0.3	∼2	0.45	13.4	3.36!
[47]	180	3.3	20	2	5.2	52	671	7.75
[76]	180	1.8	250	0.26	1	0.169	20	0.84
[77]	180	1	0.00512	∼1	4	10	369.2	7.5*
[50]	130	1.35	5	∼2	2	13*	186*	7*
[9]	90	1	0.1	0.45-0.6	∼2	1-1.8	80	1.25-2.25
[78]	28	0.55	27.24	0.35	∼2	0.64*	14	2.6*
[79]	28	0.9	15.6	0.43	0-4	1.39	1300	0.11

†Excluding the output buffer power consumption * Not calculated, given in the related reference ! Simulated performance

The measurement results of the fabricated chip are compared with those of the existing state-of-the-art architectures in Table 3.1. V_{pp} represents the peak-to-peak voltage value measured on the output load, which is listed as having a 50 Ω value in the literature. The results for 75 Ω and 100 Ω load values are also given for our work. The output pulse energy E_p and efficiency η values are calculated using Method#1 utilizing the measurement data given for each work in the table except [77], [50], and [78]. The efficiency and other calculated values, as provided by the author in these papers, have been directly included in the table without using our calculations. For example, the TX efficiency is determined in a continuous-wave test-mode of the transmitter designed in [77].

E_p represents the transmitted pulse energy, serving as a crucial figure-of-merit for comparing designs in the literature. The proposed design achieves a higher V_{pp} value, leading to a better E_p result compared to the other leading-edge designs listed in the

table, except [47], [77], and [50]. Although these designs achieve larger pulse energy and efficiency values, the energy consumption required for pulse generation (EPP) in their implementation significantly exceeds that of the proposed design. Compared to the other work listed, the proposed design also has a higher EPP value, but it is important to note that examples in the literature, such as [22], have excluded the buffer stage in their power calculations. Additionally, the proposed transmitter is designed for a higher data rate compared to the other high-efficiency designs in the table, overcoming the challenge of achieving both high efficiency and high data rate simultaneously in the transmitter design.

When the pulse width and position reconfigurability are considered with the frequency tuning capabilities, our design is highly configurable compared to existing literature with the additional ability to withstand PVT variations. While some architectures in the literature also feature pulse width/amplitude configurability, [24], [55], [78], [79], the overall efficiency of these designs is lower, except for [77], which operates at a lower data rate of 5.12 kbps compared to our work.

Another significant contribution of this design to the existing literature is the implementation of an integrated balun without the need for an additional buffer stage. The transmitter in [55] also utilizes a transformer as an output stage but it is designed for a 40 Mbps data rate and only shows simulated performance results.

3.2. Receiver Measurement Results

The presented IR-UWB receiver is designed and simulated using Cadence Virtuoso tools with the PDK for the United Microelectronics Corporation (UMC) 180 nm CMOS technology, and fabricated in UMC 180-nm mixed-mode/radio-frequency (MM/RF) CMOS process. The fabricated RX including the low noise amplifer and the output buffers, covers a total area of 1.47 mm^2. The die photograph of the chip is shown in Figure 3.9.

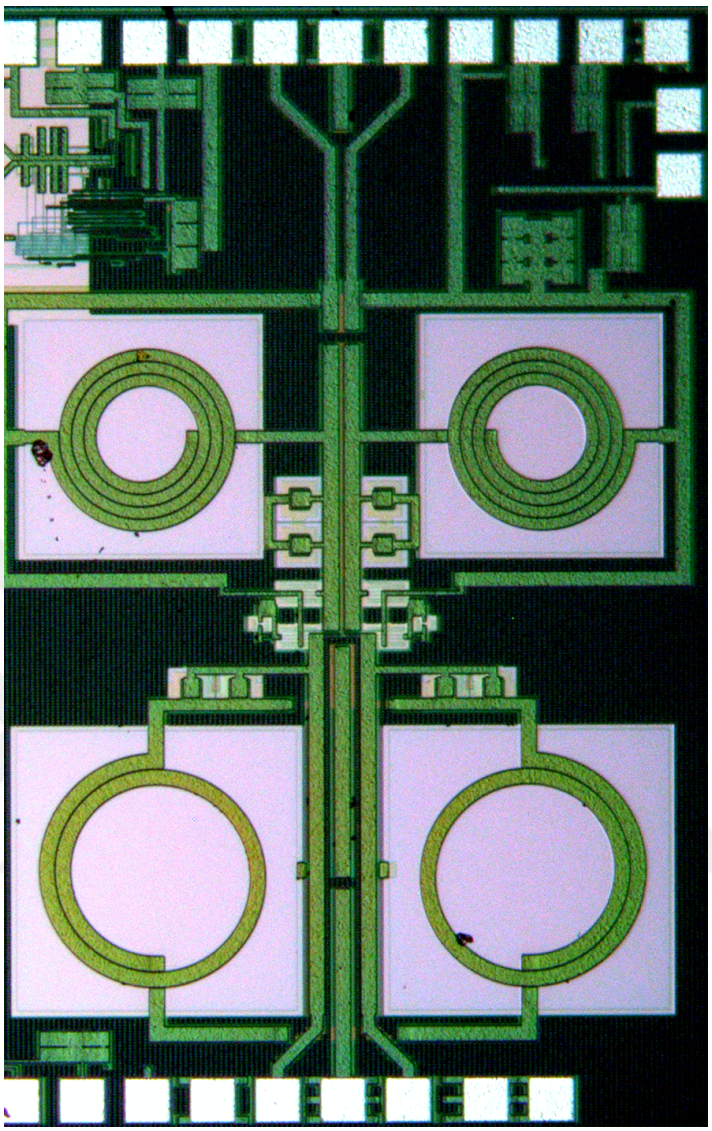


Figure 3.9. Microphotograph of the fabricated receiver.

The packaged chip is soldered to LNA PCB to create the measurement setup given in Figure 3.10. The off-chip gate inductor L_g is placed in series to the input of the receiver and R_{BIAS} resistor with 150 ohm value is connected to the output to bias the source follower stage for the successful operation. The input bias current nodes are connected to each other and supplied with a 1.4 mA current source for proper biasing.

The implemented RX architecture is designed to work with the standard 50 ohm antenna and the s-parameters measurements are conducted using Keysight N5242A PNA-X network analyzer with 50 ohm ports. The results are listed in Figure 3.11.

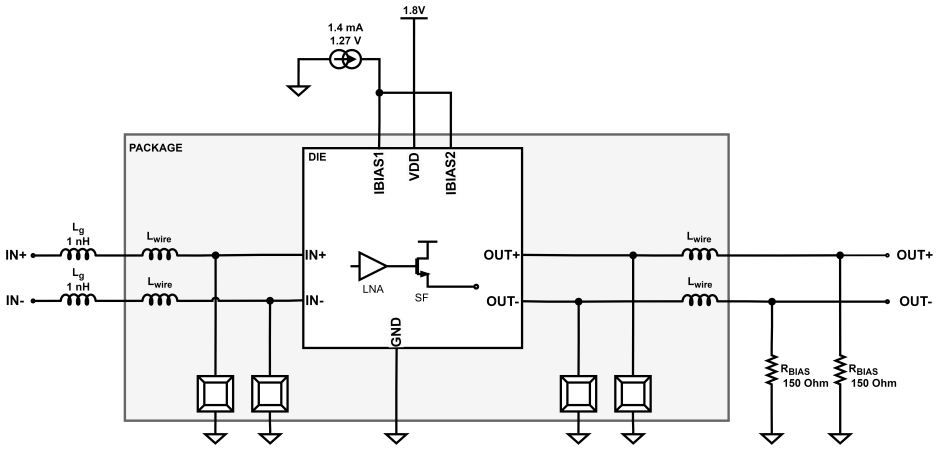


Figure 3.10. Measurement Setup.

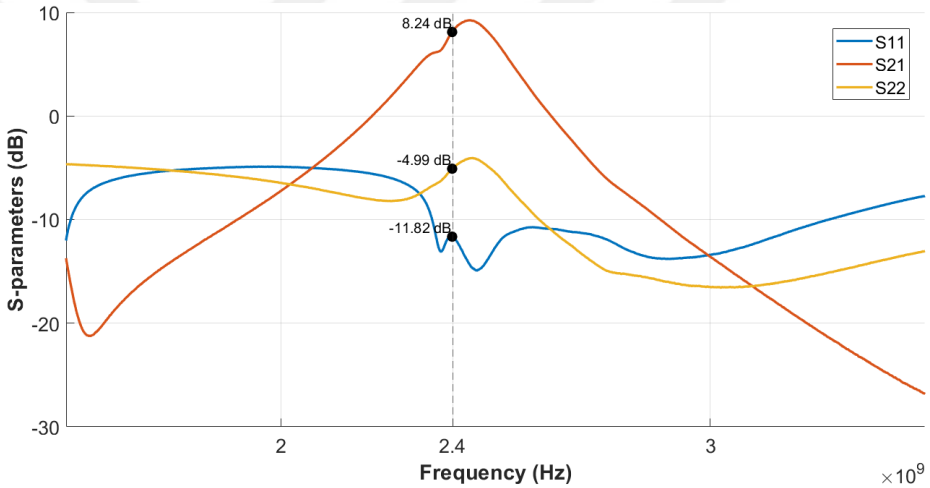


Figure 3.11. S parameters measurements.

S-parameters measurement results show that the input and output reflection coefficients, S11 and S22 are acceptable. S11 is less than -10 dB at the frequencies of interest, as desired. Output reflection, s22 is around -4.99 dB around the frequency of interest. It is indeed higher than the desired range however this value is not a concern because LNA will be followed by a VGA stage and matching can be realized at that configuration. The s21 parameter which is the power gain of the LNA is recorded as 8.24dB at 2.4 GHz frequency offset.

The results of the frequency domain measurements taken using Rohde & Schwarz FSWP 26 GHz Spectrum Analyzer are shown in Figure 3.12. A 2.4 GHz single-tone signal is generated by the Rohde & Schwarz SMA100B signal generator and applied to

the input of the LNA. The applied signal level is -25 dBm. The signal power at the positive output of the LNA is measured as -17dBm on the spectrum analyzer. The 8 dB gain between the output and input of the LNA verifies the s-parameter measurements.

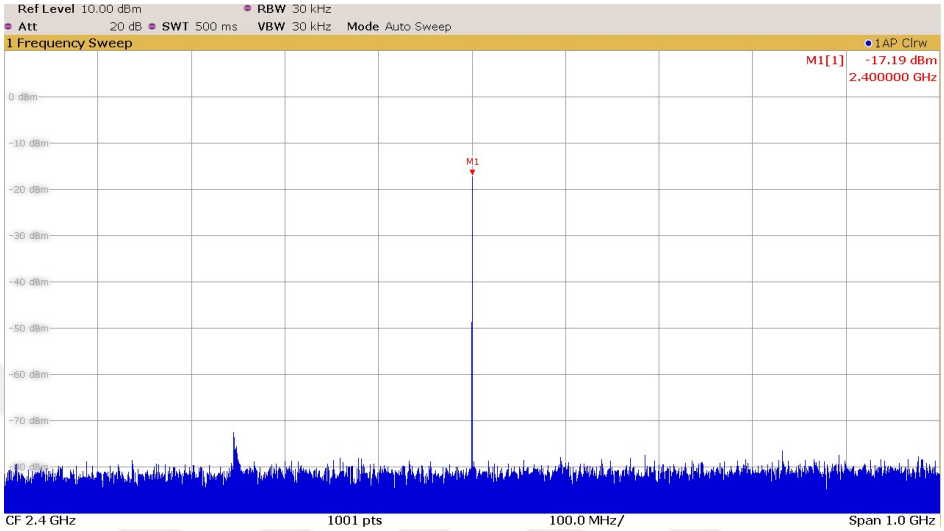
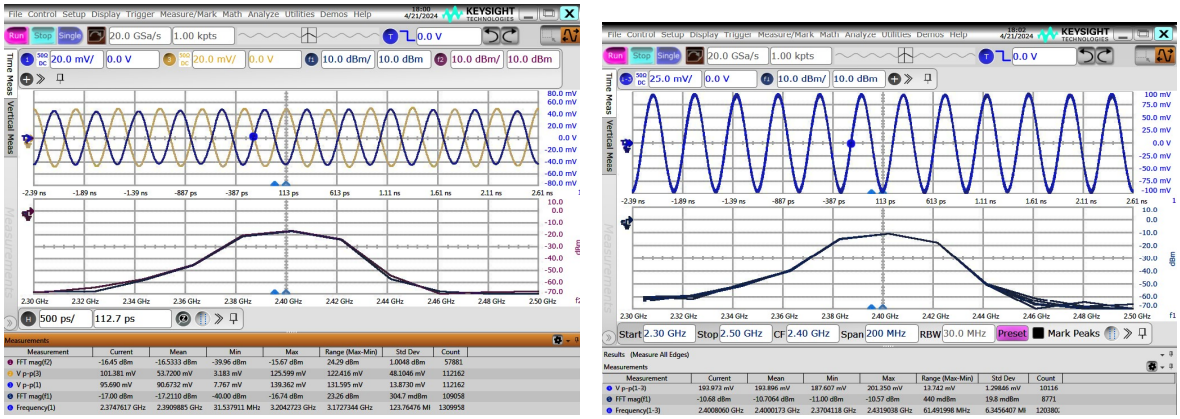


Figure 3.12. Frequency domain single tone measurement of the LNA output.

Additionally, a time domain measurement is performed on the LNA to analyze the differential output performance. Time domain measurements visualize the output waveform behavior and phase balance between the the differential outputs. A single-tone sinusoidal signal at a 2.4 GHz frequency is applied to the input of the LNA by using the R&S SMA100B signal generator. The output of the LNA is recorded with a Keysight DSA91204A 12 GHz 40 GSa/s Digital Signal Analyzer. Time domain measurements are shown in Figure 3.13. The blue line in Figure 3.13 (a) is the positive and the yellow line is the negative output of the differential LNA. It can be seen that the phase difference between differential pairs is 180 degrees. Figure 3.13 (b) shows the differential output. The 3 dB increase in the magnitude of the combined output shows that the differential pair of the LNA output is well balanced.



(a) (b)

Figure 3.13. Measured time domain response of the receiver front-end (a) output pair (b) differential output.

3.3. Transceiver Measurement Results

The output waveform from the fabricated transmitter is sent to the input of the fabricated receiver in the measurement environment for the UWB signal transmission test. An attenuator block is also used in the LNA input port to lower the amplitude of the incoming signal. The single-ended measurement has been performed due to the unavailability of a 1:1 balun, with one input is terminated to ground for this reason. The measurement setup is given in Figure 3.14.

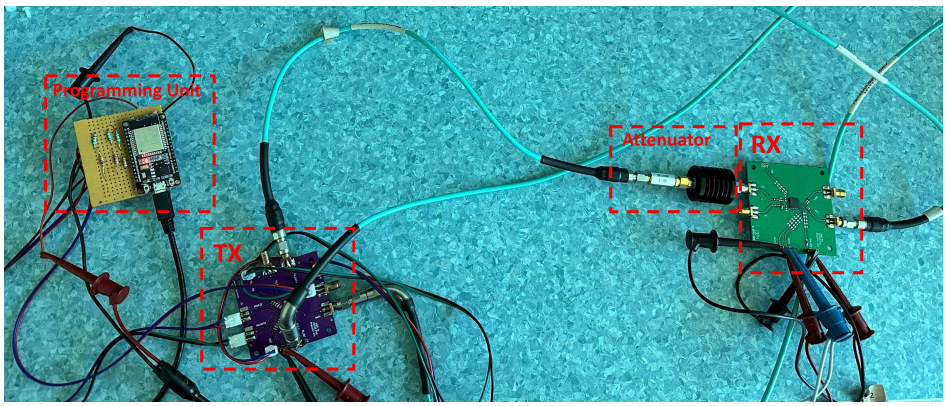


Figure 3.14. Measurement Setup.

The TX output signal with a power of -15 dBm was attenuated using a 16 dB attenuator. The signal measured at the input of the LNA had a power of -31 dBm, and the measured output power of the LNA was -25 dBm. Consequently, the recorded

power gain for the proposed architecture was measured as 6 dB. The results are listed in Figure 3.15.

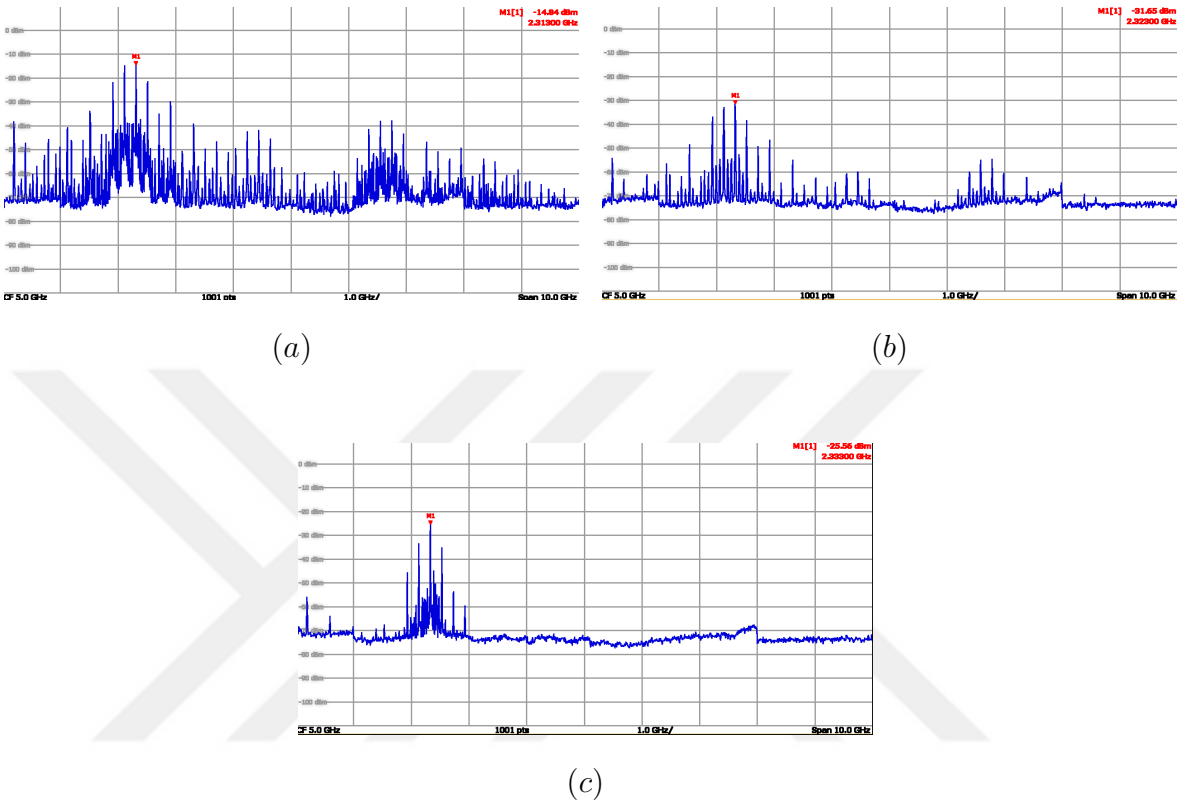


Figure 3.15. Spectrum waveform in (a) transmitter output, (b) LNA input, and (c) LNA output respectively.

Time domain measurement is also performed for the transceiver architecture to analyze the output performance. The UWB signal coming from TX output is attenuated and applied to the input of the receiver. The output signal in single-ended configuration is recorded with a Keysight DSA91204A 12 GHz 40 GSa/s Digital Signal Analyzer and shown in Figure 3.16. A sinusoidal shape output waveform with reduced pulse width is observed due to the limited bandwidth of the LNA as expected.

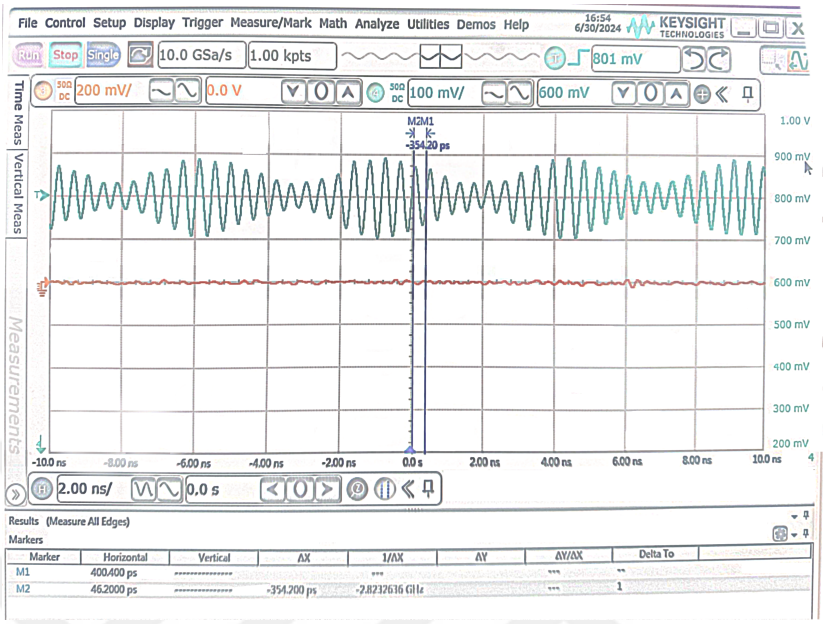


Figure 3.16. Output waveform measured at the LNA output

4. CONCLUSION AND FUTURE WORK

In this thesis, the fabricated IR-UWB transmitter and receiver designs have been presented in UMC 180 nm CMOS technology. The IR-UWB TX is based on a switchable and configurable LC oscillator. A custom-designed balun is used instead of an inductor in the LC tank and employed as a buffer stage at the same time. The reconfigurable pulse generation and on/off switching schemes are utilized to obtain high efficiency at the 200 Mbps data rate. The transmitter's configurability extends to key parameters such as pulse width, pulse position, and center frequency tuning. Using digital configuration bits, the digitally configurable pulse generator produces OscPair_ON and OscPair_OFF signals with adjustable widths and starting points. This precise control over pulse characteristics helps to determine how much charge injection and removal are introduced to the proposed transmitter and to selectively turn on and off the circuit. By adjusting the pulse width and position, we can tailor it to accommodate different bandwidths or output pulse energy values. Furthermore, the configurable delay unit suppresses the PVT variations with a suitable configuration of selection bits, thus optimizing system performance. Additionally, center frequency tuning, facilitated by configuration bits, enhances the transmitter's versatility for applications requiring different center frequencies. Collectively, these features provide the flexibility necessary for the transmitter to adapt to diverse applications while delivering consistent high performance. The overall transmitter has an output swing of 0.812, 1.142, and 1.132 Volts between the differential antenna ends, with an efficiency of 4.16%, 5.76%, and 4.05% measured on 50, 75, and 100 Ω antenna loads, respectively. The proposed transmitter is a good candidate for long-range applications with the combination of the high data rate and large output swing features and can be used with non-coherent receivers in low-cost and low-complexity architectures.

A differential common-source (CS) cascode LNA with inductive source degeneration is implemented in the RF front-end of the IR-UWB receiver side. The variable gain amplifier (VGA) and Gilbert mixer blocks are also designed to support potential future applications in both coherent and non-coherent receiver architectures. The

fabricated components include the IR-UWB receiver front-end, featuring the cascode CS LNA and a source follower buffer stage at its output, which was specifically used to facilitate LNA measurements. The fabricated RX, consisting of the low-noise amplifier and output buffers, occupies a total area of 1.47 mm^2, with the measured S21 gain of the amplifier recorded at 8.24 dB. The transmitted UWB signal from the proposed transmitter was successfully captured on the receiver side during transceiver chip testing.

Future work will involve designing the remaining receiver blocks and testing both coherent and non-coherent receiver designs using the existing fabricated transmitter.

5. PUBLICATIONS

Related scientific publications are listed below. Figures produced in these publications, for which the copyright was transferred to the respective publisher, have been reused in this thesis in accordance with the publisher's editorial policy on the reuse of author-produced text and graphics.

- M. Albayrak, G. Dundar, O.Z. Batur, "High Data Rate and Energy Efficient Configurable IR-UWB Transmitter with an Integrated Balun", Preprint submitted to AEU-International Journal of Electronics and Communications.

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