A LOW-NOISE LOW-POWER CMOS INTERFACE FOR A GMR BIOSENSOR APPLICATION

by

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ABSTRACT

A LOW-NOISE LOW-POWER CMOS INTERFACE FOR A GMR BIOSENSOR APPLICATION

The thriving demand in the need of early disease detection of modern medicine dictates an effective and cheap bio-detection system for organic samples. The enzymatic, nuclear or fluorescent labeling approaches have proven inefficient and expensive to realize. Recent developments in magnetic nanotechnologies have shown serious potential for biomolecular detection by labeling the organic molecules with appropriate magnetic nanotags. For sensing those nanotags, giant magnetoresistive spin-valve (GMR SV) sensors possess great promise for sensitive biosensing applications. This project proposes an CMOS (UMC 0.18 um technology) interface for a specific ultra sensitive (<100nT) GMR SV sensing element, which consumes low power and amplifies the low level noisy sensor signal without adding additional noise, then converts the signal to digital data. Each design step has been described with necessary trade-offs and the selections. The theory behid the GMR SV sensor and magnetic nanobeads, the selection and the modeling of the sensing element are also covered. The performance evaluation of each block-sub-block and main block is given with simulation results.

ÖZET

DÜŞÜK GÜRÜLTÜLÜ VE DÜŞÜK GÜÇ HARCAMALI GMR BİYOSENSÖR ARAYÜZÜ TASARIMI

Modern tıbbın gelişimi ve tedavi yöntemlerinin artması ile hastalıkların erken teşhisinin önemi de büyük bir artış göstermektedir, bu artış organik örnekler için ucuz ve kolay uygulanabilir teşhis ve tanı koyma methodlarına arzı da yanında getirmektedir. Mevcut uygulanan yöntemler (enzimatik, nükleer yada florosan etiketleme) hem pahalı ve temini zor, hem de uygulaması gerek hasta, gerek kurumlar ve uzmanlar için meşakatlidir. Son yıllarda ayrıca gelişim gösteren bir bilim dalı bu konudaki açığı kapatmak için ciddi bir potansiyel vaat etmektedir, manyetik nanoteknoloji. Teşhis edilecek organik partiküllere uygun olarak seçilen manyetik nano etiketler sayesinde biyolojik yapı taşları işaretlenerek herhangi bir manyetik sensör sayesinde elektriksel sinyale dönüşümü mümkün olmaktadır. Bu nano etiketlerin okunması sürecinde dev magnetorezistans dönen valf sensörleri (GMR SV) hassas ölçümler için ciddi bir potansiyel ortaya koymaktadır. Bu proje spesifik bir ultra hassas (<100nT) GMR SV sensör için tasarlanmış bir CMOS (UMC 0.18 um teknolojisi) arayüz ortaya koymaktadır. Bu arayüz gürültülü ve düşük gerilimli sensör sinyalini alıp üzerine mümkün olduğunca gürültü eklemeden yükselterek en sonunda da sayısal koda dönüştürme sürecini kapsamaktadır. Tasarım aşamalarının her biri ve bu aşamalarda verilen kararlar, gerekli ödünleşim ilişkileri ile beraber detaylıca incelenmiştir. GMR SV sensörlerin ve sinyal oluşumunda kullanılan manyetik nano-partiküllerin altında yatan teori ve bunların modellenme süreci de ayrıca incelenmiştir. Her bloğun, alt blokların ve üst blokların performans değerlendirmesi de simülasyon sonuçları ile belirtilmiş ve irdelenmiştir.

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LIST OF SYMBOLS

3D	Three Dimentional
A	Ampere
B	Magnetic Field Density
C	Capacitance
Co	Cobalt
Cu	Copper
dB	Decibel
f	Frequency
Fe	Iron
gm	Transconductance
GND	Ground
H	Magnetif Field
Hz	Heartz
I	Current
J	Joule
k_B	Boltzmann Constant
μ	Micro
m	Mili
Meg	Mega
n	Nano
Ni	Nickel
Oe	Oersted
pH	Measure of Acidicy
R	Resistance
T	Tesla
Ta	Tantalum
USD	US Dollars
V	Volts
V_{DD}	Positive supply voltage

V_t	Threshold voltage
Vref	Reference Voltage
V_{SS}	Negative Supply Voltage
W	Watt
wt%	Percentage by weight

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
AFE	Analog Front-End
AMR	Anisotropic Magnetoresistance
CCIA	Capacitevely Coupled Chopper Amplifier
CLK	Clock
CM	Common Mode
CMFB	Common Mode Feedback
CMOS	Complementary MOS
CMR	Common Mode Rejection
CMRR	Common Mode Rejection Ratio
DC	Direct Current
DNA	Deoxyribo Nucleic Acid
ENOB	Effective Number of Bits
GBW	Gain Bandwith Product
GMR	Giant Magneto Resistance
GMR SV	Giant Magneto Resistance Spin Valve
IOS	Input Offset Storage
LSB	Least Significant Bit
MOS	Metal-Oxide-Semiconductor
MR	Magnetoresistance
MSB	Most Significant Bit
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
PM	Phase Margin
RNA	Ribonucleic Acid
SAR	Successive ApproximationRegister
SNR	Signal-to-Noise Ratio
TMR	Tunneling Magneto Resistance

1. INTRODUCTION

As the scientific knowledge of biochemistry and electronics has improved in the last century, a cross section between those areas emerged, which is the biosensor technology. The term biosensor was first used by Cammann [2], and refers to the device that senses the effects or presence of the biological or chemical reactions or substances and reacts to them proportionally in an output form of its own. The area of biosensors covers many applications such as detection of pH, temperature, magnetic field, organic particles in bio-fluids, drug discovery, DNA, food quality and naturality, metabolic rate and bio-electrical signals. The large area of usage and the technological advances in their production made the sensors more and more appealing over the years. Their role in modern medicine is especially crucial as seen with the requirement of the new generation MRI, ECG, tomography and nuclear imaging devices. The exponential increase in the market evaluation of biosensors also shows the popularity and the importance of this area, the expectation for the market to grow from USD 21.2 billion in 2019 to USD 31.5 billion by 2024 [3].

The detection of an organic particle such as a cell, DNA, RNA, virus, enzyme, glucose etc. is not a straight forward process because organic systems use a totally different architecture than our semiconductor and electricity-based computer systems. For example, cells also have many sensors inside and, on their membranes, but those sensors use the chemical matching ability of protein-based enzymes, mostly described as the “lock and key” analogy. Electrical circuitry and computers do not have an ability to read that type of data, so it is required to use something that interacts with those organic molecules and brings the suitable information for the biosensor. The simplest example for this approach may be the X-ray, which uses very high energy electromagnetic radiation to pass through the human body and gives an output by using the penetrability difference of the radiation. One of the many other solutions is to use some tags to interact with organic molecules by chemical properties like enzymes and also detectable for the sensors and other electrical systems.

Although, it seems that the sensing ability of a sensor is the main parameter, it is also important to understand that a sensor is as useful as our ability to read, process, and compute its output data. Thus, the interface circuitry is equally important as the sensor itself and must be designed properly for the purpose. A sensor interface is basically acting as a translator for us, to read out the information from the complex sensors and to generate a suitable output signal or digital code. The main specs for the sensor interfaces are the power consumption, noise, fabrication ease, stability, repeatability, accuracy, area, and the cost.

The goal of this project is to design an electronic interface that takes the analog μV level continuous signal from a specific GMR-SV sensor array which is biased with a quasi-DC magnetization field and DC current and convert it to a binary code as accurately and as efficiently as possible. Since the application is about biomolecular recognition detection, the target is biomolecules which are labeled super paramagnetic or non-remnant ferromagnetic particles. For this application, Dynal M-280 microbeads (2.8μm diameter) were chosen. These particles have micrometer scale and are attachable to biomolecules. Under a small magnetic field, these particles acquire a magnetic moment, which produces a fringe field over the sensor. This induces a change in magnetoresistive sensor resistance, which is detected by passing a DC current through the resistive bridge.

There are three main blocks in the project, which also separates the chapters of the thesis. First one is the sensor selection and modeling; this section covers some required information and analytical and electrical modelling steps of the GMR-SV sensor. The next chapter is the analog front-end, which is the part that the noisy, small analog signal is amplified for the data acquisition block. The following chapter is the analog to digital converter, where the analog data is converted to a digital code for the register. This chapter also includes the details and challenges through the process. A brief conclusion is also presented at the end of the thesis for analyzing the results, commenting on them, and also presenting an opportunity for future work in the area.

2. SENSOR SELECTION AND MODELING

2.1. Brief Information about MR Sensors

First, it is important to define the magnetoresistance (MR) and analyze some common types of sensors. MR is the tendency of a material to react to an applied magnetic field through a change in its electrical resistance [4]. It is important to notice that the magnetoimpedance, a phenomenon causing of the material to change its total impedance value (which includes the resistance part also an imaginary reactance part) by the applied magnetic field, while an alternating current flows through is not the same concept (Magnetoimpedance) [5]. In our case it is simply,

$$R = f(B) \tag{2.1}$$

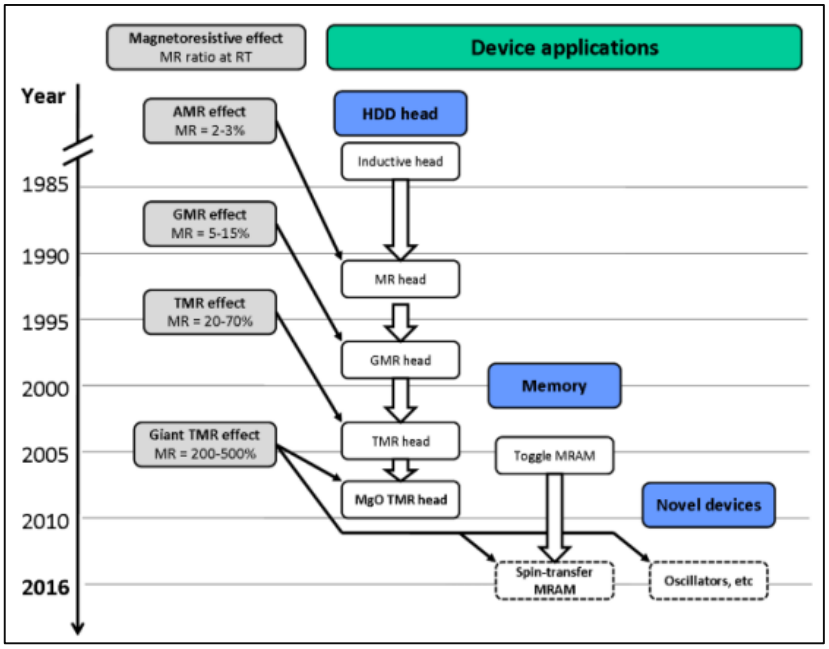


Figure 2.1. The evolution of the MR [6]

Even though the discovery of MR was in 1856 by Lord Kelvin, the improvements and implementation of the materials as sensors in the market was the in early 90s with replacing the inductive read heads with AMR sensors. For a clear review, it might be helpful to see the difference and the market shares of the sensors. Figure 2.1 represents the timeline and MR ratios of most popular MR structures, and Figure 2.2 shows the market shares for 2005. In that year the total market size of magnetic sensors was 965 million USD. With new values and trends, of a market size of USD 2.65 billion by the year 2022 was predicted according to the report of Grand View Research, Inc. [7].

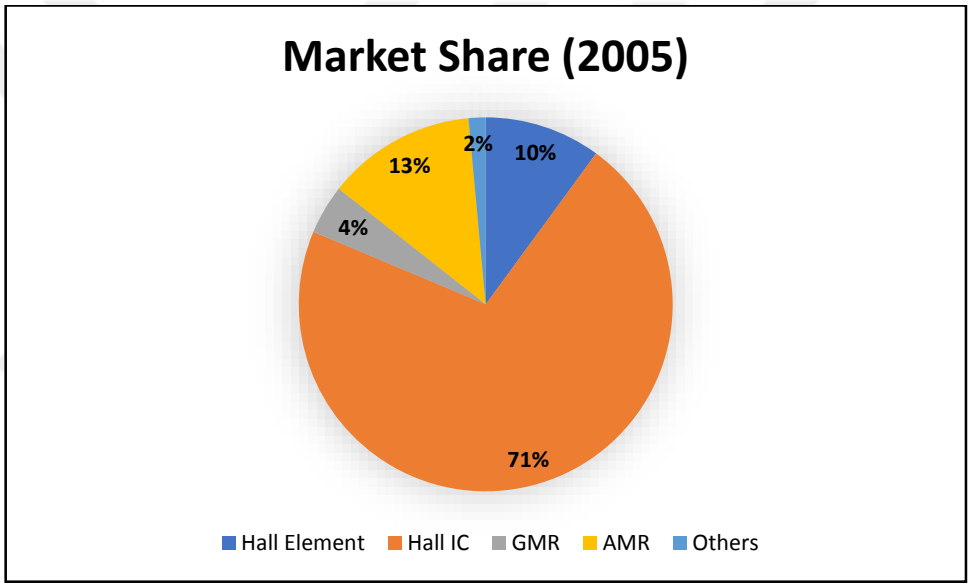


Figure 2.2. The market share of the magnetic sensors (2005) [7]

However, MR sensors have similar properties and working principle, the MR ratios gives us a huge difference in performance. Nevertheless, for TMR and other new MR sensors, it is important to say that the fabrication complexity is another problem. GMR and AMR sensors are fabrication friendly structures, but with TMR things get more complicated. So, for now, it is more practical to use an improved version of a standard multilayer GMR, Spin Valve GMR sensor. This sensor is easy to fabricate, highly imtegratable with CMOS systems (even with on-chip applications), linearizable, and the MR ratios are acceptable for even nT fields [8].

Once, the structure for the application is determined, the details of the GMR-SV structure should be studied. The most important specs are the detection limit, sensitivity, and linearity. Thus, those three must be satisfied with chosen sensor. To figure out those specs and create an electrical model, we initially need to cover the theory behind the sensor and moreover the mathematics of its interaction with the micro beads.

2.2. Spin Valve Sensor Structure

The history of spin valves begins in 1991 [9]. The first sensor design and verification and their first implementation as read heads were made in 1994 [10]. Spin valves basically have the same GMR effect, and they replaced the AMR read head applications with great pace [11].

In GMR multilayers, the magnetization direction relies on the conductive layer (Cu) spacer thickness, which results in oscillatory coupling [12]; however, in the SV structure, one layer is pinned while the other is free to rotate. For a standard SV structure, there are two ferromagnetic layers and a Cu spacer, as shown in Figure 2.3. The MR ratio increases fast with the decrease in the Cu thickness until the continuity level of the Cu layer (1.5- 1.8 nm for Ta buffers). Nevertheless, this kind of decrease results in an increase in interlayer ferromagnetic Néel coupling, so the optimum levels for the Cu layer are usually found to be around 2-2.5 nm. Referred to the lattice Boltzmann equation model, the MR ratio and the ferromagnetic layer thickness relation depends on the interfacial transmission coefficients at Cu/F interfaces and on the spin-dependent bulk mean free paths in the ferromagnetic layer. The choice in the type of ferromagnetic material ($Co_{90}Fe_{10}$, $Ni_{81}Fe_{19}$, Fe) and its thickness (6 nm to 3.5nm) determines the maximum MR occurrence [13].

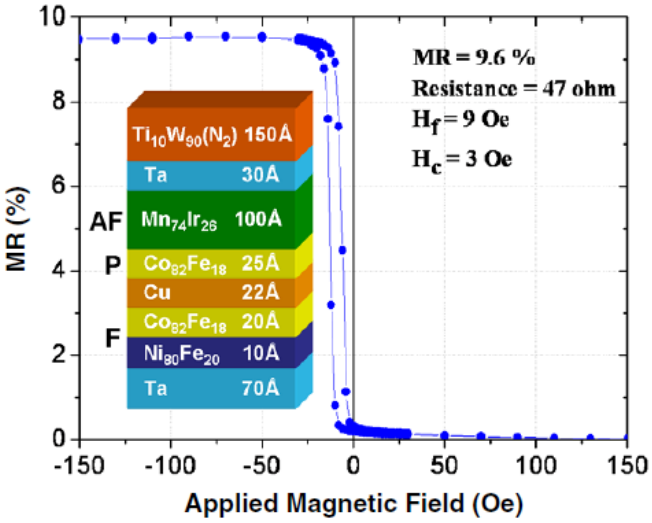


Figure 2.3. A typical SV structure, with two ferromagnetic layers [14]

To use SV structures or any type of material as a sensor, we must linearize its transfer characteristics. In our case this can be easily achievable by inducing the transverse magnetization direction in the pinned layer, whereas the free layer is in the longitudinal direction. Figure 2.3 illustrates the transfer curve, the biasing and a conceptual diagram of an unshielded spin valve sensor with perpendicular layers (better for sensor application). To understand the relations and the biasing, Equation 2.2 gives us the standard output voltage expression for an unshielded SV sensor.

$$\Delta V = \frac{1}{2}\left(\frac{\Delta R}{R}\right) R_{\mathrm{sq}} I \left(\frac{W}{h}\right) \langle \cos(\Theta_f - \Theta_p) \rangle \qquad (2.2)$$

In this expression, $\Delta R/R$ is the maximum MR of the SV sensor (8-20%), R_{sq} stands for the sensor sheet resistance (typically varies between 15-20 Ω/sq), W is the width of the read element, h is the sensor height, I is the current, Θ_f is the angle between the free layer magnetization and the longitudinal normal direction, and Θ_p is for the pinned. For a linearized output the Θf,Θp values should be 90° and 0°. For simplification (assume the magnetization of layers is uniform and W>>h), the expression takes the form:

$$\Delta V = \frac{\frac{1}{2}\left(\frac{\Delta R}{R}\right) R_{sq} I \left(\frac{W}{h}\right)\left(H_a + H_{bias} + H_{coupling}\right)}{H_{keff}} \tag{2.3}$$

and,

$$\langle \sin(\Theta_f) \rangle = \frac{\left(H_a + H_{bias} + H_{coupling}\right)}{H_{keff}} \tag{2.4}$$

In Equation 2.3, H_{keff} is the effective anisotropy field and H_{bias} is the bias field used to center the transfer curve [15]. $H_{coupling}$ stands for the sum of the ferromagnetic Néel coupling between two layers.

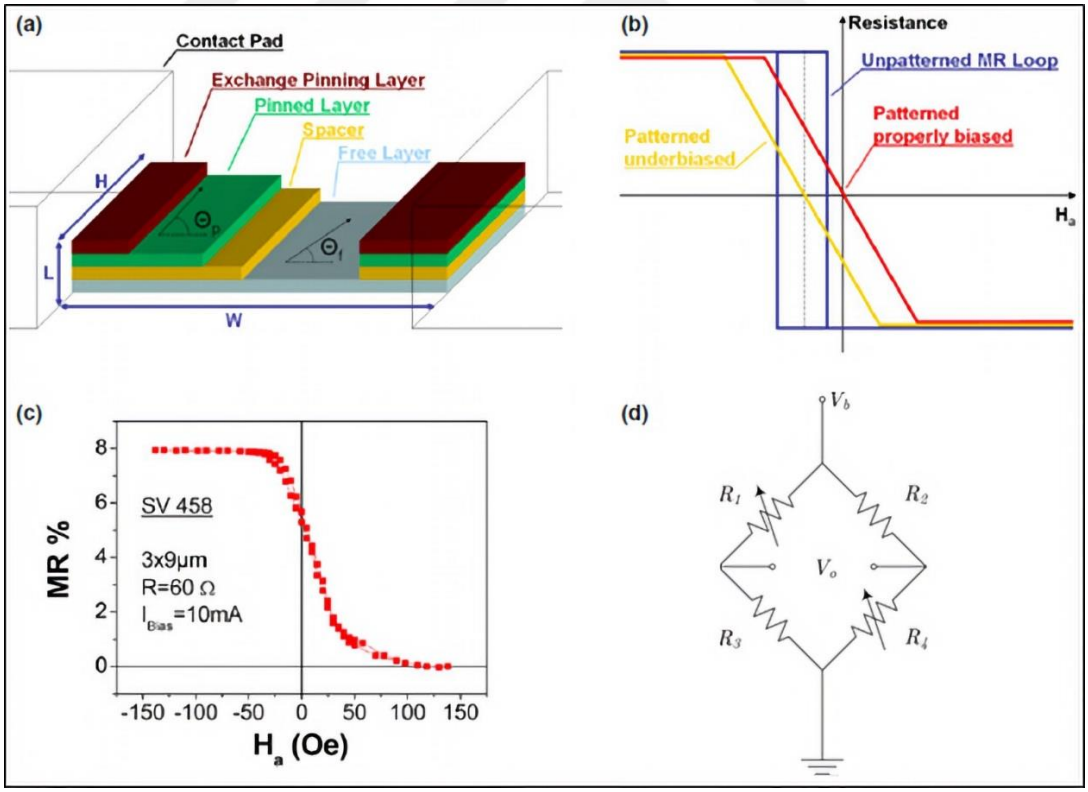


Figure 2.4. (a) Unshielded Spin valve sensor schematic, (b) linearized transfer curve for different biasing conditions, (c) the experimental transfer curve (INESC-MN), (d) the bridge configuration.

The transfer curve is the main output characteristic of the sensor. Figure 2.4(c) shows us a common curve for a specific sensor. This curve shows that the resistance change in the sensor is not changing linearly with the external field. To see more clearly, Figure 2.5 shows the resistance change rather than MR ratio. It is obvious that we need to determine the linear range of the sensor and work inside that range. The saturation field is also another important parameter for those sensors, which is the point that sensor will not react appreciably to the increase of the field after this value.

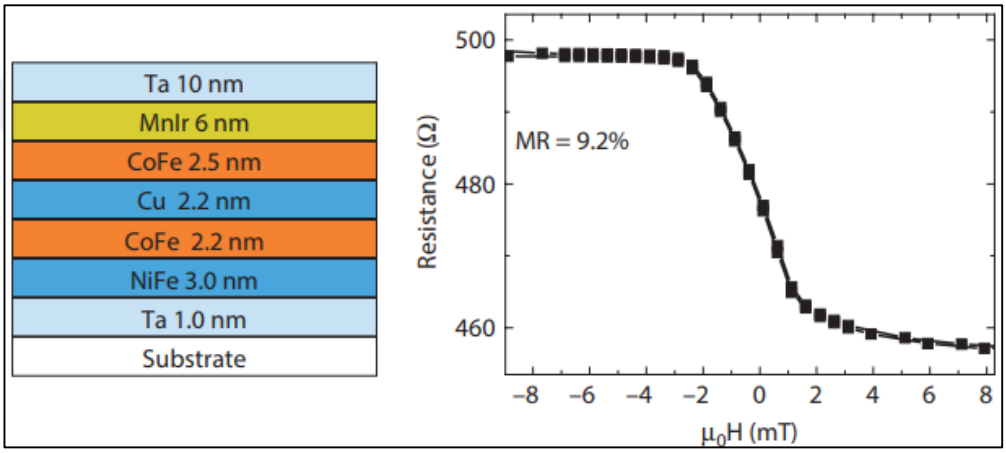


Figure 2.5. The transfer curve and typical structure of a 10x2 μm^2 active area SV stack [16].

When it comes to detectivity, it is important to look at the signal-to-noise ratio (SNR) and the noise considerations of the sensor. Detectivity denotes the lowest magnetic field that produces a signal which is higher than the noise floor. Thus, the noise characteristic of the sensors should be investigated first. The inevitable thermal noise, which is mainly caused by the random thermal motion of electrons is given by the expression:

$$S_{Vth}\left(\frac{V^2}{Hz}\right) = 4k_B TR \tag{2.5}$$

Here, T is temperature, R is the sensor resistance, and k_B is the Boltzmann constant. It is important to note that this noise is only dependent on R and T values so that the only option to decrease the noise is to select a low resistance sensor, which also is not limitless since it creates a trade-off between signal level and bias current. Another noise type for us to consider is shot noise, which can be calculated by the simplified equation:

$$S_{Vsh}\left(\frac{V^2}{Hz}\right) = 2qIR^2 \tag{2.6}$$

When it comes to shot noise, sensor resistance is even more effective for the noise floor consideration, nonetheless, the electron charge (q) dominates this expression and for most applications, shot noise is negligible. Especially in biomolecule detection applications like ours, the frequencies are in the quasi-DC range so the main noise source for us to deal with is 1/f (flicker) noise. Before analyzing the 1/f noise behavior, it is required to analyze the trade-off between the signal level, noise floor, sensitivity, detection limit, and SNR of the sensor.

The simplest version of the output voltage of the sensor can be written as,

$$V_{out} = \big(R_0 + \delta R(H)\big)I \tag{2.7}$$

If the sensor is linearized and properly biased with a centered transfer curve, Equation 2.7 becomes,

$$V_{out} = \left(R_0 + \frac{\delta R}{\delta H}.H + \cdots\right)I \tag{2.8}$$

The next terms with the higher power of H can be neglected due to their extremely low values, so that the expression yields the sensitivity value which is,

$$S(T^{-1}) = \frac{\delta R}{\delta H}/R_0 \tag{2.9}$$

In this expression, R_0 is the initial resistance of the sensor and this parameter is very suitable for us to compare the different sensors and to obtain their detectivity value, which corresponds to the PSD divided by the sensitivity. For example, if the noise floor and the sensitivity of sensor are given, as 10nV/sqrt (Hz) and 10V/V/T respectively, the detection limit of this sensor will be 1pT for 1V of bias voltage.

As mentioned before, for the low frequency applications the noise floor is determined by the 1/f noise of the sensor. The Equation 2.10 which is proposed by Hooge [17] gives us a good approximation of the SV 1/f noise value.

$$S_{v\left(\frac{1}{f}\right)}\left(\frac{V^2}{Hz}\right) = \gamma . I^2 . \frac{R^2}{N_c . f} \tag{2.10}$$

Here, the dimensionless Hooge parameter and N_c which is the number of carriers are in our case experimentally found for the selected sensor and placed in the expression. Hence, this expression may not very accurate for calculating the exact noise value, but it is suitable to observe the relation of the 1/f noise with the sensor parameters and modify the sensor design for lower noise levels. In our application the 1/f noise of the sensor will be the main issue for the detection limit and sensitivity. By the guidance of this information and expressions, the SNR of the sensor may be found by,

$$SNR\left(\frac{V}{V}\right) = \frac{V_b}{V_n} . \frac{\Delta R}{R} = \Delta R . \frac{I_b}{V_n} \tag{2.11}$$

2.2. Micro-beads and Surface Equations

To create an analytical or an electrical model, it is vital to understand and investigate the magnetic beads, their properties, and their interaction with the sensor surface. Since the sensor response depends on the fringe field of the microbeads, the first consideration for the beads will be to have a high magnetization. They must be small enough such that they do not hinder the biomolecular processes; furthermore, they must have non-remnant state in magnetic moment to avoid clustering when suspended in the solution. The magnetization field must be applied to those beads, in order to create the fringe field. This external field may be DC, AC, or DC+AC.

There are many useful options in the market for bio-recognition purposes, one of them is Dynal M-280 beads [18]. These 2.8 μm-diameter beads are composed of magnetic γ-Fe_2O_3 and Fe_3O_4 nanoparticles dispersed in a polymer matrix, with an average magnetic ingredient of 17 wt% [19]. The nanoparticles within those beads are usually named as superparamagnetics. Due to their small sizes, they have the ambient thermal energy greater than the magnetic alignment energy, which allows them to spontaneusly demagnetize at room temperature, thus creating the fringe field we need. Nonetheless, Dynal M-280 beads have good biocompatible surface properties and are monodispersed in size. However, their magnetization characteristics are not quite optimal. Besides having a relatively low saturation level for magnetization, the magnetic content among the beads varies much (with a standart deviation of 72%), and some of the beads are non-magnetic [18]. To obtain a larger and more consistent signal from the labels, it may be more useful to work with a 100% magnetic content [20]. To observe a more ideal behavior compared to M-280, figure 2.6 shows also NiFe beads produced by an industrial carbonyl process that creates polydispersed, pollycrystalline spherical particles with 800nm to 4μm diameter [21].

Although it seems like the main property of the beads is the magnetization ability, it is actually the second step. The first one is the magnetic moment of the beads, from the which the magnetization may be found. Thus, the definition of the magnetic moment is, the quantity that represents the magnetic strength and orientation of an object that produces a magnetic

field. The connection between magnetic moment and the magnetization is given in Equation 2.12.

$$M\left(\frac{kA}{m}\right) = \frac{m_0}{V}\left(\frac{emu}{m^3}\right) \tag{2.12}$$

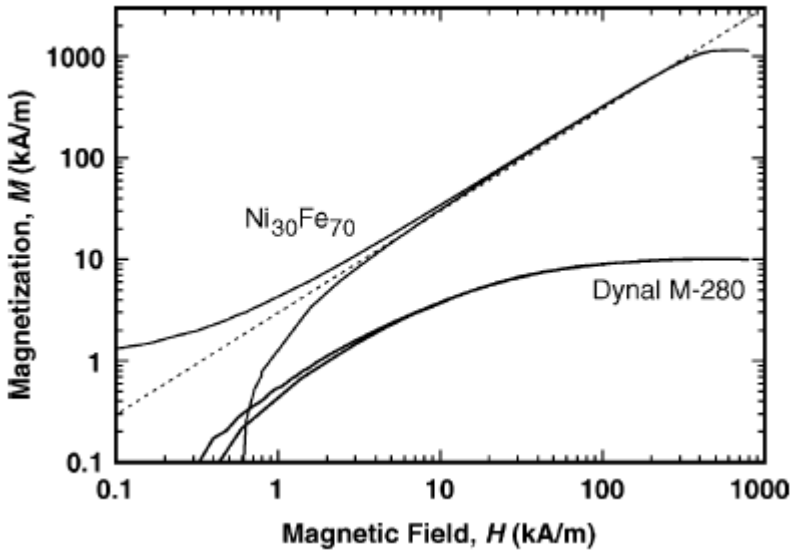


Figure 2.6. Magnetization versus the magnetic field for Dynal M-280 and NiFe microbeads, the dashed line shows the theoretical maximum for an ideal paramagnetic sphere [1]

Magnetization is the magnetic moment per volume. If we assume the beads are perfectly spherical, magnetization is given by,

$$M\left(\frac{kA}{m}\right) = \frac{m_0}{\frac{4}{3}\pi r^3}\left(\frac{emu}{m^3}\right) \tag{13}$$

The magnetic moment of the beads should be determined. This is quite difficult because of the complexity and non-linearity of the formulation. Hence, another way

approach is to check the experimental data for the Dynal M-280 beads with a specific excitation field and get the value from there. The magnetization moment is a non-linear function of *B* field. A magnetic particle is characterized by its susceptibility.

$$M = \chi H \tag{2.14}$$

The fringe field of a particle on the plane of the sensor is,

$$H_x(x,y,z) = \frac{m_0}{4\pi}\left\{\frac{3x^2}{(x^2+y^2+z^2)^{2.5}} - \frac{1}{(x^2+y^2+z^2)^{1,5}}\right\} \tag{2.15}$$

Where the *z* direction is the out of plane direction while *x* and *y* are the transverse and longitudinal directions to the sensor. The *H-B* conversion is simply,

$$B = \mu_0 H \tag{2.16}$$

Now, all the required information about the relation between the parameters and variables to solve the surface equations of the sensor are available. Assuming that we have a sensor with an active area of A (Equation 2.17) and let us investigate the surface equations.

$$A(m^2) = x.y \tag{2.17}$$

In Figure 2.7, *a* is the radius of the bead, *r* is the distance between the center of the bead and the crossing point of the magnetic field, *z* is the distance between the bead and the active area which is *a+t*, where t is the overlayer thickness between the sensor and the bead surface. Incorporating these into the Equation 2.15, (the *x* and *y* direction components of the

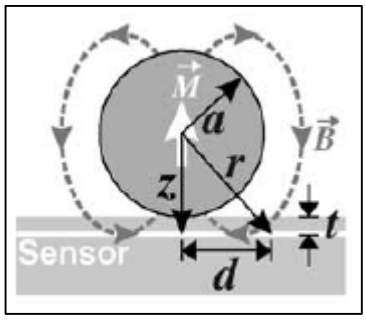


Figure 2.7. The cross section of the bead over the active area

magnetic field is low enough to ignore) we can find the maximum *B* field (at the center) created by the demagnetization of the bead, over the sensor, which is given in Equation 2.17.

$$B_{x,max}(0,0,z=a+t)=\frac{m_0}{4\pi}\left\{-\frac{1}{(a+t)^3}\right\} \tag{2.17}$$

This magnetic field produced by the demagnetization of the M-280 beads is the driving force to get information about the bio-molecule being searched in the assay. However, this is just the maximum value of the *B* field. Incorporated into the sensor resistance equation should be the average *B* field through the active surface [1].

$$B_x\big(x,y,(a+t)\big)=\frac{\iint B_{x,max}\big(x,y,(a+t)\big)\,dxdy}{A} \tag{2.18}$$

Equation 2.18 shows an interesting relation, that the B_x field over sensor is inversely proportional to the sensor size. This means that lower detection limits it is wise to use smaller sensors in a form of an array. Some experimental data, which consists of different magnetic particles and two different sizes in active area of the sensor are given in Table 2.1. The given data allows the comparison of different beads and sensor sizes.

Table 2.1. Examples of magnetic properties. The magnetic moment and magnetization measured at a magnetizing field of 15 Oe. [1].

Diameter (nm)	Magnetization (magnetic moment) kA m^{-1} (emu)	B_{max} (T)	$\langle B_b \rangle$ over a $6 \times 2\ \mu m^2$ area (T)	$\langle B_b \rangle$ over a $80 \times 2.5\ \mu m^2$ area (T)
2800	0.40 (4.60×10^{-12})	-1.12×10^{-4}	0.37×10^{-4}	2.79×10^{-6}
2000	0.48 (2.01×10^{-12})	-1.16×10^{-4}	0.24×10^{-4}	1.67×10^{-6}
250	20.1 (1.64×10^{-13})	-4.79×10^{-4}	4.67×10^{-6}	2.46×10^{-7}
130	17.8 (2.05×10^{-14})	-1.10×10^{-4}	6.04×10^{-7}	3.14×10^{-8}
100	0.34 (1.78×10^{-16})	-1.14×10^{-6}	5.28×10^{-9}	2.74×10^{-10}
50	0.85 (5.56×10^{-17})	-4.88×10^{-7}	1.6×10^{-9}	8.61×10^{-11}

2.3. The Signal Generation Process & Analytical Model

The theoretical background required to analyze the SV sensor, the magnetic beads and their interaction was provided in earlier sections. Now, an analytical model will be built, and the signal will be produced over this model. Before beginning, it is important to define the inputs and outputs of the sensor block. The only inputs for the model are the DC bias current (or voltage), the excitation AC magnetic field, and the frequency of this field. The only output will be the differential AC voltage in the resistive bridge.

So far, the magnetic microbeads for the process has been determined, but sensor selection is still an issue. The sensor for this thesis is selected based on the amount of experimental data and low detection limits. For the structure of the sensor given in Figure 2.9, the required data were obtained from the literature [8] [22]. This SV sensor has 7.5% MR ratio, and if sized properly, it can detect the required levels for our application.



Figure 2.8. The chosen GMR-SV structure

Signal generation consists of four different steps (B_{ext} to M, M to $B_{x,avg}$, $B_{x,avg}$ to ΔR, ΔR to ΔV), which are illustrated in the schematic given in Figure 2.10. The first step is to choose the excitation AC magnetic field and its frequency. Since the purpose of the design is biomolecule detection, the frequency can be DC to 1 kHz, the choice in this thesis is 200 Hz, which is again a common frequency for this type of application. The magnitude selection is not that simple. Because of the non-linear behavior of the bead magnetization, it is required to pick a linear region on the magnetization curve of the M-280 beads and remain in that region. After the close examination of the magnetization characteristic of M-280 beads, the linear-like region was selected as B_{ext} from 0.8 kA/m to 4.8 kA/m (10 Oe-60 Oe). An analytical model created in the mathematics software Mathcad®. The necessary formulations have already been given in sections 2.1 and 2.2. The calculation steps were also given in preceding paragraph in details.

The AC excitation field was determined (Figure 2.11.a), the magnetization values of the beads in this region were picked from the diagram given in Figure 2.6, and magnetization as a function of B_{ext} was obtained (Figure 2.11.b).

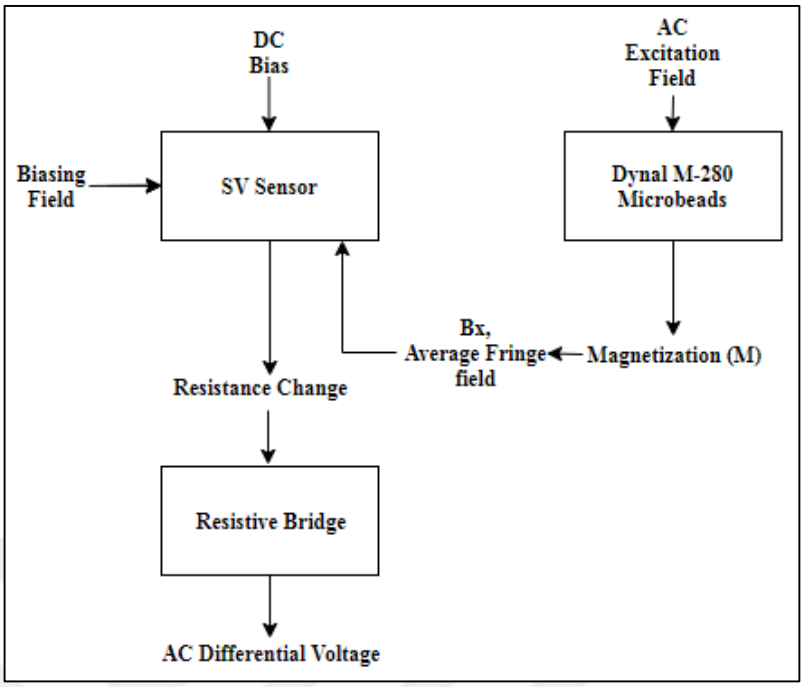


Figure 2.9. The signal generation process.

From the signal given in Figure 2.11, the magnetic moment of the beads was calculated by using Equation 2.12, within the assumption of the beads being perfectly spherical, then from Equation 2.15 the fringe field H_x was found as a function of magnetic moment (m_0).

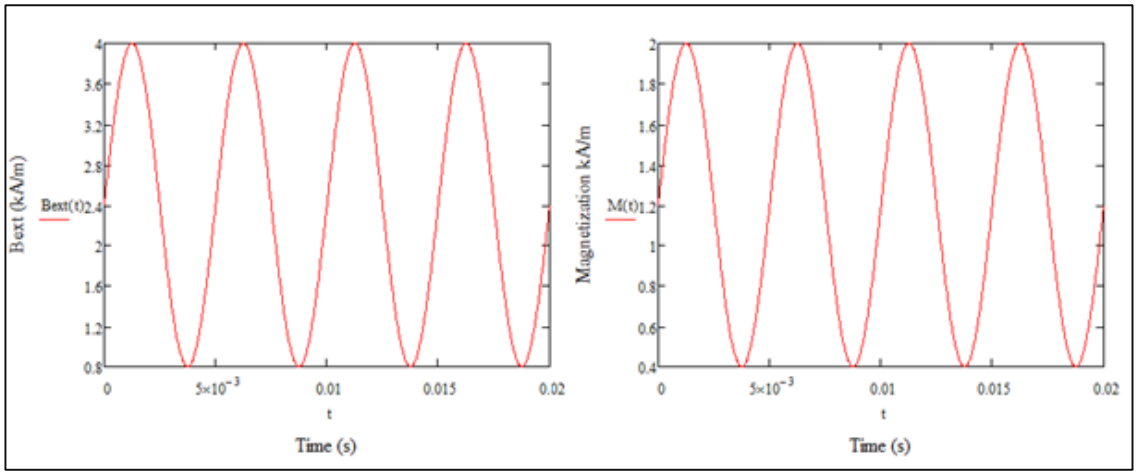


Figure 2.10. The excitation field required to magnetize the beads (a), the magnetization as a function of Bext and time (b).

$H_{x,max}$ was transformed into $B_{x,max}$ by using Equation 2.16 and the average fringe field $B_{x,avg}$ was found by Equation 2.18. This is the field that the sensor will detect, and it is shown in Figure 2.12.

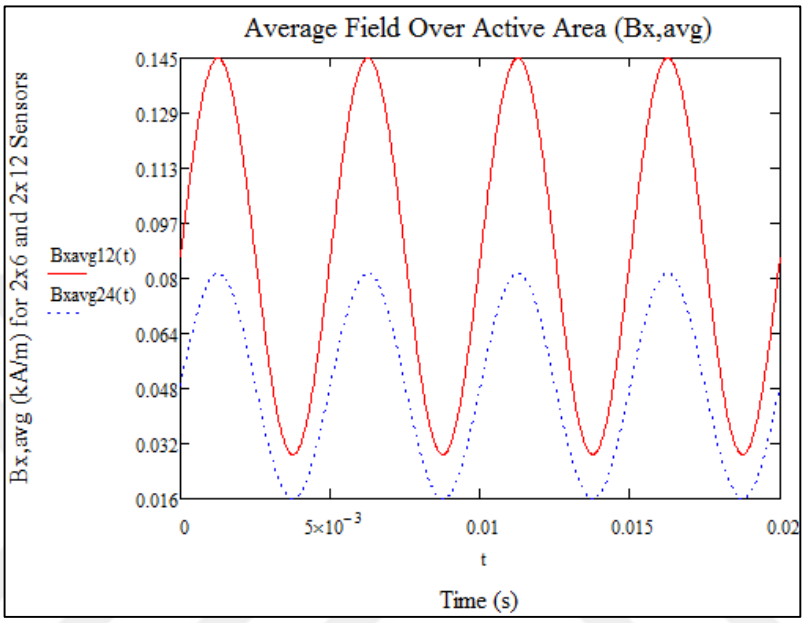


Figure 2.11. The average field over the active area, red line represents 2x6 µm and dashed line 2x12 µm.

Detection of the average field $B_{x,avg}$ by the sensor results in resistance change (ΔR). Even though this ΔR seems to be read out by a simple current flow, a Wheatstone bridge configuration is always a better option for the first step of the resistive sensors. By this implementation, the input signal will be differential, which will be more accurate in terms of resistance mismatch, thermal effects and other unwanted secondary effects. Although there are different variations of bridge configurations (Figure 2.13), the full bridge seems like the best choice in terms of linearity and signal level. Nonetheless, in the case of GMR, this setup is very hard to build. Because of the orientation dependence in the fabrication steps of the GMR structure, usually a half bridge configuration is preferable.

In this thesis, the bridge arrangement is slightly different. The differential advantage of the half bridge is very useful to eliminate the parasitic resistance change due to magnetic

side effects. Thus, the sensor is placed on one branch and a reverse biased version of the same sensor is placed on another branch. This identical reference sensor is also covered by a protective shield, so that it has no interaction with magnetic microbeads. Other two constant resistors are selected to be equal to R_0, the initial resistance of the sensor, so that the setup works like a unique element Wheatstone bridge. Though this setup results in signal level reduction,

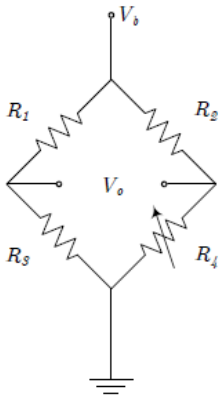
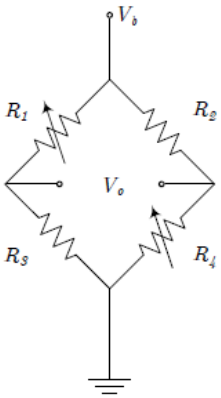
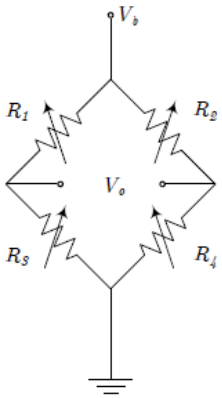
Unique element	Half bridge	Full bridge
		
$R_1 = R_2 = R_3 = R;$ $R_4 = R + \Delta R$	$R_2 = R_3 = R;$ $R_1 = R_4 = R + \Delta R$	$R_1 = R_4 = R + \Delta R;$ $R_2 = R_3 = R - \Delta R$
$V_o = V_b \frac{\frac{\Delta R}{R}}{2\left(2 + \frac{\Delta R}{R}\right)}$	$V_o = V_b \frac{\frac{\Delta R}{R}}{2 + \frac{\Delta R}{R}}$	$V_o = V_b \frac{\Delta R}{R}$

Figure 2.12. The Wheatstone bridge configurations and the output voltage equations

it offers more than it takes. It should be kept in mind that the noise of the sensor is also reduced along with the signal so there is not any significant loss in SNR.

Since the $B_{x,avg}$ to ΔR conversion of the sensor is modeled by the Expression 2.3, R_0 and the DC bias current (voltage) values must be known. The sheet resistance of the sensor was taken from [8] [22] (for the sensor size used in this project R_0=54Ω) and the bias voltage of the bridge was set as 0.864 V ≈0.9V (this is the required bridge voltage for 8mA sensor bias current). Magnetoresistance is an even function of the magnetic field, so the response of the sensor will be at twice the field frequency. The bridge output signal is given below.

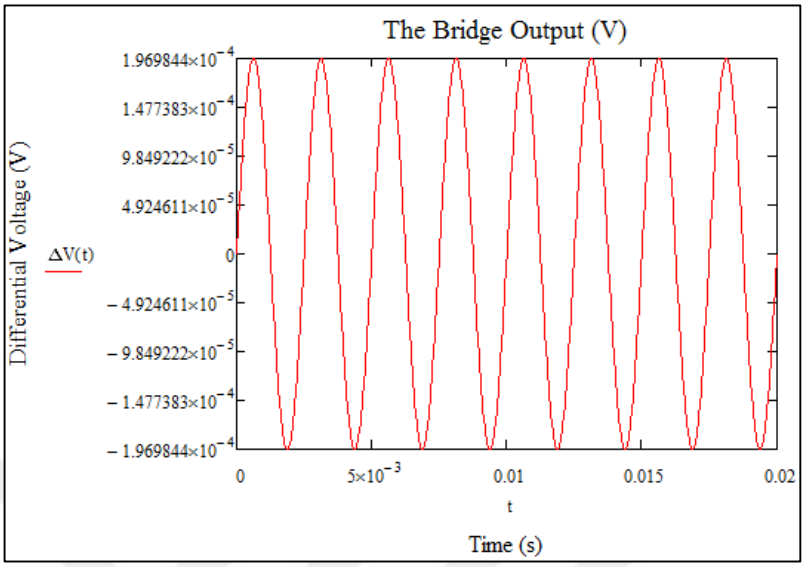


Figure 2.13. The differential output voltage of the Wheatstone bridge

This output signal corresponds to a single bead over the active area; however, this will not be the case once the active area interacts with the assay. The saturation point of the sensor surface interaction with the number of beads is given in (19). According to this expression, up to four beads can be detectable for this sensor. Since it is the minimum case, all the following calculations and simulations will be for only one bead over the sensor. The maximum number of beads will be four.

$$n_{sat} = \frac{2A}{\pi r^2} = 3.898 \tag{2.19}$$

When an output signal is read from a sensing element, another vital consideration is noise. The signal output means nothing if it is already buried under the noise floor. Thus, the three main noise contributions described earlier must be calculated for the same inputs.

First, the thermal noise density is calculated from Expression 2.5, the result is given below.

$$S_{Vth} = 0.946 \frac{nV}{\sqrt{Hz}} \tag{2.20}$$

Shot noise is obtained by using Equation 2.6 and is given below.

$$S_{Vsh} = 2.734 \frac{nV}{\sqrt{Hz}} \tag{2.21}$$

Since the selected frequency of operation is rather low, the 1/f noise will be the main problem in the detection limit. The expression given in Equation 2.10, allows a frequency sweep to be performed and compared with experimental data. The simulated data looks very similar to the experimental data in literature. Since the sensor dimensions in our application are different, it is not possible to have exact numbers, but the error is not crucial. The results for 1/f noise are given in Figure 2.15.

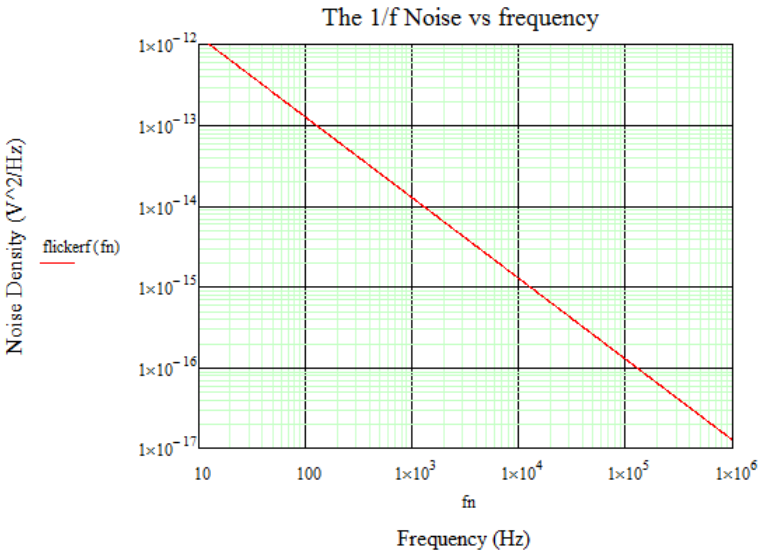


Figure 2.14. Sensor 1/f noise versus frequency

$$S_{\frac{V1}{f}}(400Hz) = 0.22\ \mu \frac{V}{\sqrt{Hz}} \tag{2.22}$$

As expected, the 1/f noise density dominates the output noise of the sensor. When it comes to minimum detection limit, since the other noise components are negligible compared to 1/f noise, the required value for the rms noise will be the 1/f noise only. Thus, the detection limits versus the frequency and the sensing are given in Figure 2.16.

$$Detection\ Limit\ (D) = \frac{1}{S}\sqrt{\left(\frac{\gamma}{A.f}\right)} \tag{2.23}$$

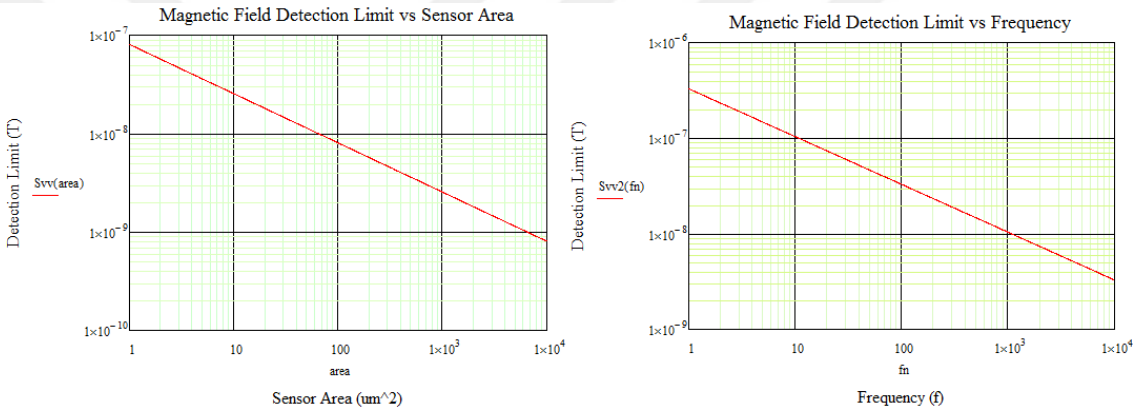


Figure 2.15. The detection limit graph vs sensor area (left), and frequency (right)

For the selected sensor size in this project and at the frequency of 200 Hz, the minimum detectable field is,

$$D(200Hz) = 23.2\ nT \tag{2.24}$$

So far, all the experimental data, the sensor dimensions, and the selected inputs were used to have a signal generation process. The resistive bridge differential signal, the output noise, and the signals in the intermediate steps of the process were modeled analytically.

2.4. The Electrical Model

There are only three inputs for the electrical model, which are given to SPICE with ".param" command (*Vb, f, B_{ext}*). The complete schematic of the electrical model is given in Figure 2.17.

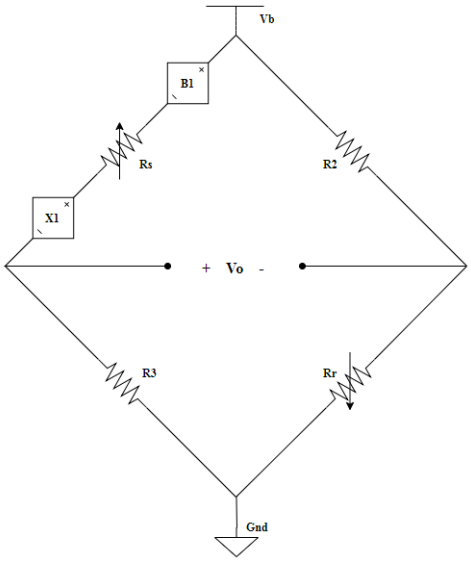


Figure 2.16. The electrical model of the resistive bridge

Since the triggering signal is the external AC excitation field, it will be the first step of the procedure. The magnetic field expression put into the line and magnetic field was integrated into the circuit as a sinusoidal voltage source. This source is not connected to the circuit, it only drives the behavioral source *B1*. The output of *B1* is the ΔV of the SV sensor. Since the resistance change in SPICE is not very useful, with this method, the behavioral voltage source helps us to implement the required expressions to the sensor model. Circuit has two nodes with a voltage difference of V and it is put into a mathematical expression to get the output voltage or current by a controlled voltage source.

So, the DC biased sensor bridge is separated from the noise source. The noise source implementation is more complicated because the noise signal includes infinite number

random signals with different frequency components, and LT SPICE does not have a behavioral noise source. One way to solve the problem is to use a behavioral noise source if available, another way to implement the noise is create a subcircuit which is fed by the sensor output and creates an output with quite large in terms of noise and small in terms of signal. The frequency characteristics of the 1/f noise was obtained by an RC circuit. A huge resistor value was used, to obtain a noise density conforming to the calculations. The results are depicted in Figures 2.18 and 2.19.

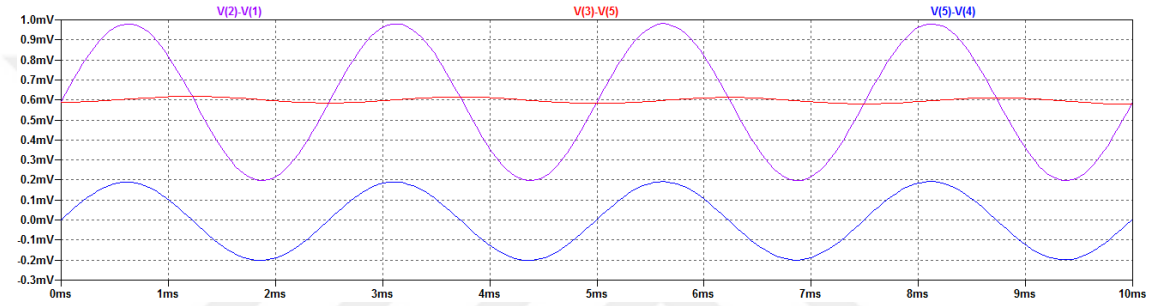


Figure 2.17. The bridge output (blue), the ΔV of the sensor (purple) and the noise source output (red)

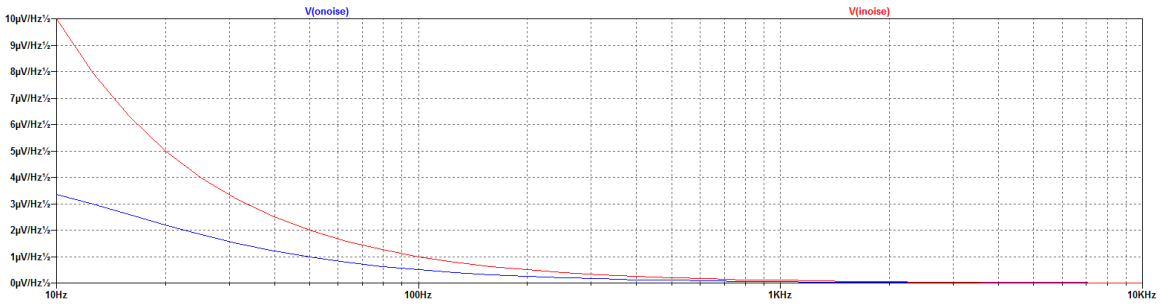


Figure 2.18. The input-output noise density of the sensor model

The output noise density is approximately a quarter of the input noise density. This noise reduction happens due to the Wheatstone bridge configuration, as expected. On the contrary, the bridge output is only the half of the sensor signal ΔV, which is in fact not possible. In calculations of ΔV, the current reduction factor (due to resistance change) was already included, so that the observed sensor signal (ΔV) in the simulation is already reduced

by half. This discrepancy is caused because of using ΔV instead of ΔR. Since the shot noise and thermal noise are ignorable compared to 1/f noise, they were not included in the model. By using the output data, the SNR was found as 46dB which is in the common range for this type of sensors, and it is perfectly normal to get less than 50 dB with this type of small-sized, minimum field detection kind of sensor.

$$SNR_{SV} = 20\log\left(\frac{\Delta \mathrm{V}}{\mathrm{V}_{\mathrm{n_{rms}}}}\right) = 46dB \tag{2.25}$$

The electrical model of the sensor was built and simulated in SPICE and the output voltage signal was obtained by using only three input parameters according to the calculations. The signal and noise simulations were matched with the analytical results.

2.5. Summary

Since the focus of the application is designing a low-noise and low-power interface for the selected bioparticle-sensing application, the secondary effects in the sensor parasitic, quantum mechanics in the sensor structure (spin-dependent electron transportation, spintronics), layer level sensor design and fabrication steps, highly non-linear bead magnetization equations were not included. As a matter of fact, the sensor design may also be a complete thesis subject with more modern technologies (TMR sensors, CMR sensors, shielded GMR sensors, Flexible AMR sensors, 3D-GMR applications) or with extreme specs with additional performance improvements (pico-tesla level detection limits, ultra-low power, etc.). The summary for the sensor side is given in the Table 2.2.

Table 2.2. The summary of the sensor selection and modeling.

Sensor Sizes	2 μm x 6 μm
Sensor bias current (I_b)	0.8 mA
Detection Limit	23.2 nT
Sensor initial Resistance (R_0)	54 Ω
Magnetic beads	Dynal M-280
Bead diameter	2.8 μm
Excitation Field (B_{ext})	0.8 - 4 kA/m sine wave with 2.4 kA/m offset
Excitation Field Frequency (f_B)	200 Hz
Differential Bridge signal (single bead)	200 μV peak sine wave
Saturation limit for the beads (Nc)	4
Output signal frequency (f_o)	400 Hz
Thermal Noise Density	0.946 nV/√Hz
Shot Noise Density	2.734 nV/√Hz
1/f Noise Density	0.22 μV/√Hz
SNR	46 dB

3. ANALOG FRONT-END

3.1. The Art of Designing Sensor AFE

When it comes to design electronic circuitry for sensing applications, the process usually includes [23],

- The sensor array (identical or different sensors)
- A proper biasing
- Analog front end electronics (usually begins with a preamplifier)
- A data acquisition system (ADC)

In the given chain (Figure 3.1) the most challenging part (for most of the applications) is usually the design of AFE, because that section is the first electronic part that has to deal with the extremely low and noisy output signal of the sensor. A common structure for the AFE circuitry may include preamplifier, filters, operational amplifiers, lock-in amplifiers or sometimes different integrated circuits for specific applications.

A typical bio-application sensor output voltage (or current) generally has a small amplitude level with noisy power spectrum and low frequency. The first approach with this signal should be filtering and amplifying the low-level signal to a proper level for the following circuitry. The requirements for the front-end electronics, beside processing the extremely low sensor signal levels, are to have low power consumption, small die area and components compatible with integrated circuits.

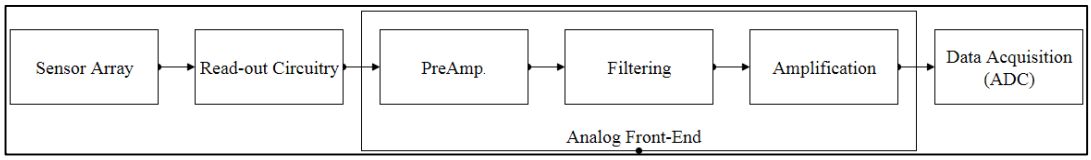


Figure 3.1. The sensor interface block diagram.

There are three inevitable design metrics for to begin the AFE design.

- The input source impedance
- The bandwidth
- The minimum input signal level

In our case, the resistive sensor array impedance is not very large; on the contrary, for a single sensor it is around 60Ω which gives the designer, the freedom of aiming for slightly lower input impedances. The bandwidth of the signal is in our case 400 Hz. But as precaution, it is wise to take it as 500Hz for a design specification. This bandwidth is very design friendly in terms of gain-bandwidth trade off. However, the minimum signal level to process is an issue. Because, 0.2mV to 0.8mV signal levels dictate the AFE to have an input referred noise much smaller than these levels. Moreover, the low-power consumption and the large voltage gain requirements make it even more challenging.

3.2. The Selection of the Topology

Sensor selection and modeling was covered in the second chapter. The input signal is a continuous sine wave with 400 Hz frequency, zero offset, and 0.2, 0.4, 0.6, or 0.8 mV magnitude depending on the number of the magnetic beads.

The high gain, very large CMRR, high input impedance, and good noise characteristics of the instrumentation amplifier (IA), makes it a popular choice in front-end electronics. One

of the simplest and most popular IA configurations is the three-OPAMP IA. Although, it seems like a perfect choice in terms of given specifications, it is also power hungry, which is undesirable. The resistance mismatch and die area are other problems. The resistance values for an IA are usually a bit large for IC applications.

A more suitable topology for this application is capacitively coupled chopper instrumentational amplifier (CCIA). The main reasons to select this topology are discussed below.

The capacitive coupling helps with the DC common mode signal rejection, without any power consumption, if the applied voltage is less than the breakdown voltage level of on-chip capacitors. Hence, wide common mode voltage rejection range (CMVR) can be achieved.

CCIA usually contain a multistage amplifier with a feedback loop, thus being able to produce high enough output gain.

The chopping technique is one of the most effective ways to design a low-noise amplification stage. In our case, the main noise spec is that the input referred noise must be considerably small compared to the input voltage, which is in the micro-volt level. It is known that the amplifiers generally do not have a good response for low frequency signals due to high 1/f noise region. So, the solution is to push the signal away from the 1/f corner frequency of the amplifier (especially the first stage), by applying chopping. Although, chopping is marvelous in terms of noise reduction, everything comes with a price, and in this case the nice large input impedance of the amplifier actually has been replaced by the SC resistance of the input choppers, which is in the range of kΩ to MΩ, which is not acceptable for many of the operations so it may be required to use an impedance boost loop. Another problem with chopping is that the up-modulated offset and 1/f noise of the amplifier would result in ripples in the output. A low-pass filter is the most basic way to eliminate that

ripple but instead of using large passive components, which is usually necessary, we will look for power efficient and small sized alternative methods.

It is possible to design a power efficient CCIA, because the main trade-off for power consumption is the current-noise relation. With the advantage of the chopping and using capacitive elements instead of resistive ones, it is possible to design circuits with very low currents and still have nice noise characteristics.

3.3. CCIA Structure

Although CCIA have enjoyed increasing popularity recently, in fact, the invention of the capacitively coupled chopper amplifiers was in 1940 [24]. The input signal has been modulated by a chopper, then amplified and demodulated, but the problem with that circuit was there was no CM rejection. Thus, the DC CM voltage was also modulated. To prevent this CM voltage amplification problem, the giant leap was to implement the configuration full-differential manner. In fully differentially configuration, the rejection problem of the CM voltage was solved. The differential signal was up-modulated by the input choppers, passed through the input capacitors, amplified then de-modulated to the baseband by the output choppers. The rejection of CM voltage however, brings another problem, the requirement for the CM level of the amplifier. To solve this, the first approach was using biasing resistors with a reference voltage to fix the input and output CM levels of the amplifiers. Nonetheless, the output resistors limited the gain (transconductance) of the amplifier so the trade-off between those variables was an issue.

The first capacitively coupled chopper instrumental amplifier is relatively young topology. The first implementation was in 2007 [25] by Timothy Denison. The elimination of the output capacitance and resistances was a huge breakthrough. Instead of those, a capacitive chopped feedback loop was implemented for defining the closed loop gain of the system. Since, the designer was intending to use that system for bio-applications, he also added a DC servo loop to filter out the huge DC component.

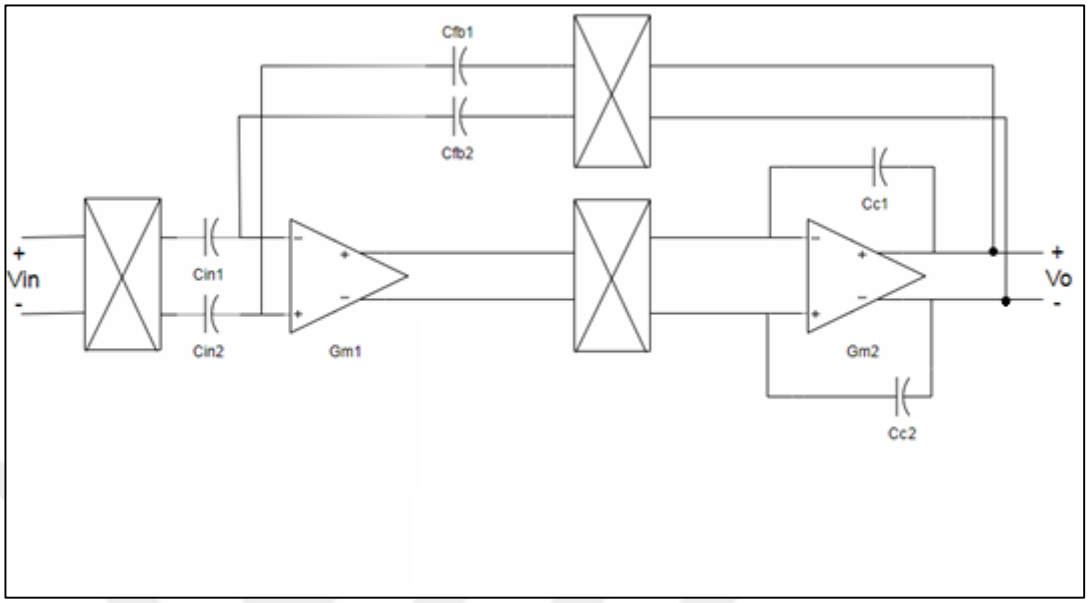


Figure 3.2. The electrical schematic of the CCIA

The circuit schematic in this thesis is given in Figure 3.2. It includes a main signal path with two stage fully-differential chopper amplifier, input capacitances and Miller compensation capacitances, a negative feedback loop with capacitances and another chopper to determine the closed-loop gain. Although a two-stage structure may have a large enough open-loop gain, it is not wise to get almost 1000 times gain with that structure due to large mismatch of capacitances in the feedback branch and the input branch. So, a simple way to bypass that problem is adding a cascade gain amplifier after the CCIA to divide the gain and reduce the mismatch between capacitances.

There are four different active blocks in the system and ten capacitors. The active blocks will be discussed on the following pages.

3.3.1. The Choppers

As explained before, the chopping technique reduces the offset and noise disturbances by modulation and demodulation of the small low frequency signals, and upmodulating the

offset and noise of the amplifier (Figure 3.3), thus enabling a low noise low offset behavior for the system. Chopping consists of two synchronized polarity-reversing choppers, one for modulation another for demodulation. The individual choppers include four fast enough switches driven by a clock signal with two complementary phases at a chosen frequency (Figure 3.4). In CMOS technology, those switches may be selected as MOSFETs, usually NMOS due to speed advantage.

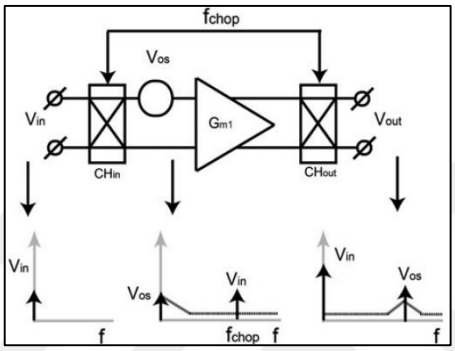


Figure 3.3. The chopping technique in frequency domain [26].

As a design parameter, it is vital to select a proper chopping frequency (f_{chop}). It must be much higher than the signal frequency, and higher than the 1/f noise corner of the first stage of the amplifier (since the main noise source for the AFE is that stage). Nevertheless, it also should not be much higher due to the switched capacitor effect of the input chopper, which determines the input impedance of the CCIA (Equation 3.1). The charge injection and clock feedthrough errors also increase with f_{chop}.

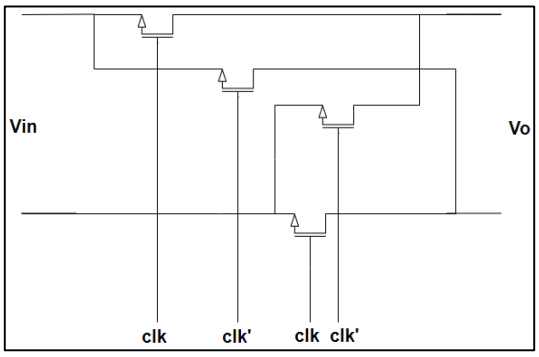


Figure 3.4. The schematic of a chopper with NMOS devices

So, an optimal point will be around the 1/f noise corner of the G_{m1}. In our case it has been chosen as 10 kHz, which is much higher than our signal band and higher than the 1/f noise corner of the Gm_1 (8.5kHz).

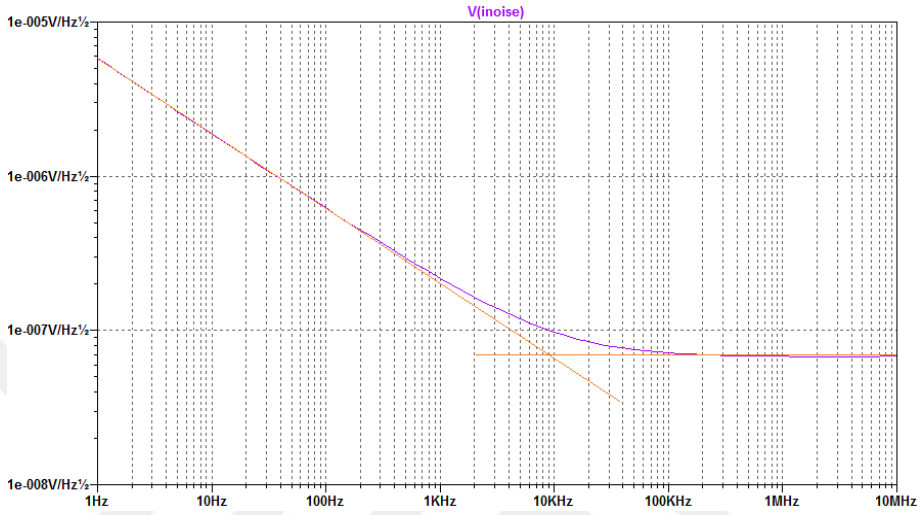


Figure 3.5.1/f noise corner of the Gm_1

Frequency selection is not the only thing matters with choppers, perfect symmetry in the layout are also very important. Sizing of the MOSFETs is a straight-forward operation, they all sized to the minimum of the technology (UMC 0.18 in our case). This is due to the speed requirements, as well as minimizing the charge injection errors which increase with the device size.

In case of very large DC CM voltage level signals or very parasitic sensitive applications, there are more advanced chopper topologies (protected by diodes, used as a latch circuitry...etc.), but in our application this is not a concern; the simple one is always better if there is no reason to modify it.

Input impedance is one of the main parameters for amplifiers; fortunately, the huge input impedance caused by the gate of the input differential pair MOS devices handles that problem well. Since in our case, the input impedance level is determined by the input

chopper and the capacitance, additional impedance boosting might be necessary in situations where high input impedance is required. Substitution of the f_{chop} and C_{in} values in Equation 3.1 yields a very high Z_{in} which is suitable for the application at hand.

$$Z_{in} = \frac{1}{2\pi f_{chop} C_{in}} = 159M\Omega \tag{3.1}$$

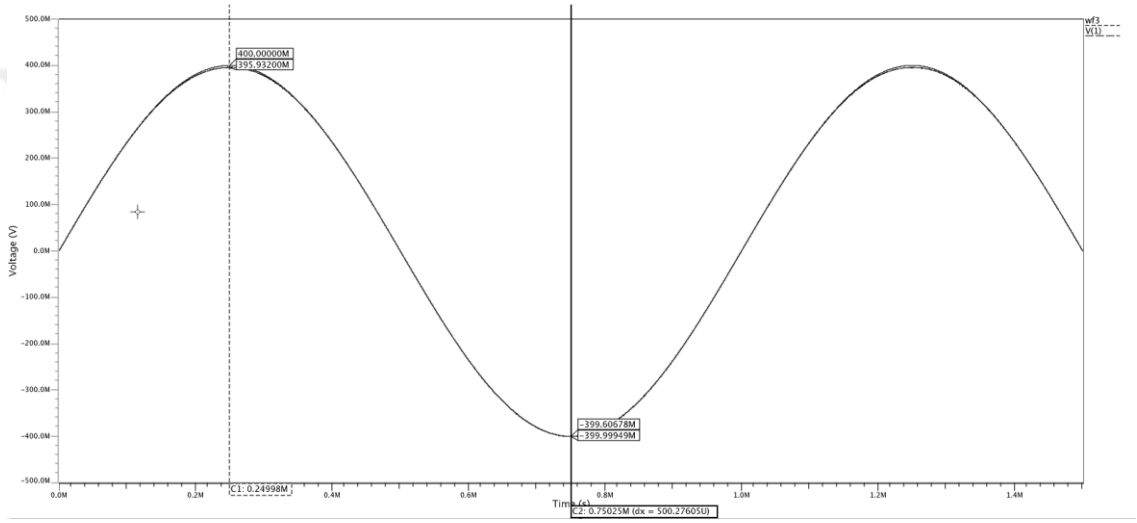


Figure 3.6. The pre-layout transient response of two cascading choppers.

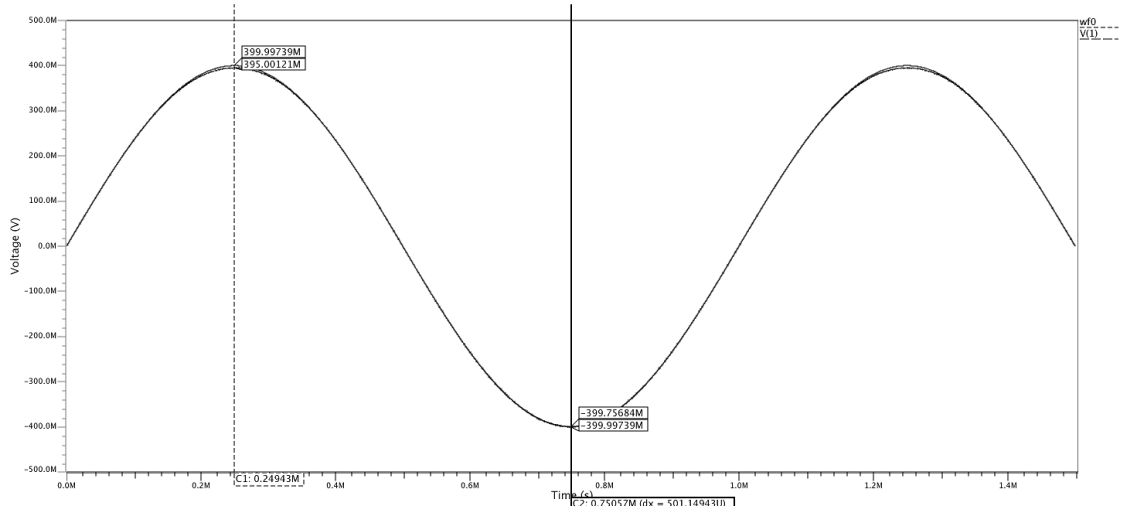


Figure 3.7. The post-layout transient response of two cascading choppers.

3.3.2. The Two-Stage Amplifier

In amplifier design, the usual criterion is large gain. Since the bandwidth in this case is very small, it helps in terms of gain bandwidth trade-off. The required bandwidth is 500 Hz and the desired gain we are looking for is at least 500 to 1000 V/V. If there were no power consumption restraints, this would be very easy to obtain because a simple multi stage amplifier usually has around 10^5 or higher open-loop gain, which then may be adjusted by a feedback loop. Nonetheless, the main idea in this thesis will be obtain a large closed loop gain, while dissipating very low power and having a large output swing.

For the first stage, folded cascode OTA was chosen to obtain a large enough DC gain. The input drivers biased close to weak inversion to have larger g_m without much power consumption. Thus, the bias current chosen as 2 μA (1 μA for each driver), which affects the noise and the gain directly. The device sizing was made according to this current and reasonable overdrive voltages except for the input drivers. They have 0.1 V as overdrive voltage.

For the second stage, the chosen topology is a simple class-A output stage, with lower gain but very large output swing. The gain was sacrificed in this stage. Since the operation do not rely on any speed considerations or step response, it is not required the circuit to have a very large DC gain. The DC gain must be high enough not to have large gain errors in the feedback configuration and amplifier must match the gain bandwidth product (GBW) specification. On the other hand, the output swing is an issue. Even though the input signal for the amplifier is very small, the targeted output for 1000 V/V gain will be close to supply limits (for max. beads 0.8mV x 1000 = 0.8 V). Thus, the output range must be large enough to accommodate these values and note that, it will already be limited by the common mode feedback circuit (CMFB), due to fully-differential configuration. Half the current of the first stage has been selected for biasing this stage.

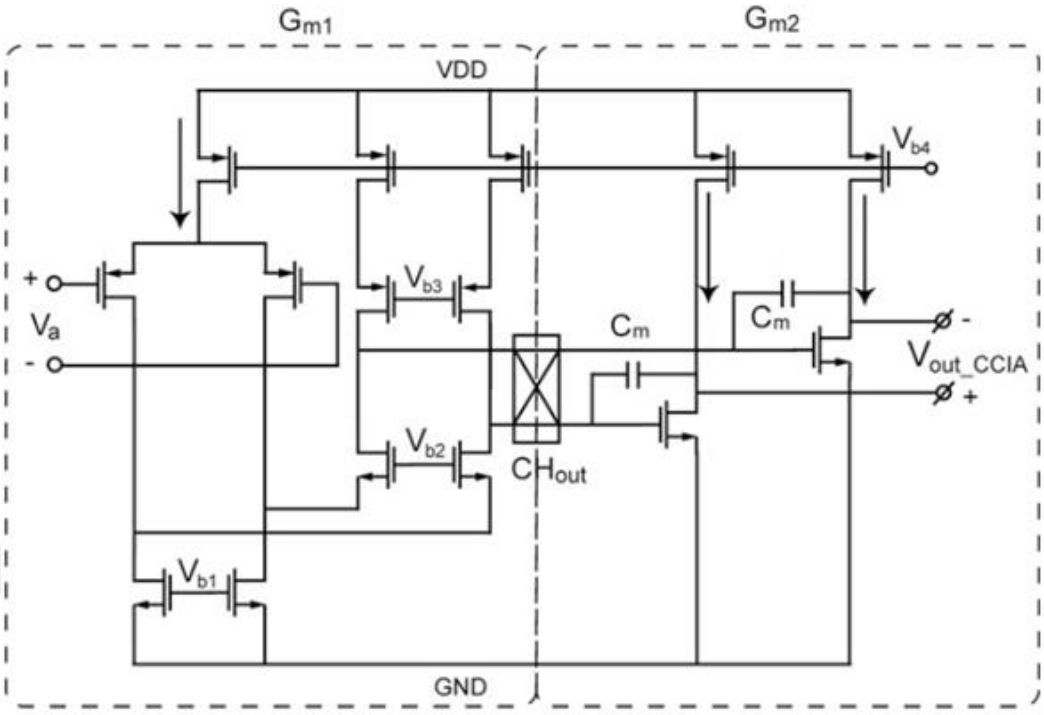


Figure 3.8. The Schematic of the two-stage Miller compensated chopper amplifier

The fully-differential configuration offers many advantages for designers, such as, increased common mode rejection, noise immunity, larger output swing and reduced even-order harmonic distortions. However, it also has a problem with common mode voltage level of the output. So, this common mode voltage has to be set by adding a common mode feedback circuit. This circuit basically takes the signal and compares it with a reference voltage (which is the desired CM level) and sets the level by feedback. The chosen circuitry for this purpose is a differential difference amplifier (DDA) topology, which is quite popular CMFB circuit. Since it does not have large passive noisy components like resistors, or power-hungry components like voltage buffers. It limits the output swing by two overdrive voltages, but this is also not a big issue since we already have smaller output levels than *Vdd* and *Vss*, also a very large swing, because of the fully differential configuration and the simple topology of G_{m2} stage.

3.3.3. Frequency Compensation

Frequency compensation is very important to have a stable interface circuit. The main function of C_{in} is to remove the DC component and isolate the input common mode voltage, thus theoretically any selection will be okay. However, in practice, there are some limitations. The first one is die area; it should be as small as possible to save area. Second, it determines the input referred noise time constant; it should be small for fast settling time and large for noise considerations. Moreover, the input impedance of the amplifier is determined by switched capacitance resistance with f_{chop}, so it should be small. As a reasonable trade-off C_{in} values are selected as 4.5 pF, which is an applicable value for integrated circuits.

For a stable system it is vital to select proper Miller compensation capacitances. The dominant pole, which is the closest pole to the origin is given by following expression.

$$f_d = \frac{1}{2\pi g m_2 R_1 R_2 C_m} \tag{3.2}$$

R_1 and R_2 are the output resistance of the amplifier stages. In the beginning the miller capacitance values were taken as 1 pF and the results were checked by using analytical calculations and by simulation results, then trimmed to 6 pF and continued with that. Substitution of the relevant values into Equation 3.2 yields a dominant pole of approximately 1.5 kHz. The non-dominant pole can be calculated from Equation 3.3.

$$f_{nd} = \frac{g m_2}{2\pi C_L} \tag{3.3}$$

For this expression, it is necessary to select a load capacitance as well. Since the load has not been designed yet, an exact capacitance value is not known. Still the calculations

were made by using different possible values. For worst case scenario, 3 pF was chosen, which is considerably large. That will lead the non-dominant pole position as 6.5 kHz. This is a problem, since those two poles are not very far away from each other. The zero position is calculated by,

$$f_z = \frac{gm_2}{2\pi C_m} = 265\ kHz \tag{3.4}$$

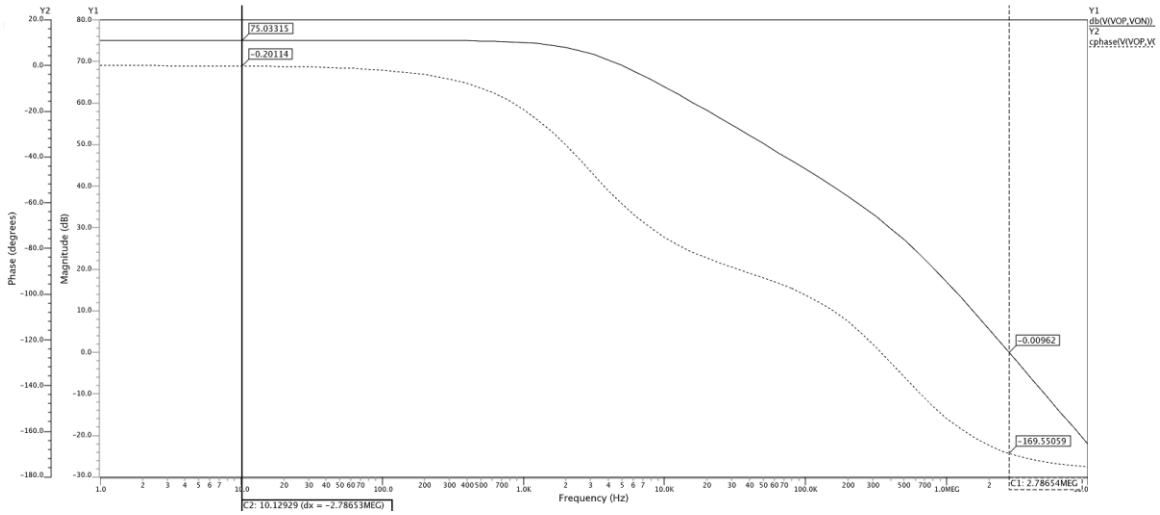


Figure 3.9.The open-loop AC response without compensation

The open-loop frequency response of the circuit without any compensation has a phase margin approximately zero, which is not acceptable. When Miller capacitances were added, phase margin becomes 64 degrees. The phase margin ideal range for stability and its expression is given in Equation 3.5.

$$Phase\ Margin = \tan^{-1}\left(\frac{f_{nd}}{f_{cl}}\right) = 180° - phase(@0dB) \tag{3.5}$$

$$2 \leq \frac{f_{nd}}{f_{cl}} \leq 4 \quad , \quad 63° \leq PM \leq 76° \tag{3.6}$$

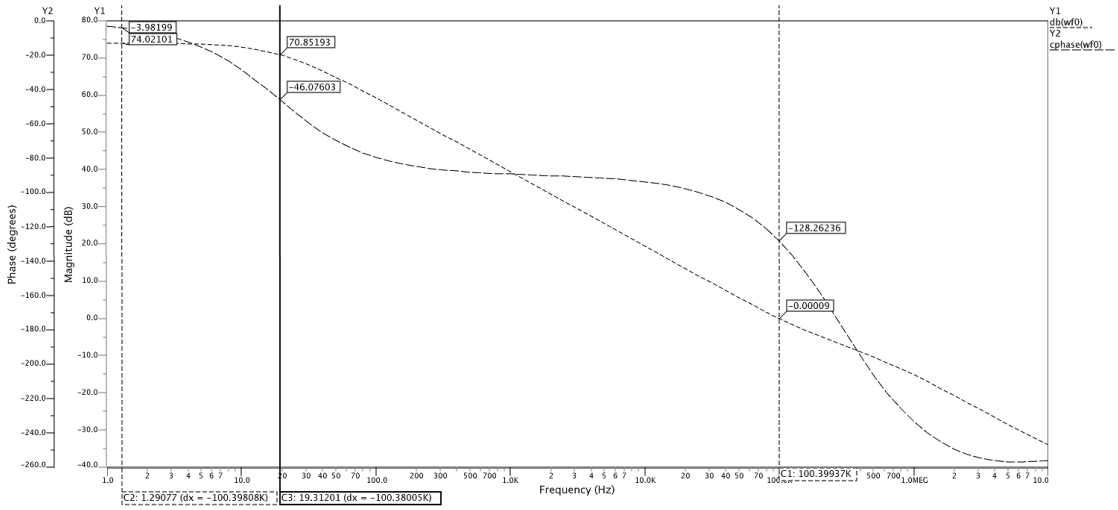


Figure 3.10. The open-loop AC response with compensation (Post-layout).

3.3.4. The Extra Gain Stage (Gm3)

Same structure (folded cascode) with Gm1 has been used with additional capacitive feedback and the total gain of the AFE has been distributed among the amplifiers to prevent capacitive mismatch in the feedback loop. Since this is just an extra single gain stage, the process is simple, no compensation is required, the system has 69dB gain and 90 degrees phase margin. For noise considerations, the third stage input referred noise will be reflected reduced by the gain of the preceding stages, so it is not very important. The simulation results are given below.

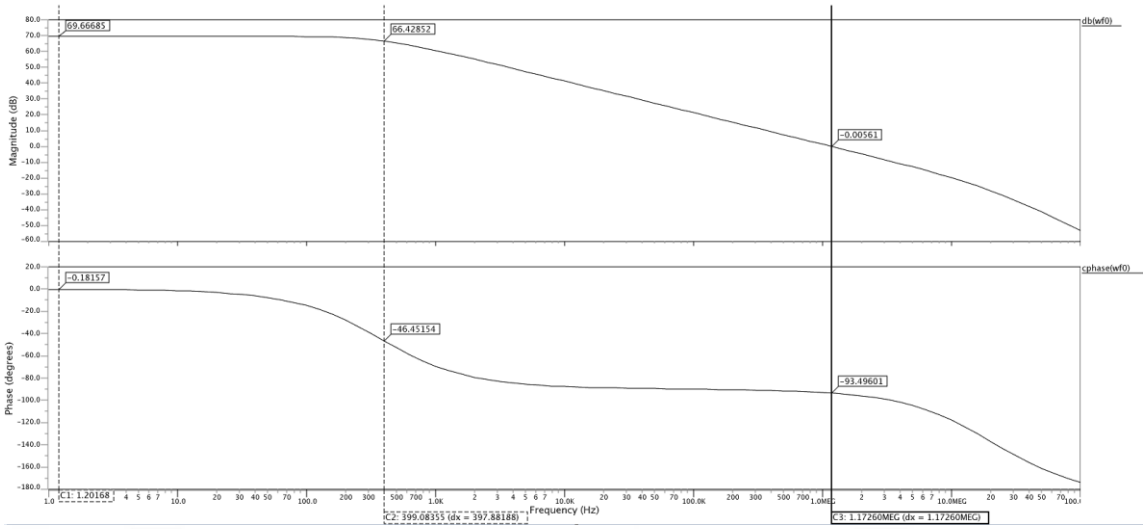


Figure 3.11. The pre-layout AC response of the gain stage

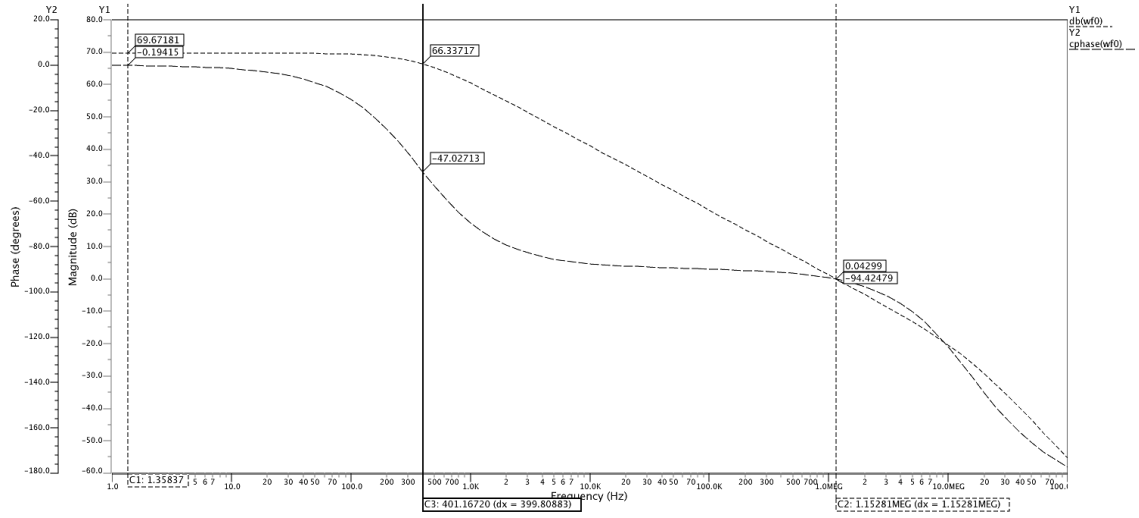


Figure 3.12. The post-layout AC response of the gain stage

3.4. Simulation Results

The simulation results for the discussed circuitry are given in following figures.

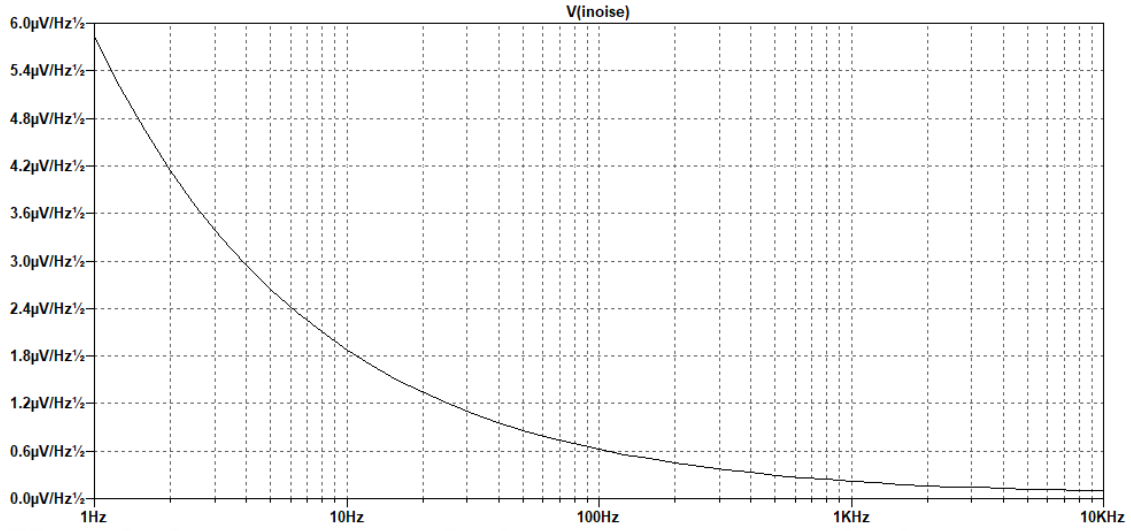


Figure 3.13. The input noise of Gm1 (0.3 µV/sqrt(Hz))

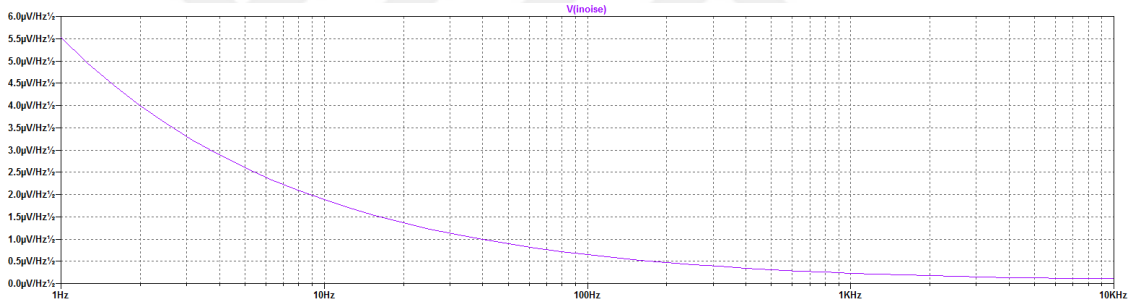


Figure 3.14. The input noise of the system (345nV/sqrt(Hz))

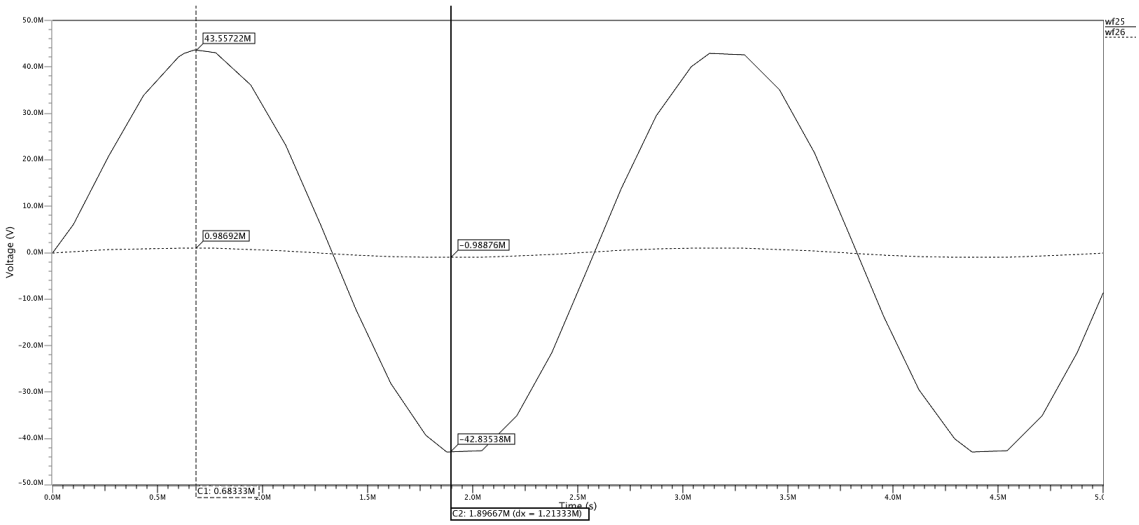


Figure 3.15. Transient analysis of the output of CCIA for 1mV sine input signal

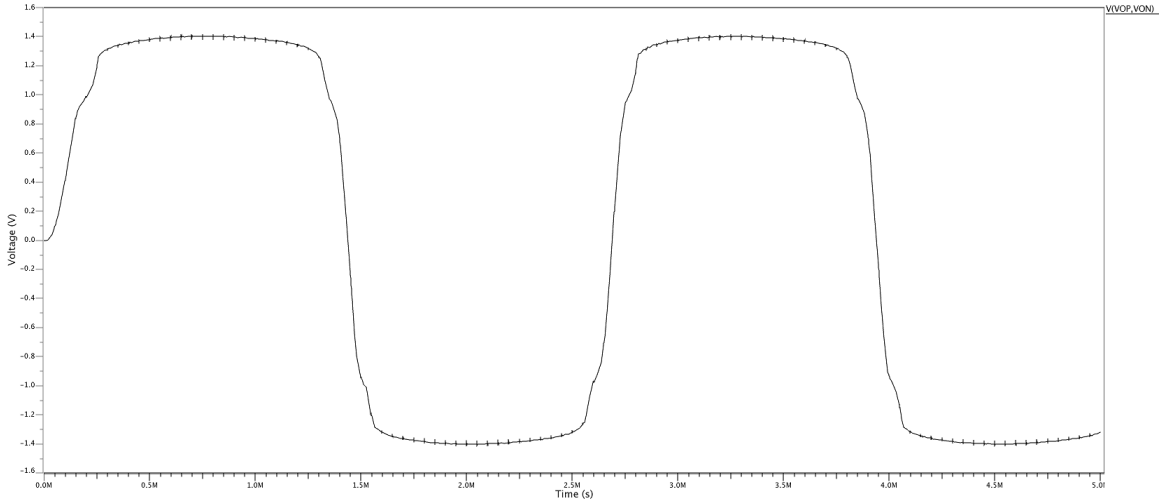


Figure 3.16. The output range of the circuit

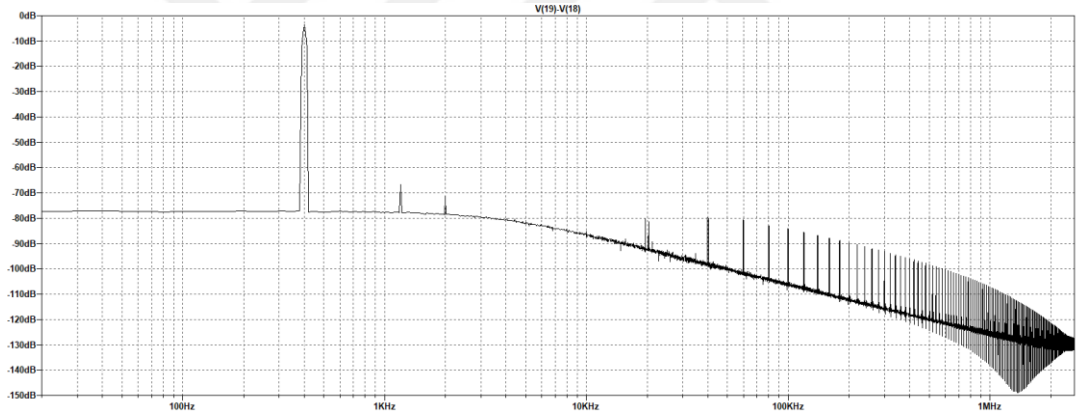


Figure 3.17. AFE FFT simulation

3.5. Summary

In this chapter the design steps and simulation results of the analog front end have been discussed. The given design matches the specifications in the end, with stable characteristics. However, it is vital to design a proper layout for this circuitry. Special care must be taken for the symmetry of the chopper layout. The summary of the designed analog front end is given in Table 3.1.

Table 3.1. The circuit parameters of the Analog Front End.

Input Impedance	150 MΩ
Output Range	1.25 to -1.25
Input Referred Noise density	345 nV/sqrt(Hz)
Open-loop gain (CCIA)	74.6 dB
Open-loop gain (Gain Amp)	69dB
Closed-loop gain (Total)	60 dB (1000 V/V)
Power Consumption	16.2 μW
Supply Voltages	0.9 to -0.9
Bias Current	1 μA
Phase Margin (CCIA)	64°
Gain Error (CCIA)	0.89 %

4. ANALOG TO DIGITAL CONVERTER (ADC)

Analog to digital converters are usually the final step of data acquisition systems. They convert real time analog signals to the digital code, which can be manipulated by computer software and systems. A simple data acquisition process is shown in Figure 4.1.

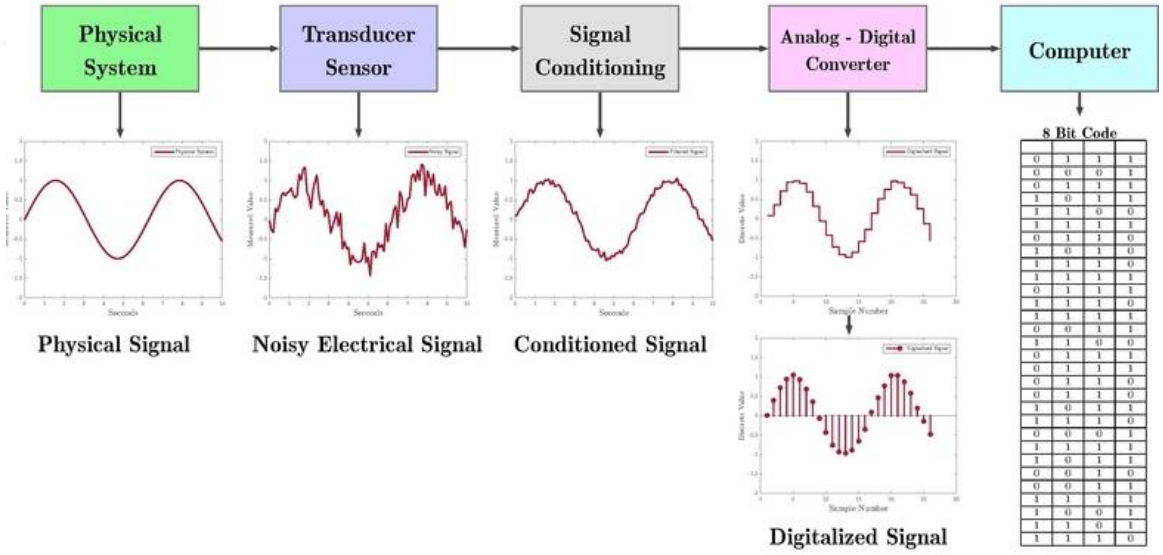


Figure 4.1. A simple data acquisition process.

There are four basic specifications to check when it comes to design a proper ADC. The first is the SNR limitation; this is very important to target a resolution for the application. The LSB voltage level must be higher than the input noise level of the ADC, which means that the number of bits must be set properly, or the last extra bits will give irrelevant information. So, the effective number of bits (ENOB) will be determined by this limitation. The formulation for ENOB is given below.

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{4.1}$$

In this equation, the tricky part is that it is not possible to know the exact SNR of the ADC input before designing it. Nevertheless, the output noise of the system that feeds the ADC gives an idea and with a margin of 10% of the input noise will be a good target to achieve for the design. SNR value for the circuitry that feeds the ADC is 59 dB, after the margin it becomes 53 dB.

$$ENOB = \frac{53 - 1.76}{6.02} = 8.51\ bits \tag{4.2}$$

8 bits resolution is enough for the application. In a bio-sensor interface application, the requirement is only to control a presence of some bio-molecules and 8-bits is more than enough for this purpose, thus there is no need to push the resolution specification higher.

Another specification for the ADC design is sampling frequency. The Nyquist criterion states that sampling rate f_s must be higher than two times the signal frequency.

$$fs > 2 \times f_{signal} \tag{4.3}$$

In this application, with 8-bits conversion resolution the sampling frequency is taken as.

$$f_s = 2^8 \times f_{signal} \tag{4.4}$$

$$f_s = 25.6\ kHz \tag{4.5}$$

The number of cycles is also an issue, for 8-bit conversion there must be 8 cycles, one for each bit, one cycle for sampling the input and in this case, an additional one for autozeroing and resetting the system. That last cycle depends on the designer's choice, since

this design aims for a low-noise application, an extra cycle for autozeroing is not much of a sacrifice to make. So, the conversion period and each cycle period will be given in following expressions.

$$t_{conv} = \frac{1}{f_s} \cong 40\ \mu s \tag{4.6}$$

$$t_{cycle} = \frac{t_{conv}}{10} \cong 4\ \mu s \tag{4.7}$$

To achieve this cycle period, the master clock must be set properly, the master clock frequency is given below.

$$f_{clk} = \frac{1}{t_{cycle}} = 256\ kHz \tag{4.8}$$

There are several ADC architectures, it is important to choose the right architecture which fits the best to design parameters. Each has their own advantages and disadvantages, so it is key to choose the specific architecture that matches better with the thesis specs. Without giving too much detail in the theory, those advantages and the selection process will be briefly explained in the next subsection.

4.1. Architecture Selection

Although there are many ADC architectures, three are used most commonly: The delta-sigma ADC, the successive approximation (SAR) ADC, and the pipeline ADC. The delta sigma ADC oversamples the signal by a large ratio and filters the signal band. Having an internal LPF is an advantage, plus it is very accurate in quasi DC frequencies and it has a high-resolution potential, moreover it has a low cost which is good for fabrication. The

power consumption is controllable in this architecture, it allows a nice trade-off between sampling speed, resolution and power consumption [27]. The problem with delta-sigma converters is that they are only applicable with continuous time periodic signals. They also have a considerable latency problem which is not good for speed considerations.

Successive approximation ADC is another choice for some applications. It uses a sample and hold circuit to sample the input signal and then compares it cycle by cycle to a reference voltage level. SAR ADC has typically very small cycle latency and high accuracy. It is also very power efficient due to no OPAMP involvement and easy to design and implement in both discrete and continuous time signals. As drawbacks, it has low conversion rates (2-5 MHz) and lower resolution than delta-sigma.

Table 4.1. Three popular ADC structures comparison.

Topology	Conversion Rate	Resolution	Comment
SAR	≤4 Msps ≤1.25 Msps	≤16-bit ≤18-bit	Low Cost Low Power Simple operation
Delta-Sigma	≤4 ksps ≤4 Msps ≤10 Msps	≤31-bit ≤24-bit ≤16-bit	Moderate cost Moderate power
Pipeline	≤200 Msps ≤250 Msps ≤550 Msps	≤16-bit ≤14-bit ≤12-bit	Fast Expensive Power Hungry

The pipeline ADC is the last choice, this one has a more specific working range which is very high-speed applications like video sampling. It is power hungry, considerably complex to design, has low resolution values and delay. It is not necessary to dive into more details about this one because it has almost the completely opposite characteristics to the specifications in this work.

It is obvious that the best choice for this project is SAR ADC, due to its very good power efficiency and simplicity. Since speed is not a concern with a 400 Hz analog input signal and low resolution is not a problem for a sensor interface application, the purpose is not to convert complex signals that carry sensitive information like audio or video. Those facts give the designer the chance to benefit from the advantages and avoid the disadvantages of the SAR ADC.

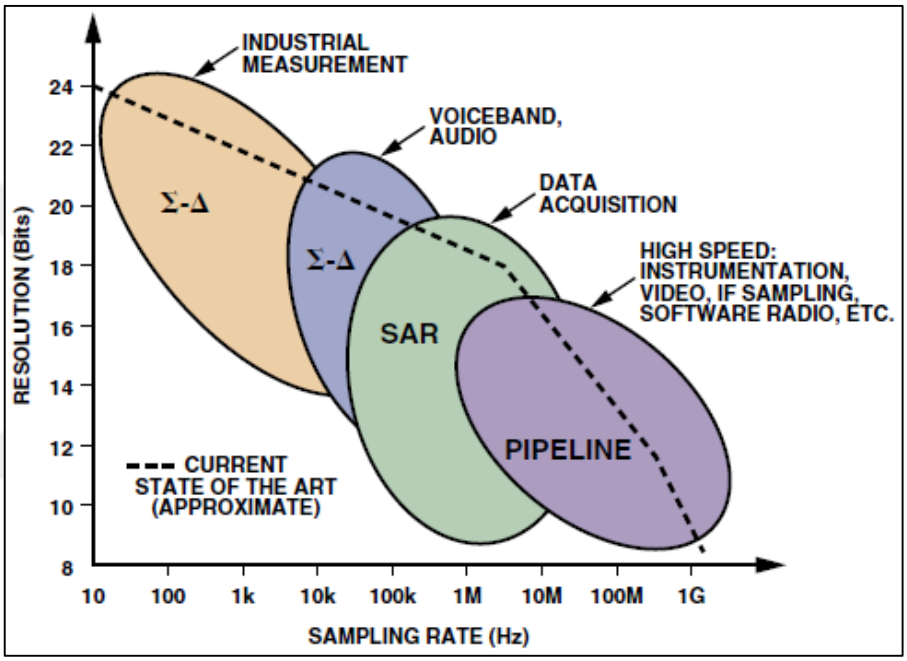


Figure 4.2. ADC architectures with applications, resolution versus sampling rates. [28]

4.2. The Successive Approximation Register ADC

SAR converter takes a snapshot for each signal level at that time frame, by using a sample and hold circuitry. So, it has a very small latency and it is applicable with both continuous and discrete time signals. It has a very precise control over the sampling time, which gives the opportunity to synchronize it with an external event. The conversion process is performed in two main steps, the sampling (acquisition) and conversion phase.

During the sampling phase, the sample-and-hold (S&H) switches connect the input signal with some capacitors. The conversion phase starts immediately after sampling occurs, the switches disconnect the signal path and the comparator compares the capacitor voltage with the DAC output value. Through the control of the SAR logic over the capacitor switches, the comparison goes on until the LSB is set and the digital code is obtained. A very common structure for the SAR ADC and an example of 4-bit conversion are given below.

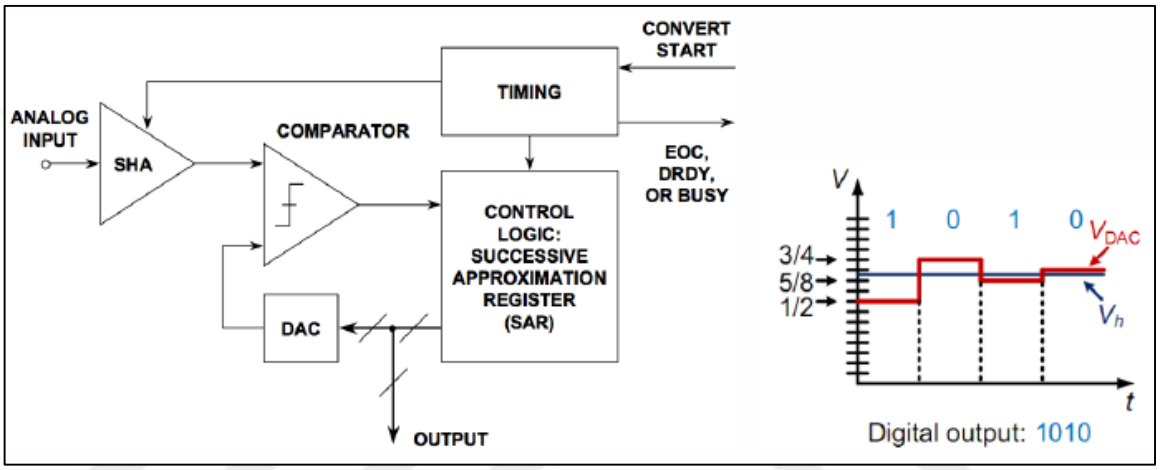


Figure 4.3. A simple SAR ADC structure and a 4-bit analog-to-digital conversion [28]

Although, it would be nice to have a simple topology with high power efficiency, noise is also another consideration for this design. Thus, like the remaining of the circuitry, a fully differential topology has been applied, which is very beneficial to obtain a better CMR, twice the dynamic range (important for comparator design) and immunity to common-mode noise. Furthermore, two different capacitive arrays for S&H and DAC cause additional problems by adding parasitic capacitances, layout difficulties and power dissipation. A simple solution for these is to use a single capacitive array for both purposes and use switching with proper timings. To understand how it works, a simple 3-bit SAR ADC is given in Figure 4.4 with further explaining.

During the sampling phase, the bottom plates of the capacitors are connected to the input signal, while the top plates are connected to V_{cm}. Then, the reset switch that connects

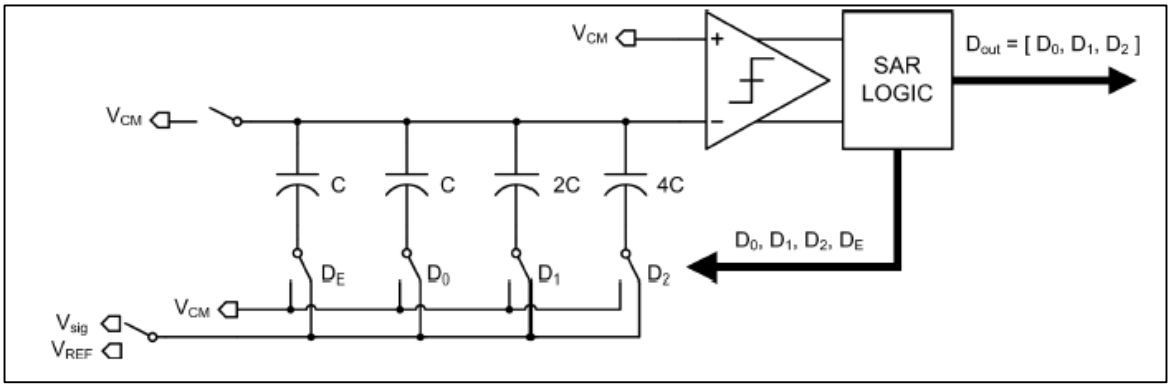


Figure 4.4. 3-bit single-ended SAR ADC

both top plates and comparator input to V_{cm} is opened and the bottom plates are connected to V_{cm}, this simple operation is called as "bottom plate sampling" and V_{cm}-V_{sig} is now stored on the top plates and connected to the comparator input. The MSB switch (D2) then is connected to V_{ref} and the first conversion is realized. The SAR logic either leaves this switch at V_{ref} or connects it back to V_{cm} depending on the comparator output. The same process happens until the conversion ends. Then, the digital code is sent to the register and all the switches are reset for another cycle. It is important that an additional LSB capacitor is added to the end of the array which completes the total value of capacitive array equal to 8C, so that a proper division may be performed. The control of this extra cap is very easy because after the sampling phase, it is connected to the V_{cm} all along. Next, the fully differential structure will be explained progressively along the switches.

In the fully differential version, a similar operation happens with two main differences. There are two identical capacitive arrays connected to the inputs of the comparator and there are two different reference voltages. Moreover, there is another bit added to the output with no extra capacitor in the array (D3), this is the sign bit of the system which is now also the MSB. It is not a surprise that the sign bit is the most significant one because it completely affects the evaluation of the data. After the sampling phase comparator starts the conversion before any V_{ref} connections and determines which input is higher. If V_{ip} is higher, then the sign bit is determined as 1, otherwise it is 0. Depending on this sign bit decision, the proper

reference voltages are connected to the branches, then other bits are determined by the same binary search algorithm as single-ended version as explained in preceding paragraph.

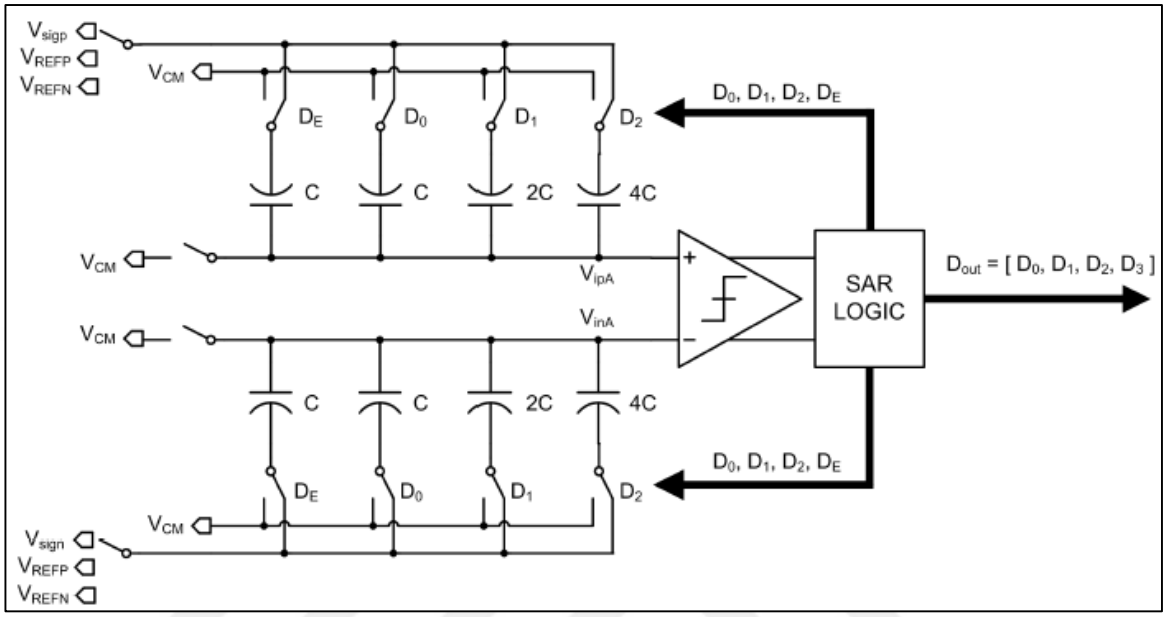


Figure 4.5. 4-bit fully differential SAR ADC

There are four main blocks to design in the SAR ADC, which are the capacitive array, the switches, the comparator and the SAR control logic. Each will be discussed in next sections to explain the details of design steps for each block.

4.2.1. The Capacitive Array

The same capacitor array is shared for both S&H and DAC circuitry. Since the S&H is more flexible to design, the main interest will be the DAC specifications. An array of binary weighed capacitors is a popular choice for DAC [29]. After sampling the input signal to the bottom plates of the array, they are either connected to the V_{ref} or V_{cm} to obtain a DAC output by voltage division.

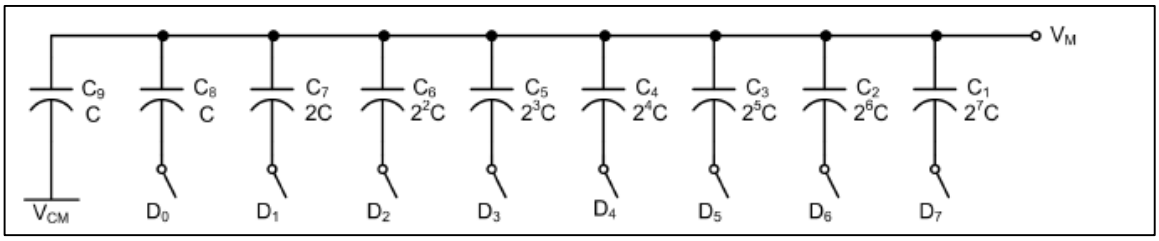


Figure 4.6. Binary weighed capacitor array.

V_M may be found by the given expression, m is the number of capacitors connected to V_{ref}, n is the binary multiplier of the last capacitor.

$$V_M = V_{cm} + \left(V_{ref} - V_{cm}\right)\left(\frac{m}{2^{n+1}}\right) \tag{4.9}$$

This array may seem very useful and easy to implement but it has a major drawback. As the resolution gets higher, the MSB cap will be unreasonably large, which results in more dynamic power consumption, parasitic capacitance effect, and capacitor mismatch. One simple solution to prevent these is splitting the array. However, in this design, the resolution is only 8-bits and one bit is already the sign bit which does not need an additional capacitor. Thus, there will be only seven binary weighed capacitors which means that the capacitor is 2^6 times the unit capacitor. Hence, it is not necessary to split the array.

All capacitors in the array are built as multiples of a unit capacitor. The selection of the unit capacitor is driven by two main limitations. One comes from the technology limitation and the other comes from the thermal noise determined by the capacitors. It is also important to keep the unit capacitor as small as possible to reduce the power dissipation. In technological limitation, there is nothing to do, in the thermal noise limitation, the kT/C noise SNR must be larger than the ADC signal-to-quantization-noise ratio (SQNR). Equation 4.12 must be satisfied in terms of kT/C limitation.

$$SNR_{th} = 10 \log \frac{\frac{FS^2}{2}}{\frac{4kT}{C}} \tag{4.10}$$

$$SQNR_{ADC} = 6.02n + 1.76 \tag{4.11}$$

$$SNR_{th} > SQNR_{ADC} \tag{4.12}$$

When Equation 4.10 and 4.11 are subtituted in Equation 4.12, it becomes,

$$C \geq 0.6\, fF \tag{4.13}$$

That means kT/C noise is not a limitation for this design because any chosen capacitor value will be already higher than 0.6 fF. Aside from this one and the technology limits (in UMC 180nm technology, the unit limits for a metal-insulator-metal capacitor is 2 fF [30]), the sampling leakage is also a concern due to low speed operation. Consequently, a capacitor value of 20 fF has been selected for the unit capacitor. The capacitive array layout and the layout plan is given in the following figure. Whole array occupies 130x110 μm^2 area.

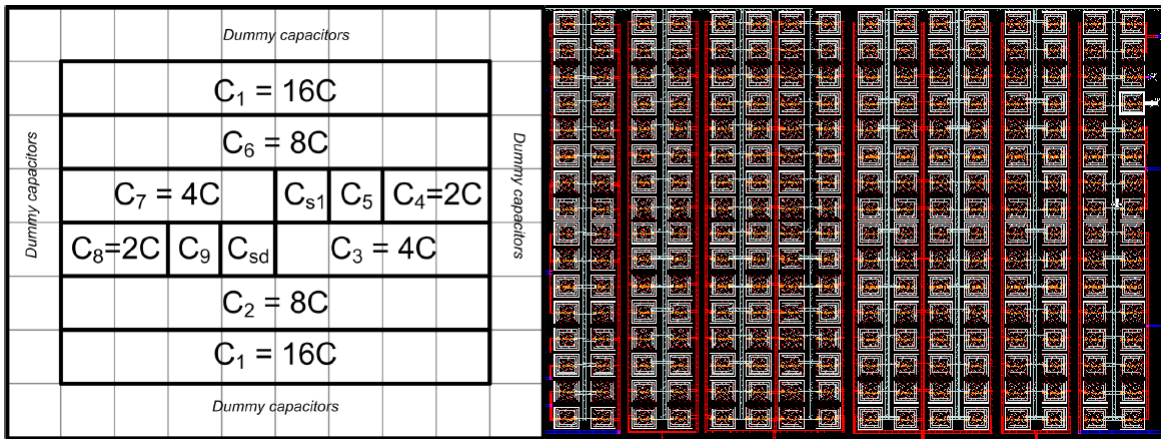


Figure 4.7. The floor plan and the capacitive array layout.

4.2.2. The Switches

Designing proper switches are vital for capacitive array applications for both resetting and relaying node voltages. Switched capacitor arrays are used for the S&H and DAC applications. The input signal and the reference voltages are applied to the bottom plate of the capacitors by complex switches on the other hand, the common-mode voltage V_{cm} is applied to the top plate of the capacitor by a simple NMOS switch. So, there are two groups in terms of switch designing process.

The bottom plate switches relay the input signal, common-mode voltage, or reference voltages to the bottom plates by the control of related clocks. The top plate switch for both branches resets the voltage at the inputs of the comparator by passing V_{cm}. Before the design steps, it is important to set those voltages.

$$-0.9\ V \leq V_{sig} \leq 0.9\ V \tag{4.14}$$

$$V_{cm} = 0\ V \tag{4.15}$$

$$V_{refp} = V_{cm} + V_{dd} = 0.9\ V \tag{4.16}$$

$$V_{refn} = V_{cm} - V_{dd} = -0.9\ V \tag{4.17}$$

Only NMOS transistors are used to implement switches that passes the V_{refn}, V_{cm} and only PMOS transistors are used for V_{refp}, due to reduction in the body effect. However, when it comes to pass the input signal, it might be close to 0.9 or -0.9 so the best solution is to use a CMOS transmission gate which includes both NMOS and PMOS switches with almost rail to rail dynamic range.

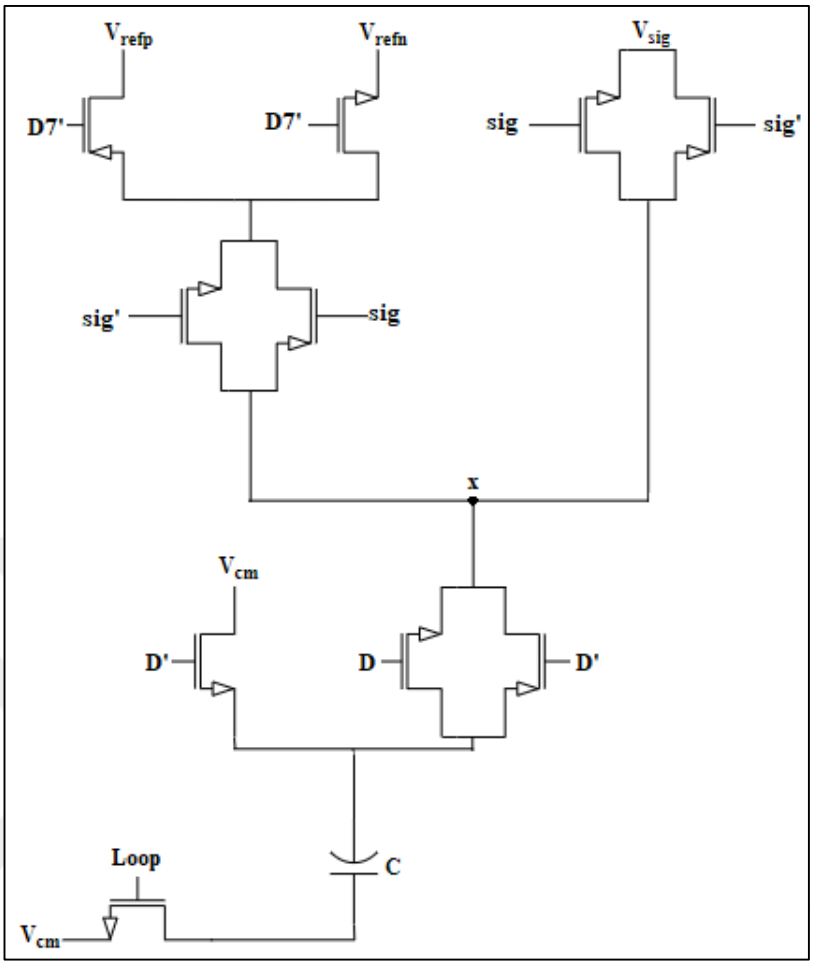


Figure 4.8. The switch structures.

Figure 4.8 illustrates the switch structure for the capacitive array. In this schematic, the point above node *x* is common for the entire branch, below node x, the bottom plate sampling operation takes place by two switches controlled by same digital signal. The signal *D*' comes from the SAR logic circuitry and it depends to the comparator result for each bit. Each bit controls the required capacitor connection. The top plate switch is a simple NMOS which is controlled by a clock named "Loop". The control clocks and the Loop clock will be discussed in next sections.

The sizing for these switches is limited by the speed requirements. Since the operation in this project is not a high-speed operation, it is a straight forward process to size these switches properly. The cycle takes place in 4 µs, due to speed requirements of the operations

the wise way to split this time is giving 3.3 µs to the pre-amp and 0.7 µs to the DAC+ latch. The settling time of 0.35 µs is preserved for the DAC and it is very easily obtainable with minimum size switches. Simulations show that the simple switching operation takes place in few nano-seconds range with minimum sized switches. The PMOS to NMOS sizing ratio should be kept around 2.25 due to the electron mobility ratio, and the series switches must be sized properly due to series resistances.

4.2.3. The Comparator

In the design steps of a SAR ADC, the most significant part is the comparator, because, it is the most power-hungry component of the ADC. It is also it is the point in the circuit that the binary search algorithm takes place. During the binary search phase, the comparator must decide which input node has the higher voltage and then it drives the SAR control logic, which provides the proper digital values for the DAC. The main specification for a comparator is that it must discriminate voltage levels as small as half of the LSB.

For an ideal case, a simple latch may perform this operation by itself. Nonetheless, this is not possible due to high offset voltage of the latch and large kickback noise. To prevent this problem, a simple solution is adding a pre-amplifier before the latch and use its gain to reduce the offset. Moreover, offset cancellation techniques are applicable with pre-amplifier structures and not with the latch. However, in this case the kickback noise is still a problem, but this time for the preamplifier inputs. Thus, the preamplifier is designed as a two-stage amplifier as shown in the Figure 4.9, the details about the kickback noise and additional gain stage will be discussed in the preamplifier design steps.

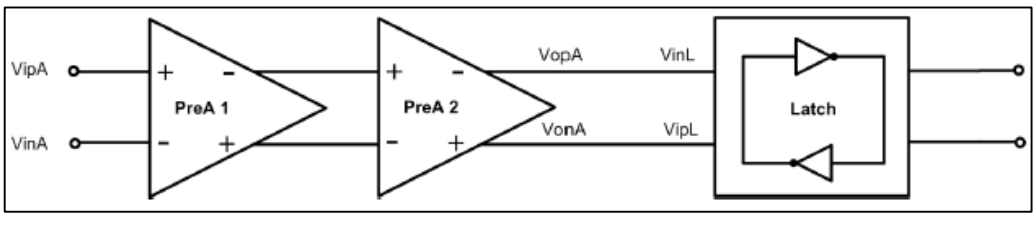


Figure 4.9. The structure of the comparator.

To be able to design the proper preamplifier, it is first necessary to design the latch that the preamplifier will drive. A dynamic latch with simple topology has been chosen to reduce the power consumption, the transistor level schematic is given below. When the control signal "*Lat*" is low, the reset phase is performed, and the output nodes are pulled to V_{DD}. The control signal is high when the regeneration phase is on, the circuit determines which input signal is higher in this phase, by the help of two cross-coupled inverters. The decision is therefore taken on the rising edge of the control signal "*Lat*".

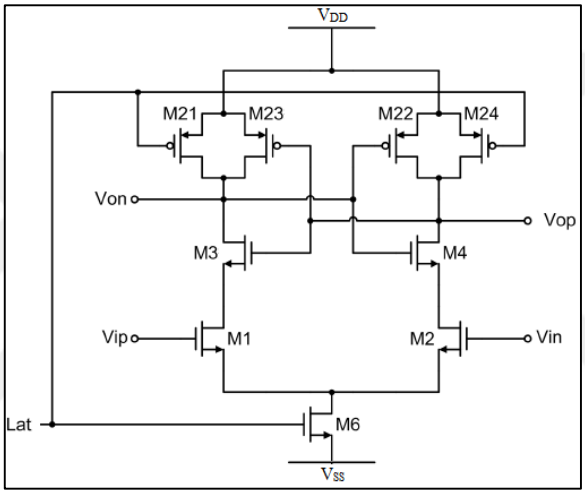


Figure 4.10. The dynamic latch.

Since a dynamic latch is selected, the power consumption is reduced. It consumes power only when it is triggered by the control signal; otherwise, during the reset phase there is no current flow. Besides the power efficiency, it also works quite fast, because the NMOS transistors M1 and M2 enter to the active region immediately after triggering. The reason behind this is that the source voltages of the M3 and M4 are equal to V_{DD}-V_T while the drain voltage of M6 is V_T below the latch input common mode voltage [31]. The latch post-layout transient response is given in Figure 4.11, to show the required time for the latch to respond.

Metastability is another issue in the art of designing comparators, so the digital circuitry shown in next figure is chosen as load of the dynamic latch to limit its influence. When the control signal is low (reset phase), the output logic keeps its outputs *Q* and *Q'* at

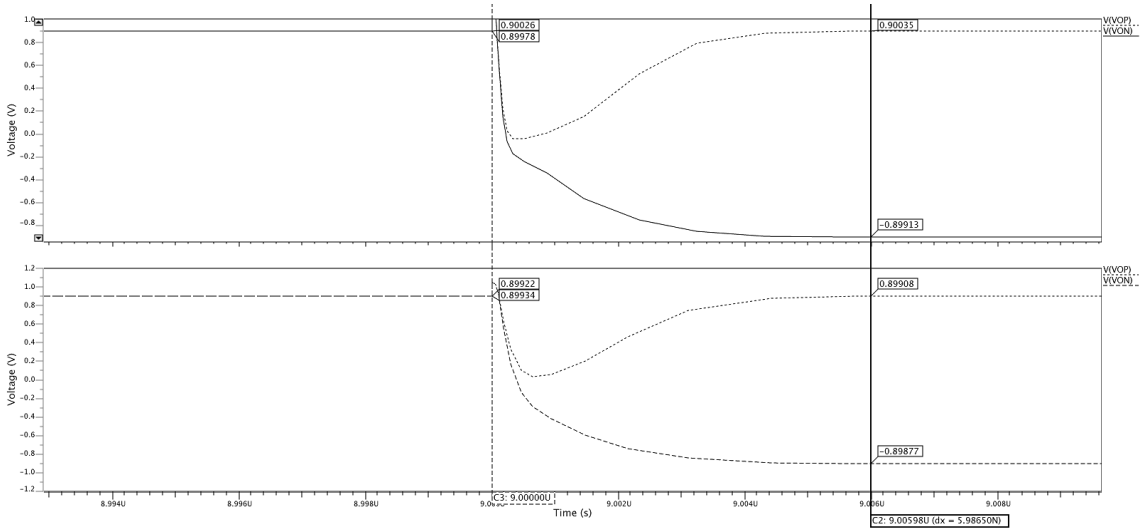


Figure 4.11. The transient response of the dynamic latch.

the same value, while during the regeneration phase it provides the output result taken from the latch. In case of metastability error occurrence, both output nodes of the latch remain close to V_{DD} and the metastability circuitry maintains the previous values. So, the metastability error limited in a range of ±1 LSB.

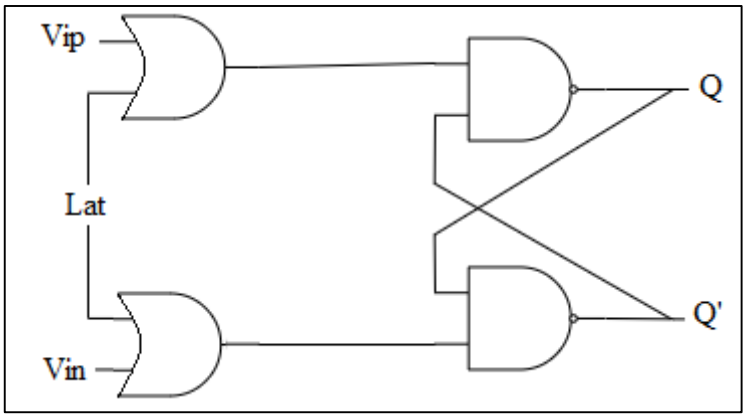


Figure 4.12. The metastability circuitry.

The designed dynamic latch will be the load of the preamplifier and the main purpose of adding the preamplifier to the latch is to reduce the errors due to offset of the latch. There are four main specifications for the design steps. The first is the gain specification; the total

gain of the preamplifier must be large enough to overcome the offset of the latch. The relation between them is given in Equation 4.18.

$$LSB > \frac{V_{off,Latch}}{A_v} \tag{4.18}$$

The second specification is the speed requirement; the time reserved for the preamplifier to settle is approximately 3.3 µs. The slew rate calculation will be performed for the latch input capacitance, which is just an approximation, but SPICE simulations will be more accurate. The simulation result shows that as expected, there is not a problem in terms of the speed specification. The output signal settles in under 20 ns even for a load of 10 fF, which is larger than the gate capacitance of the latch. The limitation and the result are so far apart from each other that it probably will not be a problem even after layout simulations.

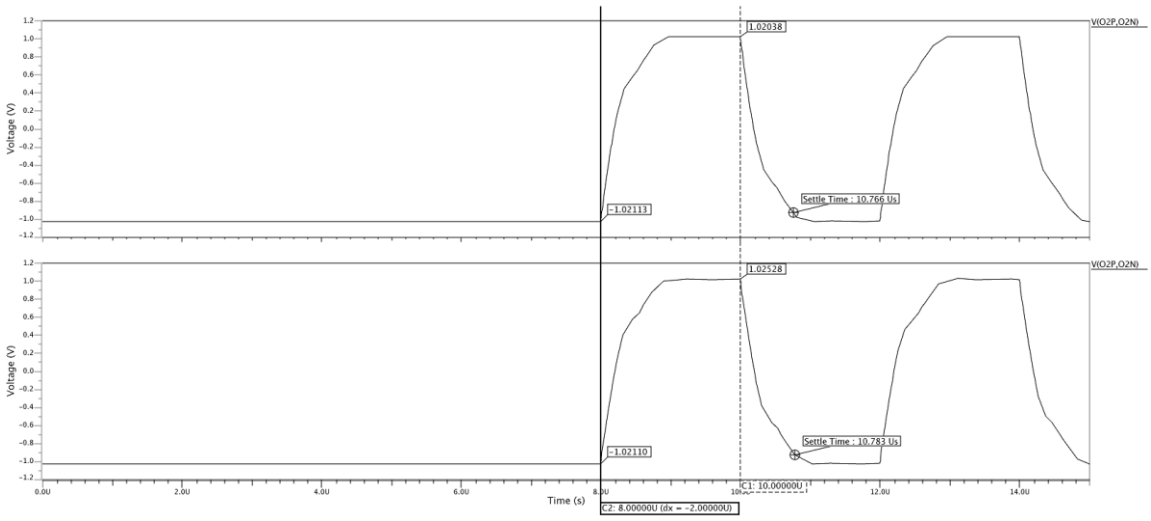


Figure 4.13. Preamplifier settling time (Pre-layout on top, post-layout at bottom).

The third specification is the power consumption, which is a main specification for the whole design as well. A general rule of thumb for SAR ADC design is reserving the half of

the power consumption for the preamplifier; therefore, the design considerations will be set for a preamplifier which is as power efficient as possible.

Finally, the last specification is the parasitic effect due to the input capacitances of the preamplifier. Since the gate-drain capacitance may affect the DAC performance, it is important to keep the first stage input transistors as small as possible.

The small unit capacitor selection in the capacitive array makes the DAC sensitive to the gate-drain parasitic capacitance of the input pair of the preamplifier. The charge redistribution may be affected due to the kickback noise. When the input signal is sampled on the top plate node of the array, this value will be amplified by the preamplifier immediately. Nevertheless, due to presence of the C_{gd} of the input pair, the large variations in the output node may affect the input node through this capacitance. This effect is called the "kickback noise" due to its behavior of kicking back from the amplified output to sensitive input nodes. It acts like a negative feedback path and affects the binary search process [32]. A very simple and useful solution for this is to use an additional gain stage with higher gain. Apart from the kickback noise issue, high gain at the first stage also makes the output voltage saturate and makes the ADC non-linear in some regions, which makes even more useful to set the first stage gain lower.

Since the gain requirement is lower for the first stage, it is just a differential NMOS pair with a diode-connected PMOS load. Another advantage of the additional stage is, now it is possible to use small-sized driver transistors in the input nodes which might be bad for gain considerations but very helpful to reduce the C_{gd} parasitic capacitance. To improve this solution even more, capacitive neutralization technique is applied to these nodes [32].

Since the problem is the output to input gate-drain overlap capacitance of input transistors, it is possible to add two dummy transistors which approximately brings an input capacitance close to C_{gd}. To achieve a good match in these capacitances, the dummy transistors should be sized with same channel length with the input transistors and half the

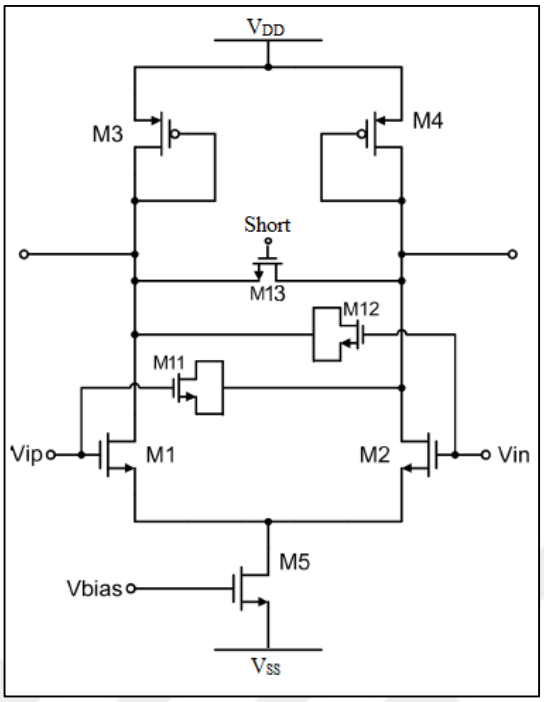


Figure 4.14. The preamplifier first stage.

channel width [32]. Therefore, the kickback noise through these overlap capacitances is reduced.

$$\left(\frac{W}{L}\right)_{dummy} = \frac{1}{2}\left(\frac{W}{L}\right)_{input} \tag{4.19}$$

The second stage design is easier compared to the first stage. The only specifications require attention are the power consumption and the gain. The power consumption is directly proportional to the tail current, which is selected as 1 µA for each branch. Selecting the tail current too low causes problems with gain and noise so that 1 µA is low enough for a low-power application and high enough to avoid such problems. Remember that the preamplifier is the most power-hungry part, so this is the place to save power for performance.

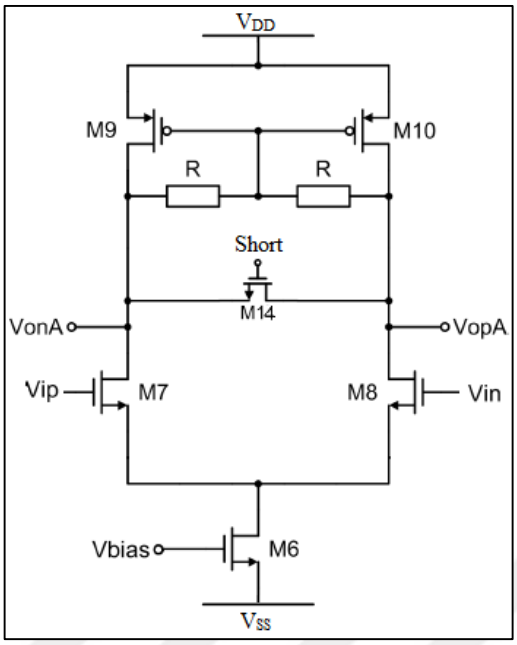


Figure 4.15. The preamplifier second stage.

The input transistors of both stages are designed to operate in weak-moderate inversion due to requirement to high driver transistor transconductances in a low power operation, while others are in strong inversion state. The gain relations are given below.

$$A_v = A_{v1}.A_{v2} \tag{4.20}$$

$$A_{v1} \approx \frac{gm_1}{gm_3} \tag{4.21}$$

$$A_{v2} \approx gm_7.R \tag{4.22}$$

The first stage gain and the total gain post layout simulation outputs are shown in the following AC sweep simulation results. As planned, the first stage gain is as low as 5 dB, which is approximately 1.8 V/V. The total gain for the preamplifier, on the other hand is 33dB. That means the second stage gain is 28 dB (45 V/V).

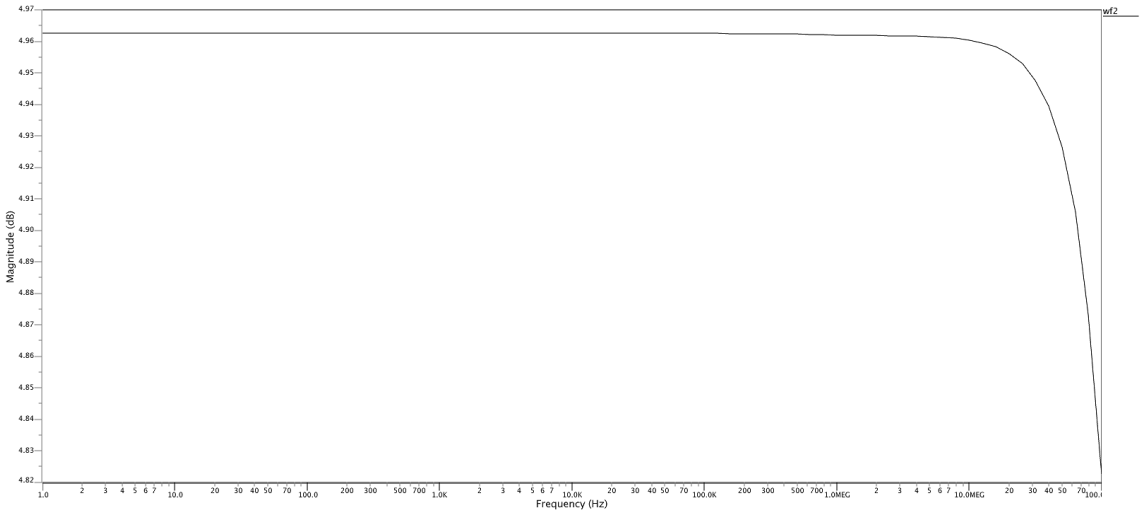


Figure 4.16. The first stage gain of the preamplifier.

Offset voltage of the comparator, which is signal independent, also causes an error in the decisions. Applying a simple offset reduction technique to the preamplifier is a solution for the issue, as mentioned unlike the latch, preamplifier is very suitable for to apply such techniques [33]. The input offset storage (IOS) technique is the one that is applied to the preamplifier. It is basically, operating the preamplifier in a unity-gain negative-feedback loop and storing the offset voltage of the preamplifier across the capacitors that connected into the input nodes. The offset cancellation calculation is given in Equation 4.23.

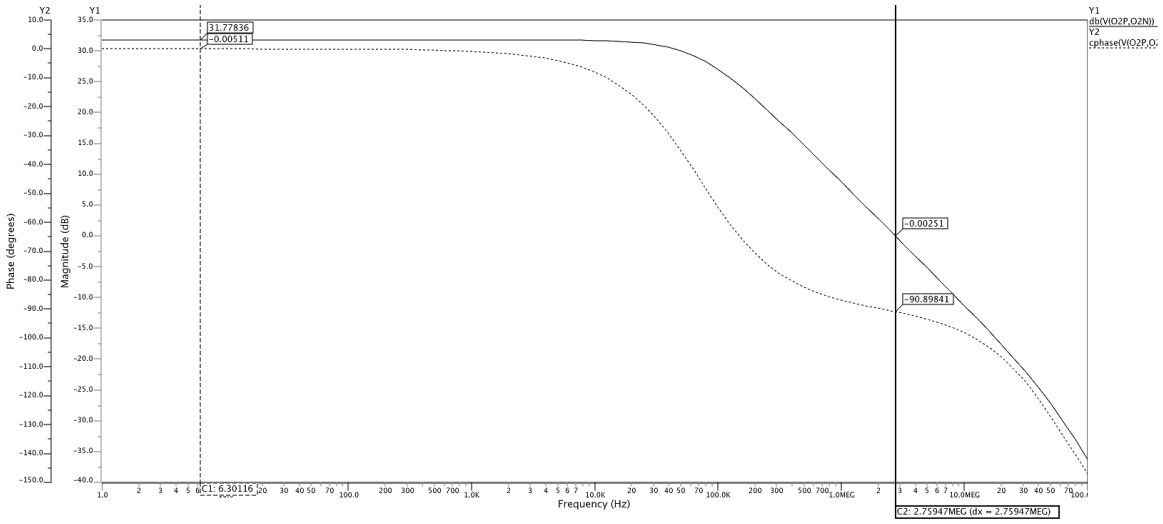


Figure 4.17. The total gain of the preamplifier.

$$V_{os} = \frac{V_{ospreamp}}{1 + A_v} + \frac{\Delta Q}{C} + \frac{V_{oslatch}}{A_v} \tag{4.23}$$

In Equation 4.23, the C value is the total input capacitance, ΔQ is the charge injection due to the loop switch mismatches. For a perfect offset cancellation, the capacitance and the preamplifier gain should be very large. As solution for large capacitance requirement, without even adding any capacitor to the circuit, the entire capacitive array may be used for this operation with proper switching. On the other hand, for the gain issue, the total preamplifier gain of the system is good enough for this application. In terms of power consumption, IOS is a very efficient technique which costs only a negligible switching power to the system.

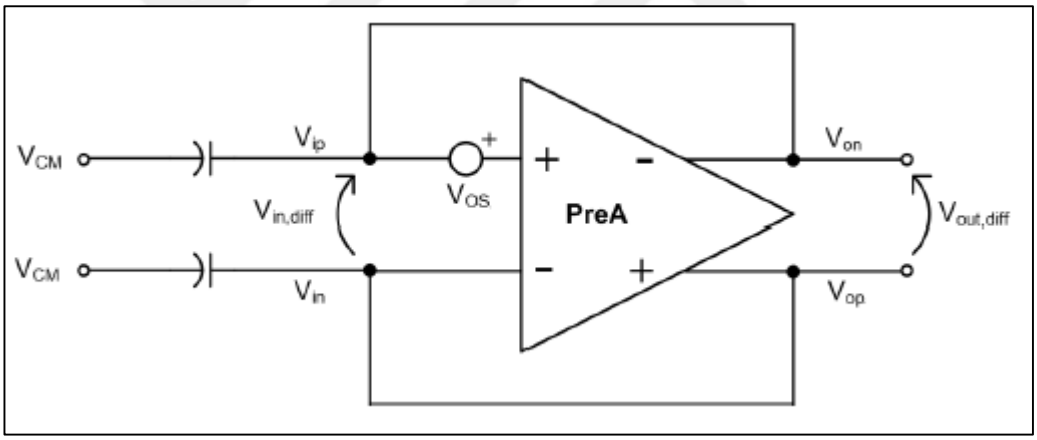


Figure 4.18. Closed-loop configuration of the preamplifier for input offset cancellation.

In order to explain the offset cancellation process, the closed-loop operation is shown in Figure 4.18. The entire capacitive array is shown as a single capacitance for each branch and offset voltage is added as an additional source. In this system, the preamp is in a negative feedback unity gain configuration. The following equations show the offset cancellation principle.

$$V_{outd} = V_{ind} \tag{4.24}$$

$$V_{outd} = (V_{ind} + V_{OS}).-A_v \tag{4.25}$$

Solving Equation 4.24 and 4.25 together, it becomes:

$$V_{outd} = V_{OS}.-\frac{A_v}{1+A_v} \tag{4.26}$$

When this output value is referred to the input:

$$V_{ind} = \frac{V_{outd}}{A_v} = -\frac{V_{OS}}{1+A_v} \tag{4.27}$$

Equation 4.27 shows that the input offset of the preamplifier is reduced by the DC gain A_v. So, the IOS technique reduced the preamplifier offset voltage significantly without adding any large passive components or power-hungry active circuitry.

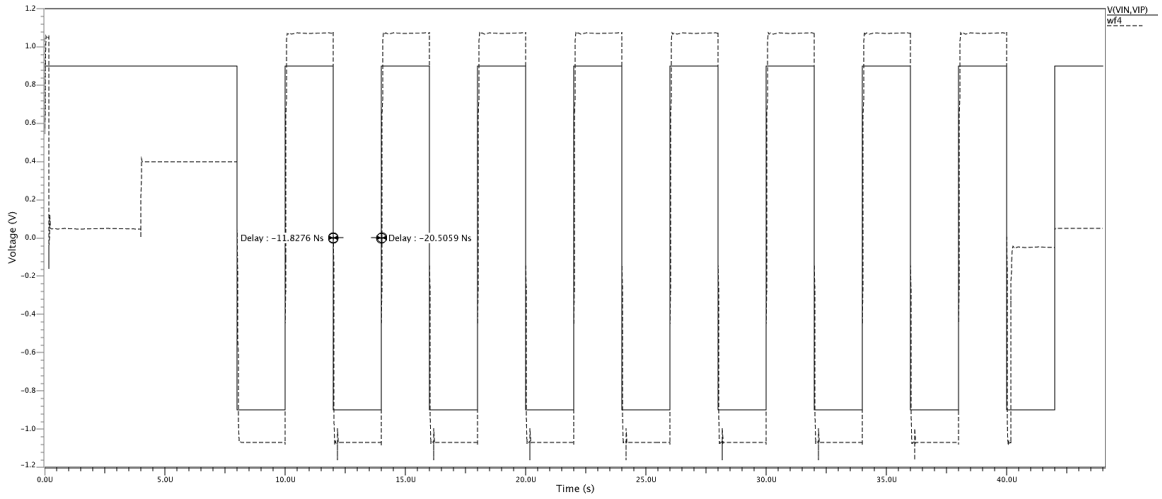


Figure 4.19. The comparator delay time post-layout simulation.

4.2.4. The SAR Control Logic

A control logic circuitry is essential for the SAR analog-to-digital converters, and it is the digital part of the operation. It is required in this design to control both the sample-and-hold operation and the DAC binary search algorithm. Once the latch makes its decision, the

result is stored in the register and the DAC digital input is updated accordingly to that decision. As a SAR control logic structure, the one proposed in [34] is used. In this circuit, two rows of set/reset D-flip-flops are used to generate the digital input of the DAC. The first-row flip-flops act as a shift register that shift a logic 1 while each flip-flop of the second row is first set to logic 1 and then eventually, they reset to logic 0, depending on the result of comparison coming from the latch.

To understand the SAR operation and the control logic, it is important to study the timing diagrams and the clocks. The conversion takes place in ten cycles, with 4 µs for each cycle. A delay factor of 0.18 µs is selected to trigger the required sub-blocks. The first cycle is reserved to reset the output voltages of the comparator stages by the control signal "*Short*".

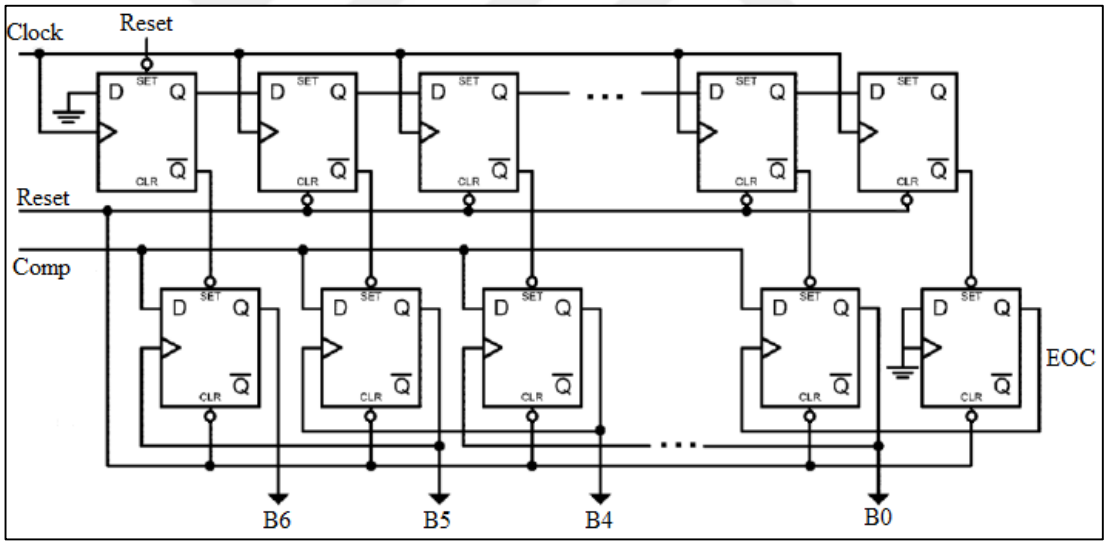


Figure 4.20. The SAR control logic structure.

The second cycle is the sampling cycle. The sample and hold operation happen in this cycle. The input signal is sampled on the bottom-plates of the capacitors since the control signals of "*Loop*" and "*Sign*" are both high. In this cycle, the preamplifier is operating in the closed loop configuration, so the offset cancellation is also taking place. It is vital to note that, "*Loop*" must go low just before the ending of the cycle to realize the bottom-plate sampling.

The remaining eight cycles are for the 8-bit conversion. In cycle three, all the bottom plates of the capacitor array are connected to the common-mode voltage V_{cm}, thus the sampled charge on the bottom plates is redistributed to the inputs of the comparator. The first comparison is executed right away since the closed-loop operation and offset cancellation have already ended and the MSB, which is also the sign bit, is determined at the beginning of the cycle four, when the latch is triggered.

The MSB is already set in the fourth cycle and the proper reference voltages (V_{refn} or V_{refp}) are connected to the array according to the sign bit. The V_{ref} to V_{CM} switching also occurs depending on the result of the last comparison, so the DAC input signal is set to its half range value. Hence, the cycles from four to ten are used to determine the remaining bits with same binary search principle. In the beginning of each cycle, the DAC provides a new voltage based on the previous bit decision, while the preamplifier amplifies the difference between the nodes, and the dynamic latch determines the comparison result when its triggered (when Latch control signal is high).

4.3. Summary

It is important to observe that the DAC input D_{IN} is equal to the digital output of the ADC while the first six bits are determined (from cycle four to cycle ten), but it is reset at the beginning of the new conversion period. Therefore, the value of the last bit of digital output is ready to be saved in a register during the cycle one of the new period, when the end-of-conversion (EOC) signal goes high. The result and summary of ADC is given below with comparator differential signals and bit outputs.

The Figure 4.22 shows clearly, the first two cycles spared for resetting the system and reducing the comparator offset, the sampling happens in the third cycle and the DAC starts to operate afterwards. The FFT of the ADC input also given below, which gives information about the noise characteristics and ENOB for the results, which is actually worse than expected due to layout problems. It is quite normal to have ENOB less than 8, due to 8-bit

resolution but it seems the total noise contribution of the system and the layout parasitics made the design suffer in SNR evaluation and the new ENOB is 7.2 as given in the table.

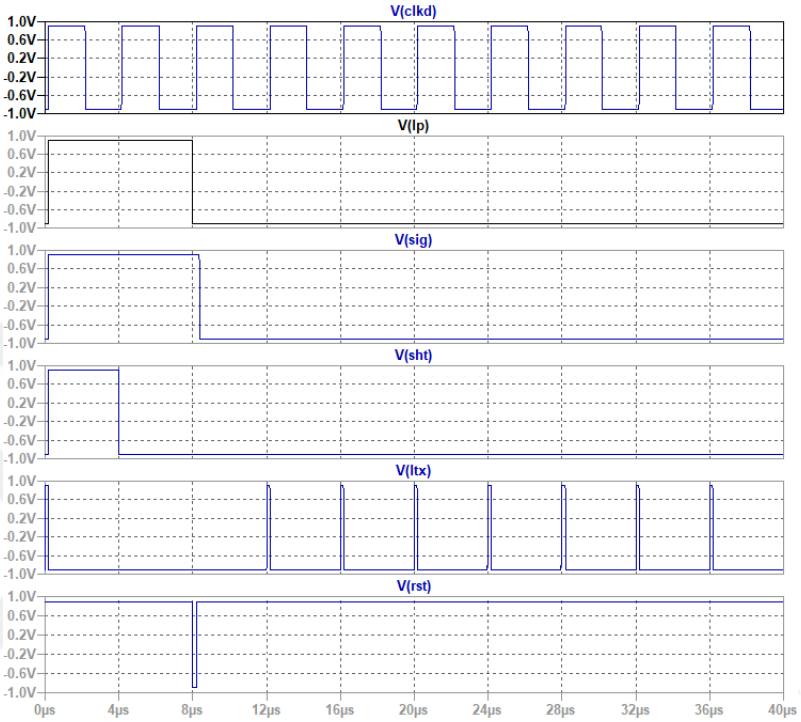


Figure 4.21. The timing diagram of the control signals for one conversion period (Top to bottom signal names: "*Clock*", "*Loop*", "*Sign*", "*Short*", "*Latch*", "*Reset*").

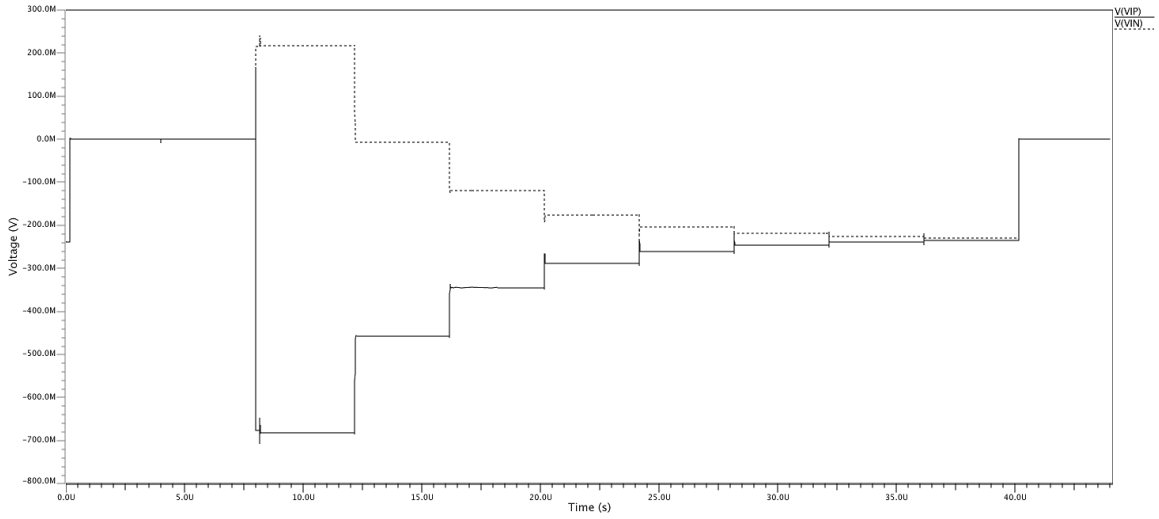


Figure 4.22. The 8-bit SAR ADC comparator inputs for rail-to-rail input voltage.

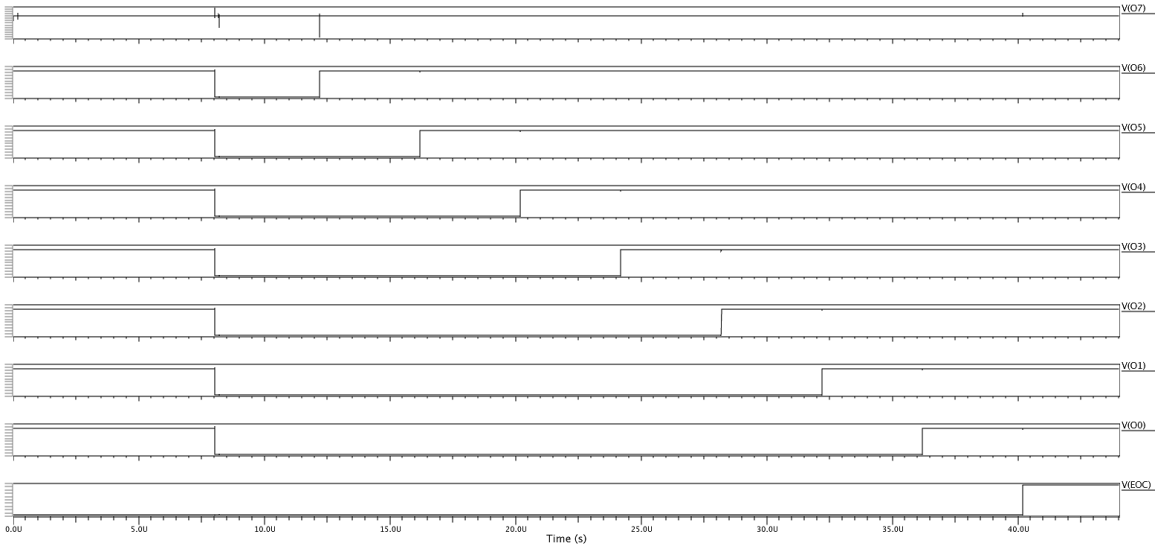


Figure 4.23. The bit outputs for 0.9 V differential input.

The ADC is sensitive enough to detect and response low level signals, even as low as 1 LSB. Since the application does not requires high precision data conversion, further performance evaluation on bit errors does not given. The sensor input varies between 0, 0.2, 0.4, 0.6 to maximum of 0.8 μV, that means the minimum converted voltage for the ADC to handle will be approximately 0.2 V peak, which is easy to handle.

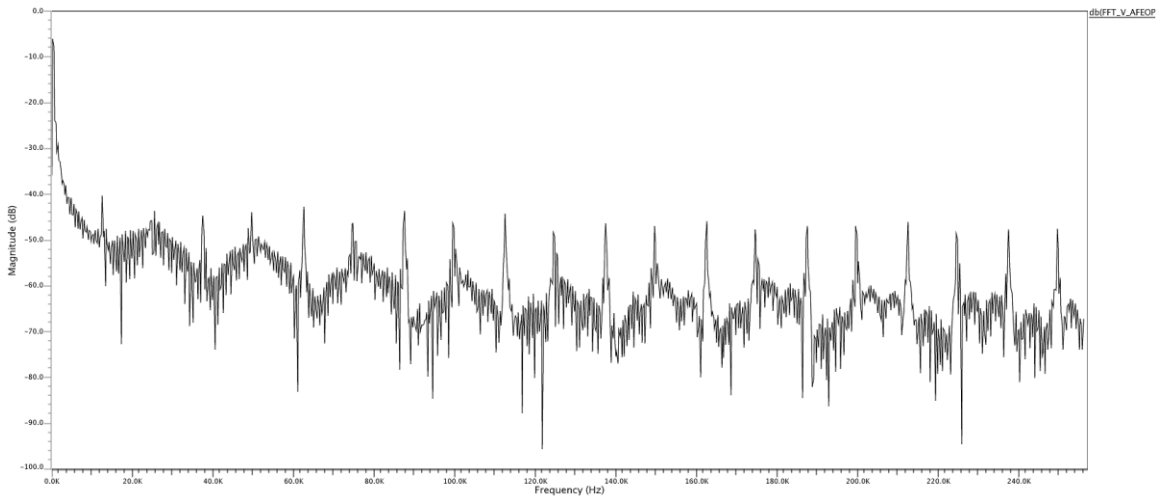


Figure 4.24. The post layout FFT of the ADC input.

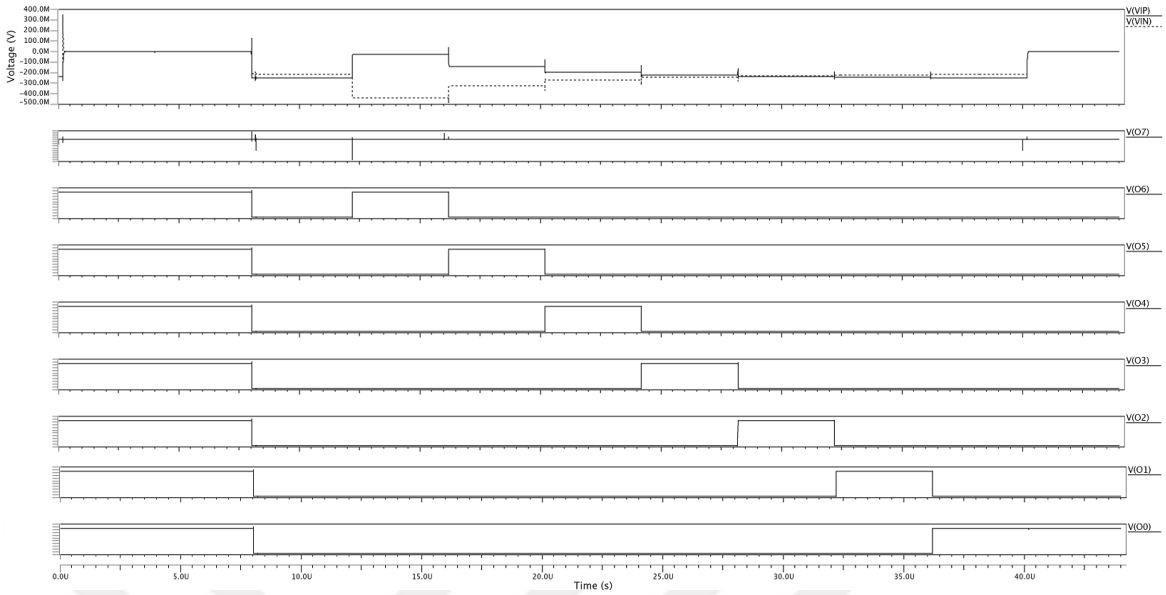


Figure 4.25. The transient response of the ADC for 8 mV (1 LSB) input signal.

Table 4.2. The performance evaluation of ADC.

Resolution	8 bits
Sampling Rate	25.6 kHz
Supply Voltages	+0.9/-0.9 V
Full Scale Range	1.8 V_{pp}
ENOB	7.2
Area	<150 μm^2
Power consumption	11.2 µW
Power consumption (Without biasing)	7.6 µW
FOM (Pre-Layout)	180.6 fJ/samp
FOM (Post-Layout)	1.55 pJ/samp
SNR of the system (Post-layout)	45 dB

The literature comparison is given in Table 4.3, which shows that for a comprehensive design task like this (sensor model and its noisy input, analog-front-end and the data converter together) it is quite normal to have an average value in the FOM, most of the given

work in the area covers only one of the given blocks, in the table all given references are published ADC designs.

Table 4.3. The literature comparison table.

Parameter	[35]	[36]	[37]	[38]	[39]	This Work
Technology (nm)	350	180	130	45	180	180
Sampling rate (kS/s)	1280	4.1	1	-	40	25.6
Power (µW)	140.7	0.850	0.053	330	10	7.6 (ADC)
ENOB (bits)	9.7	6.9	9.12	9.1	10.75	7.2
FOM (fJ/samp)	132	1700	94.5	1980	322	1550
Resolution (bits)	10	8	10	10	11	8

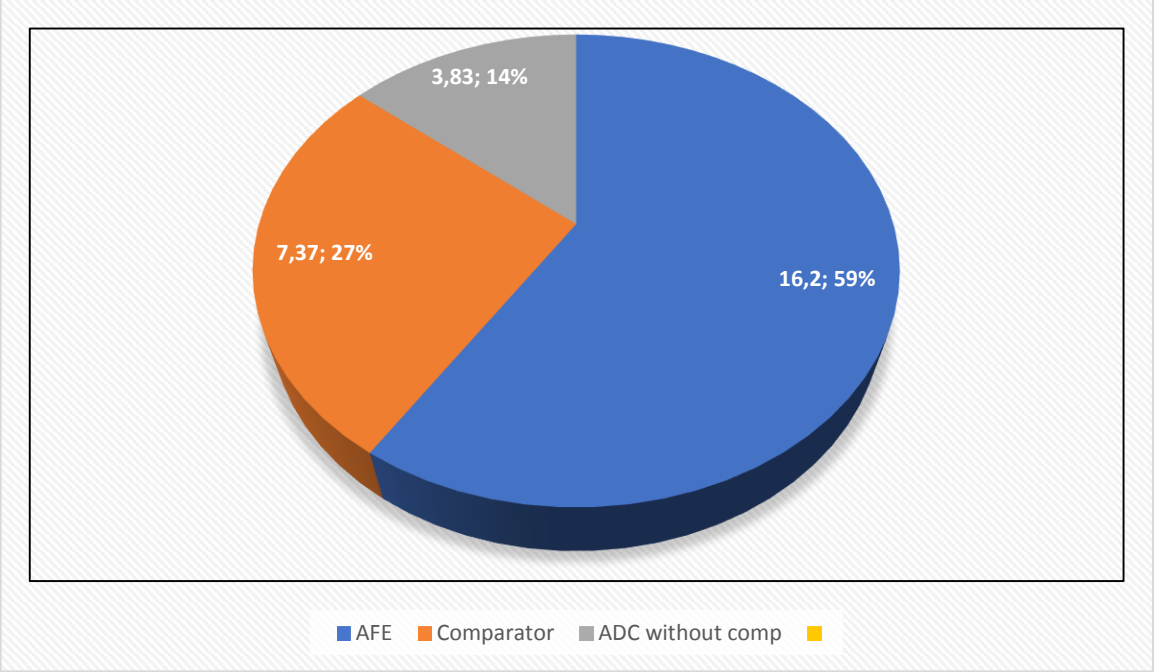


Figure 4.26. The power consumption distribution (µW).

5. CONCLUSION

Improvements in the sensor industry have made the interface design more and more crucial for proper read-out systems. Especially with magnetoresistive sensors, it is also possible to build an on-chip sensor with the interface and build an excellent sensor and interface system together with lower costs. The details in the sensor electronics and proper selection with application specifications are discussed, a smaller sized sensor was selected due to the low-level detection specification (below 100nT) and the path of the differential sensor signal was given in detail with each step and selection. The labeling of the organic material is another issue, the Dynal M-280 magnetic nanotags were selected for this application, because of their prevalence, susceptibility, good magnetization behavior, and compatibility with many organic materials. As the main block of the analog-front-end, CCIA structure has been chosen and an additional gain block was added to that block to decrease the capacitive mismatch effects. With this block, the required gain has been achieved without draining too much power. The feedback loop capacitors provide good DC common mode rejection in the inputs, also bring lower noise compared to the resistive feedback. Choppers were added to the amplifier inputs, outputs of the first stage and the feedback path to decrease the offset and the 1/f noise of the first stage. Since the transistors are biased with lower currents the noise would be a problem especially the first stage noise with very low-level inputs and high gain in overall system, dynamic range issues may arise. Due to chopping, the analog-front-end was capable to amplify the signal without adding considerable noise on it. In the next step a data converter was chosen to convert the analog signal to digital code. For this thesis, the chosen structure is SAR ADC, due to its very good power requirements and capability for continuous conversions. The drawbacks of the SAR architecture such as speed and resolution are not much of a problem with bio-applications. Three main blocks form the SAR structure. The DAC was realized by a simple capacitive array and V_{CM} based charge redistribution process was selected for charge redistribution, which consumes much lower power than conventional one [40]. The comparator has two auto-zeroed preamplifier stages, dynamic latch, and metastability circuitry. Preamplifiers help boost the DAC output levels for the latch, and more importantly the first stage was chosen with lower gain and autozeroed to prevent from adding noise or offset on the signal and the second stage was

chosen with considerably larger gain to reduce the high latch offset. The latch was chosen as a dynamic latch, which means that it compares the inputs only when the control signal is triggered, so there is no unnecessary power consumption from that sub-block. For the metastability error in the latch output levels, there is an additional circuitry was utilized, which holds the latch output at the same level until triggered. SAR logic is straight forward choice for that type of structure, which is a synchronous system driven by a clock and reset signal.

In conclusion, the presented interface has proven to be promising for low-power sensor applications. All the primary specifications have been achieved and the overall performance of the system is satisfactory. All the performance evaluations of the blocks were given at the end of the chapters. The work done in the thesis may be go even deeper by using more sensitive sensors like TMR sensors or adding some additional blocks to CCIA, like ripple reduction loops or impedance booster loops or improving the SAR ADC resolution, speed, or die area requirement.

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