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Controlling trapping potentials and stray electric fields in a microfabricated ion trap through design and compensation

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Abstract. Recent advances in quantum information processing with trapped ions have demonstrated the need for new ion trap architectures capable of holding and manipulating chains of many (>10) ions. Here we present the design and detailed characterization of a new linear trap, microfabricated with scalable complementary metal-oxide-semiconductor (CMOS) techniques, that is well-suited to this challenge. Forty-four individually controlled dc electrodes provide the many degrees of freedom required to construct anharmonic potential wells, shuttle ions, merge and split ion chains, precisely tune secular mode frequencies, and adjust the orientation of trap axes. Microfabricated capacitors on dc electrodes suppress radio-frequency pickup and excess micromotion, while a top-level ground layer simplifies modeling of electric fields and protects trap structures underneath. A localized aperture in the substrate provides access to the trapping region from an oven below, permitting deterministic loading of particular isotopic/elemental sequences via species-selective photoionization. The shapes of the aperture and radio-frequency electrodes are optimized to minimize perturbation of the trapping pseudopotential. Laboratory experiments verify simulated potentials and characterize trapping lifetimes, stray electric fields, and ion heating rates, while measurement and cancellation of spatially-varying stray electric fields permits the formation of nearly-equally spaced ion chains.

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1. Introduction

Research with trapped atomic ions has progressed rapidly in recent years [1–3], driven in large part by interest in developing a large-scale quantum information processor. Much recent work has focused on scaling experiments to larger numbers of ions, with particular developments in multi-ion entanglement [4, 5] and quantum simulation [6–8]. One plan for working with large numbers of ions utilizes anharmonic trapping potentials to stabilize chains against structural instabilities [9]. An alternative approach involves interconnected networks of many trapping zones [10, 11]. Both approaches require the use of many trap electrodes; as experiments move toward larger scales, it is imperative that ion trap technologies keep pace.

One technology that is particularly amenable to scaling and complex geometries is the surface-electrode trap [12, 13], where all of the electrodes are in a common plane. This geometry is easily miniaturized, which is advantageous for scaling both because more electrodes may be fit into a given area and because multi-qubit gate-operation times scale favorably with decreasing trap dimensions. Planar geometries are also amenable to microfabrication as a monolithic structure, eliminating the challenges of aligning and assembling the components of (more traditional) multi-substrate or macroscopic four-rod Paul traps. Microfabrication also enables simultaneous construction of many virtually identical traps, and should permit assembly of combinations of linear sections with junction elements [14–16] to form interconnected networks of many trapping zones.

In this work we present a microfabricated trap that incorporates three features which improve the fine control of trapping potentials: microfabricated on-chip capacitors that locally suppress radio-frequency (RF) pickup on dc electrodes, a top-level ground layer covering 97% of the chip surface that simplifies modeling of trap potentials by shielding electrode leads, and a loading aperture which, along with locally shaped RF rails, reduces deformation to the RF

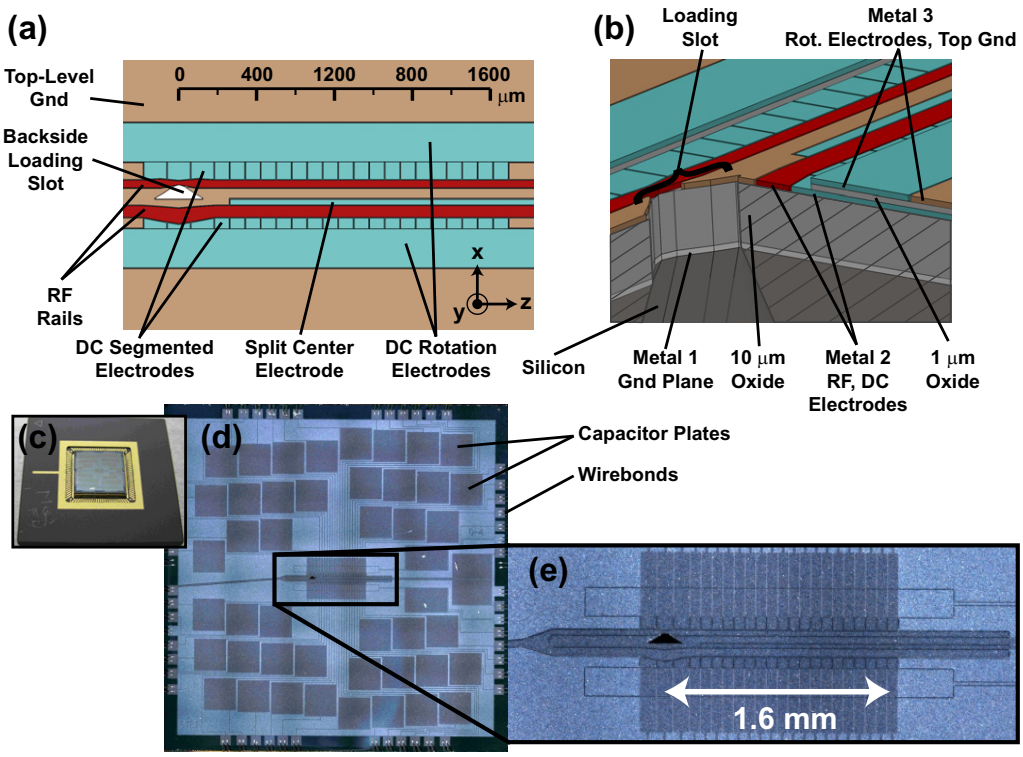

Figure 1. (a) A schematic view of the active region, and (b) a cutaway view showing internal layers (vertical direction is 10 × expanded to make thin internal layers visible). (c) A packaged trap mounted in a 100 pin CPGA. (d) Dark-field optical microscope image of the trap chip. Note the arrangement of the wire bonds, which permit optical access at 90° and 45°. (e) An enlargement of the active region. The darker shade indicates components fabricated in the middle metal layer, including RF rails, dc electrodes and on-chip capacitors. Components are effectively visible even where covered by the top metal layer due to layer print-through and slight differences in surface roughness.

pseudopotential tube in which ions are confined. Traps are fabricated on silicon substrates from patterned layers of aluminum and silicon dioxide (SiO_2) using standard CMOS-compatible techniques similar to those described in [17]. We have used several of these traps to study lifetimes and heating rates of single ions and to create single- and dual-species ion chains. Using a single ion as a probe, we experimentally characterize the spatial and temporal dependence of stray electric fields along the length of the trap. Treating the measured fields as model inputs, we derive global nulling potentials that cancel stray fields throughout the trap, enabling the formation of nearly-equally spaced ion chains in anharmonic potential wells.

2. Trap design

The trap is based on an asymmetric five-wire geometry [12] with a split center dc electrode and segmented outer dc electrodes (figure 1). Three metallic conducting layers are created from

99% Al/1% Si[3] and are separated from one another by SiO_2. The bottom metal layer forms a ground plane that prevents RF electric fields from penetrating into the RF-lossy p^{++}-doped silicon substrate. A thick insulating layer of 10 μm of SiO_2 between the middle (electrode) layer and this ground plane limits the capacitance and power dissipation of the RF electrodes. A second ground plane covering most of the trap is separated from the electrode layer by a 1 μm SiO_2 layer. This top ground defines the outer boundary of the segmented control electrodes and forms the second plate for capacitors patterned into the electrode leads (see below).

The trap is designed around a target ion height of 63 μm.[4] Dc and RF rail widths and locations are chosen using the conformal mapping described in [18] to obtain this height while rotating the natural (dc) secular axes 25° from the trap normal. This axis rotation ensures that both radial secular modes may be Doppler-cooled by a single laser oriented along the trap surface. RF rails 30 and 50 μm in width provide strong radial confinement at modest voltages (radial secular frequencies of ∼4 MHz at ∼100 V for $^{40}Ca^{+}$) while keeping power dissipation low. The dc rails are segmented into control electrodes with a 79 μm pitch (except for those around the loading slot, which are 120 μm). Additional dc electrodes that run along the entire length of the trap permit axis rotation and micromotion compensation over long chains of ions. All gaps between electrodes are 4 μm wide near the ion, expanding to 10 μm under the top-level ground to reduce the probability of unintended shorts or RF breakdown. Electrical connections are made via wire bonds strategically placed around the trap perimeter to provide optical access along key directions.

2.1. Shaped loading slot

A common failure mode for surface-electrode traps is shorting between electrodes due to neutral atom flux contaminating the trap surface during trap loading; such contamination can also negatively impact trap heating rates [19, 20]. One solution is to pierce the trap substrate with a slot, allowing the neutral atom source to be relocated behind the trap, so that the trap substrate prevents accumulation on the electrodes (first utilized in [17]). These 'back-side loading slots' must necessarily lie directly below the pseudopotential null, causing variations in trap strength over the slot as well as pseudopotential barriers at the slot edges. Loading slots also locally affect the ion height, requiring adjustments to laser heights as ions are shuttled into or away from the loading zone. One resolution is to extend the loading slot along the entire trap [21]. However, this increases sensitivity to stray fields from sources behind the chip, reduces ion lifetime while loading due to collisions between neutrals and trapped ions, and complicates deterministic loading of a particular number or sequence of ions. Alternatively, spatially separating the loading slot from computational regions [14, 15] restricts pseudopotential deformations from the slot to remote areas. However, this strategy cannot be used if optical or other components [22] need to be integrated adjacent to computational regions.

[3] 99% Al/1% Cu has recently replaced 99% Al/1% Si for metal layer deposition. While Al/Si is more easily etched during trap fabrication, 'whiskers' can grow out of the trap surface during bakeout which can scatter laser light or even form shorts between adjacent electrodes. Al/Cu metalization does not form these whiskers, though it does still form hillocks that can roughen the trap surface during extended bakeout at temperatures exceeding 200 °C.

[4] 63 μm is 1.5 times the trap-edge waist size of a 397 nm laser focused to minimize light scatter, adequate to largely eliminate diffraction from the edge of the chip.

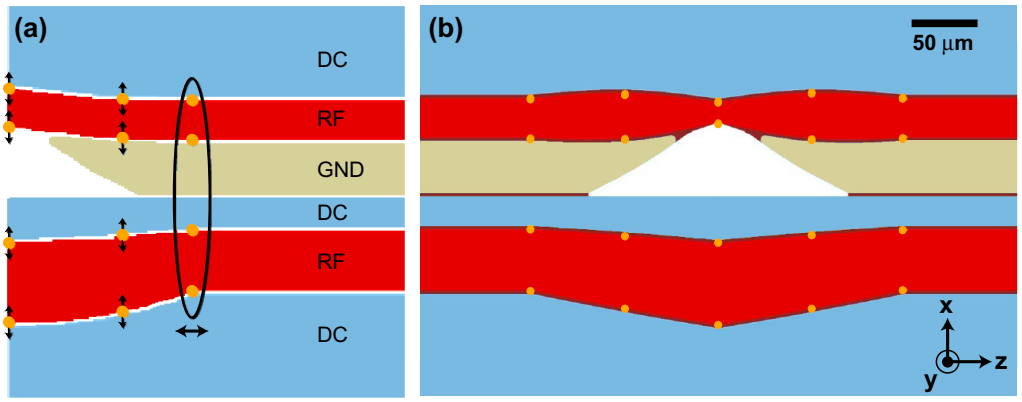

Figure 2. Loading slot and RF rail optimization. (a) Initial geometry and control points used as a starting point for the optimization. Due to symmetry considerations only half of the slot need be simulated. (b) Final optimized shape.

To address these issues it is desirable to minimize local pseudopotential deformations and maintain a constant ion height over the loading zone. This may be accomplished by replacing the parallel RF rails with shaped rails to correct for the perturbation caused by a loading slot. As a starting point, we define an initial geometry that qualitatively addresses the problem (figure 2). Firstly, a modified slot with tapered edges is introduced (here a trapezoid). Secondly, the separation between the RF rails is increased around the slot, raising the height of the pseudopotential tube [18]. Third, the rail widths are increased, strengthening the radial confinement. To optimize this modified geometry the shape is characterized in terms of a set of twelve variable 'control points' (nine degrees of freedom) that completely define the edges (figure 2(a)). The locations of these points are systematically varied with a downhill-gradient search. Overlap between each new geometry's electric field and a target field serves as a fitness function to measure progress towards a solution. Fields are calculated with an in-house boundary element method (BEM) electrostatics solver capable of solving problems with more than 10^6 unknowns, similar to those described in [23, 24].

Using this procedure we find an improved slot geometry that reduces variations in ion height from the 17 μm resulting from the rectangular slot in the trap described in [17] to less than 3 μm (figure 3). The optimized geometry largely adheres to the qualitative model described above, with the exception of the central 'pinch' in the narrower RF rail which compensates for a bend in the pseudopotential tube in the $\hat{x}$-direction that would otherwise result from the asymmetry of the loading slot.

2.2. Top-level ground

A major difficulty for the design and use of segmented ion traps is the challenge of accurately simulating the electric fields produced by complicated electrode geometries. BEM solvers, commonly used to simulate trapping potentials, work by discretizing (meshing) the electrode surfaces into small elements (often triangles) and then solving for the charge density on the electrodes and the associated fields. Since the charge density exhibits a singularity along electrode edges, a fine mesh is required in these areas; a coarser mesh is adequate away from

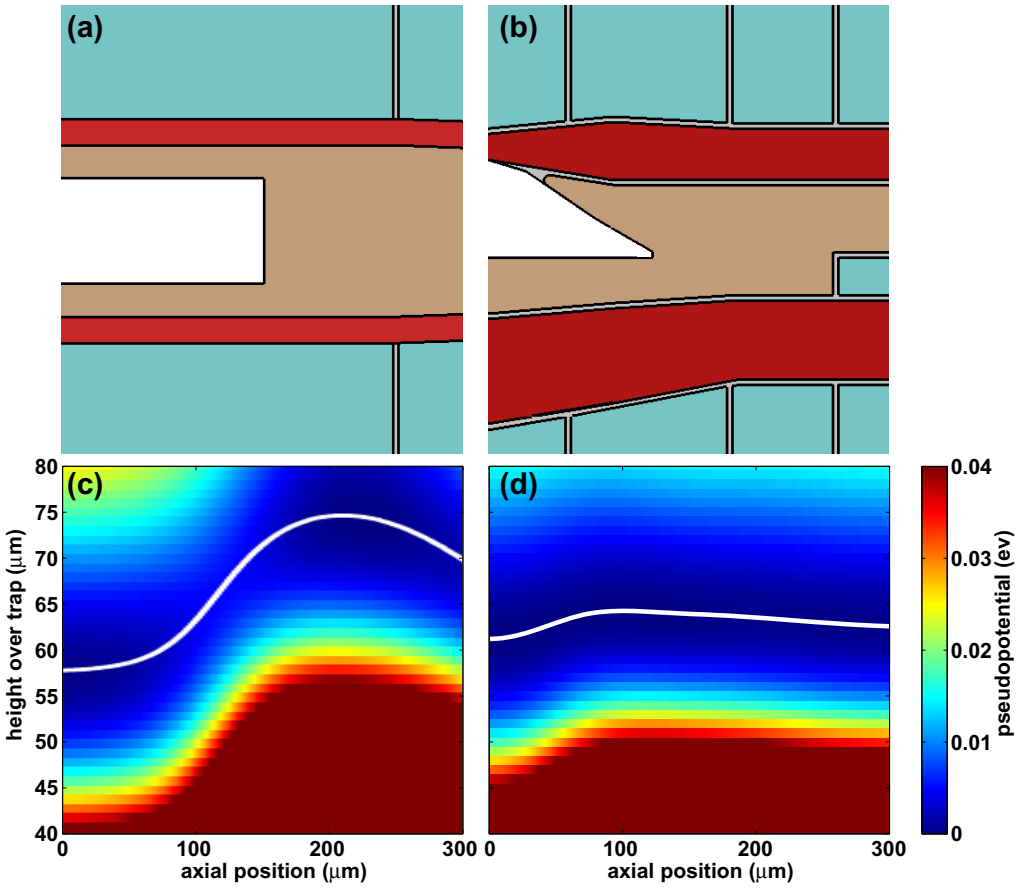

Figure 3. Back-side loading slot comparison. (a) The slot geometry in [17], and (b) the modified slot geometry. (c, d) Pseudopotential resulting from (a) and (b), respectively; horizontal scale is shared throughout. Simulations are for 60 MHz RF drive frequency and 3.5 MHz radial secular frequencies. The white line represents the height of the RF-null. Note especially the reduced variation in ion height at the edge of the load zone in the optimized geometry.

edges. Even with this 'adaptive meshing', complicated electrode geometries generally have tens or hundreds of thousands of elements.

To reduce the problem size (and the corresponding requirements for computation time and computer memory), a conventional approach is to restrict the modeling to the immediate vicinity of the ion. While this is a reasonable approximation in some situations, increased modeling accuracy requires the inclusion of more distant pieces of the trap geometry. Such accuracy is especially important when calculating transport waveforms (sets of smoothly varying potentials) that merge and separate ions, because these waveforms balance the fields from many electrodes, magnifying small errors. Unfortunately, distant areas generally contain electrode leads and other small features, requiring fine meshing and dramatically increasing problem size. A better solution to improve modeling accuracy is to shield these distant areas with an additional ground plane above the electrode layer. This replaces the many edges of individual electrode leads with a single large feature, most of which may be coarsely meshed. An added ground plane also

improves the match between modeling and experiment by shielding the ion from insulating trap features that might otherwise be at an undetermined potential. Additionally, the top metal layer protects underlying structures from scratches incurred during wafer dicing and trap packaging, increasing yield.

2.3. On-chip capacitors

The top-level ground may be used in combination with the middle metal layer to form capacitive filters for the dc electrodes. Such capacitors are an essential element for reducing RF pickup on these control electrodes. Placing the capacitors close to the trap is important, because their effectiveness is impaired by any intervening resistance or inductance, such as that of a lead between the trap and a vacuum feedthrough [25]. The trap described here incorporates 1 mm^2 capacitor plates into the leads for the dc control electrodes (see figure 1(d), providing 60 pF to ground. Along with the stray capacitance between individual dc electrodes and the RF rails (calculated to be $\sim 1.4 \times 10^{-3}$ pF), these capacitors create a capacitive divider that shorts RF signals to ground, suppressing the RF pickup by a factor of approximately 4.3×10^4.

3. Fabrication and packaging

Trap fabrication uses standard silicon very-large-scale-integration (VLSI) processing steps [26]. To begin, we clean a p^{++}-doped silicon wafer (0.5 mm thickness) using a piranha etch followed by a buffered oxide etch, removing contaminants and surface oxidation to ensure good metal adhesion. We then etch most of the way through the wafer from the back side with potassium hydroxide (KOH) to form a tapered rectangular relief that will later become the loading slot. A 1 μm layer of aluminum, bonded to the wafer with a 30 nm titanium underlayer, is deposited on the front side to form the bottom ground plane. This layer is lithographically patterned and plasma-etched to define the trap loading slot and alignment marks for ensuing layers. We then deposit a thick (10 μm) film of low stress oxide ($\sim$20 MPa for a 10 μm layer) via plasma-enhanced chemical vapor deposition (PECVD) to separate the electrode layer from the bottom ground plane; 10 μm is adequate to reduce the RF-electrode capacitance to $\sim$1 pF. A second aluminum layer (also bonded with a 30 nm titanium adhesion layer) is deposited on top of this oxide. This layer contains essential trapping structures, including RF and dc electrodes, electrode leads, capacitor plates, and wire bond pads; it is also patterned with photolithography and plasma-etching.

We then deposit the top-level ground, a 1 μm aluminum layer (again bonded by a 30 nm titanium underlayer) over 1 μm of oxide. A deep inductively-coupled plasma (ICP) oxide etch removes oxide exposed in the gaps between electrodes. To complete the loading slot an ICP–Bosch etch from the back side of the wafer removes the remaining substrate material in the KOH etched region to open the loading slot aperture. We coat the back side with a titanium adhesion layer and 300 nm of gold to prepare the chips for ultra-high vacuum (UHV) compatible mounting. The wafer is then cleaned and diced into chips. Final die-level oxygen plasma and argon plasma treatments prepare the trap surface for wire bonding.

To package the traps for vacuum installation, chips are mounted to a ceramic pin grid array (CPGA) carrier via a 1.2 mm tall slotted alumina spacer with 80/20 Au/Sn solder (figure 1(c)). The spacer raises the top of the chip above the CPGA perimeter to permit access for laser beams parallel to the trap surface. Aluminum wires (25 μm diameter) are wedge bonded to the

chip and carrier to make all electrical connections with two wires used on each connection for redundancy. The resulting carrier/trap package is ready for in-vacuum installation.

4. Experimental characterization and control

To date we have trapped ions in ten of these traps. We have extensively characterized five, measuring stray electric fields and secular mode frequencies, determining heating rates, and quantifying ion loss during ion transport. We have built single-species chains of up to twelve ions as well as shorter multi-species chains. All data presented here were collected with $^{40}Ca^{+}$ and/or $^{44}Ca^{+}$. As calcium trapping has been reviewed elsewhere [3], we confine discussion of our particular experimental setup to the appendix.

4.1. Ion shuttling and model verification

Ions may be moved between different points in the trap by applying a transport waveform to the dc control electrodes. Waveforms are constructed by deriving potential sets that create an axial harmonic well at regularly spaced intervals (usually every $10\,\mu$m) throughout the trap. Our waveforms typically are designed for an axial secular frequency $\omega_z = 2\pi \times 1$ MHz for ^{40}Ca and a 12° rotation of the radial axes from the trap normal. Intermediate waveform positions are generated by interpolating between adjacent wells to produce smooth transport.

Sequentially updating dc control voltages according to the appropriate transport waveform generates a moving potential well that can shuttle an ion between different locations. Waveforms for merging and splitting of multiple ions between adjacent potential wells may be generated in a similar fashion from suitable superpositions of wells when ion-ion repulsion is included in the model. Typical waveforms utilize 1000 steps for transport across the entire 1.4 mm length of the trap, giving a maximum ion velocity of $0.7\,\mathrm{m\,s^{-1}}$ at 500 kHz DAC update rate. Modeled potential wells show excellent agreement with their implementation in fabricated traps. We characterize axial harmonic wells by measuring secular frequencies and ion positions at $10\,\mu$m intervals, finding agreement with simulations at the 3% level throughout the entire trap excepting the loading zone. We find that loading rates and agreement with simulation in the vicinity of the load zone are sometimes improved by locally perturbing the potentials to counteract stray electric fields near the slot. These fields may arise from sources behind the trap and penetrate the slot, or from stray charge nearby. Stray charge near the loading slot is thought to originate from poor collimation of the UV photoionization laser [27].

4.2. Stray field measurement and global compensation

The close proximity of the lasers to the trap in small surface-electrode traps can lead to the accumulation of stray charges [27, 28]. These charges create fields that push ions away from the pseudopotential null, sometimes distorting the potential enough to prevent trapping. Uncompensated stray fields cause excess micromotion which negatively impacts Doppler cooling, fluorescence collection, and ion heating rates [29]. They also affect the spacing and stability of ion chains and may contribute to ion loss during shuttling operations. Detailed measurement and characterization of stray fields is therefore essential for optimizing trap operation.

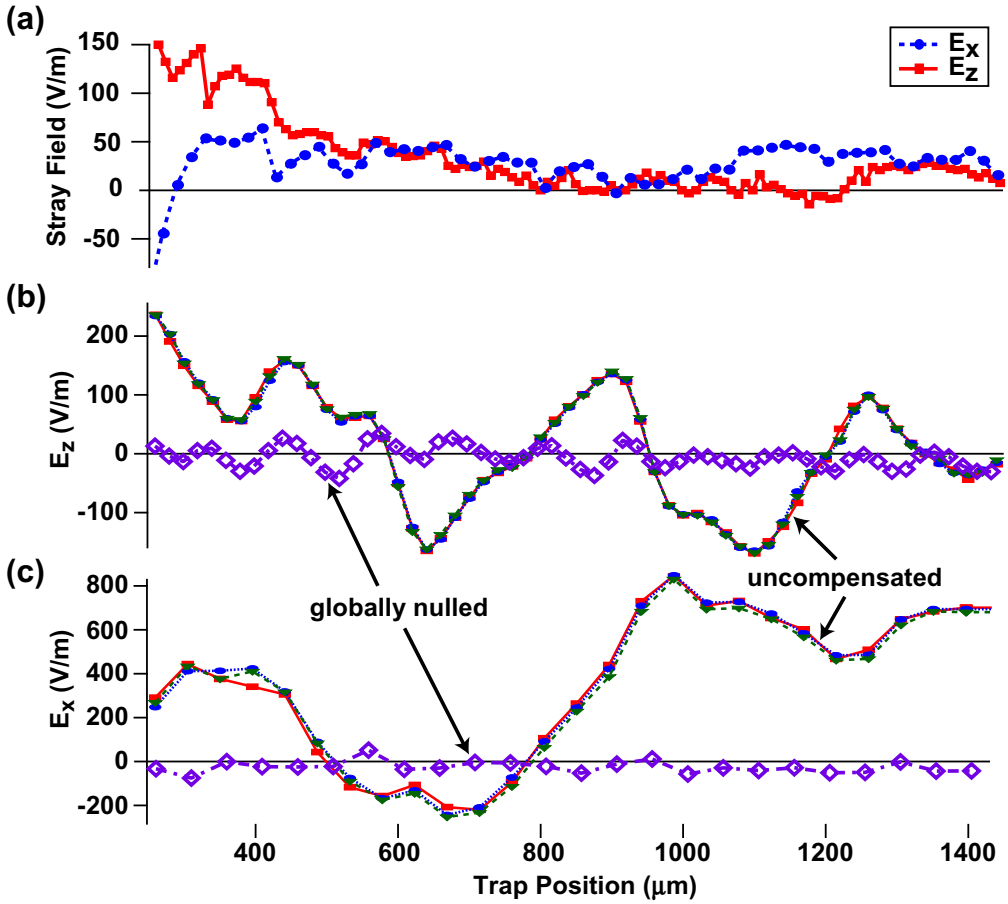

Figure 4. Stray field stability and compensation. (a) E_x and E_z as measured in a typical trap. (b) E_z and (c) E_x in a trap with unusually large stray fields, measured on three consecutive days after initial transient charging behavior had saturated. Stray fields are simultaneously cancelled to less than $50\,\mathrm{V\,m^{-1}}$ throughout the entire trap ($\diamond$) by applying a global nulling potential. Typical error-bars are 10 and $20\,\mathrm{V\,m^{-1}}$ for E_z and E_x, respectively.

Along the $\hat{z}$-direction the dominant effect of stray fields is to shift the location of the harmonic well created by the dc potentials. For a stray field E_z, ion mass m, and axial secular frequency ω_z, the shift is given by $z_{\mathrm{ion}} = eE_z/m\omega_z^2$. Scaling the strength ω_z of the axial well while simultaneously monitoring the position of an ion allows us to extract the magnitude of the stray field. By automating this procedure and measuring at many ion locations, we produce a detailed map of E_z (figure 4(a)). Measurement precision is approximately $10\,\mathrm{V\,m^{-1}}$, limited by the effective size of our camera pixels ($1.6\,\mu\mathrm{m}$).

To measure stray fields along $\hat{x}$ [5] we follow a procedure similar to that outlined in [30]: the (resolved) micromotion sidebands on the 397 nm cooling transition are minimized by applying a known field via the dc electrodes. This determines the stray field with a precision of

[5] Stray fields along a direction $\hat{n}$ do not in general cause micromotion purely along $\hat{n}$. However, in our trap the RF pseudopotential axes are only slightly rotated from the trap normal, so micromotion along the $\hat{x}$ and $\hat{y}$ directions is predominantly due to stray fields E_x and E_y, respectively.

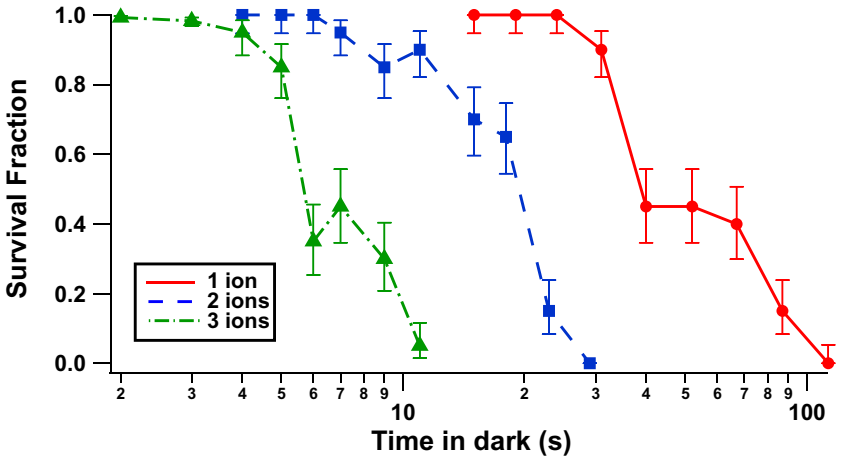

Figure 5. Lifetimes without Doppler cooling for single ions and small chains trapped in a harmonic ($\omega_z = 1$ MHz) well. Survival is defined as the entire chain remaining intact; no distinction is made between the loss of one or several ions.

approximately 10–20 V m^{-1} (figure 4(a)). In principle, stray fields along $\hat{y}$ could be measured in the same way. Unfortunately, lasers aligned in the $\hat{x} - \hat{z}$ plane are insensitive to micromotion along $\hat{y}$, so alternative methods [31, 32] are more practical. As fields along $\hat{y}$ do not strongly impact Doppler cooling or shuttling fidelity in this trap, we do not map them exhaustively in general. However, we can indirectly extract E_y from the splitting between the radial secular modes, which depend on E_y due to anharmonicities in the RF-pseudopotential. Comparison of measured and modeled splittings allows us to estimate E_y, which is usually less than 200 V m^{-1}.

We find that stray fields vary at the level of approximately 100 V m^{-1} per day during the first few days of trap operation, possibly due to laser-induced charging of surface contaminants and oxide. This variation saturates after approximately one week, after which stray fields vary at the level of a few tens of V/m or less (figures 4(b) and (c)). After saturation the secular mode frequencies are stable to one part in 10^{-4} over hours and one part in 10^{-3} over days during normal trap operation.

We use the measured stray field profile as a model input to calculate a trap-specific field-nulling potential that simultaneously cancels these fields along nearly the entire trap. Nulling solutions are calculated from the BEM model by varying the applied potentials on all segmented electrodes in a downhill-gradient search to match the measured E_z and E_x while maintaining $E_y = 0$. In addition to matching the measured fields, the optimization minimizes $\delta E_z/\delta x$ and $\delta E_z/\delta y$ to prevent the secular axes from being skewed relative to the pseudopotential symmetry axis. Two additional first order parameters remain unconstrained, corresponding to a radial quadrupole field rotated at an arbitrary angle. However, this causes only slight variations in radial secular axis directions and frequencies for which we may account with further experimental characterization. Nulling solutions generally require only modest ($\sim\pm 1$ V) voltages and cancel stray fields to less than 50 V m^{-1} (figures 4(b) and (c)).

4.3. Trapping lifetime and ion chains

The trapping lifetime of a single Doppler-cooled ion is many hours or longer. The lifetime without cooling is approximately 45 seconds and is strongly non-exponential: losses are

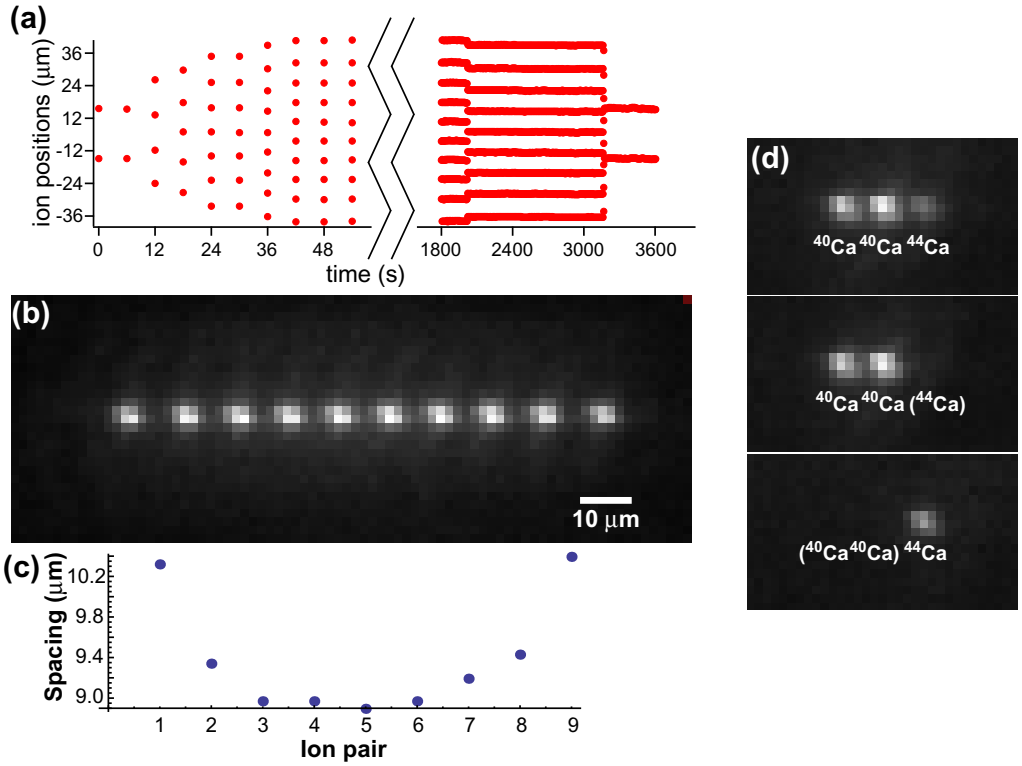

Figure 6. Ion chains. (a) Ion-by-ion chain formation. During the first 42 s individual ions are loaded into a well at the loading zone and shuttled to a chain stored 900 μm away. After 42 s loading and shuttling is stopped and the chain is held in a static anharmonic potential well with continuous Doppler cooling. This 10-ion chain was stored for approximately 30 minutes before ion loss. (b) CCD image of a 10-ion chain. (c) Spacings between ion pairs in (b), demonstrating less than 5% variation in spacing for the central eight ions (a factor of three times more uniform than for a harmonic well with the same central spacing). Error-bars are comparable to the size of the points. (d) A mixed-isotope chain. (top) The chain is illuminated with two frequencies of Doppler cooling light. (lower panels) Only one of the two frequencies is used.

negligible for the first 25 s after cooling is stopped. Chains of two or three ions display similar loss characteristics with shorter lifetimes (figure 5).

An advantage of this trap geometry is the ability to deterministically load rare isotopes or mixed-species chains with a predetermined number and sequence of ions. Whereas ions trapped in geometries with long, open loading slots are susceptible to charge exchange collisions during loading [33], the small slot in our geometry localizes the neutral atom flux and significantly reduces the likelihood of collisions for ions trapped far from the slot. By loading an ion in a potential well located above the loading slot, transporting it across the trap, and merging it with a second (static) well, it is possible to construct a chain of ions one ion at a time. Laser frequencies for photoionization and Doppler cooling at the loading zone may be chosen independently for each ion loaded, making it possible to build a chain with any desired sequence of ions. We utilize automated chain-loading routines that control laser frequencies and trapping

potentials while analyzing camera images for ion positions in real-time so as to load chains of a particular size and isotopic sequence (figure 6). Mixed-isotope chains may be cooled with only a single wavelength [34] (i.e. sympathetic cooling). We cool chains of $^{40}Ca^{+}$ and $^{44}Ca^{+}$ with a single laser tuned near the $^{40}Ca^{+}$ cooling transition. However, we find that the 842 MHz isotope shift is too small to permit robust sympathetic cooling using $^{44}Ca^{+}$ as the 'coolant' ion since in this case the laser is blue detuned relative to $^{40}Ca^{+}$, causing Doppler-heating on that isotope.

Stability and lifetime of ion chains can be improved by utilizing a 'flat-bottomed' potential instead of a harmonic well. Such anharmoinc potential wells are designed to hold ion chains with nearly-equal spacing between ions, mimicking the confinement that would be provided by placing a half-infinite chain of equally-spaced ions at each end of the trapped chain. This potential shape allows long chains of many ions to be stored without transitioning to a zig-zag structure [9] as more ions are added. Forming these potentials requires the use of many (>10) dc electrodes to strengthen the curvature at the edge of the well and compensate for the repulsive effect of the chain's space charge, but they provide greater trap depth and improved chain lifetime compared to harmonic wells [9]. Spacing between ions in such wells is extremely sensitive to axial stray fields. Any curvature in the axial field profile distorts the chain by clustering ions together or spreading them apart, and this effect is amplified as the number of ions grows. Nevertheless, after cancelling stray fields (section 4.2), we are able to construct ion chains with less than 5% variation in spacing between all but the end ions (figures 6(b) and (c)).

4.4. Ion heating

A critical parameter for any ion trap is the rate at which an ion is heated. The largest source of heating in ion traps remains incompletely understood, but it seems to be related to contaminants on the trap surface and is generally much larger than that expected from Johnson noise [35]. Following Turchette *et al* [20], we determine the heating rate by monitoring the ratio of the motional sideband intensities on the calcium $^{2}S_{1/2} \rightarrow {}^{2}D_{5/2}$ transition at 729 nm (figure 7). We find a heating rate of 0.41(4) quanta ms^{-1} at an axial secular frequency of 1.37 MHz, corresponding to a spectral noise density $S(E) = 3.9(4) \times 10^{-12}$ $V^2\,m^{-2}$ Hz. This is the lowest spectral noise density measured at room temperature to date for traps fabricated with CMOS techniques [35], and it is comparable to reported heating rates in other traps of similar size.

5. Conclusion

We have developed and characterized a surface-electrode ion trap fabricated with CMOS compatible techniques. In contrast to previous CMOS traps, this trap adds a third, grounded metal layer that shields the ions from potentials on distant trap structures, thereby reducing computational requirements for accurate electric-field modeling. By combining accurate simulations with precise, detailed measurements of stray electric fields, we generate dc potentials that null these stray fields simultaneously throughout large regions of the trap. This makes possible the reliable merging of potential wells for deterministic loading of ion chains and the formation of equally-spaced ion chains in anharmonic potential wells. Ion heating is low enough to incorporate this trap design into a future large-scale quantum information processor.

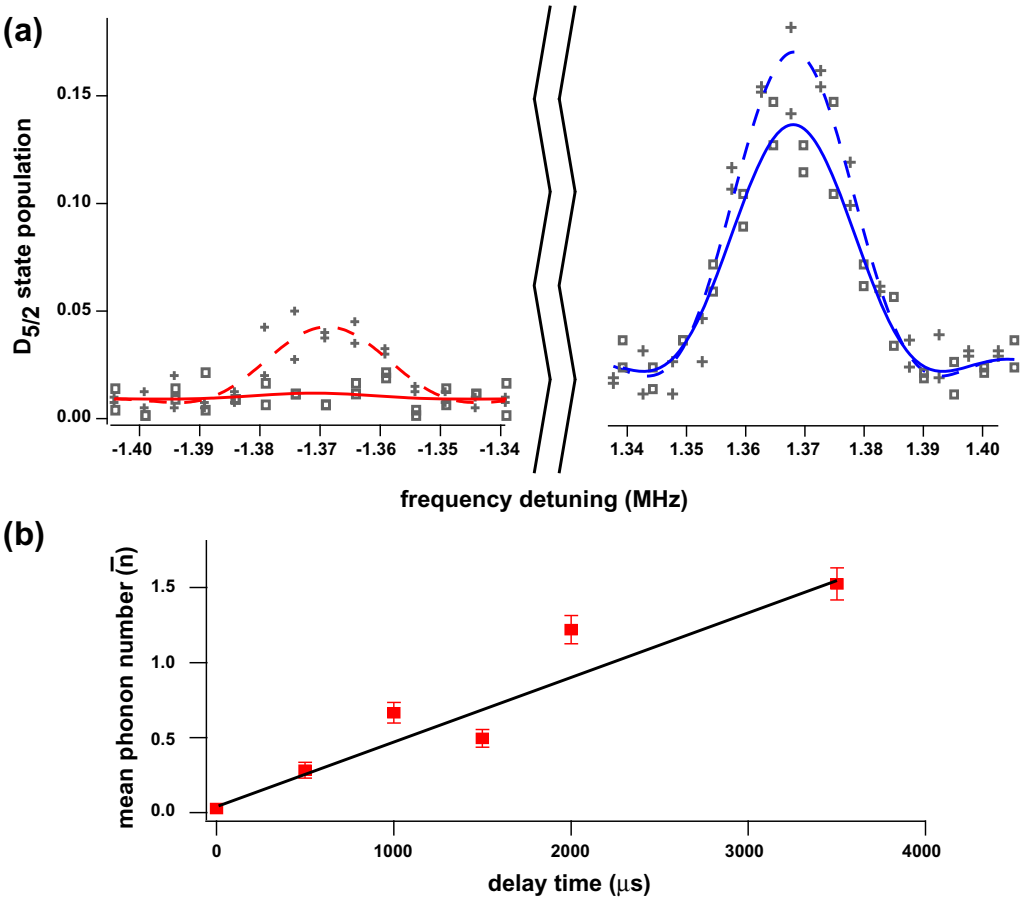

Figure 7. Ion heating. (a) Axial motional sidebands on the 729 nm $S_{1/2} \rightarrow D_{5/2}$ transition. Data indicated with squares (□) is taken immediately following sideband cooling, while crosses (+) are after a delay of 0.5 ms. (b) Heating of the axial secular mode ($\omega_z = 2\pi \times 1.37$ MHz). A linear fit yields a heating rate of 0.41(4) quanta ms^{-1}.

Acknowledgments

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Appendix. Experimental details

A.1. Vacuum installation

The CPGA/trap package is installed into a 100-pin socket formed by sandwiching individual pin receptacles between two UHV compatible PEEK plates. Each receptacle is crimped to a Kapton insulated wire, and the wires are bundled into four groups of 25 wires which terminate at commercial PEEK DB-25 connectors. The socket is screwed to a stainless steel (SS) base and rigidly mounted inside a 4.5-inch spherical octagon (Kimball Physics). A resistive oven beneath the socket produces neutral atoms directed through the loading slot. A SS screen (100 lines-per-inch, 80% optical transmission), attached above the carrier, shields the trap from stray electric fields. Low resistance electrical feedthroughs on two side ports of the octagon are used to feed the calcium oven and the trap RF. The top of the octagon is closed with a viewport for ion imaging and fluorescence collection. After the socket has been installed, the chamber is baked for ten days at 240 °C without a trap. We then install the trap and re-bake. Duration and temperature of this final bakeout are limited to 8 h at 200 °C followed by 24 h at 180 °C to avoid increasing trap surface roughness (see footnote 3). This bakeout is still adequate for an ion pump and a titanium sublimation pump to maintain a chamber pressure of approximately 1×10^{-9} Pa.

A.2. Trap operation

A helical resonator ($Q \sim 50$, driven with $\sim$0.5 W at 50–60 MHz) provides RF potentials for the trap. Injected RF power is monitored by a capacitive divider on the resonator output, allowing for active stabilization of the applied voltage to reduce drifts in the ion secular frequencies. The typical RF amplitude used for our measurements is approximately 200 V peak-to-peak (Vpp), but drive voltages of up to 500 Vpp or more can be tolerated without arcing. Dc potentials are supplied by National Instruments 12-bit PXI-6713 DAC cards, providing $\pm$10 V at update rates up to 500 kHz. Simple resistor-capacitor low-pass filters with a 20 kHz 3 dB cutoff immediately outside the vacuum chamber suppress noise at the update frequency and smooth applied waveforms during ion shuttling. We have found that these filters are inadequate to prevent heating during transport and have recently replaced them with third-order Butterworth low-pass filters (40 kHz cutoff) [24]. Three pairs of coils compensate stray magnetic fields and create a 4 G field along $\hat{x}$ (figure 1) to define a quantization axis.

A.3. Lasers and detection optics

Light is delivered to the vacuum chamber by single-mode optical fibers and focused across the trap surface. Beam waists ($\sim$30 μm) are chosen to minimize light scatter. Photoionization lasers (423 and 377 nm) are aligned to the loading zone along the $\hat{x}$ direction (see figure 1) so as to minimize overlap with trap electrodes and any associated charging. Repump lasers (866 and 854 nm) are aligned along $\hat{z}$ to uniformly illuminate the entire trapping region. Linearly polarized beams at 397 nm propagate along $(\hat{x} - \hat{z})$ for Doppler cooling. One of these beams is steered by a servo mirror (Optics in Motion) for computer-controlled tracking to any point along the trap. A third σ^- polarized 397 nm beam propagates along the magnetic field direction for optical pumping and state preparation. A 729 nm laser drives the $^2S_{1/2} \rightarrow {}^2D_{5/2}$ electric quadrupole transition and is used for sideband cooling and coherent operations.

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