LOW POWER SIGMA DELTA ANALOG TO DIGITAL CONVERTER DESIGN METHODS

by

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ABSTRACT

LOW POWER SIGMA DELTA ANALOG TO DIGITAL CONVERTER DESIGN METHODS

Sigma delta analog to digital conversion is an effective way of converting analog signals to digital signals when high signal to noise ratio and low power consumption is needed. Instead of comparing the input signal with references, the sum of differences of the signal between each comparison is compared differentially or with references. This operation could be achieved with integrators and a transfer function in *s* or *z*-domain. When this comparison is performed more frequently than the Nyquist rate of the signal which is called oversampling, less quantization error is obtained. Thus, high signal to noise ratio and less harmonics in the system is obtained.

Due to increase in mobile systems, power consumption became an important issue. Hence, engineers are more focused of efficiency of the systems. In this thesis, methods about designing low power sigma delta analog to digital converters with high performance are studied. Initially, 2nd order conventional and feed-forward discrete time sigma delta analog to digital converters with single-bit and multi-bit quantizers are studied. Next, 3rd order discrete time and 2-1 multi-stage sigma delta analog to digital converters are investigated. Afterwards, continuous time sigma delta conversion with different type of integrators is studied. Furthermore, a hybrid structure containing both discrete and continuous time integrators is investigated. In the meantime, the layout of the designs are prepared. Performance results of all the designs are obtained with post-layout simulations as well as the test results of the produced integrated circuits. Post-layout simulations show that the performance of the designs are close to the results of the designs with best results in the literature.

ÖZET

DÜŞÜK GÜÇLÜ SİGMA DELTA ANALOG SAYISAL ÇEVİRİCİ TASARIM YÖNTEMLERİ

Sigma delta analog sayısal çevirim, yüksek işaret gürültü oranı ve düşük güç tüketimi ile analog işaretleri sayısal işaretlere çevirmenin etkili yöntemlerinden biridir. Giriş işaretini kaynak değerleri ile karşılaştırmak yerine işaretteki değişimlerin toplamı farksal olarak ya da değişik kaynaklar ile karşılaştırılır. Bu işlem tümlev alıcılar sayesinde *s* veya *z*-uzayında bir transfer fonksiyonu ile gerçekleştirilir. Aşırı örnekleme, yani karşılaştırmanın Nyquist frekansından daha sık olarak yapılması halinde sistemde daha düşük nicemleme gürültüsü oluşur ve daha az harmonik ile yüksek işaret gürültü oranı elde edilir.

Hareketli sistemlerin yaygınlaşması nedeniyle güç tüketimi önemli bir sorun haline gelmiştir. Bu nedenle mühendisler sistemin verimi ile daha çok ilgilenmeye başlamışlardır. Bu tezde yüksek performansa ve düşük güç tüketimine sahip sigma delta analog sayısal çevirici tasarım yöntemlerinden bahsedilmektedir. Öncelikle, ikinci derece, geleneksel ve ileri beslemeli, ayrık zamanlı, tek ve çok-bit nicemlemeli sigma delta analog sayısal çeviriciler hakkında çalışmalar yapılmıştır. Sonra üçüncü derece ayrık zamanlı ve 2-1 çok katlı sigma delta analog sayısal çeviriciler incelenmiştir. Sonrasında, değişik tümlev alıcı devre yapısına sahip sürekli zamanlı sigma delta analog sayısal çeviriciler hakkında çalışmalar yapılmıştır. Buna ek olarak, hem sürekli hem de ayrık zamanlı tümlev alıcılardan oluşan bir karma yapı incelenmiştir. Sonraki adım olarak bu tasarımların serimleri hazırlanmıştır. Tasarımların serim sonrası benzetimlerden elde edilmiş başarım sonuçları elde edilmiş ve üretilen tümdevrelerin test sonuçları ile başarım sonuçları yinelenmiştir. Tasarımların serim sonrası benzetimlerden elde edilmiş başarım sonuçları, en iyi yazılı eserlerdeki tasarımlarla benzer başarım sonuçları göstermektedir.

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LIST OF SYMBOLS

g_m	Transistor Conductance
k	Boltzmann Constant
L	Integrator Order
n	Quantizer bit
OSR	Oversampling Ratio
T	Temperature

LIST OF ACRONYMS/ABBREVATIONS

ADC	Analog to Digital Converter
BW	Bandwidth
CT	Continuous Time
DAC	Digital Analog Converter
DT	Discrete Time
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FoM	Figure of Merit
IC	Integrated Circuit
MASH	Multi-Stage Noise Shaping
NTF	Noise Transfer Function
OPAMP	Operational Amplifier
OSR	Oversampling Ratio
PCB	Printed Circuit Board
SAR	Successive Approximation Register
SD	Sigma Delta
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
STF	Signal Transfer Function

1. INTRODUCTION

The growing popularity of mobile devices has increased the importance of low power designs. As battery life is a significant problem for mobile devices, engineers are continuously focusing their efforts on lowering the power consumption of components within these devices. Since digital domain signal processing has become popular due to its applicability in the field of electronics and programming, analog to digital converters (ADC) have a key role in bridging the gap between analog and digital worlds. Although there are many types of ADCs in the literature, Sigma delta (SD) ADCs are capable of achieving high SNR with low power consumption thanks to oversampling and digital filtering. A SD modulator consists of three blocks which are the modulator filter, the quantizer and the digital to analog converter (DAC) as depicted in Figure 1.1 [1]. The digital outputs obtained with the SD modulator are transferred to a digital filter where the digital outputs are obtained after filtering and decimation. Digital filter design is beyond the scope of this thesis and will not be discussed in detail in this thesis. The analog input entering the modulator filter is integrated and quantized afterwards. If the output of the modulator is sampled at a higher frequency than the Nyquist rate, the ratio between the sampling frequency and the Nyquist frequency is called oversampling ratio (OSR). The digital output of the modulator is turned into an analog signal in the DAC circuit and reduced from the analog input for the next sampling cycle. Therefore, instead of integrating the analog input, the difference between the analog input and the DAC output (delta) is added to the previous data (sigma) in the modulator. This operation causes the analog input signal to be transferred to the output with a signal transfer function (STF). Nevertheless, the modulator filter shapes and reduces the noise caused by the quantizer in the desired bandwidth with a noise transfer function (NTF) achieving high SNR in the meantime with the help of oversampling.

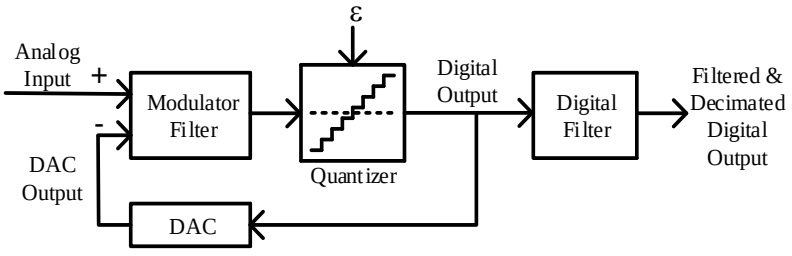

Figure 1.1. SD Modulator Block Diagram.

The first block in SD ADCs is the modulator filter block which has the option to be designed in either discrete time (DT) or continuous time (CT) or even a combination that may be called hybrid design. Although the modulator filter may be implemented directly, it is usually composed from integrators. The number of integrators defines the order of the modulator. Furthermore, each integrator increases the suppression of the in-band quantization noise in the bandwidth thanks to oversampling. DT integrators are designed in *z*-domain whereas the CT integrators are designed in the *s*-domain. The analog input and the DAC output signals, which are generally chosen as voltage are transferred to the quantizer with the desired transfer function. Nonetheless, there are some examples of current mode SD ADCs in the literature where these quantities are currents. Low pass filters are the most commonly used versions of the modulator filter block for suppressing the quantization noise in the desired bandwidth. However, the application might require a specific bandwidth which causes the modulator filter block to be designed as a bandpass filter.

The second block in SD modulators is called the quantizer block. This block is usually designed as a flash ADC with the desired resolution. However, it is quite typical to perform only 1-bit conversion leading to only a single comparator. A Successive Approximation Register (SAR) ADC can also be used as a quantizer which will be investigated in Chapter 2.

The third block in SD ADCs is the DAC block. It can be designed as any type of DAC in the literature, which is the most suitable for the ADC.

The SNR of a SD ADC is calculated as in (1.1) and (1.2) with the chosen values of the order (L), number of quantization bits (n) and OSR. Figure 1.2 shows the relationship of OSR with SNR and effective number of bits (ENOB). Here, ENOB represents the resolution of an ideal ADC that would have the same SNR with the designed ADC. ENOB is calculated as (1.3) and each additional bit in the quantizer increases ENOB by 1.

$$SNR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} OSR^{2L+1} 2^{n-1} \tag{1.1}$$

$$SNR[dB] = 1.76 + 3.01(log_2(2L+1) - 2Llog_2\pi + (2L+1)log_2 OSR + 2(n-1)) \tag{1.2}$$

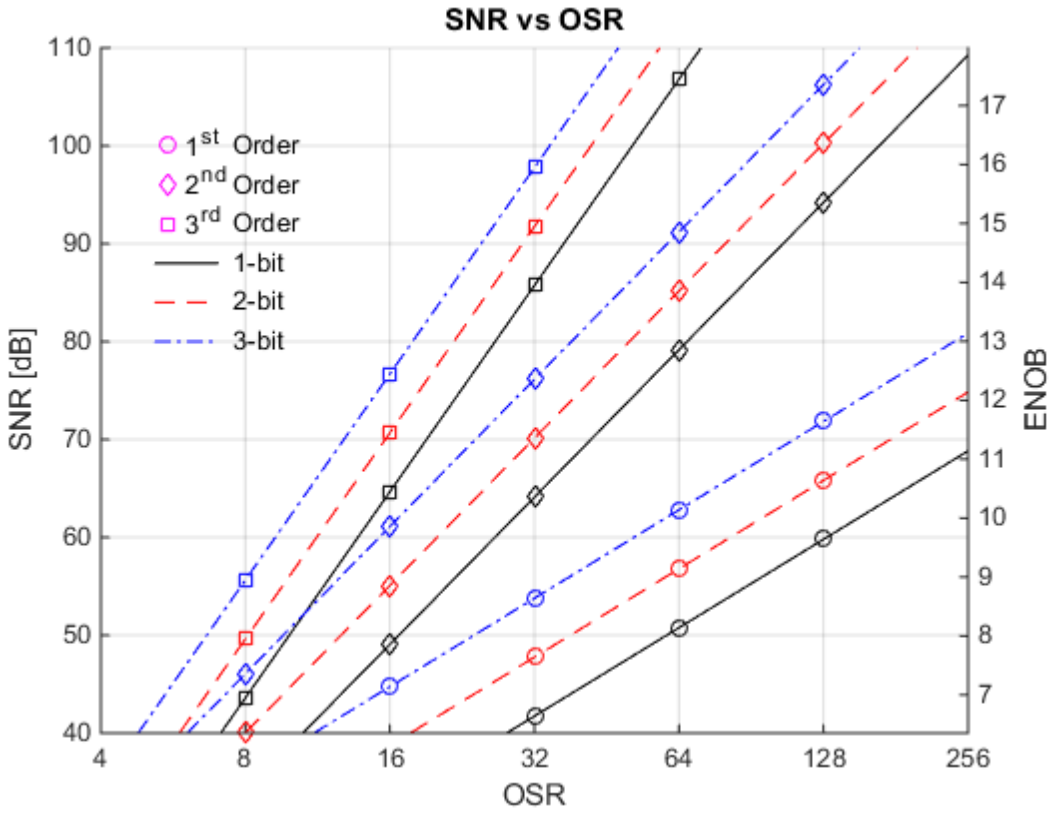

Figure 1.2. SNR and ENOB vs OSR.

$$ENOB = \frac{SNR - 1.76}{6.02} = \frac{log_2(2L+1)}{2} - Llog_2\pi + \frac{(2L+1)log_2 OSR}{2} + (n-1) \qquad (1.3)$$

According to Figure 1.2, high order SD ADCs can achieve high SNR values with lower OSR. Thus, high order SD ADCs have better power efficiency. Nevertheless, the transfer function for noise shaping is difficult to obtain and the SD ADC can be unstable for certain inputs. Thus, the SD ADCs are usually designed 2nd order. In 2nd order SD ADCs, high SNR can be achieved via choosing the OSR high, but the bandwidth requirements of the integrators are increased with high OSR which leads to high power consumption. Thus, multi-bit quantization is another method to obtain high SNR. Nonetheless, the circuit becomes very complex with multi-bit quantization. The signals have to be compared with 2^n-1 references by 2^n-1 comparators and 2^n references have to be used as feedback in *n*-bit quantization. Moreover, the linearity of these references affects the performance and matching methods in the DAC and using a data weighted averaging circuit would be needed. Hence, the area, the power consumption, and linearity requirement of these references makes multi-bit design very complicated. Even though there is study to reduce the number of

integrators in the literature [2], the reduction in power consumption is minimal while the SD ADC becomes very complex. Therefore, the order of the ADC, the resolution of the quantizer and the OSR have to be optimized to attain low power consumption.

The FoM formulated in (1.4) combines the speed, power consumption, and resolution providing a measure to evaluate various ADCs against each other. FoM value is very low if the ADC has low power consumption. However, an ADC usually has an even lower FoM if it has a higher SNR which means it is not possible to make a fair comparison between two ADCs with different SNR values. FoM, on the other hand, is effective in comparing two ADCs with similar SNR values. Table 1.1 provides a comparison of the ADC performances with different values of *L, OSR* and *n* by using (1.2) and (1.4).

$$FoM = \frac{Power}{2BW \times 2^{ENOB}} \tag{1.4}$$

Table 1.1. Comparison of the SD ADC performances with different *L*, *OSR* and *n*.

L	*OSR*	*n*	SNR [dB]	ENOB	Power required to achieve FoM=10 fJ/conv [µW]	Power required to achieve FoM=50 fJ/conv [µW]	Power required to achieve FoM=100 fJ/conv [µW]
2	32	3	76.15	12.36	2.62	13.12	26.25
2	32	4	82.17	13.36	5.25	26.25	52.50
2	32	5	88.19	14.36	10.50	52.50	104.99
2	64	1	79.16	12.86	3.71	18.56	37.12
2	64	2	85.18	13.86	7.42	37.12	74.24
2	64	3	91.20	14.86	14.85	74.24	148.48
2	128	1	94.21	15.36	21.00	104.99	209.98
3	16	3	76.70	12.45	2.80	13.98	27.96
3	32	1	85.73	13.95	7.91	39.54	79.09
3	32	2	91.75	14.95	15.82	79.09	158.17
3	32	3	97.77	15.95	31.63	158.17	316.34
3	64	1	106.80	17.45	89.47	447.37	894.75
4	16	3	91.93	14.98	16.15	80.73	161.47
4	32	1	106.98	17.48	91.34	456.71	913.41

SNR is very important in ADC design. The SD ADC should have a high enough SNR for the application that it is intended for. It is difficult to calculate SNR in DT applications. Normally, digital outputs for each clock cycle are obtained after long transient simulations.

These digital outputs are used in a MATLAB code to find the FFT response of the ADC for different frequencies. FFT operation requires the output to contain a number to the power of 2 clock cycle length samples. Also, a large number of samples should be chosen if the OSR is also large. When more samples are taken, the degree of accuracy in the results are improved up to a point. Therefore, this number is usually chosen as 512 or 1024 times the OSR. The output of the FFT will show the power spectrum of the ADC output from very low frequencies up to half of the sampling frequency. If the output of the ADC contains an input signal at a specific frequency, the FFT simulation will contain that signal in which the power of the signal is calculated. Afterwards, each individual power at the frequency within the band of interest is added up. The power of the noise in the bandwidth is calculated by subtracting the signal power from the total power in the bandwidth. The ratio of the signal power and the noise power gives us the signal to noise and distortion ratio (SNDR) of the ADC. Since, the noise power contains the power of harmonics here, SNDR is smaller than SNR and useful to observe the effects of harmonics.

Moreover, SNR is affected not only by the quantization noise but also other noise sources. The other dominant noise sources are the *kT/C* noise caused by the switching capacitances in the 1st integrator and the noise of the opamp used in the integrator. There might be further effects from some of the components in the design such as non-linear gain of the opamps and DAC non-linearity which can cause harmonics. In particular, if there is non-linearity in the ADC, the FFT response will contain the reflections of the input signal at multiple times the frequency of the signal which are called harmonics. If the harmonics have very low power according to the FFT result, they are tolerable. Normally, the 3rd harmonic is the dominant harmonic because even harmonics are cancelled due to fully differential design. Furthermore, the 5th or higher harmonics are generally very small and ignorable compared to the 3rd harmonic. SNDR includes the effects of the harmonics in addition to other noise sources. Therefore, SNDR is used instead of SNR to find ENOB, so that the performance is measured more effectively. Since the bandwidth is chosen as 25 kHz in all designs in this thesis, all analog test inputs are at 7 kHz to observe the effect of the third harmonic clearly in the ADC.

The noise at the higher frequencies will be removed via a digital filter to obtain a clean analog to digital conversion. The digital filter must have higher order to fulfil the

required noise shaping effects. Also, the ratio of the data output frequency of the digital filter and the sampling frequency is usually a number to the power of 2. Moreover, FFT operation which requires a sample size that is a number to the power of 2, is needed to measure the signal to noise ratio (SNR) in the bandwidth. As a result, the OSR of the modulator is generally chosen as a power of 2.

This thesis will focus on design methods of low power SD ADCs for the applications in audio frequencies with high resolution. The aim of this thesis is to obtain analog to digital conversion for the signals audio frequencies with high resolution and low power consumption. The desired resolutions of the ADCs in the thesis are generally 12-15 bits with the bandwidth up to 25 kHz. Chapter 2 includes a series of DT SD ADCs with different transfer functions and structures. Chapter 3 will focus on CT SD ADCs. Chapter 4 includes the hybrid design of SD ADCs. Chapter 5 summarizes the test of the ICs sent to production that contain the designs introduced in the thesis. Chapter 6 will offer a comparison of the designed ADCs in the thesis as well as the conclusion.

2. DISCRETE TIME SIGMA DELTA ANALOG DIGITAL CONVERSION

DT SD ADCs are the most common type of SD ADCs as documented by the numerous DT SD ADC designs in the literature. The main advantage of using a DT SD ADC is the ease of calculation and implementation of STF and NTF in *z*-domain. A delayed integrator can be designed as in Figure 2.1 for a transfer function of (2.1) in *z*-domain. Here, *A* is the input, *B* is the DAC reference, V_{cm} is the virtual ground, and *D* is the output. The inverted versions of these signals are also assumed to be present. Furthermore, the ratio of the capacitances determines the gain of the integrator. θ_1 and θ_2 are non-overlapping inverted clock signals and θ_{1d} and θ_{2d} are the similar clock signals which rise later and fall earlier than θ_1 and θ_2. In θ_1, the input signal *A* charges the capacitor C_1. In θ_2, the DAC reference signal *B* is subtracted from the signal that was accumulated in the capacitor C_1 and the difference is transferred to the capacitor C_2. For each clock cycle, the difference of the signals (delta) are added and collected at the output (sigma). Also, the output can be used for the following circuit in the next θ_1 clock cycle. Additionally, Figure 2.2 shows the non-delayed integrator in *z*-domain with the transfer function (2.2). This schematic is very similar to the delayed integrator but the clock signals are different. In θ_2, the DAC reference signal *B* charges the capacitor C_1. Then, the input signal is subtracted from the reference voltage and transferred to the output in θ_1. The integration operation is performed in the same clock cycle without any delay.

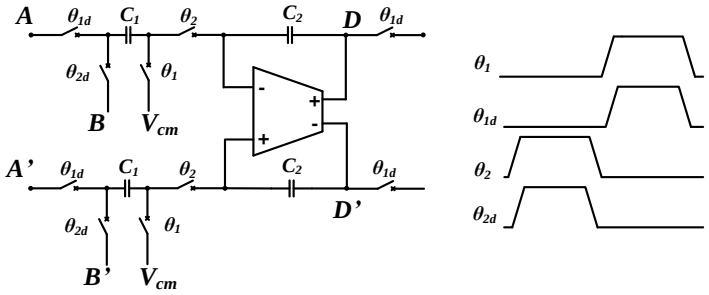

Figure 2.1. Schematic of the delayed integrator.

$$H(z) = \frac{D}{A-B} = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} \tag{2.1}$$

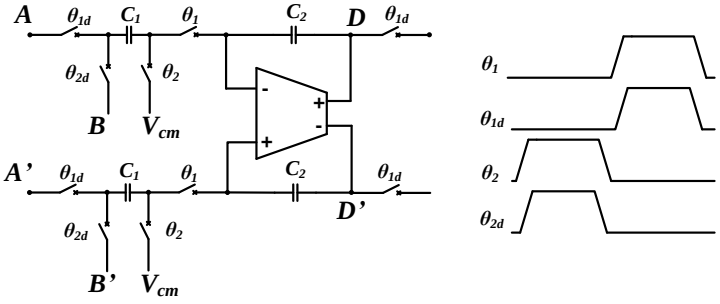

Figure 2.2. Schematic of the non-delayed integrator.

$$H(z) = \frac{D}{A-B} = \frac{C_1}{C_2}\frac{1}{1-z^{-1}} \tag{2.2}$$

A DT SD ADC transfers the input to output directly or with a delay (z^{-k}). However, the quantization noise ε is multiplied with the coefficient $(1-z^{-1})^{L}$, so that the quantization noise is reduced in lower frequencies and increases in higher frequencies. This is called noise shaping. With the help of oversampling, the noise in the desired bandwidth is suppressed, initiating high SNR values. Each additional order of the integrator in the ADC multiplies the noise with $(1-z^{-1})$ so that the noise will be smaller for the desired frequencies. Figure 1.2 shows that it is very difficult to achieve high SNR when the order chosen is 1. Thus, ADCs are generally chosen as second order or higher. However, [3] managed to generate third order noise shaping with two opamps and digital paths while [4] managed to generate third order noise shaping with a single opamp. Power consumption is greatly decreased in these studies even though additional digital circuits are required. Furthermore, inverter-based integration method [5] is an alternative way of obtaining integrators for the DT SD ADCs.

2.1. Second Order DT SD ADC Types

In 2nd order SD ADCs, the quantization noise is shaped by multiplying $(1-z^{-1})^{2}$ via a 2nd order DT filter while the input is transferred to the output of the circuit without any change as seen in (2.3). Here, the input might be the same or delayed by one or two clock cycles. There are many 2nd order DT SD ADC designs in the literature and some of them will be examined in this chapter.

$$Y|_{k=0,1,2} = Xz^{-k} + \varepsilon(1-z^{-1})^2 \tag{2.3}$$

2.1.1. Conventional 2nd Order SD ADC

The conventional 2nd order SD ADC is seen in Figure 2.3. The transfer function of this design is given in (2.4). The input is delayed for two clock cycles at the output and the 2nd order shaping is applied to the noise. (2.5) shows that the first integrator output *U* is dependent not only on the quantization noise ε, but also the input *X*. If a high OSR is selected, the change at the input for each clock cycle will be very small according to the approximation as seen in (2.6). Therefore, $X(1-z^{-1})$ will be omitted because it will be very small. If the quantizer is 1-bit, the value of ε will be very large when the amplitude of the sine wave *X* is much lower than the DAC reference *Y* which leads to high output swings at the output of the first integrator.

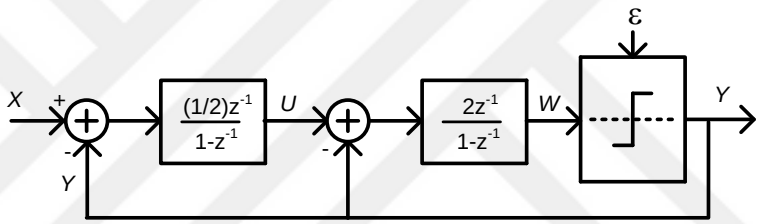

Figure 2.3. Conventional 2nd order SD ADC.

$$Y = Xz^{-2} + \varepsilon(1 - z^{-1})^2 \tag{2.4}$$

$$\begin{aligned} U = \frac{Xz^{-1}}{2}(1 + z^{-1}) - \frac{\varepsilon}{2}(1 - z^{-1})z^{-1} &= \frac{Xz^{-1}}{2}[2 - (1 - z^{-1})] - \frac{\varepsilon}{2}(1 - z^{-1})z^{-1} \\ &\approx Xz^{-1} - \frac{\varepsilon}{2}(1 - z^{-1})z^{-1} \end{aligned} \tag{2.5}$$

$$\begin{aligned} X(1 - z^{-1}) \to X\left[\sin\left(2\pi f_{in}t + \theta + \frac{\pi f_{in}}{f_s}\right) - sin\left(2\pi f_{in}t + \theta - \frac{\pi f_{in}}{f_s}\right)\right] \\ = X\left[\sin(2\pi f_{in}t + \theta) \times cos\left(\frac{\pi f_{in}}{f_s}\right) + cos(2\pi f_{in}t + \theta) \times sin\left(\frac{\pi f_{in}}{f_s}\right)\right. \\ \left. - sin(2\pi f_{in}t + \theta) \times cos\left(\frac{\pi f_{in}}{f_s}\right) + cos(2\pi f_{in}t + \theta) \times sin\left(\frac{\pi f_{in}}{f_s}\right)\right] \\ = X\left[2cos(2\pi f_{in}t + \theta) \times sin\left(\frac{\pi f_{in}}{f_s}\right)\right] \\ \cong X\left[2cos(2\pi f_{in}t + \theta) \times \left(\frac{\pi f_{in}}{f_s}\right)\right] = X\left(\frac{2\pi f_{in}}{f_s}\right)cos(2\pi f_{in}t + \theta) \end{aligned} \tag{2.6}$$

Afterwards, the same ADC is investigated in SIMULINK as seen in Figure 2.4 using the SD toolbox [6] and the behaviour models [7]. Ideally, 2nd order systems would achieve 94.21 dB SNR when OSR is chosen as 128 and the quantizer is 1-bit according to Table 1.1. Next, a sine input with ¼ times the feedback reference amplitude is applied for the system and 80.4 dB SNDR achieved as seen in Figure 2.5. The histogram of the integrator outputs are seen in Figure 2.6. If the input amplitude is increased, SNDR also increases to a certain level. However, the 3rd harmonic appears in the system if the input amplitude is high because large integrator output swings prevent the SNDR become as much as expected.

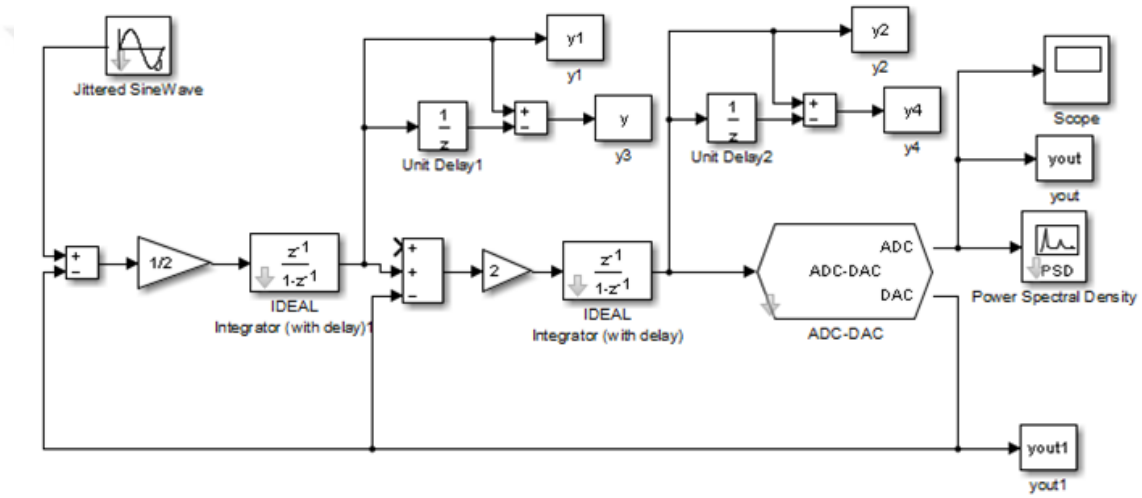

Figure 2.4. SIMULINK diagram of the conventional 2nd order SD ADC.

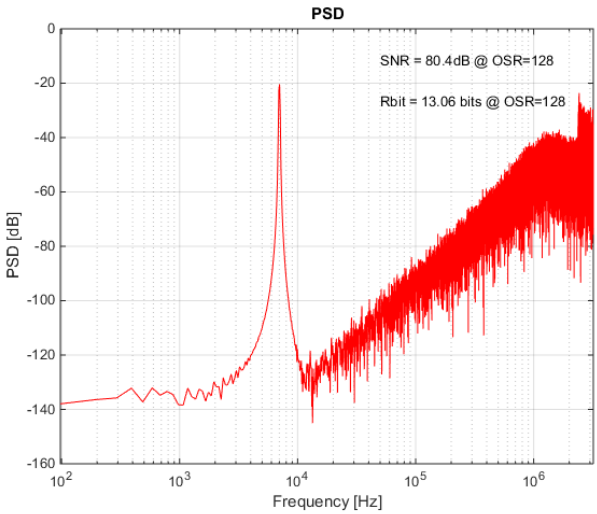

Figure 2.5. FFT of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ¼.

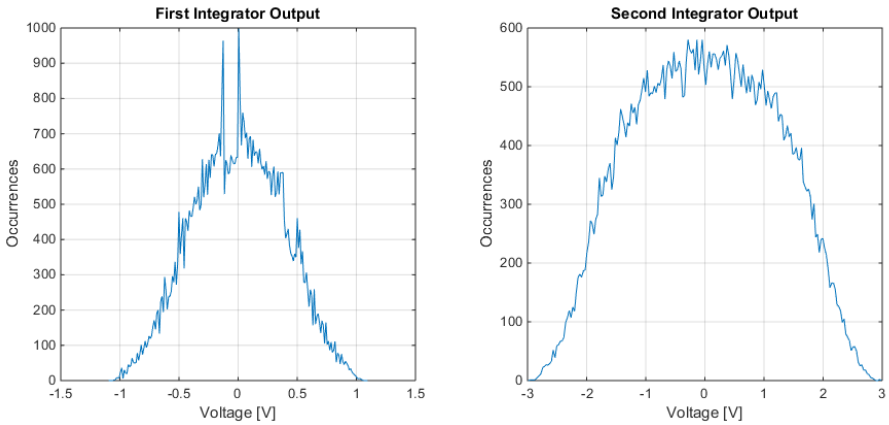

Figure 2.6. Integrator output histograms of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ¼.

Figure 2.7 shows the FFT result of the ADC and Figure 2.8 shows the output histograms of the integrators when input amplitude is ½ times the feedback reference value. As seen, very small 3rd harmonic is present in the system and the integrator output swings are very large according to the histograms. If the input amplitude is increased to ¾ times the reference levels, SNDR decreases significantly due to the 3rd harmonic as seen in Figure 2.9. Moreover, the 5th harmonic is present in the system accompanying an increase in integrator output swings as seen in Figure 2.10. Furthermore, there will be many harmonics in the FFT plots while SNDR dramatically drops as seen in Figure 2.11 if the input amplitude is as large as DAC reference levels. Also, the integrator output swings become quite large as seen in Figure 2.12.

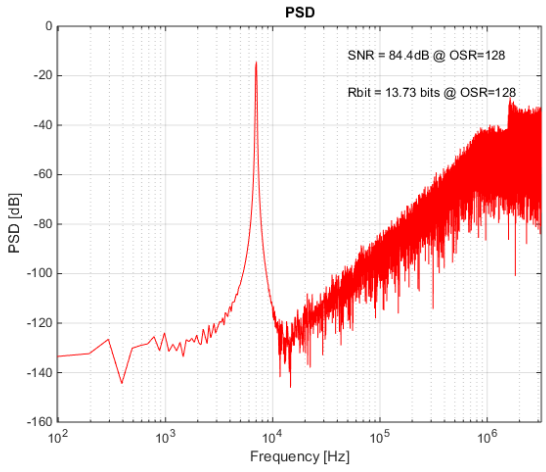

Figure 2.7. FFT of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ½.

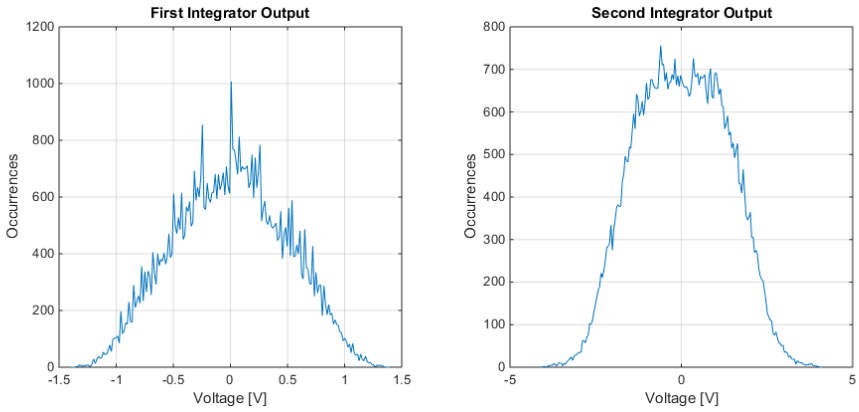

Figure 2.8. Integrator output histograms of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ½.

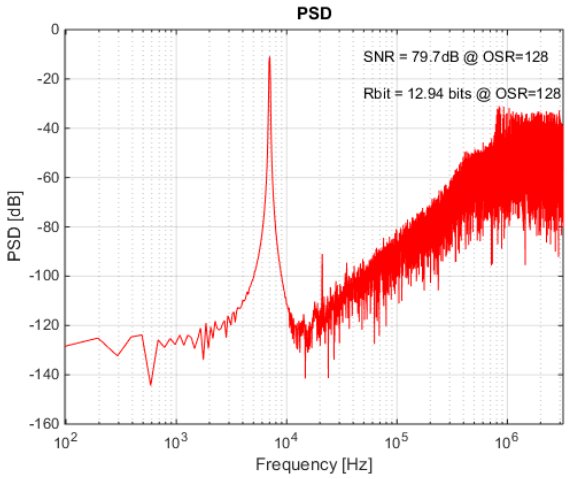

Figure 2.9. FFT of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ¾.

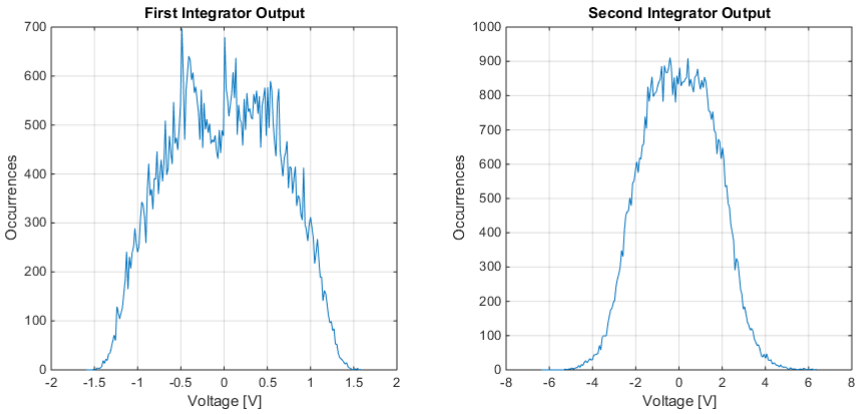

Figure 2.10. Integrator output histograms of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ¾.

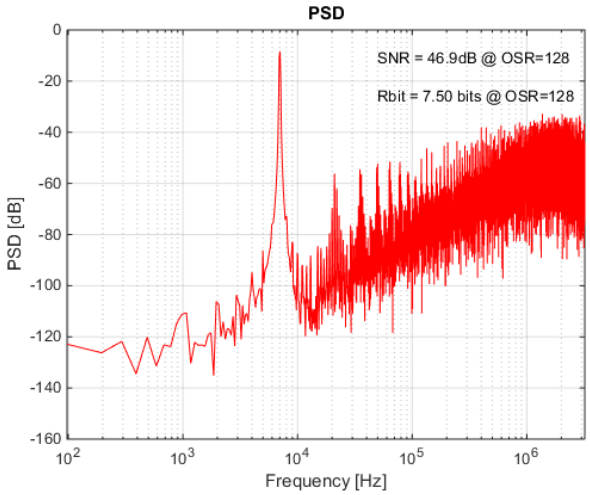

Figure 2.11. FFT of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of 1.

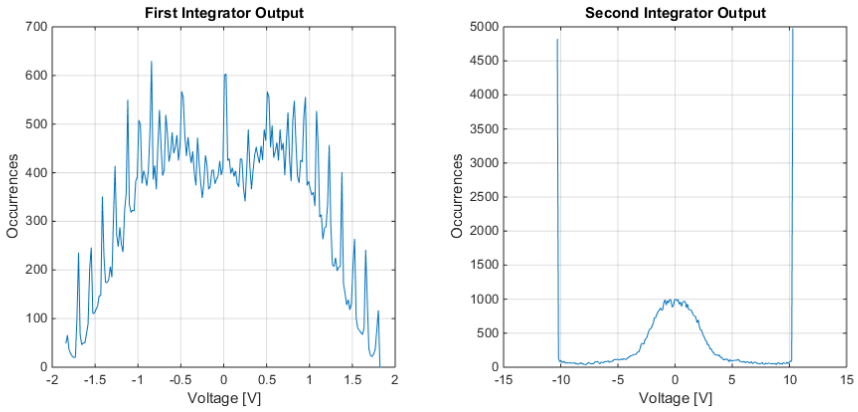

Figure 2.12. Integrator output histograms of the conventional 2nd order SD ADC when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of 1.

According to Table 1.1 , 91.2 dB SNR would be achieved when OSR is chosen as 64 and the quantizer is 3-bits. The SIMULINK diagram in Figure 2.4 is updated according to these parameters. As seen in Figure 2.13, 91.3 dB SNR is achieved when the input amplitude is 0.8 times the reference levels. This value is more than the calculated result because multi-bit quantization allows the input amplitude to be larger as compared to single-bit quantization and to be operated beyond the calculated level. The integrator output histograms in Figure 2.14 show that integrator output swings greatly decrease because of multi-bit quantization. The analog input and the DAC output seen in Figure 2.15 show that the quantization error ε is much lower than that of 1-bit quantization. Each additional bit in the quantizer halves the quantization error and grants 6.02 dB gain in SNR.

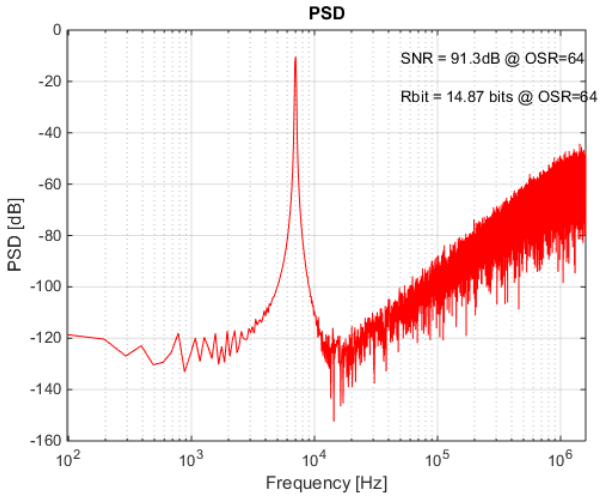

Figure 2.13. FFT of the conventional 2nd order SD ADC when OSR is chosen 64 and the quantizer is 3-bit for input amplitude and reference ratio of 0.8.

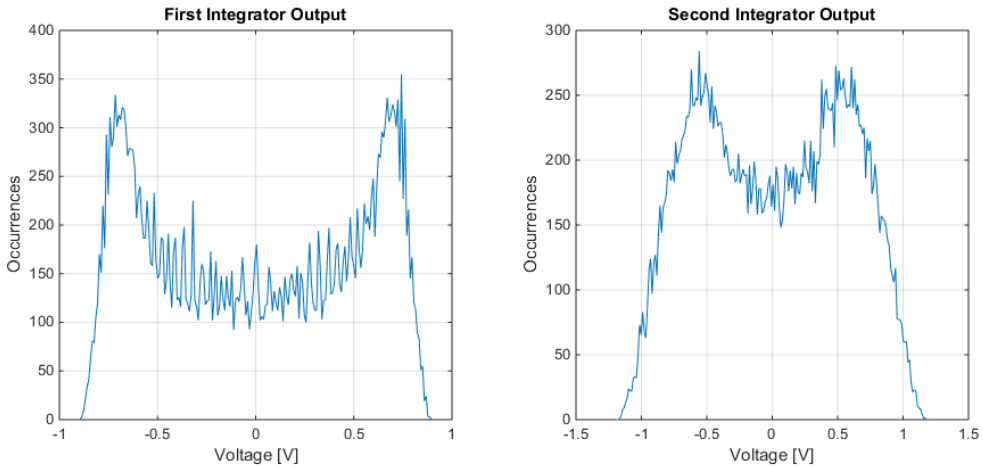

Figure 2.14. Integrator output histograms of the conventional 2nd order SD ADC when OSR is chosen 64 and the quantizer is 3-bit for input amplitude and reference ratio of 0.8.

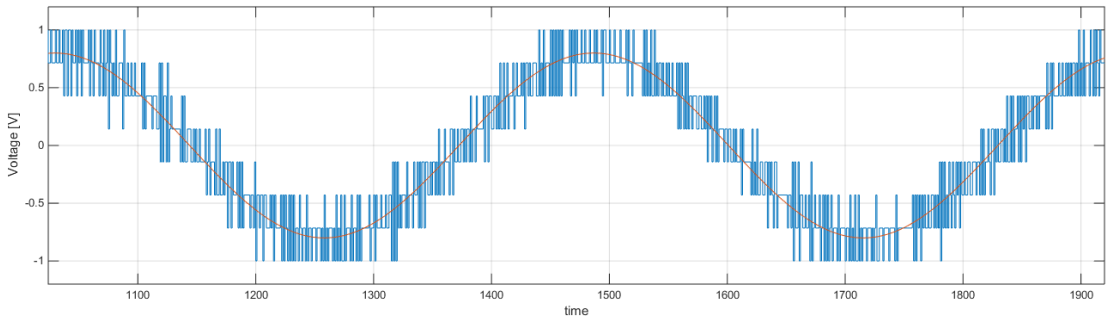

Figure 2.15. The input and the DAC output of the conventional 2nd order SD ADC when OSR is chosen 64 and the quantizer is 3-bit for input amplitude and reference ratio of 0.8.

2.1.2. Feed-Forward Path in Conventional 2nd Order SD ADC

Although the output swings are reduced significantly with multi-bit quantization in the conventional 2nd order SD ADC, the integrator outputs are still large because it is dependent on the input *X*. Therefore, [8] suggested using a feed-forward path as seen in Figure 2.16 to reduce the swing at the first integrator output. By using a feed-forward path, the new transfer function becomes (2.7). The output contains not only the input and the shaped quantization noise, but also the change at the input. The change at the input is not critical for high OSR values and can be neglected. However, the first integrator output is no longer dependent on the input *X* as seen in (2.8). Now, it is dependent on the change at the input which is small. The system is simulated in SIMULINK as in Figure 2.17 to verify this behaviour. First, the OSR is chosen 128 and the quantizer is 1-bit. Figure 2.18 shows that the ADC has the same SNDR when the input is half the DAC references. Nevertheless, the output swing of the first integrator depicted in Figure 2.19 is greatly reduced as compared to the previous design. Afterwards, the OSR is decreased to 64 while the quantizer is increased to 3-bits. Figure 2.20 shows the FFT results of the updated ADC when the input is 0.8 times the DAC reference. A reduction in SNDR from 91.3 dB to 90.3 dB can be observed, probably due to undesired terms in the transfer function as given in (2.7) but the first integrator swing has become very low as depicted in Figure 2.21.

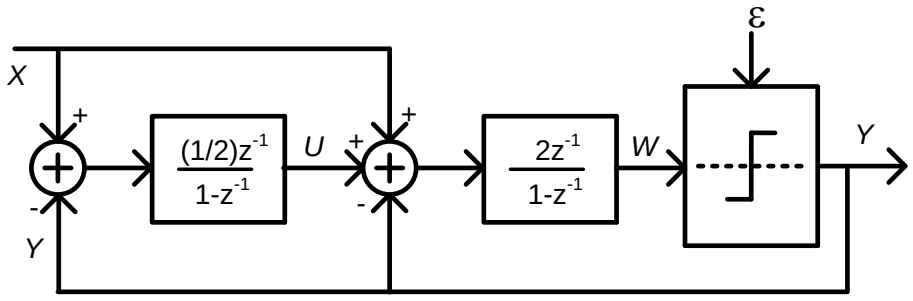

Figure 2.16. Using feed-forward path in conventional SD ADC.

$$Y = Xz^{-1} + Xz^{-1}(1 - z^{-1}) + \varepsilon(1 - z^{-1})^2 \tag{2.7}$$

$$U = \frac{1}{2}Xz^{-1}(1 - z^{-1}) + \frac{1}{2}\varepsilon z^{-1}(1 - z^{-1}) \tag{2.8}$$

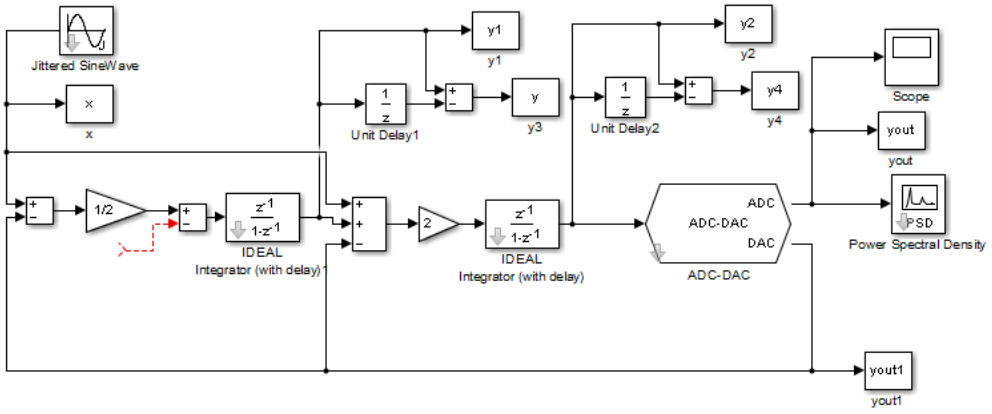

Figure 2.17. 2nd order SD ADC with feed-forward path in SIMULINK.

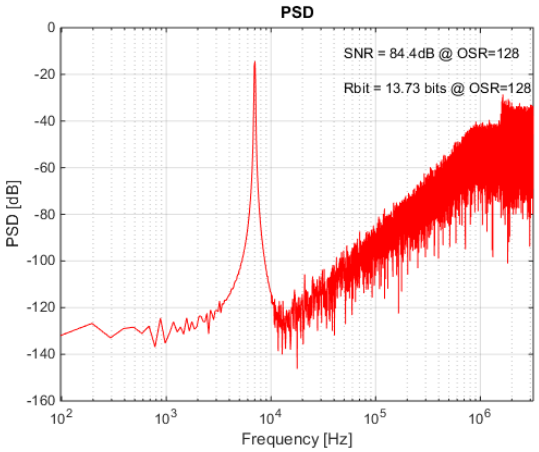

Figure 2.18. FFT of the 2nd order SD ADC with feed-forward path when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ½.

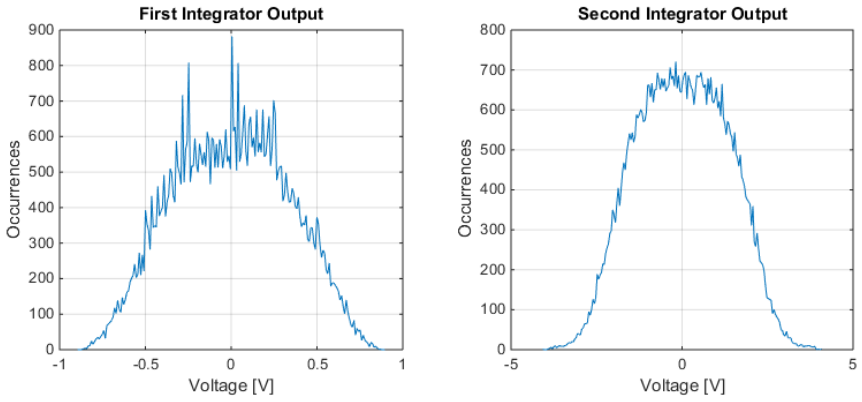

Figure 2.19. Integrator output histograms of the 2nd order SD ADC with feed-forward path when OSR is chosen 128 and the quantizer is 1-bit for input amplitude and reference ratio of ½.

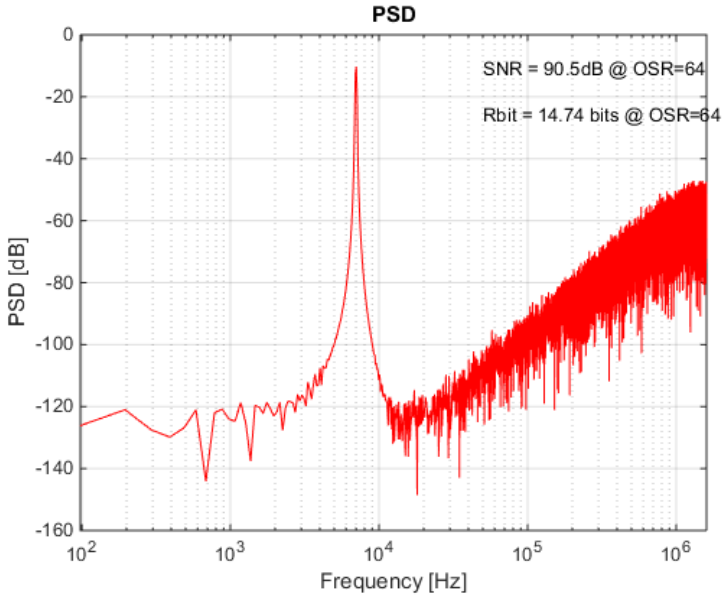

Figure 2.20. FFT of the 2nd order 3-bit SD ADC with feed-forward path when OSR is 64 for input amplitude and reference ratio of 0.8.

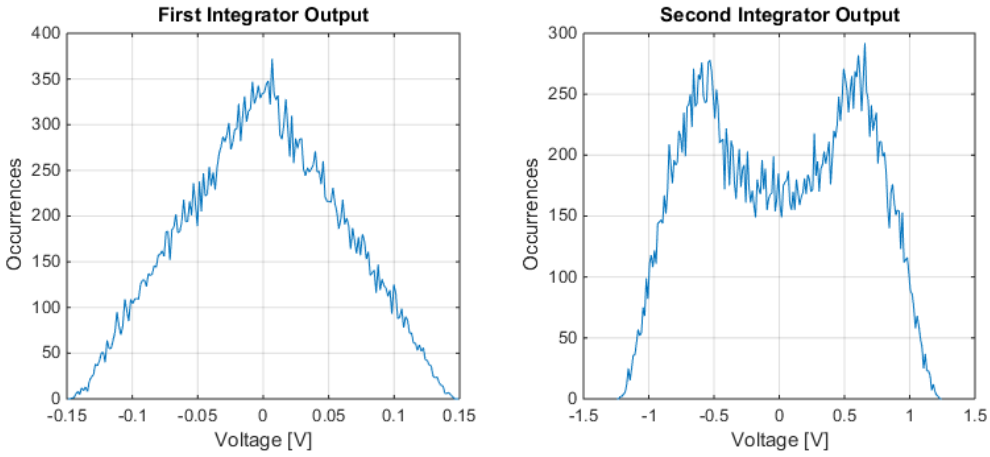

Figure 2.21. Integrator output histograms of the 2nd order 3-bit SD ADC with feed-forward path when OSR is 64 for input amplitude and reference ratio of 0.8.

Feed-forward paths and multi-bit quantization greatly decreased the first integrator output swings. Hence, the opamps in the integrators no longer require high output swing and simple opamps can be used in the integrators. Moreover, gains of opamps generally changes with the output voltage because transistors are non-linear devices. This non-linearity causes additional noise and it can be more effective than quantization noise or *kT/C* noise when the output swings are very large. The 2nd integrator output swings are still large but they can be lowered by reducing the coefficient of the 2nd integrator.

When the quantizer is 1-bit, the differential outputs are be compared with each other. Thus, attenuating the quantizer inputs by reducing the coefficient has no negative effect other than increasing the effect of the opamp output noise. If the opamp output noise is still much smaller than the quantization noise, the attenuation is acceptable. However, the output signals will be compared with each other and additional reference levels if the quantizer is multi-bit. Hence, the reference levels should be attenuated proportionally to the integrator outputs. In addition, the 1st integrator output can be reduced even further by reducing the 1st integrator coefficient and decreasing the coefficient of the DAC references in the 2nd integrator. Thus, Figure 2.16 can be updated as Figure 2.22, where OSR is selected as 128 for 1-bit quantization. The SIMULINK version is also updated to that in Figure 2.23 and the FFT result in Figure 2.24 is the same as the result in Figure 2.18. Nevertheless, the 1st integrator output swing in Figure 2.25 is reduced to 25% of that in Figure 2.19 and the 2nd integrator output swing in Figure 2.25 is reduced to 12.5% of that in Figure 2.19.

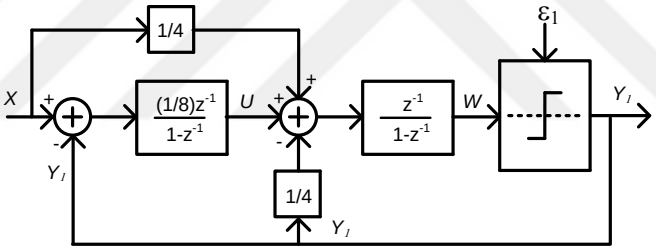

Figure 2.22. SD ADC with feed-forward path and reduced coefficients.

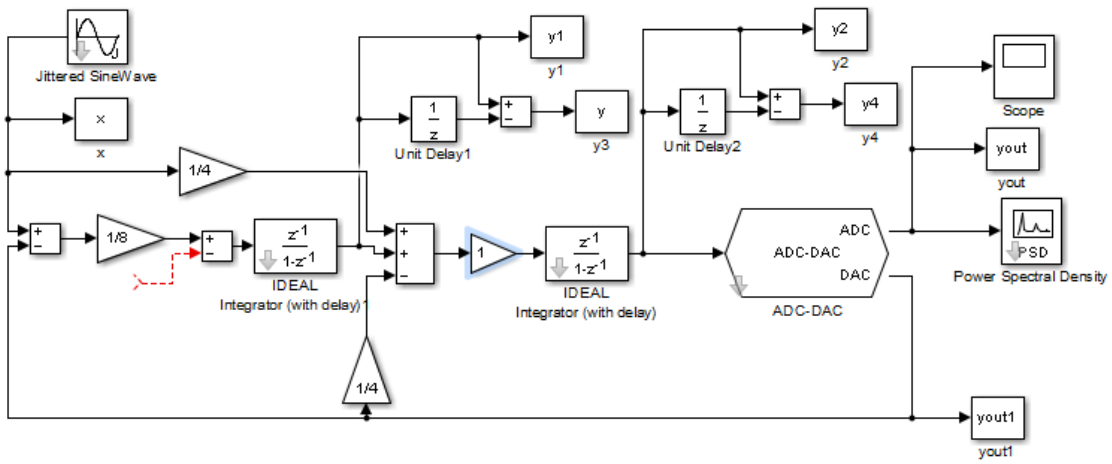

Figure 2.23. SIMULINK diagram of the SD ADC with feed-forward path and reduced coefficients.

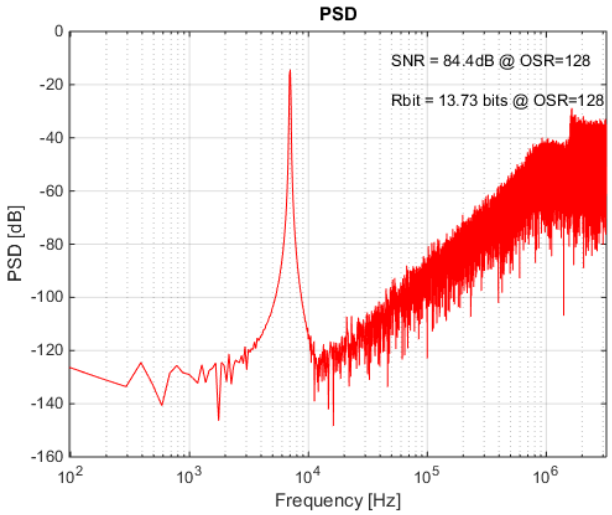

Figure 2.24. FFT of the SD ADC with feed-forward path and reduced coefficients.

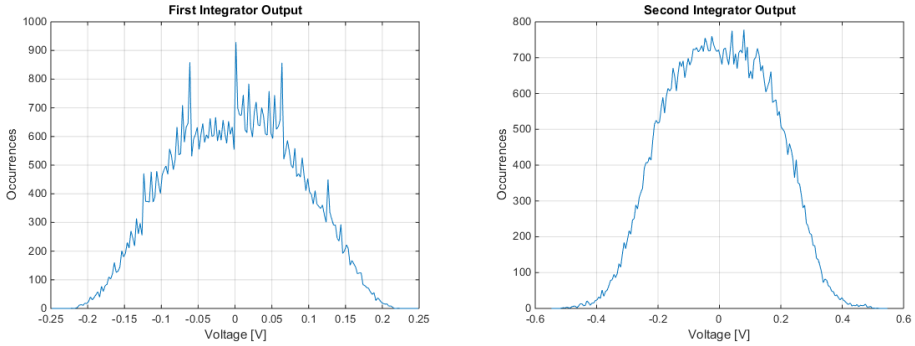

Figure 2.25. Integrator output histograms of the SD ADC with feed-forward path and reduced coefficients.

Feed-forwards paths and lower coefficients significantly reduce the integrator output swings. If the output swings of the integrators are large, opamps in the integrators need to have high slew rate to charge the capacitor correctly during switching. Also, gains of opamps usually change with the instantaneous output voltage. This error is generally negligibly small as long as the output transistors are still in the desired operating regions or the output swing is kept within certain limits. Thus, simpler opamps can be used when the integrator output swings are low. Moreover, the DAC voltage references can be used as supply voltage or ground and the input amplitude can be large as the integrator outputs are low. This is due to the fact that the input signal voltage can be up to 80% of the DAC outputs without hurting the output swing. If the signal amplitude increases, the ratio of the signal to the noise sources other than quantization noise also increases, thus resulting in higher analog to digital conversion performance.

Feed-forward paths are usually applied as seen in Figure 2.26 [9]. The proposed structure in Figure 2.27 is a simpler method of applying the same feed-forward path to the input of the previous integrator instead of the output to perform the transfer function (2.9). The feed-forward path can be achieved by using cross-coupled capacitors. The input signals are transferred to the output with a gain of $-C_1/C_2$ with these capacitors. Here, the switched capacitor structure around C_1 is required for the opamp to operate properly. In both cases, the transfer function will be as in (2.9) and the total load capacitance of the integrator will be approximately the same. However, there will be fewer switches used in the integrators and the effect of the switched capacitor *RC* time constant on the transfer function will be less due to using fewer switches. Moreover, the integrator output will be *U'* instead of *U* as in Figure 2.28 and (2.10) and this method can be used to reduce the output swings of the integrators. Also, adding signals before the integrator would help for some application in which addition operation is critical and difficult to perform. However, this method increases the output swing in the circuit in Figure 2.28 as in (2.10). So, the advantage to lower the output swing is lost but the addition can be performed easier. The first integrator output swing is dependent on the input *X* now and the output swing is increased. The SIMULINK diagram is updated as in Figure 2.29 and the integrator output histograms are obtained as in Figure 2.30. However, this increase in swings is not critical and the transistor level design for this structure is performed.

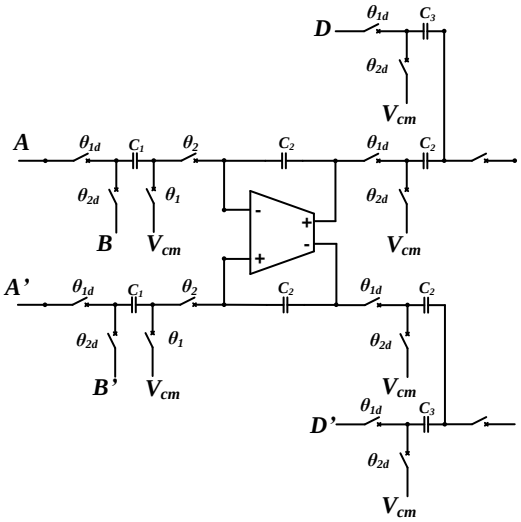

Figure 2.26. Usual feed-forward path application.

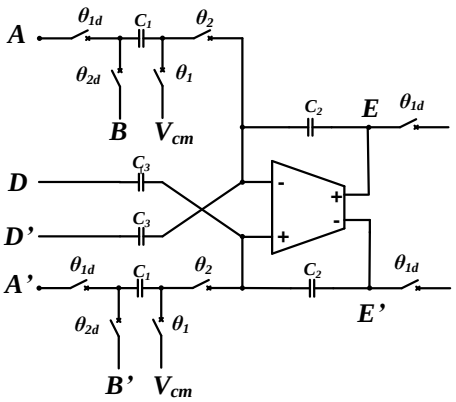

Figure 2.27. Proposed feed-forward path application.

$$E = \frac{C_1}{C_2}(A - B)\frac{z^{-1}}{1 - z^{-1}} + \frac{C_3}{C_2}D \tag{2.9}$$

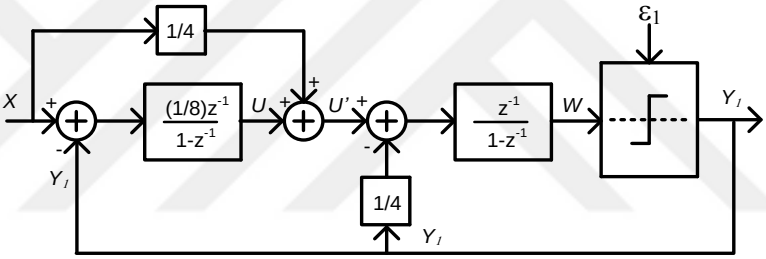

Figure 2.28. Diagram of the proposed feed-forward path method.

$$U' = U + \frac{1}{4}X = \frac{1}{8}X(2 + z^{-1} - z^{-2}) + \frac{1}{8}\varepsilon z^{-1}(1 - z^{-1}) \tag{2.10}$$

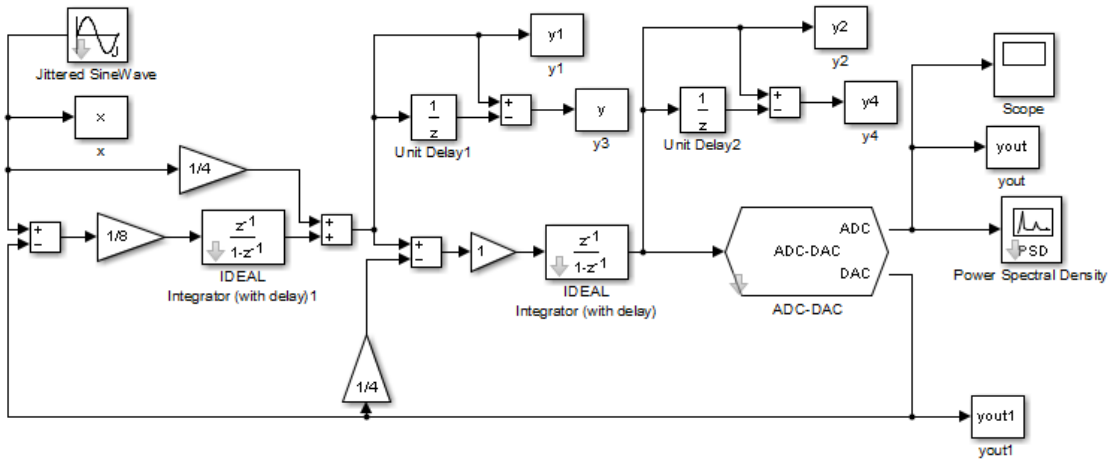

Figure 2.29. SIMULINK diagram of the proposed feed-forward path method.

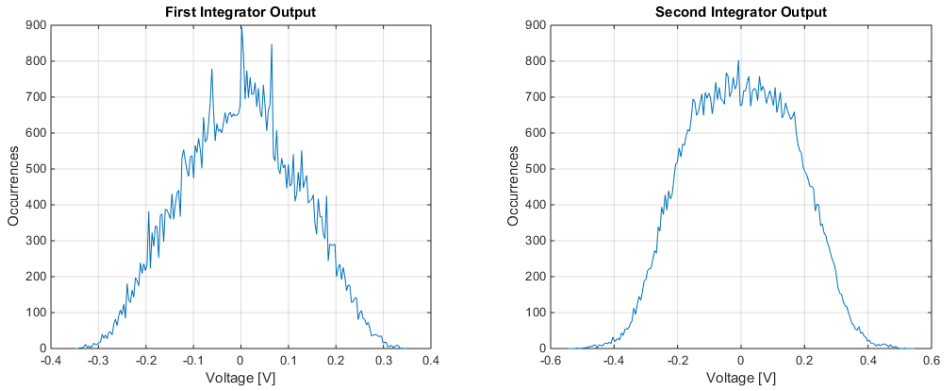

Figure 2.30. Output histograms of the integrators with proposed feed-forward path.

The overall schematic of the proposed feed-forward 2nd order ADC is in Figure 2.31. UMC 130 nm technology is chosen for this design. A capacitive DAC circuit is used in this SD ADC. The capacitances C_1 and C_5 are chosen 100 fF and the other capacitances are calculated according to the coefficients of the integrators. Small coefficients of the first integrator enable employing the supply voltage and ground for DAC references, thereby eliminating extra reference voltages and simplifying the design. The necessary switches are controlled by the comparator output and the clock signal via NAND circuits.

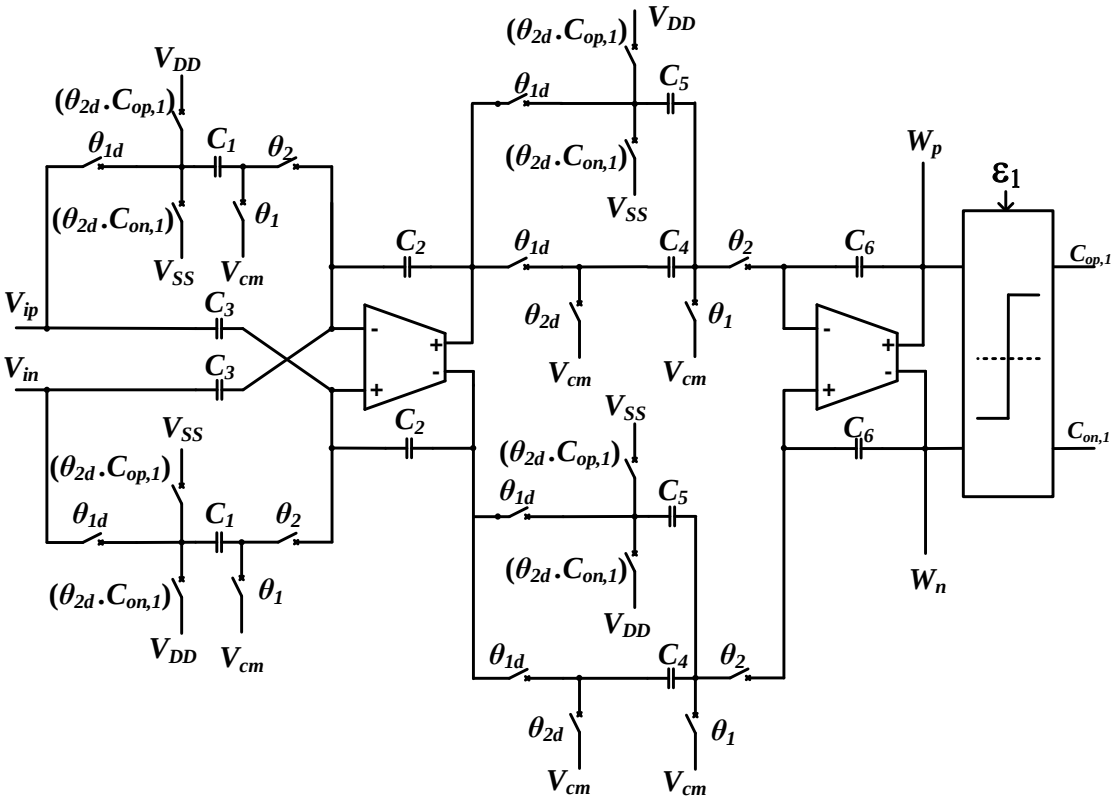

Figure 2.31. Schematic of the proposed 2nd order feed-forward SD ADC.

Generally, using a bootstrapped switch is used [10]. However, two transmission gates following each other as in Figure 2.32 are used as switches here [6]. Transmission gates have lower ON resistances and using another transmission gate with half the size reduces charge injection and clock feedthrough. However, inverted clock signals are required for the control of the switch. Thus, the clock signals θ_1, θ_{1d}, θ_2, θ_{2d} and the inverted versions are produced via a clock distribution circuit as in Figure 2.33. The inverters in the clock distribution circuit cause enough delay for generating the non-overlapping clock signals. The D flip-flop with the schematic in Figure 2.34 at the input halves the signals frequency assuring 50% duty cycle. Therefore, a clock signal with twice the chosen sampling frequency is used as an input. Afterwards, the layout of the clock distribution circuit is prepared as in Figure 2.35.

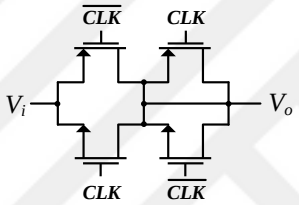

Figure 2.32. Transmission gates used as a switch.

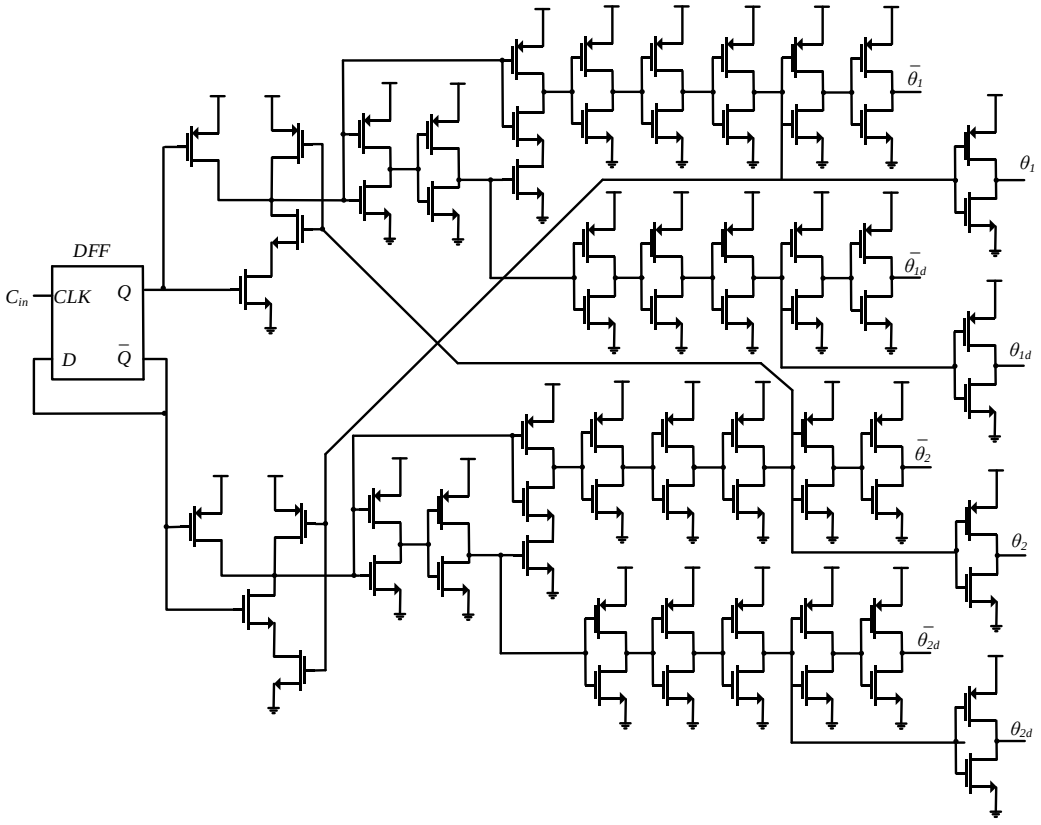

Figure 2.33. Clock distribution circuit.

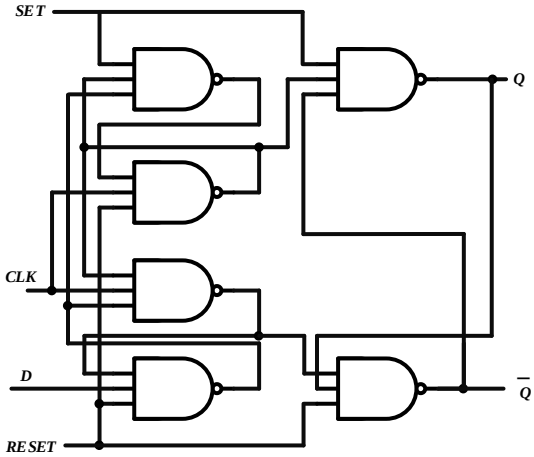

Figure 2.34. D-flip flop circuit with rising edge and set and reset options.

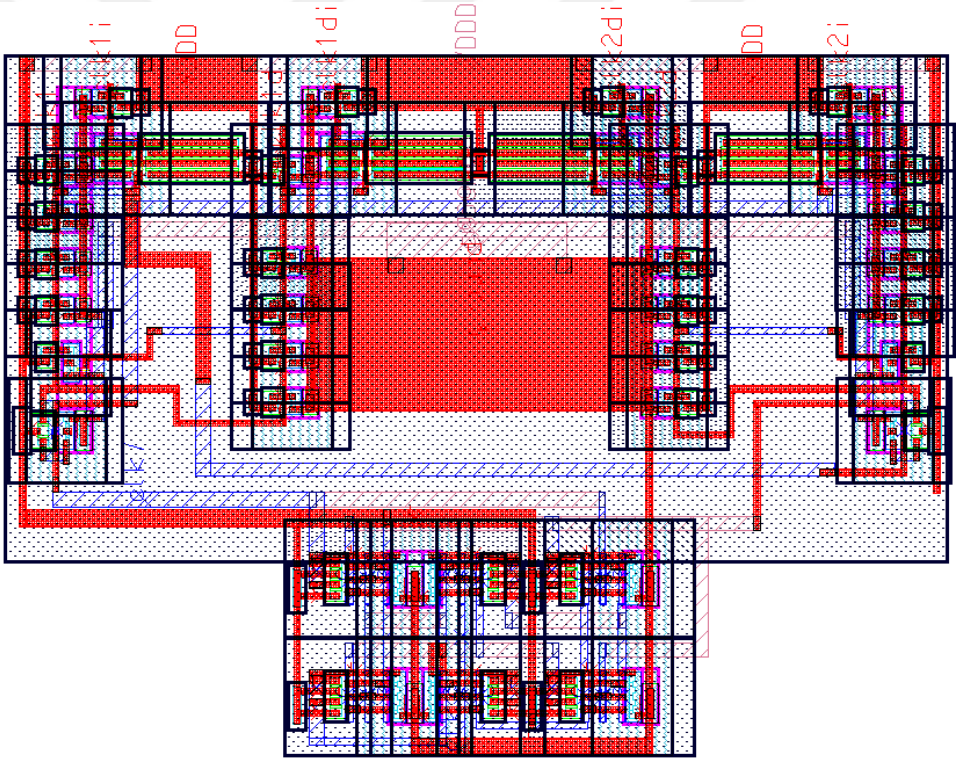

Figure 2.35. Layout of the clock distribution circuit.

A fully differential comparator circuit is needed for the decision and generation of the outputs of the SD ADC. Figure 2.36 shows the designed dynamic comparator with SR latch [11]. When the clock signal is enabled, the comparison is performed and the result is transferred to the latch part. As long as the clock signal is not enabled and the comparator is reset by turning the input transistors off while the data is stored in the latch part. Afterwards, the layout of the comparator is prepared as in Figure 2.37.

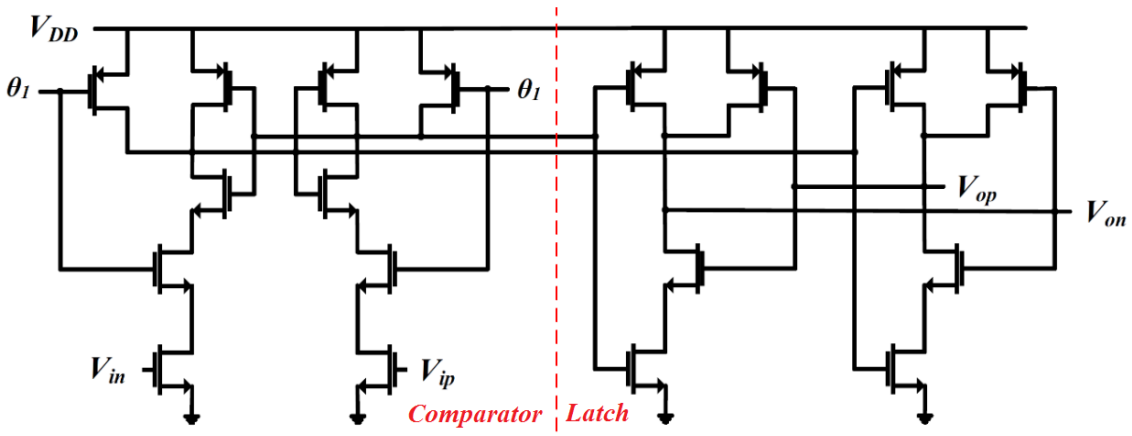

Figure 2.36. Dynamic comparator with SR latch.

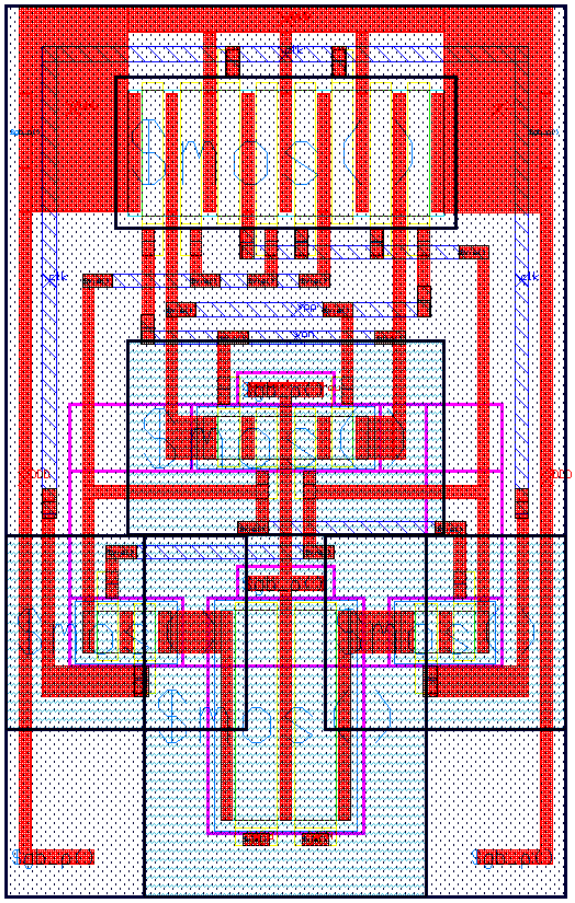

Figure 2.37. Layout of the dynamic comparator with SR latch.

Since the coefficients of the integrators are very low, the output swing of the integrators will also be small. Thus, the proposed architecture allows the use of opamps with lower output swing margins and less linearity. Although, many opamps with adaptive biasing or class AB output stage were investigated in this thesis, it was concluded that these

complicated opamps have instability problems or high power consumption. Since the requirements of the opamps are reduced by the low coefficients of the integrators, the most suitable opamps to be used are the simplest opamps in the literature. A telescopic cascode opamp cannot be chosen because UMC 130 nm technology has 1.2 V supply voltage. Thus, three folded cascode opamps are designed as shown in Figure 2.38 with their specifications in Table 2.1. All of the opamps have 72 dB gain and 500 fF load capacitances are connected to their differential outputs for AC simulations. The layouts of the 1st, 2nd and 3rd opamps are depicted in Figure 2.39, Figure 2.40 and Figure 2.41. The first integrator load capacitance in the ADC is calculated as approximately 720 fF according to (2.11). The opamps in the integrators have to have a gain bandwidth product several times the sampling frequency. According to the AC analysis performances of the designed opamps in Figure 2.42, the 2nd opamp is chosen for the 1st integrator. The load of the 2nd opamp is calculated approximately 300 fF as stated in (2.12). The load capacitance is less than half of the 1st integrator but the output swing of the 2nd integrator is more than the 1st integrator. Thus, 2nd opamp is chosen for the 2nd integrator again.

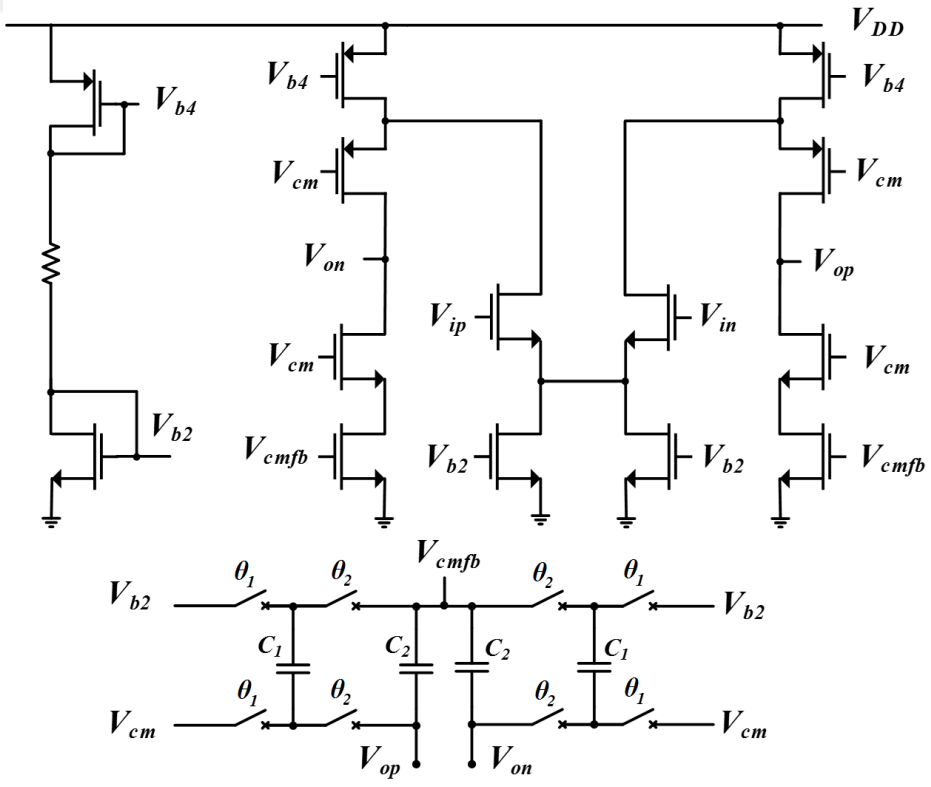

Figure 2.38. The folded cascode opamp topology with switched capacitor CMFB circuit.

Table 2.1. Specifications of the designed folded cascode opamps.

	Folded Cascode Opamp 1	Folded Cascode Opamp 2	Folded Cascode Opamp 3
Gain	72 dB	72 dB	72 dB
Load Capacitance	500 fF	500 fF	500 fF
Gain-Bandwidth Product	8.3 MHz	16.2 MHz	30.5 MHz
Phase Margin	84°	78°	69°
Power Consumption	10.35 µW	20.7 µW	41.4 µW

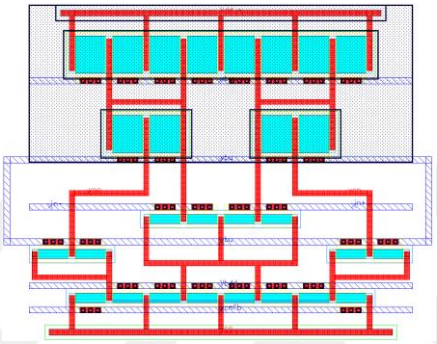

Figure 2.39. Layout of the 1st folded cascode opamp.

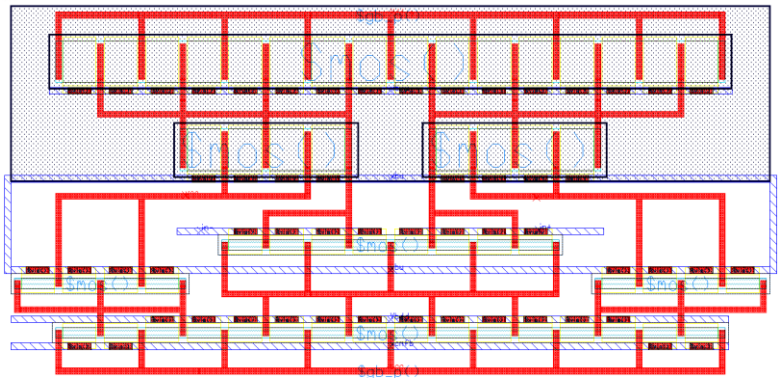

Figure 2.40. Layout of the 2nd folded cascode opamp.

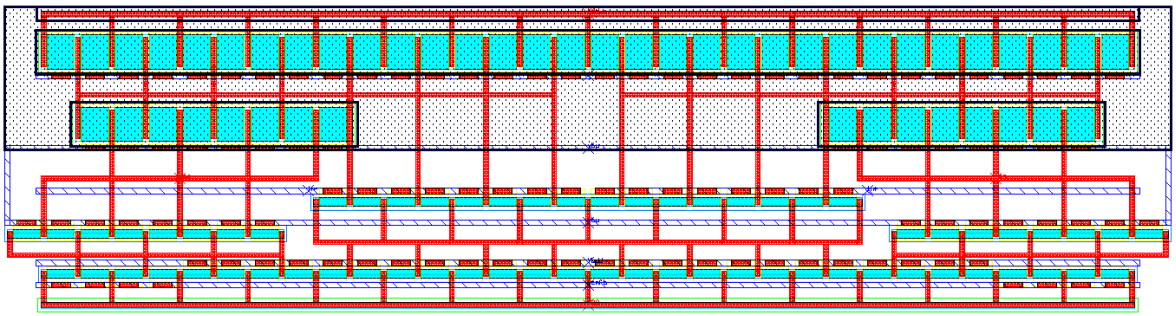

Figure 2.41. Layout of the 3rd folded cascode opamp.

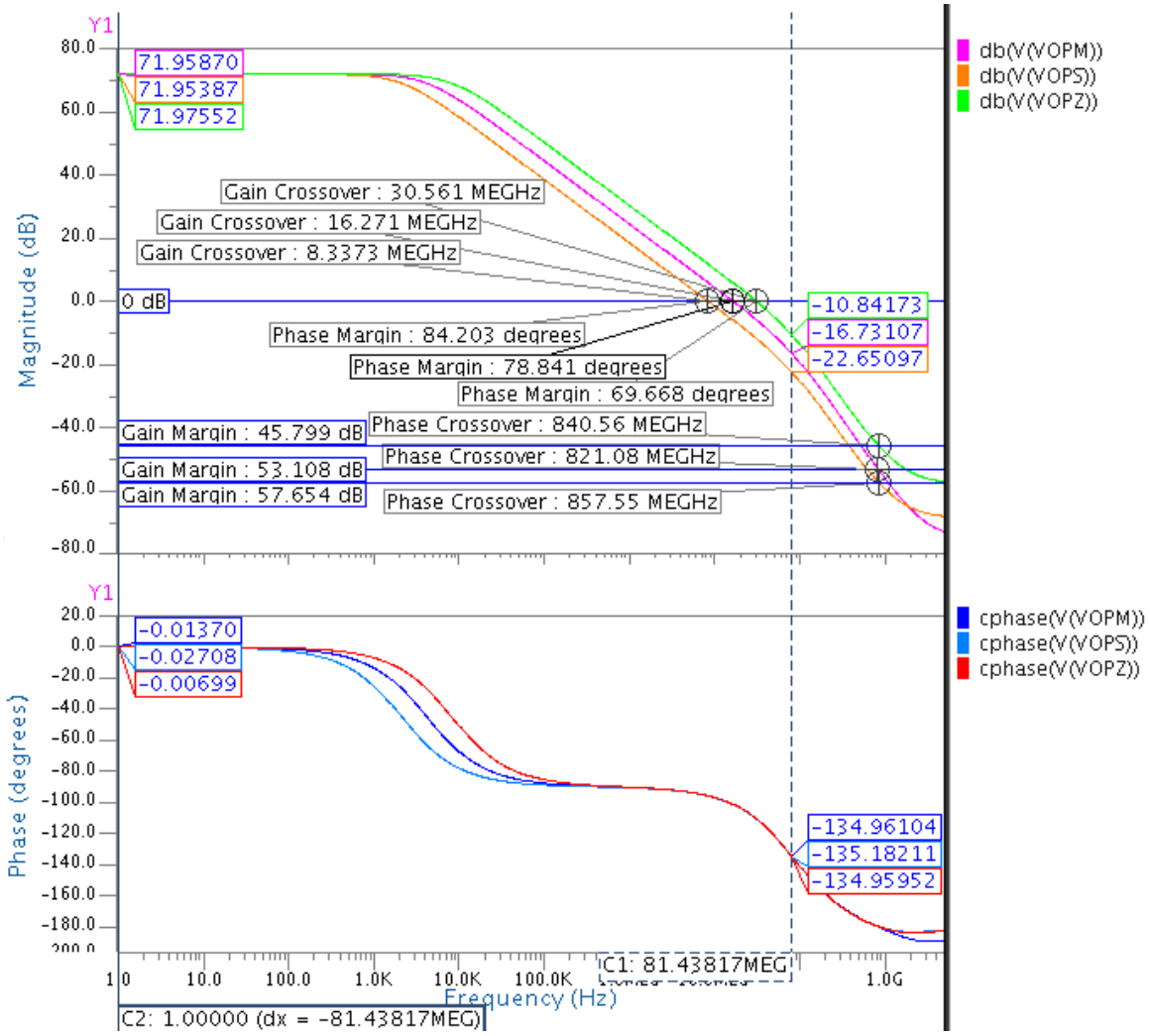

Figure 2.42. The AC analysis performance of the designed opamps.

$$C_{Load,1} \cong C_4 + C_5 + C_{CMFB} + \frac{C_2 \times (C_1 + C_3)}{C_2 + C_1 + C_3} \tag{2.11}$$

$$C_{Load,2} \cong C_{CMFB} + \frac{C_6 \times (C_4 + C_5)}{C_6 + C_4 + C_5} \tag{2.12}$$

The bias part of the folded cascode opamp consumes 2.64 µW power. A single bias circuit is sufficient to bias both opamps. The layout of the bias circuit is depicted in Figure 2.43. Capacitances are connected to the bias nodes V_{b2} and V_{b4} to reduce the noise. Moreover, a switched mode CMFB is also used to adjust the output DC voltage of the opamp [12]. Since the ADC operates in DT, the same clock signals are used for the CMFB circuit. Although the CMFB circuit increases the load of the opamps, it does not consume additional power like other CMFB circuits and it is commonly used in DT ADCs. Furthermore, the layout of the CMFB circuit is prepared as in Figure 2.44.

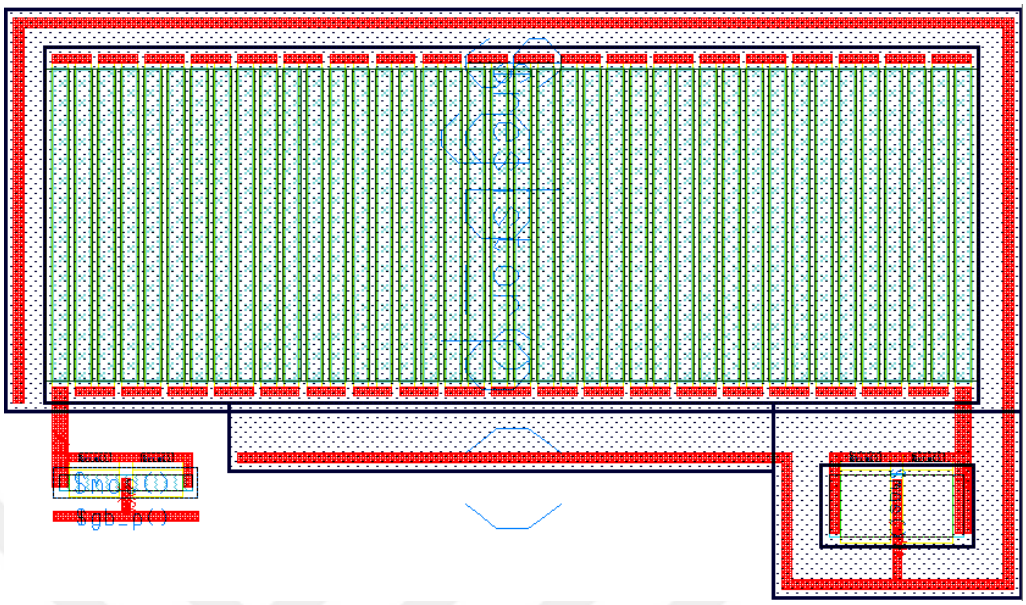

Figure 2.43. Layout of the bias circuit of the folded cascode opamp.

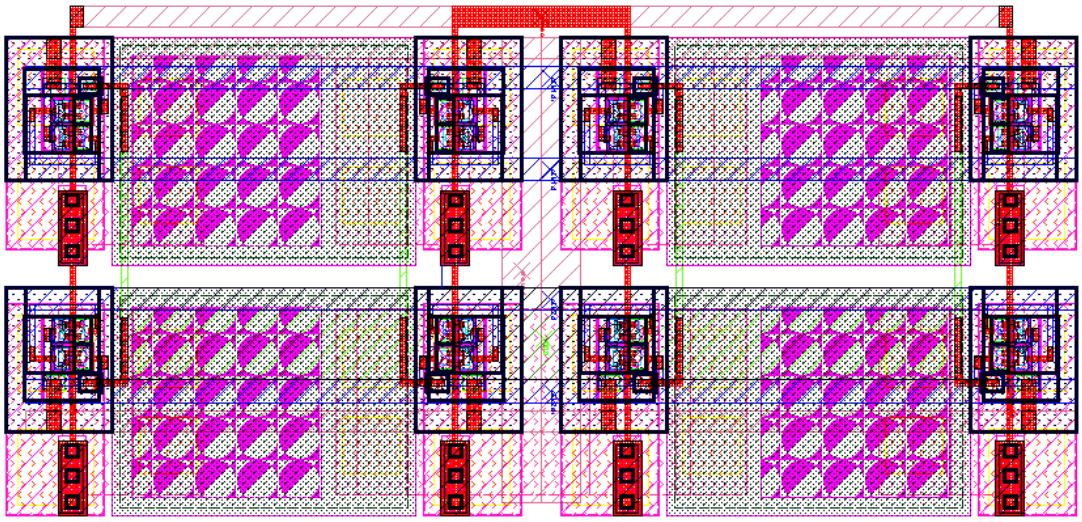

Figure 2.44. Layout of the switched capacitor CMFB circuit.

The overall layout of the ADC is depicted in Figure 2.45. The sampling frequency is chosen as 6.4 MHz procuring 128 OSR when the bandwidth is 25 kHz. Moreover, the inputs of the ADC are 7 kHz differential sine signals. After waiting for the start-up of the ADC for 700 µs, 32768 clock cycles of output data obtained via 5120 µs long transient analysis is transferred to MATLAB. The FFT of the output is depicted in Figure 2.46. Post-layout simulations show that this feed-forward 2nd order DT SD ADC has 72.9 dB SNDR with 54.5 µW power consumption and its FoM is 304 fJ/conv.

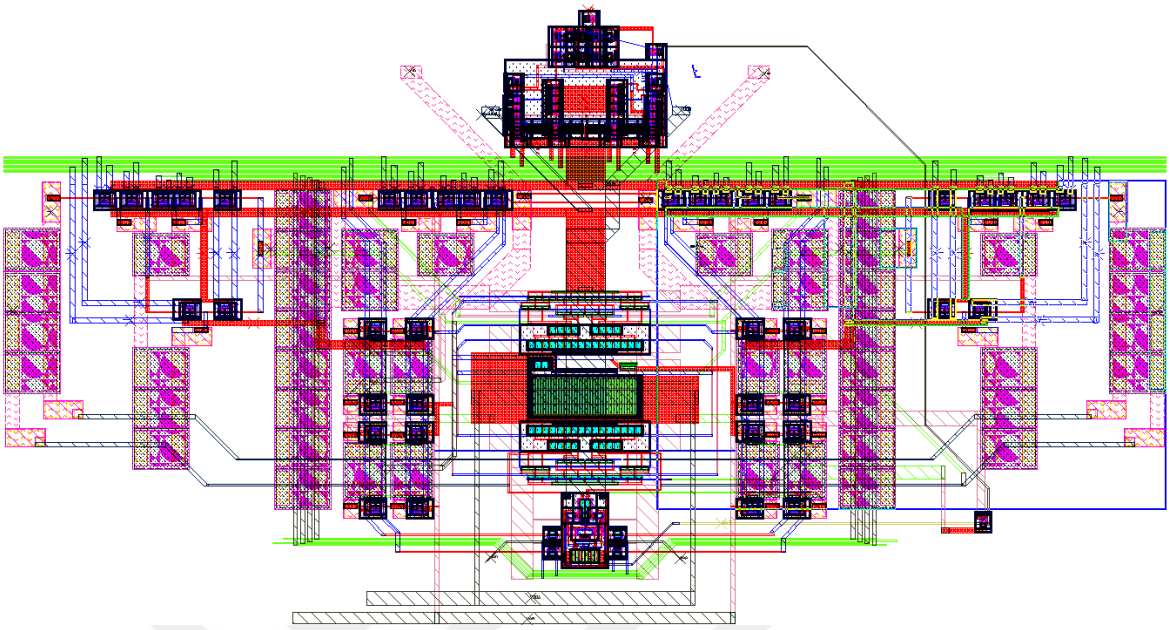

Figure 2.45. The overall layout of the 2nd order feed-forward SD ADC.

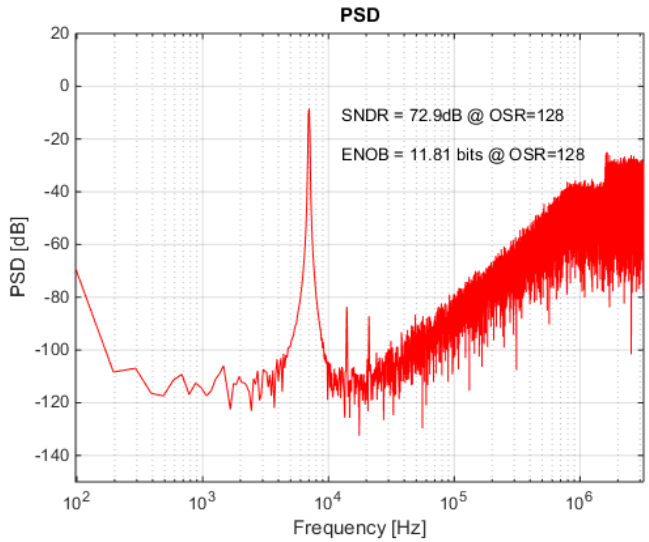

Figure 2.46. Post-layout simulation result of the feed-forward 2nd order DT SD ADC.

2.1.3. Feed-Forward Path Optimization in Conventional 2nd Order SD ADC

The proposed feed-forward path method works well but the integrator output swing can be reduced by adjusting the coefficient of the feed-forward path as in Figure 2.47. When the feed-forward path coefficient is *k*, the transfer function of the ADC becomes (2.13) and the integrator output *U'* becomes (2.14). If the input *X* is assumed to be the same as delayed

version of the input Xz^{-1}, U' is never dependent on k as seen in (2.15) because $X(1-z^{-1})$ is omitted. Thus, the proposed feed-forward method causes the input X to occur at the output of the first integrator for this architecture. Hence, the first integrator output swing cannot be reduced as intended. However, the output as given in (2.16) doesn't contain $X(1-z^{-1})$ when k is 1/8. Hence, the feed-forward ADC is updated with the feed-forward path coefficient reduced to 1/8. This is very easily realised by halving C_3. The new DT SD ADC has similar output histogram and SNR after SIMULINK simulations. However, the capacitive load of the 1st integrator is reduced from 720 fF to 660 fF which provides minor relaxation for the opamp.

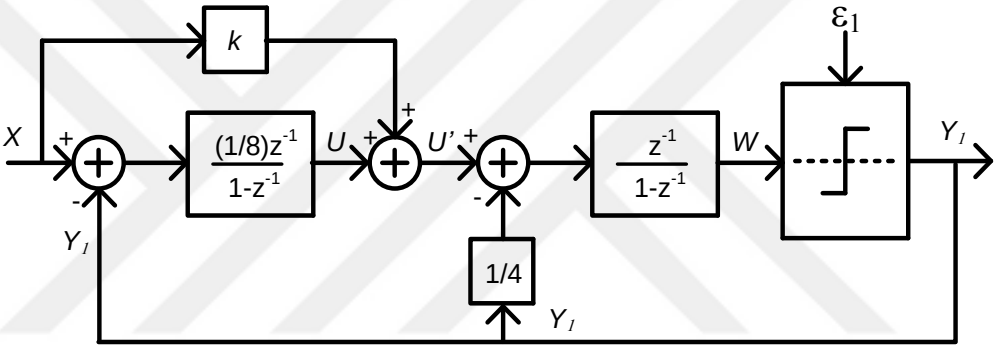

Figure 2.47. Conventional 2nd order SD ADC with feed-forward path coefficient k.

$$Y = 8kXz^{-1} + (1-8k)Xz^{-2} + \varepsilon(1-z^{-1})^2 \tag{2.13}$$

$$U' = X\left[k + \frac{1}{8}z^{-1} + \left(\frac{1}{8} - k\right)z^{-2}\right] + \frac{1}{8}\varepsilon z^{-1}(1-z^{-1}) \tag{2.14}$$

$$If\ Xz^{-2} \cong Xz^{-1} \cong X \rightarrow U' \approx \frac{1}{4}X + \frac{1}{8}\varepsilon z^{-1}(1-z^{-1}) \tag{2.15}$$

$$Y = Xz^{-1} + \varepsilon(1-z^{-1})^2 \tag{2.16}$$

Post-layout simulations show that this 2nd order feed-forward DT SD ADC has 80.3 dB SNDR as in Figure 2.47. The FoM becomes 129 fJ/conv because of 54.5 µW power consumption. Afterwards the prepared layout is sent to production.

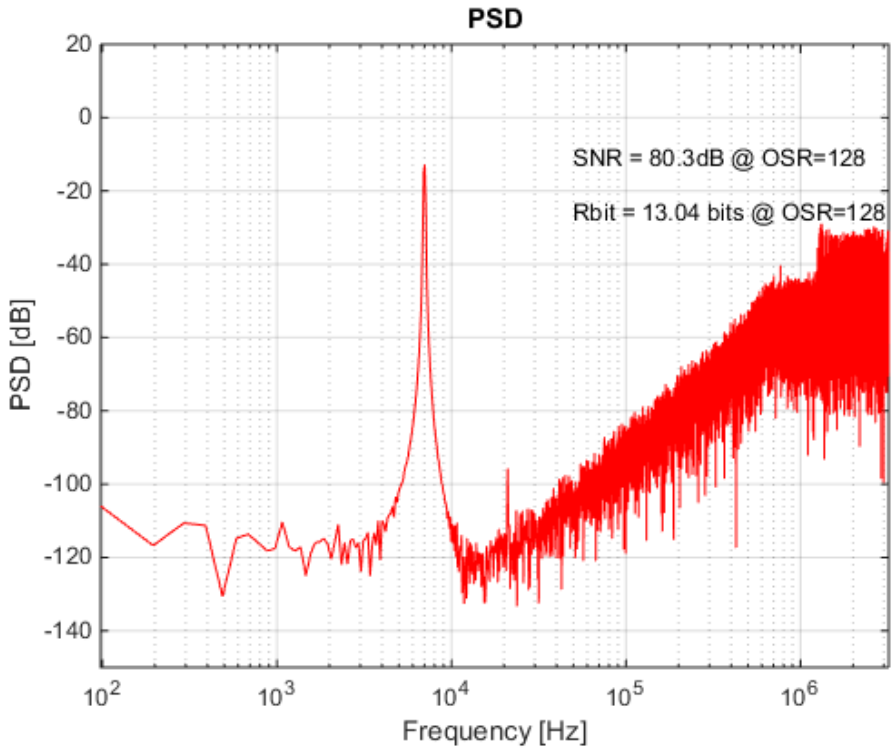

Figure 2.48. Post-layout FFT result of the 2nd order SD ADC.

2.1.4. Multi-bit Feed-Forward SD ADC

The proposed feed-forward method helps to obtain addition operation easier. Thus, the proposed feed-forward path method is extremely suitable for realising the 2nd order feed-forward structure in Figure 2.49 [6]. In this design, the outputs of the integrators are only dependent on the quantization error. The transfer function of the ADC is given in (2.17) and the integrator outputs can be written as (2.18) and (2.19). The proposed feed-forward method makes the 2nd integrator output *W'* as in (2.20) instead of *W*. Thus, the 2nd integrator is still dependent on the input. Multi-bit quantization helps to reduce the 1st integrator output but the new 2nd integrator output will still be high. However, the 2nd integrator coefficient and the feed-forward path coefficients are reduced as in Figure 2.50 to reduce the swing of the 2nd integrator output. Hence, this ADC is designed with 3-bit feedback in SIMULINK as in Figure 2.51 and the output of the ADC is shown in Figure 2.52. Figure 2.53 shows the histograms of the integrator outputs and the quantizer input. The integrator output swings are very low and the same opamps of Figure 2.38 can be used now. Figure 2.54 depicts that the ADC has 91 dB SNR according to the SIMULINK simulations.

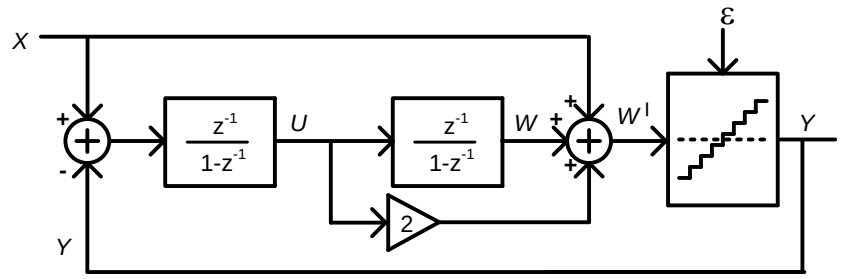

Figure 2.49. The 2nd order feed-forward ADC in [6].

$$Y = X + \varepsilon(1 - z^{-1})^{-2} \tag{2.17}$$

$$U = -\varepsilon z^{-1}(1 - z^{-1}) \tag{2.18}$$

$$W = -\varepsilon z^{-2} \tag{2.19}$$

$$W' = X + \varepsilon(-2z^{-1} - z^{-2}) \tag{2.20}$$

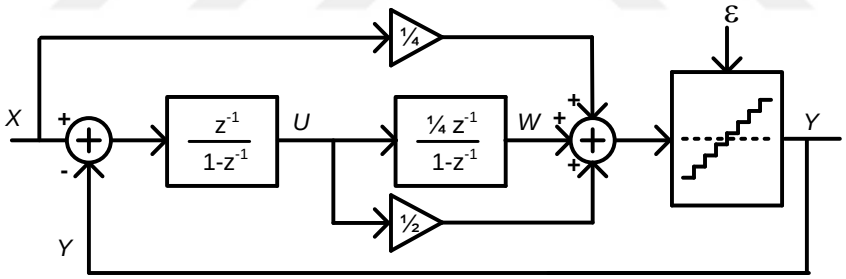

Figure 2.50. The updated version of the 2nd order feed-forward ADC in [6].

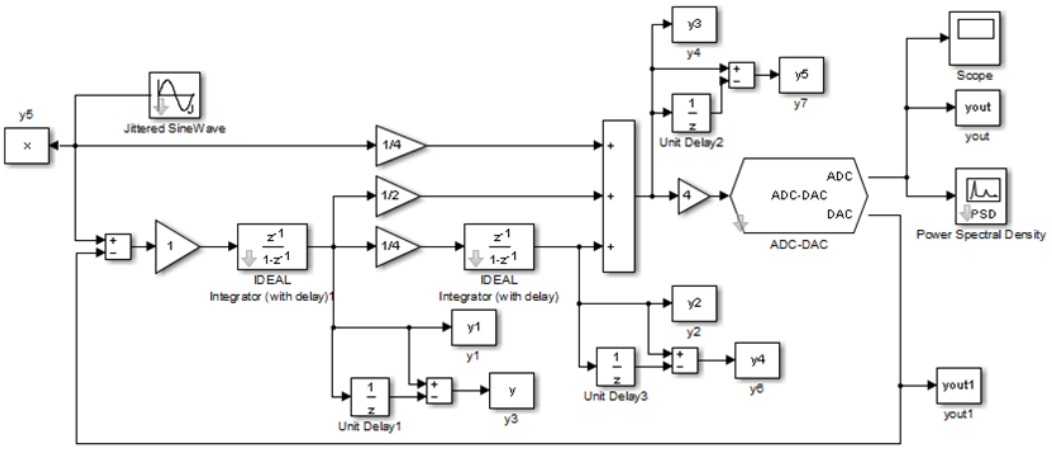

Figure 2.51. The updated 2nd order feed-forward ADC in SIMULINK.

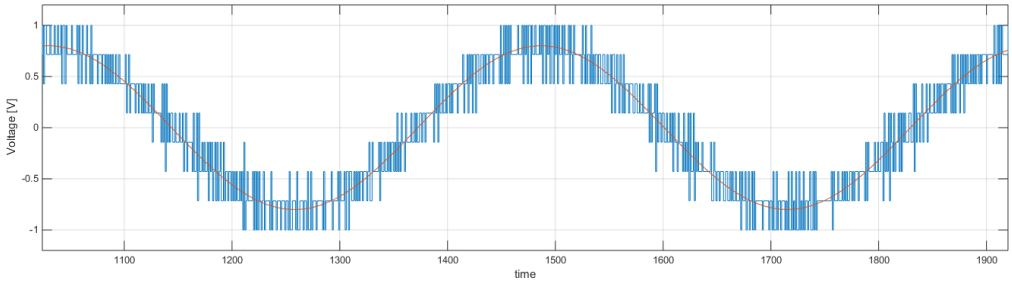

Figure 2.52. The output of the updated 2nd order 3-bit feed-forward ADC in SIMULINK.

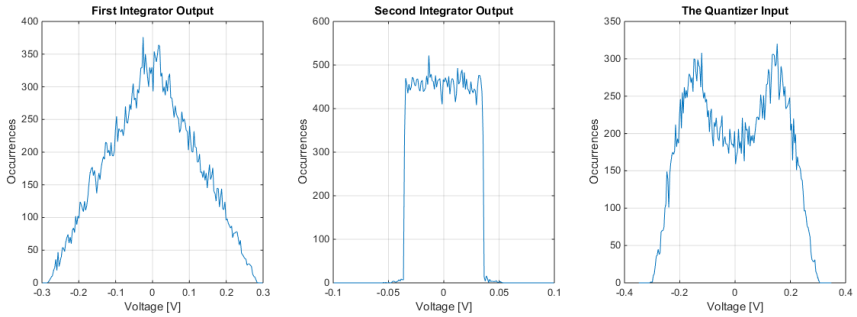

Figure 2.53. The histograms of the integrator outputs and the quantizer input of the updated 2nd order 3-bit feed-forward ADC in SIMULINK.

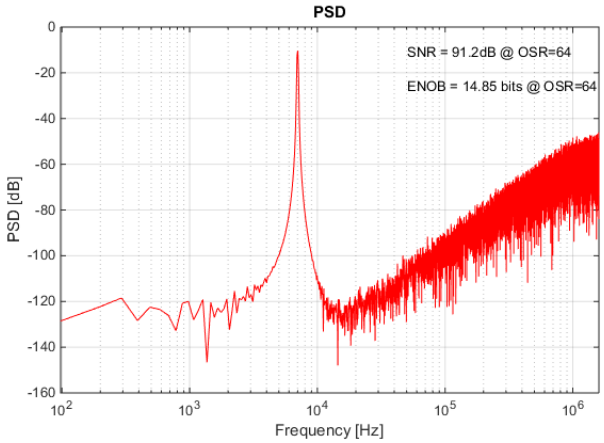

Figure 2.54. FFT of the updated 2nd order 3-bit feed-forward ADC in SIMULINK.

The overall schematic of the new feed-forward ADC is seen in Figure 2.55. In this circuit, a 3-bit capacitive DAC is used. According to the DAC control signals, the supply voltage or the ground becomes the DAC reference for each capacitance. The integrator coefficient becomes $7\times C_1/C_2$ for the first integrator. The capacitive DAC is controlled with data weighted averaging circuit outputs and the clock signals via NAND circuits. The previously designed clock distribution circuit is also used in this ADC.

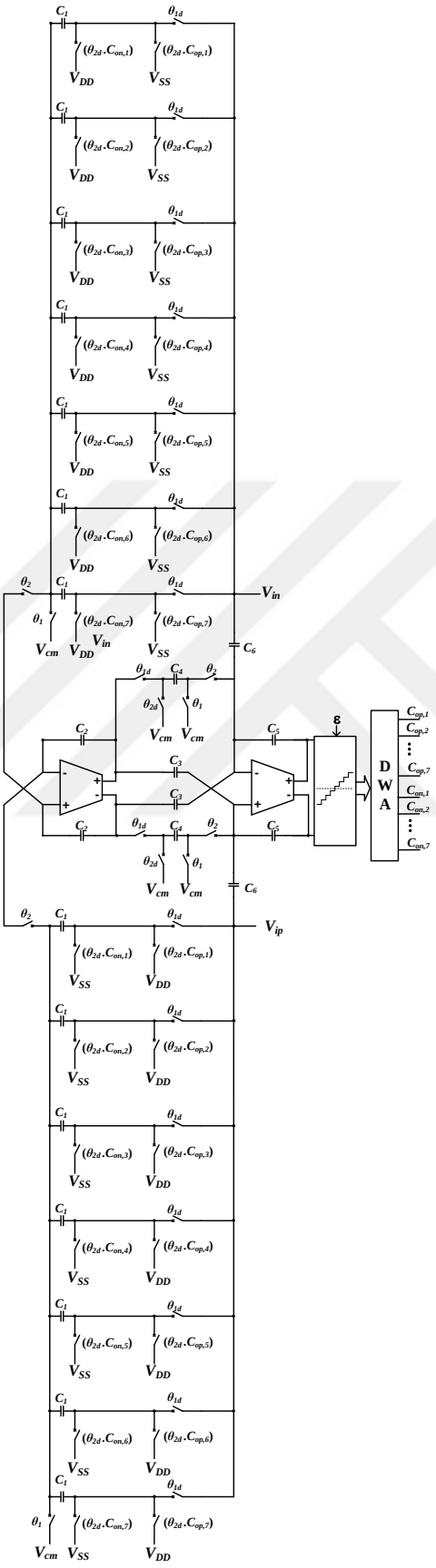

Figure 2.55. The circuit of the 2nd order 3-bit feed-forward ADC.

The minimum size capacitance 100 fF is used for C_1 and C_3. The other capacitances C_2, C_4, C_5 and C_6 are calculated according to C_1 and C_3. Thus, the 1st integrator load capacitance becomes approximately 630 fF according to (3.7) while the 2nd integrator load capacitance becomes approximately 400 fF according to (3.7). These values are very similar to the previous ADC. However, the third folded cascode opamps are used in this ADC to relax the specifications. After fabrication, the clock signal frequency can be increased as well as the bandwidth while keeping the OSR the same or increasing OSR while keeping the bandwidth the same so that the limits of the ADC can be seen. Moreover, the CMFB circuit is updated as half circuits in Figure 2.56 and added to the layout symmetrically.

$$C_{Load,1} \cong C_4 + \frac{C_5 \times C_3}{C_5 + C_3} + C_{CMFB} + \frac{C_2 \times 7 \times C_1}{C_2 + 7 \times C_1} \tag{2.21}$$

$$C_{Load,2} \cong \frac{C_5 \times (C_3 + C_4 + C_6)}{C_5 + C_3 + C_4 + C_6} + C_{CMFB} \tag{2.22}$$

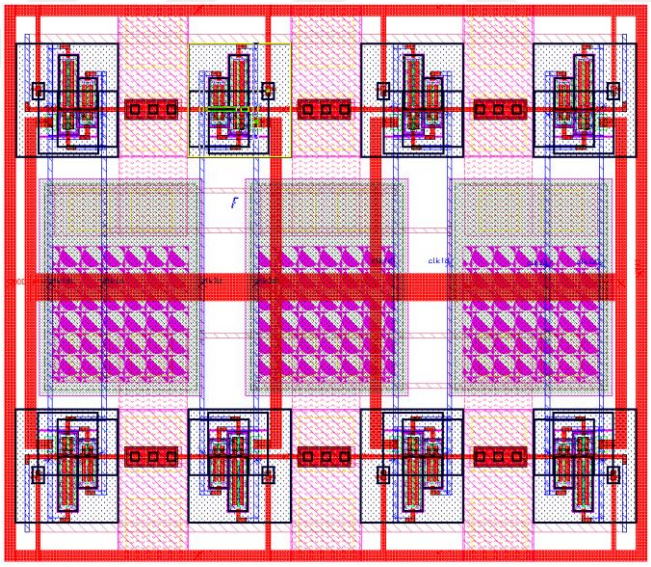

Figure 2.56. Layout of the updated CMFB half circuit.

The quantizer block requires 2^n–1 comparators for n-bit quantization. Therefore, the area increases greatly if the resolution of the quantizer increases. 3-bit quantization is sufficient according to SIMULINK results. Thus, seven comparators are required for quantization. Since the quantizer inputs are differential, these differential signals have to be compared with differential references as well. Consequently, there are 4 inputs for

comparison. Usually, preamplifiers are used before comparators to add the integrator outputs and the reference signals. However, seven preamplifiers are required for 3-bit quantization and they usually consume a lot of power. Although preamplifiers have advantages such as kickback protection, a 4-input comparator is designed as seen in Figure 2.57 to have less power consumption in total. The layout of the comparator is prepared as Figure 2.58. Additionally, the reference voltages are generated with a resistor string. Large capacitances are connected between each node of the resistor string and ground to reduce the effect of the kickback.

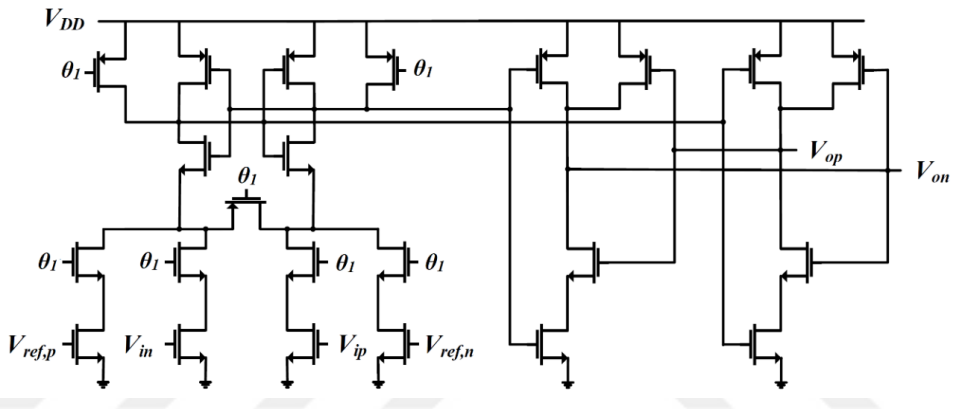

Figure 2.57. 4-input comparator used in the quantizer block.

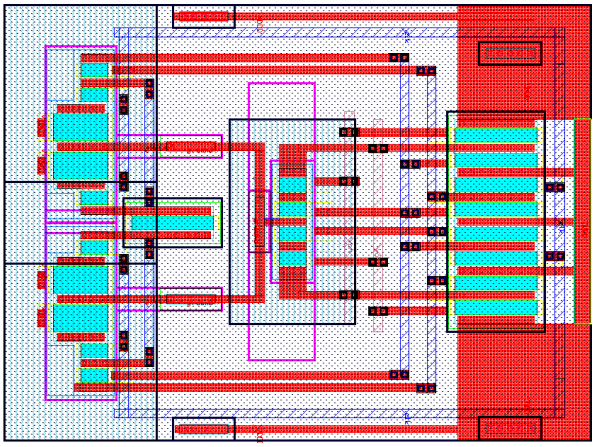

Figure 2.58. The layout of the 4-input comparator.

Data weighted averaging is a commonly used method in multi-bit ADCs [13]. Usually, 2^n-1 thermometer coded control signals are applied to specific DAC circuits. Nevertheless, the next 2^n-1 control signal rotates as much as the value of the signal in data weighted averaging. This realises a 1st order noise shaping and greatly reduces the third

harmonics in the FFT plots of the ADC with improved performance. Normally, most significant bits of the thermometer code are often low while the least significant bits are often logic high. Since the capacitance values change with the process, this causes an unbalance on the capacitive DAC which causes harmonics in the FFT graphs. Nonetheless, each capacitance is used for each data for a similar number of times in the long term in data weighted averaging. Generally, data weighted averaging can be designed with a code in digital domain but it is designed full custom with only NAND and NOR circuits for this ADC to have improved performance. The DWA circuit contains no transmission gates and consumes 2.5 µW for 3.2 MHz clock frequency and 1.2 V supply voltage. The operation of the DWA circuit is depicted in Figure 2.59. Here, the pulse signal is applied to a switch when the output of one of the comparators is high. For the next clock, only one comparator output is logic high again. Thus, a pulse signal is applied to the next switch this time. Afterwards, two comparator outputs are high which leads to two pulse signals to be transferred to the following two switches. The number of pulse signals and the rotation becomes as much as the number of logic high outputs of the comparators. These pulse signals are used for the capacitive DAC control signals and include the clock data in them. Therefore, the inverse and delayed versions are generated in the meantime. Moreover, the starting bit data has to be stored in the circuit while all the comparator outputs are high or low. So, each switch is turned on equal times on average in the long transient time. The schematic of the data weighted averaging circuit is seen in Figure 2.60. The layout of the data weighted averaging circuit is depicted in Figure 2.61.

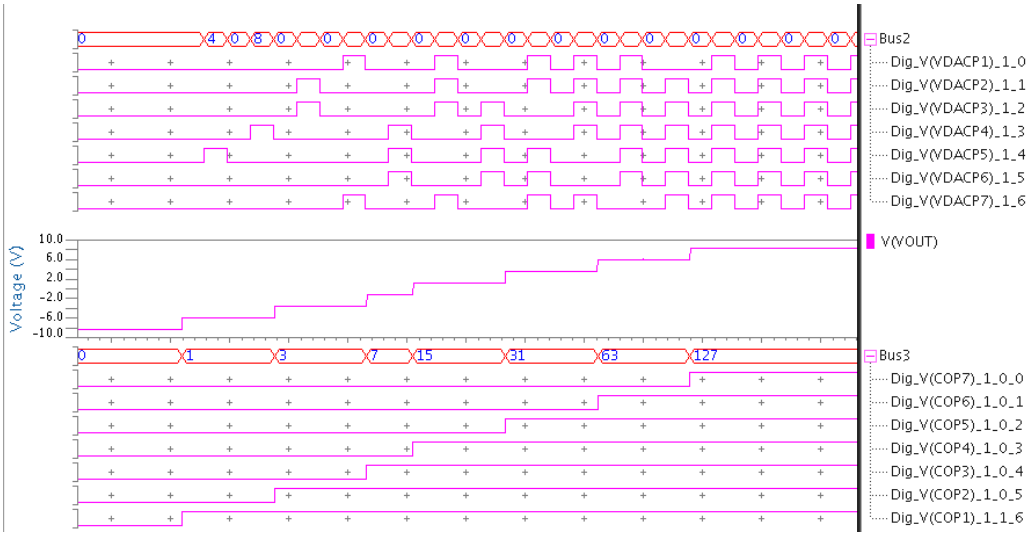

Figure 2.59. DWA circuit operation.

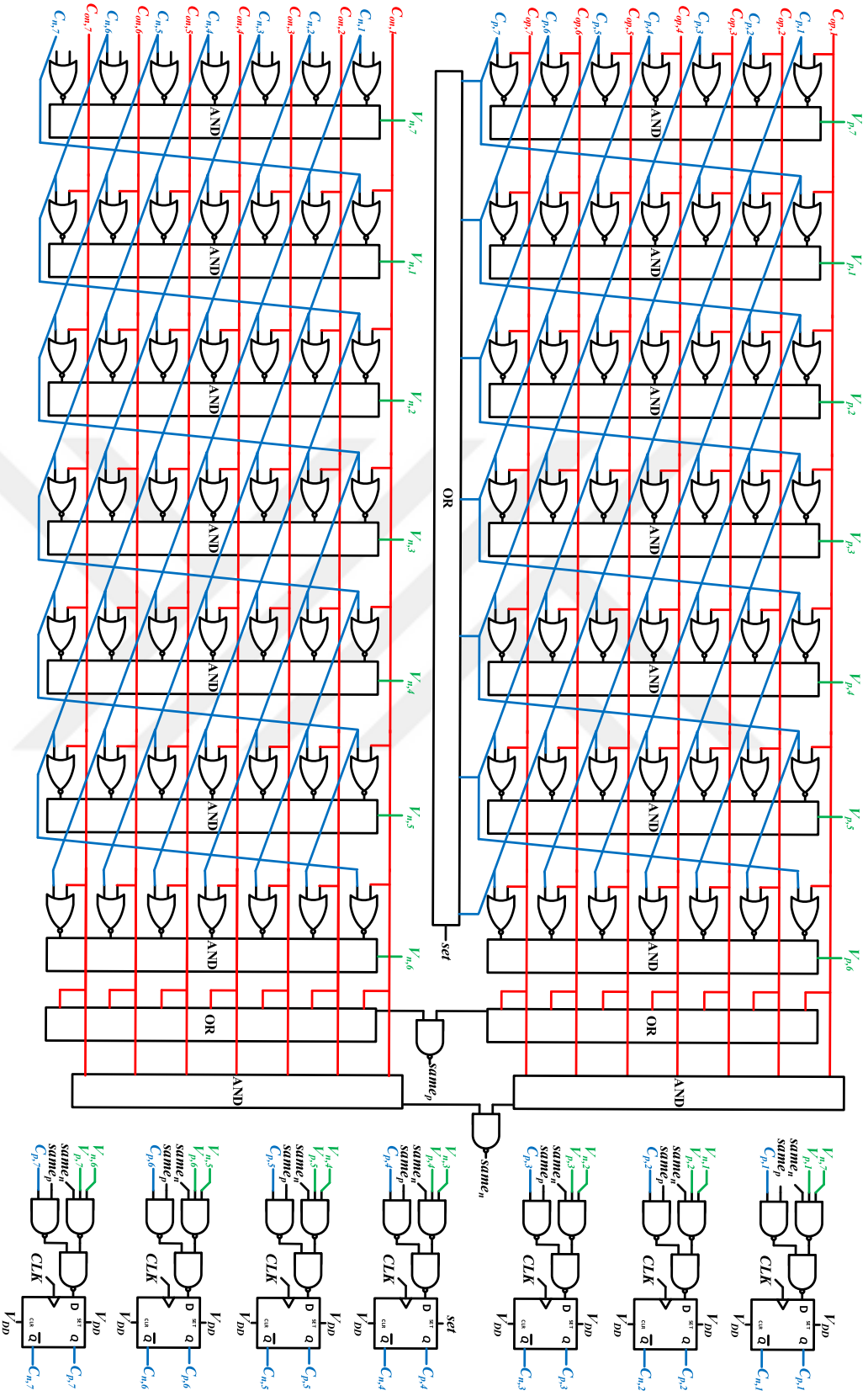

Figure 2.60. Schematic of the data weighted averaging circuit.

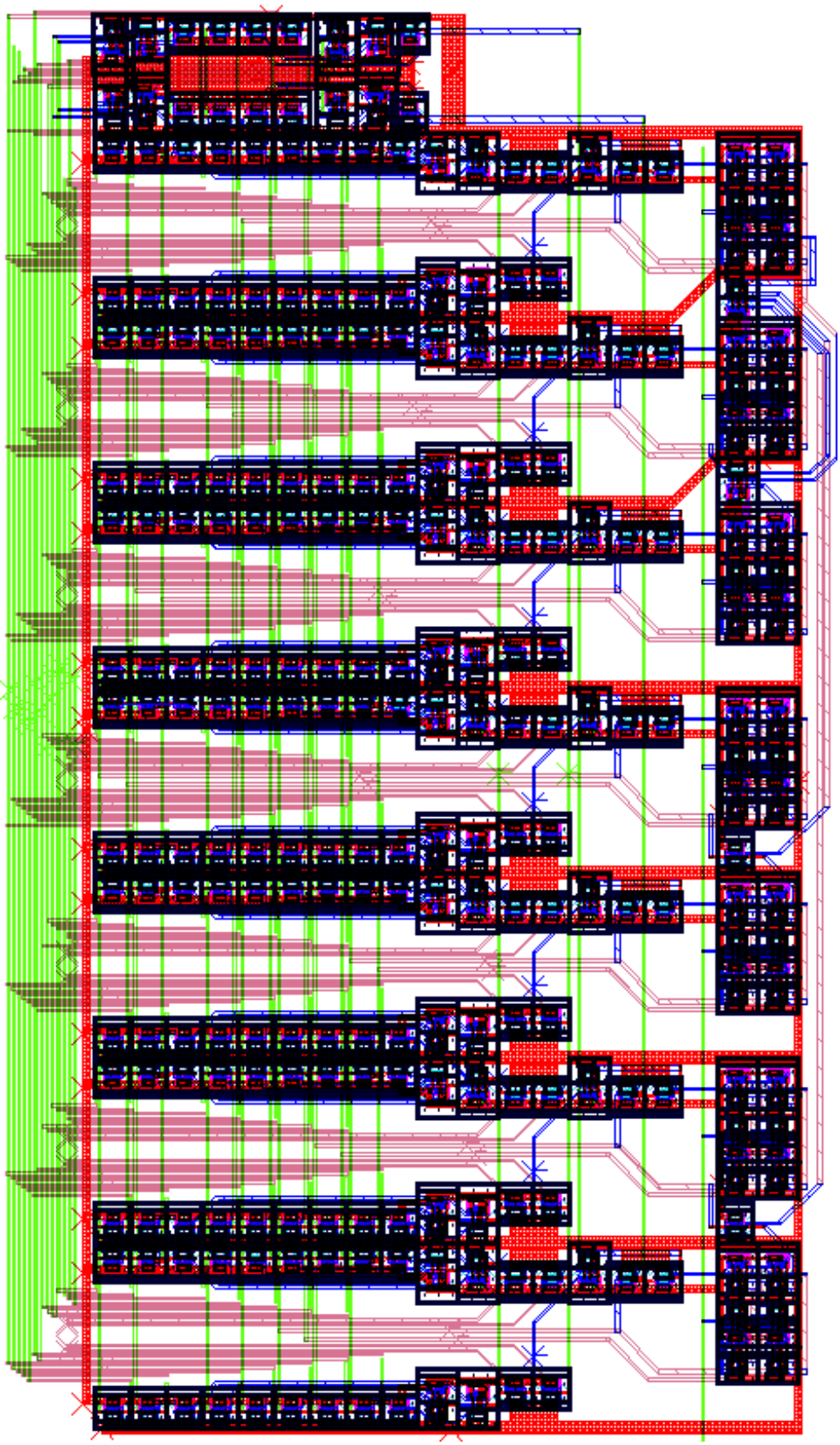

Figure 2.61. Layout of the data weighted averaging circuit.

Afterwards, the overall layout is prepared as in Figure 2.62. However, ELDO could not perform post-layout simulations. Thus, simulations were performed on a circuit by connecting with post-layout models at each sub-circuit manually. These show that this 2nd order 3-bit feed-forward SD ADC has 87 dB SNDR as in Figure 2.63. FoM is calculated as 112 fJ/conv with 102.5 µW power consumption.

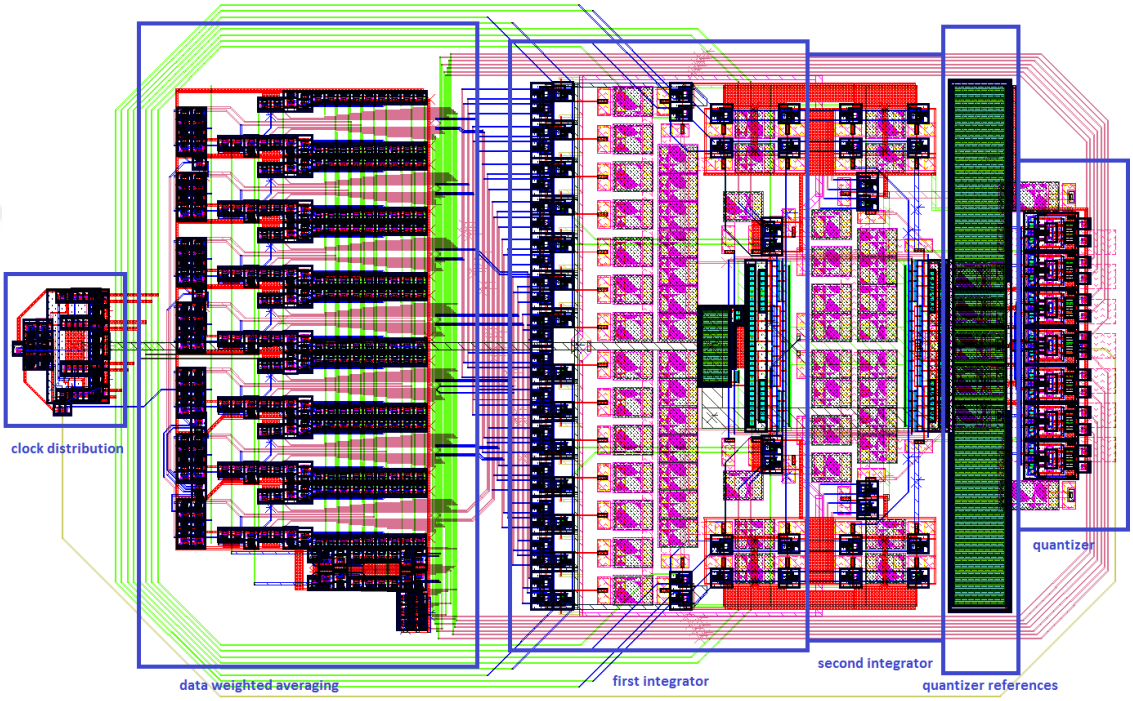

Figure 2.62. Overall layout of the 2nd order 3-bit feed-forward SD ADC.

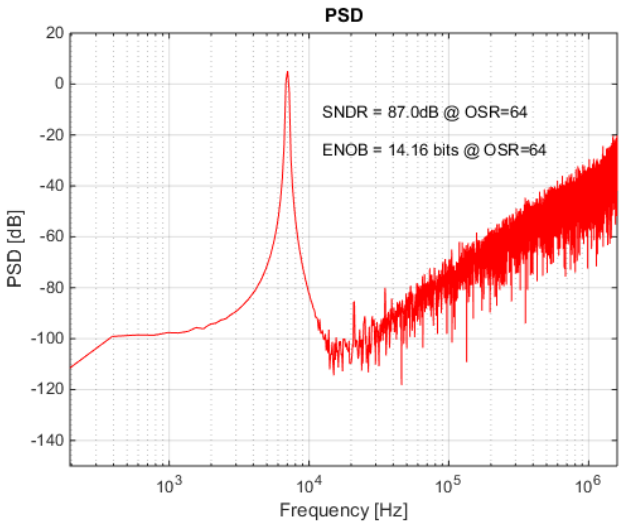

Figure 2.63. FFT results of the 2nd order 3-bit feed-forward SD ADC.

2.1.5. Feed-Forward Method in SD ADCs with Successive Approximation

SD ADCs and SAR ADCs are both widely used and have different advantages with respect to each other. As SD ADCs require an ADC block, a SAR ADC can be used inside the SD ADCs as a quantizer block instead of a Flash ADC [14]. Usually, an opamp or some switches are used to obtain feed-forward paths as well as the proposed method in the previous sections. However, the coefficients of the SAR are combined with the coefficients of the addition at the output of the SD ADC in Figure 2.49 and addition operation is done inside the SAR ADC. The new ADC schematic is shown in Figure 2.64 with the SAR ADC.

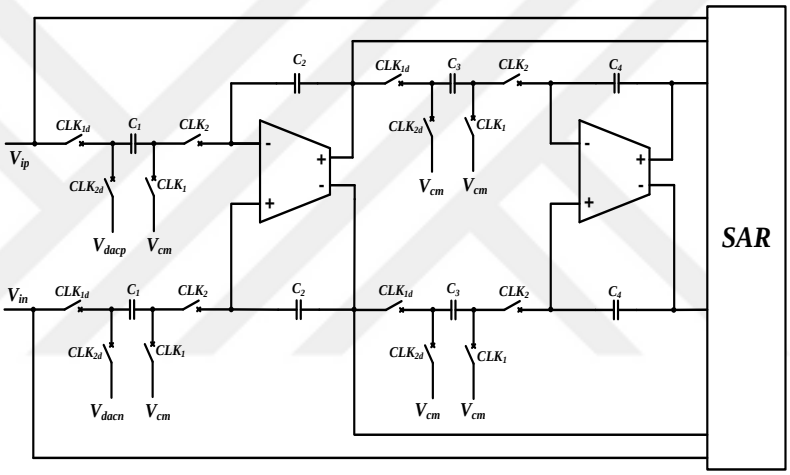

Figure 2.64. 2nd order feed-forward SD ADC with SAR ADC.

For 3-bit quantization, a fully differential SAR ADC is designed. The operation logic of the SAR can be seen in Figure 2.65. The fully differential SAR ADC circuit is designed according to this logic and the circuit can be seen in Figure 2.66. The operation logic of the SAR can be summarized as follows:

- During CLK_A, three inputs are stored on the capacitances of C, $2C$ and C which are also equal to the coefficients of the addition at the output of the sigma delta modulator. Those input signals are attenuated at this phase.

- During CLK_B, the charges stored in those capacitances are transferred to the input of the comparator. The inputs of the comparator are the opposites of the signals due to charge transfer. At the end of this phase, the comparator compares the two

differential signals and finds a result which is the most significant bit. Since the inputs of the comparator are reversed, the results of the comparator are also reversed. According to the most significant bit result, V_{DACP1} becomes a positive or negative reference value while V_{DACN1} is its inverse.

- During CLK_C, the charge at the input of the comparators is reduced or increased according to the most significant bit. At the end of this phase, another comparison is made and the middle bit is obtained. According to the middle bit result, V_{DACP2} becomes a positive or negative reference value while V_{DACN2} is its inverse. In the meantime, the most significant bit is delayed with a D flip-flop circuit.

- During CLK_D, the charges at the input of the comparator are reduced or increased according to both middle bit and the most significant bit. This time, the most significant bit and the middle bit are delayed while the least significant bit result is achieved from the comparator.

- Finally, all the bit values are found and transferred to the DAC to generate a reference voltage to be used in sigma delta ADC. These bit values remain the same until the next results are ready. Meanwhile, it is again CLK_A phase and the new quantization has started.

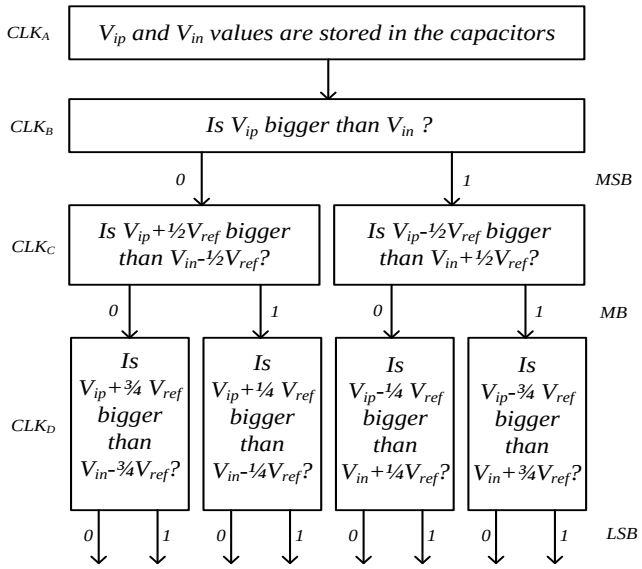

Figure 2.65. The operation logic of the SAR ADC.

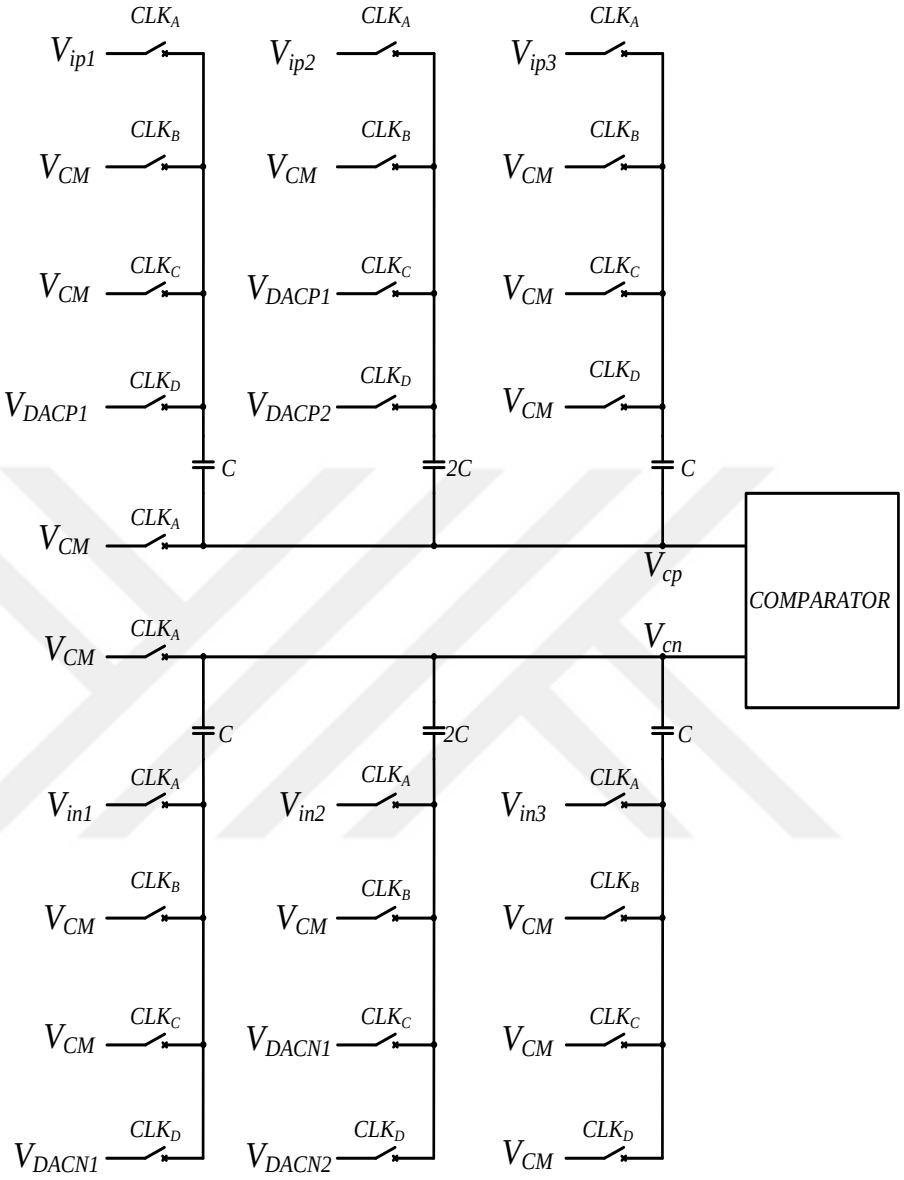

Figure 2.66. Switch level of SAR ADC used in the SD ADC.

This SAR ADC structure is fully differential and the main advantage of this SAR ADC is the requirement of fewer capacitors than regular SAR structures. Besides, the addition block in sigma delta ADC is removed in this topology by using the SAR ADC which also uses only one comparator. However, the opamps have to have a faster settling time because the outputs have to charge the sampling capacitors in the SAR ADC in fast clock cycles. Figure 2.67 depicts the SAR ADC behaviour in time domain according to ELDO simulations.

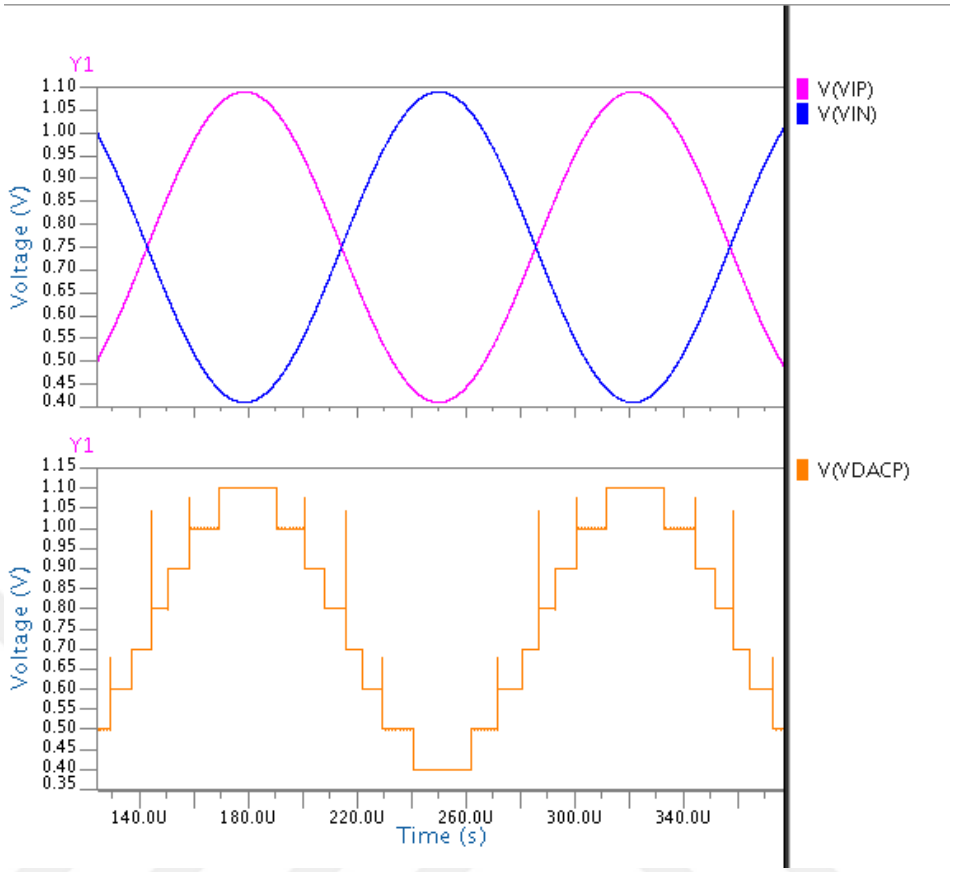

Figure 2.67. SAR ADC behaviour in time domain in ELDO.

UMC 180 nm technology is chosen for this ADC. The clock distribution circuit in Figure 2.33 and the comparator in Figure 2.37 are designed again with minor modifications in this technology. A SAR ADC uses *n+1* non-overlapping clocks for *n*-bit quantization. Here, D flip-flop circuits are used with some NAND and NOR circuits to generate the SD and SAR ADC clocks. Accordingly, the clock signals are as in Figure 2.68.

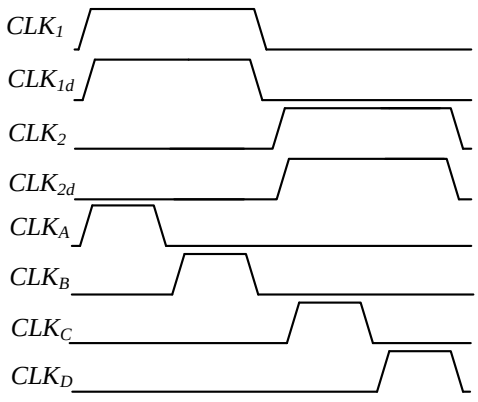

Figure 2.68. The clock signals used in the ADC.

Since the supply voltage is 1.8 V, the telescopic cascode opamp in Figure 2.69 is used in integrators. This opamp has 52 dB gain and 4 MHz bandwidth for 0.5 pF loads while 1 µA is flowing through each branch. The bias circuit also has 1µA current flowing through its branch. A switched capacitor CMFB is also used to obtain the desired DC output values. Moreover, NMOS transistors are used as switches in the design instead of transmission gates because the supply voltage is higher in UMC 180 nm technology.

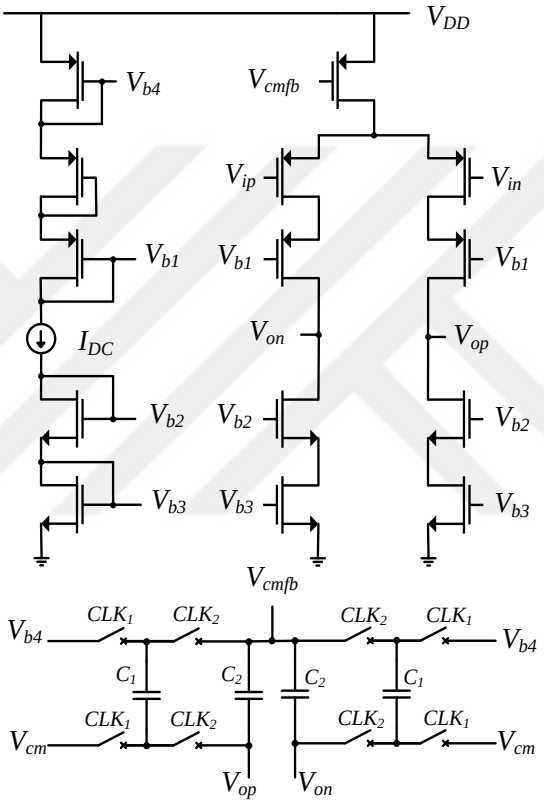

Figure 2.69. Telescopic cascode opamp used in the integrators.

Another block that is needed is the DAC block. A resistive DAC is designed for the ADC which can be seen in Figure 2.70. At each clock cycle, the required switches start operating according to the SAR ADC results and the capacitors are charged in SD ADC. When SAR ADC reference voltages and the common mode voltage are obtained from the same resistive string, third harmonics can be seen in the FFT result. Therefore, the common mode reference voltage and the SAR ADC reference voltages will be provided by an outside source as supply voltages.

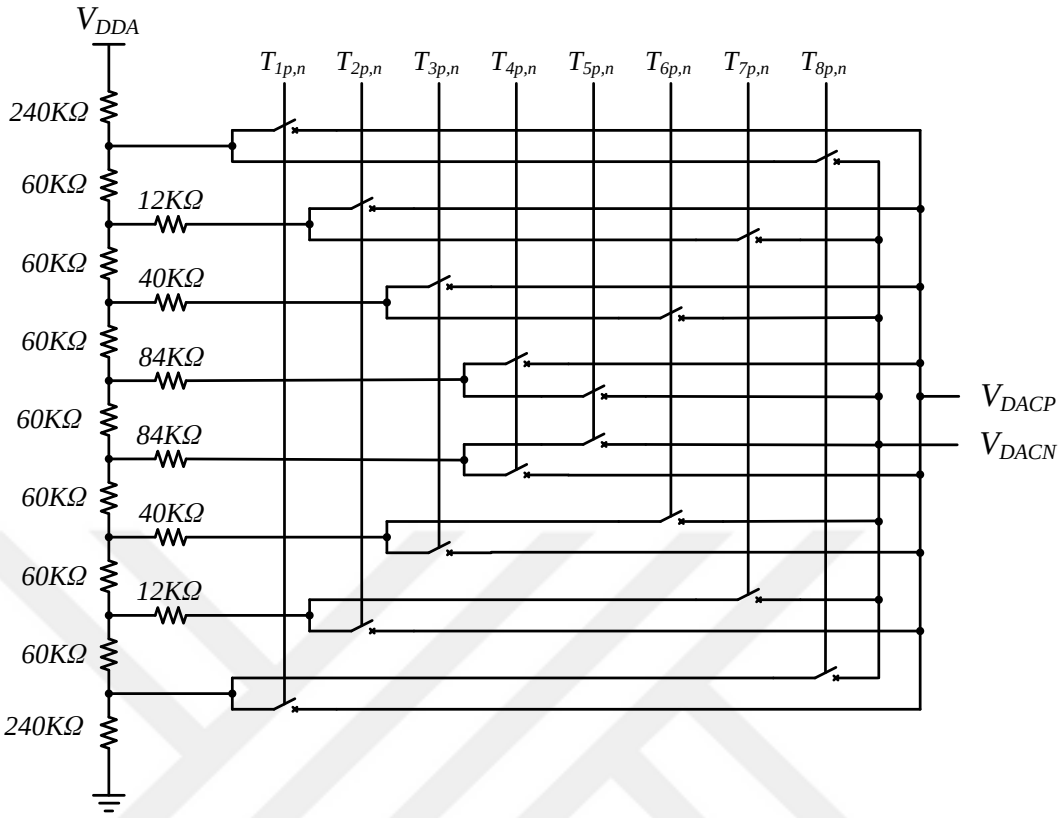

Figure 2.70. Resistive DAC circuit used in the ADC.

Afterwards, the design of 2nd order 3-bit SD ADC is completed with the SAR ADC and the resistive DAC. The specifications of the ADC are given in Table 2.2 and a transient analysis is done with for 32768 clock cycles. During the pre-layout simulation, the logic outputs are saved and transferred to MATLAB to find the SNDR of the SD ADC. According to the FFT result in Figure 2.71, SNDR is calculated as 76.8 dB as expected. FoM is calculated 60 fJ/conv according to the results.

Table 2.2. Specifications of the 2nd order SD ADC with SAR quantization.

Specifications	**Value**
Integrators and Bias Circuit	9 µW
Clock Distribution Circuit	0.8 µW
Resistive DAC	2.5 µW
SAR ADC	4.6 µW
Total power consumption	16.9 µW
OSR	32
Signal Bandwidth	25 kHz
SNDR	76.8 dB
ENOB	12.46 bit
FoM	60 fJ/conv

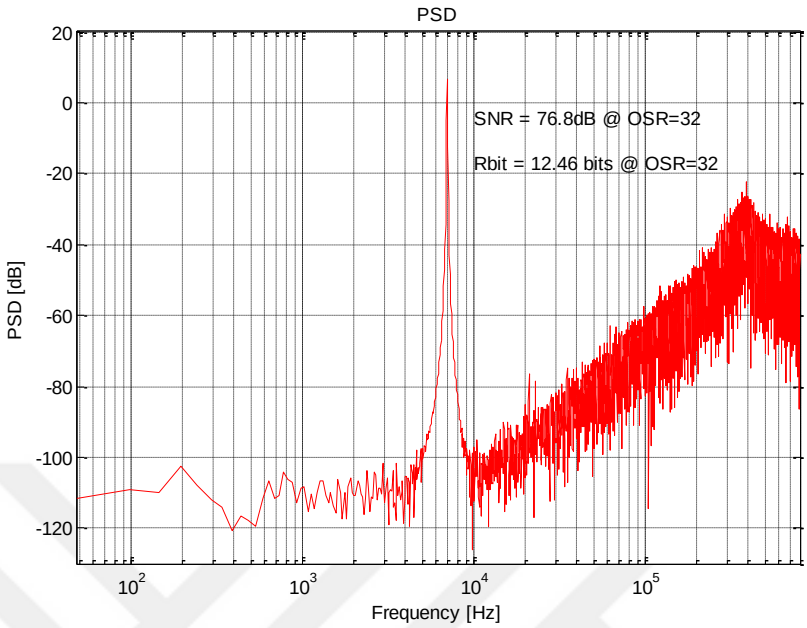

Figure 2.71. FFT results of the 2nd order SD ADC with SAR quantization.

2.2. Third Order DT SD ADC Types

3rd order SD ADCs are the most suitable architectures for low power applications. A 3rd order SD ADC with an OSR of 32 has similar SNR to a 2nd order SD ADC with an OSR of 64. Although an additional opamp is used as an integrator, the opamp specifications are relaxed by approximately two times because the OSR is also halved. Therefore, the opamps used in the integrators have less power consumption. Correspondingly, the digital power consumption is halved because the sampling frequency is reduced by half. Hence, 3rd order SD ADCs have less overall power consumption than 2nd order SD ADCs.

2.2.1. Feed-Forward 3rd Order 3-Bit SD ADC

Although there are many 3rd order SD ADCs in the literature, the ADC in Figure 2.72 is chosen because of its transfer function in (2.23). Because of this transfer function, the integrator outputs do not contain any input signal *X* and only contain the quantization noise signal ε as seen in (2.24), (2.25) and (2.26). Hence, the integrator outputs are very small when multi-bit quantization is applied. So, the 3rd order 3-bit SD ADC is modelled in SIMULINK as in Figure 2.73 and the integrator output histograms are observed as in Figure

2.74. It is observed that the 1st and 2nd integrator output swings are low while the 3rd integrator output swing is high. When FFT operation is applied to the output of the ADC in Figure 2.75, the resulting SNR is calculated as 95.9 dB as depicted in Figure 2.76.

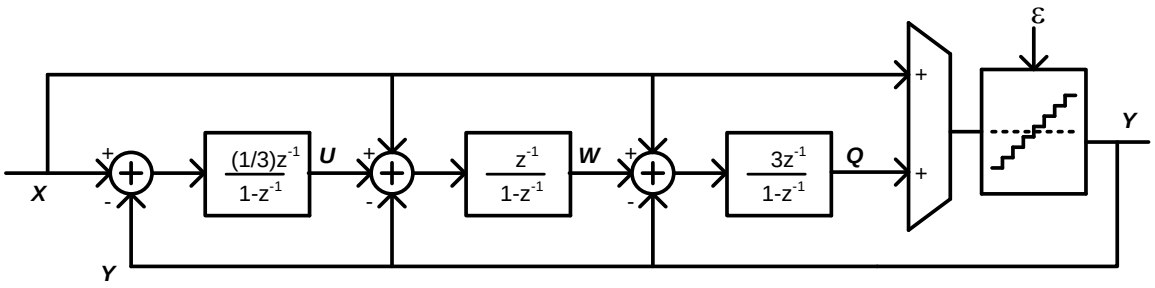

Figure 2.72. 3rd order multi-bit SD ADC.

$$Y = X + \varepsilon(1 - z^{-1})^3 \tag{2.23}$$

$$U = \frac{1}{3}\varepsilon z^{-1}(1 - z^{-1})^2 \tag{2.24}$$

$$W = \varepsilon\left(z^{-1} - \frac{5}{3}z^{-2} + \frac{2}{3}z^{-3}\right) \tag{2.25}$$

$$Q = \varepsilon(-3z^{-1} + 3z^{-2} - z^{-3}) \tag{2.26}$$

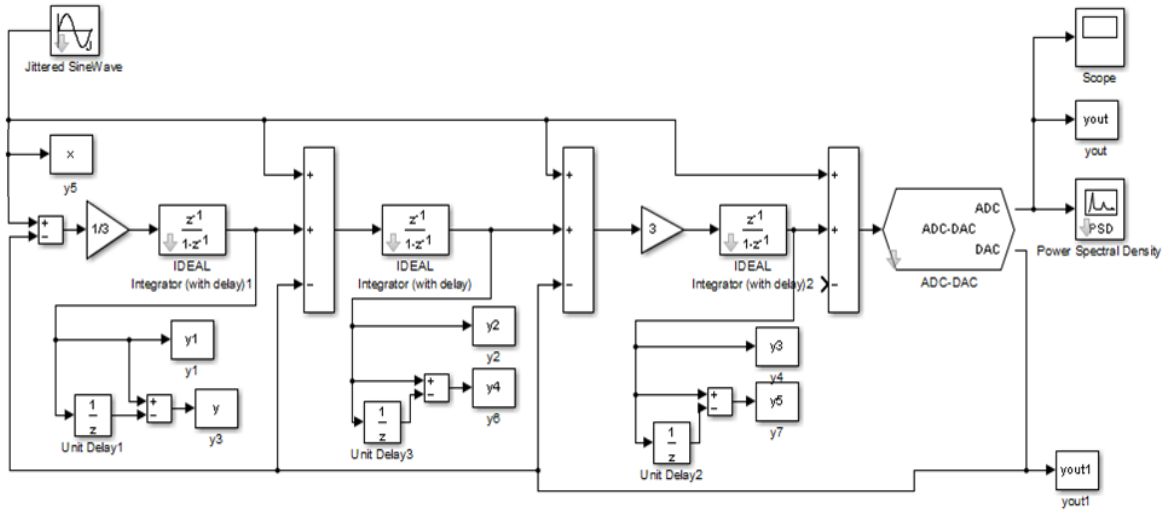

Figure 2.73. 3rd order 3-bit SD ADC in SIMULINK.

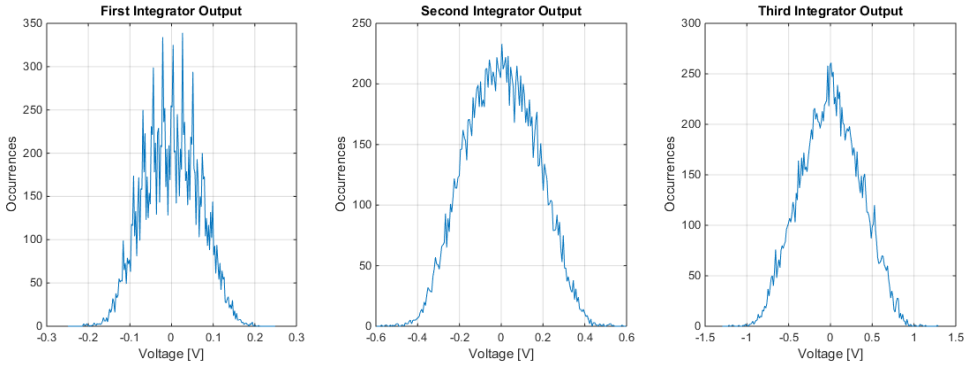

Figure 2.74. Output histograms of the integrators in 3rd order 3-bit SD ADC.

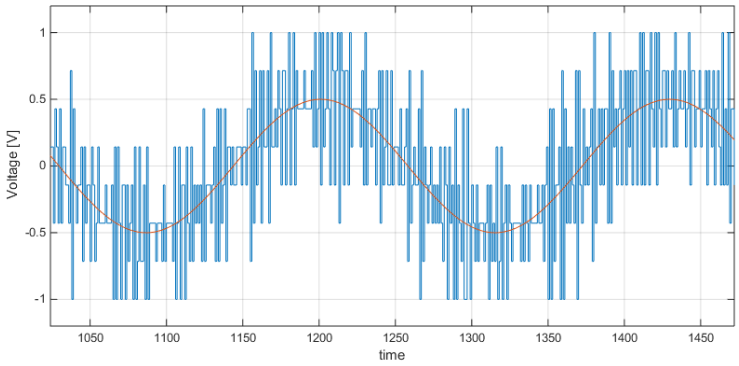

Figure 2.75. The output of the 3rd order 3-bit SD ADC in SIMULINK.

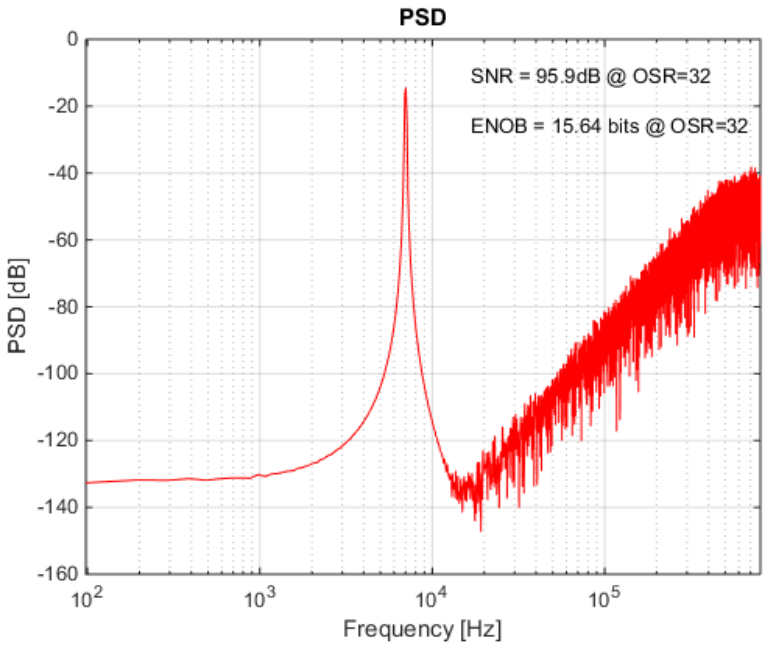

Figure 2.76. FFT of the 3rd order 3-bit SD ADC in SIMULINK for input amplitude and reference ratio of 0.5.

Although the SNR results are quite good, 3rd integrator output swing is very high in this ADC. To lower the 3rd integrator output swings, the quantization reference levels are increased by 20% in SIMULINK as in Figure 2.77. This changes the transfer function but the 3rd integrator output swings are lower as depicted in the integrator output histograms in Figure 2.78. Furthermore, the FFT results provided in in Figure 2.79 shows that the SNR of the updated ADC is slightly better than the previous version.

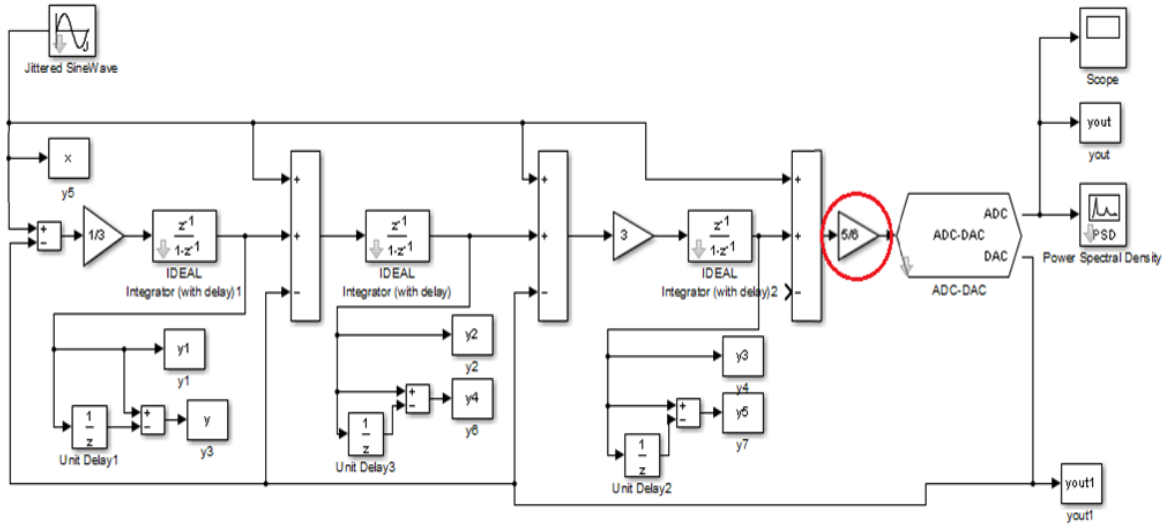

Figure 2.77. 3rd order 3-bit SD ADC with quantization reference levels increased 20%.

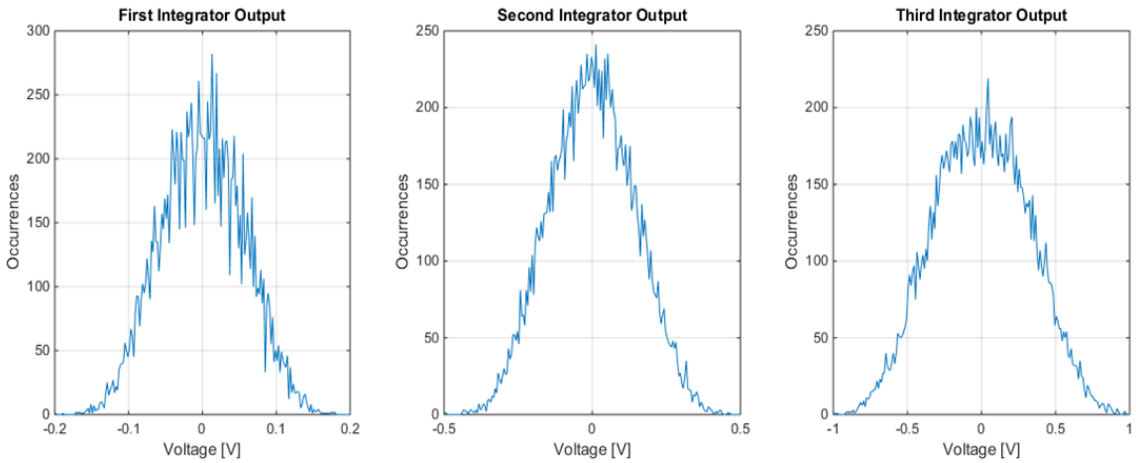

Figure 2.78. Integrator output histograms for the updated 3rd order 3-bit SD ADC.

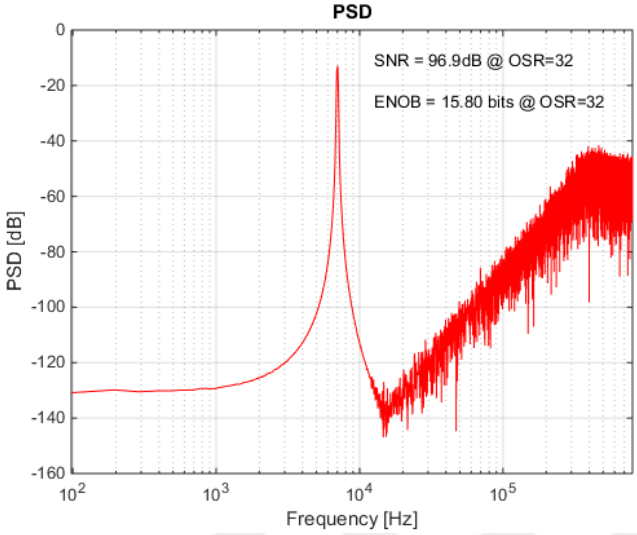

Figure 2.79. FFT graph of the updated SD ADC in SIMULINK for input amplitude and reference ratio of 0.6.

Since the 3rd order 3-bit SD ADC SIMULINK results are quite good, the schematic in Figure 2.80 is prepared as a 3rd order SD ADC in UMC 180 nm technology. Capacitances are chosen as C_1=C_3=C_4=C_5=C_6=C_7=105 fF, C_2=315 fF, C_8=35 fF and C_9=C_{10}=120 fF. Here, regular NMOS transistors are used as switches in the design because the supply voltage is 1.8 V in UMC 180 nm technology. The whole structure is fully differential and a conventional feed-forward path is used rather than the proposed feed-forwards method. Furthermore, the addition operation before the comparator is obtained by a non-delayed switched capacitor circuitry which attenuates the added signals by sharing the charges between the sampling capacitors.

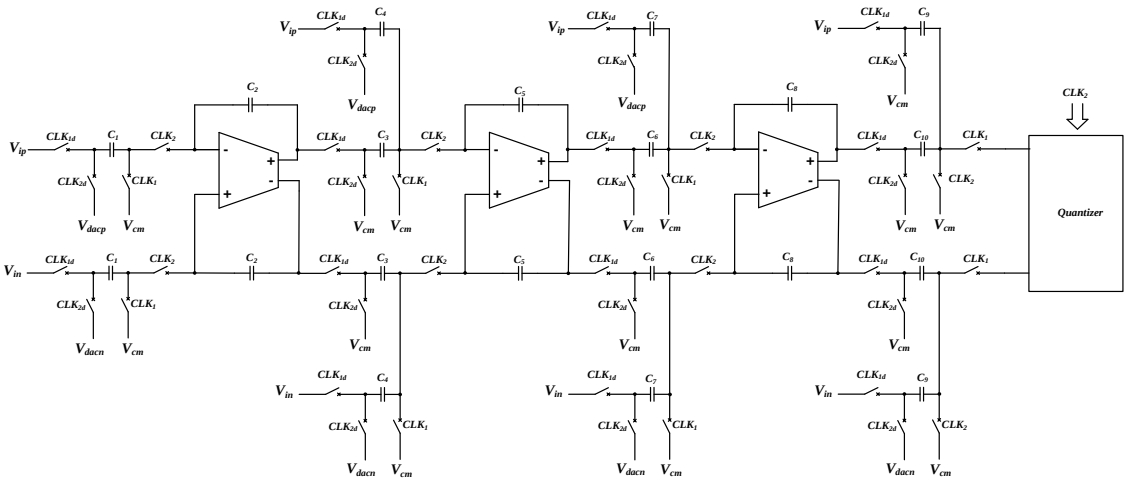

Figure 2.80. 3rd order SD ADC schematic.

Double sampling is a method used in switched capacitor circuits [15]. In a delayed integrator, the sampling capacitor is charged during θ_1 and the charge is normally transferred to the output in θ_1. Thus, the output of the opamp stays the same in a clock cycle and changes in the other clock cycle. However, another switched capacitor circuit can be used in the integrator as in Figure 2.81. Now, the first sampling capacitor is charged during θ_1 while the other sampling capacitor is charged during θ_2. The charge in the first sampling capacitor is transferred to the output during θ_2 while the charge in the other sampling capacitor is transferred to the output during θ_1. Thus, the integration operation is performed in both clock cycles, hence doubling the integration frequency in the meantime. The circuitry used is similar and the load of the opamps are the same because the sampling capacitors are not connected to the inputs of the opamps at the same time. Although the OSR is doubled, the opamp requirements stay the same. Moreover, the output of the opamp changes in both clock cycles as the opamp operates in both clock cycles. However, matching of the sampling capacitances is very important here.

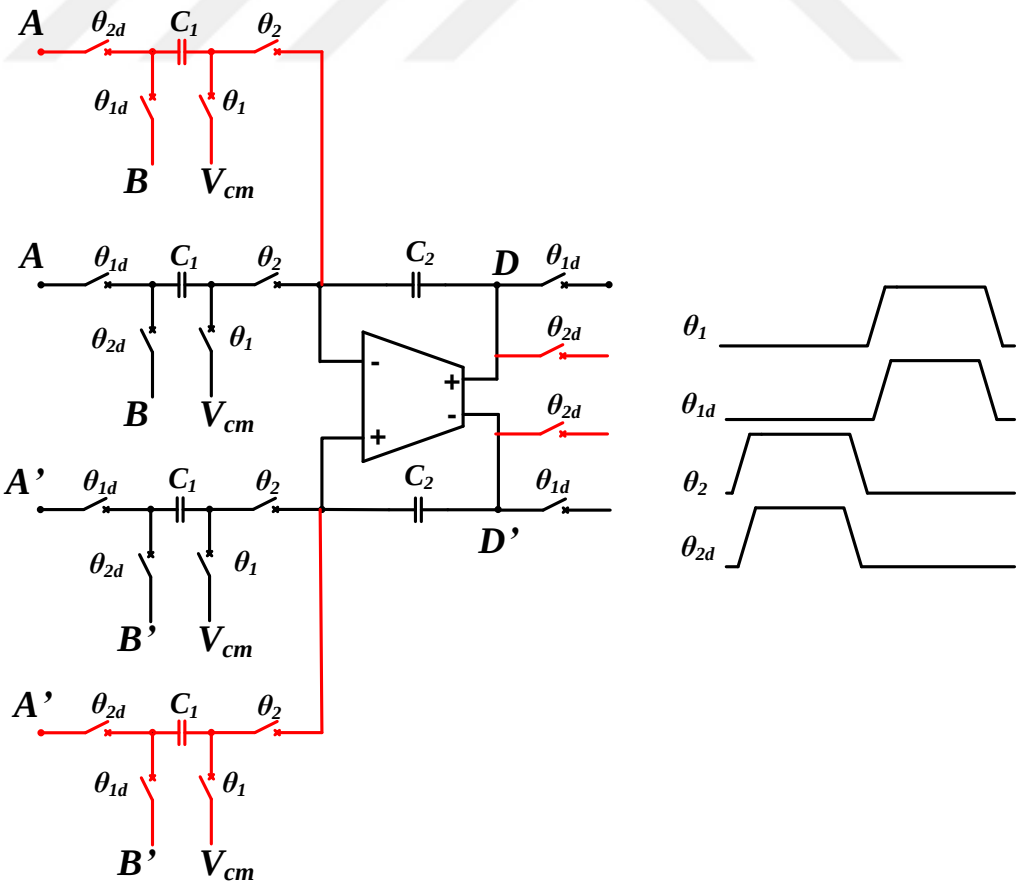

Figure 2.81. Application of double sampling method.

Consequently, the double sampling method is used for this ADC as in Figure 2.82. Although double sampling increases the complexity of the SD ADC, it helps the performance of the ADC. Performing the comparison and the addition operation simultaneously is difficult to achieve in double sampling. Therefore, 14 comparators are used for 3-bit quantization instead of 7 comparators. During CLK_1, the output of the filter is compared by the first quantizer block. During CLK_2, the output of the filter is compared utilizing the other quantizer block while the first quantizer is reset. Back during CLK_1, the second quantizer block is reset. The latched outputs of the quantizers are chosen by the appropriate clock and comparison is performed at twice the sampling frequency in the end. This again effectively doubles the OSR. For 25 kHz bandwidth and 32 OSR, sampling frequency is normally 1.6 MHz but with the help of double sampling, 800 kHz clock frequency is used instead.

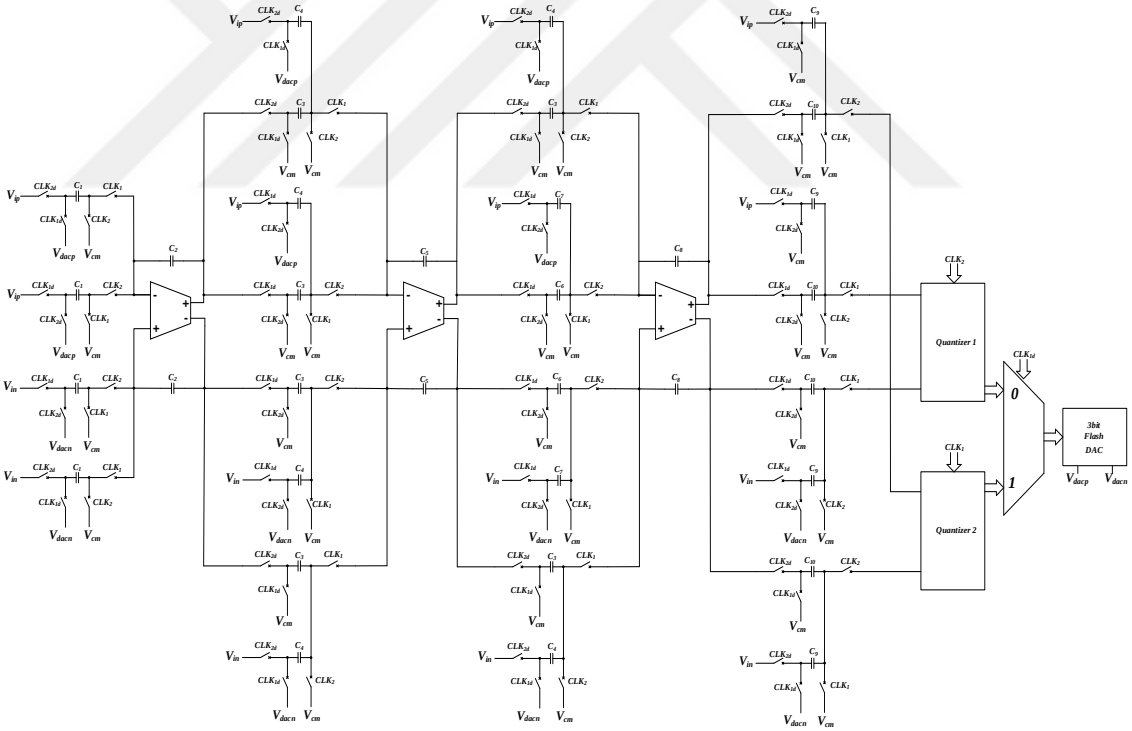

Figure 2.82. 3rd order SD ADC with double sampling method.

The earlier version of the clock distribution circuit in Figure 2.33 is employed here. The earlier version of the clock distribution circuit does not contain a D flip-flop that halves the sampling frequency and helps against clock jitter by providing equal duty cycles.

Even though adaptive biasing techniques [16] and class AB opamps [17] and many other opamps [18] are investigated, simple opamps had the same performance with lower power consumption. Since the supply voltage can be chosen as 1.8 V in UMC 180 nm technology, telescopic cascode opamps are chosen because they have less power consumption than folded cascode opamps and two-stage opamps for the same performance. Thus, the earlier versions of the telescopic cascode opamps in Figure 2.69 are used here too. The earlier version of the opamp has half the power consumption and GBW of the telescopic cascode opamps explained earlier in Figure 2.69. 0.5 µA current is flowing through the bias circuit and through each branch of the telescopic cascode opamp. For that reason, the total power consumption of the bias circuit and three opamps is 6.3 µW. Furthermore, telescopic cascode opamps have 52 dB gain and 2 MHz bandwidth for 0.5 pF loads. The switched mode CMFB circuit is also updated. Instead of using one CMFB circuit, two identical CMFB circuits that operate in different clock cycles, are used to keep the output DC voltage at the desired level.

The quantizer block consists of a resistive string, 14 comparators, and 7 multiplexers which can be seen in Figure 2.83. The resistive string determines the voltages that will be added to or subtracted from the differential outputs. Here, the addition block before the quantizer halves the signals because the charges are shared between two sampling capacitors. Normally, the reference levels would be between 450 mV and 1050 mV with 100 mV steps. In this case, the reference levels are chosen between 570 mV and 930 mV with 60 mV steps because the signals are halved before the quantizer because of switched capacitor addition circuit. Moreover, the reference levels are increased 20% to reduce the 3rd integrator swing as introduced. The current flowing through the resistive string that determines reference levels for comparison is 0.2 µA and the supply voltage is selected as 1.5 V which is the same supply voltage of the digital circuits. Therefore, the power consumption of this resistive string is 0.3 µW. The output of the comparators 1 to 7 are chosen during CLK_2 and the outputs of the comparators 8 to 14 are chosen during CLK_1 by the multiplexers at the output of the comparators. Afterwards, seven thermometer code outputs are transferred to 6 XOR and XNOR blocks to have 8 bit positive and negative digital codes. Next, this digital code is encoded by an encoder into 3 bit output. XORs, XNORs and the encoder can be seen in Figure 2.84.

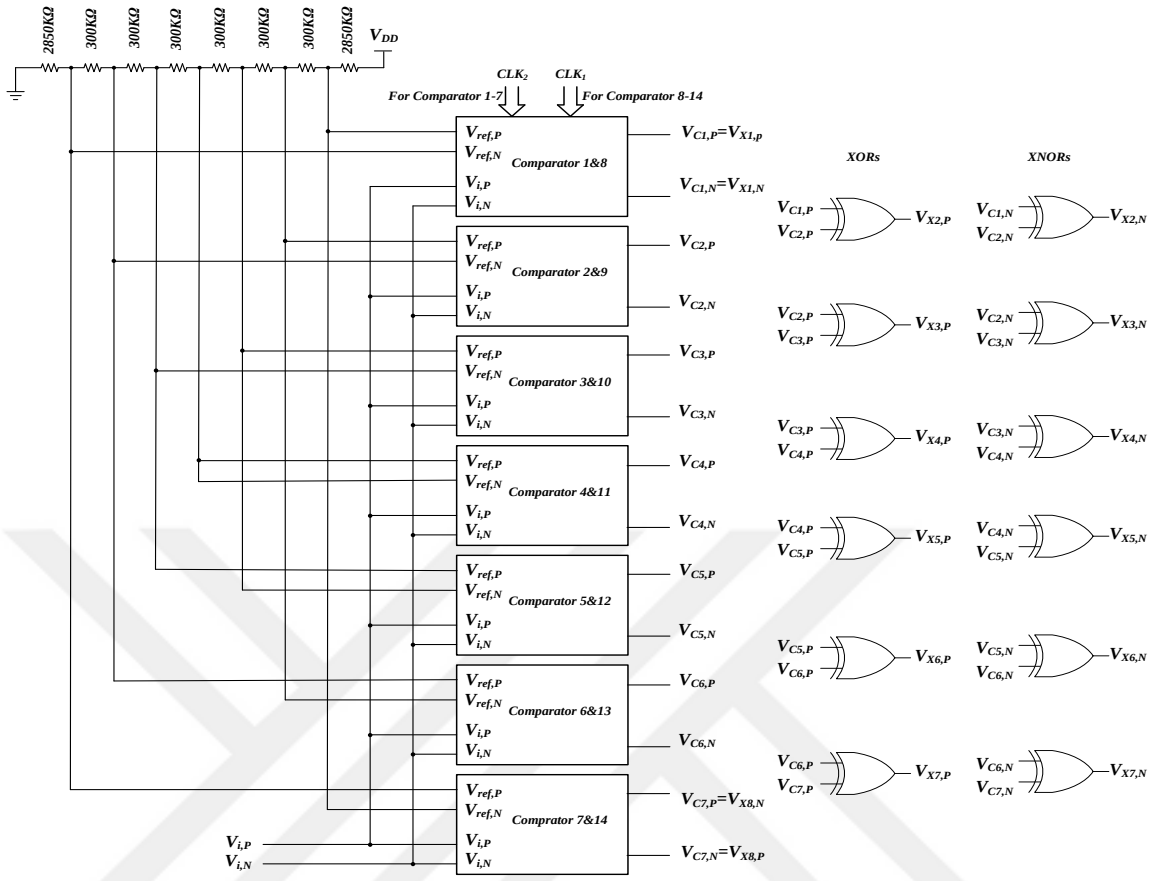

Figure 2.83. Quantizer block in the 3rd order SD ADC.

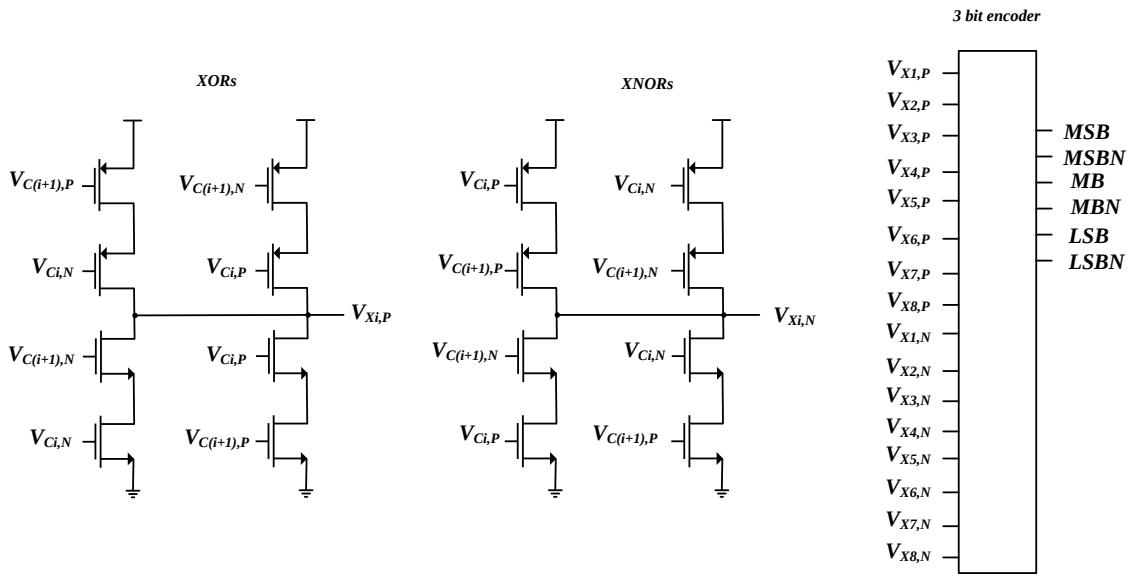

Figure 2.84. XOR and XNOR circuits used to generate encoder input signals.

The 4-input comparator architecture in Figure 2.57 has already been discussed. The earlier version of this comparator is depicted in Figure 2.85 and it is used in the quantization

block with a supply voltage of 1.5 V. It is still fully differential and has the ability to add reference voltages to the inputs during the comparison. Besides, there are latches at the output of the comparators that saves the last result even though the clock signal resets the comparator.

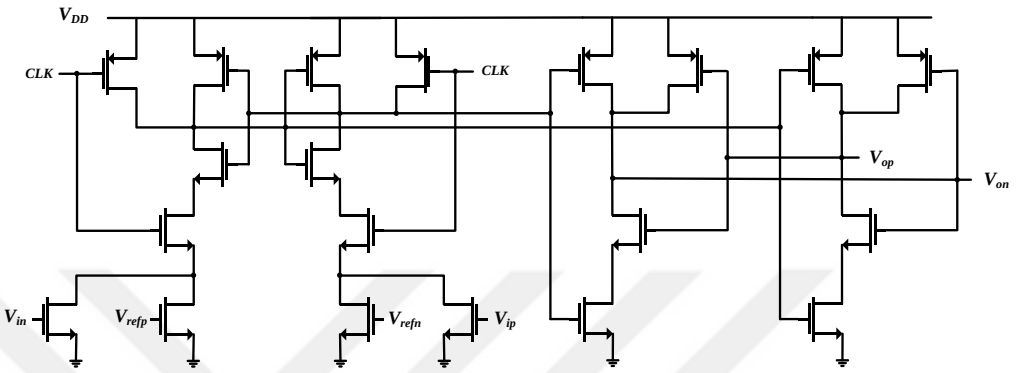

Figure 2.85. 4-input comparator circuit used in the quantizer.

As a result, the whole quantization block consumes 0.9 µW power which is calculated by the average current drawn from the supply voltage observed in a long transient analysis. Although more comparators are employed, the clock frequency is halved when double sampling is used. Therefore, the total switching and the power consumption of the quantization block are alike in both double sampling and normal sampling when OSR is 32.

There are many options for DAC implementation. Since this design operates with 1.8 V, rail to rail operation is impossible to achieve because of telescopic cascode opamps. Thus, DAC references are chosen between 400 mV and 1100 mV with 100 mV steps. Moreover, the *RC* time constant of the feedback is very important because the DAC is connected to all three integrators in this architecture. The first alternative is to use a resistive string with a buffer after the resistive string. However, this causes high power consumption by the buffer even though the resistance values are chosen to be high. Furthermore, there are two outputs of the DAC which require two opamps to be used as buffers. Since the opamps will be in unity feedback configuration, the telescopic opamps cannot be utilized due to their low output swings. Moreover, a differential opamp doesn't have enough gain to operate as needed. Thus, new opamps have to be designed and it is assumed that they will have very high power consumption and additional noise contribution. A *R-2R* circuit can also be used instead of a resistive string but it still requires buffers in the design. Although, unity gain

circuits such as those in Figure 2.86 can be used as unity gain opamps, they cause too much power consumption and again, too much noise.

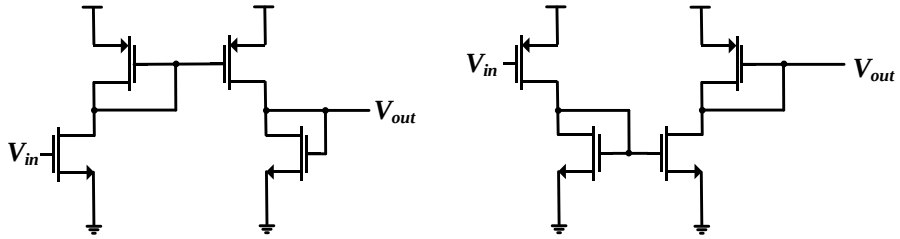

Figure 2.86. Unity gain circuits.

A switched DAC circuit, which is shown in Figure 2.87, is simulated for the feedback circuit. There are three transistor couples with bias currents $4I$, $2I$ and I controlled by the most significant bit, the middle bit, the least significant bit and their inverse. Three of the six switches in the switched DAC are always turned on according to the digital outputs of the encoder. According to the bit value, one of the transistor couples is turned on letting the current flow through either the positive or the negative DAC output branch. Thus, the total current passing through the output branches are determined by the bit values and the desired output voltage is obtained with the resistors in each branch. However, this DAC has worse *RC* time constant than a resistive string when they have similar power consumption.

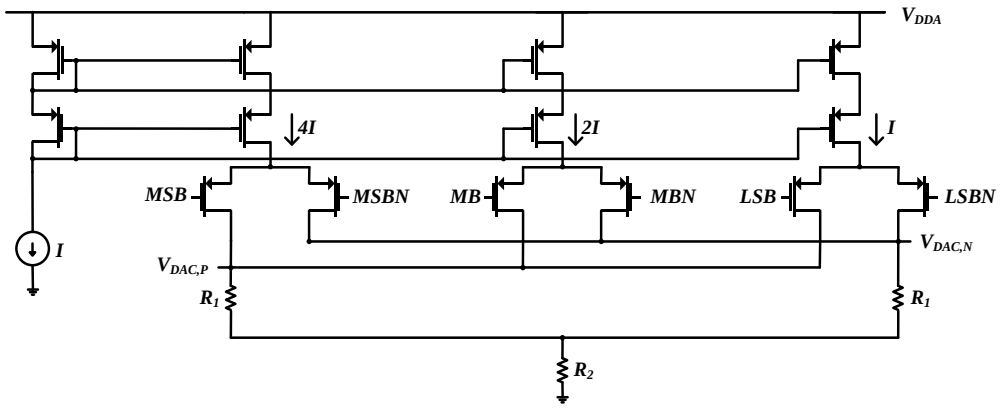

Figure 2.87. Switched DAC circuit.

Capacitive DAC circuits which have been used in 2nd order feed-forward DT SD ADC designs can also be used in the feedback circuits as they are easy to implement directly into the filter block. Nonetheless, the feedback is used in three differential nodes and this causes the design to become very large. Also, the capacitances have to be matched.

Correspondingly, the capacitances cannot be selected to be too small because each switch also has parasitic capacitances which will affect the accuracy of the operation adversely. This leads to high load capacitance in the integrators. Furthermore, any of the capacitive DAC circuits in Figure 2.88 still require a resistive string to operate.

Frequency domain results show that the noise floor became more than quantization noise or the third harmonic became much more after using capacitive DAC when simulated in the ADC. Moreover, a rail to rail capacitive DAC that operates without a resistive string is also investigated, as in Figure 2.89. However, the integrator load capacitance becomes very high because of the feedback capacitance of the integrator especially with the integrator coefficient of 1/3. Despite this, the problem with the high noise floor continued and good results were not achieved.

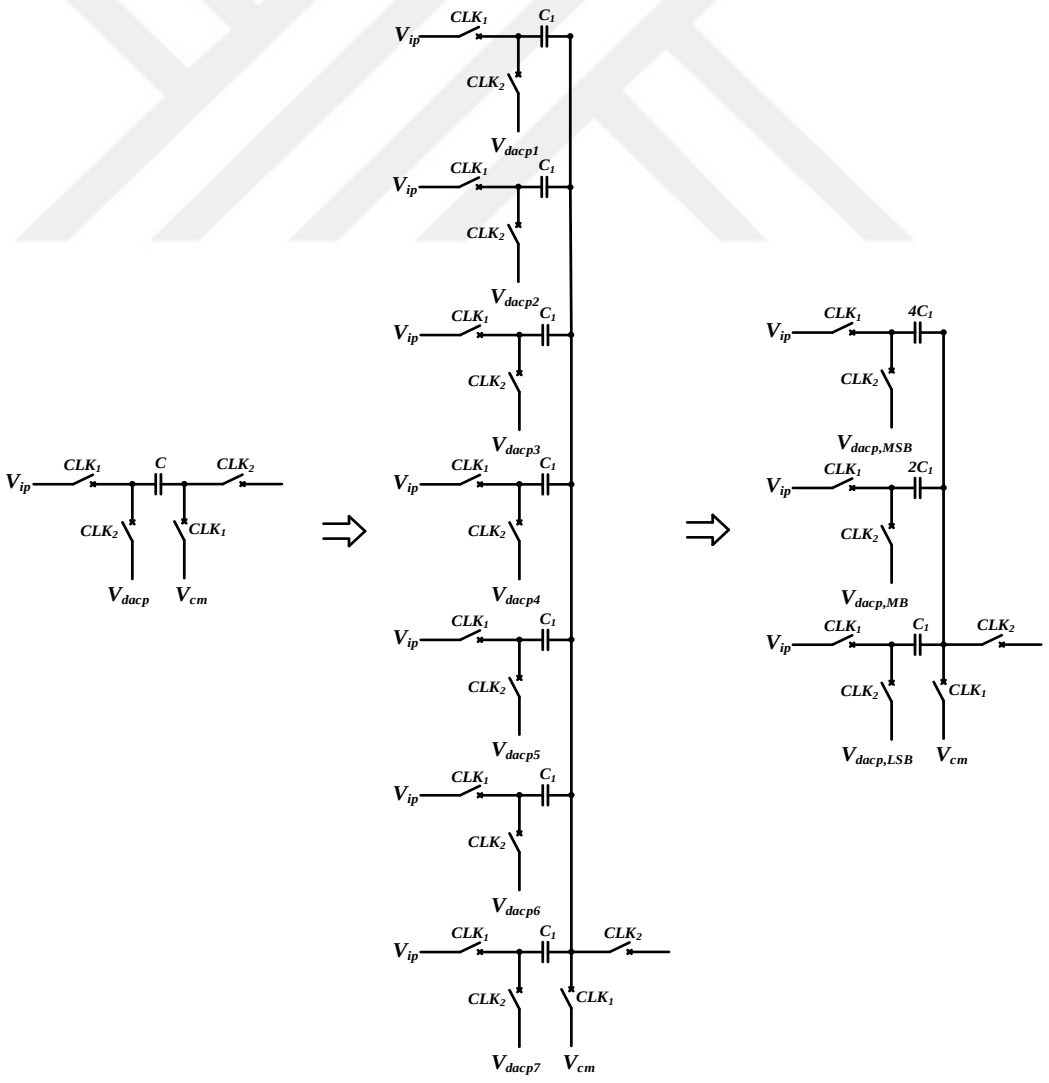

Figure 2.88. Capacitive DAC circuits.

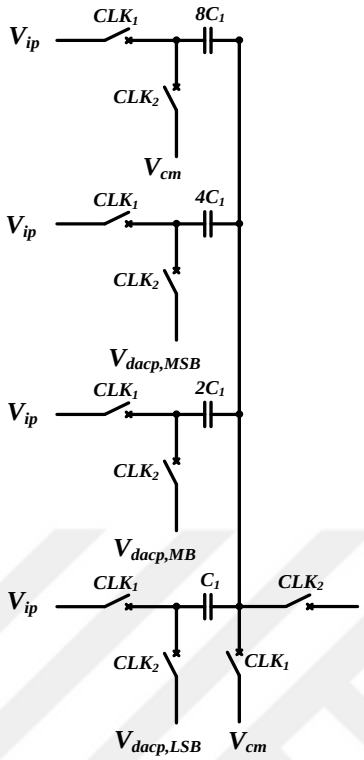

Figure 2.89. Rail to rail capacitive DAC circuit.

As a result, the resistive DAC is the simplest solution as a DAC in the system. The resistances in the DAC can be changed to provide the necessary *RC* time constant to charge the sampling capacitors at each clock cycle effectively. Also, extra resistances are serially connected to the switches, as in Figure 2.90, to have the same output resistances. Here, it is assumed that the resistances of the transmission gates used as switches are smaller than the resistances connected serially. The output resistances of the nodes are adjusted to be the same as calculated in (2.24), (2.25) and (2.26). The DAC is more linear with this method and better results were achieved. The supply voltage is chosen as 1.5 V because it is twice the common mode voltage value. Thus, the DAC levels change between 400 mV and 1100 mV with 100 mV steps. Initially, ideal resistors are used in the DAC to observe the results. According to the resistance values, the SNR value changes due to the third harmonic. For an *R* value of 60 kΩ, the third harmonic is negligible and less than the quantization noise. Furthermore, the current passing through the resistive string is 1.66 µA and the power consumption of the DAC becomes 2.5 µW. However, when polysilicon resistors are implemented, each resistor has parasitic capacitance related to its size. If the resistor width is large, the parasitic capacitances becomes high and the *RC* time constant becomes worse. Therefore, resistance values should be reduced, which increases the power consumption.

The other option is to reduce the width of the polysilicon resistors which results in a deterioration in matching of the resistors. However, the parasitic capacitance will be reduced and *RC* time constant will be sufficiently low to avoid the third harmonic in the frequency domain result. Thus, resistances with different width and length were simulated to observe the results. After many long transient analysis and FFT results, Table 2.3 is formed as a result of these simulations.

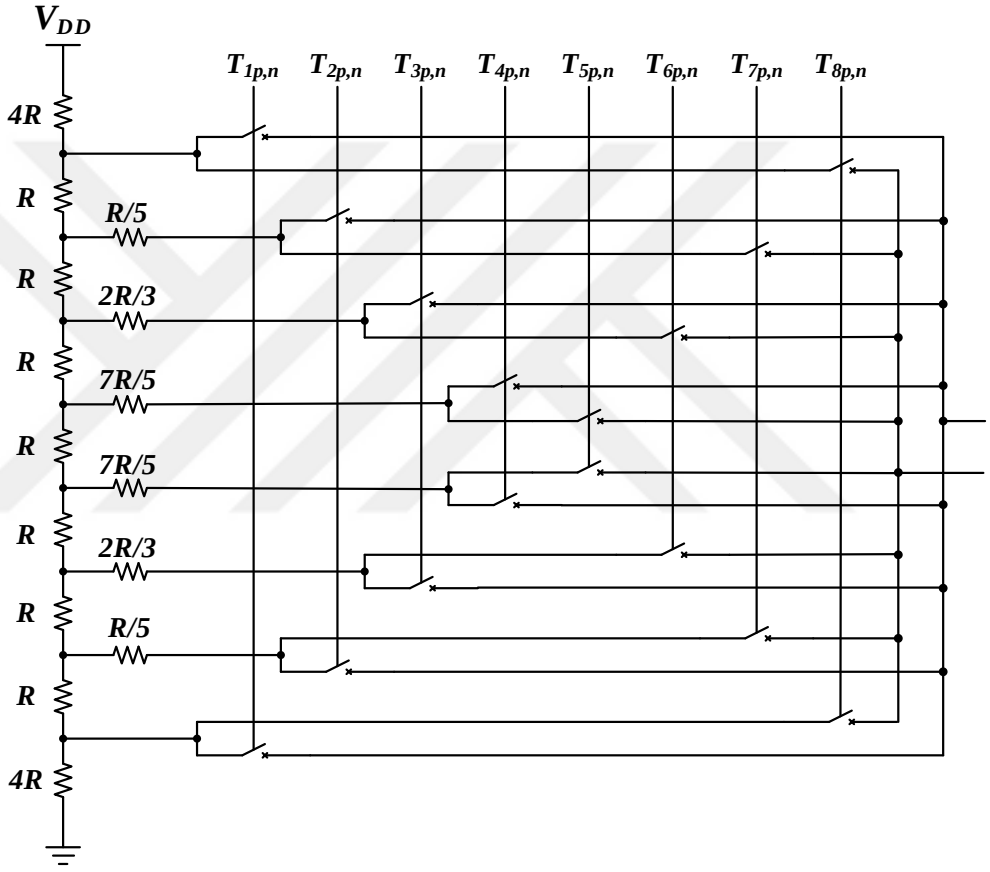

Figure 2.90. Resistive DAC.

$$4R \mathbin{/\!/} \left(R + R + R + \frac{R}{2}\right) + R_{S,ON} = 4R \mathbin{/\!/} \frac{7R}{2} + R_{S,ON} = \frac{28R}{15} + R_{S,ON} \tag{2.27}$$

$$\begin{aligned}(4R + R) \mathbin{/\!/} \left(R + R + \frac{R}{2}\right) + \frac{R}{5} + R_{S,ON} &= \left(5R \mathbin{/\!/} \frac{5R}{2}\right) + \frac{R}{5} + R_{S,ON} \\ &= \frac{5R}{3} + \frac{R}{5} + R_{S,ON} = \frac{28R}{15} + R_{S,ON}\end{aligned} \tag{2.28}$$

$$(4R+R+R) /\!/ \left(R+\frac{R}{2}\right)+\frac{2R}{3}+R_{S,ON}=\left(6R /\!/ \frac{3R}{2}\right)+\frac{2R}{3}+R_{S,ON} \\ =\frac{6R}{5}+\frac{2R}{3}+R_{S,ON}=\frac{28R}{15}+R_{S,ON} \tag{2.29}$$

$$(4R+R+R+R) /\!/ \frac{R}{2}+\frac{7R}{5}+R_{S,ON}=(7R /\!/ 0.5R)+\frac{7R}{5}+R_{S,ON} \\ =\frac{14R}{30}+\frac{7R}{5}+R_{S,ON}=\frac{28R}{15}+R_{S,ON} \tag{2.30}$$

Table 2.3. Simulation results with DACs with different resistances.

Width of the Resistors (µm)	R value (kΩ)	DAC Power Consumption (µW)	SNDR	ENOB	Total Power Consumption (µW)	FoM (fJ/conv)	Chosen ?
ideal	60.00	2.50	93.7	15.27	10.40	5.26	
1.00	30.00	5.00	87.2	14.19	12.90	13.78	
1.00	20.00	7.50	88.9	14.48	15.40	13.52	
1.00	15.00	10.00	88.1	14.34	17.90	17.24	
0.80	40.00	3.75	87.5	14.24	11.65	12.02	
0.60	30.00	5.00	90.6	14.76	12.90	9.31	
0.50	60.00	2.50	85.4	13.89	10.40	13.67	Yes
0.50	40.00	3.75	90.8	14.79	11.65	8.22	
0.50	30.00	5.00	91.9	14.97	12.90	8.02	
0.50	20.00	7.50	93.1	15.17	15.40	8.34	Yes
0.40	60.00	2.50	91.0	14.82	10.40	7.17	
0.40	40.00	3.75	92.8	15.12	11.65	6.53	
0.30	75.00	2.00	92.0	14.99	9.90	6.08	Yes
0.30	60.00	2.50	92.7	15.11	10.40	5.90	
0.30	50.00	3.00	92.9	15.14	10.90	6.04	
0.30	40.00	3.75	94.5	15.41	11.65	5.37	Yes
0.30	30.00	5.00	93.6	15.26	12.90	6.59	

According to the results in Table 2.3, four of the resistance values were chosen and four layouts were prepared. Each of the designs has very good FoM values according to the results of the transient simulations with the extracted parasitic capacitances and resistances of the sub-circuits layouts. Figure 2.91 shows the layout of a 3rd order SD ADC sent to production.

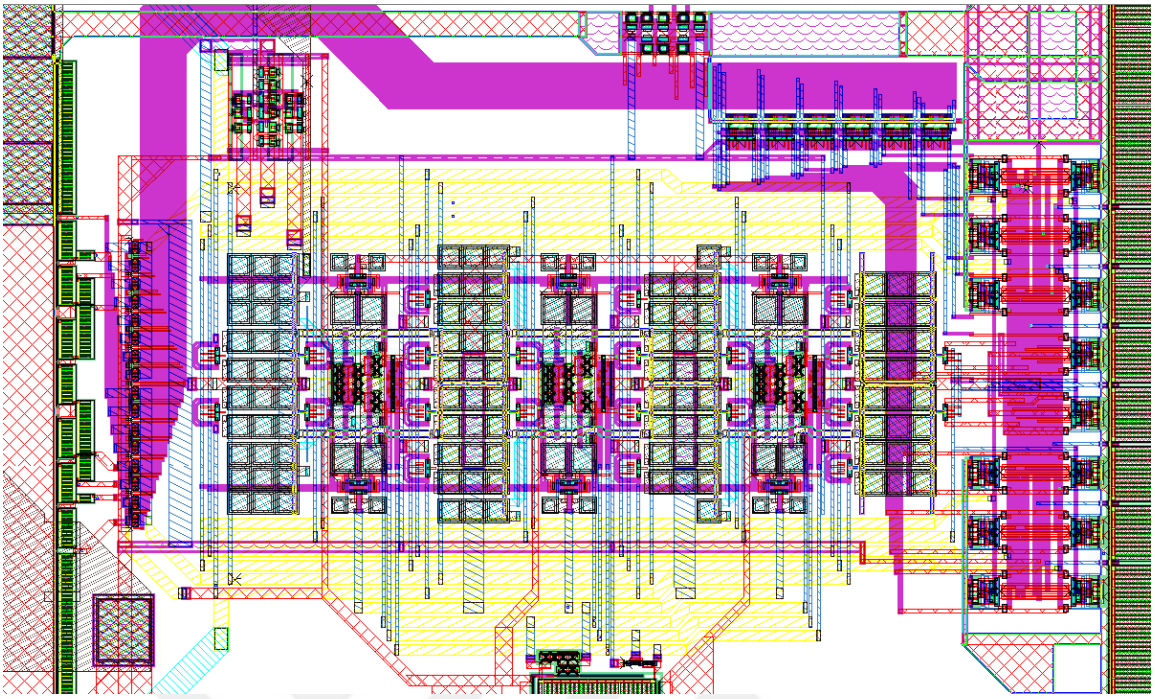

Figure 2.91. Layout of the 3rd order SD ADC.

2.2.2. Updated Feed-Forward 3rd Order 3-Bit SD ADC

Since there were problems in the post-production measurements of the 3rd order SD ADC, a new 3rd order SD ADC architecture is needed. It was deduced that the addition block before the quantizer caused the instability. Thus, the feed-forward path connected to the node before the quantizer was removed in the 3rd order SD ADC and the block diagram in Figure 2.92 is obtained. Here, α represents the gain of the multi-bit quantizer. When the transfer function (2.31) is solved to find Y, (2.32) is obtained if α is chosen to be $3/K$. In that case, the 1st, 2nd and 3rd integrator outputs U, W, and Q are found as (2.33), (2.34) and (2.35). Here, it is assumed that $X(1-z^{-1})$, is very low compared to X and it is negligible as explained before. Thus, both U and W values contain $X(1-z^{-1})$ and the effect of the input at both U and W nodes are ignored because of high OSR. Since U and W nodes are mostly dependent on the ε value, using a multi-bit quantizer makes the ε value very small minimizing the swing at the U and W nodes. However, the 3rd integrator output changes with the input because the 3rd integrator output node Q still contains the input signal X in it. K is the 3rd integrator coefficient as in Figure 2.92, which can be chosen as desired and it doesn't have any effect on the transfer function expect for amplifying the ε as seen in (2.32). Nonetheless, SIMULINK results show that the circuit becomes unstable when K is chosen to be larger than 3. Thus, the K value

was chosen as 2.5 for this design. Moreover, the 3rd integrator differential outputs should be compared with reference voltages in a multi-bit design. To reduce the output swing of the 3rd integrator further, *K* and all the reference voltages in the quantizer are also scaled down. If *K* and all the reference voltages are divided by 2.5, the changes at the outputs of the 1st and 2nd integrators will stay the same while the 3rd integrator output swing is reduced. Therefore, the required output swing margin of the opamps will be low. Keeping these in mind the 3rd order SD ADC architecture was modelled in SIMULINK as in Figure 2.93 and the output swings were quite low as deduced from the histograms in Figure 2.94. The output of the 3rd order SD ADC is depicted in Figure 2.95 and the ADC can achieve 95.9 dB SNR as in Figure 2.96.

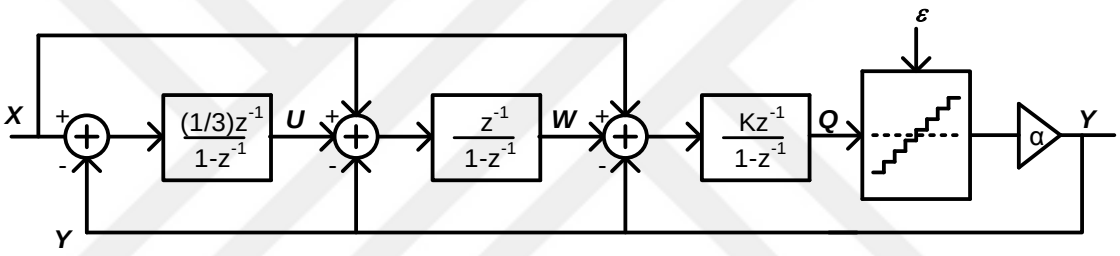

Figure 2.92. Updated 3rd order SD ADC architecture.

$$K/3\,\frac{(X-Y)z^{-3}}{(1-z^{-1})^3}+K\frac{(X-Y)z^{-2}}{(1-z^{-1})^2}+K\frac{(X-Y)z^{-1}}{1-z^{-1}}+\varepsilon=\frac{Y}{\alpha} \tag{2.31}$$

$$Y=Xz^{-3}+3Xz^{-1}(1-z^{-1})+\frac{3}{K}\varepsilon(1-z^{-1})^3 \tag{2.32}$$

$$U=\frac{X}{3}z^{-1}(1-z^{-1})-\frac{3}{K}\varepsilon z^{-1}(1-z^{-1})^2 \tag{2.33}$$

$$W=\frac{X}{3}(1-z^{-1})(3z^{-1}-2z^{-2})-\frac{3}{K}\varepsilon z^{-1}(3-5z^{-1}+2z^{-2}) \tag{2.34}$$

$$Q=Xz^{-3}+3Xz^{-1}(1-z^{-1})-\frac{3}{K}\varepsilon z^{-3}-\frac{9}{K}\varepsilon z^{-1}(1-z^{-1}) \tag{2.35}$$

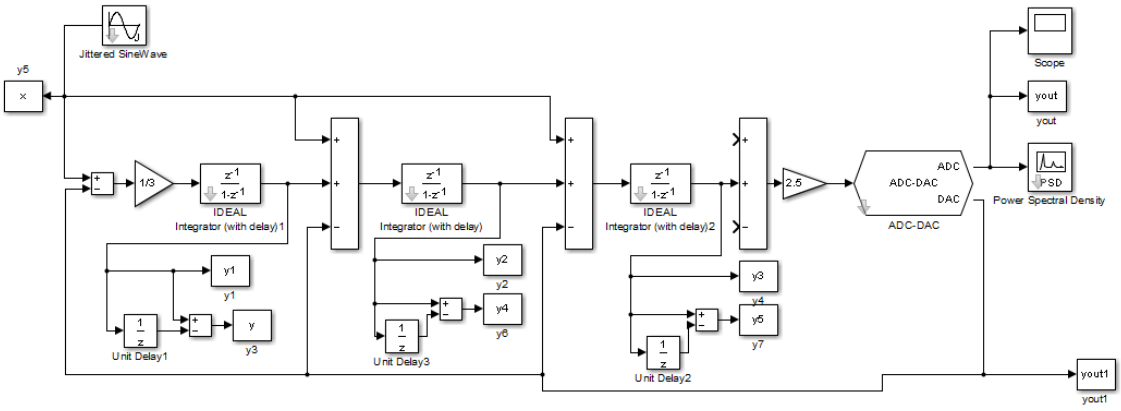

Figure 2.93. Updated 3rd order SD architecture in SIMULINK.

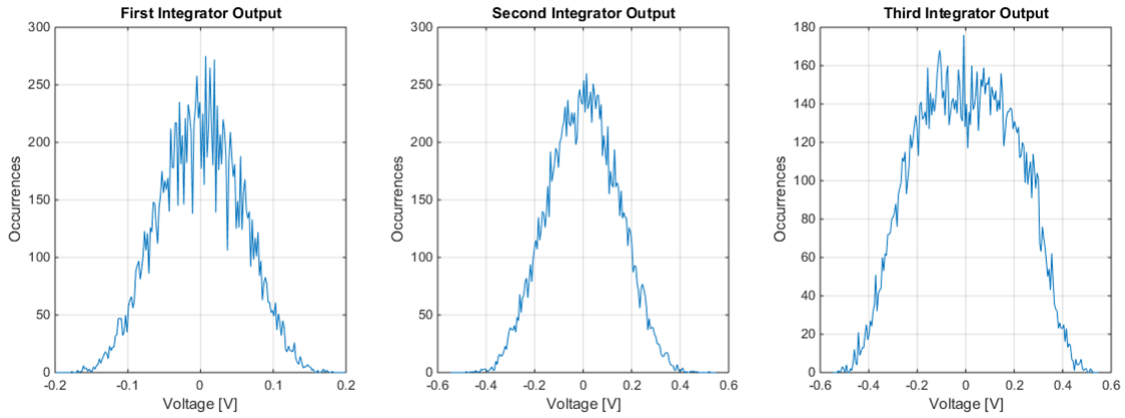

Figure 2.94. Integrator output histograms of the updated 3rd order 3-bit SD ADC for input amplitude and reference ratio of 0.6.

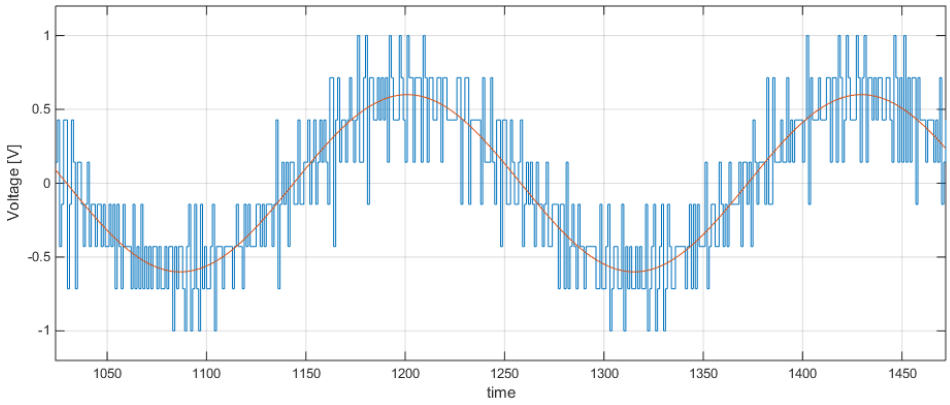

Figure 2.95. The output of the updated 3rd order 3-bit SD ADC.

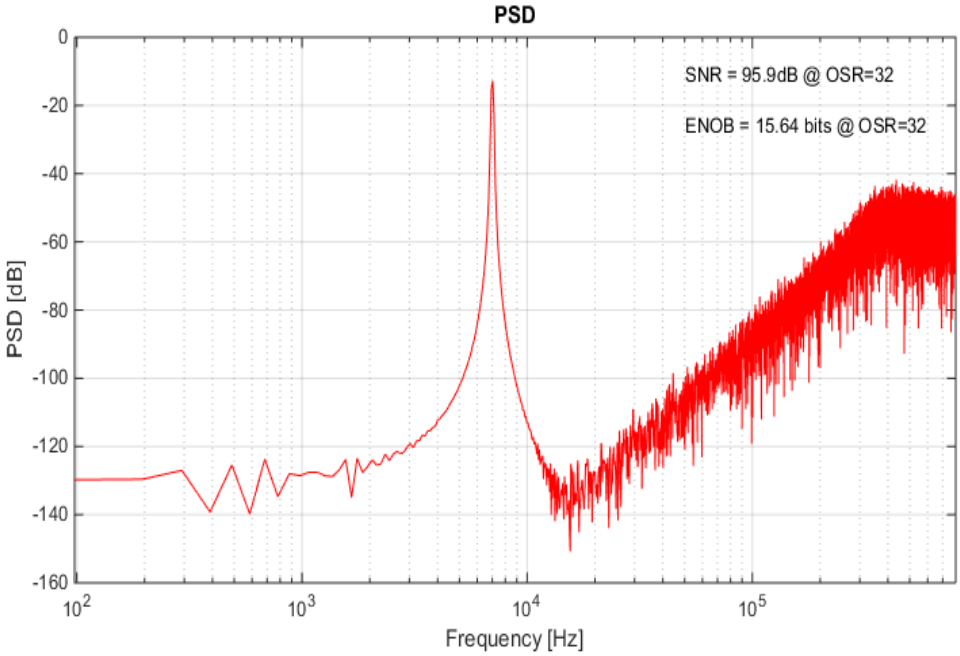

Figure 2.96. FFT result of the updated 3rd order 3-bit SD ADC.

The updated 3rd order 3-bit SD ADC circuit schematic is depicted in Figure 2.97. The addition block before the quantization is removed in the updated design. Thus, only 7 comparators with double the clock frequency are used here instead of 14 comparators. The clock signal is now transferred to a D flip-flop, which is included before the clock distribution circuit to obtain the quantizer clock and to improve the clock duty cycle. Moreover, the 3rd integrator output swing is reduced by reducing the 3rd integrator coefficient to 1 and the ADC reference levels by 2.5 instead of selecting the 3rd order integrator coefficient as 2.5. In this case, the new reference voltages will be between 630 mV to 870 mV with 40 mV steps instead of 450 mV to 1050 mV with 100 mV steps. The reference values are generated via a resistive string. Furthermore, the DAC references are generated through the same resistive string structure but the *R* value is chosen as 33k. Also, the telescopic cascode opamps are updated. Each opamp has 52 dB gain and 4 MHz bandwidth for 0.5 pF loads while 1 µA is flowing through each branch. The bias circuit also has 1 µA current flowing through its branch. Finally, the layout is prepared as in Figure 2.98.

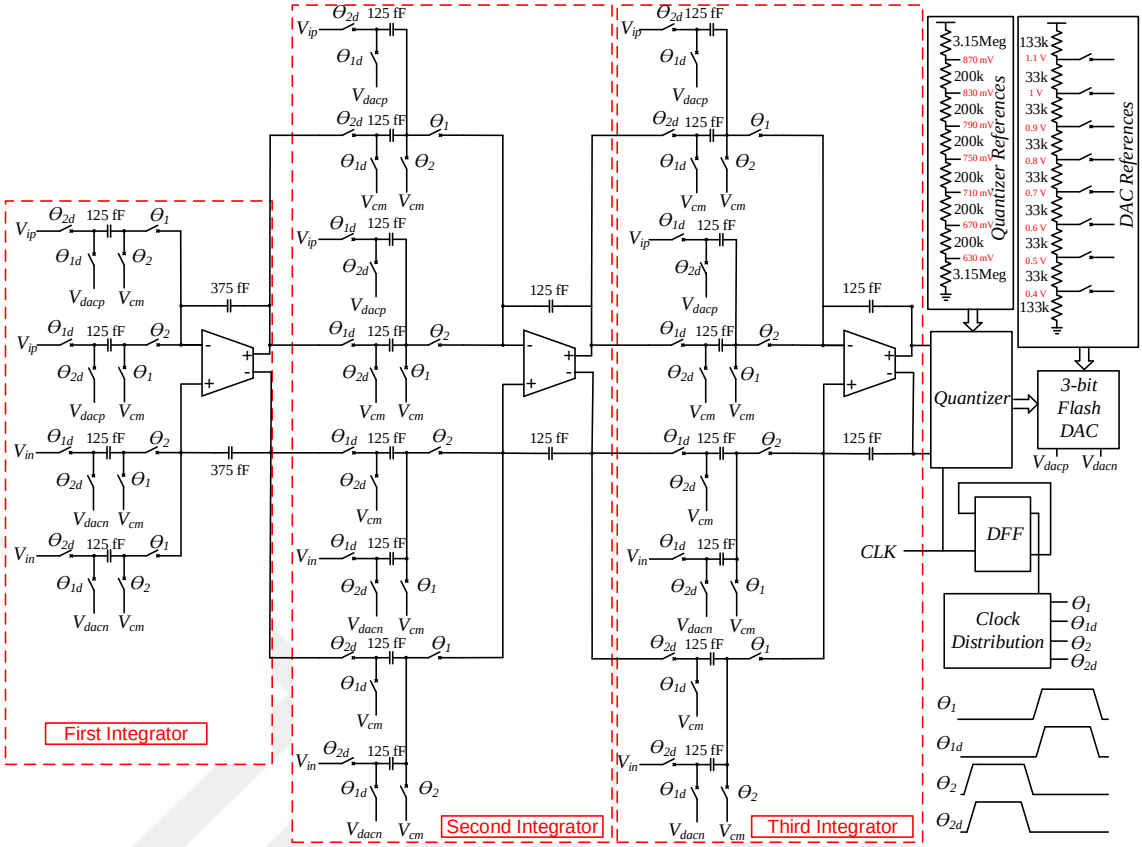

Figure 2.97. Updated 3rd order 3-bit SD ADC schematic.

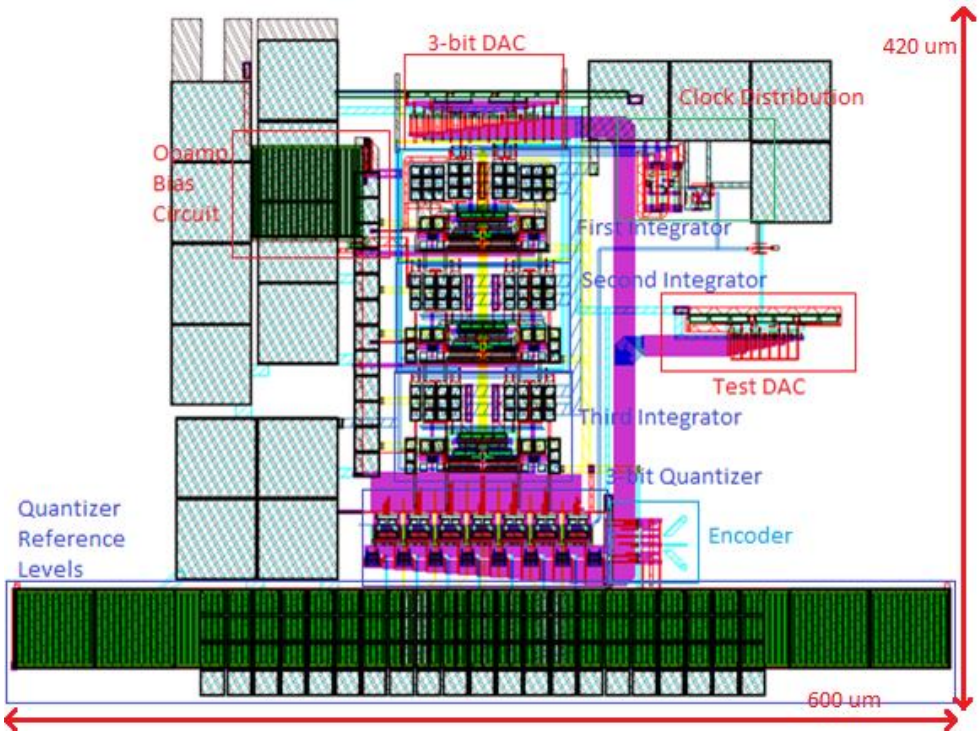

Figure 2.98. Layout of the updated 3rd order 3-bit SD ADC.

Differential sinusoidal signals with 200 mV amplitude are applied as inputs to the 3rd order SD ADC. Figure 2.99 shows the post-layout FFT result of the ADC while Figure 2.100 shows the FFT result with noise included. Figure 2.101 shows the SNDR of the FFT results with different values of inputs with and without noise added. Figure 2.102 is the detailed version of the same graph for high input amplitudes. Interestingly, the ADC oscillates after some time for sinusoidal inputs with 230 mV amplitude when the noise is added. This explains the sudden drop in Figure 2.101. However, FFT results show that up to 78.8 dB SNDR is achieved when noise is included. For process variation, post-layout simulations with slow-slow and fast-fast transistor models are also performed. When noise is added, the SNDR reaches 83.5 dB with slow-slow models as in Figure 2.103 while it is 78.8 dB with fast-fast models as depicted in Figure 2.104. Table 2.4 shows the detailed power consumption of the sub-circuits in the ADC. A 78.8 dB SNDR with 28.2 µW power consumption leads to 79 fJ/conv FoM value for typical models. According to slow-slow models, FoM is calculated as 42.4 fJ/conv for 83.5 dB SNDR and 26 µW power consumption. However, fast-fast models increase FoM value back to 86.6 fJ/conv for 78.8 dB SNDR and 30.9 µW power consumption.

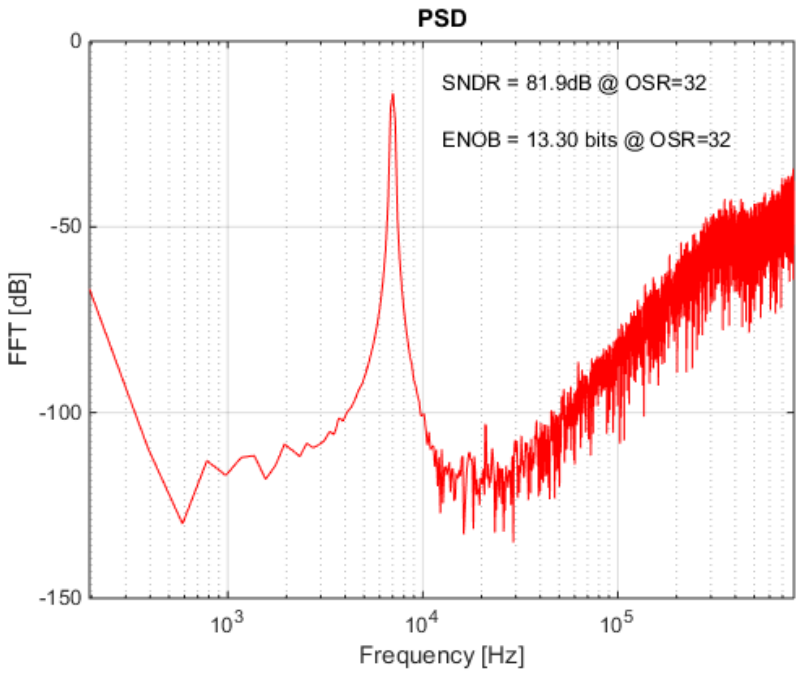

Figure 2.99. Post-layout FFT results of the 3rd order 3-bit SD ADC for 200 mV differential sine inputs.

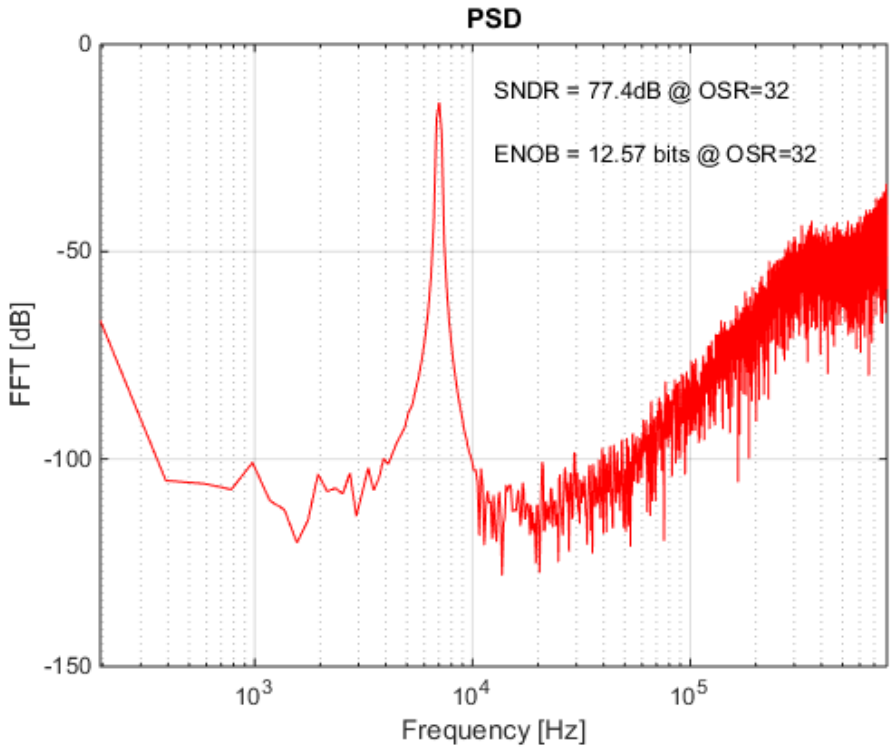

Figure 2.100. Post-layout FFT results of the 3rd order 3-bit SD ADC for 200 mV differential sine inputs with noise included.

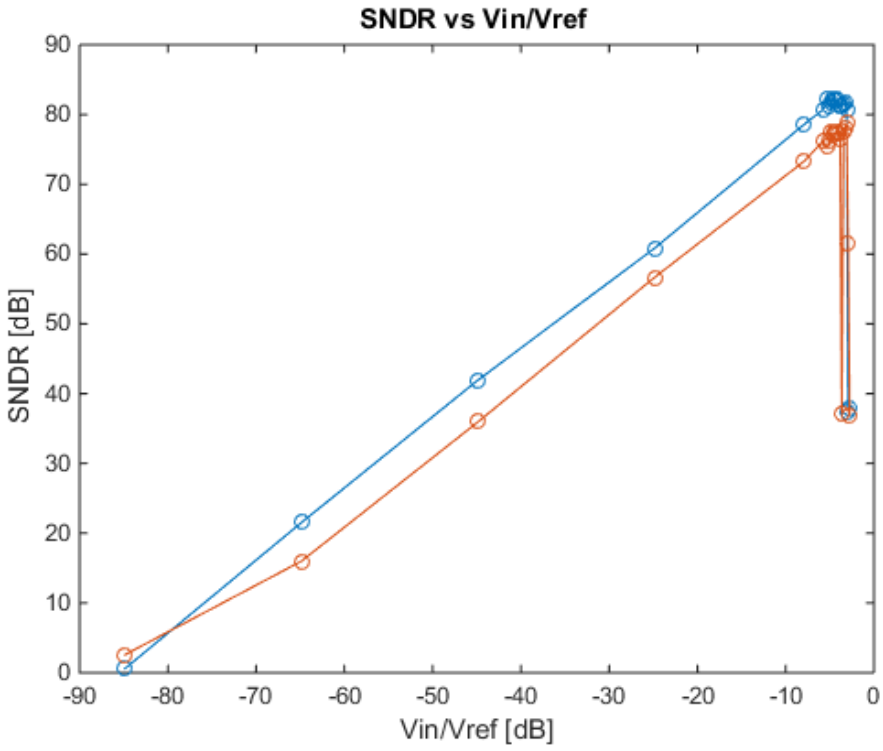

Figure 2.101. The change of SNDR with the input amplitude.

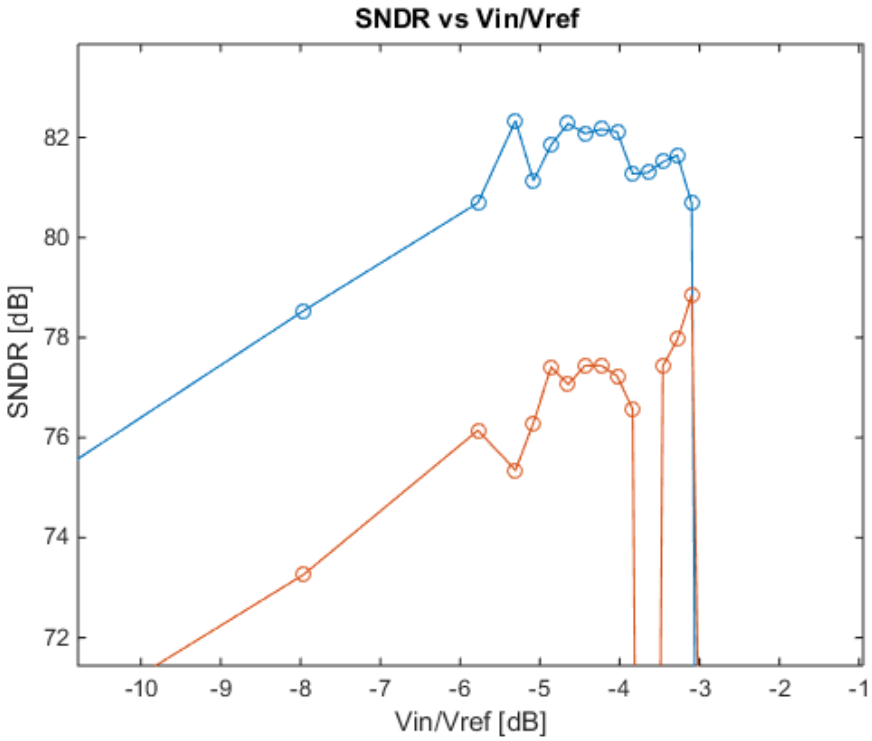

Figure 2.102. The change of SNDR with the input amplitude for high inputs.

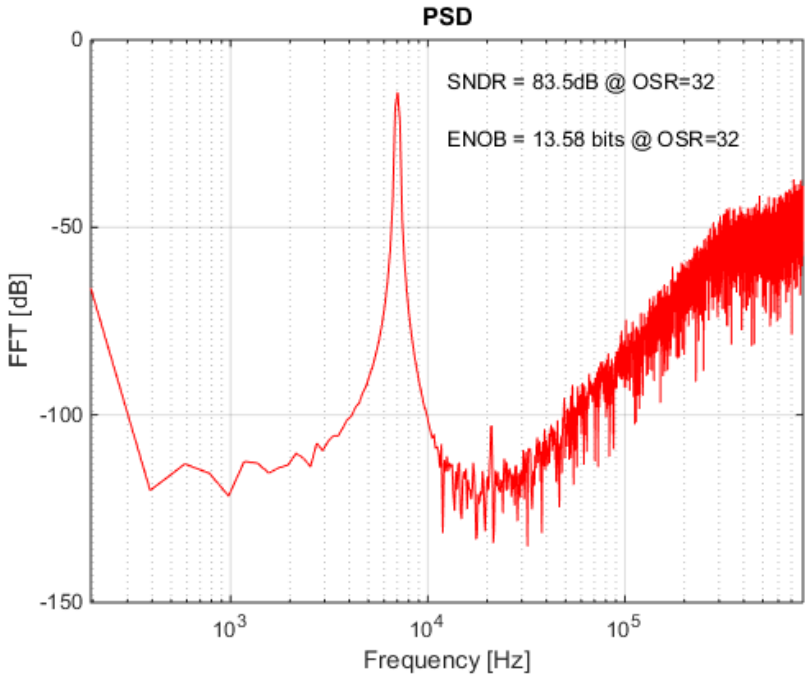

Figure 2.103. Post-layout FFT results of the 3rd order 3-bit SD ADC for 200 mV differential sine inputs with slow-slow transistor models and noise included.

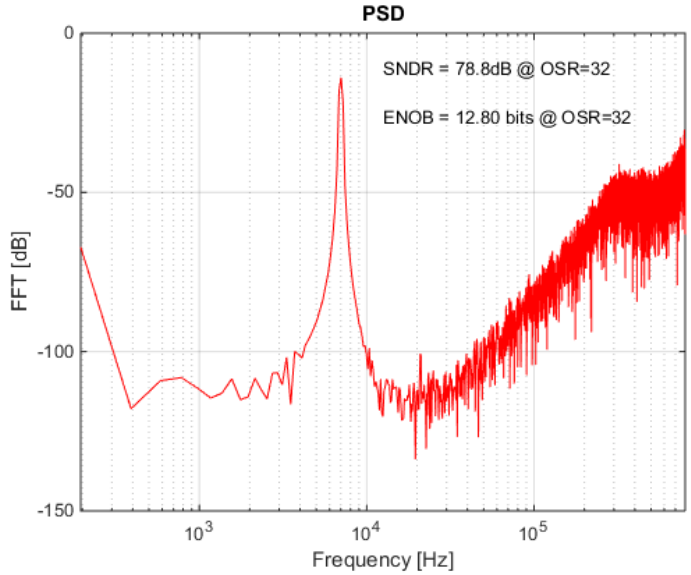

Figure 2.104. Post-layout FFT results of the 3rd order 3-bit SD ADC for 200 mV differential sine inputs with fast-fast transistor models and noise included.

Furthermore, input frequency is changed as the input amplitude is kept constant. The SNDR stayed around 83 dB without active device noise and 78 dB with the noise added as seen in Figure 2.105.

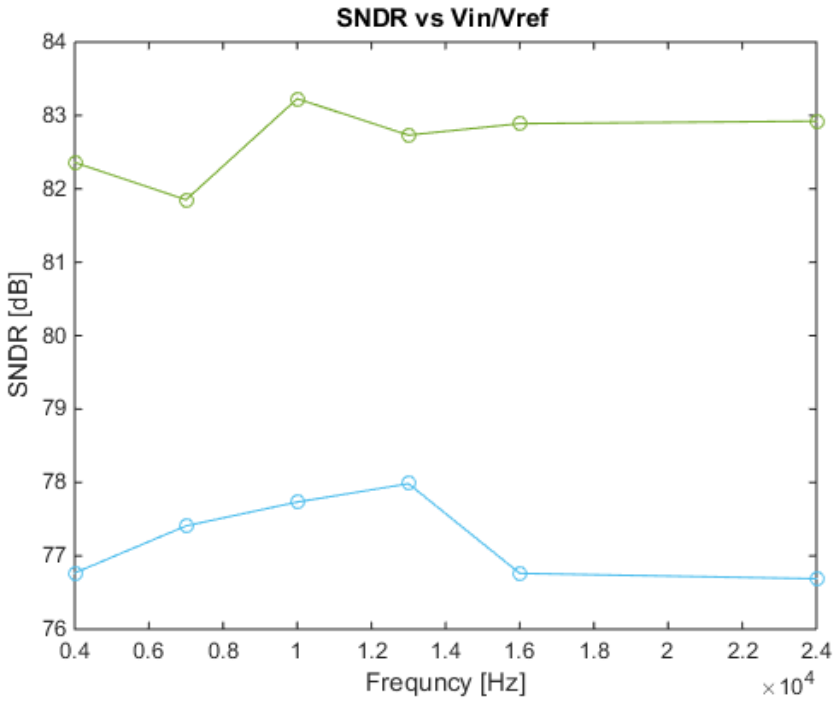

Figure 2.105. The change of SNDR with input frequency when noise is included and not included.

Table 2.4. Power consumption of the 3rd order 3-bit SD ADC.

SD ADC Models	Integrator & Bias Circuits (µW)	Clock Distribution Circuits (µW)	DAC References (µW)	Comparators & Digital Part (µW)	Total (µW)	SNDR (dB)	FoM (fJ/conv)
Regular	11.7	4.05	7.05	5.4	28.2	78.8	79
Slow-Slow	10.2	3.75	7.05	5	26	83.5	42.4
Fast-Fast	13.1	4.45	7.05	6.3	30.9	78.8	86.6

2.3. DT MASH SD ADC Types

Using MASH SD ADCs is another option to achieve high order noise shaping. As stability is a big issue for SD ADCs with greater than 2nd order, two or more SD ADCs can be used to achieve higher order noise shaping. Therefore, MASH SD ADCs are usually designed as 2-1, 2-2 or even 2-1-1. Figure 2.106 is a proposed 2-1 MASH SD ADC obtained by using the 2nd order SD ADC of Figure 2.47. Here, the quantization noise ε_1 is obtained by subtracting the quantizer input from the output of the 1st SD ADC with the necessary coefficients according to the transfer function of the 1st SD ADC. Subsequently, the quantization error is used as the input of the other 1st order SD ADC. By using the SD ADC outputs (2.36) and (2.37), the overall SD ADC output (2.38) is achieved mathematically with digital circuits. Here, the quantization noise of the 1st SD ADC ε_1 is removed by this operation and the quantization noise of the 2nd SD ADC ε_2 has 3rd order noise shaping. The quantization is usually multi-bit in MASH SD ADCs because output swings of the integrators increase as the order of the ADC gets higher. Since each additional bit in the quantizer halves the quantization noise, integrator output swings reduce due to the dependency to the quantization noise when multi-bit quantization is performed. However, 1-bit quantization is used here and the integrator coefficients are lowered, reducing the integrator output swings alternatively. Furthermore, testability is easier with 1-bit quantization. Afterwards, the circuit is modelled in SIMULINK as in Figure 2.107. The integrator output histograms become as depicted in Figure 2.108 when the input amplitude to DAC feedback reference ratio is 0.3. The swing in the outputs as shown by the histograms increases when this ratio becomes larger. Therefore, this ratio is kept low even though SNR

might increase with larger ratio. The FFT of the simulation results of the 2-1 MASH ADC is shown in Figure 2.109, obtaining an SNR value of 94.2 dB.

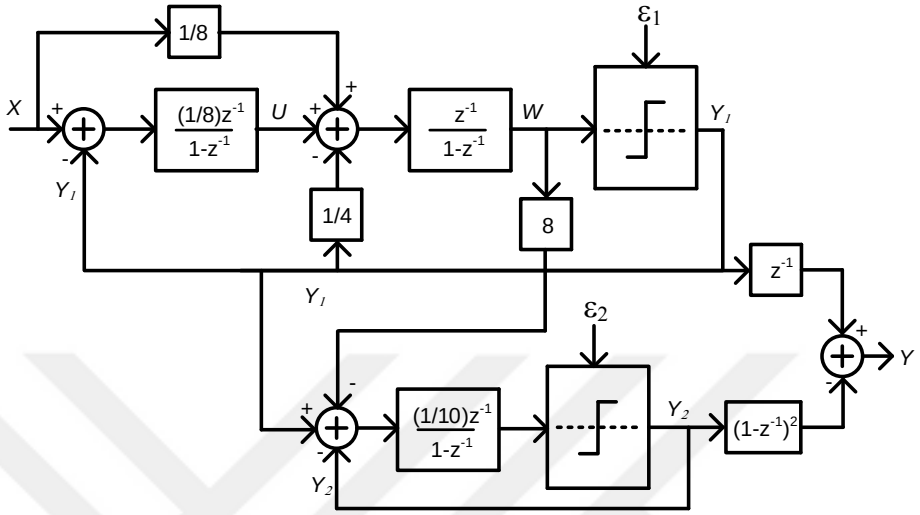

Figure 2.106. 2-1 MASH SD ADC.

$$Y_1 = Xz^{-1} + \varepsilon_1(1 - z^{-1})^2 \tag{2.36}$$

$$Y_2 = \varepsilon_1 z^{-1} + \varepsilon_2(1 - z^{-1}) \tag{2.37}$$

$$Y = Y_1 z^{-1} - Y_2(1 - z^{-1})^2 = Xz^{-2} - \varepsilon_2(1 - z^{-1})^3 \tag{2.38}$$

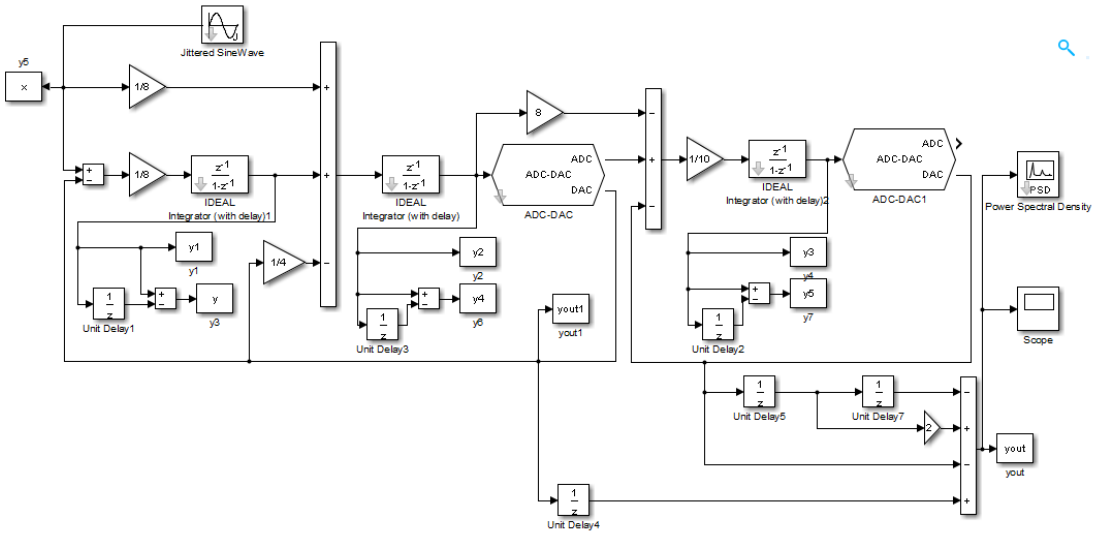

Figure 2.107. 2-1 MASH SD ADC in SIMULINK.

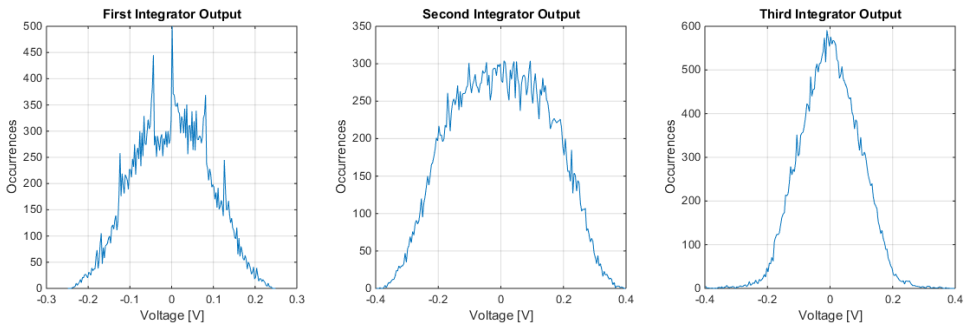

Figure 2.108. The integrator output histograms of the 2-1 MASH SD ADC in SIMULINK.

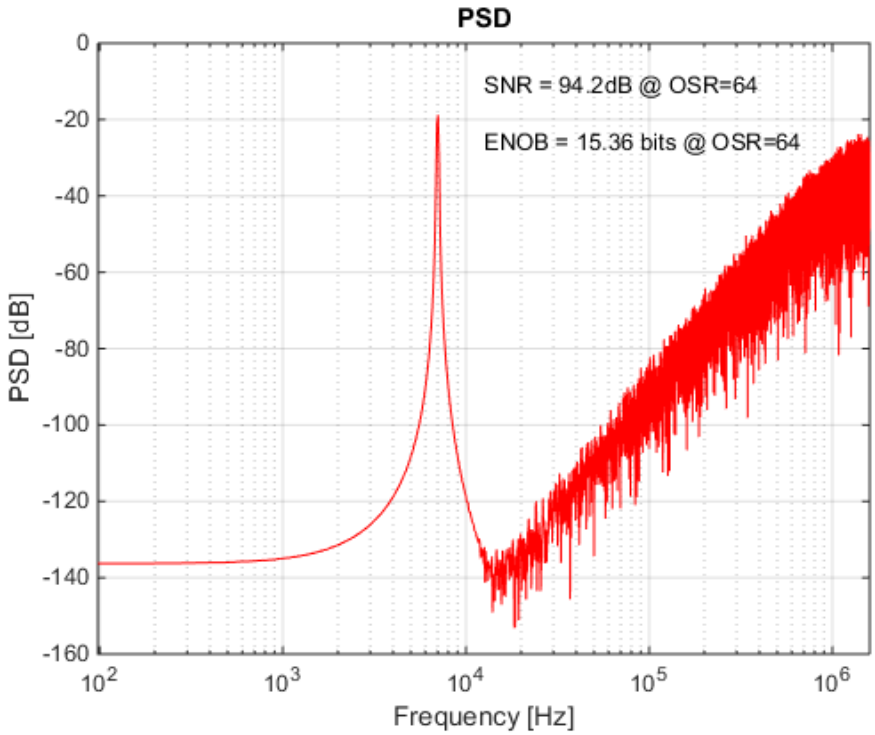

Figure 2.109. FFT of the 2-1 MASH ADC in SIMULINK.

The circuit in Figure 2.110 is added to Figure 2.31 to bring the 2-1 MASH SD ADC together. The quantizer outputs of the ADCs are added outside the chip via a MATLAB code. Thus, two 1-bit outputs are taken as output data instead of a 3-bit output. In this design, the load of the integrators are larger than the 2nd order ADC in Figure 2.47. Therefore, the folded cascode opamps are replaced with the high power versions according to the AC analysis of the folded cascode opamps with different sizes in Figure 2.42. Afterwards, the layout of the ADC is prepared as in Figure 2.111. FFT of the post-layout simulations in Figure 2.112 show that 2-1 MASH ADC have 83.5 dB SNDR and 225 fJ/conv FoM.

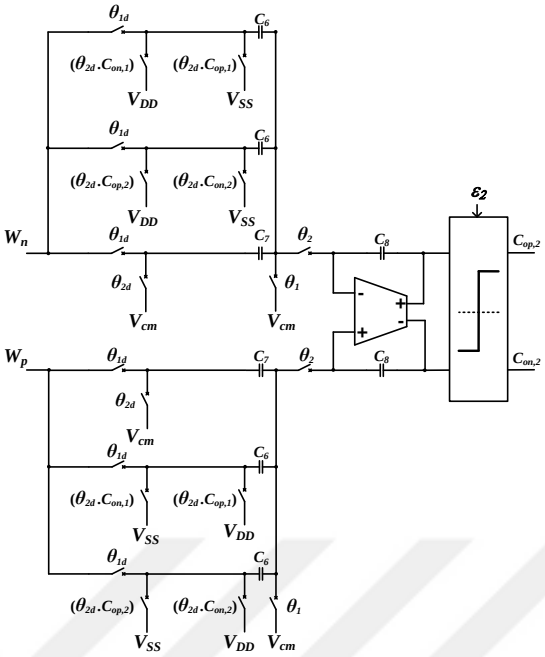

Figure 2.110. The schematic of the additional part for 2-1 MASH SD ADC.

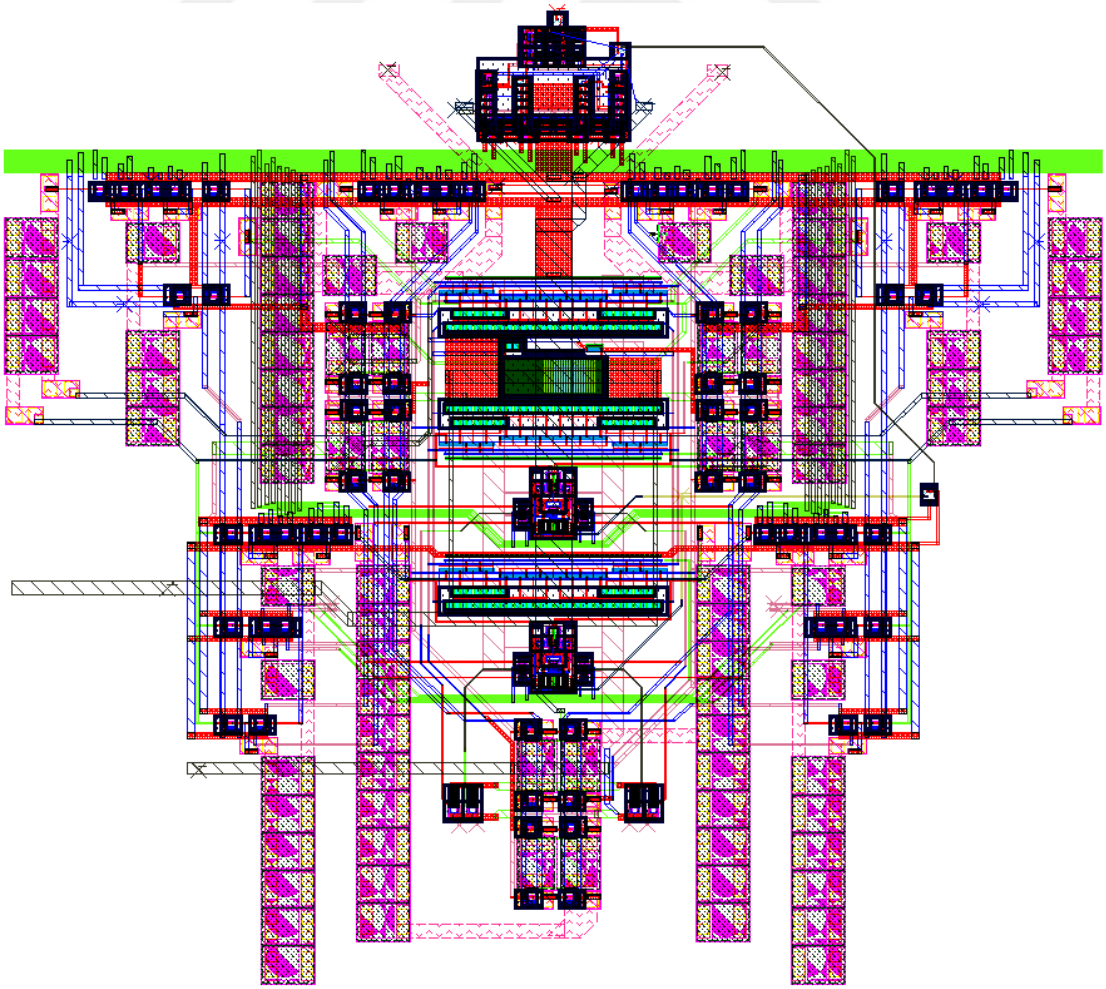

Figure 2.111. The layout of the 2-1 MASH SD ADC.

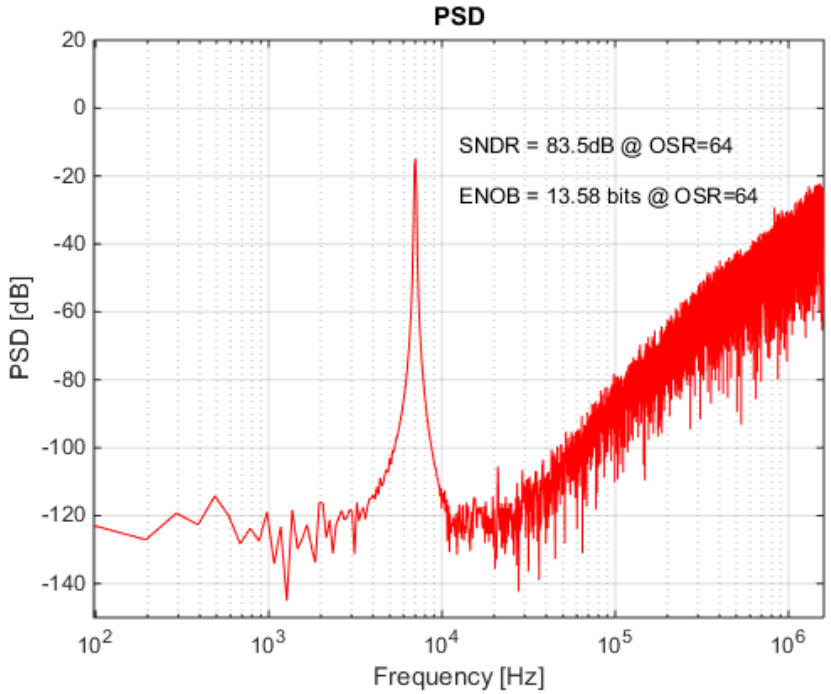

Figure 2.112. FFT of the 2-1 MASH after post-layout simulations.

2.4. DT SD ADC Summary

In this chapter, 2nd and 3rd order DT SD ADCs with single-bit and multi bit quantizers are studied. Different methods such as conventional and proposed feed-forward path and SAR ADC quantization are applied to lower the power consumption even more. Likewise, a 3rd order SD ADC with 2-1 MASH architecture is also studied. Many opamps such as telescopic cascode, folded cascode and class AB opamps are used in the integrators to optimize the power consumption for the desired performance. In some designs, double sampling method is used to relax the specifications of the opamps. Different type of DACs are used in each design according to the structure of the ADC and the resolution of the quantization. The layouts of the DT ADCs are prepared and post-layout simulations show that the DT ADCs have very high performance for their power consumption compared to the ADCs in the literature.

3. CONTINOUS TIME SIGMA DELTA ANALOG DIGITAL CONVERSION

The CT Sigma Delta ADCs have certain advantages and disadvantages compared to DT Sigma Delta ADCs. The DT integrators inside the ADC are replaced with CT integrators. Now, the transfer function is in the *s*-domain instead of *z*-domain and the noise should be shaped in *s*-domain.

Slew rate is less of a problem with CT SD ADCs because a capacitor is not required to be filled within a clock period as in DT ADCs. Since the slew rate requirements are relaxed, a large OSR can be used to have high SNR values. Nevertheless, opamps are not ideal and have limited gain as a result of which the integration operation ceases at low frequencies [19]. Hence, the behaviour is similar to being attenuated at low frequencies and the ratio of the signal path to feedback path becoming lower than the desired value affecting the transfer function. Opamps also have limited gain-bandwidth product which adds another pole to the system. This pole should be very far away from the sampling frequency so that it won't affect the integration at the same frequency. The Bode plots of an ideal and a real ideal integrator is shown in Figure 3.1

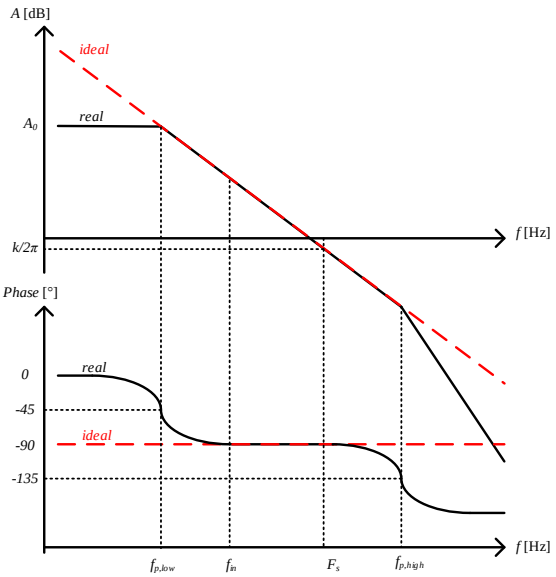

Figure 3.1. The Bode plots of an ideal and a real integrator.

In addition, CT SD ADCs are vulnerable to clock jitter. Multi-bit ADC design is undesirable in many cases since the DAC linearity is crucial. DAC power consumption might also increase when the design is multi-bit. Therefore, an optimum design for our case is a 2nd order single-bit design with OSR 128 or 256 to achieve more than 90 dB SNR.

[20] introduces the CT equivalents of *z*-domain integrators as seen in (3.1) and (3.2) for NRZ feedback DAC. These transformations might be applied to the DT applications. Hence, DT integrators might be replaced with CT integrators and the desired STF and NTF can be obtained.

$$\frac{k\mathrm{z}^{-1}}{1-\mathrm{z}^{-1}} = k\frac{F_s}{s} \tag{3.1}$$

$$\frac{k\mathrm{z}^{-2}}{(1-\mathrm{z}^{-1})^2} = k\frac{½sF_s + F_s}{s^2} \tag{3.2}$$

Figure 3.2 is a common architecture for the 2nd order CT SD ADCs in the literature. The output swing of the first integrator can be reduced by choosing k_{11} and k_{12} as 1/8. Hence, k_{21} becomes 2/3 and k_{22} becomes 1/8 to match the coefficients and the structure is investigated in SIMULINK as in Figure 3.3. According to these simulations, 85.8 dB SNR is achieved when OSR is chosen 128 as in Figure 3.4. The output histograms of the integrators in Figure 3.5 show that the output swings are quite low. If the OSR is increased to 256, the obtained SNR achieved is increased to 98.5 dB as in Figure 3.6 but, the output histograms in Figure 3.7 are similar to these in Figure 3.5.

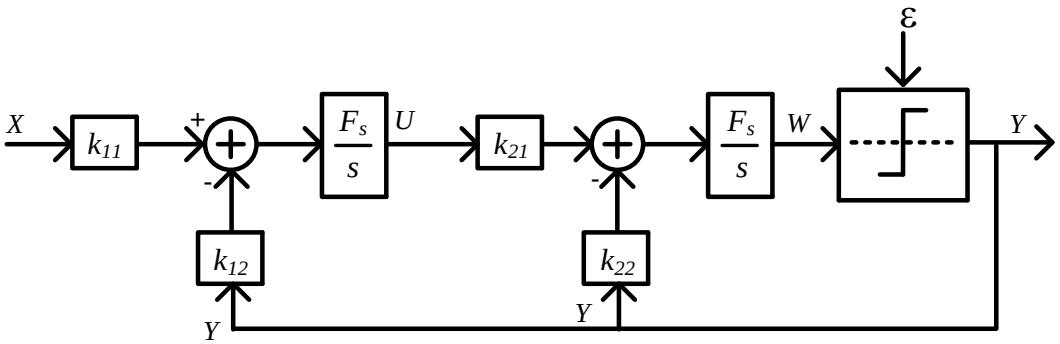

Figure 3.2. CT 2nd order SD ADC.

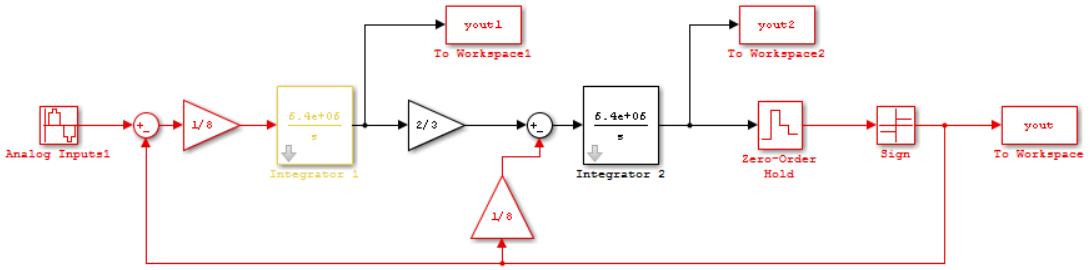

Figure 3.3. CT 2nd order SD ADC in SIMULINK.

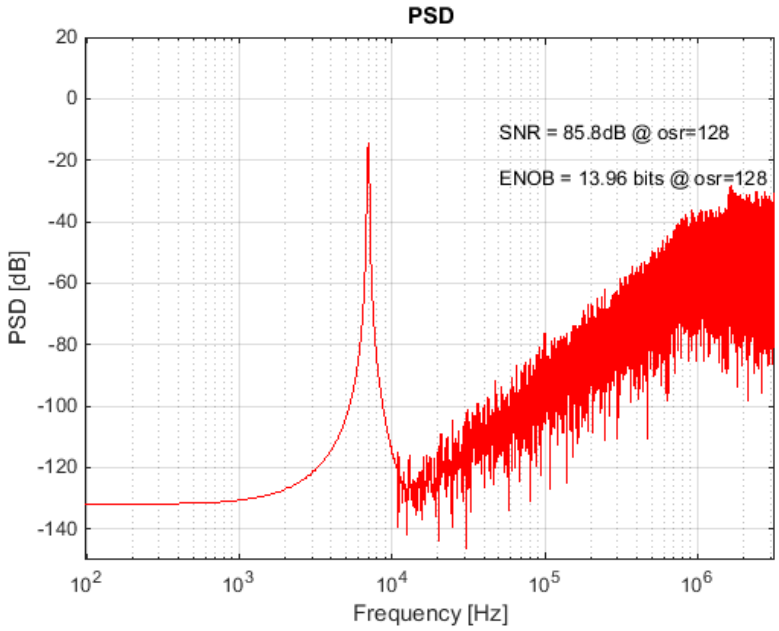

Figure 3.4. FFT of the CT 2nd order SD ADC in SIMULINK.

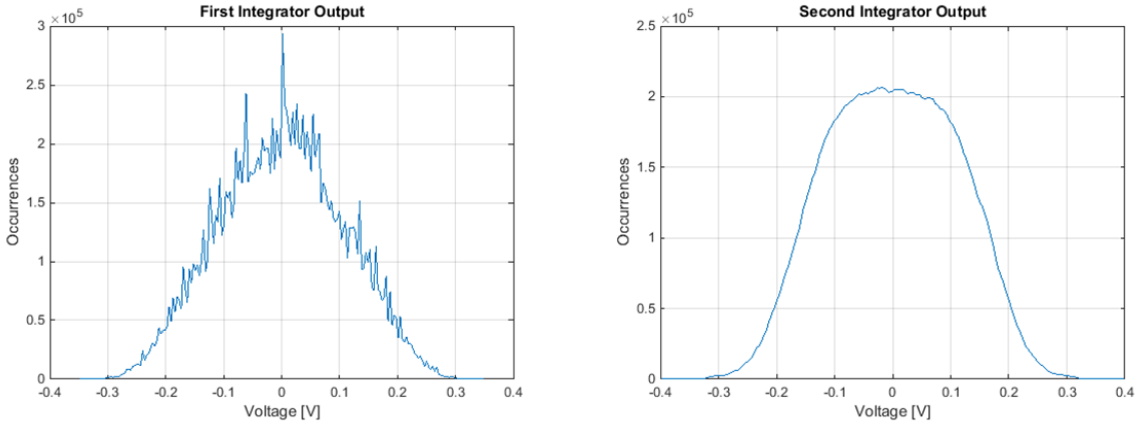

Figure 3.5. Integrator output histograms of the CT 2nd order SD ADC in SIMULINK.

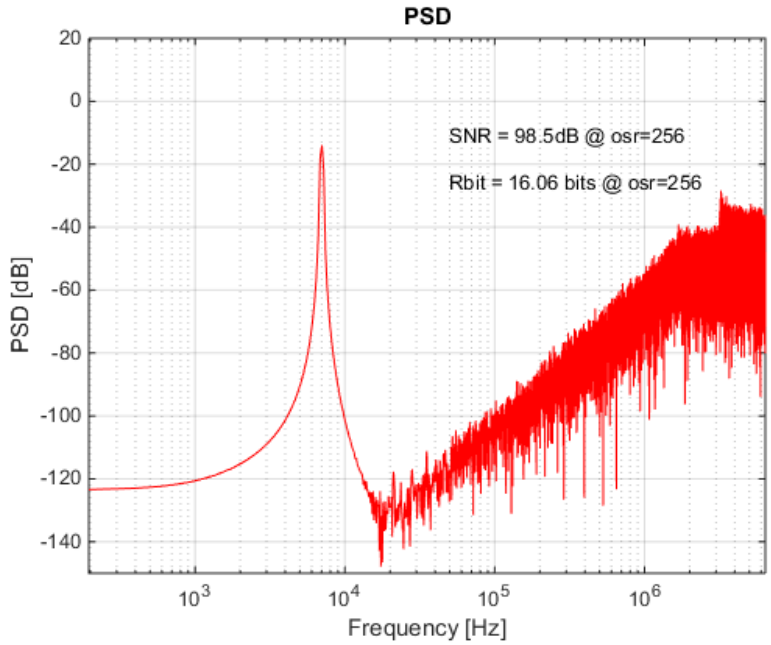

Figure 3.6. FFT of the CT 2nd order SD ADC in SIMULINK for 256 OSR.

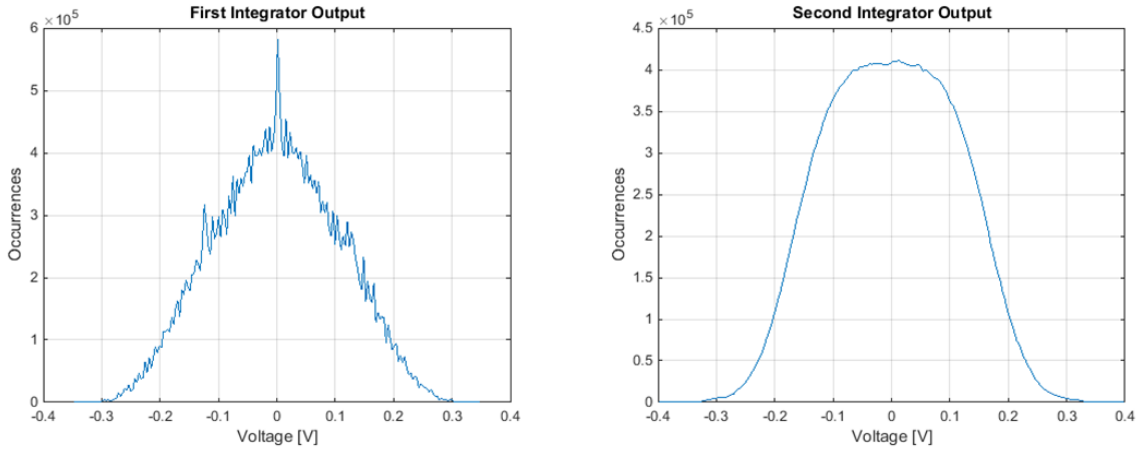

Figure 3.7. Integrator output histograms of the CT 2nd order SD ADC in SIMULINK for 256 OSR.

Using the transformation methods introduced in [20] and the *z*-domain designs, a new feed-forward 2nd order CT SD ADC in Figure 3.8 is achieved. It is based on the DT SD ADC architecture in Figure 2.49. The feed-forward path of the input is removed from this design and the DT integrators are replaced with CT integrators. Afterwards, the coefficients are tuned via the SIMULINK results of the CT ADC. The best performance results are obtained when k_1 is chosen 0.2 while k_2 is chosen 5/9. Here, the performance does not change

when k_1 changes and the first integrator operates like a gain stage. Thus, k_1 is chosen a small value to attenuate the signal so that the integrator output becomes swing low. Even if k_1 changes dramatically due to process variations, the ADC operates properly and the desired noise shaping is achieved. Furthermore, there is still noise shaping even if k_2 is reduced to 0.4, or is increased to 0.65 with a of slight performance drop. The transfer function of the filter of the proposed structure is calculated as (3.3).

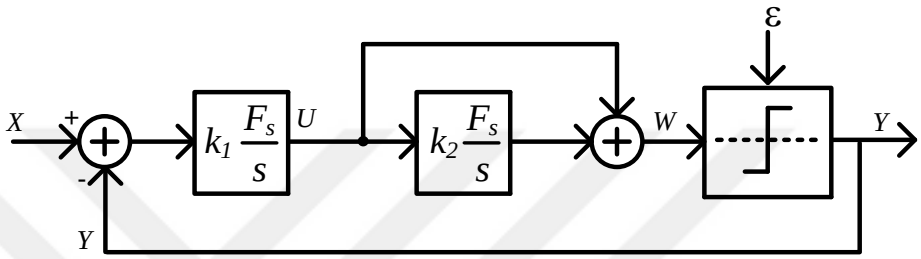

Figure 3.8. Proposed 2nd order CT SD ADC.

$$TF = k_1 \frac{F_s}{s}\left(1 + k_2 \frac{F_s}{s}\right) \tag{3.3}$$

The proposed CT 2nd order SD ADC is observed in SIMULINK as shown in Figure 3.9. For an OSR of 128, 83.6 dB SNR is achieved as shown in Figure 3.10 and the integrator output histograms are laid out in Figure 3.11. The SNR of the SD ADC increases up to 96.6 dB when an OSR of 256 is chosen as in Figure 3.12, while the integrator output histograms stays similar as shown in Figure 3.13.

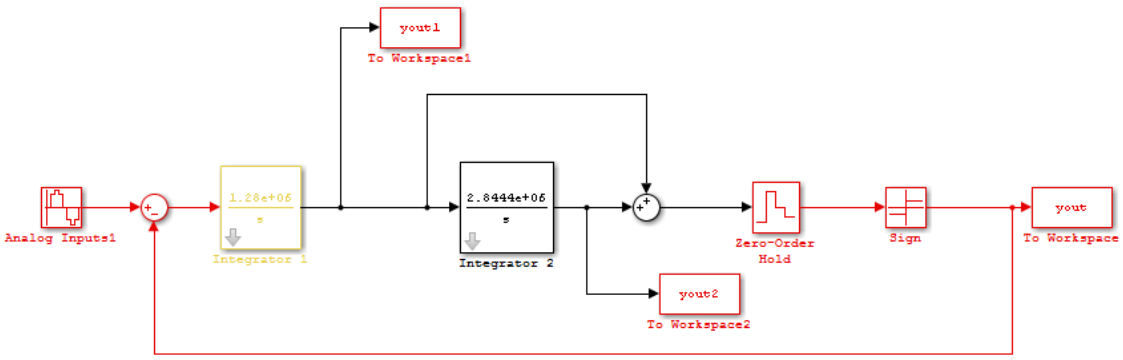

Figure 3.9. The proposed 2nd order CT SD ADC in SIMULINK.

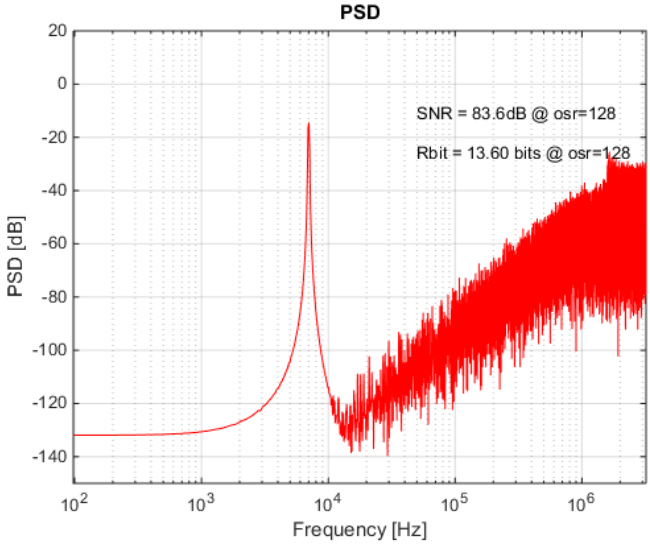

Figure 3.10. FFT of the 2nd order CT SD ADC in SIMULINK for 128 OSR.

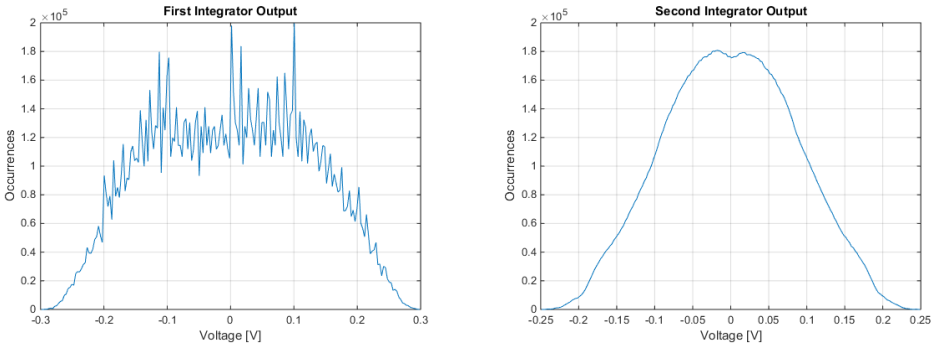

Figure 3.11. Integrator output histograms of the 2nd order CT SD ADC in SIMULINK for 128 OSR.

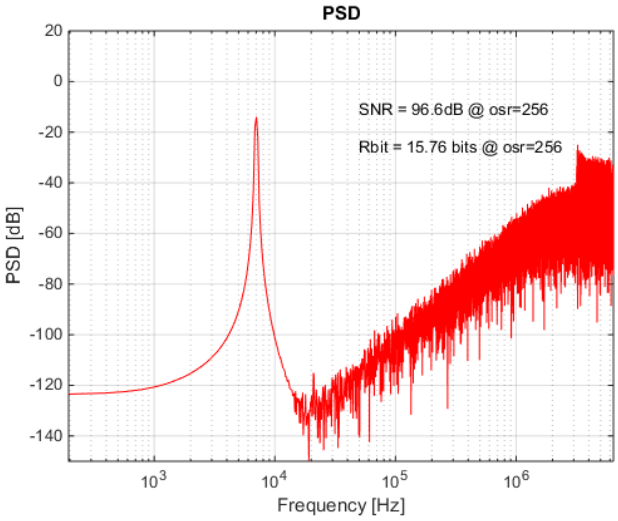

Figure 3.12. FFT of the 2nd order CT SD ADC in SIMULINK for 256 OSR.

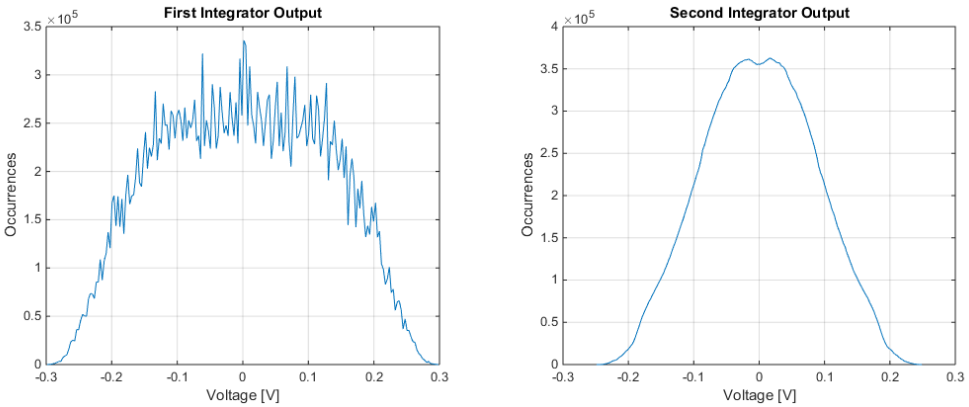

Figure 3.13. Integrator output histograms of the 2nd order CT SD ADC in SIMULINK for 256 OSR.

These CT SD ADCs can be implemented with different types of integrators. The types of integrators are investigated in this section.

3.1. g_m-C Integrators

The low pass filters used as integrators in the CT SD ADC can be implemented with a g_m-C circuit as seen in Figure 3.14. The coefficients of each integrator can be calculated as in (3.4). A transconductance amplifier can be used as the g_m circuit in the integrator. The most crucial part of this transconductance amplifier is to have constant g_m. Thus, a folded cascode opamp with both NMOS and PMOS inputs as in Figure 3.15 is designed and used as a g_m circuit. Even though the folded cascode opamp has both NMOS and PMOS inputs to obtain constant g_m, simulations results showed that very high third harmonics occurred because of the non-linear g_m of the integrators.

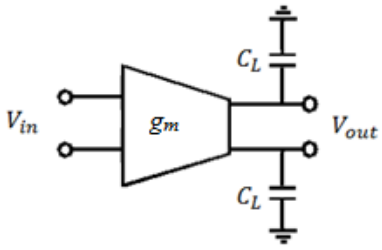

Figure 3.14. A g_m-C integrator.

$$H(s) = \frac{g_m}{sC_L} = k\frac{F_s}{s} \tag{3.4}$$

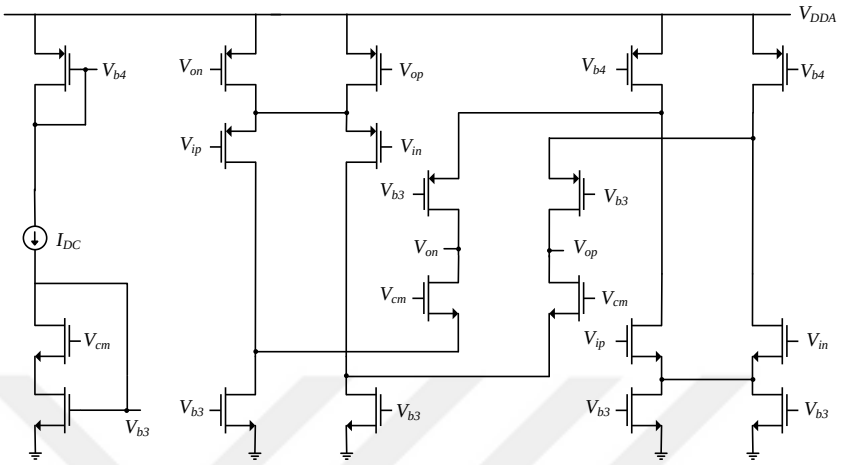

Figure 3.15. Folded cascode opamp with both NMOS and PMOS inputs.

Afterwards, a telescopic cascode opamp with source degeneration is designed as in Figure 3.16. Even though the source degeneration resistances improved the linearity, the gain drops dramatically. Therefore, high noise floor has been observed in Sigma Delta ADC results. Hence, the gain of this telescopic cascode opamp was improved with gain boosting and using a regulated cascode method as in Figure 3.17.

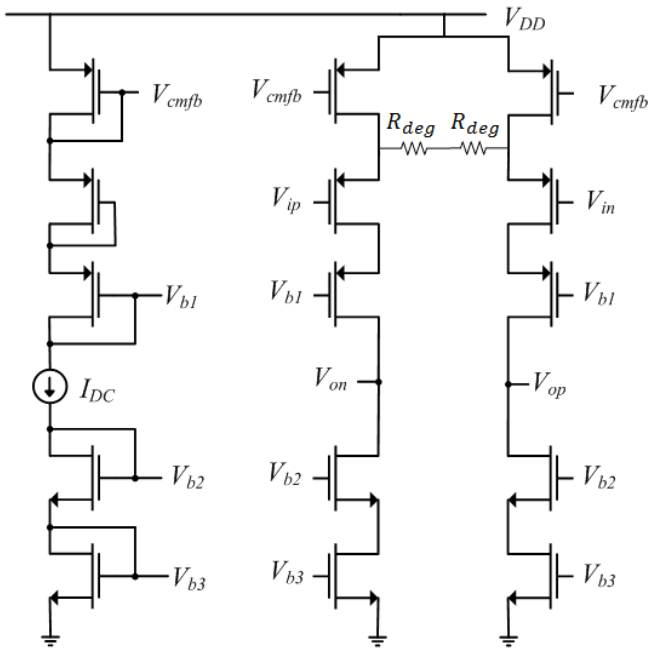

Figure 3.16. Telescopic cascode with source degeneration.

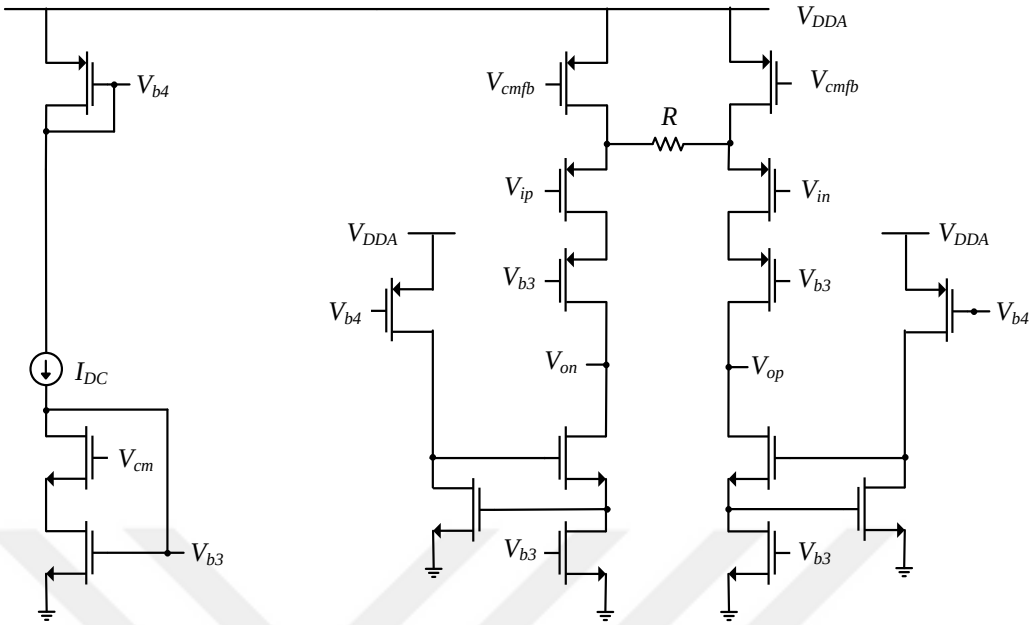

Figure 3.17. Telescopic cascode opamp with source degeneration and gain boosting method.

Source degeneration and regulated cascode improve the performance, but the non-linearity problem persists, which causes third harmonics in the system. The lowest third harmonic achieved was 70 dB lower than the signal with an unacceptably high power consumption value. Furthermore, two g_m circuits are used to add two signals which doubles the power consumption of each integrator. In conclusion, it is not advantageous to use g_m-C integrators. However, [21] has studies for optimization of g_m-C integrators in CT SD ADCs as a future study.

3.2. Active *RC* Integrators

The second type of CT ADCs studied are the CT SD ADCs with active *RC* integrators. The transfer function of the active *RC* integrator with an ideal opamp is given in (3.5). However, the gain of the opamp is limited and the transfer function of the integrator is calculated as in (3.6) which acts as a low pass filter. The opamp also has limited gain-bandwidth product which causes an additional pole in the system. This makes the transfer function very complicated. However, the effect of the finite gain of the opamp is both the same in DT and CT and the DC gain of the opamp has to be more than OSR according to [20]. Likewise, [8] suggests that the DC gain should be more than π times the OSR for

negligible performance degradation in DT SD ADCs. The effect of the gain-bandwidth product is less severe in CT than DT SD ADCs according to [20]. Thus, by choosing the gain-bandwidth product of the opamps two to five times the sampling frequency of the system would be sufficient. However, different phase shifts occur for the signal and the feedback path in the transfer function due to gain error and gain-bandwidth product. This makes the design even more complicated. Such issues have been widely studied in the literature [22].

$$H(s) = \frac{1}{sRC} = k\frac{F_s}{s} \tag{3.5}$$

$$H(s) = \frac{\frac{A(s)}{RC(1+A(s))}}{s + \frac{1}{RC(1+A(s))}}\Bigg|_{A(s)=\frac{A_0 BW}{s+BW}} = \frac{A_0 BW}{1 + sRCBW(A_0+1) + s^2RC} \tag{3.6}$$

Opamp linearity and the output swing margin are very important for active *RC* design too. If the opamp is not linear enough, the gain changes with the output swing, which causes third harmonics in the frequency domain. Therefore, the same telescopic cascode with regulated cascode and source degeneration is used as an opamp in the 2nd order SD ADC with active *RC* integrators is seen in Figure 3.18. Figure 3.19 shows the frequency domain result of the SD ADC. Here, the third harmonic and the high noise floor degrades the performance of the SD ADC. If the opamp is replaced with a regular telescopic cascode opamp, the SNR drops even further due to the high noise floor and the third harmonic.

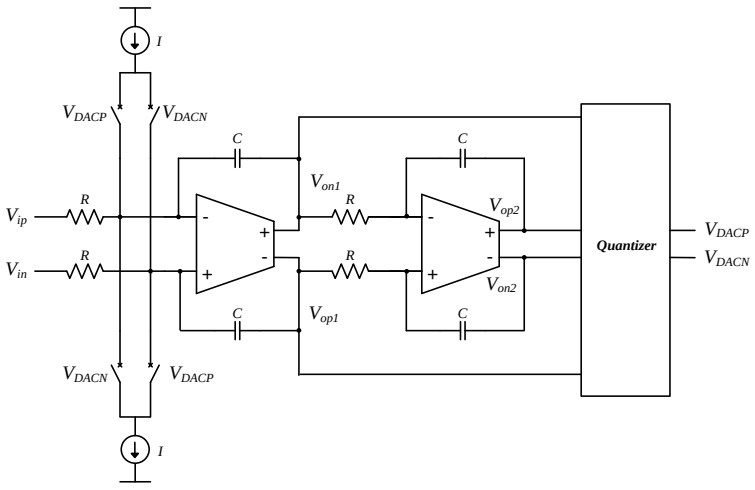

Figure 3.18. A 2nd order SD ADC with active *RC* integrators.

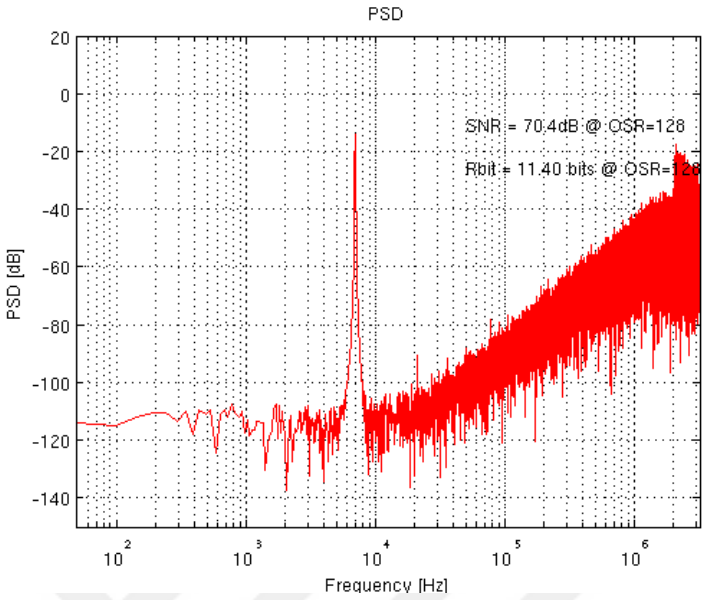

Figure 3.19. FFT of the SD ADC with active *RC* integrators.

Another CT SD ADC with active *RC* integrators can be obtained by using the feed-forward architecture. The proposed 2nd order CT SD ADC in Figure 3.8 is designed with active *RC* integrators and the proposed feed-forward method used in DT SD ADCs. The addition block after the second integrator can be implemented easily with the proposed feed-forward method and the overall circuit becomes as in Figure 3.20. This structure is realised using ideal resistors, capacitors and a comparator, but the designed folded cascode opamps. 84.8 dB SNDR is achieved in this case as seen in Figure 3.21 proving that the proposed feed-forward path method works as a CT feed-forward SD ADC. Likewise, similar results can be achieved by designing a good comparator, a CT common mode feedback circuit and an opamp with large swing margin.

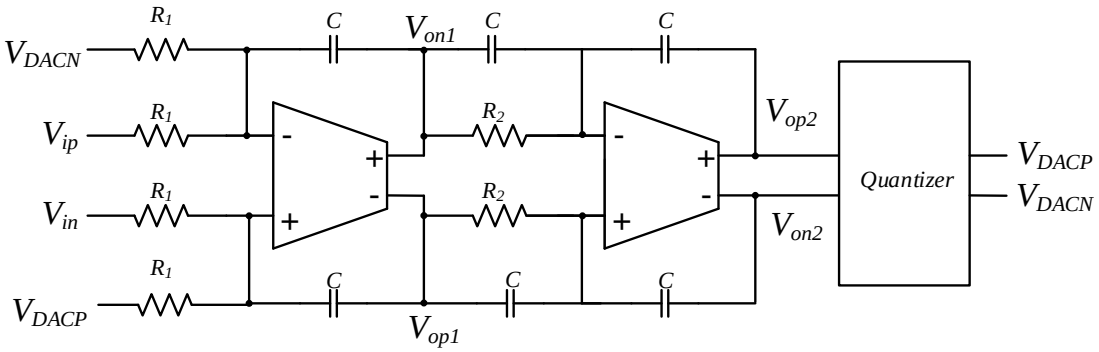

Figure 3.20. Feed-forward CT 2nd order SD ADC with Active *RC* integrators.

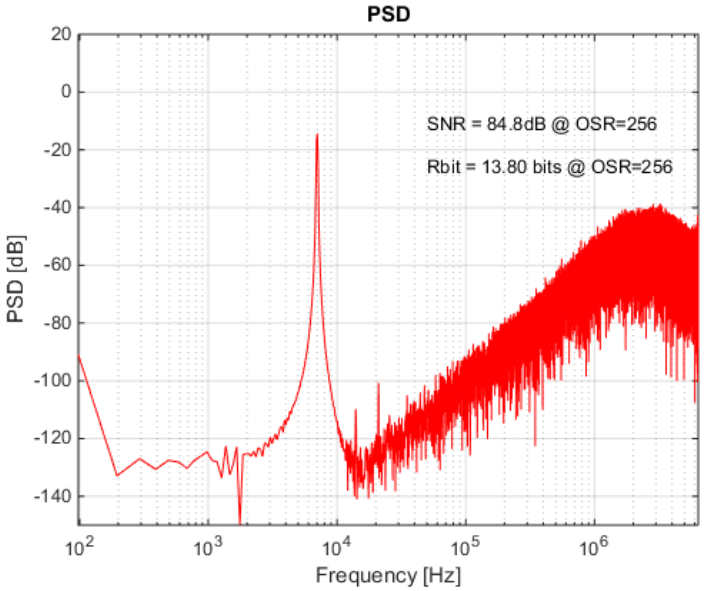

Figure 3.21. FFT of the feed-forward CT 2nd order SD ADC with active *RC* integrators using ideal components and comparator and the designed folded cascode opamps.

Furthermore, it can be seen that the transfer function of the feed-forward architecture can be implemented with only one opamp with the help of inductors as in (3.7) and Figure 3.22. However, the value of the inductance becomes very high for the desired transfer function and it is only possible to implement the SD ADC if the inductors are used as discrete elements outside the IC. Nevertheless, the design contains only one opamp and has very low power consumption. Simulation results are shown in Figure 3.23 when the CT SD ADC is designed with an ideal active *RLC* integrator and ideal comparator.

$$TF = k_1 \frac{F_s}{s}\left(1 + k_2 \frac{F_s}{s}\right) = \frac{R + \frac{1}{sC}}{sL} \tag{3.7}$$

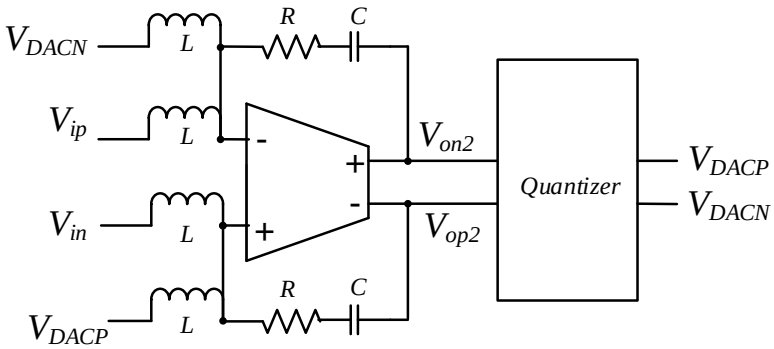

Figure 3.22. CT 2nd order SD ADC with a single active *RLC* integrator.

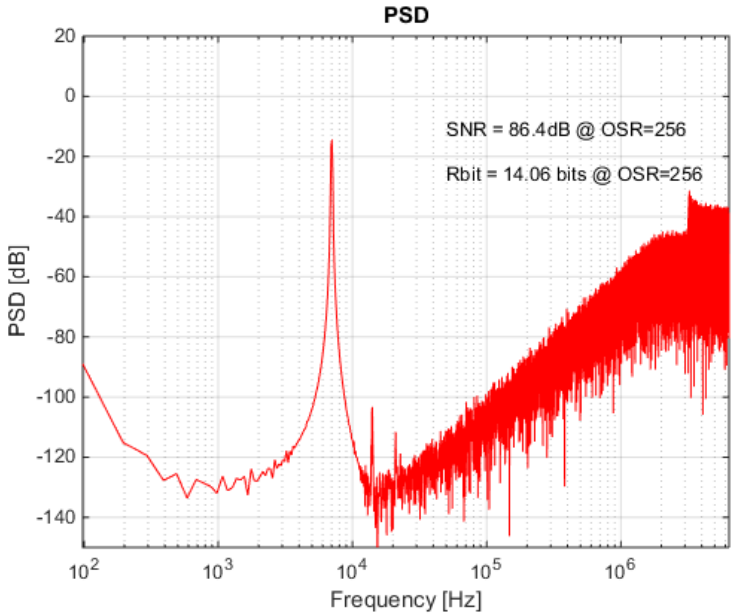

Figure 3.23. FFT of the CT SD ADC with ideal active *RLC* integrators.

3.3. Current Mode Integrators

In current mode design, integrators operate in current mode, meaning that the current input is integrated and transferred to the output. [23] claims that the integration could be done more efficiently in current mode. Hence, the circuit in Figure 3.24 is designed as a current mode integrator inspired by the cascaded version of the current mode integrator in [23].

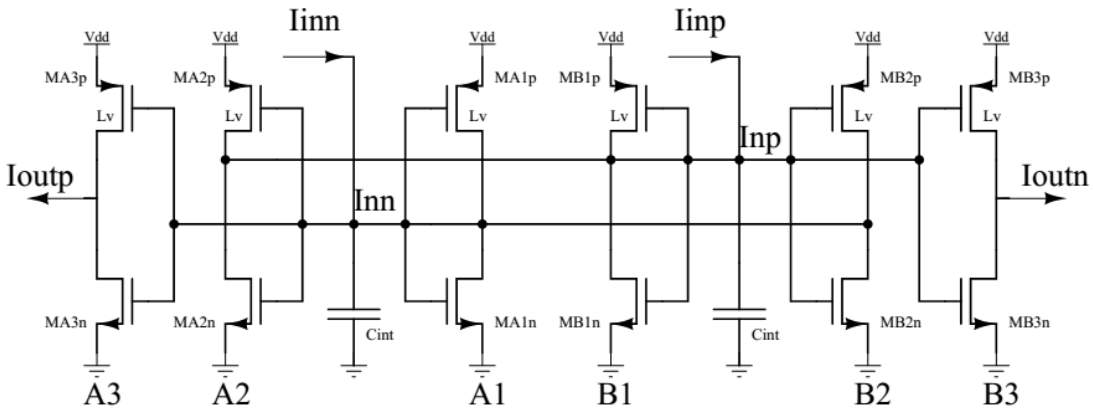

Figure 3.24. Current mode integrator.

The CT 2nd order SD ADC in Figure 3.8 is well suited for current mode operation. Hence, it can be implemented as the circuit in Figure 3.25 in current mode with the current mode integrator [24]. Since the signals are current, addition operation is easier. However, the best comparison is made in voltage mode. Thus, a current to voltage converter as in Figure 3.26 is used to convert the current signal into a voltage signal before comparison. According to the comparator output, a current steering DAC provides current feedback as in Figure 3.27. Thus, the overall ADC layout becomes as depicted in Figure 3.28 in UMC 180 nm technology. Simulation results without the noise of the active devices show that the ADC has a very high performance according to Figure 3.29. Furthermore, it doesn't have large third harmonics or high noise floor because the voltage change at the output is very low.

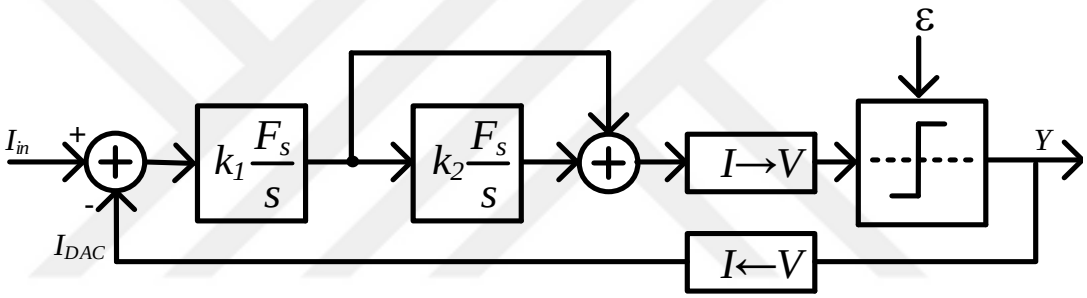

Figure 3.25. Current mode 2nd order SD ADC.

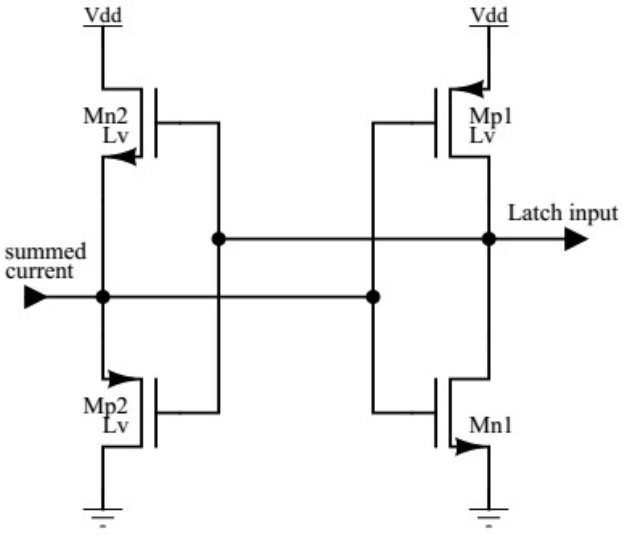

Figure 3.26. The pre-amplifying circuit which is also used for current mode addition and current to voltage conversion.

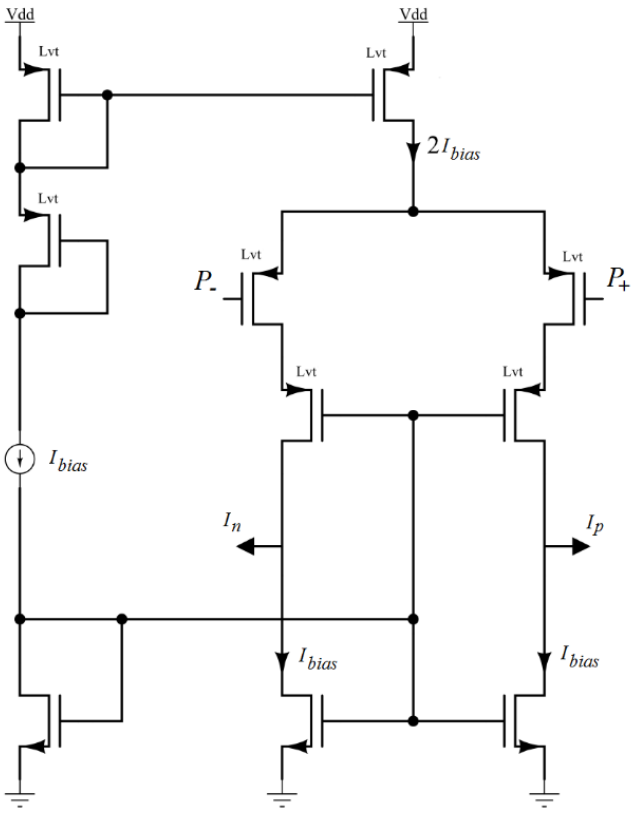

Figure 3.27. Current steering DAC.

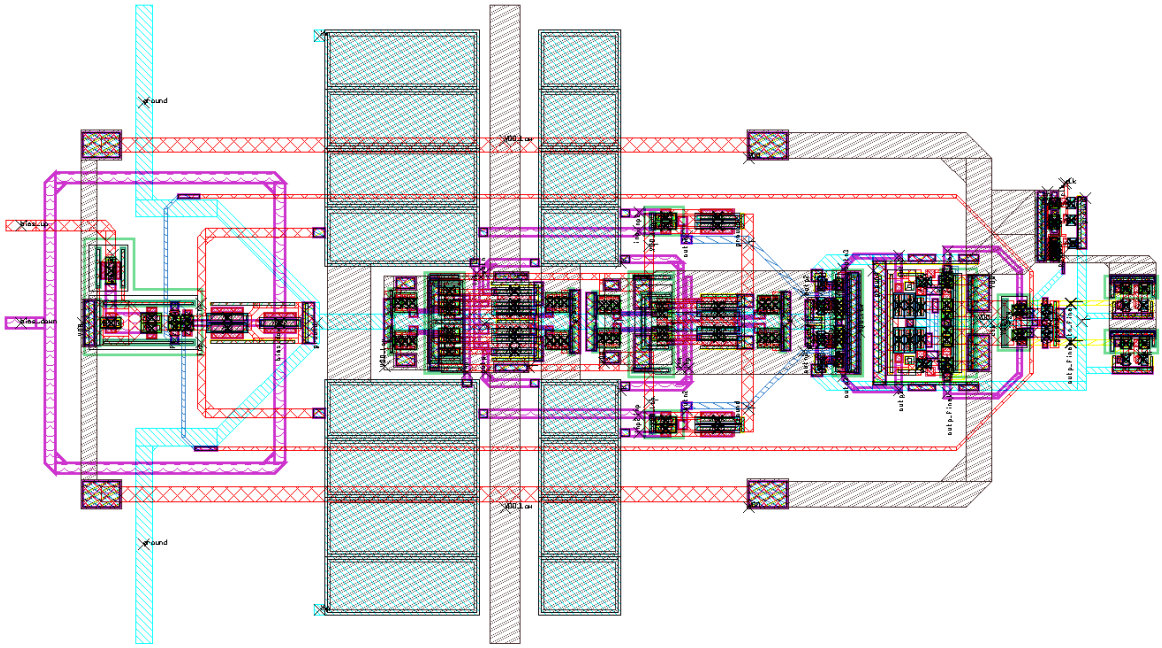

Figure 3.28. Layout of the CT 2nd order SD ADC in UMC 180 nm technology.

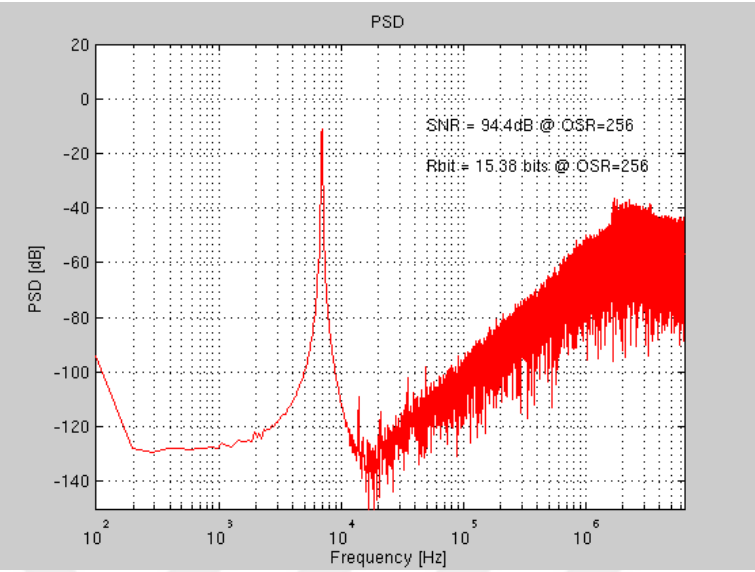

Figure 3.29. FFT of the current mode 2nd order SD ADC.

The results in Figure 3.29 are those of a CT SD ADC with the current inputs. However, it is very complicated to use two differential direct current sources as inputs for the circuit in real implementation. Since this is a *C*-g_m circuit, the input is directly connected to the capacitance and the value of this capacitance increases with wires, pads, PCB and the probes. Therefore, it is not likely to achieve this performance in reality. Hence, a voltage to current converter as in Figure 3.30 is used to convert two differential voltage inputs to current inputs. It is very difficult to obtain constant transconductance and the performance of the ADC weakens. So, the new SNDR becomes 87.2 dB as in Figure 3.31.

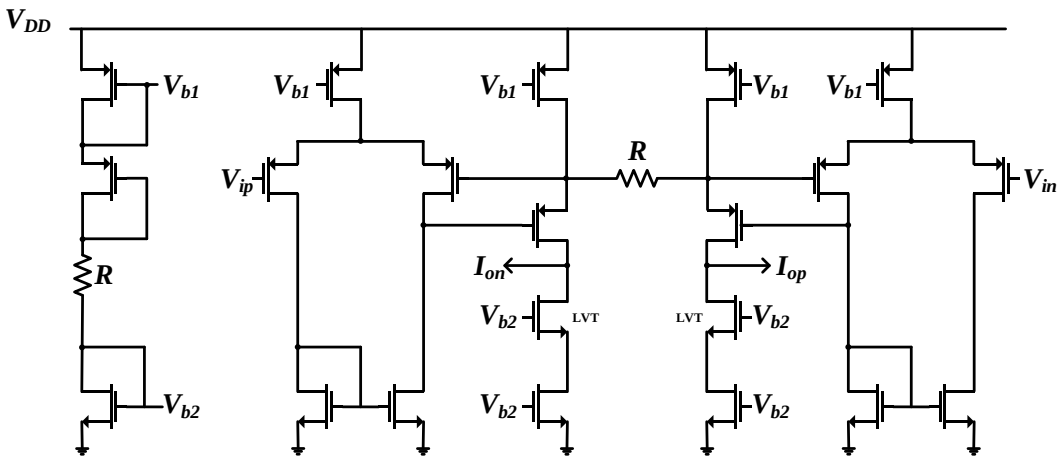

Figure 3.30. Voltage to current to converter.

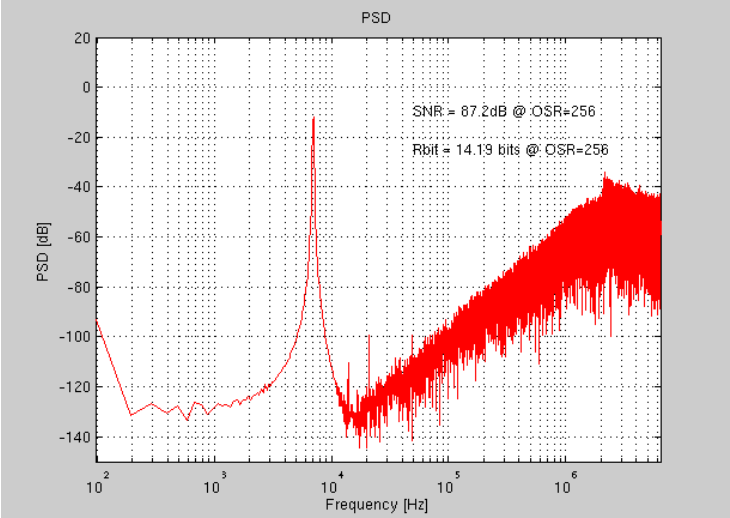

Figure 3.31. FFT result of the current mode 2nd order SD ADC with voltage to current converters.

It can also be seen that the performance degrades dramatically when the noise of active devices is included in the transient simulation. The SNDR drops to 60.8 dB with the noise of the active devices as in Figure 3.32. The reason for high noise floor is still under investigation.

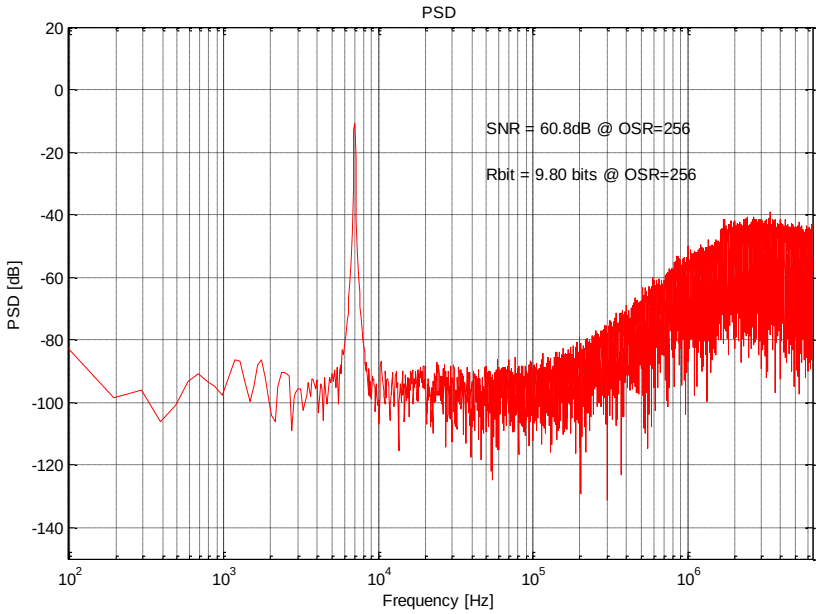

Figure 3.32. Post-layout FFT of the current mode 2nd order SD ADC with the noise of the active devices included.

Table 3.1. Specifications of the 2nd order CT SD ADC.

Specifications	**Value**
Integrators	2.15 µW
Comparator	0.95 µW
DAC	0.65 µW
Preamplifier	0.65 µW
Total power consumption	4.45 µW
Voltage to current converter	2.5 µW
Total power consumption with voltage to current converter	6.95 µW
OSR	256
Signal Bandwidth	25 kHz
SNDR ideal	94.4 dB
ENOB ideal	15.38 bit
FoM ideal	2.1 fJ/conv
SNDR with voltage to current converter	87.2 dB
ENOB with voltage to current converter	14.19 bit
FoM with voltage to current converter	7.4 fJ/conv
SNDR with the noise of the active devices	60.8 dB
ENOB with the noise of the active devices	9.8 bit
FoM with the noise of the active devices	100 fJ/conv

The current mode CT 2nd order SD ADC is designed with the same topology in UMC 130 nm technology as well. However, OSR is reduced to 128 and the integrators are relaxed by increasing their power consumption for the new design. It is also expected that the noise of the integrators would reduce with the DC current passing through each transistor. The layout which is prepared as symmetrical as possible is depicted in Figure 3.33. Furthermore, the post-layout simulation results including and excluding the noise of active elements is seen in Figure 3.34. There is still a high noise floor in the design when the noise of the active elements are included. Even without the noise, there is a third harmonic most probably caused by the addition and preamplifier circuits. Furthermore, the current inputs are still a problem and there was not enough time for the voltage to current converter design. Nevertheless, the layout is sent for production with the other SD ADCs designed in UMC 130 nm technology.

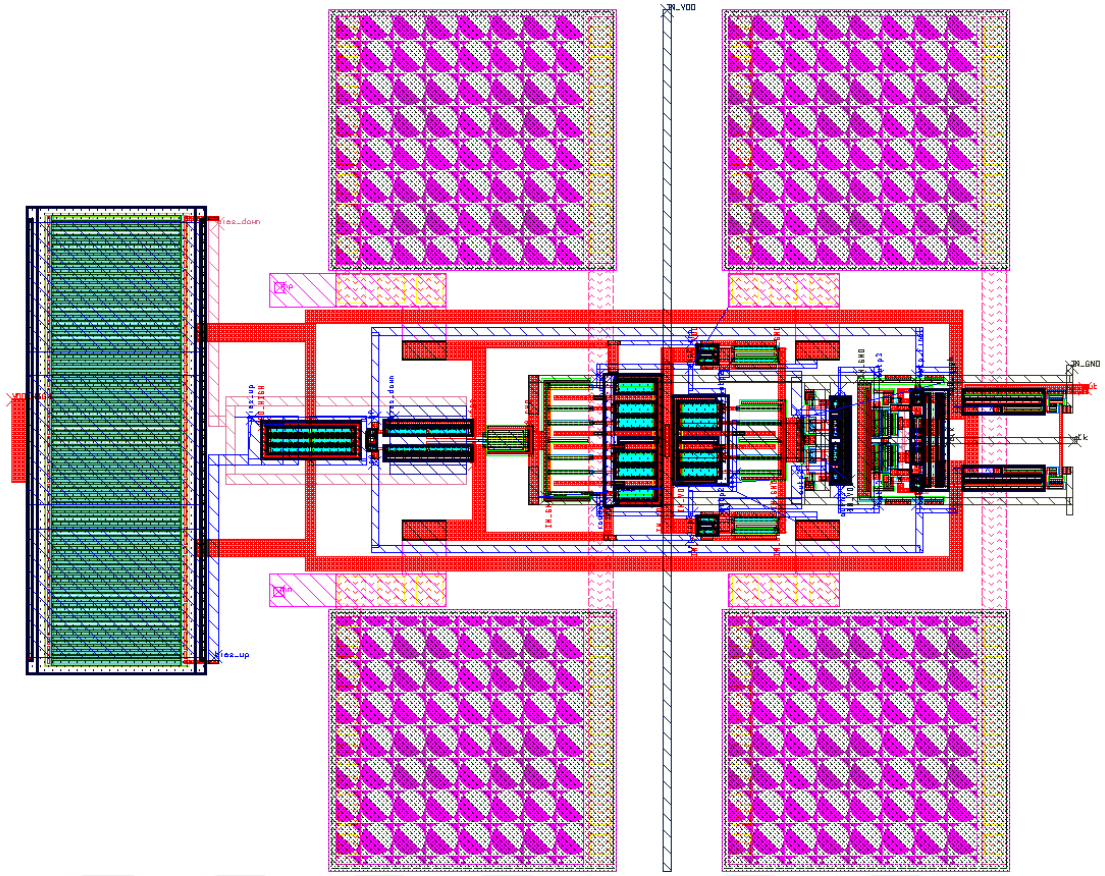

Figure 3.33. The layout of the CT current mode SD ADC redesigned in UMC 130 nm technology.

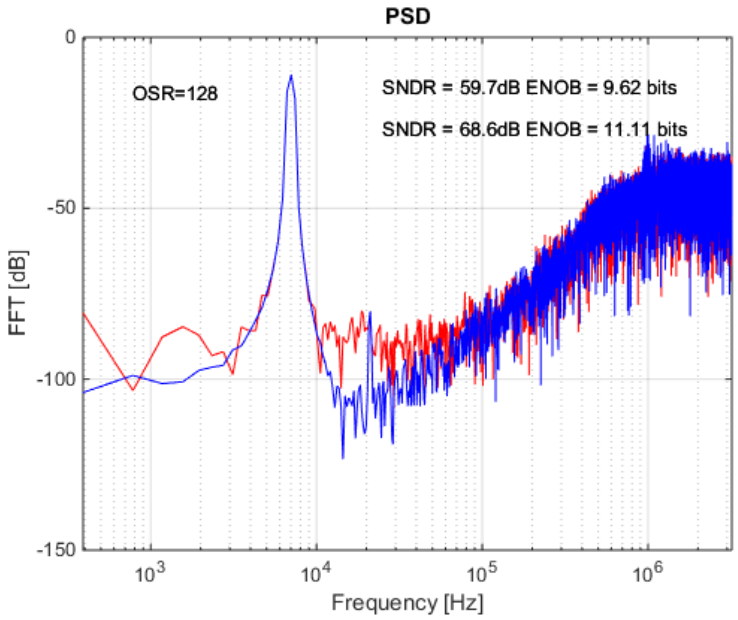

Figure 3.34. FFT results of the CT current mode SD ADC redesigned in UMC 130 nm technology.

3.4. CT SD ADC Summary

In this chapter, 2nd order CT SD ADCs with different architectures are studied. In some of the designs, feed-forward method is applied. Different opamps are used in the integrators for the desired performance. Different type of DACs are used in each design according to the structure of the ADC. The layouts of the CT ADCs are prepared and post-layout simulations again show that the CT ADCs have very high performance for their power consumption compared to the ADCs in the literature.

4. HYBRID TIME SIGMA DELTA ANALOG DIGITAL CONVERSION

The SD ADCs are generally designed in DT or CT as examined previously. However, the literature contains a few designs that includes both DT and CT structures [25]. The quantization part in CT designs are actually in DT while the integrators operate in CT. So, if some of the CT integrators are replaced with DT integrators, a hybrid SD ADC is achieved. Since the load of the first integrator is critical in DT ADCs, a typical method to obtain a hybrid ADC is to replace the first integrator with a CT integrator. So, the feed-forward path of the input *X* in Figure 2.49 is removed from the circuit and the ADC in Figure 4.1 to convert a DT SD ADC into a hybrid SD ADC. In this case, the transfer function of the circuit turns into (3.7). $X(1\text{-}z^{-1})$ has a minor effect on the output and it is negligible when OSR is high.

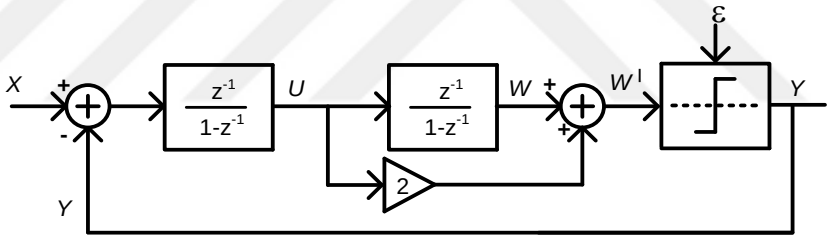

Figure 4.1. Updated DT 2nd order SD ADC.

$$Y = Xz^{-1} + Xz^{-1}(1 - z^{-1}) + \varepsilon(1 - z^{-1})^2 \tag{4.1}$$

The transfer function of a delayed DT integrator in *z*-domain is the same as that of a CT integrator in the *s*-domain [20]. As a result, the first integrator is replaced with a CT integrator and a hybrid SD ADC is achieved as seen in Figure 4.2. Thus, the opamp slew rate specifications are relaxed because a CT integrator is used as the first integrator. Also, a small coefficient is chosen for the CT integrator, so that the output swings are reduced. Despite this, it is not easy to determine exactly the coefficient in a CT integrator due to process variations. Hence, a 1-bit quantizer is used to make the circuit less sensitive to these variations. Instead of aiming for a high SNR and having a large OSR value, the proposed hybrid design is more suitable for use in low power applications in which such a high SNR

is not required. The new hybrid ADC architecture is also suitable for the proposed feed-forward method. The CT integrator is obtained with an active RC circuit. Also, double sampling method is used to relax the second opamp specifications. Figure 4.3 shows the schematic of the hybrid design, which is focused on very low power applications. The low power consuming folded cascode opamps with AC analysis results in Figure 2.42 are used here. Following this, the layout of the hybrid ADC is prepared as in Figure 4.4. The opamps are replaced with medium power consuming versions for higher performance and the design is updated for comparison.

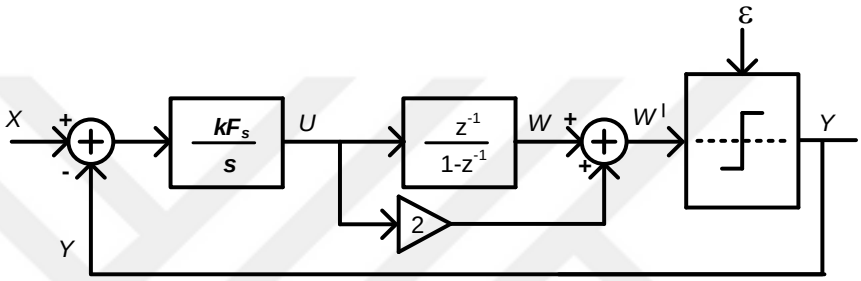

Figure 4.2. 2nd order hybrid SD ADC.

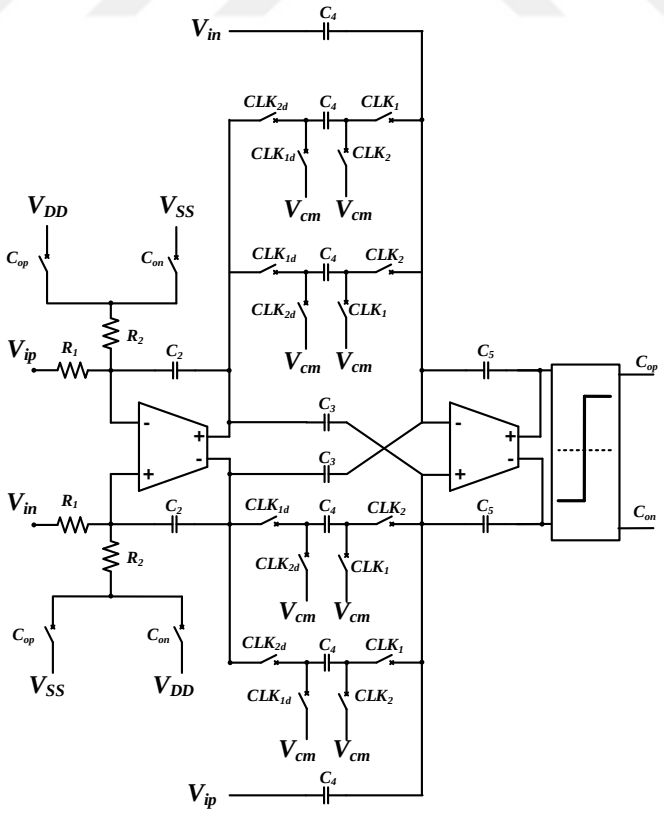

Figure 4.3. Schematic of the 2nd order hybrid SD ADC.

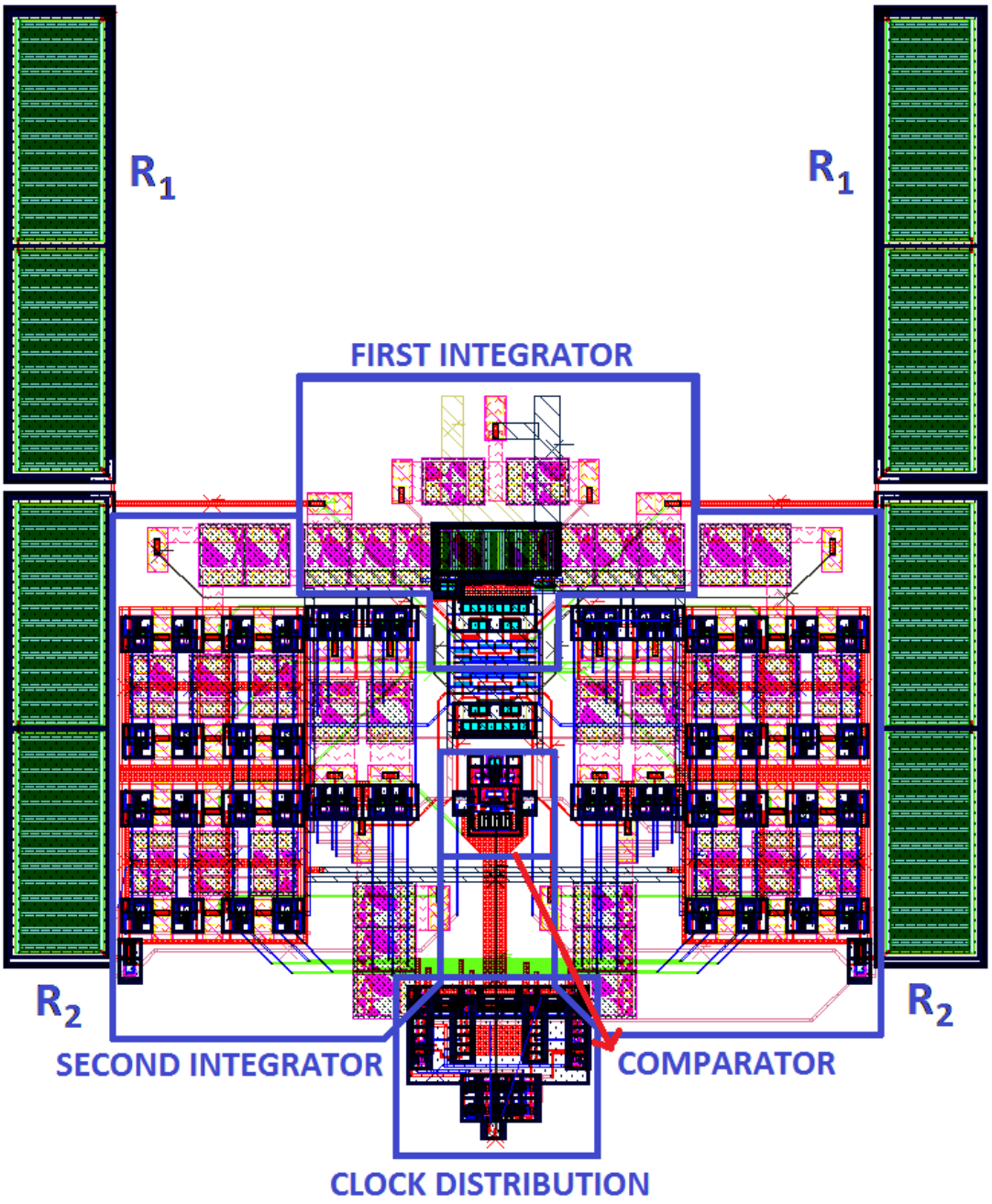

Figure 4.4. Layout of the 2nd order hybrid SD ADC.

The sampling frequency for the hybrid SD ADC is selected as 1.6 MHz but the value of the OSR is still 64 for the 2nd order hybrid ADC, due to double sampling. Figure 4.5 is the FFT result derived from the post-layout transient analysis of the hybrid SD ADC.

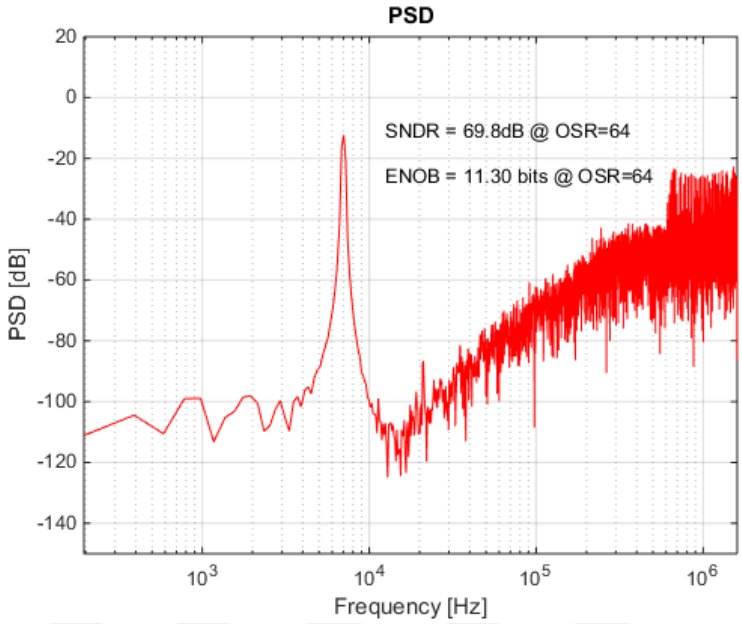

Figure 4.5. FFT result of the 2nd order hybrid SD ADC.

In this chapter, a 2nd hybrid SD ADC is studied. The feed-forward path is applied to lower the integrator swings. Folded cascode opamps are used in the integrators to optimize the power consumption for the desired performance. Double sampling method is used to relax the specifications of the opamps. A resistive DAC is used in the design which is very suitable for the CT part of the circuit. The layout of the hybrid SD ADC is prepared and post-layout simulations show that the hybrid SD ADC has high performance for the power consumption compared to the ADCs in the literature.

5. IC TEST RESULTS

The SD ADC designs are sent to production so that experimental tests can be done. During the Ph.D., three integrated circuits are sent to production and they are introduced chronologically.

5.1. IC 2011

The first IC sent to production with the layout in Figure 5.1 contained four 3rd order SD ADCs with different feedback resistances as introduced in Section 2.2.2. Firstly, a PCB is prepared to test the four 3rd order SD ADCs. Figure 5.2 shows the PCB layout while Figure 5.3 and Figure 5.4 are the produced versions.

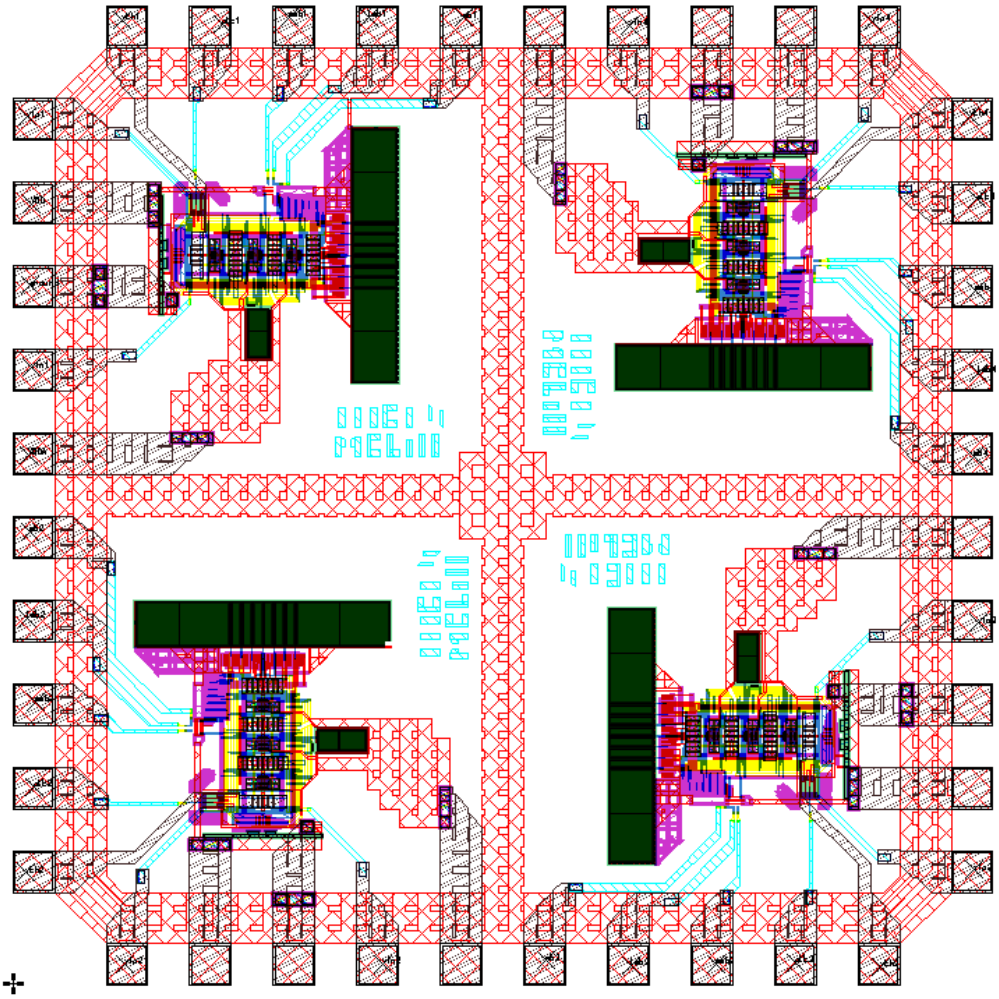

Figure 5.1. Layout of four 3rd order SD ADCs with different DAC resistance values.

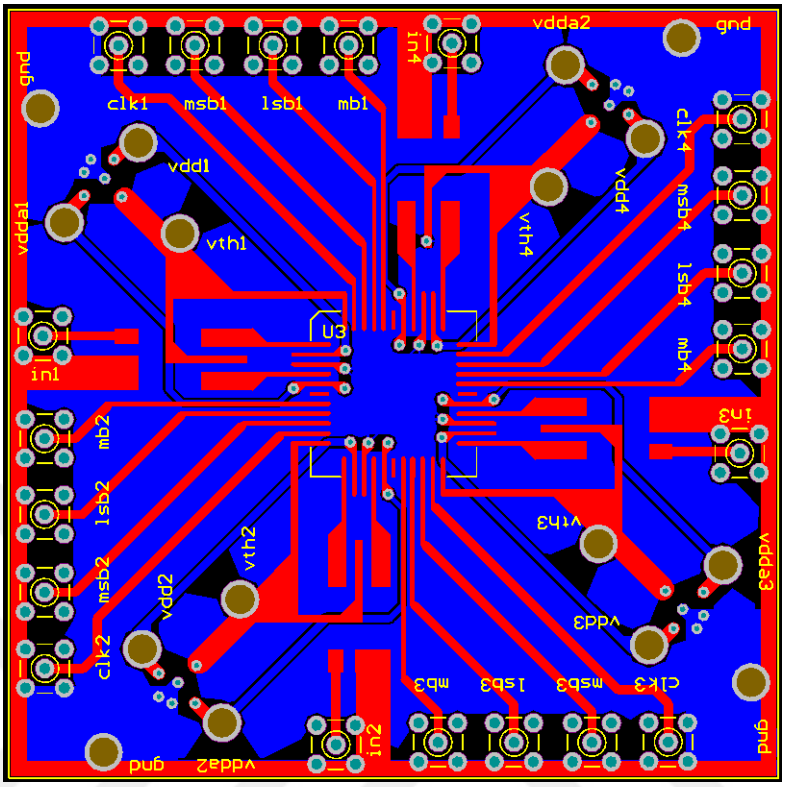

Figure 5.2. Prepared test PCB for the 3rd order SD ADC.

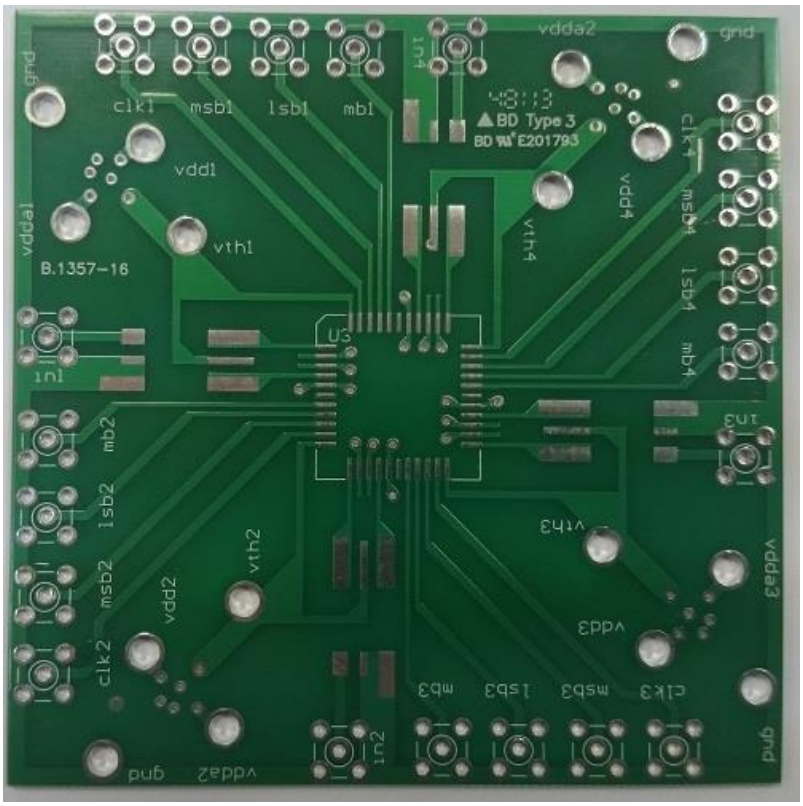

Figure 5.3. Produced test PCB for the 3rd order SD ADC.

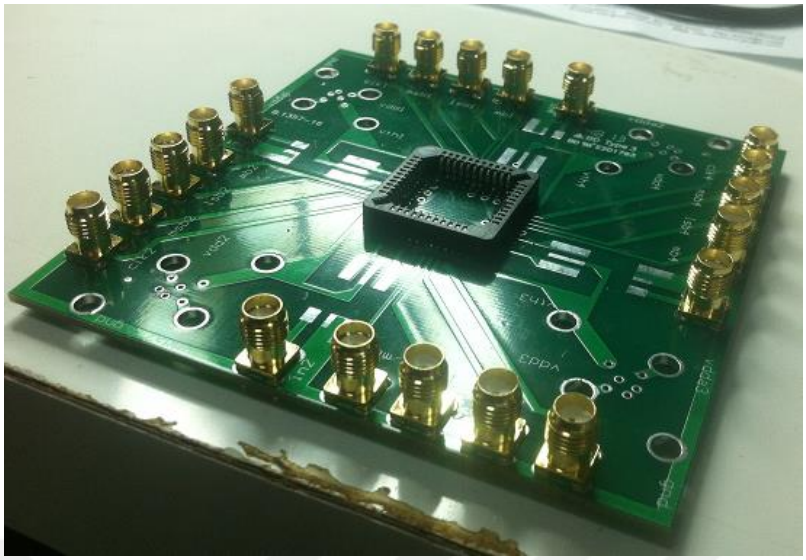

Figure 5.4. Test PCB with some components for the 3rd order SD ADC.

In the tests, an analog single ended input is converted into two differential signals via a transformer. Clock signal is obtained by a digital oscillator and the digital outputs are transferred to an oscilloscope as in Figure 5.5. The oscilloscope saves 10 million data with 2.5 giga samples per second. On the other hand, the oscillator saves data every 400 ns with a total of 4 ms. The output frequency of the ADC is 1.6 MHz due to double sampling. Therefore, the data will be accurate as digital signals if every 1612.5th data is collected as a logic signal. In total, 6400 3-bit samples are collected. Then, consecutive 4096 of these 3-bit samples are gathered and transformed in to analog signals ideally in MATLAB according their logic levels.

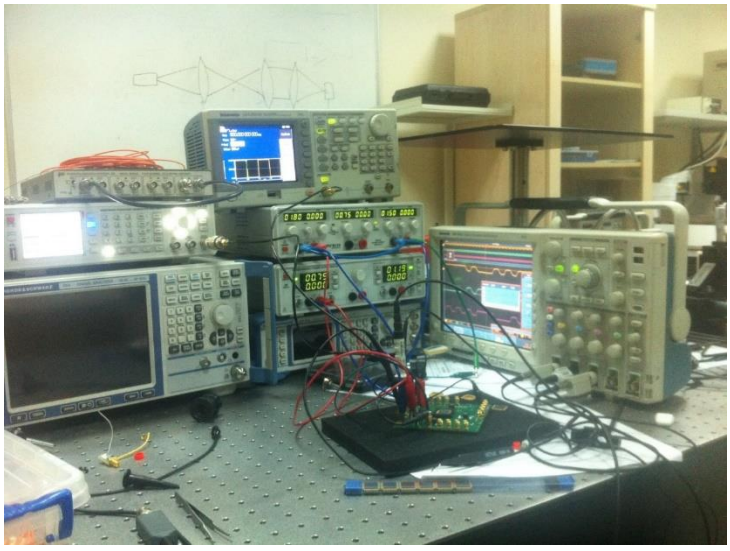

Figure 5.5. Test of the 3rd order SD ADC.

Some of the data collected from a few of the ICs contains only high logic outputs meaning that there is a stuck at 1 error in some of the ICs. However, the other ICs contain both high and low logic outputs as observed in the oscilloscope as in Figure 5.6. The samples are collected as described before and transferred to MATLAB as in Figure 5.7. The 3-bit output becomes as Figure 5.8 after an ideal digital analog conversion in MATLAB. Then, FFT result in Figure 5.9 is achieved from the MATLAB results. There is a very high noise floor in the FFT result which lowers SNDR to 21.2 dB. It is thought that this could be caused by the transformer. Therefore, a sine wave is used as an input while the other input is virtual ground of the circuit. The results didn't change and unexpected low performance continues.

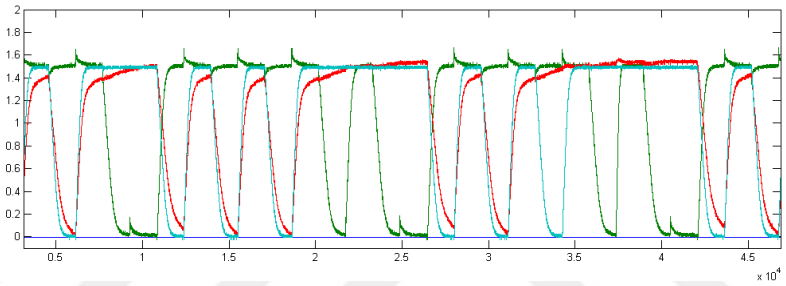

Figure 5.6. The outputs of the 3rd order SD ADC observed in the oscilloscope.

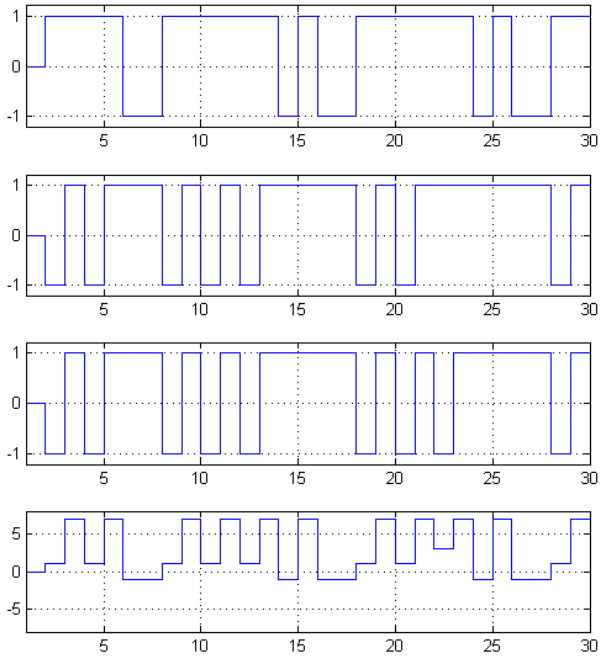

Figure 5.7. The outputs of the 3rd order SD ADC transferred to MATLAB.

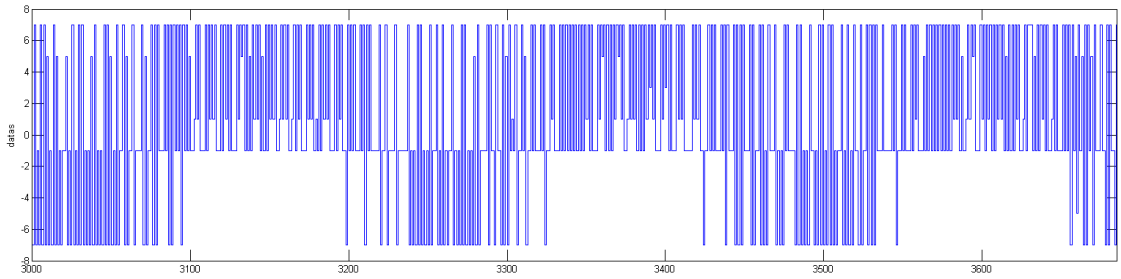

Figure 5.8. The output of the 3rd order SD ADC in MATLAB.

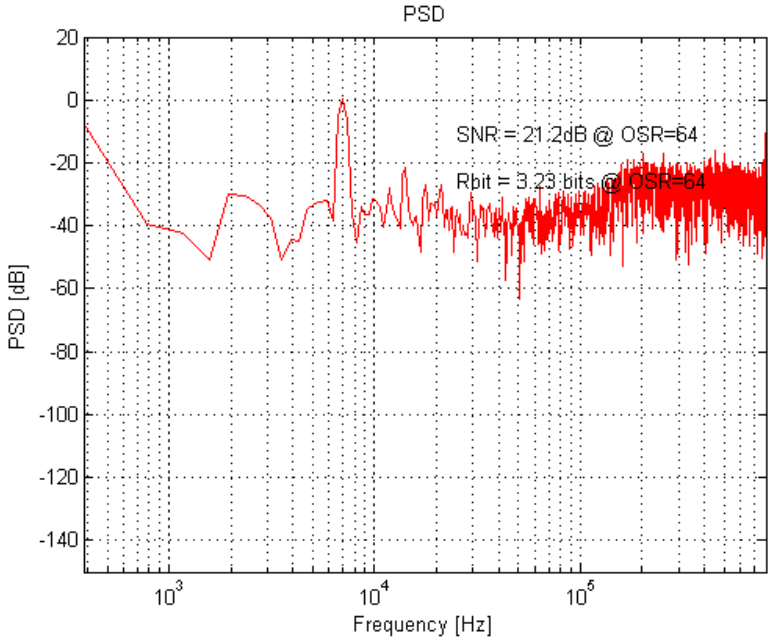

Figure 5.9. FFT results of the test ICs.

Moreover, it is thought that data obtaining had flows. As a next step, virtual ground signal is used as inputs. The outputs observed in the oscilloscope as in Figure 5.10 are transferred to MATLAB as in Figure 5.11. The new 3-bit output becomes as Figure 5.12 after an ideal digital analog conversion in MATLAB. Then, FFT result in Figure 5.13 is achieved from the MATLAB results. The expected results for zero input are having usually ±1 values and rarely ±3 values. According to these results, the ADC is unstable and the output is oscillating although there are no inputs in the ADC. The oscillation is most probably the reason of high noise floor in FFT results. Moreover, there is an offset problem because the average of the output is not 0 or even close to 0.

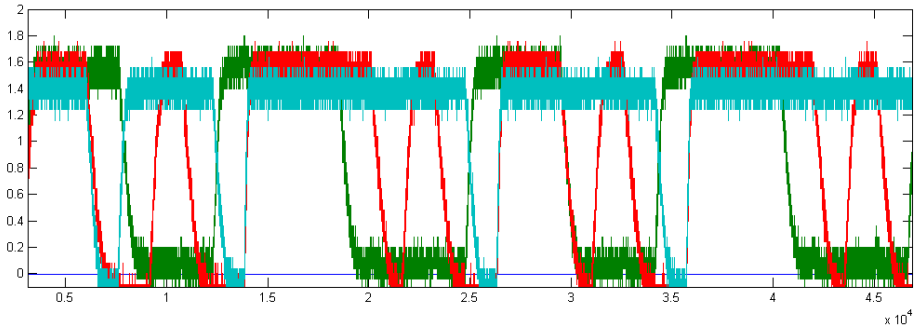

Figure 5.10. The outputs observed in the oscilloscope when the inputs are virtual ground.

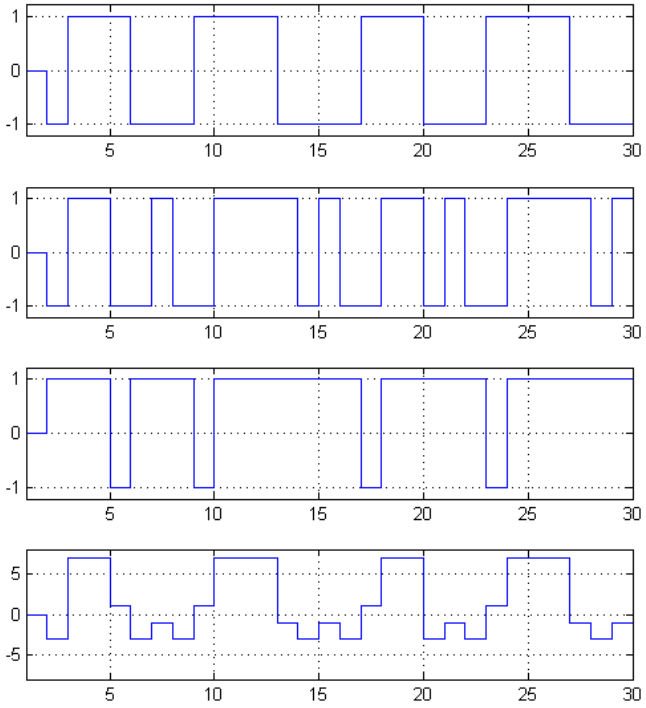

Figure 5.11. The outputs transferred to MATLAB.

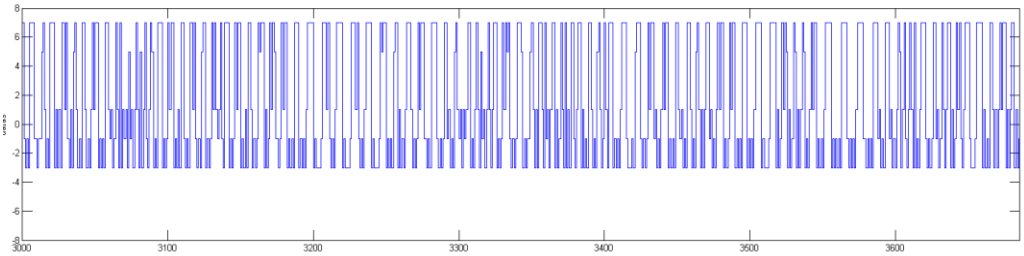

Figure 5.12. The output of the 3rd order SD ADC in MATLAB when the inputs are virtual ground.

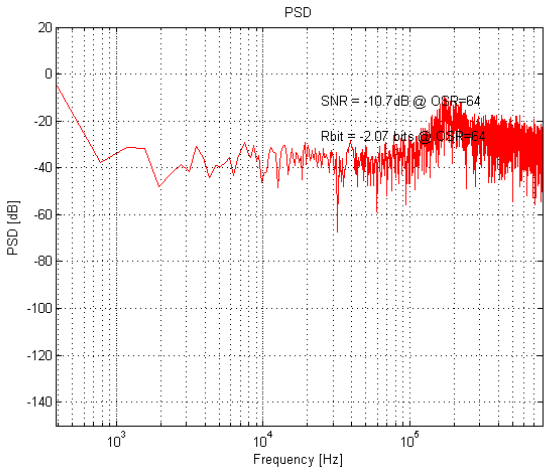

Figure 5.13. FFT results of the test IC with no inputs.

First of all, the clock frequency is reduced to 500 kHz instead of 800 kHz but the outputs are still similar to 800 kHz results. Therefore, the noise is not related with the opamp bandwidths. Afterwards, the current drawn from the voltage source is measured and compared with the calculated results. When there is no clock, there will be no switching. Thus, the total current passing through the integrators and the bias circuit should be 3.5 µA. However, it is measured as 5 µA. Since the switched capacitor CMFB circuit is not working in the meantime, it is possible to see different values here than expected because the operation region of the transistors could change. This also can be because of the resistor used in the bias circuit. If the resistor value changes, the current passing though the branches might change and this will change the overall current drawn from the voltage source. Some feedback gathered from the experienced designers says that low voltage transistors have high process variation in their threshold voltage value. This also might change the current drawn from the voltage source. Afterwards, clock is turned on and the current is measured again as 7.5 µA. The increase at the current drawn from the voltage source was expected as 0.4 µA. Nevertheless, the increase is 2.5 µA. This can happen because the CMFB circuit changes the operation region of the transistors in the opamp as well as the power spent in the clock distribution circuit would be higher than expected due to the wiring capacitances. However, it is still too high than expected. The next step is to do the post-layout simulations. Due to the timeline, only simulations with the sub-circuit parasitic resistances and capacitances added are done instead of the post-layout simulations. After 10 days of post-layout transient simulation, the output of the ADC is observed as Figure 5.14 while the FFT result is depicted

in Figure 5.15. The ADC became unstable after the layout is prepared. The instability still continues after post-layout simulations with zero inputs are done. The integrator outputs achieved from the post-layout simulations are changing more than expected as seen in Figure 5.16 which leads to instability in the ADC.

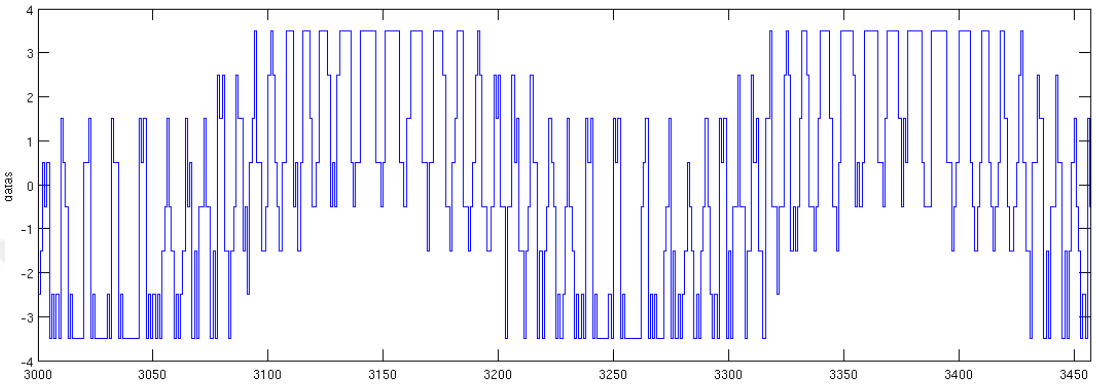

Figure 5.14. Post-layout simulations of the 3rd order SD ADC.

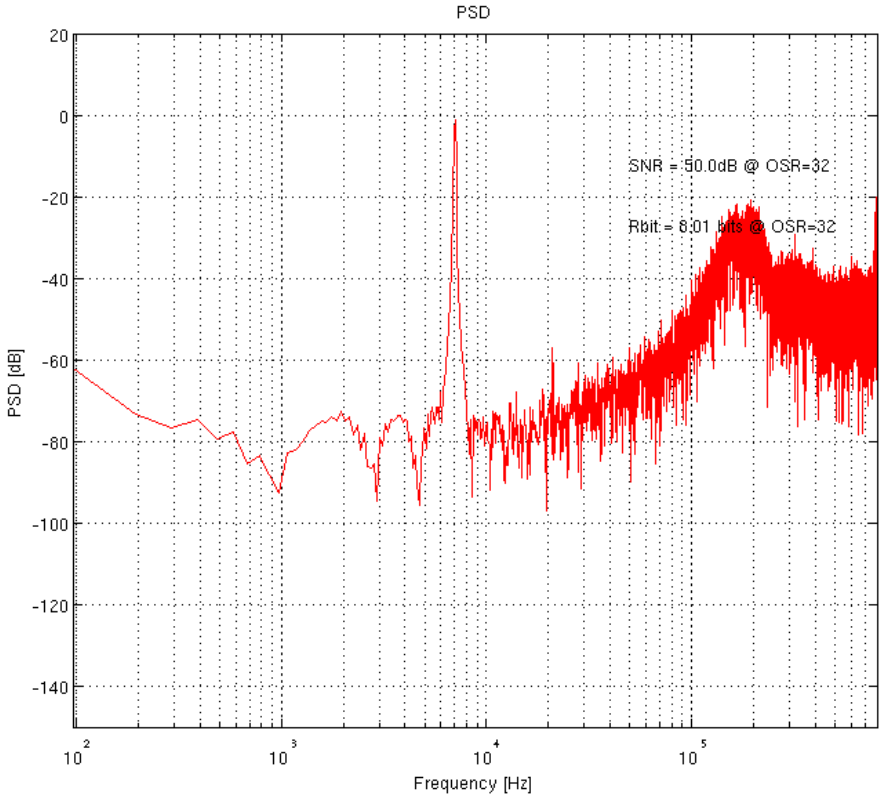

Figure 5.15. FFT of the post-layout simulations of the SD ADC.

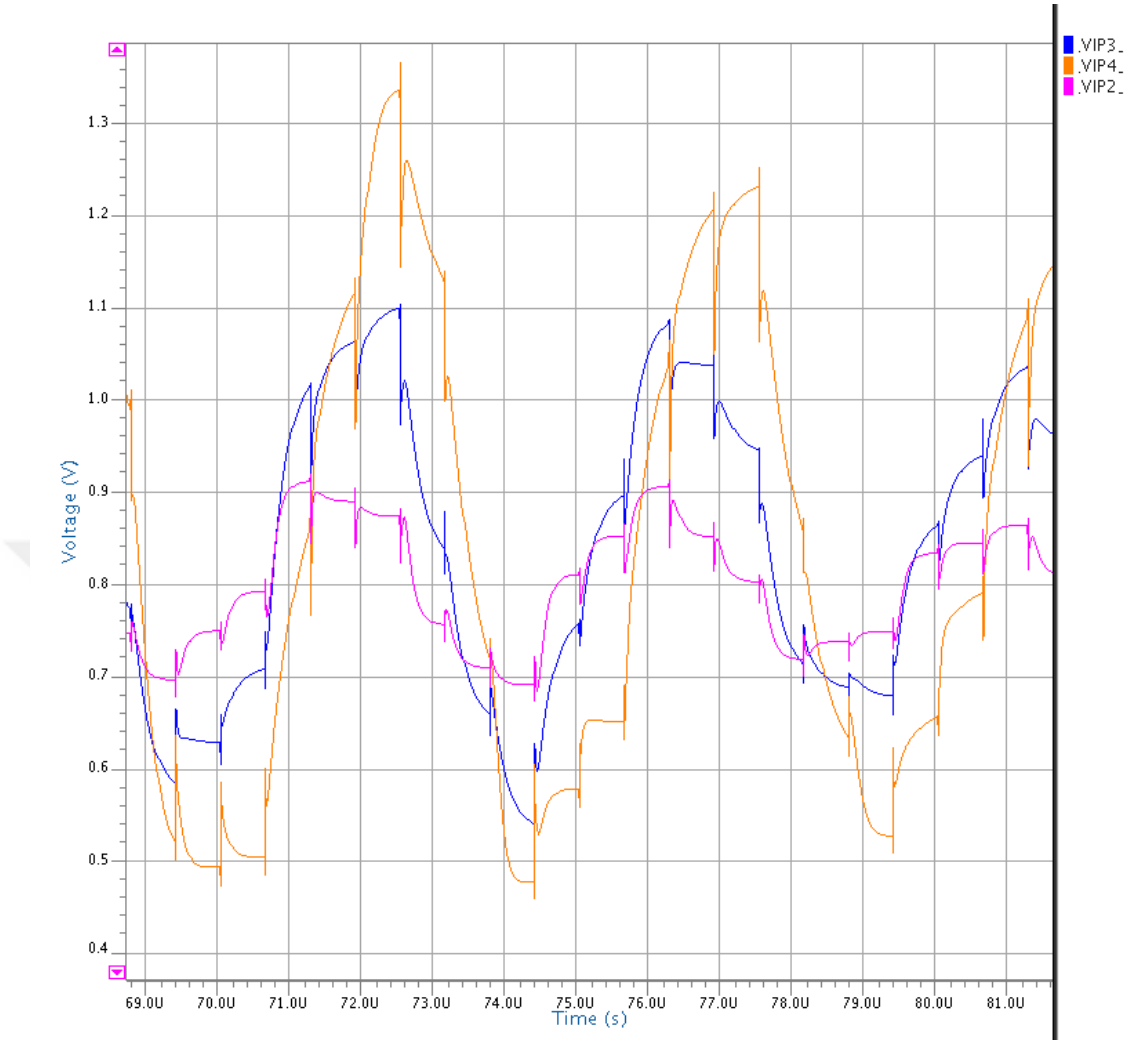

Figure 5.16. Post-layout simulations showing integrator outputs when the zero inputs are applied.

Moreover, the coefficients of the paths in the ADC are randomly changed between -2.5% and 2.5% in SIMULINK to observe the effect of the mismatching of capacitors. Even though the variety is large, SNR is always calculated between 88 dB to 92 dB in 100 simulations for input amplitude and reference ratio of ½. However, 5 out of 100 simulations had instability when the input amplitude and reference ratio is increased to ½. Even though there is no variation, SNR significantly drops when the input amplitude and reference ratio is more than ½. The input amplitude and reference ratio is affected by the variety of the coefficients and SNR significantly drops in the unstable occurrences. Furthermore, 7 out of 100 simulations have instability when the variety is between -5% and 5% for input amplitude and reference ratio of ¼.

5.2. IC 2013

The second IC sent to production contained an updated version of the 3rd order SD ADC, and 3 CT current mode SD ADCs. The first layout of the CT SD ADC is the SD ADC in Figure 3.28. The second CT SD ADC is the same ADC with less input capacitance so that the circuit might still work if there is high capacitance caused by the wiring. The third CT SD ADC is also the same ADC with a differential voltage to current converter for the inputs. However, the resistance is connected to wrong nodes in the layout of this voltage to current converter and it doesn't work properly. The overall IC is in Figure 5.17.

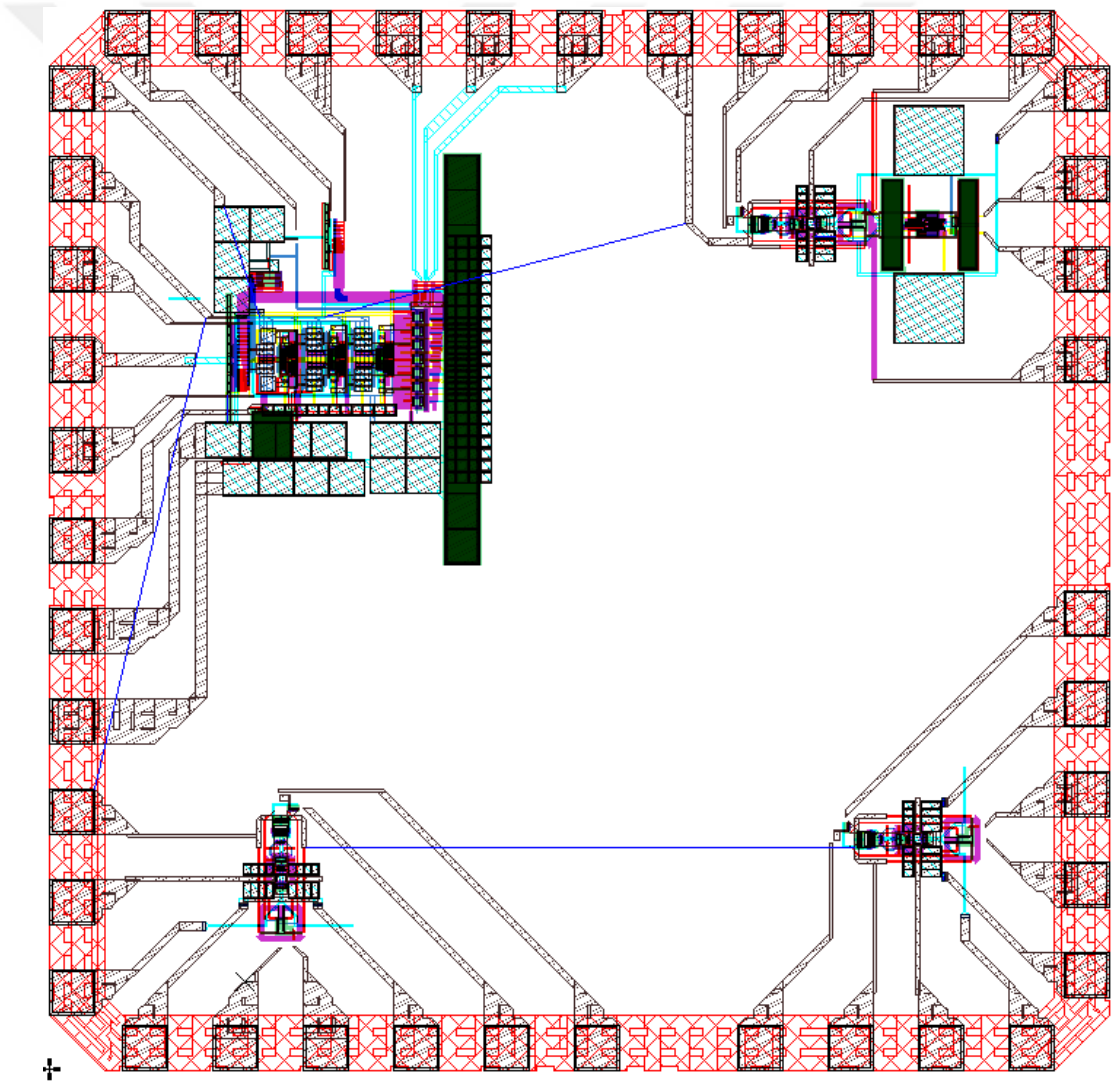

Figure 5.17. The layout of the second IC sent to production.

5.2.1. Experiments with the Updated 3nd Order SD ADC

The test PCB of the updated 3rd order SD ADC is prepared as in Figure 5.18. There is no differential low noise source generator at the lab to form the inputs for the test of the ADC. Therefore, the first test are done with a DC value and a sine input. Hence, a second harmonic is expected at the output. The circuit is biased and supplied properly with the desired input and the clock and the 3-bit digital outputs are connected to an oscilloscope. These outputs are saved on a memory stick with the oscilloscope. The oscilloscope can save 4 million data with 40 ns step sizes. Therefore 160 ms long data is saved. The clock frequency is 1.6 MHz and 32768 data is needed to test the IC which is 10.24 ms long. However, the clock might slightly change and be 1.599MHz or 1.601MHz. This would cause some data to be removed or saved wrong. Because of that, the clock signal is also saved and all the data is observed in MATLAB as Figure 5.19.

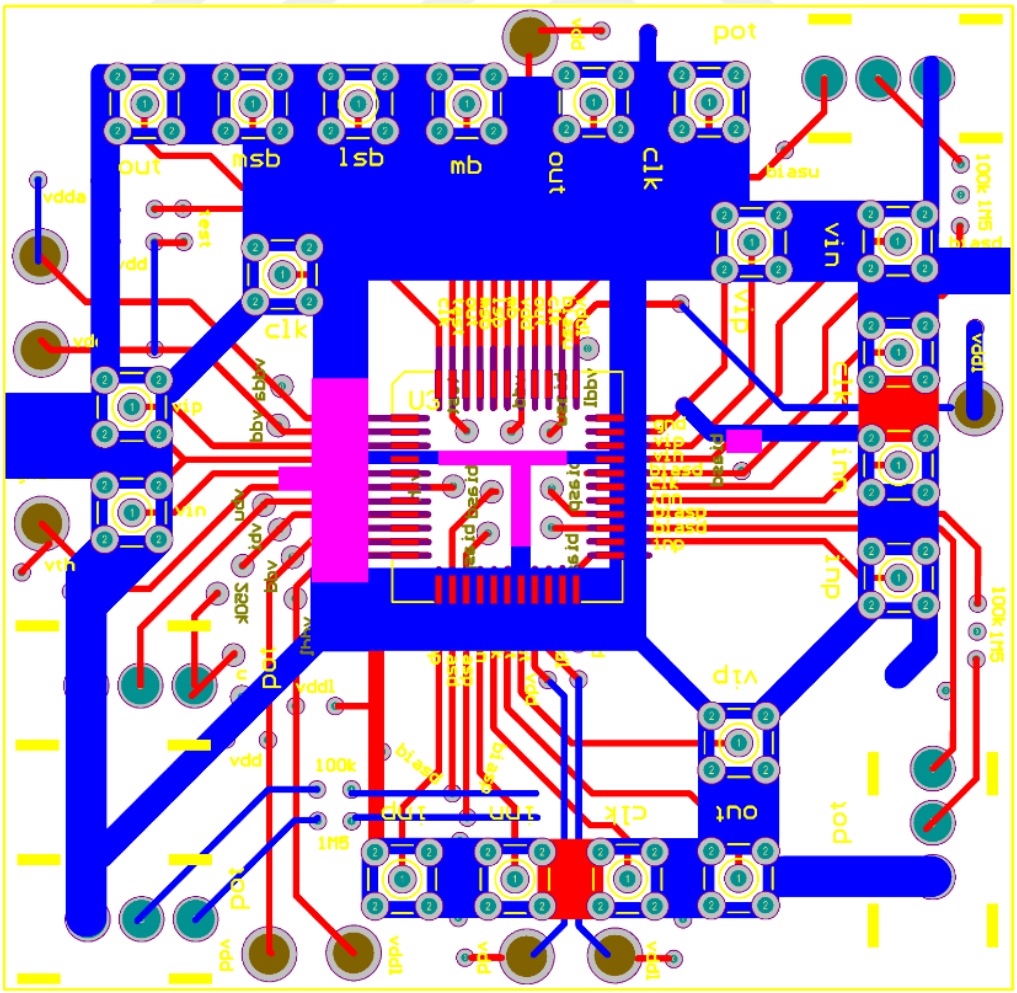

Figure 5.18. Test PCB of the updated 3rd order 3-bit SD ADC.

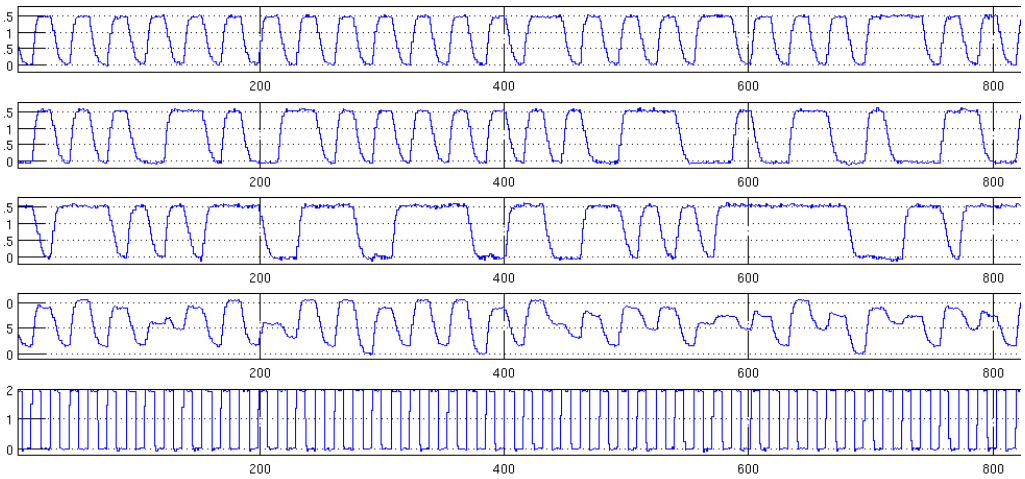

Figure 5.19. The outputs of the updated 3rd order 3-bit SD ADC observed in the oscilloscope.

When the signals in Figure 5.19 are observed, rise and fall times of the signals are very high. The inverters at the outputs should have been designed larger to drive larger output capacitances. However, the data is nearly settled when the clock changes from logic high to logic low. Thus, a code can get the data of the outputs and save those values as logic high or low depending on their values when the clock changes from logic high to logic low. Afterwards, the most significant bit is multiplied with 4, the middle bit is multiplied with 2 and they are added to least significant bit to have an ideal DAC output to do the FFT operation. Therefore, the oscilloscope is used as a logic analyzer and a very long data is saved and processed with MATLAB which is depicted in Figure 5.20.

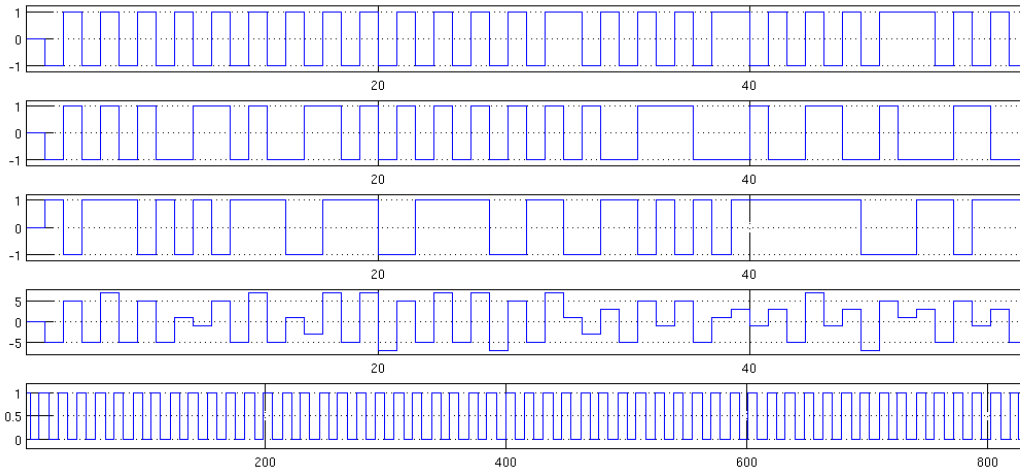

Figure 5.20. The outputs of the updated 3rd order 3-bit SD ADC transferred to the MATLAB.

The next step is the calculation of SNDR which is done in the same MATLAB code. The SNDR value is not as good as expected as shown in Figure 5.21 when a short period of the output is in Figure 5.22. Again, there is a very high noise floor than expected in the test results. So, the next step is to observe the outputs when the inputs are equal to the common mode voltage.

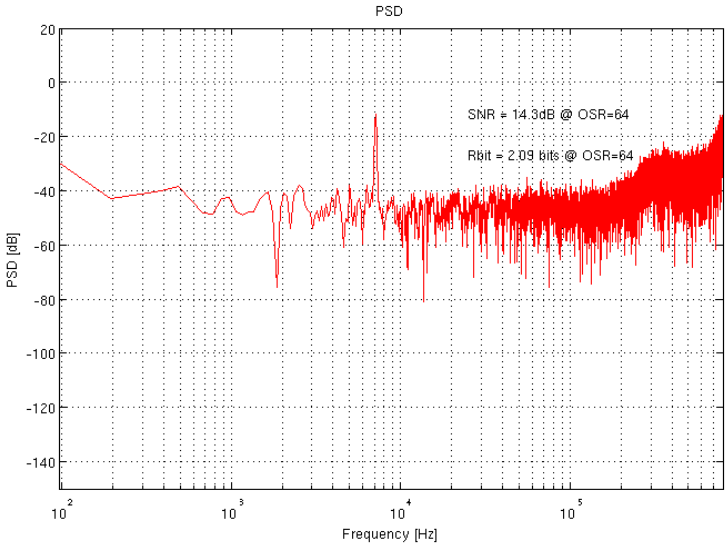

Figure 5.21. FFT of the updated 3rd order 3-bit SD ADC in the oscilloscope.

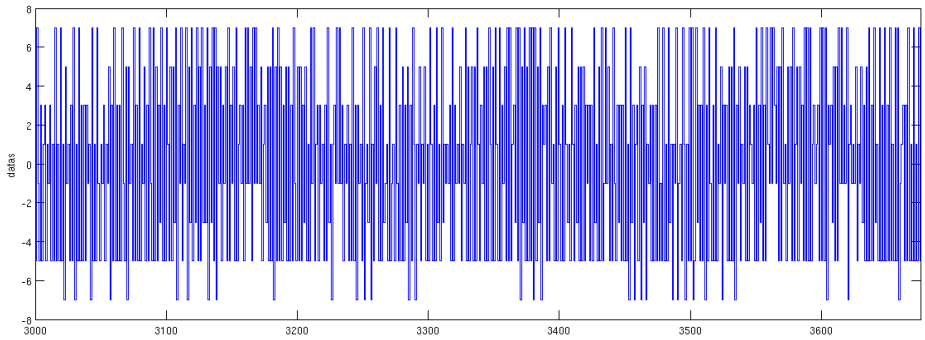

Figure 5.22. 3-bit outputs updated 3rd order SD ADC.

Furthermore, the common mode voltage is applied to both inputs to test the IC. All the data is collected by the oscilloscope again as in Figure 5.23. According to the data processed in MATLAB which is depicted in Figure 5.24, the FFT plot becomes as Figure 5.25. Instead of having a low noise floor and the desired noise shaping, the noise floor is very high and the noise shaping is not observed in the FFT plot. Moreover, a short period of

the output is depicted in Figure 5.26. In the output, it is expected to see small changes around midpoints such as “100” and “011”. Nevertheless, the output is also oscillates randomly instead of usually staying around “100” and “011”.

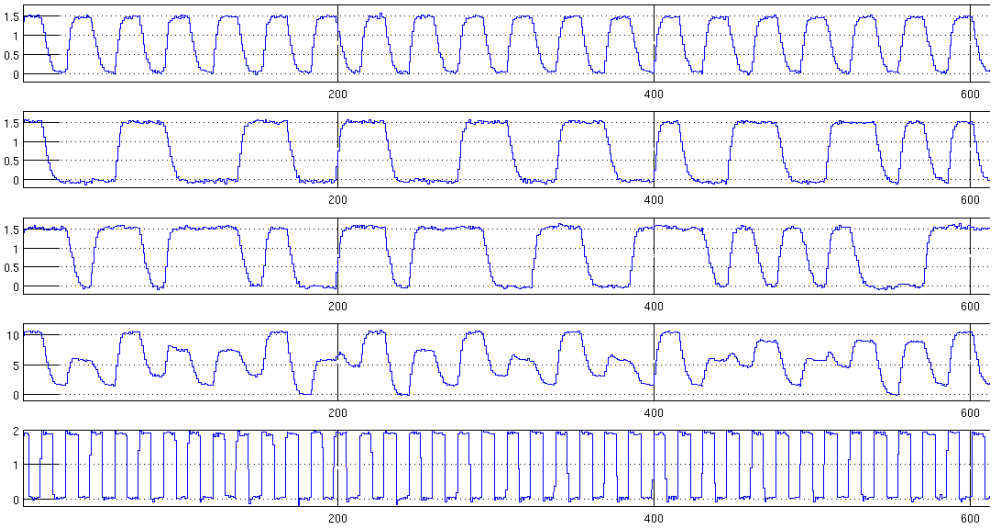

Figure 5.23. The outputs of the updated 3rd order 3-bit SD ADC in the oscilloscope when the inputs are virtual ground.

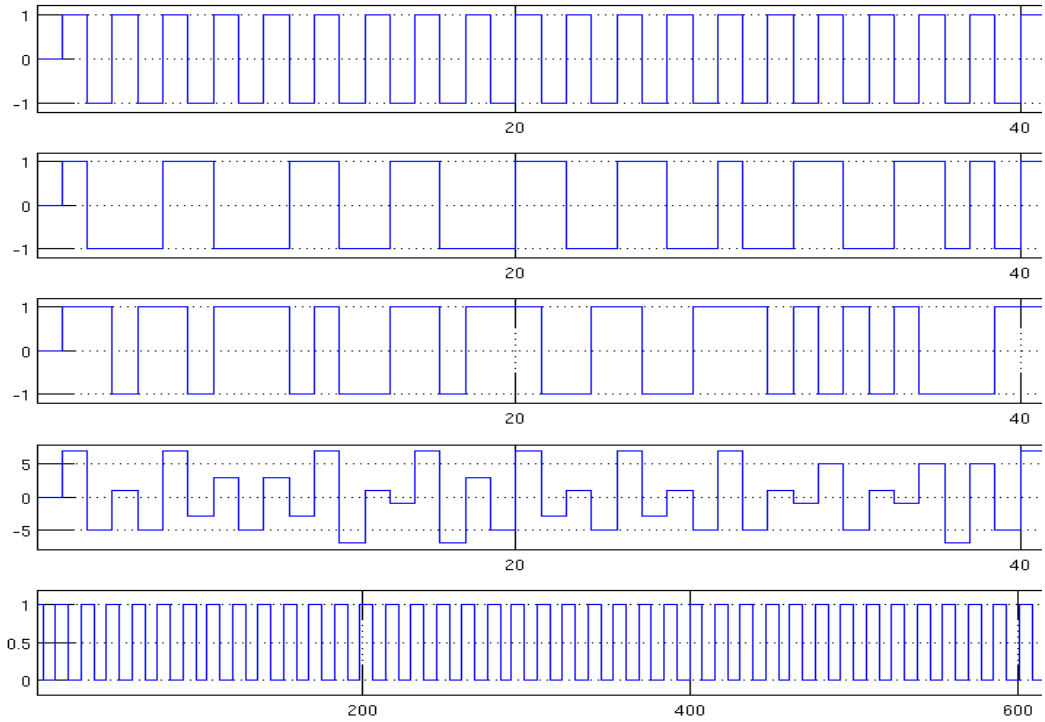

Figure 5.24. The outputs of the updated 3rd order 3-bit SD ADC transferred to the MATLAB when the inputs are virtual ground.

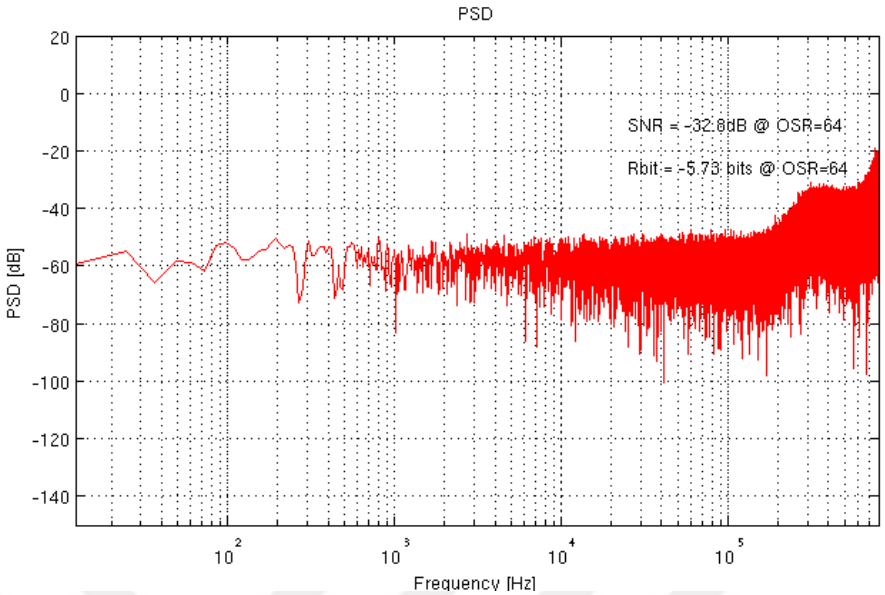

Figure 5.25. FFT of the updated 3rd order 3-bit SD ADC in the oscilloscope when the inputs are virtual ground.

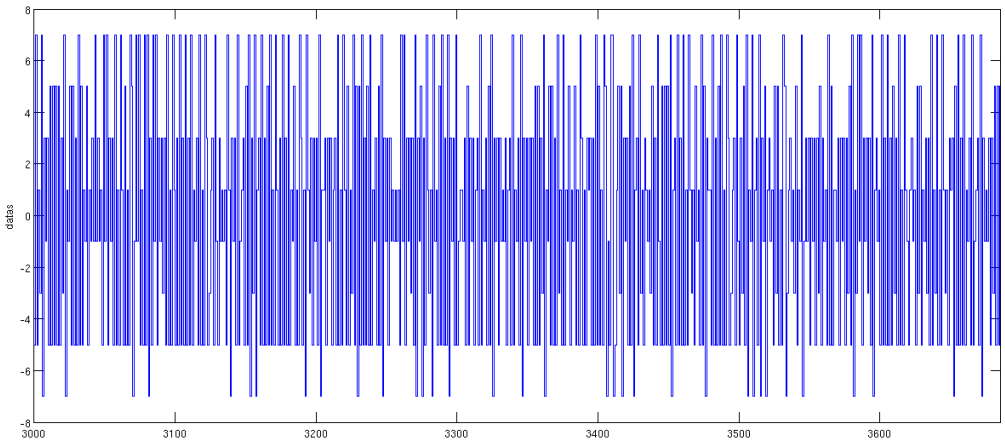

Figure 5.26. 3-bit outputs updated 3rd order SD ADC when the inputs are virtual ground.

There is an instability issue after the production most probably caused by the process variations. This instability might also be caused by the noise of the common mode voltage even though large capacitances are connected at this node to filter out the noise. Although the bias current resistor, the supply and bias voltages are adjusted, no improvement is achieved. The current consumption of the supply voltage varies from a few microwatts to a few milliwatts from IC to IC. Moreover, some of the ICs have their digital outputs stuck at "1" or "0" and stay the same even though the effects of the clock signal at the output nodes are observed. An additional problem is that the ICs don't have any ESD protection diodes

which could lead to stuck at “1” or “0” problems. After many tests, the working ICs are also broken most probably because of this issue. There were some unpackaged ICs, which are packaged after but neither of them are working.

5.2.2. Experiments with the Current Mode SD ADC

The current mode part in the IC is also tested. During the tests, it is realised that the inverters at the output of the circuit were not big enough to operate for the load of the pads, wires probes and the oscillator itself. Therefore, proper logic high or low signals could not be obtained. Thus, the ADC clock frequency is reduced to one tenth. Nevertheless, this changes the transfer function coefficient because the coefficient is directly proportional to sampling frequency. Moreover, post-layout simulations show the 2nd order SD ADC doesn’t have noise shaping when there is no input. Furthermore, the clock signal path is just next to one of the inputs and had major effect on that input turning it into a square wave voltage input with 100mV amplitude. So, it is decided to design the same ADC with the next IC produced.

5.3. IC 2015

The third IC is designed in UMC 130 nm technology and contained many ADCs as seen in Figure 5.27. Bottom left part contains the 2nd order feed-forwards SD ADC. Top left part and bottom right part contain two 3-bit feed-forward 2nd order SD ADC with different coefficients. Top right is the 2-1 MASH SD ADC while the left middle part is the current mode 2nd order CT SD ADC. Right middle part contains two hybrid ADCs with different opamps. Before the tests are done, all the source generators are tested with different oscilloscopes and all of them had second harmonics at -40 dB less than the amplitude of the input. Moreover, the third harmonics are usually around -50 dB less than the input amplitude. Thus, it is concluded that there is no test equipment to generate low noise differential inputs to test the SD ADC properly after testing the equipment. Therefore, virtual ground common voltages are used as DC inputs to observe the noise power and the noise shaping in the designs.

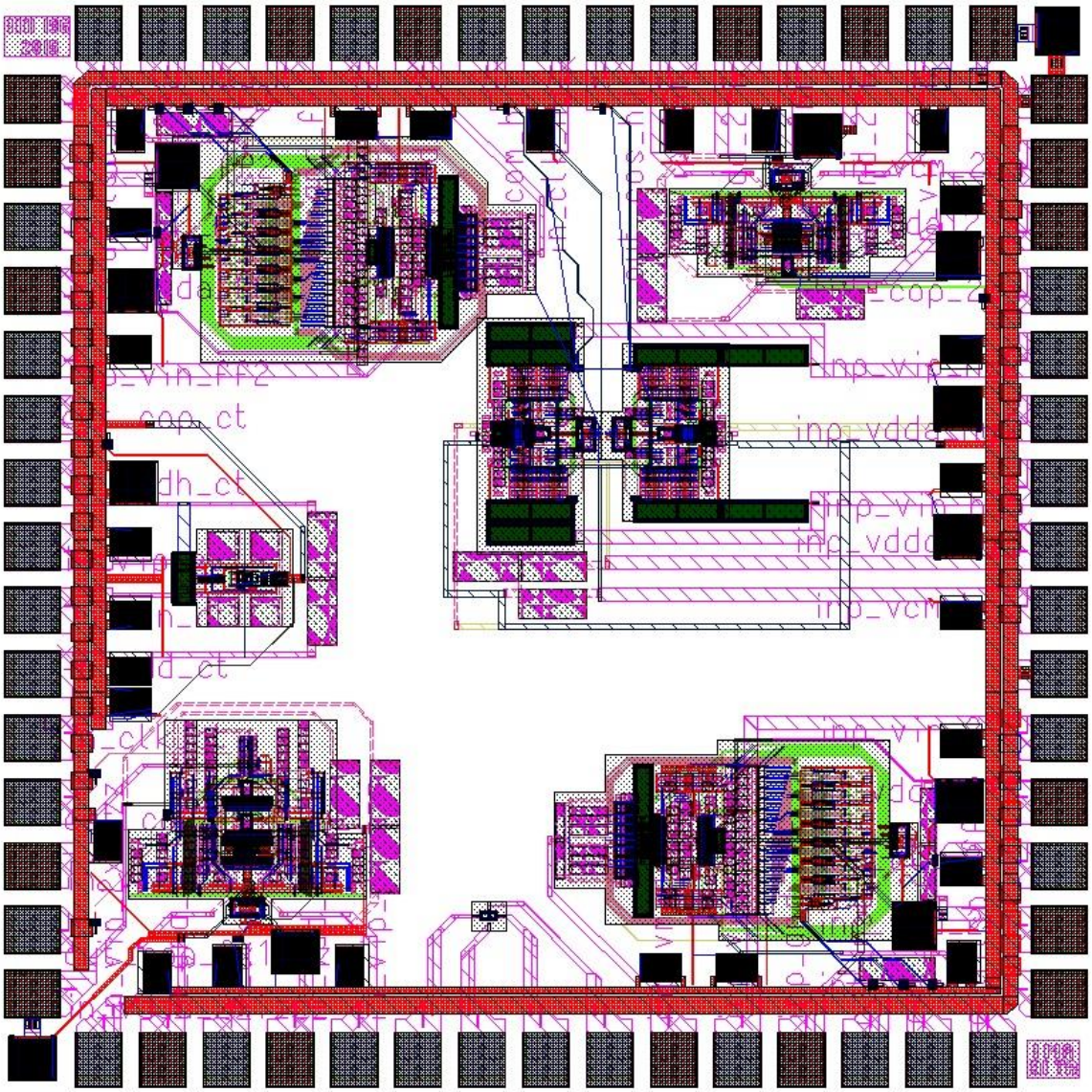

Figure 5.27. The layout of the third IC sent to production.

The clock signals and the outputs are saved via an oscilloscope that can save four million data up to 5 Giga samples per second. A MATLAB code is used to transfer the data into logic signals. The clock signal is also saved to synchronize the output data. The output data value is saved as logic high or low with the falling edge of the clock signals because it settles by then. Moreover, the clock is double the frequency of the sampling frequency because of the D flip-flop circuit used in the clock distribution block. Thus, the code is adjusted as it is going to save data every two clock cycles.

5.3.1. Experiments with the Feed-Forward 2nd Order SD ADC

First of all, the SD ADC in Figure 2.22 is tested. When DC virtual grounds are applied as inputs of the SD ADC, the FFT results become as in Figure 5.28. Here, there is noise shaping but it looks weird. All of the ICs are tested and similar results are obtained. Since there are no differential source generators to test the IC, a sine input with 100 mV amplitude with a DC voltage equal to the virtual ground is applied for an input while the other input is still virtual ground. Figure 5.29 shows that the 2nd order 1-bit SD ADC is operating as intended. The high noise in low frequencies are caused by the offset between the sine input DC voltage and the virtual ground voltage generated by different sources. If the input amplitude is increased to 200 mV, second harmonic occurs in the FFT result as in Figure 5.30 showing that the advantage of fully differential design is lost. Even though the signal power rose approximately 6 dB, the second harmonic occurred and the increase in SNDR is only 4.8 dB. The performance is expected to increase greatly by using two differential 300 mV sine inputs.

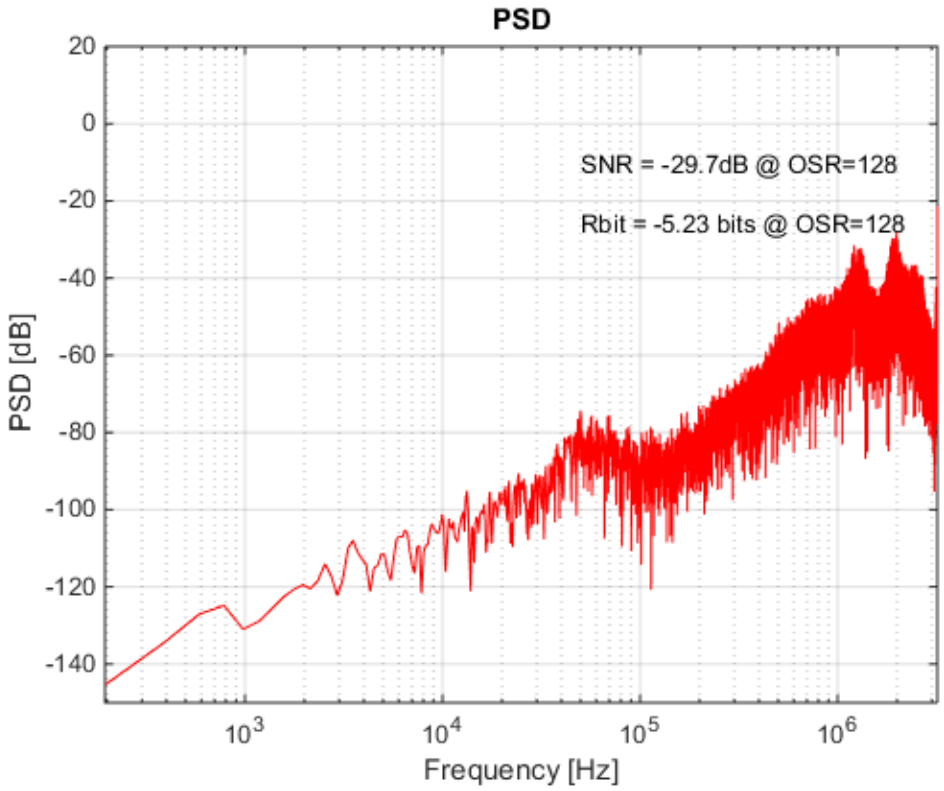

Figure 5.28. FFT of the 2nd order SD ADC tests with virtual ground inputs.

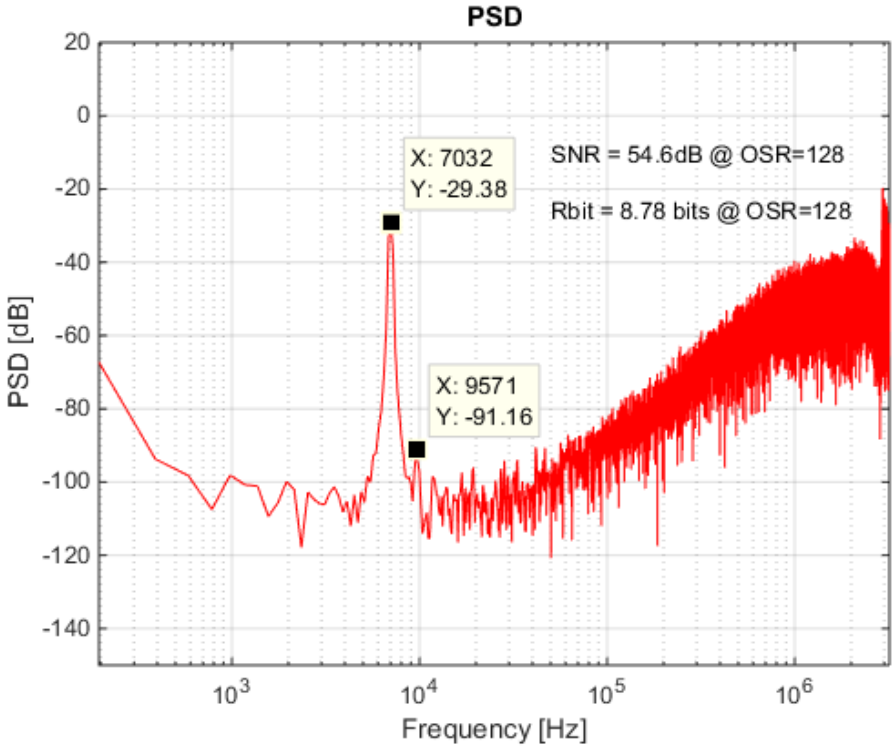

Figure 5.29. FFT of the 2nd order SD ADC tests when an input is a sine input 100 mV amplitude and the other is virtual ground.

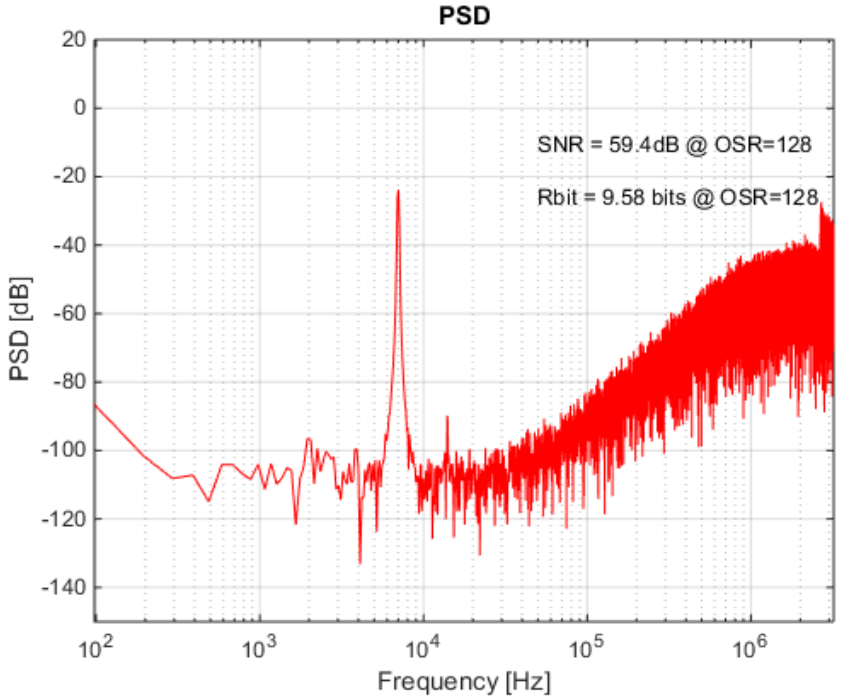

Figure 5.30. FFT of the 2nd order SD ADC tests when an input is a sine input 200 mV amplitude and the other is virtual ground.

5.3.2. Experiments with the 3-bit Feed-Forward 2nd Order SD ADC

The 2nd order 3-bit feed-forward SD ADC in Figure 2.55 is tested. The 3-bit output data saved via the oscilloscope in Figure 5.31 is decided as logic high or low at each two clock cycles when the second clock pulse drops from high to low. The 3-bit outputs are added to each other and the output is found as in Figure 5.32.

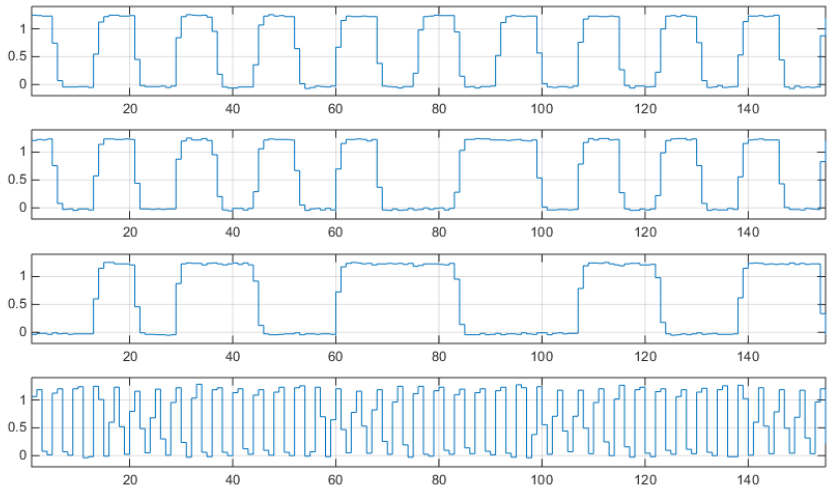

Figure 5.31. The outputs of the 2nd order 3-bit SD ADC observed in the oscilloscope.

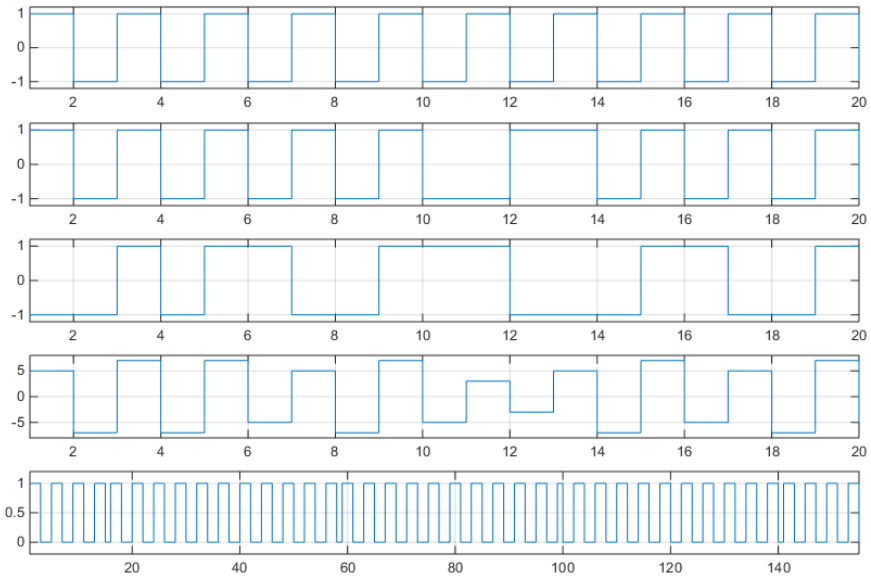

Figure 5.32. The outputs of the 2nd order 3-bit SD ADC transferred to MATLAB.

Even though the output oscillates weirdly as in Figure 5.33, the FFT of the output has low noise floor as in Figure 5.34. Furthermore, the tests of some ICs show that the output changes only between bits 011 and 100 as in Figure 5.35 and Figure 5.36 as expected, but the FFT of the output of that ICs has a high noise floor as in Figure 5.37. The results obtained from each IC has similar results to these results.

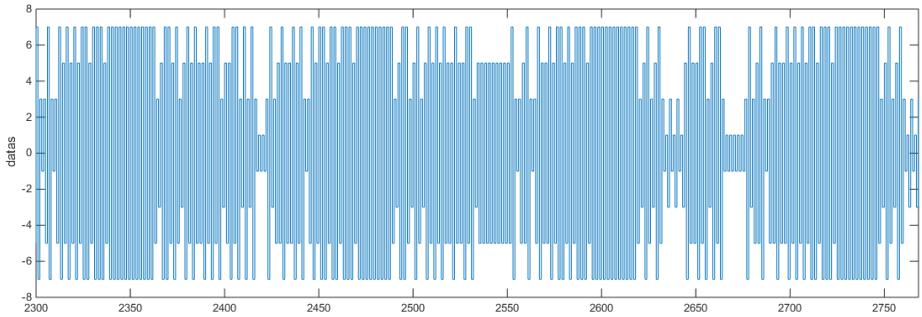

Figure 5.33. The output of the 2nd order 3-bit SD ADC.

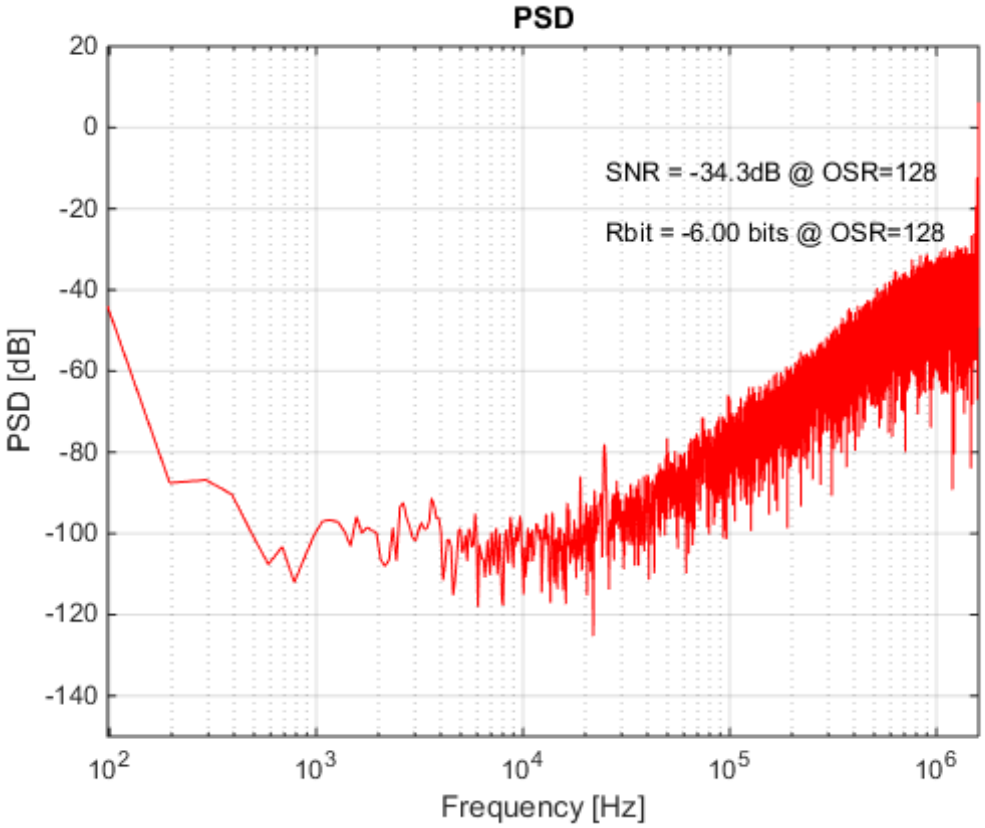

Figure 5.34. The FFT of the output of the 2nd order 3-bit SD ADC.

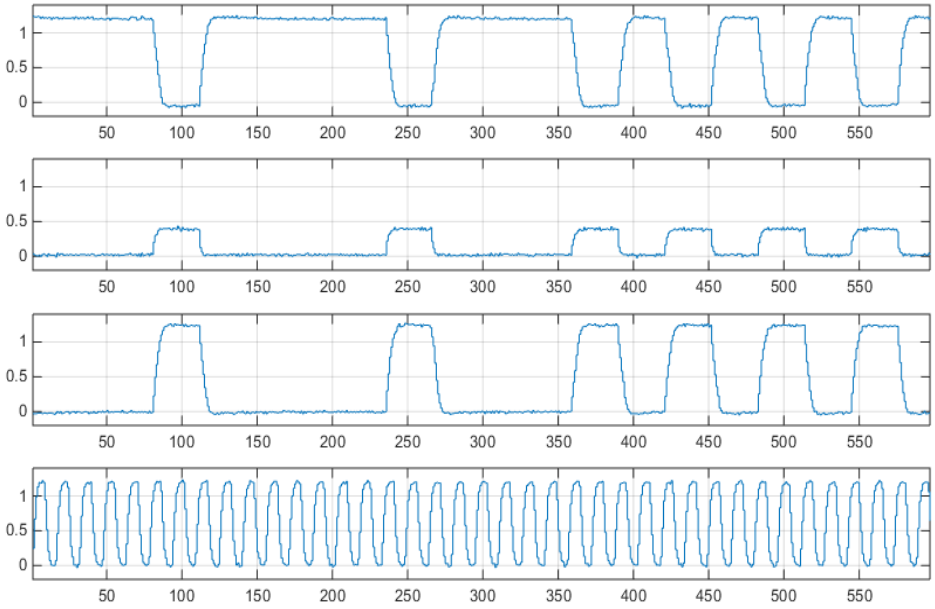

Figure 5.35. The clock and the outputs of the 2nd order 3-bit SD ADC observed in the oscilloscope.

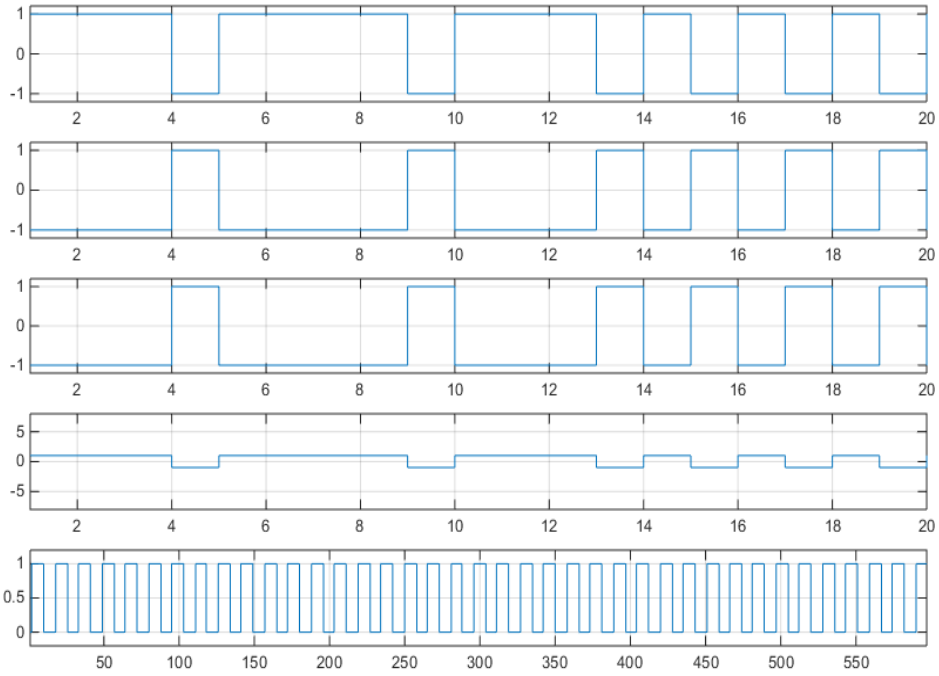

Figure 5.36. The outputs of the 2nd order 3-bit SD ADC transferred to MATLAB.

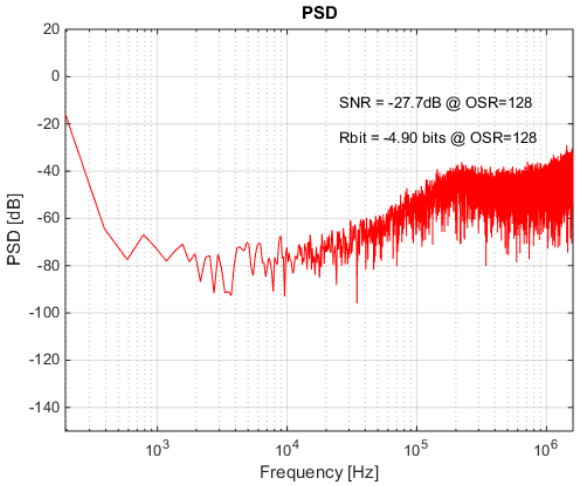

Figure 5.37. The FFT of the output of the 2nd order 3-bit SD ADC.

5.3.3. Experiments with the 2-1 MASH SD ADC

The output of the 2nd order part and the output of the 1st order part of the 2-1 SD ADC MASH is saved via the oscilloscope as saved with the same method introduced for this IC. In MATLAB, the 2nd order part output data $Y_1 z^{-1}$, the inverse of the previous clock data of the 1st order part $-Y_2$, twice of the current clock data of the 1st order part $2Y_2 z^{-1}$, and the inverse of the next clock data of the 1st order part $Y_2 z^{-2}$ are added up to obtain the digitally shaped output. So the FFT of the digitally added output becomes as Figure 5.38. Figure 5.39 shows the FFT result of the output of the 2nd order part and the 2-1 MASH part at the same time to observe 3rd order shaping clearly. However, half of the ICs are either stuck at 1 or 0 outputs.

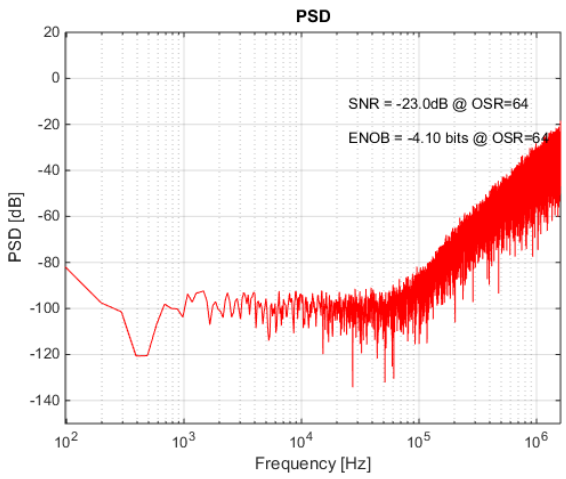

Figure 5.38. 2-1 MASH SD ADC test IC FFT result.

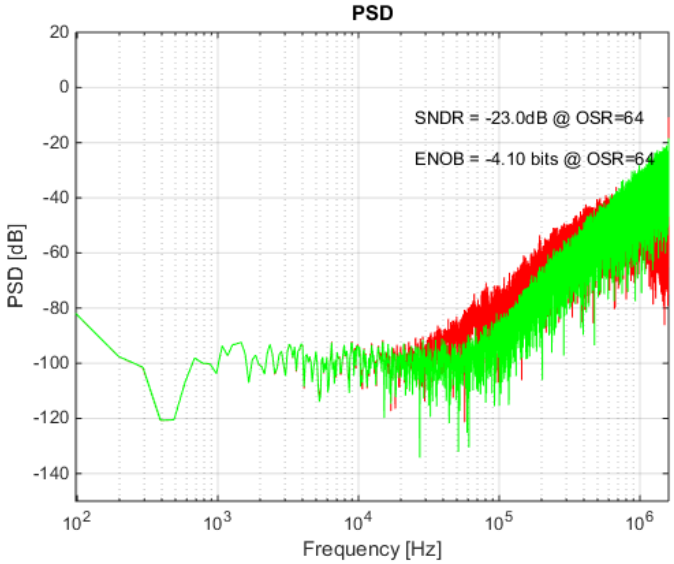

Figure 5.39. 2-1 MASH SD ADC test IC and the 2nd order part FFT result.

5.3.4. Experiments with the Current Mode SD ADC

The same 2nd order current mode SD ADC in Figure 3.33 is designed in UMC 130 nm technology. Here, it is even more difficult to apply current mode differential input signals. Therefore, current input signals are not applied by disconnecting the inputs. The clock signal and the output signals are saved at the oscilloscope as in Figure 5.40 and converted into digital signals as in Figure 5.41. The FFT of the output is shown in Figure 5.42. All of the FFT outputs are similar but they have different offsets. Even though the number of logic high outputs should be the same of low outputs, the distribution is quite different in both logic high or low and this offset causes high peak at the DC points.

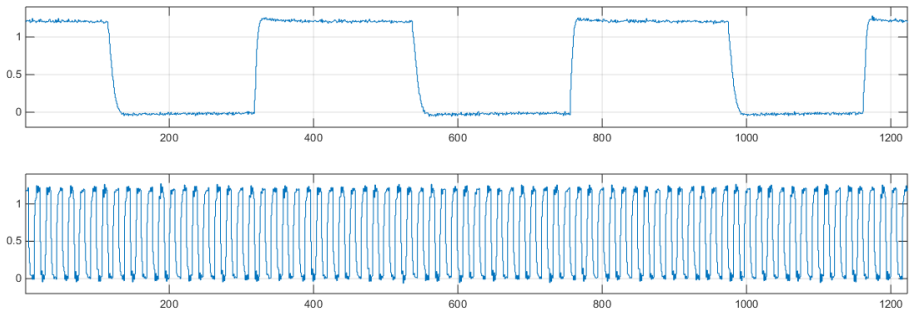

Figure 5.40. The output of the current mode 2nd order CT SD ADC observed in the oscilloscope.

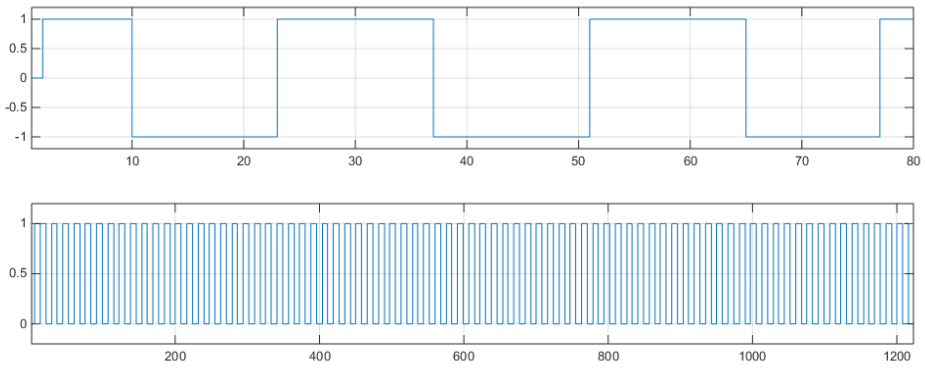

Figure 5.41. The output of the current mode 2nd order CT SD ADC transferred to MATLAB.

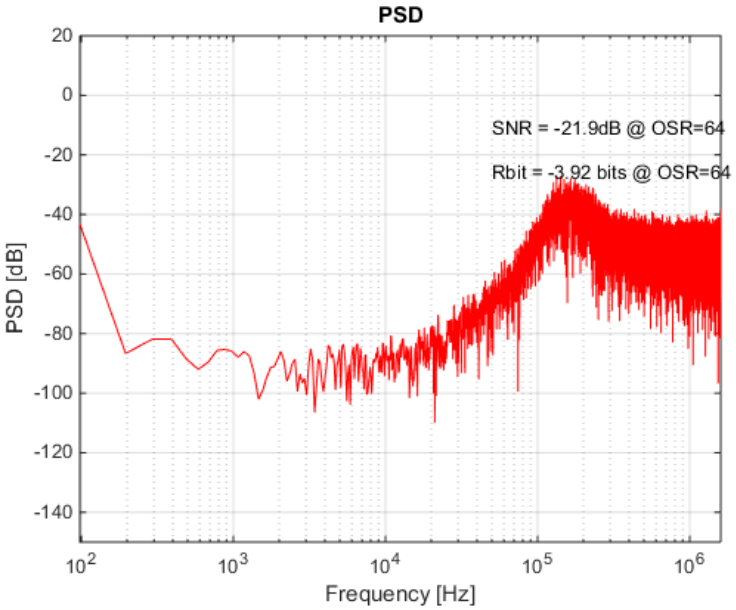

Figure 5.42. 2nd order CT SD ADC test IC FFT result.

5.3.5. Experiments with the Hybrid SD ADC

Since double sampling method is used for the hybrid design, the clock frequency is chosen 1.6 MHz for 64 OSR. The 2nd order hybrid SD ADC was designed with two different folded cascode opamps with different bandwidths. First, the ADC containing folded cascode opamps with lower bandwidth is tested. The output of the ADC is saved in the oscilloscope and transferred to MATLAB. The FFT result is depicted as in Figure 5.43 when DC common mode inputs are applied. If a sine input with 100 mV amplitude is applied to one of the inputs, the FFT result becomes as in Figure 5.44. When the input amplitude is increased to

200 mV, the frequency response becomes as in Figure 5.45. Figure 5.46 shows the frequency response when the input amplitude is increased to 300 mV. According to these tests, calculated SNDR is much lower than expected even though the signals are seen clearly and the noise at DC frequencies is removed. This is due to the jitter of the clock or the input. The power of the input signal at the applied frequency is less than expected because there is also signal at slightly higher and lower frequencies. This causes less SNDR value because the signal power is distributed between these frequencies and the distributed signal power is seen as noise by the MATLAB code as it doesn't represent a sine wave frequency response. Furthermore, there are harmonics in the frequency response caused by the source generators.

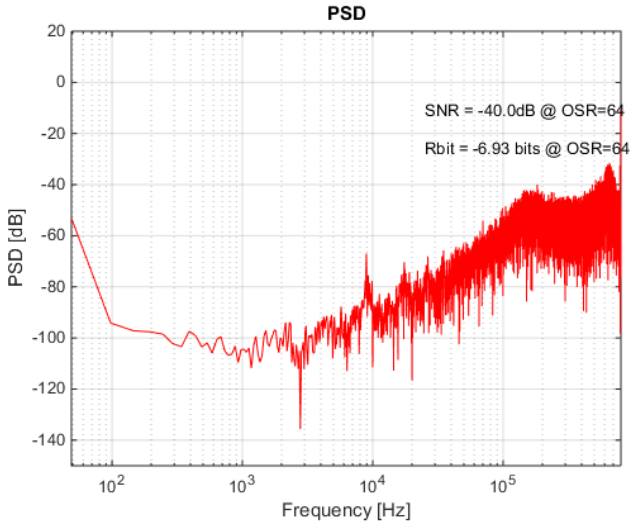

Figure 5.43. FFT of the hybrid SD ADC with DC inputs at 1.6 MHz sampling frequency.

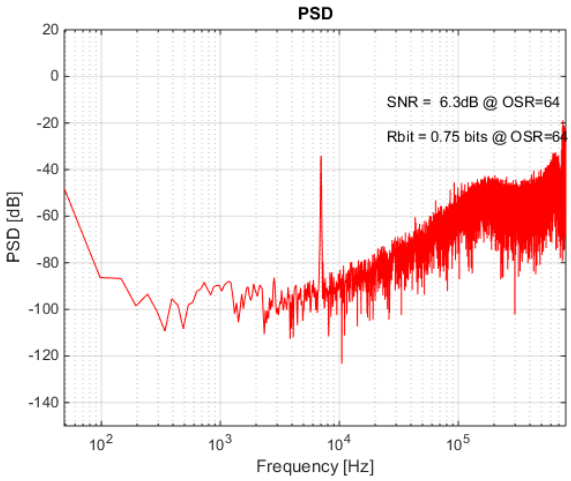

Figure 5.44. FFT of the hybrid SD ADC with a single ended input with 100 mV amplitude at 1.6 MHz sampling frequency.

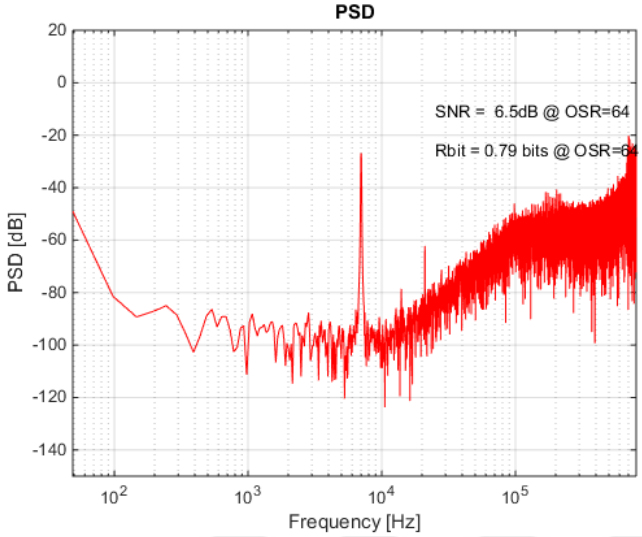

Figure 5.45. FFT of the hybrid SD ADC with a single ended input with 200 mV amplitude at 1.6 MHz sampling frequency.

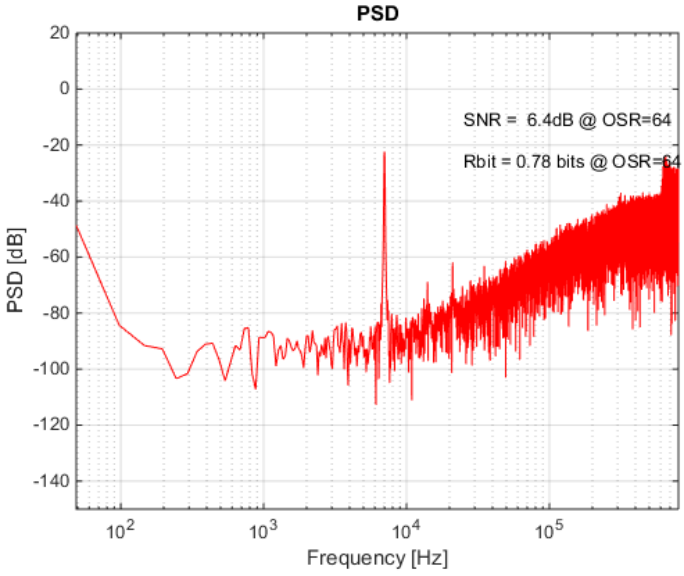

Figure 5.46. FFT of the hybrid SD ADC with a single ended input with 300 mV amplitude at 1.6 MHz sampling frequency.

As a next step, the sampling frequency is doubled. This would double the coefficient of the first integrator which would increase the voltage swing at the output of the integrators. However, the transfer function is still valid for noise shaping. The frequency response of the hybrid SD ADC would be seen in Figure 5.47 for a single ended sine input with 200 mV amplitude.

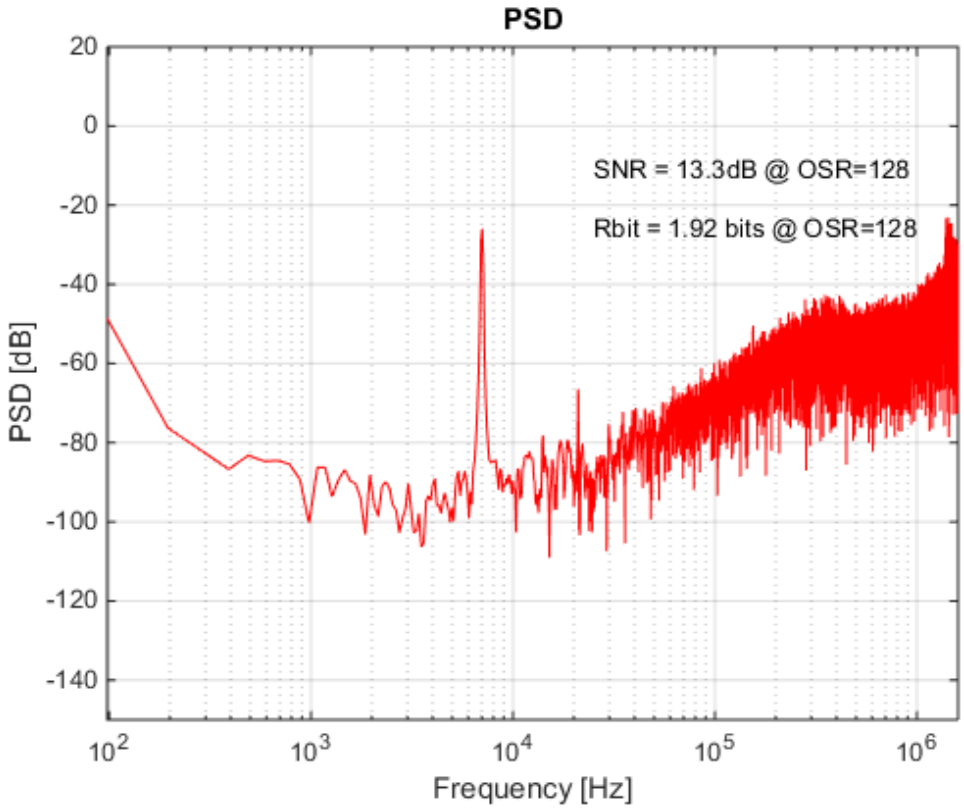

Figure 5.47. FFT of the hybrid SD ADC with a single ended input with 200 mV amplitude at 3.2 MHz sampling frequency.

The hybrid SD ADC with the folded cascode opamp with higher bandwidth is also tested. Figure 5.48 shows the frequency response test results with common mode DC inputs are used. Figure 5.49 is the frequency response test results with a single ended sine input with 100 mV amplitude while Figure 5.50 is the frequency response test results with a single ended sine input with 200 mV amplitude. When the amplitude is increased to 300 mV, is the frequency response test results becomes as Figure 5.51. The same problem with the SNDR calculation continues for these results. As a next step, the sampling frequency is doubled again. The frequency response of the hybrid SD ADC is depicted in Figure 5.52 for a single ended sine input with 200 mV amplitude. The results with the folded cascode opamp with higher bandwidth is similar to the folded cascode opamp with lower bandwidth. The second harmonic caused by the single ended inputs and the third harmonic caused by the source generators continue. However, all the results show that the hybrid SD ADC has the desired noise shaping even though the SNDR cannot be calculated correctly because of the effects of the test equipment.

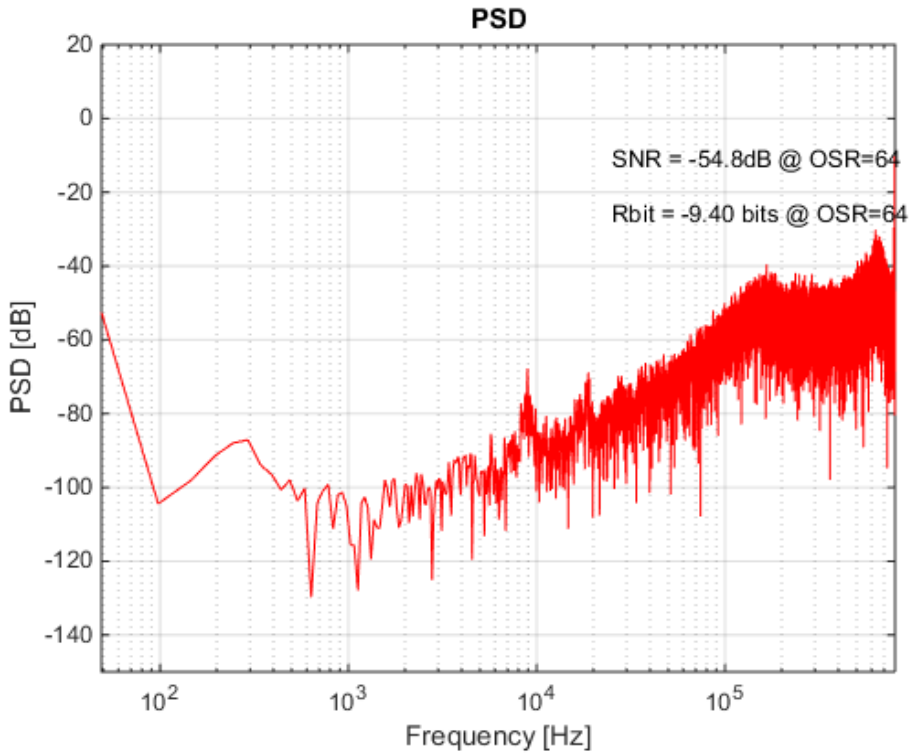

Figure 5.48. FFT of the hybrid SD ADC with DC inputs at 1.6 MHz sampling frequency.

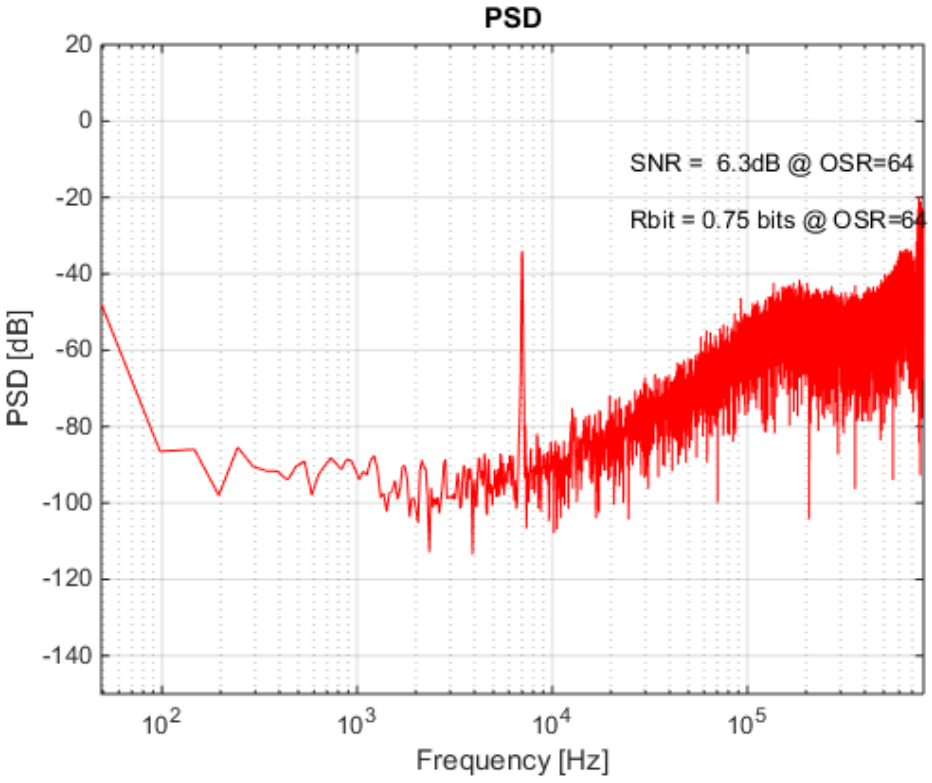

Figure 5.49. FFT of the hybrid SD ADC with a single ended input with 100 mV amplitude at 1.6 MHz sampling frequency.

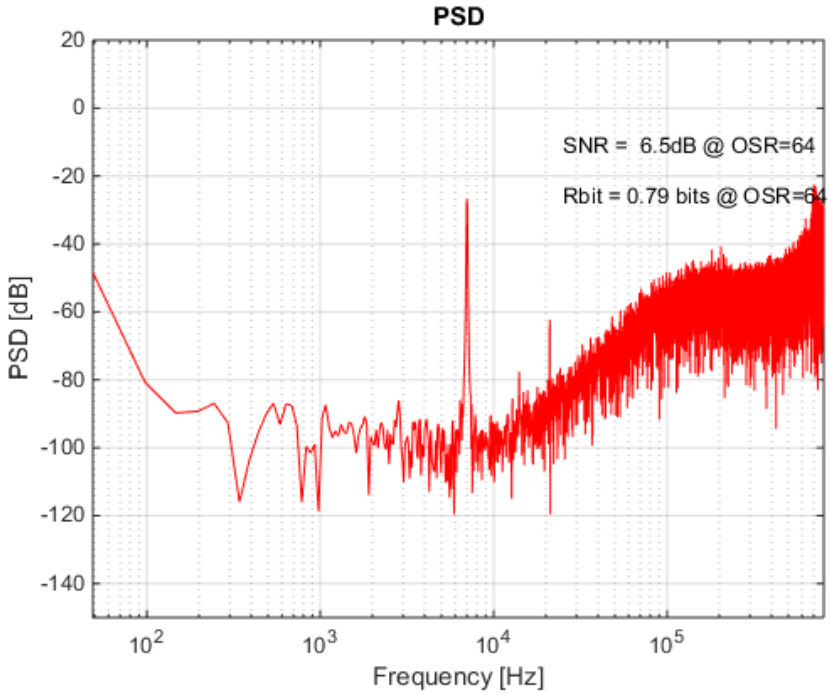

Figure 5.50. FFT of the hybrid SD ADC with a single ended input with 200 mV amplitude at 1.6 MHz sampling frequency.

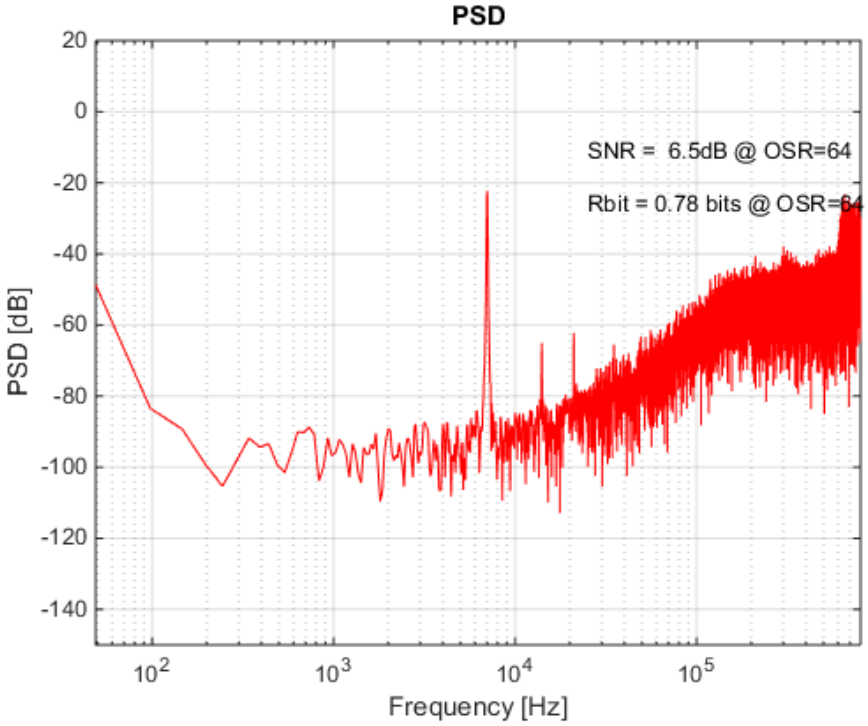

Figure 5.51. FFT of the hybrid SD ADC with a single ended input with 300 mV amplitude at 1.6 MHz sampling frequency.

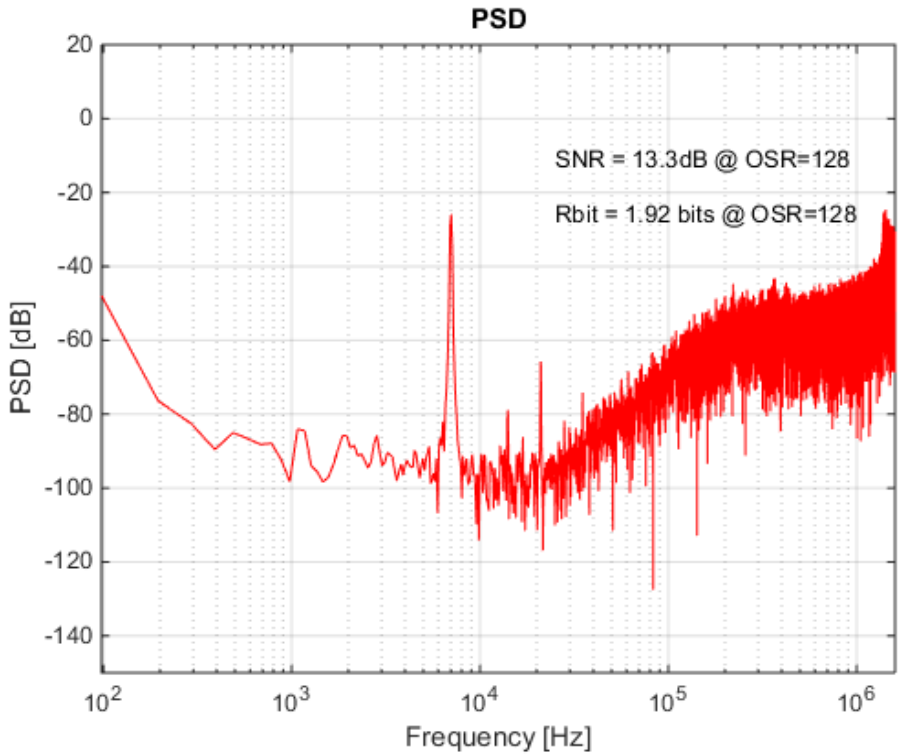

Figure 5.52. FFT of the hybrid SD ADC with a single ended input with 200 mV amplitude at 3.2 MHz sampling frequency.

5.4. IC Test Results Summary

In this chapter, the SD ADCs produced are tested to observe their performances. The test results were not as expected as the post-layout simulation results and some ADCs were not operating while the others have less performance. The signal generators used for the tests generated high noise and affected the performance of the IC test results. Moreover, the signal generators don't have the capability to generate fully differential signals for the tests of the ICs. Therefore, a single ended signal and a DC signal is used to test the ICs which caused second harmonics and low performance for the test results However, some of the SD ADCs still had good test results and high performance compared to the SD ADCs in the literature.

6. CONCLUSION AND FUTURE WORK

In this thesis, DT SD analog to digital conversion is introduced. Feed-forward, multi-bit quantization, data weighted averaging, and other power reducing methods are explained. A new feed-forward path method which helps the addition operation to be applied easily with less switches and without performance degradation is proposed. 2nd order 1-bit and 3-bit, 3rd order and MASH DT SD ADC are investigated. The output swings of the opamps kept low not to be affected by non-linear gain and slew rate problems. Furthermore, CT integrator and modulator design methods are described. Various conventional and novel CT SD ADCs with 11 to 16 ENOB are designed for an input bandwidth of 25 kHz. Furthermore, a novel hybrid SD ADC with both CT and DT integrators is designed. The layouts of the designed SD ADCs are prepared and post-layout simulations are achieved. By using the studied SD ADC architectures, three integrated circuits are prepared, sent to production and tested.

Table 6.1 also shows a comparison between the ADCs in the literature and the post-layout simulation results achieved in this thesis. While the performance of the designs with pre-layout simulation results are very good, additional noise occurred post-layout simulations decreasing FoM slightly. Experimental results are not included in the table because the tests could not be done as intended. Proper performance results could not be realized because the test equipment was not suitable for low noise applications. Still, high SNDR is obtained according to the post-layout simulations with low power consumption in these designs and the FoM value is very close to the best SD ADCs in the literature. Therefore, the proposed feed-forward path method is applicable and more suitable for some applications. Moreover, the designs in the thesis have good performance results according to [26] which contains a very detailed literature research amongst all types of ADCs.

Table 6.1. Comparison of each designed SD ADC with the literature.

SD ADC	OSR	BW (kHz)	Type	Tech (nm)	Power consumption (µW)	SNDR (dB)	FoM (fJ/conv)
[4]	16	100	DT	180	140	84	54
[27]	85	20	VCO	90	0.44	44.2	83
[28]	64	20	CT	130	28.6	79.1	97
[29]	128	24	CT	180	280	98.2	88
[30]	64	24	CT	180	90	92.5	54
[31]	48	20	DT	130	34	81	93
[32]	62.5	20	DT	130	35.2	81.7	88
2nd order feed-forward	128	25	DT	130	54.5	80.3	129
2nd order 3-bit	64	25	DT	130	102.5	87	112
2nd order with SAR (pre-layout simulations)	32	25	DT	180	16.9	76.8	60
3rd order 3-bit (pre-layout simulations)	32	25	DT	180	11.65	94.5	5.37
Updated 3rd order 3-bit	32	25	DT	180	28.2	78.8	79
2nd order CT active RC with ideal components	256	25	CT	130	-	84.8	-
Current mode without transient noise	256	25	CT	180	6.95	94.4	2.1
Current mode with transient noise	256	25	CT	180	6.95	60	100
2nd order hybrid	64	25	DT	130	27.2	69.8	216

REFERENCES

1. Boser, B.E. and B.A.Wooley, "The design of sigma-delta modulation analog-to-digital converters", *Solid-State Circuits, IEEE Journal of*, Vol. 23, No. 6, pp.1298-1308, 1988.

2. Pesenti, S., P. Clement and M. Kayal, "Reducing the Number of Comparators in Multibit ∑Δ Modulators", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 55, No. 4, pp. 1011-1022, 2008.

3. Lee, K., M. R. Miller and G. C. Temes, "An 8.1 mW, 82 dB Delta-Sigma ADC With 1.9 MHz BW and –98 dB THD", in *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 8, pp. 2202-2211, 2009.

4. Pena-Perez, A., E. Bonizzoni and F. Maloberti, "A 88-dB DR, 84-dB SNDR Very Low-Power Single Op-Amp Third-Order ΔΣ Modulator", *Solid-State Circuits, IEEE Journal of*, Vol. 47, No. 9, pp. 2107-2118, 2012.

5. Chae, Y. and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator", in *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 2, pp. 458-472, 2009.

6. Schreier, R. and G. C. Temes, *Understanding Delta Sigma Converters*, IEEE Press, New Jersey, 2005.

7. Malcovati, P., S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato and A. Baschirotto, "Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators", *IEEE Trans. Circuits Syst. I*, Vol. 50, No. 3, pp. 352–364, 2003.

8. Maloberti, F., *Data converters*, Springer, Dordrecht, 2007.

9. Norsworthy S.R., R. Schreier and G.C. Temes, *Delta-Sigma Data Converters Theory, Design, and Simulation*, IEEE Press, New York, 1998.

10. Dessouky, M. and A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping", in *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 3, pp. 349-355, 2001.

11. Yao, L., M. Steyaert and W. M. C. Sansen, *Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS*, Springer, Dordrecht, 2006.

12. Choksi, O. and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit", in *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 50, No. 12, pp. 906-917, 2003.

13. Baird, R.T. and T. S. Fiez, "Improved ΔΣ DAC linearity using data weighted averaging", *Circuits and Systems, 1995. ISCAS '95*, pp. 13-16, 1995.

14. Samid, L. and Y. Manoli, "A multibit continuous time sigma delta modulator with successive-approximation quantizer," *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, Island of Kos, pp. 4, 2006.

15. Hurst, P. J. and W. J. McIntyre, "Double sampling in switched-capacitor delta-sigma A/D converters", *Circuits and Systems, 1990, IEEE International Symposium on*, pp. 902-905, 1990.

16. Degrauwe, M., J. Rijmenants, E. Vittoz and H. De Man, "Adaptive Biasing CMOS Amplifiers", *IEEE Journal of Solid-State Circuits*, Vol. 17, No. 3, pp. 522-528, 1982.

17. Roh, J., "High-gain class-AB OTA with low quiescent current", *Analog Integr. Circuits Signal Process.*, Vol. 47, No. 2, pp. 225–228, 2006.

18. Sansen, W. M. C., *Analog Design Essentials*, Springer, Dordrecht, 2006.

19. Cherry, J. A. and W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulators for High speed A/D Conversion*, Kluwer Academic Publisher, Dordrecht, 1999.

20. Ortmanns, M. and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits And Robust Implementations*, Springer, Dordrecht, 2006.

21. Palaskas Y. and Y. Tsividis, "Dynamic range optimization of weakly nonlinear, fully balanced, Gm-C filters with power dissipation constraints", in *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 50, No. 10, pp. 714-727, 2003.

22. Keller, M., A. Buhmann, J. Sauerbrey, M. Ortmanns and Y. Manoli, "A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma–Delta Modulators", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 55, No. 11, pp. 3480-3487, 2008.

23. Aboushady, H., *Design for Reuse of Current-Mode Continuous Time Sigma-Delta Analog-to-Digital Converters*, Ph.D. Thesis, University of Paris VI, Department of Electronics, Communications and Computer Science, January 2002.

24. Parsnejad, S., M. Akcakaya and G. Dundar, "A low power second order current mode continuous time sigma delta ADC with 98 dB SNDR", *Ph.D. Research in Microelectronics and Electronics (PRIME), 2014 10th Conference on*, pp. 1–4, 2014.

25. Kwan, H.-K., S.-H. Lui, C.-U. Lei, Y. Liu, N. Wong and K. –L. Ho, "Design of hybrid continuous-time discrete-time delta-sigma modulators", *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on* , pp. 1224–1227, 2008.

26. B. Murmann, "*ADC Performance Survey 1997-2015*", http://web.stanford.edu/~murmann/adcsurvey.html, accessed at May 2016.

27. Wismar, U., D. Wisland and P. Andreani, "A 0.2V 0.44 µW 20 kHz Analog to Digital ∑Δ Modulator with 57 fJ/conversion FoM", *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European* , pp. 187-190, 2006.

28. Zhang, J., Y. Lian, L. Yao and B. Shi, "A 0.6-V 82-dB 28.6- µW Continuous-Time Audio Delta-Sigma Modulator", *Solid-State Circuits, IEEE Journal of* , Vol. 46, No. 10, pp. 2326-2335, 2011.

29. Sukumaran, A. and S. Pavan, "Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback", *Solid-State Circuits, IEEE Journal of*, Vol. 49, No. 11, pp. 2515-2525, 2014.

30. Pavan, S., N. Krishnapura, R. Pandarinathan and P. Sankar, "A Power Optimized Continuous-Time ΔΣ ADC for Audio Applications", *Solid-State Circuits, IEEE Journal of*, Vol. 43, No. 2, pp.351-360, 2008.

31. Roh , H., H. Kim, Y. Choi, J. Roh, Y. Kim and J.-K. Kwon, "A 0.6-V Delta–Sigma Modulator With Subthreshold-Leakage Suppression Switches", *Circuits and Systems II: Express Briefs, IEEE Transactions on*, Vol.56, No.11, pp. 825-829, 2009.

32. Yang, Z., L. Yao and Y. Lian, "A 0.5-V 35- µW 85-dB DR Double-Sampled ΔΣ Modulator for Audio Applications", *Solid-State Circuits, IEEE Journal of*, Vol. 47, No. 3, pp. 722-735, 2012.