HIGH PERFORMANCE ADAPTIVE SIGMA DELTA MODULATOR DESIGNS

by

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ABSTRACT

HIGH PERFORMANCE ADAPTIVE SIGMA DELTA MODULATOR DESIGNS

Improvements in VLSI technology enabled data converters with increased speed. When compared to conventional converters, sigma delta modulators have a higher sampling speed for resolution; and they are less sensitive to analog circuit non-idealities.

Despite their advantages, sigma delta converters have their own challenges . As the sampling frequency increases the second order effects such as parasitic poles in the loop filter or delay of the quantizer affect the performance of the modulator. Another drawback of the SD modulator is the saturation level limitation of the integrator which has a degradation effect on resolution. To overcome these problems, architectural or circuit level solutions should be studied.

In this thesis, saturation problem of the integrator block will be discussed. Saturation problem of the Operational Amplifier that is used in the integrator block affects the dynamic input signal range of Sigma-Delta modulators. This limitation results in inaccurate outputs of the modulator. Consequently, the saturation effect should be eliminated in such a way that the integrator block of the modulator should not enter the saturated region. The analysis is carried out in two different levels.

First, analysis is carried out at behavioral level to see the performance of the modulator excluding the transistor nonidealities. In this thesis, an adaptive modulator structure is proposed. Also, the analysis with this adaptive architecture is done with behavioral models to see the feasibility of the proposed structure before implementing it in transistor level.

The adaptive architecture includes an additional logic circuitry. This logic circuitry is triggered whenever the output of the integrator is getting close to the saturation levels and connects an extra capacitance to the feedback of the integrator. By the help of this extra capacitance, the gain of the integrator is decreased dependent on the size of this capacitor.

The proposed adaptive architecture is tested with behaviorally defined components and the result turned out to be that the adaptive modulator has a better SNR performance with respect to applied input signal range.

After verifying the improvement in performance with behavioral level analysis, implementation is made with transistor level components using 0.35 um AMS technology.

All elements that compose the modulator are designed at transistor level and tested individually. These transistor level designed elements are inserted to the modulator one by one. Adaptive and non-adaptive architecture behavioral level analysis are repeated with transistor level elements.

Finally, the analysis results of the analysis done at transistor level also supports that adaptive architecture has a better SNR performance with respect to dynamic input signal range compared to non-adaptive architecture. Thus, the proposed adaptive modulator presents an alternative solution to the resolution degradation.

ÖZET

VLSI teknolojisindeki gelişmeler yüksek hızda çalışan veri dönüştürücülerin geliştirilmesine imkan vermiştir. Geleneksel veri dönüştürücüleri ile karşılaştırıldığında, sigma delta modulatörler çözünürlük için yüksek örnekleme hızlarına sahiptir ve analog devre idealsizliklerine daha az duyarlıdır.

Sigma delta dönüştürücüler avantajlarının yanı sıra beraberinde zorlukları da getirmektedir. Örnekleme frekansının artışı ile, döngü filtresindeki parazitik kutuplar veya kuantalayıcının gecikmesi gibi ikincil derece etkiler modülatörün performansını etkilemektedir. Bir diğer dezavantaj ise çözünürlükte azalmaya sebep olan sigma delta modulatörlerin toplayıcısındaki doyma sınırlamasıdır. Bu problemlerin üstesinden gelmek için mimari ya da devre seviyesinde çözümler üzerinde çalışılmalıdır.

Bu tezde, toplayıcı bloğundaki doyum problemi tartışılmıştır. Tümlev alıcı bloğu içinde kullanılan işlemsel güçlendiricinin doyum problemi Sigma-Delta modülatörlerinin dinamik giriş işaret aralığını etkilemektedir. Bu sınırlama, hatalı modulatör çıkışlarıyla sonuçlanmaktadır. Sonuç olarak, doygunluk etkisi öyle bir yöntem ile elenmelidir ki tümlev alıcı bloğu doygun alana girmemelidir. Analizler iki farklı seviyede yapılmıştır.

İlk önce, modülatorün transistör idealsizlikleri gözardı edilip davranışsal seviyede analizleri yapılarak performansı gözlenmiştir. Bu tezde, uyarlanabilir bir modülatör yapısı önerilmiştir. Ayrıca, önerilen yapının doğrulanabilirliğini önceden belirleyebilmek için transistör seviyesinde uygulanmadan önce bu uyarlanabilir mimarinin davranışsal modellerle analizleri yapılmıştır.

Uyarlanabilir mimari, içinde bir mantık devresi bulundurmaktadır. Bu mantık devresi tümlev alıcının çıkışı doygum seviyesine yaklaştığında tetiklenmekte ve fazladan bir kapasitansı tümlev alıcının geri beslemesine bağlamaktadır. Bu fazladan kapasitansın yardımı ile, tümlev alıcının kazancı kapasitansın büyüklüğüne bağlı olarak azalmaktadır.

Önerilen uyarlanabilir mimari davranışsal tanımlı bileşenlerle test edilmiş ve neticesinde uyarlanabilir modülatorün uygulanan giriş işaret aralığı gözönünde bulundurularak daha iyi bir işaret-gürültü oranına sahip olduğu belirlenmiştir.

Davranışsal seviyede yapılan analizlerle performanstaki iyileşme doğrulandıktan sonra, ikinci aşama olarak uygulama transistör seviyesindeki bileşenler ile 0.35 um AMS teknolojisi kullanılarak yapılır.

Modülatörü oluşturan tüm elementler transistör seviyesinde tasarlanmış ve ayrı ayrı test edilmiştir. Transistör seviyesinde tasarlanmış elementler modülatöre tek tek eklenmiştir. Davranışsal seviyede yapılmış uyarlanabilir ve uyarlanabilir olmayan mimari analizleri transistör seviyesi elementler ile tekrarlanmıştır.

Sonuç olarak, transistör seviyesinde yapılan analiz sonuçları da önerilen uyarlanabilir mimarinin uyarlanabilir olmayan mimariye kıyasla işaret-gürültü performansı açısından daha iyi olduğunu desteklemektedir. Bu nedenle, önerilen uyarlanabilir modulatör çözünürlük bozulmasına alternatif bir çözüm sunmaktadır.

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LIST OF SYMBOLS/ABBREVIATIONS

C	Capacitance
dB	Decibel
e_{rms}	Rms voltage
$f_{baseband}$	Baseband frequency
$f_{Nyquist}$	Nyquist frequency
$f_{sampling}$	Sampling frequency
N	Number of bits
N_{TF}	Noise transfer function
P	Power
S_{TF}	Signal transfer function
Δ	Quantization step size
Φ1, Φ2	Clock signals
A/D	Analog to Digital
ADC	Analog to Digital Converter
BW	Bandwidth
DAC	Digital to Analog Converter
FSR	Full Scale Range
LSB	Least Significant Bit
OSR	Oversampling Ratio
PSD	Power Spectral Density
SC	Schmitt Trigger
SD	Sigma Delta
SNR	Signal to Noise Ratio
VLSI	Very Large Scale Integrator

1. INTRODUCTION

All kinds of electronic equipment that we have already adapted to our lives mostly process the data in digital form. Since the signals are mainly in the analog domain in real world, conversion from analog to digital data is a must. Analog to digital converters are implemented to serve this need. The challenge in designing these converters is to optimize their performance.

Conventional converters are not truly compatible with VLSI technology. Since they are not immune to noise and interference, they need precise analog components. They use low sampling frequency. “Nyquist Rate Converters” are conventional converters which have sampling frequency of twice the bandwidth.

The mentioned drawbacks of conventional converters directed research to look for more accurate modulators with higher performances. Oversampling converters have the advantage of digital signal processing, high compatibility with VLSI technologies and robustness to mismatch of components.

Oversampling is a technique which improves the resolution obtained from the straightforward Nyquist rate PCM conversion. Oversampling converters sample the analog waveform significantly faster than conventional converters. The sampled data is quantized with N-bit ADC.

First Sigma Delta modulator was proposed in 1962 [1]. It consists of a filter, a single-bit quantizer at its forward path and a 1-bit DAC at the feedback.

A lot of research has been done about Sigma Delta modulators so far and these studies have been collected and summarized in published books [2], [3]. Different noise shaping techniques are discussed [4]. Orders of the modulators are examined to achieve the optimized SNR performance [5].

One of the main issues with Sigma Delta modulators is the limited input dynamic range which is a result of saturated integrator block. Several studies have been carried out to overcome this problem; some of them are represented in [6], [7] and [8].

In this thesis, an adaptive structure is proposed to eliminate the effect of the saturating problem.

In Chapter 2, a brief description and theory is given for Sigma Delta modulators. In Chapter 3, statement of the problem is given. In Chapter 4, proposed adaptive system architecture is analyzed in behavioral level and comparison is done with non-adaptive structure. In Chapter 5, transistor level design of the modulator components are implemented and tested individually.

Finally, in Chapter 6, transistor level adaptive and non-adaptive modulator performances are compared. The results and conclusions are given briefly at the end.

2. THEORY OF SIGMA DELTA CONVERTERS

Among all types of analog to digital converters, sigma delta converters are chosen in this thesis for implementation because of their robust structure to component non-idealities and better SNR performance compared to other conventional converters. Also, sigma delta converters are better suited for VLSI, which is easier to implement in digital circuits. Other than that, it is better to have fast digital circuits than designing precise analog circuitry.

Sigma delta converters benefit from both noise shaping and oversampling at the same time. Thus, desired speeds and resolution could be achieved using these modulators. Relatively low frequency signals are oversampled with sigma delta converters which result in better performances rather than conventional converters like “Nyquist Rate Converters”.

In Figure 2.1, there is a representation of the process of conventional converters [9].

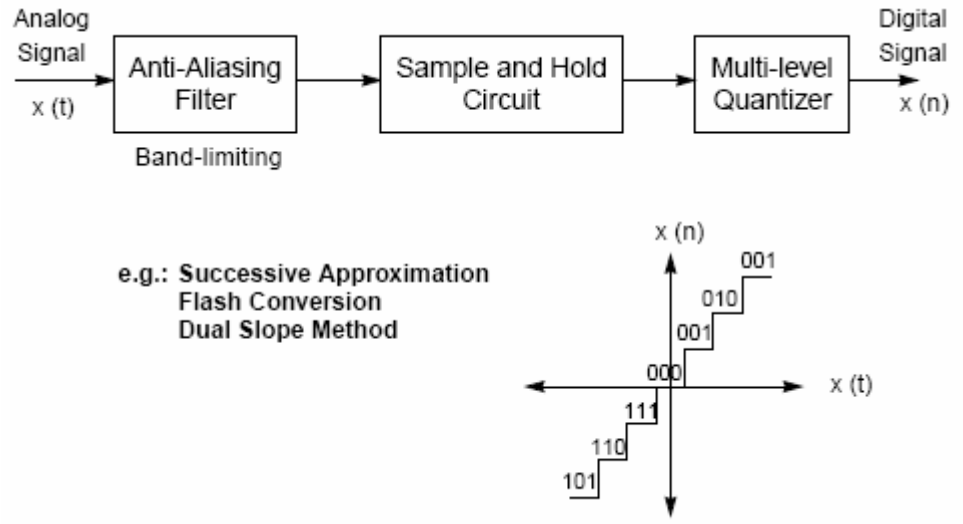

Figure 2.1. Block diagram for conventional converters [9]

In Figure 2.2, the block diagram of sigma delta modulator is shown [9].

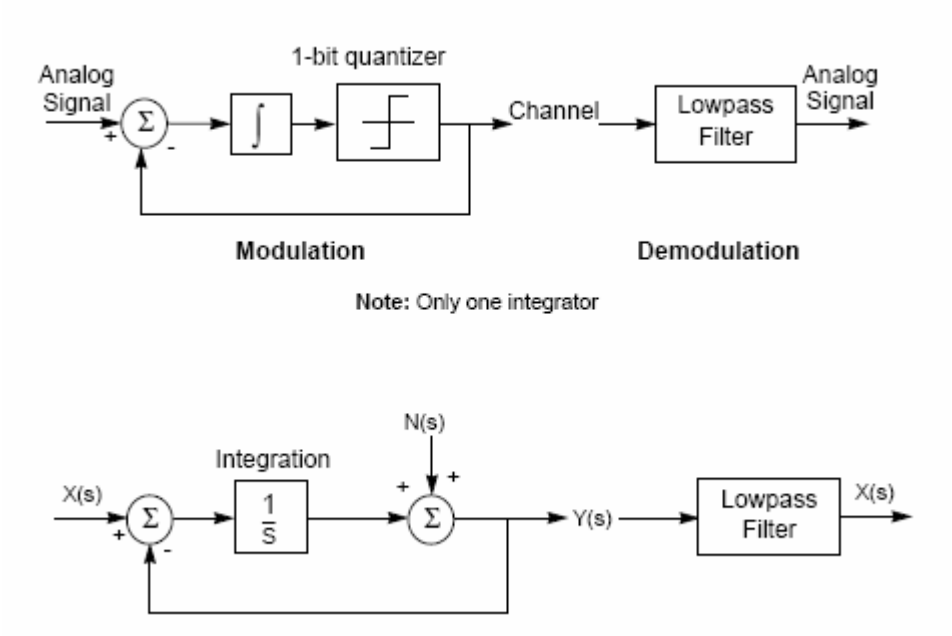

Figure 2.2. Block diagram of sigma delta modulator [9]

The quantization noise is represented with N(s) in Figure 2.2. Sigma delta modulators are suitable for digital audio and communication applications because of their noise shaping property. Sigma delta modulators use simple comparators for quantization. The quantizer encodes the integral of the signal so its sensitivity is dependent on the change rate of the signal.

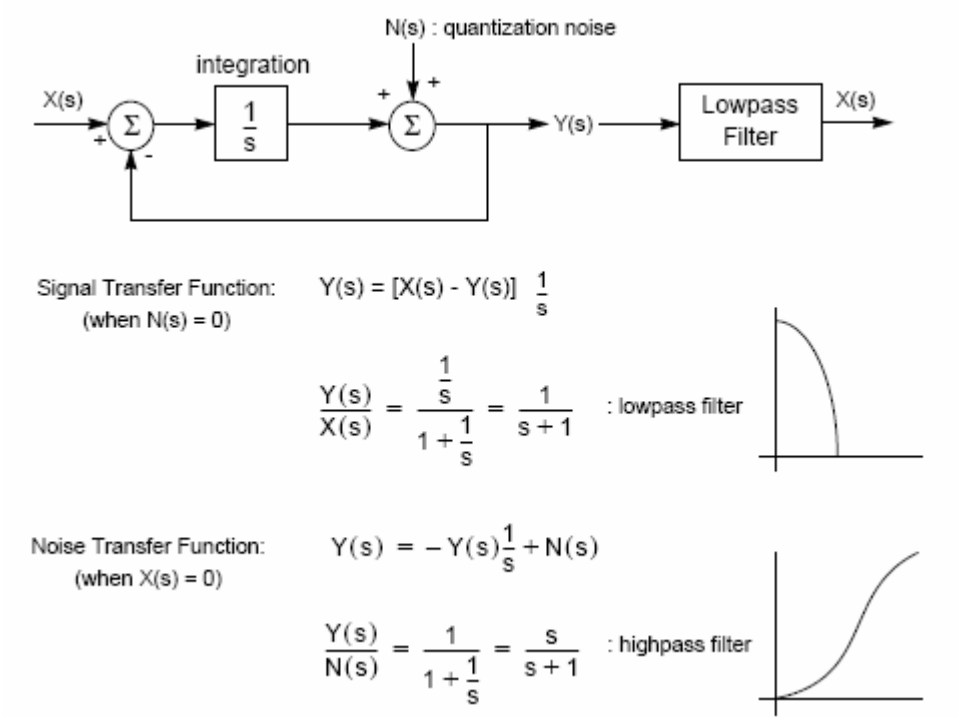

Figure 2.3. S-domain analysis of sigma delta modulator [9]

Simplified s-domain analysis of sigma delta modulator is shown in Figure 2.3 [9]. The difference between the input and sampled signal is integrated. The loop low pass filters the signal and high pass filters the noise. Input signal is unchanged unless its frequency content does not exceed cut-off frequency. On the other hand, noise is pushed into higher frequencies.

Since the signal is oversampled by sigma delta modulators, quantization noise is spread over a wide bandwidth. This leads to a sharp decrease of the noise density in the bandwidth of interest.

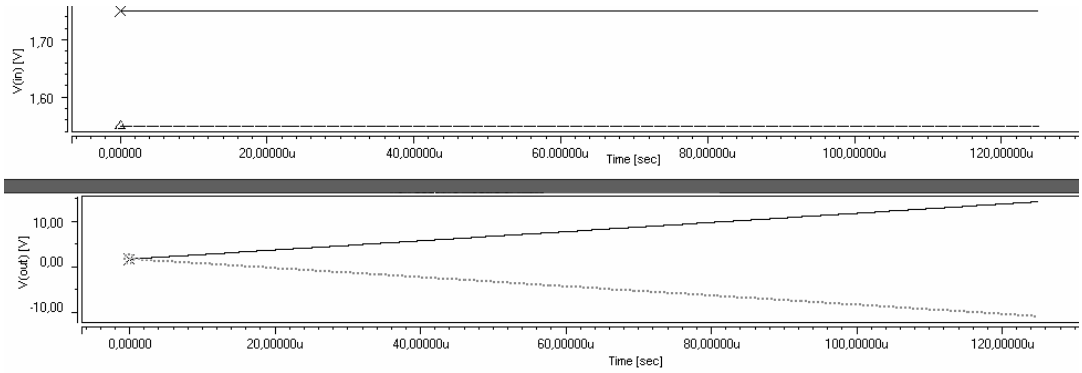

Figure 2.4. Ideal integrator DC analysis

In Figure 2.4, an ideal integrator is simulated. Differential input voltages and integrator output of the modulator is represented in the figure. Since the common-mode voltage is defined as 1.65 V DC for the integrator the differential inputs 1.75 V and 1.55 V DC are applied to test the integrator functionality. Integrator adds up the input DC voltage to the output every clock cycle.

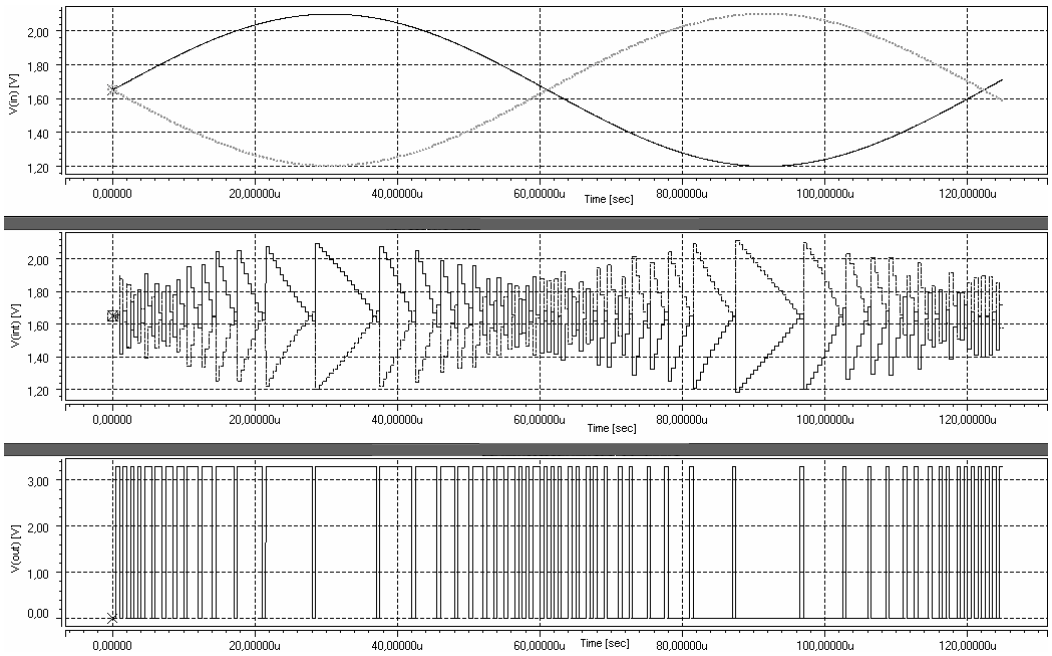

Figure 2.5. Ideal 1-bit modulator AC analysis

In Figure 2.5, AC input is applied to ideal single bit modulator and its integrator output and modulator output is represented.

Whenever input signal has a greater voltage value than the common-mode voltage, mostly ‘ones’ appear at the output. When the input has a lower value than the common-mode voltage, ’zeros’ appear more frequently. This behavior indicates that output is tracking down the input signal.

2.1. Quantization Noise

When analog to digital conversion takes place, analog input signal is mapped to predefined digital levels. Thus, quantization noise is dependent on the resolution of the converter. In Figure 2.6 quantization step Δ is shown [10].

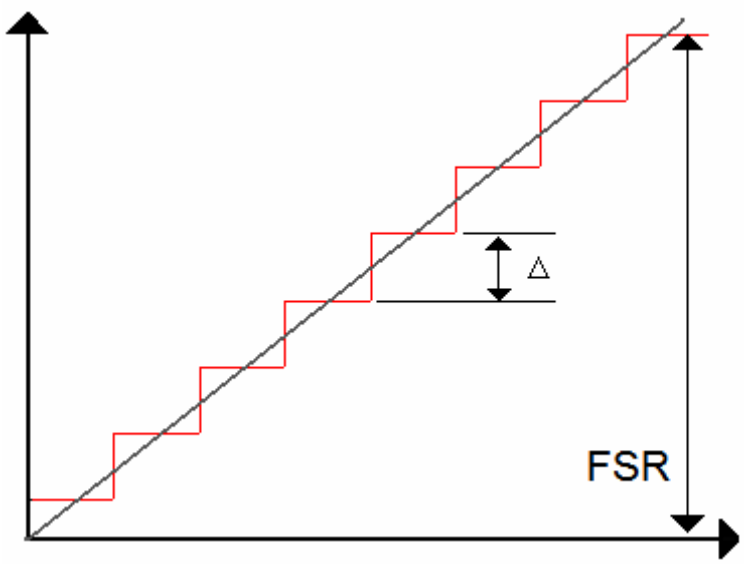

Figure 2.6. Uniform quantization [10]

Quantization step depends on the resolution of the modulator which is formulated in equation 2.1.

$$\Delta = \frac{FSR}{2^{N-1}} \tag{2.1}$$

In equation 2.1, FSR represents full scale range of the signal and N represents the number of bits of the modulator. The smaller the quantization step is, the smaller the quantization error will be that is introduced to the modulator. This dependency is shown in equation 2.2.

$$e_{rms} = \frac{\Delta}{\sqrt{12}} \tag{2.2}$$

For SNR calculation, input sine wave is also formulated depending on the quantization step size and number of bits of the modulator. Finally, SNR can be given as in equation 2.3.

$$(SNR)_{dB} = 6.02N + 1.76 \tag{2.3}$$

During these calculations, oversampling effect of sigma delta converters was not taken into account. Equation 2.3 is derived for conventional converters like Nyquist rate converters.

In this thesis, the focus will be on SD converters which include the oversampling effect on SNR performance. Thus, the derived quantization noise equation 2.3 will be recalculated with oversampling parameter OSR included.

2.2. Oversampling

Oversampling converters introduce the parameter OSR which defines the ratio of the sampling with respect to Nyquist frequency. The OSR is referenced in equation 2.4.

$$OSR = \frac{f_{sampling}}{2 f_{baseband}} = \frac{f_{sampling}}{f_{Nyquist}} \tag{2.4}$$

When oversampling is taken into account, noise power density is decreasing as a result of the widening spectrum. In Nyquist converters, quantization error was only dependent on the number of bits used, but in oversampling converters the error is also dependent on the OSR. The error could be derived using equation 2.5.

$$e^2_{rms} = \frac{\Delta^2}{12OSR} \tag{2.5}$$

It is obvious that when oversampling is applied to the modulator, quantization noise decreases in parallel with the widening spectrum. This decrease in quantization noise will have a positive effect on the SNR performance of the modulator. Since then, SNR calculation will include OSR parameter as referenced in equation 2.6.

$$(SNR)_{dB} = 6.02N + 1.76 + 3.01(OSR) \tag{2.6}$$

Since SNR has a major effect on modulator's performance oversampling is the major specification for sigma delta converters.

2.3. Noise Shaping

Noise shaping filters the noise at high frequencies and this operation helps to shape the noise out of the baseband.

In equation 2.7, transfer function of the modulator is derived.

$$Y(z) = S_{TF}.X(z) + N_{TF}.E(z) \tag{2.7}$$

E(z) represents the quantization error. STF and NTF represent the signal and noise transfer functions, respectively. Since the aim is to pass all the input signal and eliminate the quantization error from the baseband, the transfer function of the filter H(z) should be an all-pass filter for the input signal and a high-pass filter to the quantization noise.

To have a high SNR performance, STF should approach 'one' while NTF approaches 'zero'. The desired effect could be realized using an integrator which has the transfer function H(z) in equation 2.8.

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.8}$$

Regarding equation 2.8 for z=1 H(z) goes to infinity. Since the transfer function of the loop filter which will act as an integrator is H(z) the signal and noise transfer functions became as in the equations 2.9 and 2.10, respectively.

$$S_{TF} = z^{-1} \tag{2.9}$$

$$N_{TF} = 1 - z^{-1} \tag{2.10}$$

If we update the equation 2.7 with these calculations, the formula will become as in equation 2.11.

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \tag{2.11}$$

As expected, the modulator will behave as a low-pass filter to the input signal and as a high-pass filter to the quantization noise.

Modulators could also be categorized according to their orders. As the order of the modulator increases, noise shaping property gets higher. In Figure 2.7, different orders of modulator noise shaping property is shown [10].

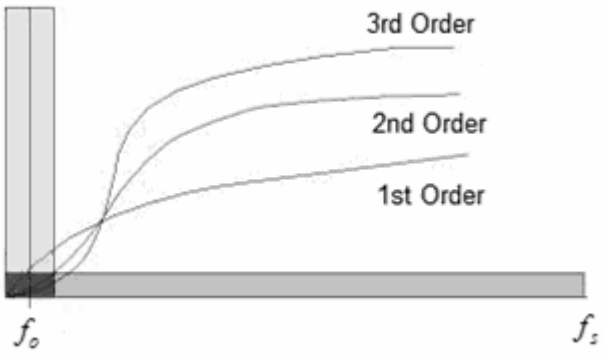

Figure 2.7. Noise shaping spectrum for different order of modulators [10]

3. PROBLEM STATEMENT

In this chapter, problem statement will be indicated and its drawbacks will be explained. The effect of the stated problem will be built up with simulation results.

While designing sigma delta modulators, the critical part is the integrator block, because it is the analog part of the circuit and introduces the saturation effect to the modulator. The integrator is implemented as a switched capacitor circuit which accumulates the input signal to the output in every clock cycle. In Figure 3.1, there is an example of a simple integrator circuitry.

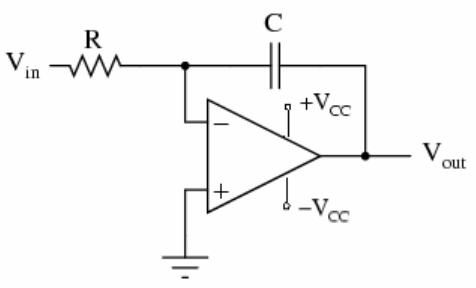

Figure 3.1. Simple integrator circuit

As a first step of behavioral design, opamp is configured ideally. While defining opamp, its small signal equivalent is used as a model. It is represented in Figure 3.2.

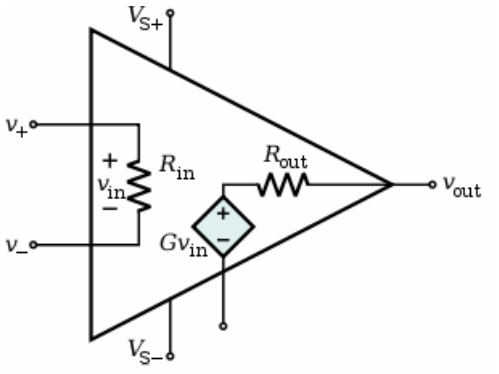

Figure 3.2. Small signal equivalent of OPAMP [25]

As a verification test, DC signal is applied to the input and confirmed that opamp sums up the input signal to the output every clock cycle. The simulation results are

represented in Chapter 3 in Figure 3.2. The SPICE netlist for the ideally designed opamp is in Appendix A.1.

When a DC signal is applied through the input of the integrator, it will sum up the input voltage of every cycle to the output. SPICE analysis is carried out to analyze the behavior of the ideal integrator. In Figure 3.2, the input and output of the integrator is shown.

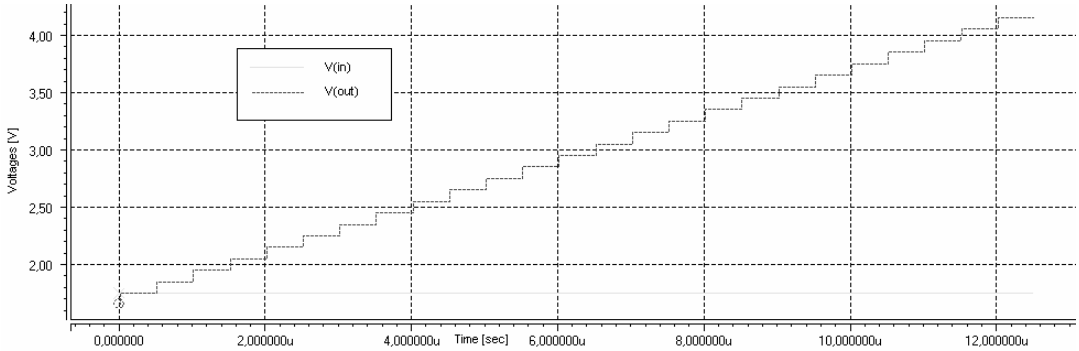

Figure 3.2. Ideal integrator behavior when input is DC

To simulate a non-ideal saturated integrator, an additional clipping circuit is included in the behavioral design of the opamp.

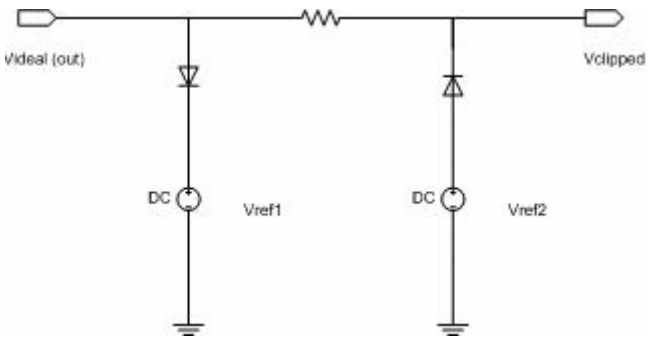

Figure 3.3. Additional Clipped circuit

The additional circuit is added at the end of the integrator to simulate the saturation effect. As shown in Figure 3.3, that output is limited with diodes according to the given reference voltages.

In Figure 3.4, the same DC input in Figure 3.2 is applied through the integrator and the output is represented.

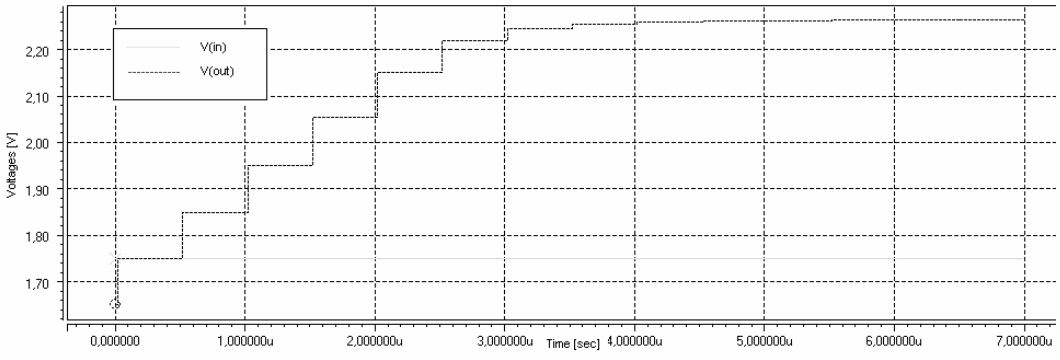

Figure 3.4. Saturated integrator behavior when input is DC

When we enable the ideal DACs at the feedback path and apply AC input signal through the modulator, the output of the integrator block for ideal and non-ideal modulators will be like in Figure 3.5 and Figure 3.6, respectively.

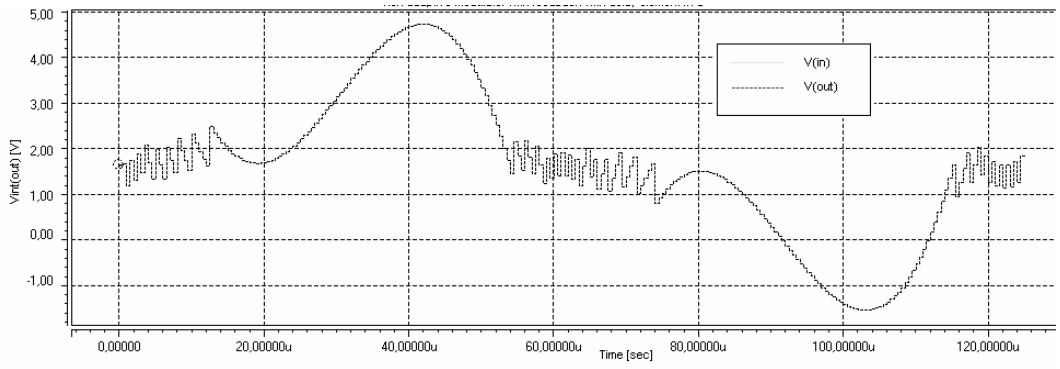

Figure 3.5. Ideal integrator output with feedback and AC input

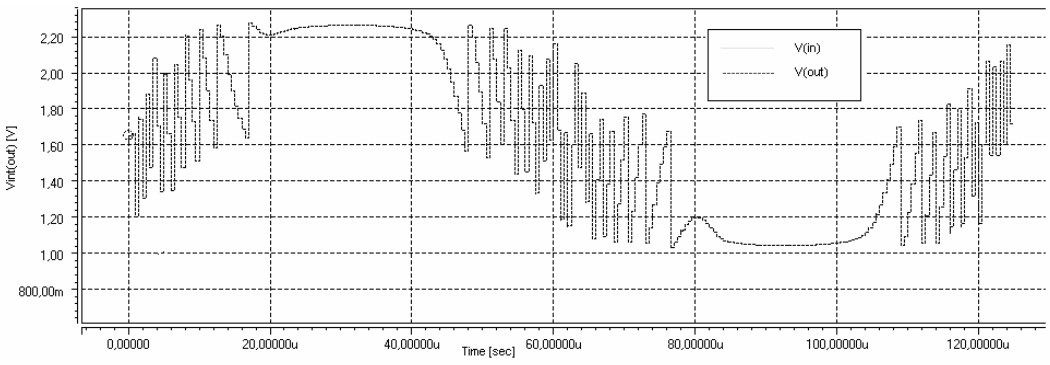

Figure 3.6. Saturated integrator output with feedback and AC input

Since for the non-ideal case the integrator output is going into saturation, the digital levels at the output will be inaccurate. Thus, the conversion output will be manipulated. Also, for the non-ideal case, the output data will not follow the analog input signal properly which depends on the severity of the saturation. This will have a degradation effect on the SNR performance over the dynamic input range of the modulator.

In the literature, several different solutions are proposed to overcome the saturation effect of the integrator in SD modulators.

One of them is based on usage of feed-forward signals and an extra quantizer which will lead up to 85% reduction of integrator swing [11]. This architecture also has a degradation effect for the harmonic distortion based on the opamp non-linearity.

Another approach to overcome the clipping of the integrator output is based on an adaptive adjustment for the feedback coefficient at the input node via an overload detector and the design effectively bounds the integrator outputs and extends the unclipping input level to full scale. [12] This leads into a significant increase in the maximum allowable input range. Moreover, the unclipped dynamic range is extended and makes the quantization noise less dependent on the input signals.

An alternative research is made for clipping integrator output which is based on using a mixed mode integrator circuit. In this method, an overload estimator (OLE) monitors both the input and output of the integrator in order to decide whether the integrator output will be saturated or not. [13] If the integrator output is expected to exceed the reference voltage and go into saturation region, a feedback signal double the size of the reference voltage is safely subtracted from the integrator input in order to make sure that integrator output stays in the unsaturated region. This approach needs adjustments in the feedback coefficients and introduces a mismatch between analog and digital paths which could diminish the advantage of mixed-mode integrators. On the other hand, with this solution it is possible to have a better dynamic range up to 12 dB.

All the approaches are based on detecting the bounds and scaling the factors for coefficients to avoid the clipping effect of the integrator. The limiting issue with these

approaches is that the solutions are proposed within initial conditions or a restricted input ranges. The criteria of stability and wide spectrum should be applicable for the provided solution.

The proposal made in this thesis is to construct a detection mechanism at the output of the integrator that will sense if the integrator output is getting close to the saturation region or not. Then, if saturation region is close, the additional circuitry will help adjust the integrator gain accordingly.

Serving this purpose, the gain of the integrator output should be adjusted. The integrator gain is tunable by its capacitances. The gain revision will be triggered with an additional logic circuitry at the output of the integrator which will sense it when the integrator will go into saturation in advance and then it will enable the extra capacitance to be introduced to the circuit. This extra capacitance will reduce the gain, so will be the step size of the integrator output accumulation. At the output, the data should be processed and filtered in such an appropriate way that the digital output bit stream will be reasonable. The quantizer and DAC will be designed with a non-uniform structure to serve the need.

4. ADAPTIVE AND NON-ADAPTIVE SYSTEM ARCHITECTURES

In this Chapter, adaptive and non-adaptive system analyses are done in behavioral level. Serving this aim, behavioral elements of the basic single-bit SD modulator is designed and tested one by one. Saturation effect is discussed for single and multi-bit modulators. Then, multi-bit modulator simulations are done to measure the SNR and resolution performance.

4.1. Non-Adaptive System Analysis

First, non-adaptive sigma delta modulators are analyzed to understand the need of the adaptive architecture. In Figure 4.1, a non-adaptive differential sigma delta modulator structure is represented [10].

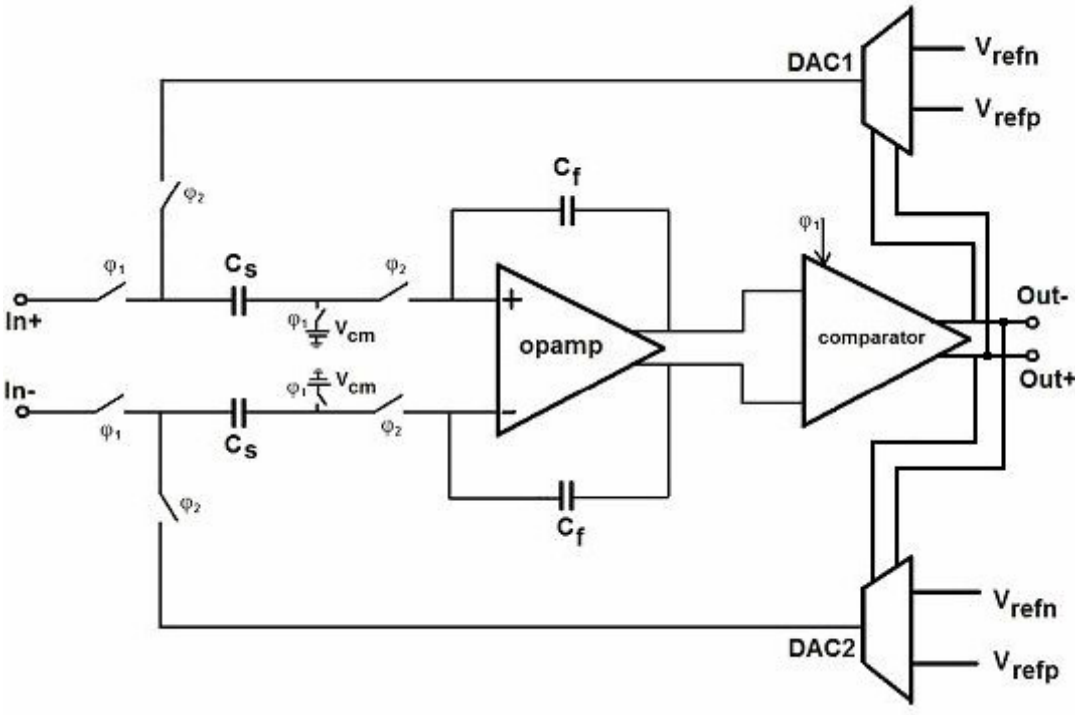

Figure 4.1. Differential sigma delta modulator block diagram

In SD modulators, the critical part is the integrator block which is realized as a switched-capacitor integrator in this thesis. The opamp used inside the switched capacitor structure has limitations for its output due to saturation levels of the opamp.

Other blocks which compose a 1st order SD modulator consist of a quantizer and digital-to-analog converters. The number of levels of the quantizer defines the resolution specification of the modulator. Digital-to-analog converter blocks are also adjusted according to the level of quantization. The digital output of the quantizer is bonded to the digital-to-analog converters. The DACs map this digital input to a proper voltage level at the output and feed it back to the input of the modulator. By this way, the DACs at the feedback path corrects the input according to the output to have a better performance.

The SPICE netlist of the sigma delta modulator in Figure 4.1 including non-ideal opamp is listed in Appendix A.3.

The input signal frequency is chosen 8 kHz while oversampling frequency is 2 Mhz. Eventually, OSR for the designed modulator is 125.

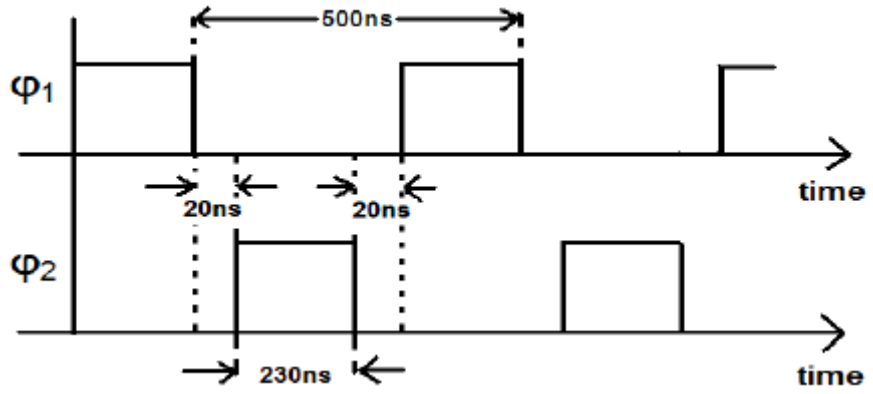

Figure 4.2. Non-overlaping clock signals

In Figure 4.2, the sampling frequency of the clock signals are shown. They are applied as non-overlapping signals to avoid inaccurate oversampling.

To understand the non-adaptive architecture, transient analyses are carried out in the behavioral level. As a first step, all SD modulator blocks are designed behaviorally and tested one by one.

In Figure 4.3, the transient analysis outputs for ideal 1-bit behaviorally modeled modulator is represented.

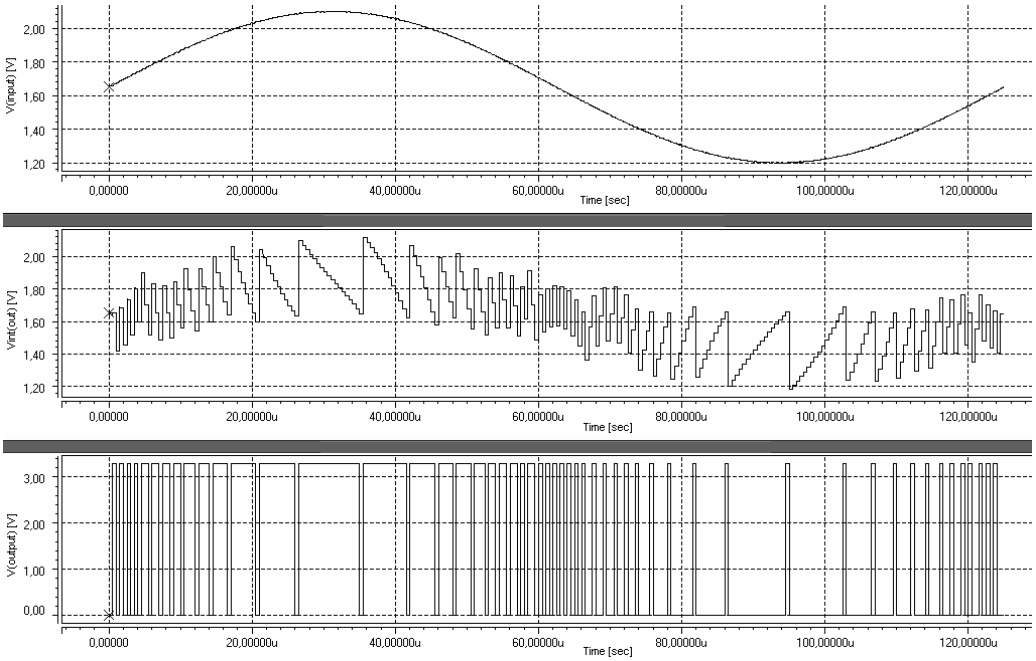

Figure 4.3. Ideal behavioral 1-bit modulator transient analyses

Integrator output follows the input in Figure 4.3. Whenever the input is close to the common-mode voltage 1.65 V DC, the frequency of the toggling at the output increases. When the input is above common-mode voltage, ‘ones’ are seen at the output mostly and when below ‘zeros’ are seen mostly. The SPICE netlist for this simulation is in Appendix A.3.

When the modulator is simulated with ideal sinusoids at the input, the SNR curve gets unexpected spikes as in Figure 4.4.

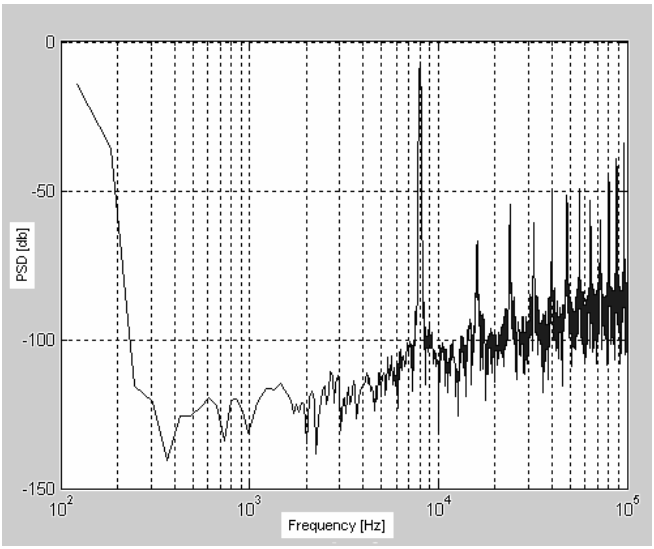

Figure 4.4. PSD plot of modulator without dither

To overcome the unwanted jumps in FFT analysis, several sinusoids with small magnitudes at different frequencies are added up to the input signal. The result is shown in Figure 4.5.

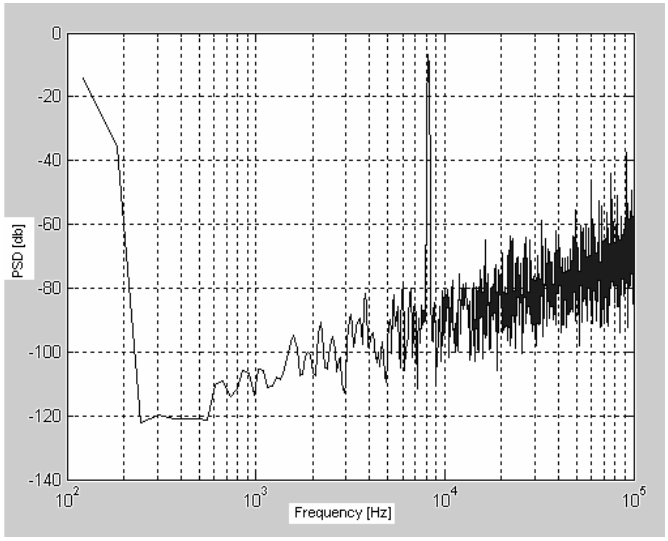

Figure 4.5. PSD plot of modulator with dither

Single-bit modulators are the most robust architectures against the saturation effect. Since there are two digital levels which consist of ‘zeros’ and ‘ones’, the signal which is above the common-mode voltage will be denoted as ‘one’; and which is lower than the common-voltage will be denoted as ‘zero’. So, even if the saturation levels are limiting the signal going through the quantizer the upper and lower bounds of the digital data will not

change, it will be ‘zero’ or ‘one’. Below is a presentation of the logic and saturation levels for a single-bit modulator in Figure 4.6 [10].

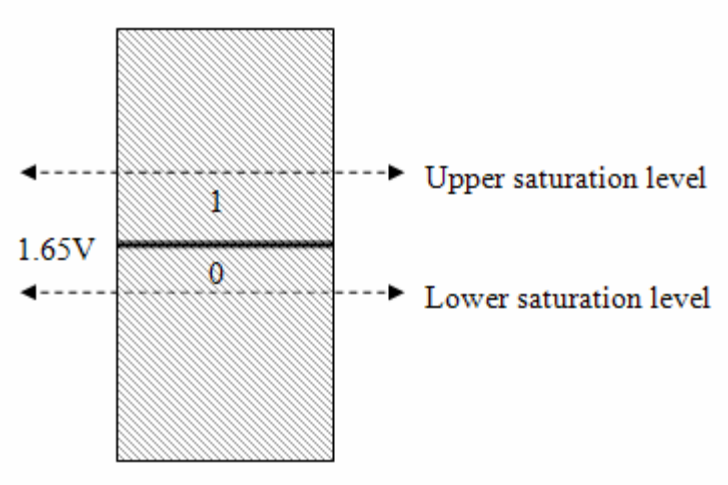

Figure 4.6. Saturation effect on single-bit modulator [10]

In Figure 4.7, 2-bit modulator quantization levels and saturation levels are represented [10].

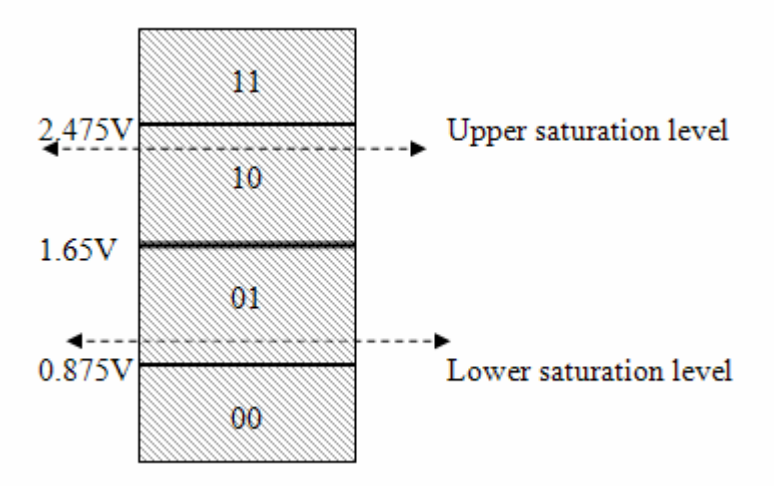

Figure 4.7. Saturation effect on 2-bit modulator [10]

As can be seen in Figure 4.7, when the saturation effect is introduced, the digital output could not go to the levels ‘11’ and ‘00’. This limitation will lead to a loss in digital data accuracy and end up in a degradation of the SNR performance of the modulator.

Transient analyses are done as an ideal 2-bit behavioral modeled SD modulator. In Figure 4.8, results are shown.

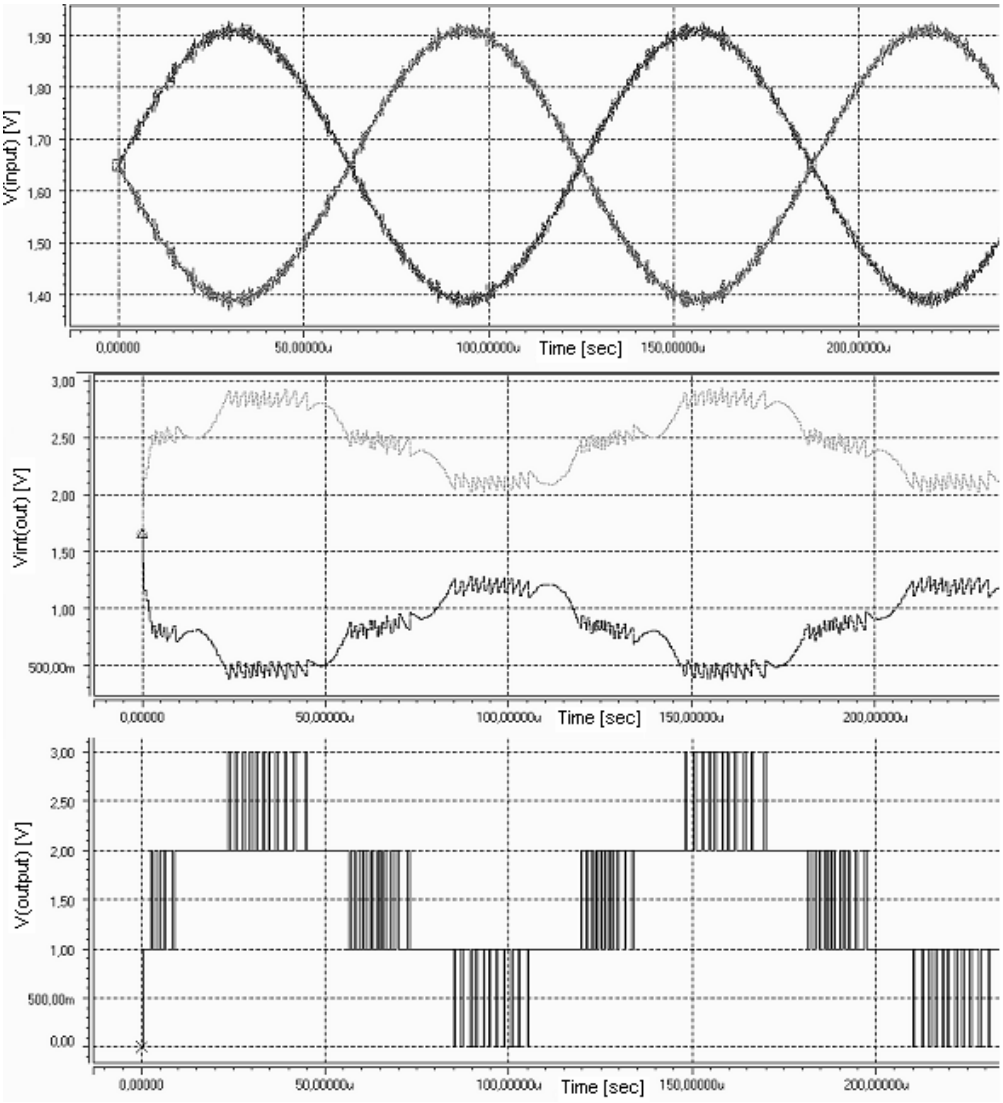

Figure 4.8. Ideal 2-bit behavioral modulator transient analyses

For the given input in Figure 4.8, digital output oscillates between 0~3, so all four states are monitored at the output. The same input is applied to 2-bit saturated non-adaptive architecture as the transient analysis is represented in Figure 4.9.

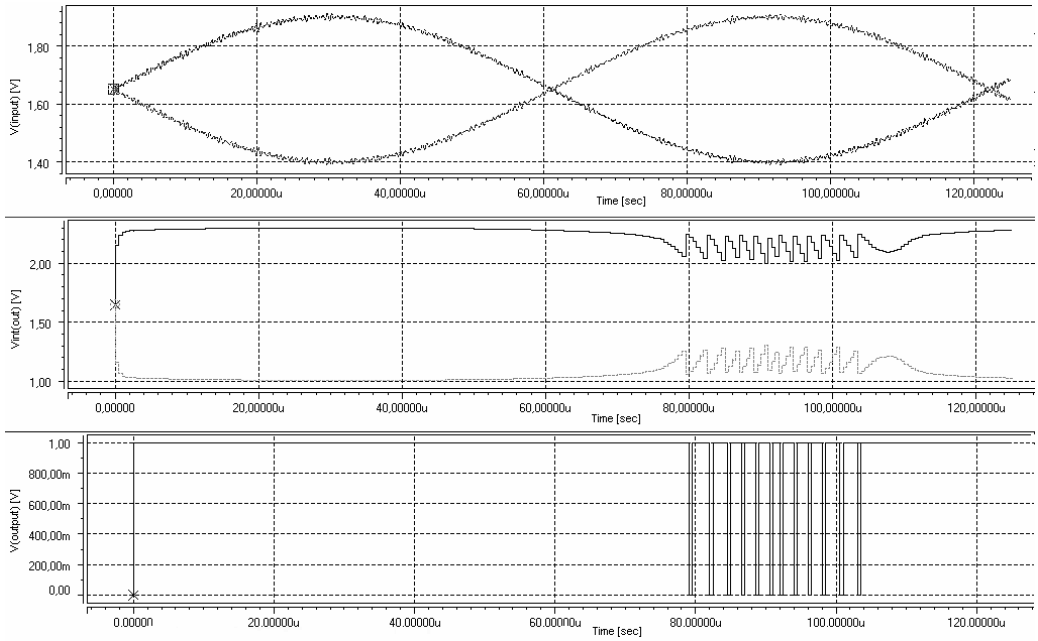

Figure 4.9. Non-Adaptive Saturated 2-bit behavioral modulator transient analysis

In the ideal case, the digital output oscillates between 0~3, but when saturation is introduced, the oscillation is only present between 0~1. It is quite clear from the ideal and saturated modulator simulation results that clipping affects the accuracy of the modulator output. This leads to corrupted digital data at the output, so the resolution decreases.

The SNR performances of the ideal and saturated architectures are measured for the same given input. The PSD plots of these simulations are represented in Figure 4.10 and 4.11.

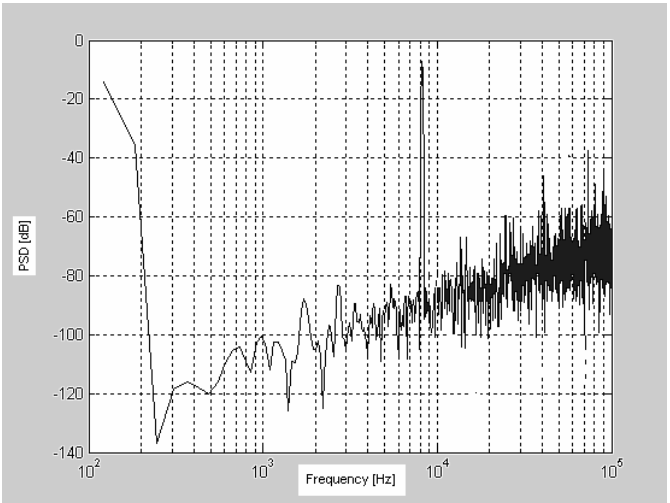

Figure 4.10. Ideal 2-bit modulator PSD plot

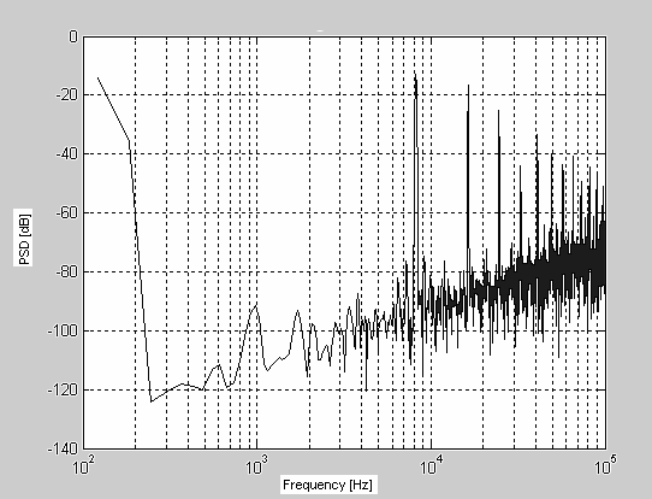

Figure 4.11. Saturated 2-bit modulator PSD plot

As could be depicted from Figure 4.10 and 4.11, the saturation has a serious effect on SNR performance in the baseband, because as the saturation limits the output, the signal converges to square wave signal which has a bad SNR figure in the baseband.

The behavioral design is extended to 4-bit modulation. First transient analyses are carried out for ideal and saturated cases. Results are shown in Figure 4.12.

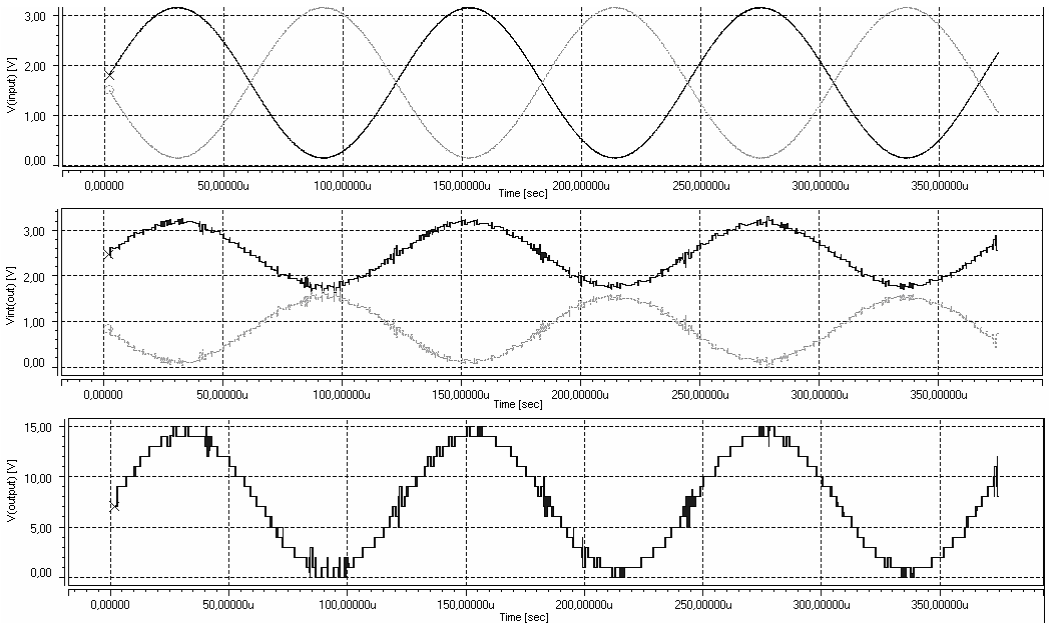

Figure 4.12. Ideal 4-bit modulator transient analysis

When saturation is introduced to the modulator, the digital output is manipulated as represented in Figure 4.13.

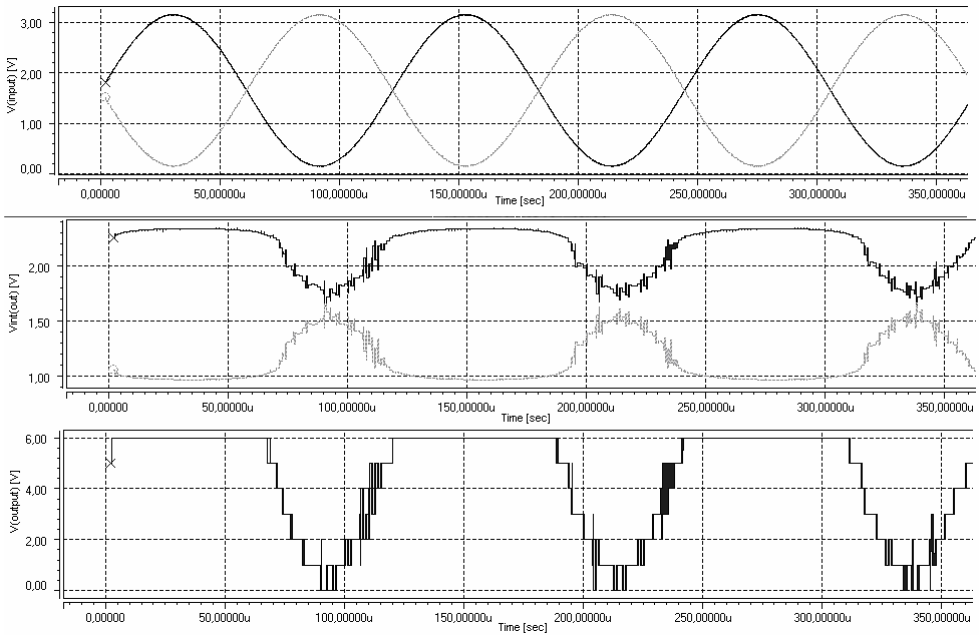

Figure 4.13. Saturated 4-bit modulator transient analysis

In the ideal case, the output changes between 0~15 whereas it changes between 0~6 for the saturated case. This degradation leads to inaccuracy at the digital output data and to a decrease in the resolution of the modulator.

SNR analyses are performed for ideal and saturated 4-bit behaviorally modeled modulators with the same given input; and results are represented in Figure 4.14 and 4.15.

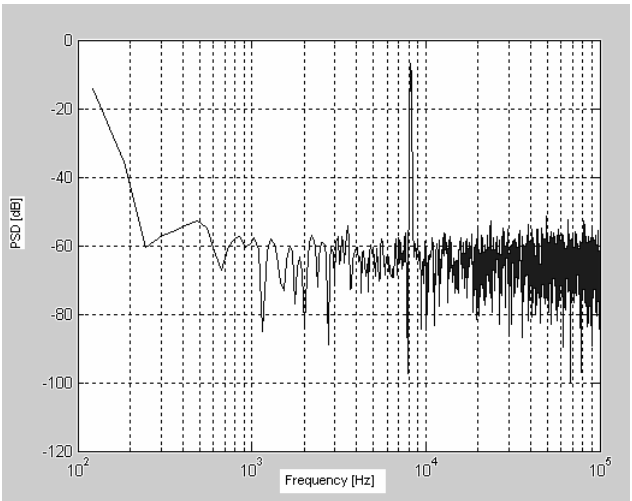

Figure 4.14. Ideal 4-bit modulator PSD plot

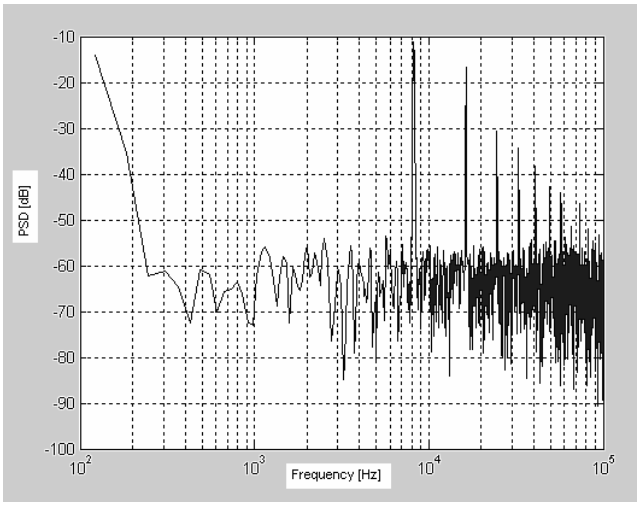

Figure 4.15. Saturated 4-bit modulator PSD plot

Saturated 4-bit behaviorally modeled modulator has a dramatic decrease in the SNR performance analysis. A lot of high spikes in the baseband are observed which result in a poor SNR performance.

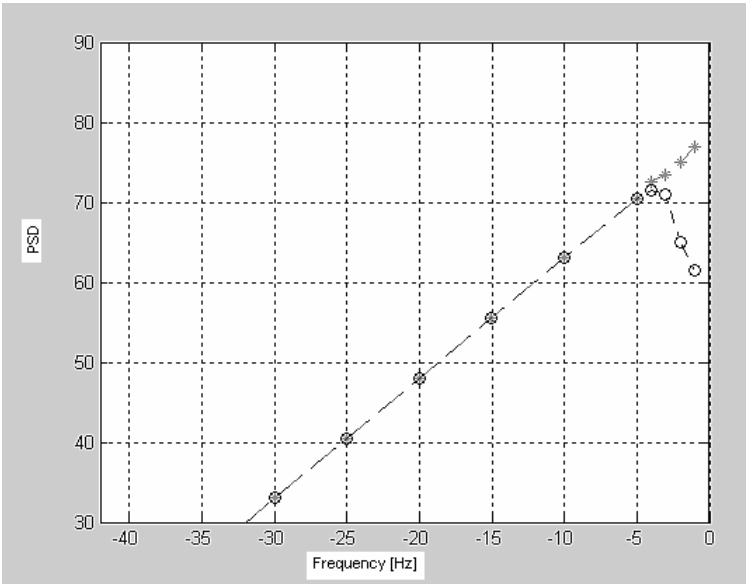

Figure 4.16. Behavioral 4-bit modulator SNR performance comparison

In Figure 4.16, behavioral element modulator analysis of the SNR performance with respect to input dynamic range is studied. For the ideal case, SNR value is increasing in parallel to the applied input signal amplitude. But for saturated case after a level of input

signal amplitude SNR performance decreases dramatically which is the side effect of the clipping.

The aim of the adaptive design is to eliminate the drawbacks of the saturated structure and improve the resolution, so is the SNR performance of the modulator.

4.2. Adaptive System Analysis

In Figure 4.17, the proposed architecture as a solution to the saturation effect is represented [10].

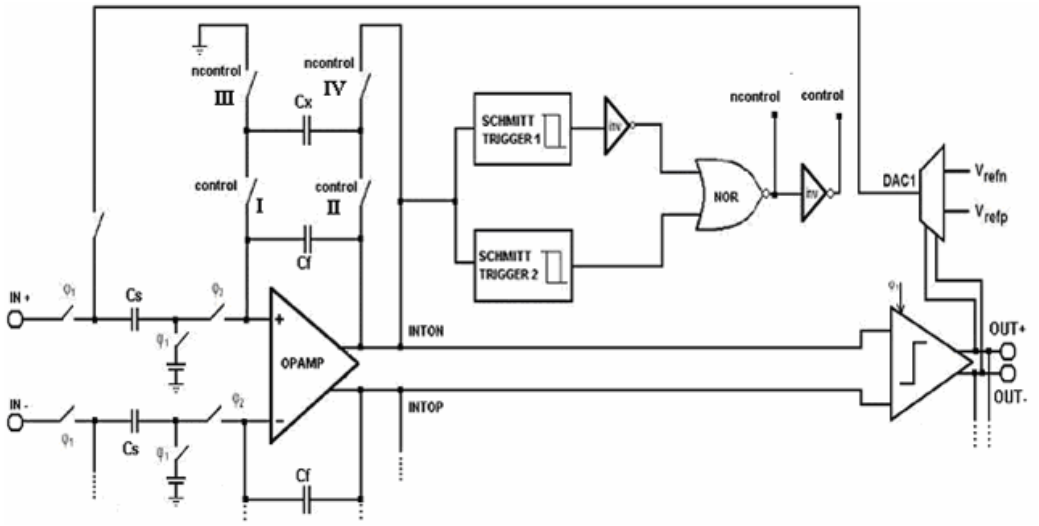

Figure 4.17. Adaptive System Block Diagram

In the proposed adaptive structure, an additional logic circuitry is inserted into the modulator. The gain of the integrator is adjusted by an extra capacitance which this additional logic circuitry activates whenever integrator output gets close to the saturation level. A safe margin is defined by the reference voltage levels of the Schmitt triggers inside the logic circuitry. Inside this safe margin, the extra capacitance Cx is disconnected from the feedback of the integrator. Outside the safe margin, an extra capacitance is added to the feedback path of the integrator and result in a decrease at the gain of the integrator which could be calculated with equation 4.1 below.

$$\frac{Out(z)}{In(z)} = \frac{C_s}{C_f} \times \frac{z^{-1}}{1 - z^{-1}} \tag{4.1}$$

In Figure 4.7, integrator output for an open loop analysis of adaptive modulator is represented.

The logic circuit that triggers the extra capacitance consists of Schmitt triggers and logic gates. When the integrator works in the unsaturated region, logic circuit will disconnect the extra capacitance by opening the switches I and II decreasing the gain of the integrator; and when the edge of the saturation of these switches close, switches III and IV will be opened. The logic control circuit is represented in Figure 4.18.

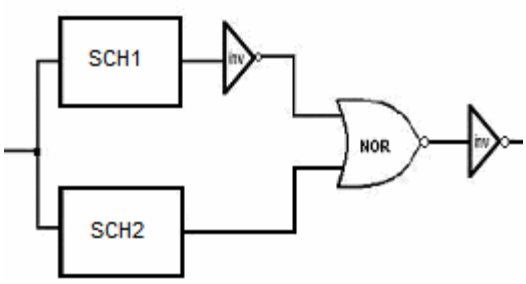

Figure 4.18. Logic control circuit [10]

While designing the logic control circuit, reference levels of the Schmitt Triggers should be defined according to the saturation levels. The leveling of the Schmitt triggers are shown in Figure 4.19. When the edge of the saturation is sensed by the logic control circuits, necessary signals are sent to the control switches.

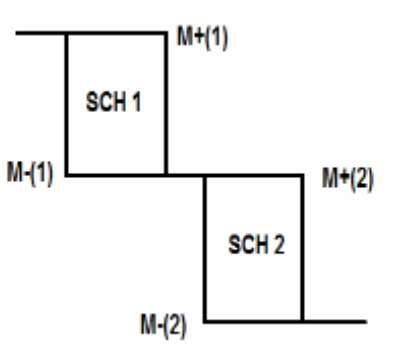

Figure 4.19. Schmitt Trigger levels

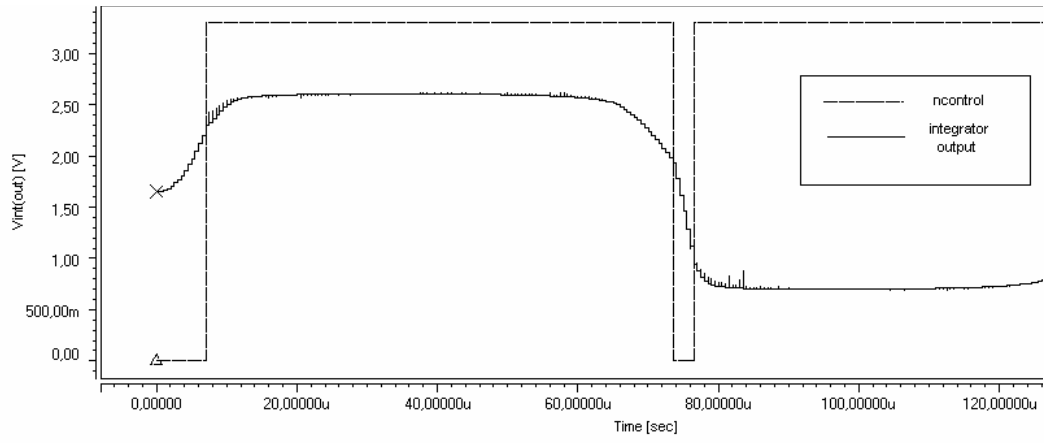

Figure 4.20. Adaptive modulator integrator output without feedback

From Figure 4.20, it can be derived that when the control signal is on, the gain of the integrator is smaller. And when the control signal is off, the integrator sums up with bigger steps.

For the proposed adaptive structure, as a first step, the integrator output is manipulated with the additional logic circuitry according to the saturation levels of the integrator. To make this change meaningful, quantizer levels of the ADC should be adjusted accordingly.

In Figure 4.21 and Figure 4.22, there are the representations for the outputs of uniform and non-uniform ADC which are applied to the adaptive structure.

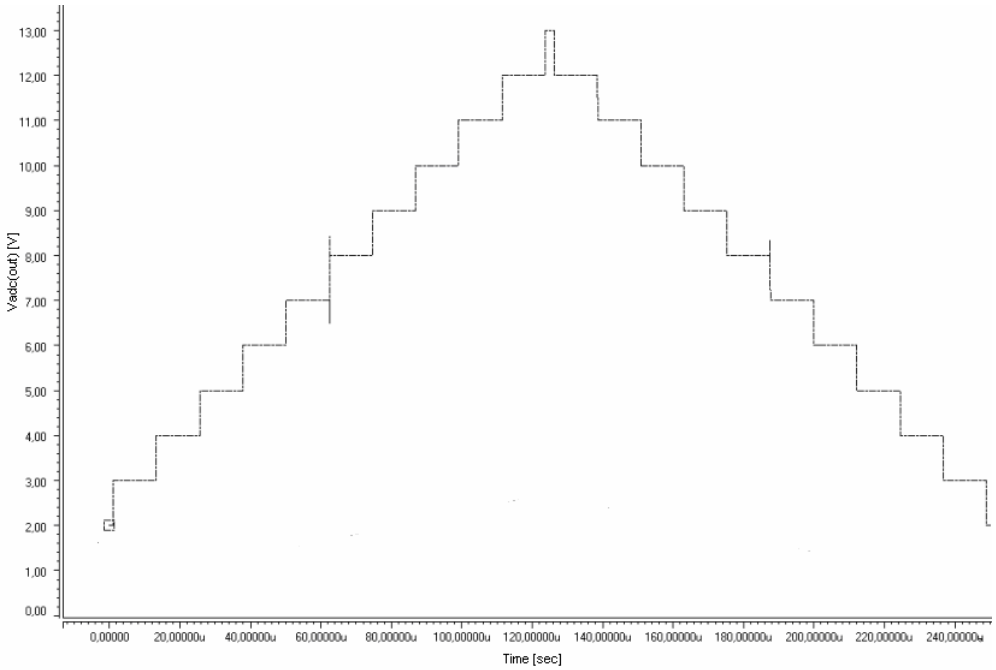

Figure 4.21. Uniform ADC output with adaptive structure

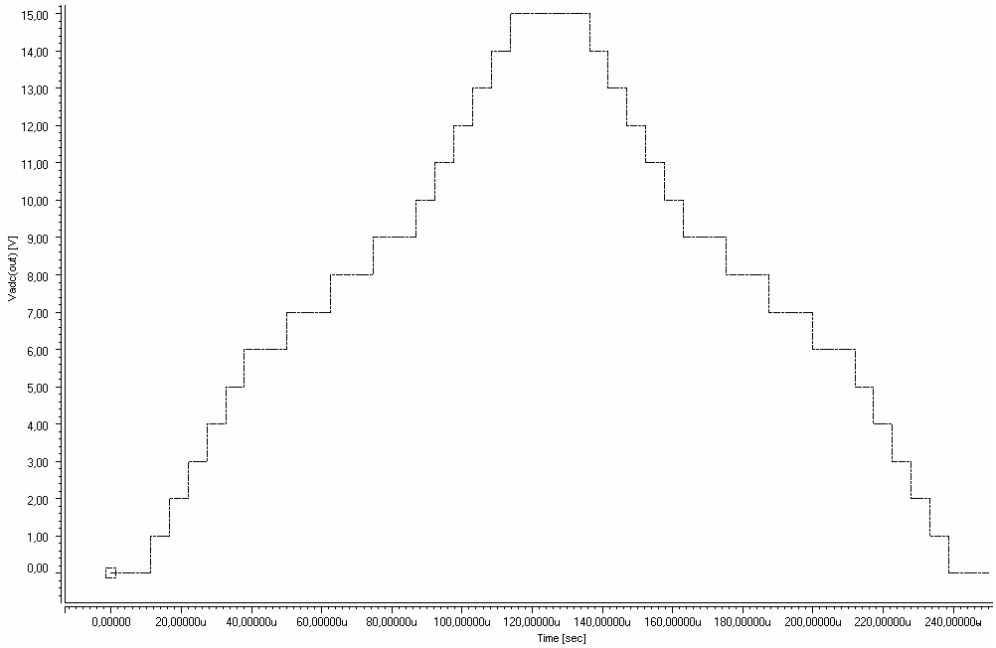

Figure 4.22. Non-uniform ADC output with adaptive structure

The same inputs are applied for Figure 4.21 and 4.22. From the non-uniform distribution, it can be easily seen that ADC output has a range between 0~15 while we have the range of 2~13 when we applied the same input to the uniform ADC. It is obvious that non-uniform quantization allows us to have a wider digital range which results in higher resolution.

Transient analyses are done to see the difference in the performance of the adaptive and non-adaptive modulators.

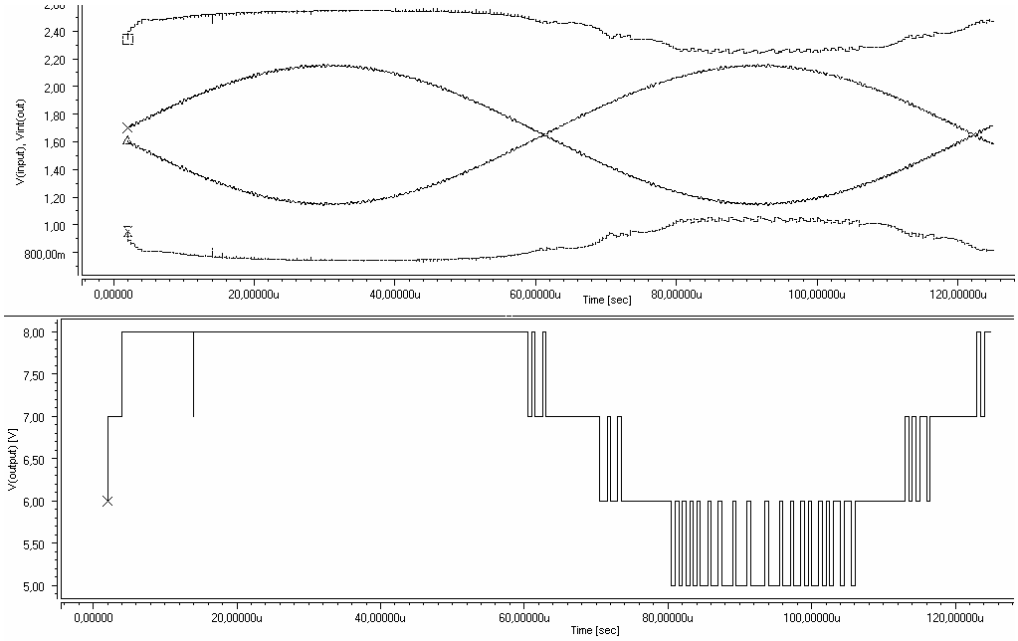

Figure 4.23. Non-adaptive behavioral modulator transient analysis

The digital output of the non-adaptive modulator is presented in Figure 4.23. The output oscillates between 5~8 for the given input. If we increase the applied input magnitude even more, the output digital data will be converging to square like waveform. Thus, the modulator will have degradation in its SNR performance.

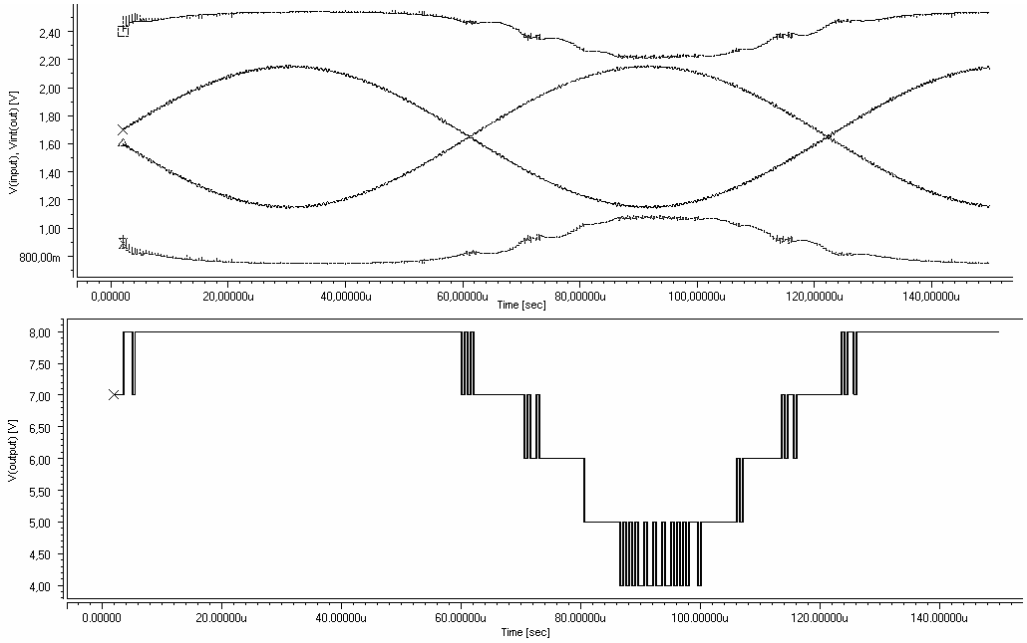

Figure 4.24. Adaptive behavioral modulator transient analysis

In Figure 4.24, the same input signal is applied but for the adaptive structure the output oscillates between 4~8. Thus, adaptive architecture has a better resolution. Also the adaptive model has a more ‘sinusoidal like’ output which will lead to better SNR performance.

In Figure 4.25, the SNR characteristics for ideal, saturated and adaptive structures with respect to input signal range are represented. All analyses are performed with behavioral models.

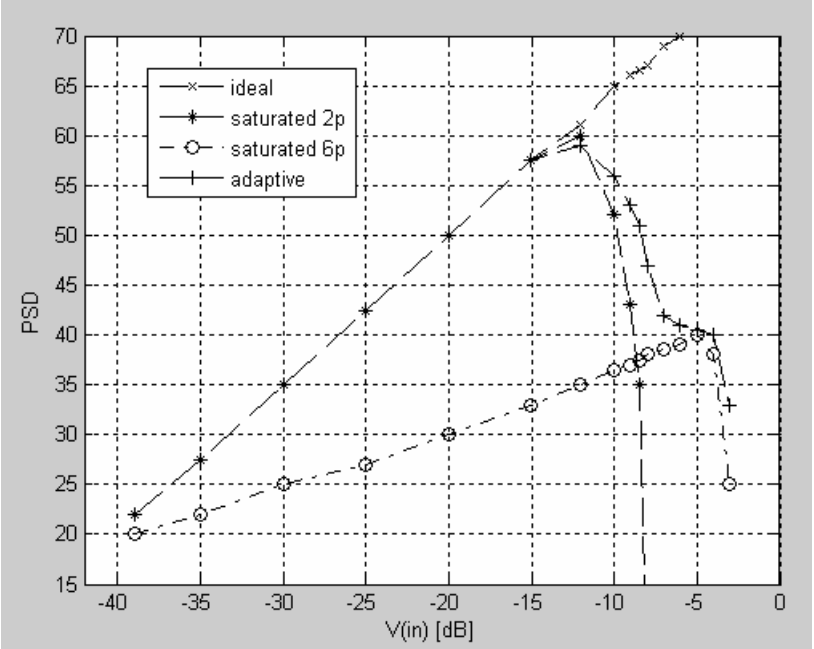

Figure 4.25. SNR performances of behavioral models

The ideal curve represents the ideally modeled modulator. The SNR analysis results with respect to applied input range. Since all components are ideally modeled, the SNR performance is linear and not limited.

The saturated 2 pF and 6 pF curves represent the clipped modeled modulator performances which are simulated with 2 pF and 6 pF capacitances at the integrator feedback path. As it can be predicted, the analysis curve which is done with 6 pF at the feedback path has a lower SNR performance.

The adaptive curve represents the proposed adaptive structure performance with respect to the applied input signal range. As it can be verified from the graph, this curve follows the curve of a saturated modulator curve with 2 pF; and when saturation is available, it gets close to the saturation modulator analysis done with 6 pF capacitance.

For adaptive modulator, when the integrator output gets close to the saturation level, it functions with the integrator which has a three times smaller gain. By this way, as it can be seen from the comparison graph, it is possible to better the dynamic range with respect to SNR by the usage of the proposed architecture.

5. TRANSISTOR LEVEL DESIGN

In this chapter, all blocks which have been modeled at behavioral level for the initial analysis are designed in the transistor level. The goal is to replace all behavioral blocks with the elements in the transistor level and re-analyze the modulator to have a more realistic idea of the performance for the proposed adaptive structure.

5.1. Opamp Design

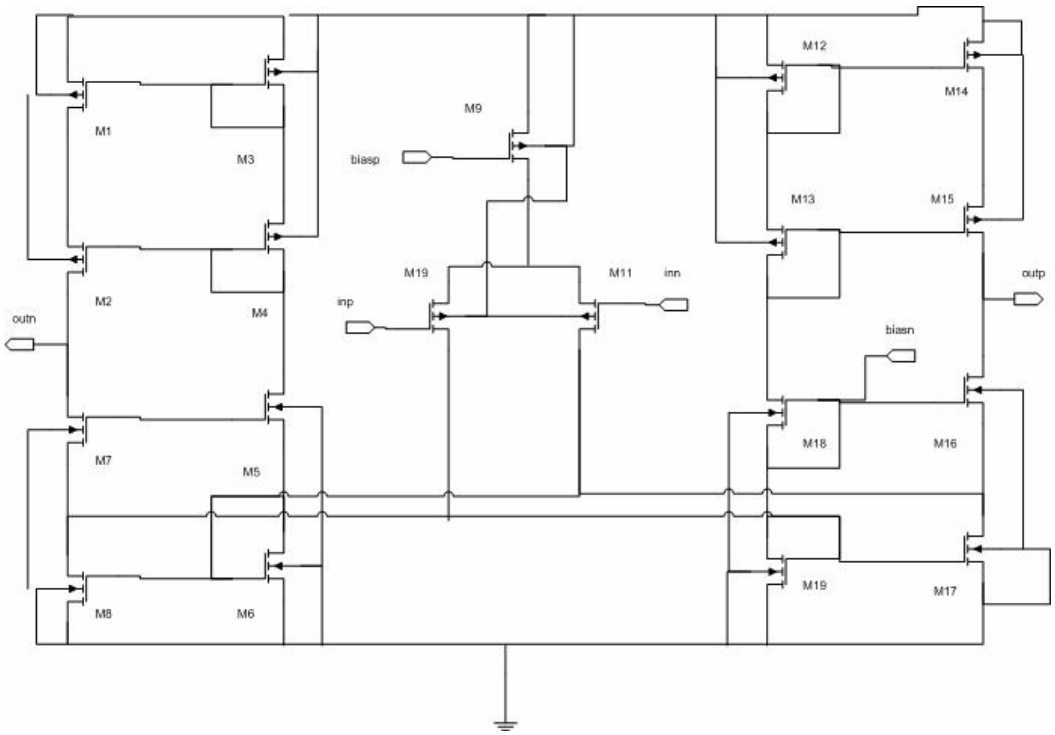

Figure 5.1. Differential Folded Cascode Opamp Schematic

Folded cascade topology is selected among various types of opamp structures regarding its simplicity and stability. AMS 0.35um technology is used for the transistor level implementation. Transistor level opamp is designed in differential form.

In Figure 5.1, the transistors M10 and M11 represent the differential input pair. M9 is the transistor which supplies the bias voltage and rails the differential input. M5, M7, M16,

and M18 are the cascade pairs for positive and negative counterparts. M1, M2, M3, M4, M12, M13, M14 and M15 are the current mirrors. And finally, M6, M8, M17 and M19 are the transistors which supply the bias voltage through the cascode pairs.

The specifications of this opamp with a load capacitance 4 pF are as follows: Gain = 75.5 dB, BW = 200 MHz, cut-off frequency = 53 kHz, SR = 181.3 V/us. The opamp has a 1.65 V offset voltage. The saturation levels for the designed opamp are 0.7 V and 2.6 V.

5.2. Switch Design

While designing switch at the transistor level, transmission gate structure is chosen with respect to its ability to eliminate the undesirable threshold voltage effects, which is the case for logic. For pass-transistor logic, NMOS transistor passes a strong ‘zero’ but a weak ‘one’ ,and for PMOS it is vice versa. By using the transistor-gate logic, we avoid weak ‘zero’ and ‘ones’.

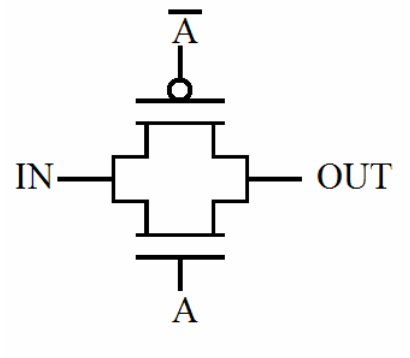

Figure 5.2. Transmission-gate switch

In Figure 5.3, the performance of the switch with clock frequency 2 Mhz is represented. When the switch is on, the output catches up the input; and when the switch is off, it does not function.

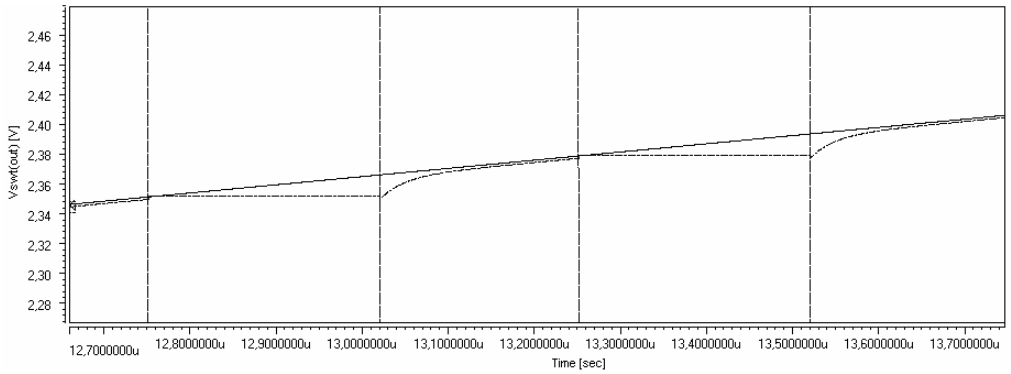

Figure 5.3. Switch performance analysis

5.3. Uniform and Non-Uniform Quantizer Design

5.3.1. Single-bit Quantizer Design

Initially, a single-bit quantizer is designed. The basic comparator design is shown below in Figure 5.4.

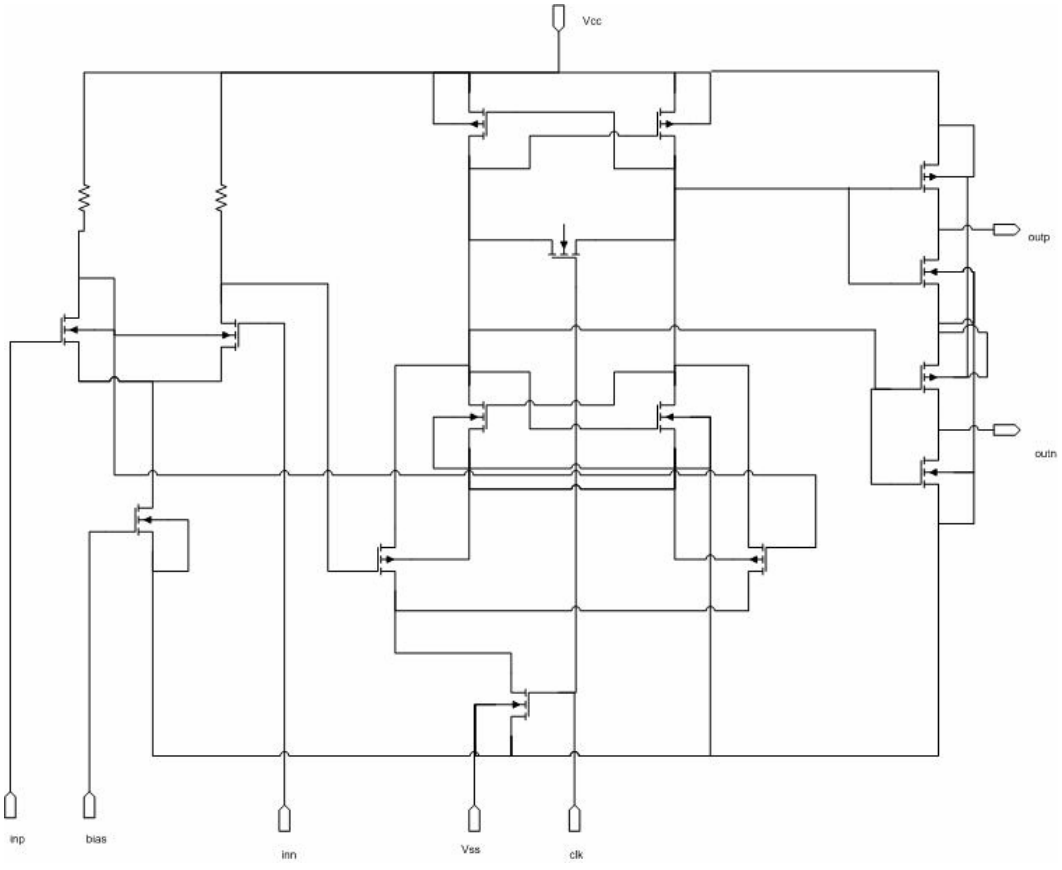

Figure 5.4. Single-bit quantizer schematic

Comparator needs 0.75 V DC biasing voltage. The comparator is designed differentially and clocked with the sampling frequency. When the clock is high, the circuit compares the input with the applied reference voltage and generates the outputs 0 V or 3.3 V DC voltages accordingly. When the clock is low, the comparator does not function.

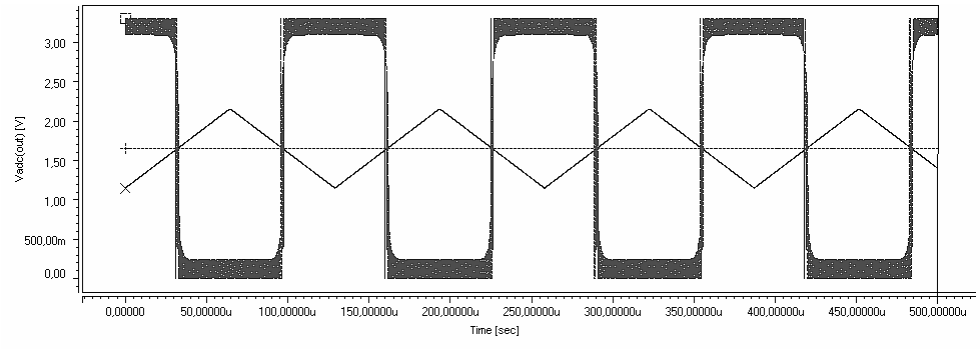

Figure 5.5. Single-bit quantizer analysis

In Figure 5.5, transient analysis result graph for single-bit comparator is represented. A ramp input is applied with frequency of 8 kHz. The clock frequency is set to 2 MHz which is the sampling frequency for the modulator. Reference voltage is 1.65 V DC. The comparator gives ‘1’ for the values above the reference voltage and gives ‘0’ for the values below. With this analysis, comparator functionality is verified.

5.3.2. 4-bit Quantizer Design

At this step, 4-bit quantizer is designed using single-bit comparators. Mainly, the reference voltages for 4-bit quantizer are adjusted with voltage division and these reference voltages are fed to single bit comparators.

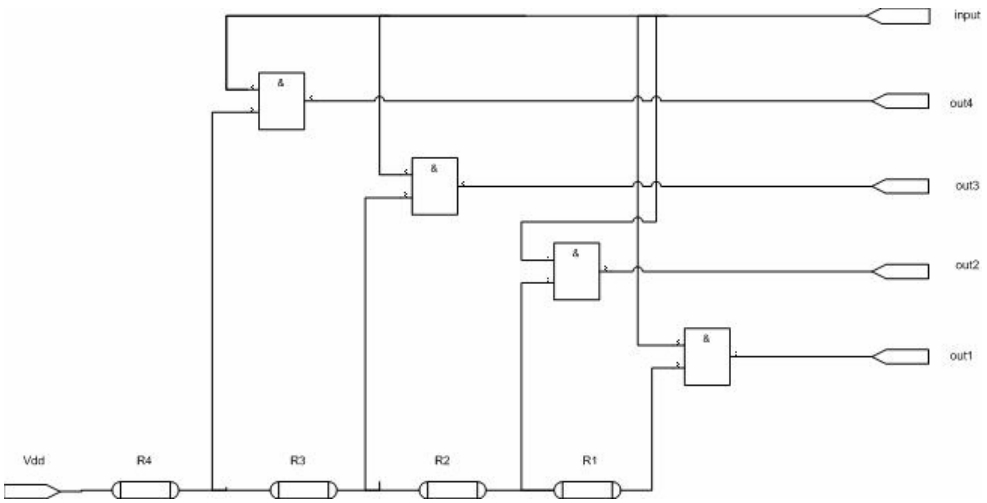

Figure 5.6. 2-bit Quantizer Schematic

In Figure 5.6, a block diagram of 2-bit quantizer structure is illustrated. The input signal is compared to reference voltages which are adjusted with resistors and gives the digital data to the output.

For 4-bit quantizer design, the same topology structure is used and transient analysis for this design is represented in Figure 5.7.

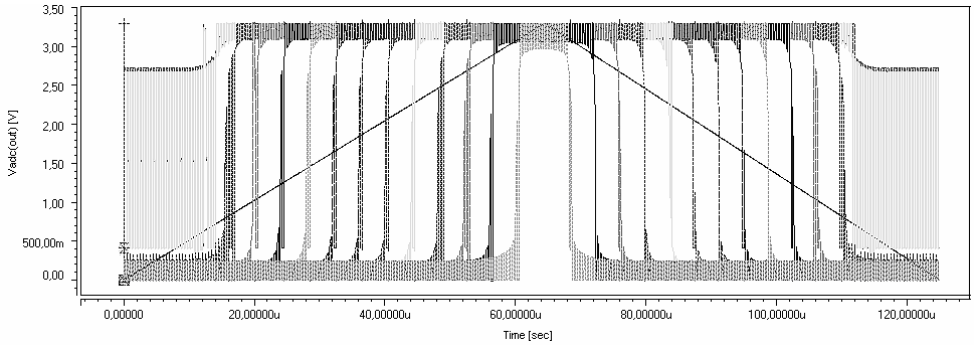

Figure 5.7. Uniform 4-bit Quantizer Analysis

As can be detected from Figure 5.7, the output of the three comparators which have the lowest three reference levels do not giving give the expected results which only take the values 0 and 3.3. This is because the reference voltages for these three are lower than the NMOS transistor threshold voltage. Since the designed opamp low saturation level does not allow these voltage levels, this inaccuracy will have no effect on our analysis.

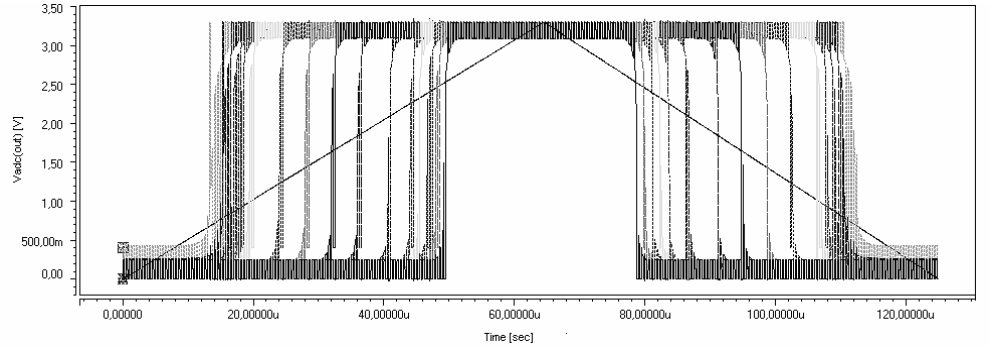

Figure 5.8. Non-uniform Uniform 4-bit Quantizer Analysis

In Figure 5.8, non-uniform 4-bit quantizer transient analysis curves are illustrated. A ramp waveform is applied to the input. The reference voltages for the non-uniform structure are adjusted to the integrator output levels. When the integrator output gets close to the saturation levels, the difference between the reference voltages becomes smaller. The only physical difference between uniform and non-uniform structure is the used reference resistors for voltage division.

5.4. Uniform and Non-Uniform DAC Design

The last step is the DAC design which is located on the feedback path of the modulator.

The quantizer outputs will be the inputs for the DAC. In DAC design, the outputs of the quantizer are fed to the transistor gate voltages which generate an amount of current depending on the formula in 5.1.

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad (5.1)$$

The idea is to tune the transistors' W and L's to get the appropriate amount of current and convert it to the voltages which will be the DAC reference voltage levels. In Figure 5.9, the schematic of the proposed DAC design is represented.

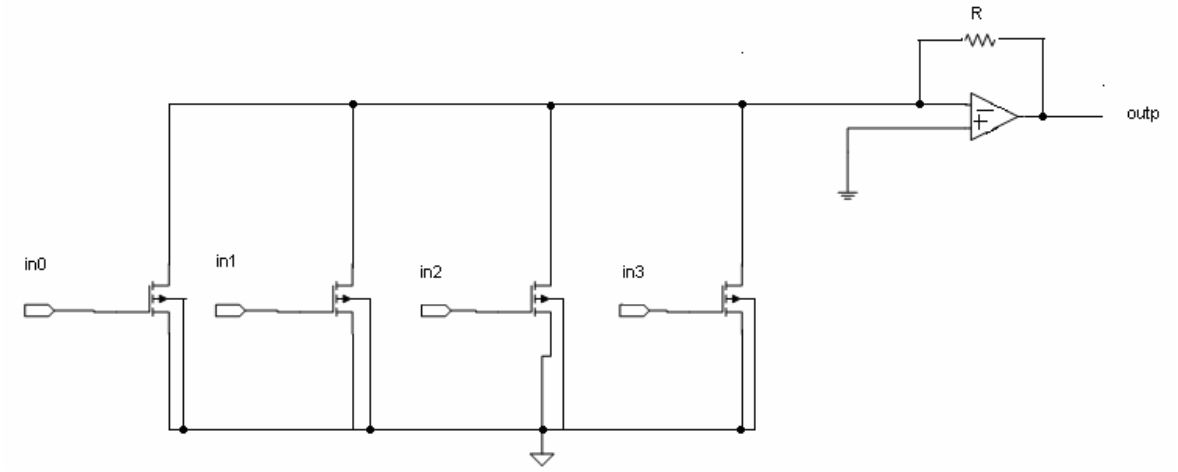

Figure 5.9. DAC design schematic

Uniform 4-bit DAC structure is designed with 15 transistors in parallel which composes the DAC reference output voltages. For the uniform structure, the current flow is uniformly distributed.

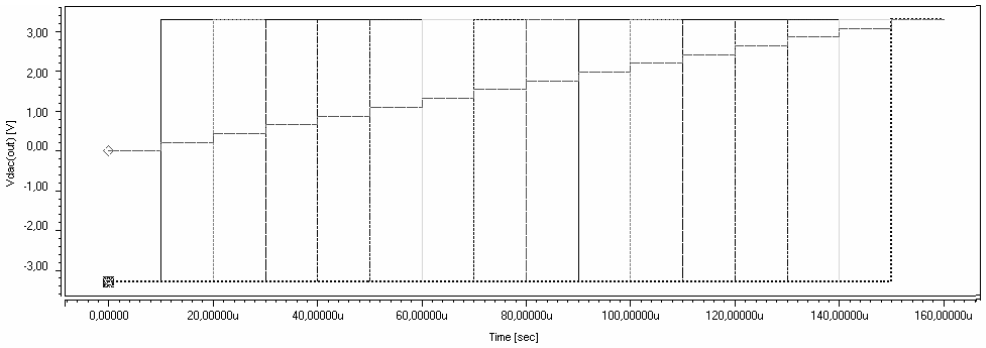

Figure 5.10. Uniform 4-bit DAC Analysis

For composing non-uniform DAC, width and lengths of the transistors are adjusted to match the non-uniform reference voltages. In Figure 5.11, non-uniform 4-bit DAC transient analysis is illustrated.

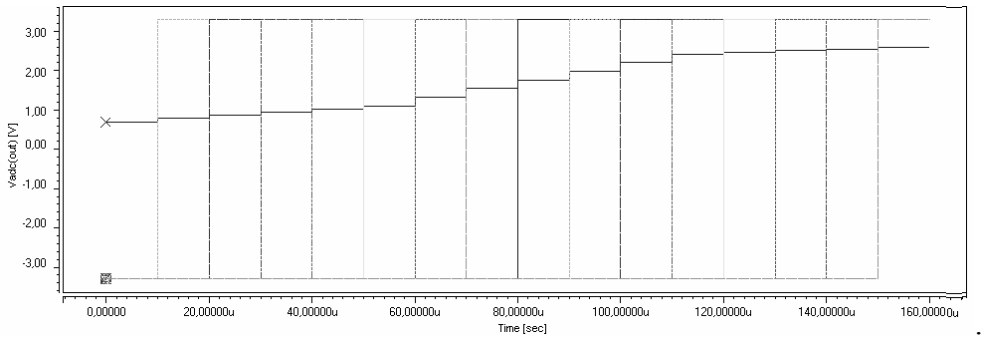

Figure 5.11. Non- Uniform 4-bit DAC Analysis

5.4.1. Uniform and Non-Uniform ADC/DAC Comparison

After concluding with the designs of the transistor level ADC and DAC, comparison analyses are performed.

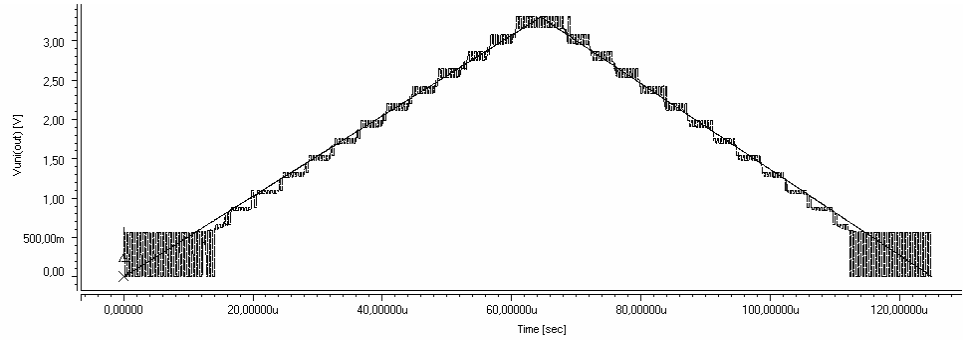

Figure 5.12. Uniform ADC-DAC Analyses

Reference to Figure 5.12, a ramp input is applied to the input of the uniform 4-bit ADC and its output is fed to uniform 4-bit DAC and output follow the input as it is expected to be. The levels below 600 mV are not properly mapped to a reference voltage, the cause for that is already described in Chapter 5.3.2.

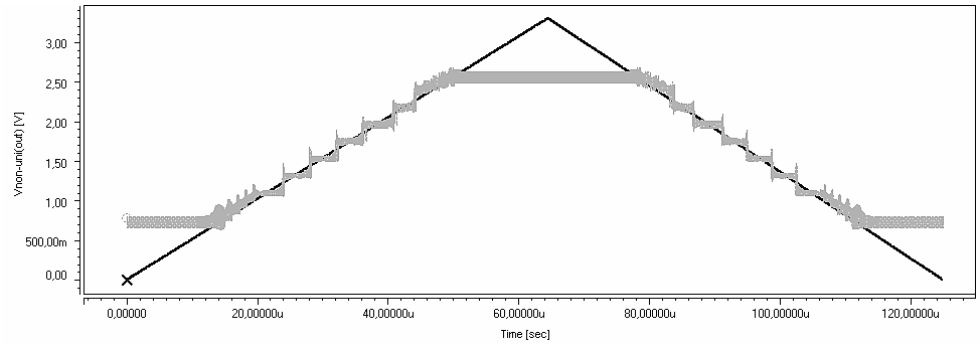

Figure 5.13. Non- Uniform ADC-DAC Analyses

In Figure 5.13, the non-uniform ADC and DAC transient analysis output is represented. Since the levels of ADC and DAC are non-uniformly distributed, the reference voltage levels change more frequently when integrator output approaches saturation level 0.7 V and 2.6 V DC.

6. TRANSISTOR LEVEL PERFORMANCE ANALYSES

The analysis using ideal behavioral models are performed for initial analysis. Then, transistor level models are designed and tested individually. For non-adaptive structure analysis, uniform quantizer and DAC are used. And for adaptive architecture analysis, non-uniform quantizer and DAC are used including the additional logic circuitry.

First, the functionality of the overall modulator is tested with transistor level elements and is verified with transient analysis. In Figure 6.1 and 6.2, there are illustrations of the transient analysis integrator and digital output of a non-uniform modulator which is designed in transistor level.

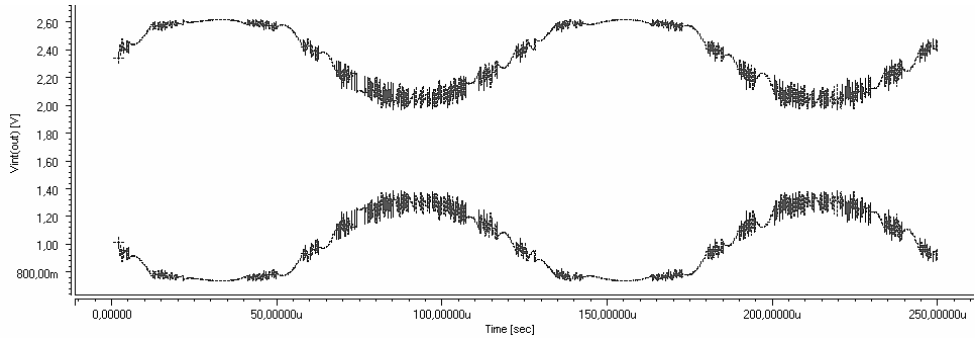

Figure 6.1. Non-uniform 4-bit modulator integrator output

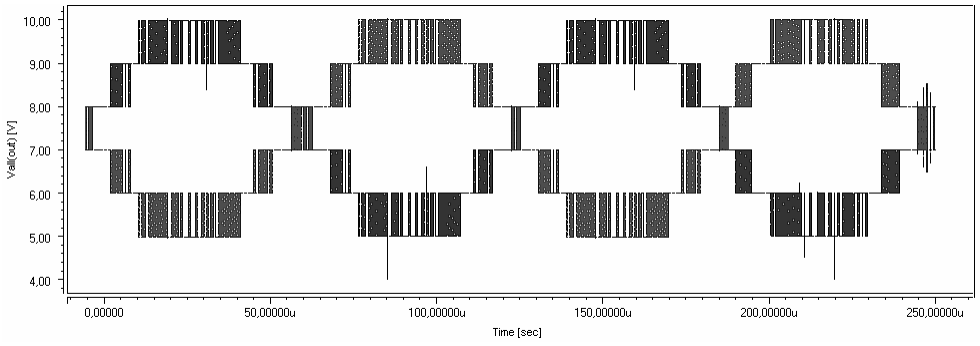

Figure 6.2. Non-uniform 4-bit modulator integrator output

In Figure 6.3, the graph on the left represents the SNR performance for a given input which belongs to the behaviorally modeled modulator whereas the graph on the right illustrates the SNR performance of the modulator designed in the transistor level.

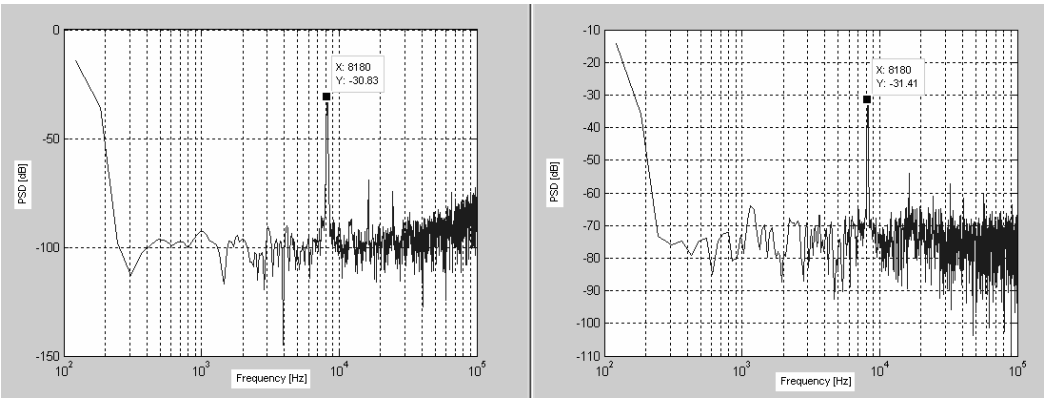

Figure 6.3. SNR comparison for behavioral and transistor level

FFT analyses of the modulator are performed for both behavioral and transistor levels. As can be followed from Figure 6.3, the input signal PSD value is more or less the same, but the noise floor is around 18 dB higher for transistor level simulation. This degradation is expected since modeling transistors and other equipment at transistor level will introduce the noise effect to the modulator.

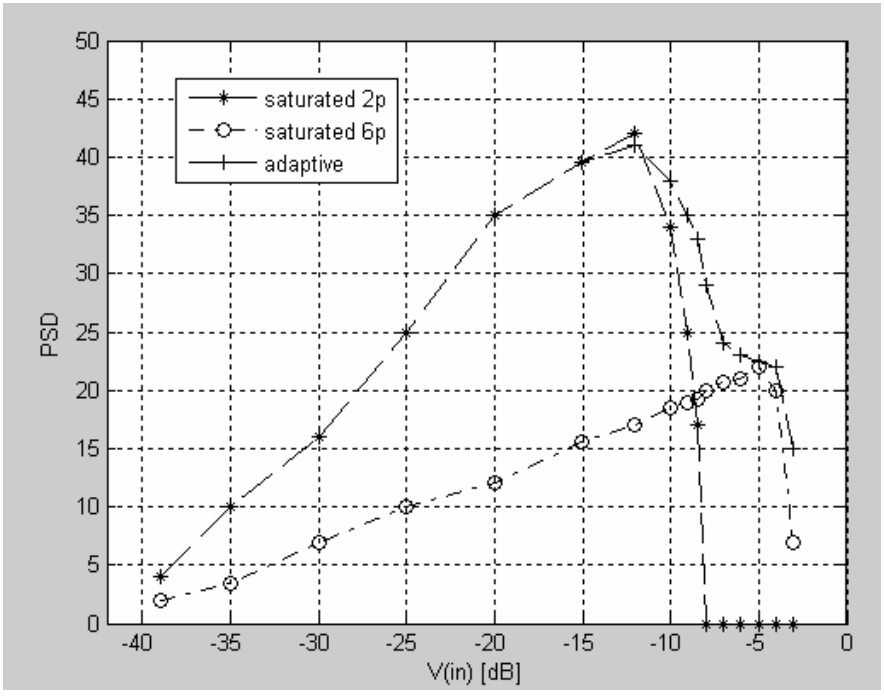

Figure 6.4. Transistor level SNR performance

With this SNR analysis, it has been shown that adaptive system architecture allows a wider input dynamic range so it has a better SNR performance than non-adaptive structure. Thus, the resolution of the adaptive structure is higher.

7. CONCLUSION AND FUTURE WORK

7.1. Conclusion

When proposed adaptive modulator design is applied, the gain of the integrator decreases. Through the edge of saturation levels, the clipping effect is avoided. This design has a healing effect on the SNR performance with respect to the dynamic input range.

Since the sampling frequency is chosen, 2 MHz and baseband frequency 8 kHz, the applied OSR is 125. The BW of the designed opamp is around 100 kHz.

It is observed that after locating the transistor level components, there is a remarkable decrease in the SNR performance of the modulator, which is around 15~18 dB. This degradation is due to the included transistor logic.

Conclusively, the proposed variable gain structure senses the saturation on the edge of saturation and decreases the gain of the integrator by the help of an additional digital circuitry, which will result in the non-stopping conversion with the real time integrator gain adjustment. Also, the proposed architecture optimizes the non-clipping input to the full-scale range.

7.2. Future Work

In this research, we focused on the performance of first order SD modulators. This should be spread to higher order modulators and their performances should be evaluated and compared accordingly.

In this study, all components are modeled in both behavioral and transistor levels. Although we have good results for the proposed adaptive structure, the modulators should be simulated in the layout level to see the real life effect of the adaptive structure, and examine if it is feasible to implement it.

APPENDIX A: SPICE NETLISTS

A.1. Behavioral level ideal opamp subcircuit definition

```
.subckt idealopamp inp inn outp1 outn1 cm
eopm1 outp cm inp inn 5k
eopm2 cm outn inp inn 5k
rin1 inp cm 100meg
rin2 inn cm 100meg
rout1 outp outp1 10
rout2 outn outn1 10
.ends
```

A.2. Behavioral level saturated opamp subcircuit definition

```
.subckt idealopamp inp inn outn3 outp3 cm
eopm1 outp cm inp inn 10k
eopm2 cm outn inp inn 10k
rin1 inp cm 100meg
rin2 inn cm 100meg
rout1 outp outp1 10
rout2 outn outn1 10

****Clipping Part**********
d1 outp1 m1 dmod
v1 m1 0 1.45
d2 outn1 n1 dmod
v2 n1 0 1.45
r1 outp1 outp2 3
r2 outn1 outn2 3
r3 outp2 outp3 3
```

```
r4 outn2 outn3 3
d3 m2 outp2 dmod
v3 m2 0 1.85
d4 n2 outn2 dmod
v4 n2 0 1.85
.model dmod d
*****************
.ends
```

A.3. Spice code for behaviorally modeled non-ideal modulator

```
.option post

***AC inputs***
vin1 in1 0 sin(1.65 600m 8k)
vin2 in2 0 sin(1.65 -600m 8k)

***Ideal switches***
xswt1 in1 2 clk1 idswt
xswt2 in2 4 clk1 idswt
xswt3 3 cm clk1 idswt
xswt4 5 cm clk1 idswt
xswt5 3 intp clk2 idswt
xswt6 5 intn clk2 idswt
xswt7 dac1 2 clk2 idswt
xswt8 dac2 4 clk2 idswt

***Ideal opamp & comparator subcircuit calling***
xopamp intp intn intop inton cm idealopamp
xcomp intop inton outp outn idealcomparator
xdac1 outpx dac1 bitlogic
xdac2 outnx dac2 bitlogic
```

```
***delay elements***
xdelayp outp outpx delayel
xdelayn outn outnx delayel

***capacitors***
c1 2 3 1p
c2 4 5 1p
cf1 intp intop 2p
cf2 intn inton 2p

***clock voltages***
Vclk1 clk1 0 pulse(3.3 0 0n 1n 1n 270n 500n)
Vclk2 clk2 0 pulse(0 3.3 20n 1n 1n 230n 500n)

***common-mode voltage***
Vcm cm 0 1.65

**********Subcircuits**********

***Delay element***
.subckt delayel in out
Edel out 0 DELAY in 0 TD=0.25us SCALE=1 NPDELAY=25
Rout out 0 100meg
.ends

*** Ideal 1-bit comparator ***
.subckt idealcomparator in1 in2 out1 out2
e1 c1 0 in1 in2 max=3.3 min=0 999k
r1 c1 out1 100
e2 c2 0 in2 in1 max=3.3 min=0 999k
r2 c2 out2 100
.ends
```

```
***Differential non-ideal opamp***
.subckt idealopamp inp inn outn3 outp3 cm
eopm1 outp cm inp inn 10k
eopm2 cm outn inp inn 10k
rin1 inp cm 100meg
rin2 inn cm 100meg
rout1 outp outp1 10
rout2 outn outn1 10

****Clipping circuitry*********
d1 outp1 m1 dmod
v1 m1 0 1.45
d2 outn1 n1 dmod
v2 n1 0 1.45
r1 outp1 outp2 3
r2 outn1 outn2 3
r3 outp2 outp3 3
r4 outn2 outn3 3
d3 m2 outp2 dmod
v3 m2 0 1.85
d4 n2 outn2 dmod
v4 n2 0 1.85
.model dmod d
*****************
.ends

***Ideal switch***************
.subckt idswt vin vout phi
g1 vin vout VCR pwl(1) phi 0 0,100g 3.3,1m
.ends

***Ideal 1bit DAC***
.subckt bitlogic in out
```

```
Gswitch1 bias1 out VCR PWL(1) in 0 1.649,1000meg 1.65,1m
Gswitch2 out bias2 VCR PWL(1) in 0 1.649,1m 1.65,1000m
Vbias1 bias1 0 2.15
Vbias2 bias2 0 1.15
.ends
**********************************************************************
.tran 0.1u 125u
.end
```

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