POWER OPTIMIZATION AND MODELING OF SWITCHED-CAPACITOR INTEGRATORS SUITABLE FOR DELTA-SIGMA MODULATORS

by

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ABSTRACT

POWER OPTIMIZATION AND MODELING OF SWITCHED-CAPACITOR INTEGRATORS SUITABLE FOR DELTA-SIGMA MODULATORS

In this thesis, the power dissipation aspects of the Switched-Capacitor (SC) integrators used in Delta-Sigma (ΔΣ) modulators are treated. ΔΣ modulators which employ oversampling are one of the most critical types of data converters and they are able to achieve high resolution at reasonably high conversion speeds. SC integrators are the key components of sampled-data ΔΣ modulators from the power consideration point of view. The structure of the SC integrator and the operational amplifier used determine the power consumption to a large extent. For this reason, firstly, the power optimization of the SC integrators is discussed via choosing the optimum SC integrator and operational amplifier design. Following that, a power model for SC integrators used in ΔΣ modulators is presented and its results are compared with the real implementations.

ÖZET

DELTA-SİGMA KİPLEYİCİLERE UYGUN ANAHTARLI-SIĞAÇ TÜMLEV ALICILARININ GÜÇ ENİYİLEME VE MODELLEMESİ

Bu tezde, Delta-Sigma (ΔΣ) kipleyicilerinde kullanılan anahtarlı-sığaç tümlev alıcıları güç harcamaları bakımından incelenmektedir. Yüksek hızda örnekleme kullanan ΔΣ kipleyicileri en önemli veri çevirici türlerinden biri olup oldukça yüksek çeviri hızlarında yüksek çözünürlüğe ulaşma yetisine sahiplerdir. Anahtarlı-sığaç tümlev alıcıları güç tüketimi yönünden örneklemeli ΔΣ kipleyicilerinin kilit bileşenleridir. Anahtarlı-sıgaç tümlev alıcının yapısı ve kullanılan işlemsel yükselteç güç tüketimini büyük ölçüde belirler. Bu nedenle, ilk olarak, en uygun anahtarlı-sığaç tümlev alıcı seçimi ve işlemsel yükselteç tasarımı yapılarak anahtarlı-sığaç tümlev alıcıların güç eniyilemesi ele alınmaktadır. Bunu takiben, ΔΣ kipleyicilerde kullanılan anahtarlı-sığaç tümlev alıcıları için bir güç modeli sunulmakta ve sonuçları gerçek uygulamalarla karşılaştırılmaktadır.

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LIST OF SYMBOLS / ABBREVIATIONS

C_f	Feedback capacitor
C_s	Sampling capacitor
C_L	Load capacitor
f_N	Nyquist frequency
f_s	Sampling frequency
V_{cm}	Common-mode voltage
Δ	Quantizer stepsize

ADC	Analog-to-Digital Converter
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DR	Dynamic Range
ENOB	Effective Number of Bits
IC	Integrated Circuit
LSB	Least Significant Bit
NMOS	N-channel Metal Oxide Semiconductor
NTF	Noise Transfer Function
OPAMP	Operational Amplifier
OSR	Oversampling Ratio
PMOS	N-channel Metal Oxide Semiconductor
SC	Switched-Capacitor
SNR	Signal-to-Noise Ratio
STF	Signal Transfer Function
$\Delta\Sigma$	Delta-Sigma

1. INTRODUCTION

1.1. Background

Most of the signals in the nature such as the sound, temperature, and images are in analog form which represents the continuous variation of physical quantities in time and in space. These signals are processed in the digital domain more effectively. That is because digital signal processing (DSP) techniques are much more advantageous than analog processing. Digital signal processing techniques present a high level of accuracy and reproducible, lossless, and high density storage. Also its flexibility, high performance and low cost are the reasons why DSP is preferred. Low cost, small size, low power consumption and high reliability are the other advantages of digital signal processing [1].

The very essential electronic components are Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) because they are the interface between the digital world and the real world. This conversion process as shown in Figure 1.1 represents the analog signal as a sequence of binary numbers which can be easily processed, stored or converted back to an analog signal. This way the real world sensors properly detect it [26].



Figure 1.1. The Analog-to-Digital Conversion process

Analog-to-Digital Conversion can be carried out using conventional Nyquist converters. These conventional high-resolution A/D converters, such as successive approximation and flash type converters, operate at sampling frequency approximately equal to twice the maximum frequency in the input signal. This is called the Nyquist rate. But these converters often do not make use of the high speeds achieved with VLSI

technology. Also, the accuracy of the digital signal is limited by the analog circuitry used in conventional A/D converters [27]. For example, high precision successive approximation conversion achieves up to 12 or 14 bits accuracy and it is even smaller in the case of flash type converters. This accuracy is inadequate in applications like high fidelity audio systems; thus, the usage of these conventional A/D converters results in poor performance of the system.

For higher resolution converters, Delta-Sigma (ΔΣ) modulation based analog-to-digital converters can be used. They are the cost effective alternative and can be easily integrated with digital signal processor ICs. In 1962, the Delta-Sigma Modulator was first introduced, but it gained importance recently with the developments in digital VLSI technologies. A low resolution A/D converter (1-bit quantizer), noise shaping and oversampling are used in ΔΣ A/D converters. With the help of oversampling and shaping the quantization noise out of band, high resolution is achieved by decimation or which is also called sample-rate reduction.

The basic operations for conversions include sampling, quantization and encoding. These steps required in an A/D converter are shown in Figure 1.2.

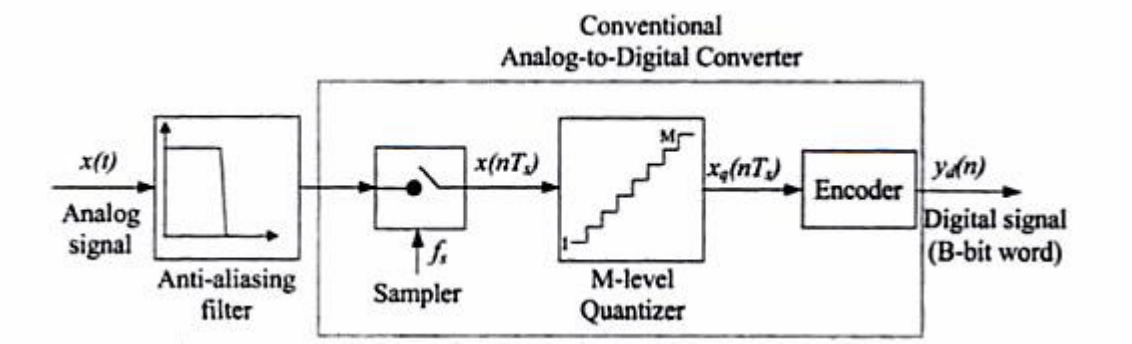

Figure 1.2. Block diagram of the basic functions of an A/D converter [1]

A continuous-time signal is transformed into its sampled-data equivalent by the sampler at uniform time intervals T_s. The output is given by

$$x'(t) = x'(nT_S) = \sum x(t)\delta(t - nT_S) \tag{1.1}$$

The input is multiplied by a sequence of delta functions; therefore, sampling a signal is equivalent to the mixing of the signal with a train of deltas [2]. The sampling rate f_s has to be at least twice that of the signal bandwidth ($f_s \geq 2f_b$) to avoid any loss of information. The information content of the signal is protected by the anti-aliasing filter. The samples are rounded to the closest quantization level in the M-level quantizer. Then, each quantized sample is encoded to the digital signal $y_d(n)$ which is a B-bit binary word.

A total of $M=2^B$ quantization levels are available because the final digital signal is a binary number of B bits. The amplitude of each quantization level for a uniform quantizer is

$$\Delta = \frac{X_{FS}}{M} \tag{1.2}$$

where Δ is the quantization step and X_{FS} is the range of the quantizer. The full signal range contains 2^B levels; thus, the quantization error corresponds to an error of one least-significant-bit (LSB) of the digital signal. A large quantization error reduces the capability to keep the signal features. This electronic noise is expressed using the signal-to-quantization-noise ratio (SQNR)

$$SQNR = \frac{P_{signal}}{P_{q-noise}} \tag{1.3}$$

which is the ratio of the signal power over the power of quantization noise. For a sine wave input signal with full scale amplitude variation, the SQNR is expressed as

$$SQNR = (6.02 \cdot B + 1.76)\ dB \tag{1.4}$$

which means SQNR and quantization error depend on the number of B bits and every additional bit of resolution improves the SQNR by 6.02 dB.

Conventional ADCs cannot fully satisfy the high resolution and dynamic range requirements in modern signal processing because of limitations in their implementation.

The sampling rate has to be increased in order to improve the situation. Sampling at a rate higher than the Nyquist rate is called oversampling and the ratio between the sampling and Nyquist rate the oversampling ratio (OSR). Oversampling is discussed in Chapter 2.

1.2. Outline of the Thesis

Chapter 2 deals with the Delta-Sigma (ΔΣ) modulation. Basic concepts of ΔΣ modulation such as oversampling and noise shaping are described along with the first and the second order ΔΣ modulators.

Chapter 3 gives brief information about the design automation tool designed earlier in MATLAB which includes automatic architecture generation for ΔΣ modulators considering component non-idealities and implementation and performance evaluation of ΔΣ modulators.

In Chapter 4, the power optimization of Switched-Capacitor (SC) Integrators is introduced. The opamp design and the SC integrator architectures are presented with explanations and simulation results.

Power modeling results are demonstrated in Chapter 5 along with the analytical background and the figures that compare the real implementations with the power model. Then, some further examples are given using different parameters and modulator architectures.

Finally, Chapter 6 brings the thesis to a close.

2. DELTA-SIGMA (ΔΣ) MODULATORS

The name Delta-Sigma comes directly from the presence of a Delta modulator and an integrator, as firstly introduced by Inose et al. in their patent application [28]. This section describes the basic concepts of ΔΣ modulation and explains the properties of low and high order ΔΣ modulators.

2.1. Oversampling

Sampling at a rate higher than the Nyquist rate is called oversampling. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{f_N} \tag{2.1}$$

where f_N is the Nyquist rate. Usually, the value of OSR is a power of 2; if the OSR is between 2 and 16 this is a mild oversampling but if the OSR is greater than 16 heavy oversampling occurs. In Figure 2.1 the oversampling is depicted. Here the OSR = 4 and the images of the signal band are not so close to one another which relaxes the specifications of the anti-aliasing filter. Also, if the SQNR is concerned, the quality of the digital signal is improved with oversampling [13].

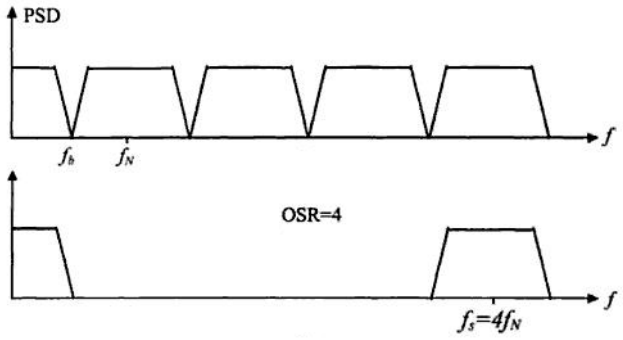

Figure 2.1. The oversampling process

The reason for the improvement in the quality of the digital signal is the distribution of the quantization noise power in a larger frequency range when oversampling is used. This is shown in Figure 2.2. Therefore there is a reduction in the power of the part of the quantization noise lying in the signal band.

With the usage of a high accuracy digital filter, the quantization noise lying outside the signal band can be eliminated. Thus, for a full scale input sine wave the SQNR is evaluated as follows:

$$SQNR_{oversampling} = 10\log\frac{V_S^2/2}{(\Delta^2/2)/\mathrm{OSR}} = SQNR_{Nyquist}10\log(OSR) \tag{2.2}$$

This equation shows that if the sampling rate is doubled and the out-of-signal-band noise is eliminated the SQNR can be improved by 3 dB or using half a bit in the resolution of the quantizer provides this, too.

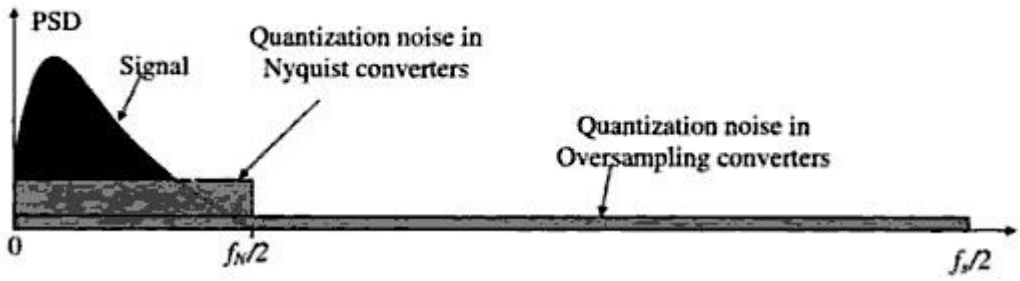

Figure 2.2. Quantization noise in Nyquist and Oversampling converters [1]

The oversampling is only appropriate in the analog world. In the digital domain, since storing and transmitting digital data is effective when using the lowest sampling rate that is compatible with the signal band, oversampling is not a suitable feature.

Also, oversampling means wasting power because the power consumption of digital circuits is proportional to the clock frequency. The sampling rate of digital oversampled signals is reduced with a decimation filter because of the disadvantages explained above.

2.2. Noise Shaping

The benefits of the oversampling can be enhanced by noise shaping and the oversampling method becomes more effective if the noise spectrum is lowered in the signal band. SQNR can be further improved by pushing the most of the in-band noise coming from the oversampling outside the signal frequency band as shown in Figure 2.3. This technique is called noise shaping and can be implemented by incorporating the quantizer in a feedback loop.

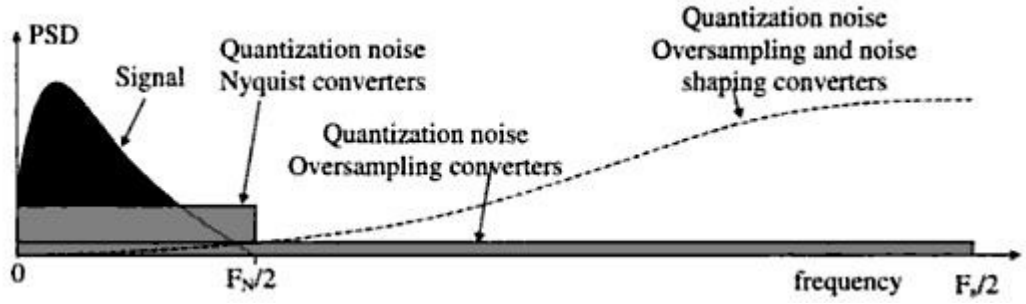

Figure 2.3. Spectrum at the output of a noise shaping quantizer [1]

Noise shaping tries to encode the integral of the input signal rather than the input signal directly. Since integration is a linear function it does not affect the system function if it is placed at the end of the system or at the beginning.

2.3. First Order ΔΣ Modulators

The first order ΔΣ modulator employs oversampling to spread the quantization noise over the $[0, f_s / 2]$ frequency band. Also it uses noise shaping in order to push most of the in-band noise out of this band to higher frequencies [3, 25].

The general form of the first order ΔΣ modulator is shown in Figure 2.4. It consists of an integrator, a sampler and an encoder. The sampler and the encoder omitted version block diagram is shown in Figure 2.5. They are omitted because they have no impact on the analysis at this level. The quantizer is replaced by its linear model in Figure 2.5.

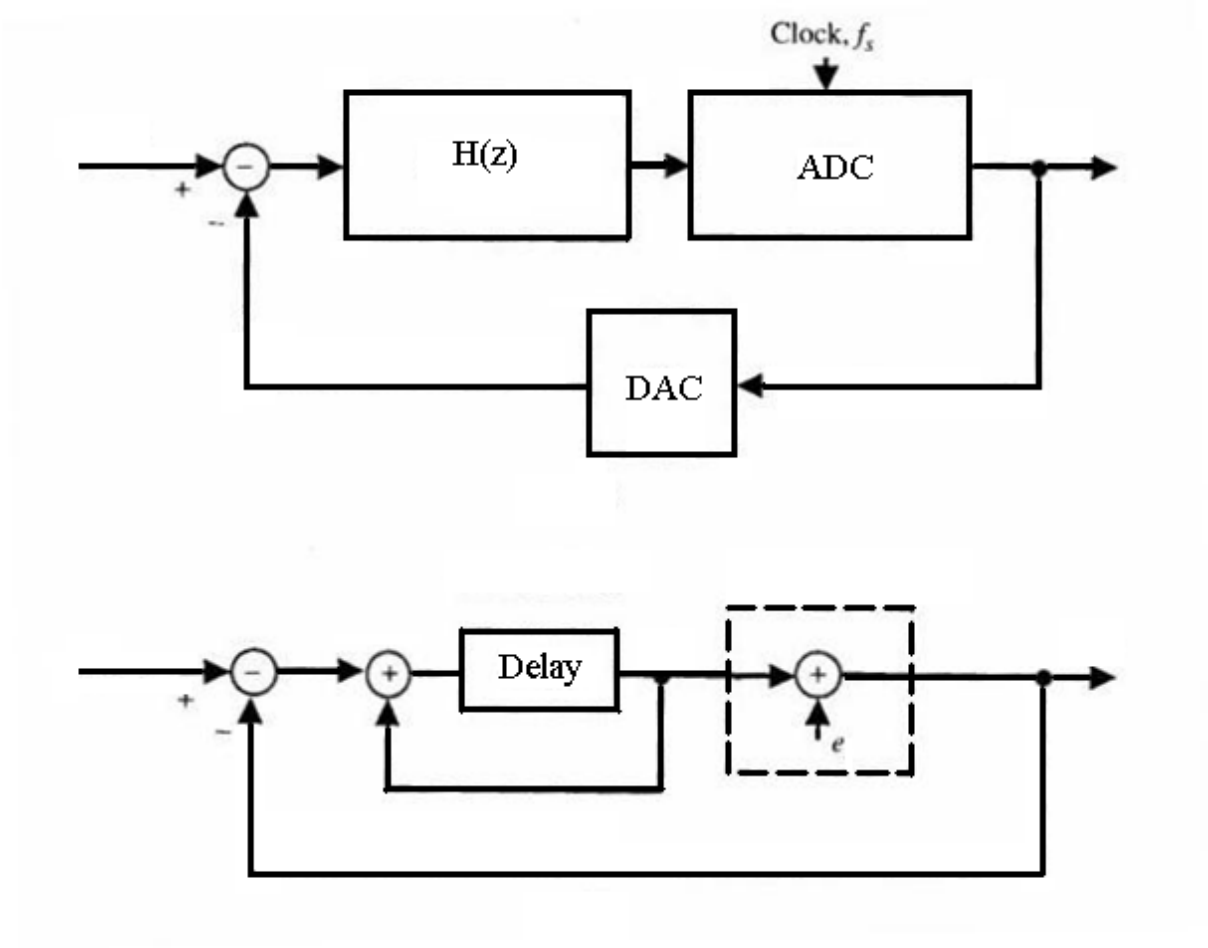

Figure 2.4. General form of a first order ΔΣ modulator

Figure 2.5 shows the block diagram of sampled-data ΔΣ which uses the transfer function

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.3}$$

to realize the analog sampled-data integration. The circuit is described by the following equation:

$$Y(z) = \{X(z) - Y(z)\}\frac{z^{-1}}{1 - z^{-1}} + E(z) \tag{2.4}$$

which is equal to

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{2.5}$$

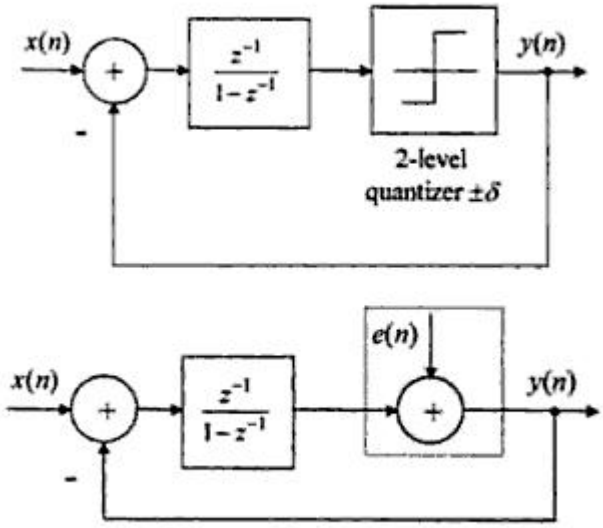

Figure 2.5. Block diagram of a first order ΔΣ modulator and its linear model

Equation (2.5) shows that there is a delay at the signal by one clock period and the noise is passed through $(1 - z^{-1})$ which means the modulator processes the signal and the quantization noise differently. Signal passes through the signal transfer function STF(z) and the quantization noise through the noise transfer function NTF(z)

$$Y(z) = X \cdot STF(z) + E(z) \cdot NTF(z) \tag{2.6}$$

and STF and NTF are:

$$STF(z) = z^{-1} \tag{2.7}$$

$$NTF(z) = 1 - z^{-1} \tag{2.8}$$

An example of the power spectral density (PSD) of the output signal is given in Figure 2.6 for small variations of frequency. One could observe that the spectrum can exhibit discrete tones which can be at multiples of the input frequency, very dense at all frequencies or they may not exist at all.

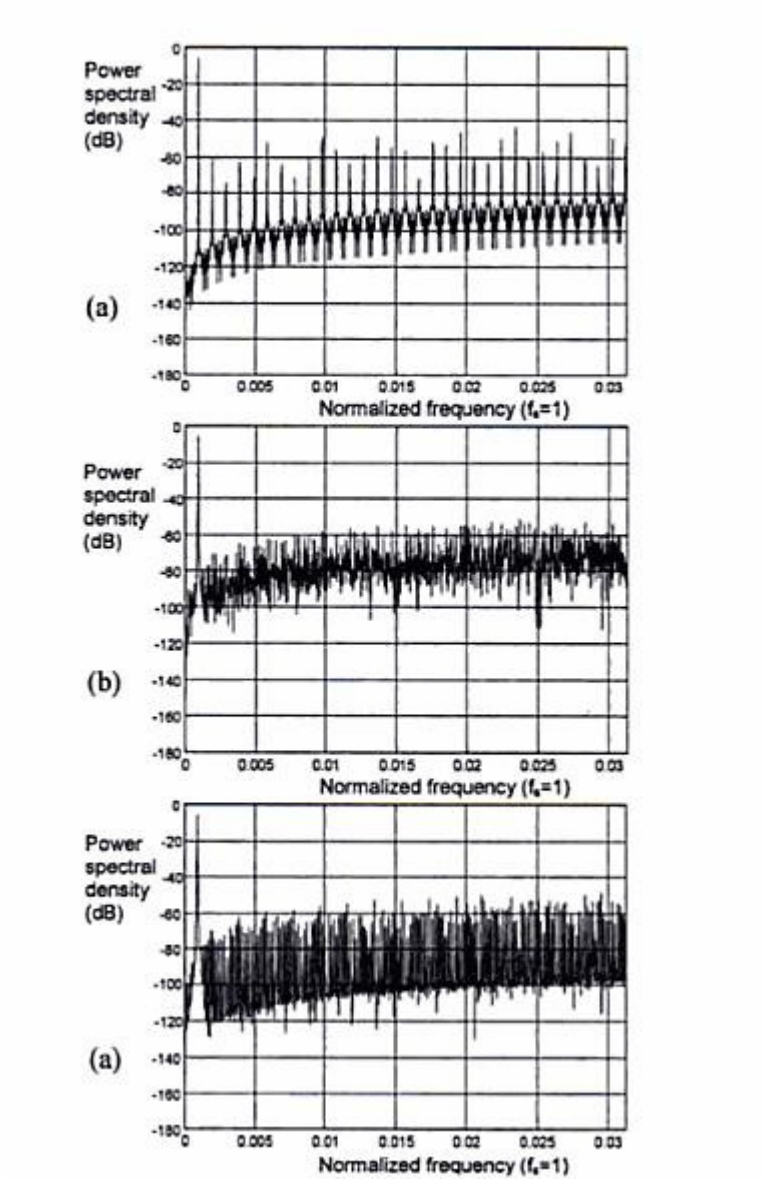

Figure 2.6. Power spectral density of the output signal of the first order ΔΣ modulator for very slight changes in the input frequency [1]

These three cases are shown in Figure 2.6 and they depend on slight changes in the frequency of the input signal. The input frequencies are 9.7656×10^{-4}, 9.7534×10^{-4} and 9.6451×10^{-4} respectively. In many applications like audio systems this is very undesirable. Although the total in-band noise is low, the tones can be audible. That limits the applications of the first order ΔΣ modulator because of its limited dynamic range (DR) and noise tones.

The maximum SNR of the first order ΔΣ modulator is given by

$$SNR = \frac{12}{8} \cdot k^2 \cdot \frac{3}{\pi^2} \cdot OSR^3 \tag{2.9}$$

where k is the number of thresholds used by the ADC. We observe that the SNR of the first order ΔΣ modulator depends on the third power of OSR which means that there is a 9 dB (1.5-bit) improvement per doubling of the OSR.

2.4. Second Order ΔΣ Modulators

In order to secure high resolutions using a 1-bit ADC, it is necessary to use a large OSR. But in some cases the output spectrum is poorly shaped and has large tones that could fall in the signal band [2]. By using two integrators around the loop better performances and features are secured. This forms a second order modulator as shown in Figure 2.7.

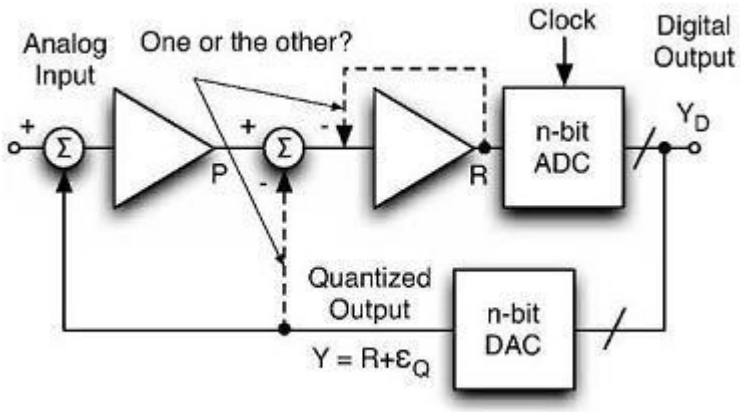

Figure 2.7. Conceptual second order ΔΣ modulator [2]

A possible sampled-data block diagram of this second order modulator is shown in Figure 2.8. The usage of two integrators in a feedback loop can make the modulator instable, so one of the two integrators has to be dumped by using one of the two options shown in Figure 2.7. One option forms a conventional approximated integrator and the other one uses a longer path and includes the quantizer in the dumping loop.

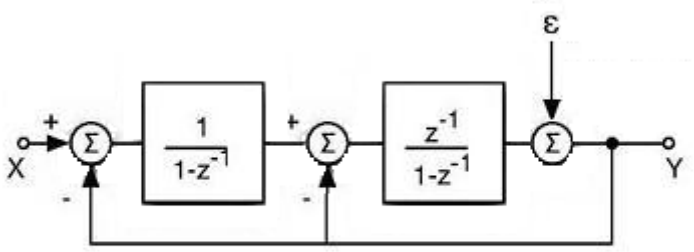

Figure 2.8. Possible sampled-data block diagram of the second order ΔΣ modulator

The sampled-data block diagram of the second order ΔΣ modulator shown in Figure 2.8 uses the second type of dumping described above and employs two integrators. One of the integrators has a delay element. This option gives the optimum signal transfer function STF.

The circuit is expressed by the following equation:

$$\left\{[X(z) - Y(z)]\frac{1}{1 - z^{-1}} - Y(z)\right\}\frac{z^{-1}}{1 - z^{-1}} + E(z) = Y(z) \tag{2.10}$$

If we rearrange equation (2.10)

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z) \tag{2.11}$$

where STF and NTF are:

$$STF(z) = z^{-1} \tag{2.12}$$

$$NTF(z) = (1 - z^{-1})^2 \tag{2.13}$$

Equation (2.11) reveals that the signal transfer function STF is just a single simple delay and the noise transfer function NTF is the square of the result obtained by a first order ΔΣ modulator and it is a second order differentiator.

The power spectral density of the output signal for low frequencies is shown in Figure 2.9. The noise is now randomized and does not have any discrete tones.

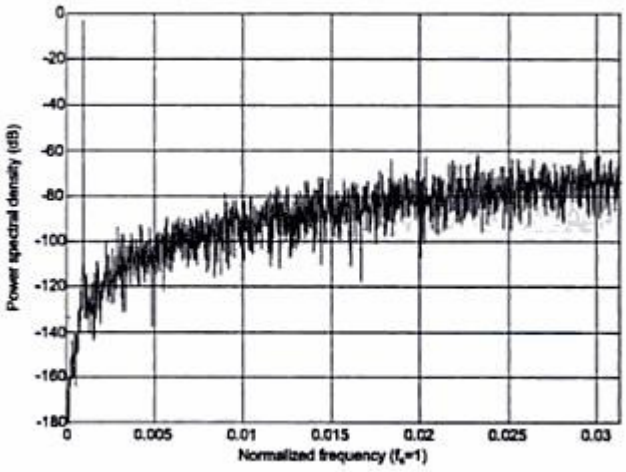

Figure 2.9. Power spectral density of the output signal of the second order ΔΣ modulator for low frequencies [1]

The maximum SNR of the second order ΔΣ modulator is given by:

$$SNR = \frac{12}{8} \cdot k^2 \cdot \frac{5}{\pi^4} \cdot OSR^5 \tag{2.14}$$

which reveals that there is an increase of 15 dB (2.5-bit) for every doubling of the oversampling ratio OSR.

2.5. Higher Order ΔΣ Modulators

Extending the order of the ΔΣ modulator from first to second is advantageous as one could observe from the previous sections. Higher order modulators are found to offer improved performance at the expense of more hardware and reduced signal range [4]. But

there are a number of problems implementing these higher order ΔΣ modulators. The most important problem is instability.

There are various architectures to implement higher order ΔΣ modulators. The most common ones in the design of high order ΔΣ modulators to be used for A/D conversion are the single-stage architectures.

The block diagram of a single-stage ΔΣ modulator is given in Figure 2.10.

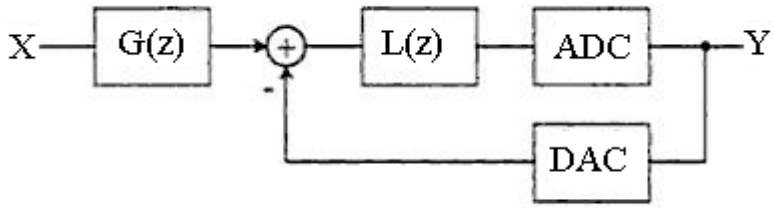

Figure 2.10. Block diagram of higher order ΔΣ modulator

These modulators consist of a loop filter L(z), a local ADC and a local DAC in a single loop. Any STF can be implemented with the addition of a pre-filter G(z). The loop filter is implemented by suitably cascading integrators which create various structures. Some of these are given in Figure 2.11 for third order ΔΣ modulators.

These structures are classified as CIDF (The Cascaded Integrators with Distributed Feedback), CIDIDF (The Cascaded Integrators with Distributed Input and Distributed Feedback) and CIDIFF (The Cascaded Integrators with Distributed Input and summed Feed-Forward).

In CIDF, all the integrators are delaying integrators; in CIDIDF, all the integrators can be delaying or non-delaying and CIDIFF employs single output feedback and the integrators can be delaying or non-delaying.

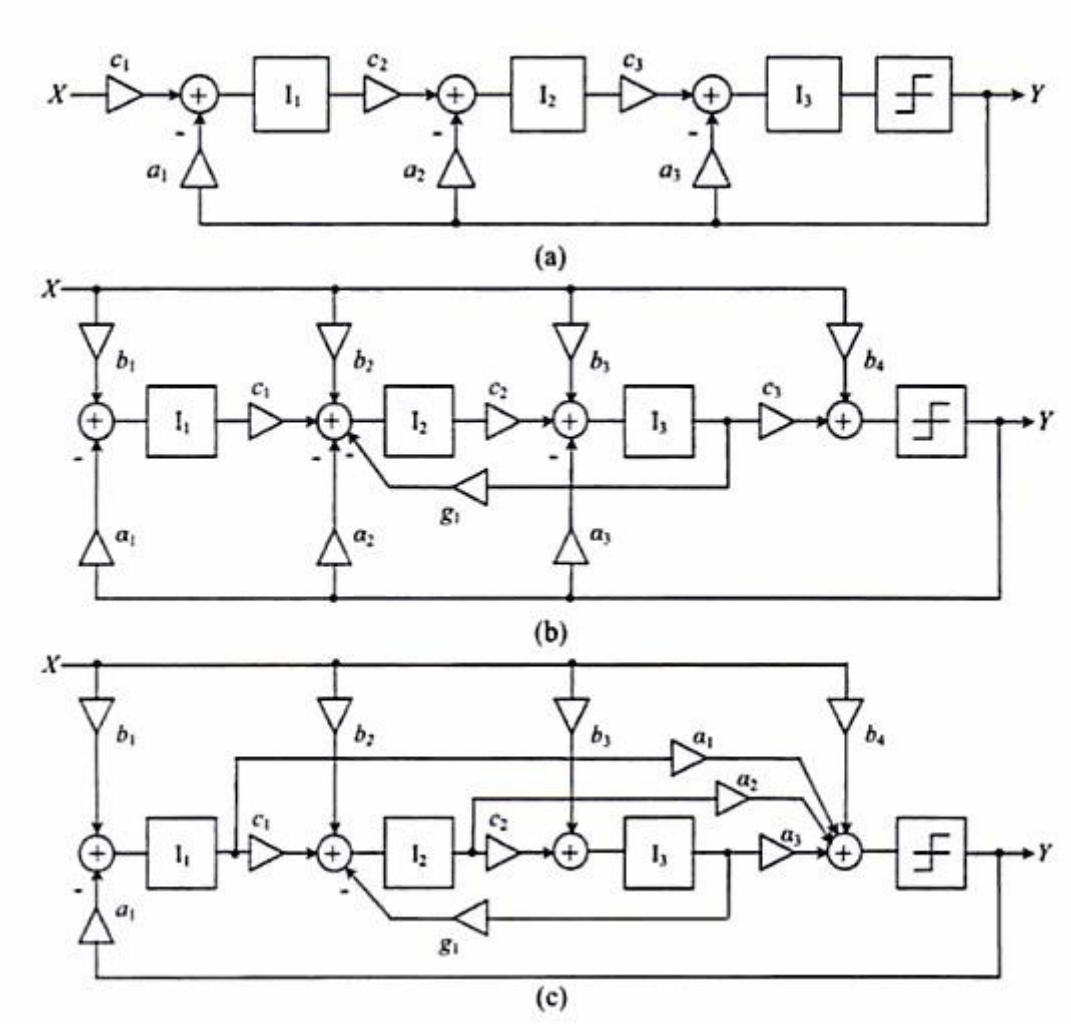

Figure 2.11. Third order single-stage ΔΣ modulator structures [1]

2.6. Multi-bit ΔΣ Modulators

The resolution of a ΔΣ modulator is increased by increasing the number of bits of the quantizer. In a multi-bit quantizer, it is easy to provide the stability of the modulator. This means that the multi-bit ΔΣ modulator is less prone to instability. Also, we get a better linear approximation at the output of the quantizer to the signal at its input.

2.7. Comparison of ΔΣ Modulator architectures

Table 2.1 gives a classification of the most popular ΔΣ modulator architectures in which the advantages and the drawbacks of each architecture is presented [5].

Table 2.1. Classification of ΔΣ modulator architectures

Delta-Sigma	**1-bit, low order**	**1-bit, high order**	**High order, cascade**	**Multi-bit**
Advantages	- Stability - Simple circuitry - Max. useful input range	- Large SNR - Smaller noise	- Large SNR - Stability - Max. useful input range	- Large SNR for very low M - Better stability - Smaller noise
Drawbacks	- High value of M needed - Presence of noise	- Conditional stability - Need of low gain integrators	- Sensitivity to circuit imperfections - Complexity of the digital part	- More complex circuitry - Sensitivity to DAC non-linearity.

3. ΔΣ MODULATOR DESIGN AUTOMATION TOOL

Regarding all design choices and possible iterations made in absence of an assisting design automation tool, the time spent for designing a Sigma-Delta ADC is very large compared to the time required for a digital design, which has a well-defined design flow and design tools. The increasing complexity of Sigma-Delta ADCs creates a demand for design automation tools [15]. Some design automation tools have been presented [5, 16, 17, 18, 19, 20, 21] in the literature and most of them have found limited use in the industry.

The tools proposed in [6, 7] are design automation tools for ΔΣ modulators generated in the MATLAB environment. The tasks of the tools include automatic architecture generation and implementation and performance evaluation of ΔΣ modulators. These tools are used in this thesis to form a base for the power optimization and modeling of switched-capacitor (SC) integrators which are used in the design of ΔΣ modulators. This chapter briefly covers these tools by explaining their operations and how they work.

3.1. The Automatic Architecture Generator

This tool works independently of the modulator order and finds all possible ΔΣ modulator topologies satisfying a desired system response with the minimum number of signal paths which in turn leads to minimum complexity. There are two basic parts in this tool. First one is the generation of the symbolic transfer functions STF and NTF for any given topology of any order and with any complexity; and the second part is the generation of all possible topologies with minimum number of signal paths which leads to minimum complexity.

3.1.1. Generation of the Parametric/Symbolic Transfer Functions

This part is a symbolic analyzer for ΔΣ modulators which works in a SPICE-like fashion. A netlist of a ΔΣ modulator in block level is given as the input. Then, it determines the input-output relation for each block in z-domain and generates an equation for each node of the architecture in terms of symbolic variables. The transfer function from

any node to any node is easily found afterwards by just writing the ratio of one node to one another.

The blocks defined to be used in the netlist are summarized in Table 3.1.

Table 3.1. Blocks that are defined in the architecture generator tool

Block	**Explanation**
INTEGRATOR	An integrator block with the z-domain transfer function of $\frac{1}{1-z^{-1}}$. No delay.
INTEGRATORD	An integrator block with the z-domain transfer function of $\frac{z^{-1}}{1-z^{-1}}$. One unit delay.
NONIDEAL_INTEGRATOR	An integrator block with the z-domain transfer function of $\frac{b}{1-cz^{-1}}$. b and c are integrator non-idealities. No delay.
NONIDEAL_INTEGRATORD	An integrator block with the z-domain transfer function of $\frac{bz^{-1}}{1-cz^{-1}}$. b and c are integrator non-idealities. One unit delay.
ADDER	A dynamic block working independently of the number of inputs to it which can add or subtract any number of signals simultaneously.
GAIN	A one-input one-output block used to model the ΔΣ modulator architecture coefficients or path gains.

Also there are some reserved terms which are IN and NOISE defining the input signal and the quantization noise, respectively. The 1-bit quantizer in the ΔΣ modulator is assumed to be an ideal unity gain element. It is defined as an adder in the netlist. The D/A converter is also ideal and is just a unity gain element.

In Figure 3.1, there is a generic second order ΔΣ modulator architecture which includes all the possible feedback and feedforward paths from g_1 to g_{15}. Assuming the integrators to be ideal, it can be defined in block level by the netlist shown in Figure 3.2.

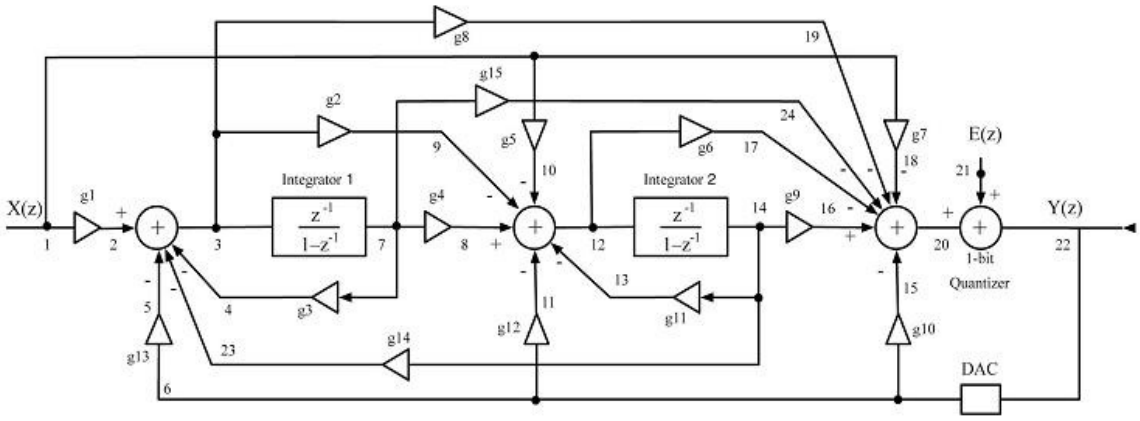

Figure 3.1. Second order ΔΣ modulator architecture with all possible paths [8]

1	IN 1	13	GAIN12 6 11
2	GAIN1 1 2	14	GAIN13 6 5
3	GAIN2 3 9	15	GAIN14 14 23
4	GAIN3 7 4	16	GAIN15 7 24
5	GAIN4 7 8	17	ADDER 2 -5 -4 -23 3
6	GAIN5 1 10	18	ADDER 8 -9 -10 -11 -13 12
7	GAIN6 12 17	19	ADDER 16 -17 -18 -19 -15 -24 20
8	GAIN7 1 18	20	ADDER 20 21 22
9	GAIN8 3 19	21	DAC 22 6
10	GAIN9 14 16	22	INTEGRATORD 3 7
11	GAIN10 6 15	23	INTEGRATORD 12 14
12	GAIN11 14 13	24	NOISE 21

Figure 3.2. The netlist for the architecture shown in Figure 3.1

After the tool gets this netlist as the input and generates symbolic expressions for each node, we get equations of every node. Then, the STF and NTF in terms of path gains (g_1 to g_{15}) are generated by using the proper fractional expressions. For example, for the architecture of Figure 3.1 x_{22} is the output node, x_1 is the signal input node and x_{21} is the

noise input node. The resulting STF and NTF in terms of path gains can be found by using the expressions of these nodes.

This part of the tool can also be used standalone as a symbolic analyzer. Various design alternatives at the block level can be evaluated by this analyzer since it is independent of the order of the architecture and the actual blocks.

3.1.2. Generation of All Possible Topologies

After the generation of the symbolic STF and NTF, this part of the tool comes into action. The generated symbolic STF and NTF are matched with user provided desired STF and NTF. In order to do that, the coefficients of the symbolic STF and NTF are matched with those of the numeric STF and NTF defined by the user.

Then, the tool generates a set of equations in terms of path gain parameters resulting from this matching. This set of equations is solved simultaneously to generate a set of solutions. Each element of this set corresponds to a set of path gains g_1 to g_{15} which in turn corresponds to a different $\Delta\Sigma$ modulator architecture. Since the number of equations is less than the number of variables the tool introduces a freedom to the user in generating many different topologies all realizing the same desired response. Then the resulting set of equations are solved by invoking MATLAB's symbolic toolbox which is constructed on the MAPLE kernel. The tool runs some checks after the solution set is obtained. It eliminates duplicated and imaginary solutions. Finally, the tool returns a set of parametric solutions for the coefficients in which the values of coefficients are defined in terms of a few other coefficients. The rest is assigning some values to the parameters in the final solution set [8].

This tool can find different topologies since occurrence of both several feedforward and several feedback paths is allowed.

A flowchart summarizing the operation of the tool is given in Figure 3.3.

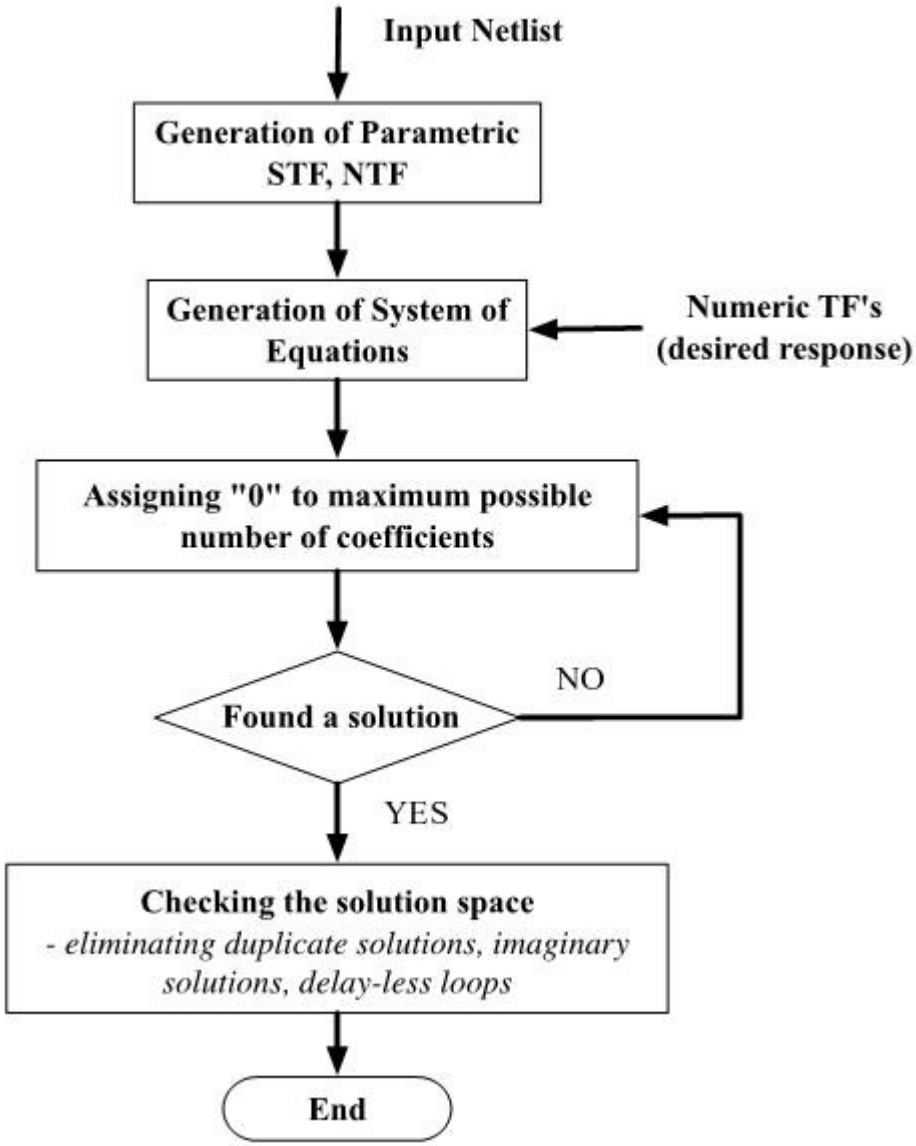

Figure 3.3. The flowchart of the automatic architecture generator tool [8]

3.1.3. The Component Non-idealities

The component non-idealities in the SC implementation of ΔΣ modulator architectures have a great impact on the system performance. Some of them can be directly mapped to the transfer functions of the system as an extra parameter. The integrator non-idealities are the most important part of those. The details of the analysis that focuses on this subject can be found in [8].

3.2. Implementation and Performance Evaluation

This tool starts its operation at the case of having all possible solutions of path gains in hand, which is achieved by the automatic architecture generator tool described in the previous section. The automatic architecture generator tool aims at finding topologies with the least number of paths, in other words, the minimization of hardware complexity. It can find various architectures with different combinations of feedforward and feedback coefficients. At that point, implementation of the architectures turns out to be an important concern. Starting from the path gains at hand, this tool aims at implementing the found architectures.

By finding general implementation rules any order of ΔΣ modulator topology implementation is possible. Then, from implementations of different architectures, some general deductions are made which leads the user to choose an architecture. Also, implementation gives some criteria to compare different architectures such as sensitivity to coefficients, area and power consumption. As a consequence, work is focused on power, area and sensitivity considerations. Finally, an approach of choosing an architecture for implementation is reached [9].

3.2.1. Implementation

In this phase, Switched-Capacitor (SC) design is used to implement the circuitry. Most integrated circuit (IC) implementations of ΔΣ modulators use SC circuits because of their numerous advantages such as ease of simulation, compatibility with VLSI technology, insensitivity to clock jitter and to the exact shape of opamp settling waveform, and highly accurate pole-zero locations set by capacitor ratios which are controllable to a high degree. Thus, the integrators in a ΔΣ modulator are usually implemented using SC circuits.

Paths with gains are inserted to the ΔΣ modulator architectures and the implementation of the coefficients in Figure 3.1 is carried out. The details of this can be seen in [9]. Finally, the implementation of the architectures is done by building ΔΣ modulators using the SC integrators, an opamp, a quantizer and a DAC.

The automatic architecture generator tool is used for finding solutions for the coefficients. From the solution set some topologies are selected and simulated to obtain the power spectral density of the output signal. Note that in ΔΣ modulators, SNR is found from the PSD graph by subtracting the highest noise component in the frequency band of 2.5 times the signal frequency from the signal.

An example of an implemented architecture is given below and more can be found in [9]. Figure 3.4 shows the block diagram of the standard second order ΔΣ modulator. In the architecture, values of the existing coefficients are $g_1= g_4=g_9= g_{12}= g_{13}=1$.

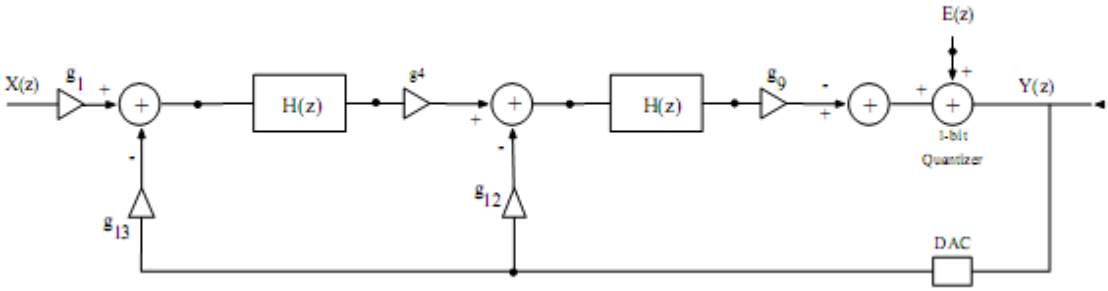

Figure 3.4. Standard second order ΔΣ modulator architecture

The PSD of the architecture is given in Figure 3.5. Signal is 42.5 dB and noise floor is at -10 dB. SNR is measured as 42.8 dB.

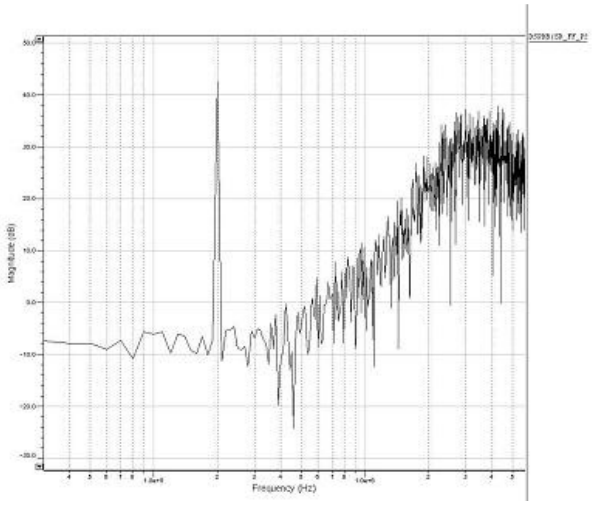

Figure 3.5. PSD of the standard second order ΔΣ modulator architecture [9]

3.2.2. Performance Evaluation

The different ΔΣ modulator architectures which realize the same STF and NTF are compared by means of some criteria which are the area occupied by the circuit, the sensitivity of the circuit and the power consumed by the circuit. Area and sensitivity considerations are not given here since they are irrelevant with the goal of this thesis. They can be found in [9].

On the other hand, the power consumption analysis presented in [9] is inadequate and improving this analysis is the main goal of this thesis. Firstly, a power optimization scheme is discussed before the power model developed from [10] is used to observe the change of power consumption in SC integrators by changing the capacitance values. Then, these power consumption results obtained from the power model and the ones obtained from the SPICE simulations are compared. The following two chapters introduce the power optimization and modeling of SC integrators.

4. POWER OPTIMIZATION OF SWITCHED-CAPACITOR INTEGRATORS

Power aspects of the design of the switched-capacitor (SC) integrators are treated in this chapter. The switched-capacitor technique is the basis for the circuit implementations of sampled-data ΔΣ modulators. It is possible to design integrators, with delay or without delay as required by modulator architectures, with switches and capacitors controlled by non-overlapped phases. Also, for the fabrication of the ΔΣ modulator as an IC, the integrators are usually built using SC circuitry. The first reason for that is the determination of the accuracy of coefficients by capacitor ratios which can be very accurate in MOS technology, and the second reason is that the value of coefficients does not depend on the sampling rate which can then be easily changed.

Thus, the switched-capacitor integrators are examined first in this chapter. Following that, the power optimization of the SC integrators is presented together with the opamp design and the simulation results. Then, the power modeling for switched-capacitor integrators are introduced. The results obtained from this are compared with the SC integrator power simulation results.

4.1. The Switched-Capacitor Integrators

Switched-capacitor building blocks are often classified into two categories: passive and active. A passive SC building block is a network composed of switches and capacitors only, whereas the active SC building block is not only built from switches and capacitors, but also active devices such as opamps. The passive SC elements are used in physical resistor simulation and sometimes they can be used to construct passive filters and voltage converters. On the other hand, active SC elements are widely adopted in the design of integrators, active filters, data converters, and so on [11].

Different architectures for switched-capacitor integrators are examined at the following sections.

4.1.1. Parasitic-Sensitive Switched-Capacitor Integrators

The inverting analog integrator is an essential building block in a continuous-time active-RC filter which is shown in Figure 4.1. Assuming the opamp is ideal, the time-domain expression of the circuit is given by

$$V_{out} = -\frac{1}{R_0 C_0}\int_{-\infty}^{t} v_{in}(\tau)d\tau \tag{4.1}$$

Using the Laplace transform, the s-domain transfer function is obtained as

$$H(s) = -\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sR_0C_0} \quad or \quad H(j\omega) = -\frac{1}{j\omega R_0 C_0} == -\frac{\omega_{-3dB}}{j\omega} \tag{4.2}$$

where ω_{-3dB} is the -3dB frequency.

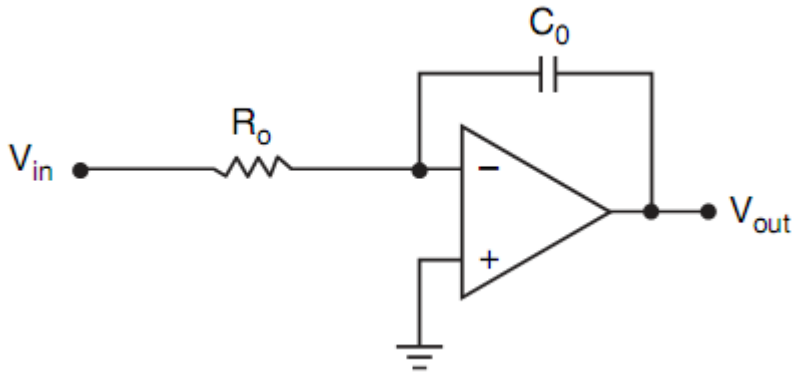

Figure 4.1. Inverting active-RC integrator

Replacing the resistor R_0 with the SC bilinear resistor simulation as shown in the first part of Figure 4.2 is the simplest way to realize an SC integrator. Its performance is sensitive to parasitic capacitances in the circuit. The input is a sampled-and-held signal clocked at $2f_{clk}$. It is sampled when Φ_1 is on. The parasitic-sensitive SC integrators given in Figure 4.2 are the parasitic-sensitive bilinear, parallel and series SC integrators, respectively.

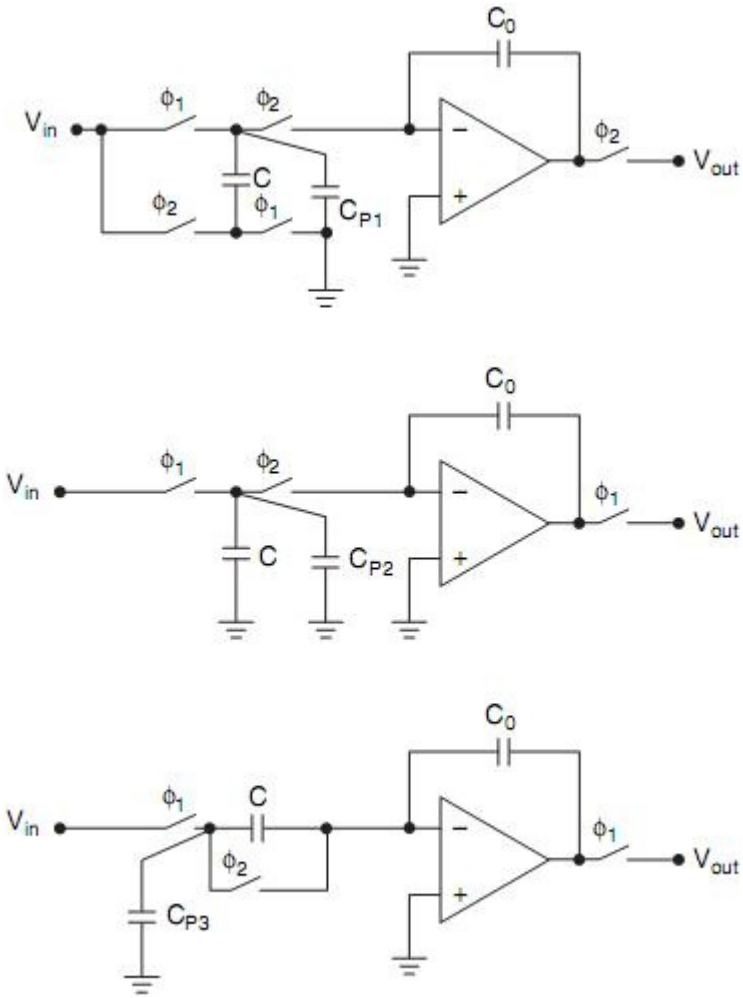

Figure 4.2. Parasitic-sensitive SC integrators [11]

The transfer function of the parasitic-sensitive bilinear SC integrator is given as

$$H_{BL}(z) = -\frac{C}{C_0}\frac{1+z^{-1}}{1-z^{-1}} \tag{4.3}$$

whereas the transfer function of the parasitic-sensitive parallel SC integrator is

$$H_{FE}(z) = -\frac{C}{C_0}\frac{z^{-1}}{1-z^{-1}} \tag{4.4}$$

and the transfer function of the parasitic-sensitive series SC integrator is

$$H_{BE}(z) = -\frac{C}{C_0}\frac{1}{1-z^{-1}} \tag{4.5}$$

The transfer functions of the parasitic-sensitive parallel and series SC integrators tells us that the parallel one has a delay element of z^{-1} whereas the series one is missing it.

4.1.2. Parasitic-Insensitive Switched-Capacitor Integrators

In practice, parasitic sensitive SC integrators are highly undesirable because the parasitic capacitances are not well controlled and can cause errors. To overcome that, some parasitic-insensitive SC integrators have been proposed by researchers.

These are the parasitic-insensitive parallel SC integrator, the parasitic-insensitive series SC integrator, and the parasitic-insensitive bilinear SC integrator which are given in Figure 4.3.

The transfer function of the parasitic-insensitive parallel SC integrator is given as

$$H_1(z) = -H_{FE}(z) = \frac{C}{C_0}\frac{z^{-1}}{1-z^{-1}} \tag{4.6}$$

whereas the transfer function of parasitic-insensitive series SC integrator is

$$H_2(z) = H_{BE}(z) = -\frac{C}{C_0}\frac{1}{1-z^{-1}} \tag{4.7}$$

and the transfer function the parasitic-insensitive bilinear SC integrator is

$$H_3(z) = H_{BL}(z) = H_2(z)\cdot(1+z^{-1}) = -\frac{C}{C_0}\frac{1+z^{-1}}{1-z^{-1}} \tag{4.8}$$

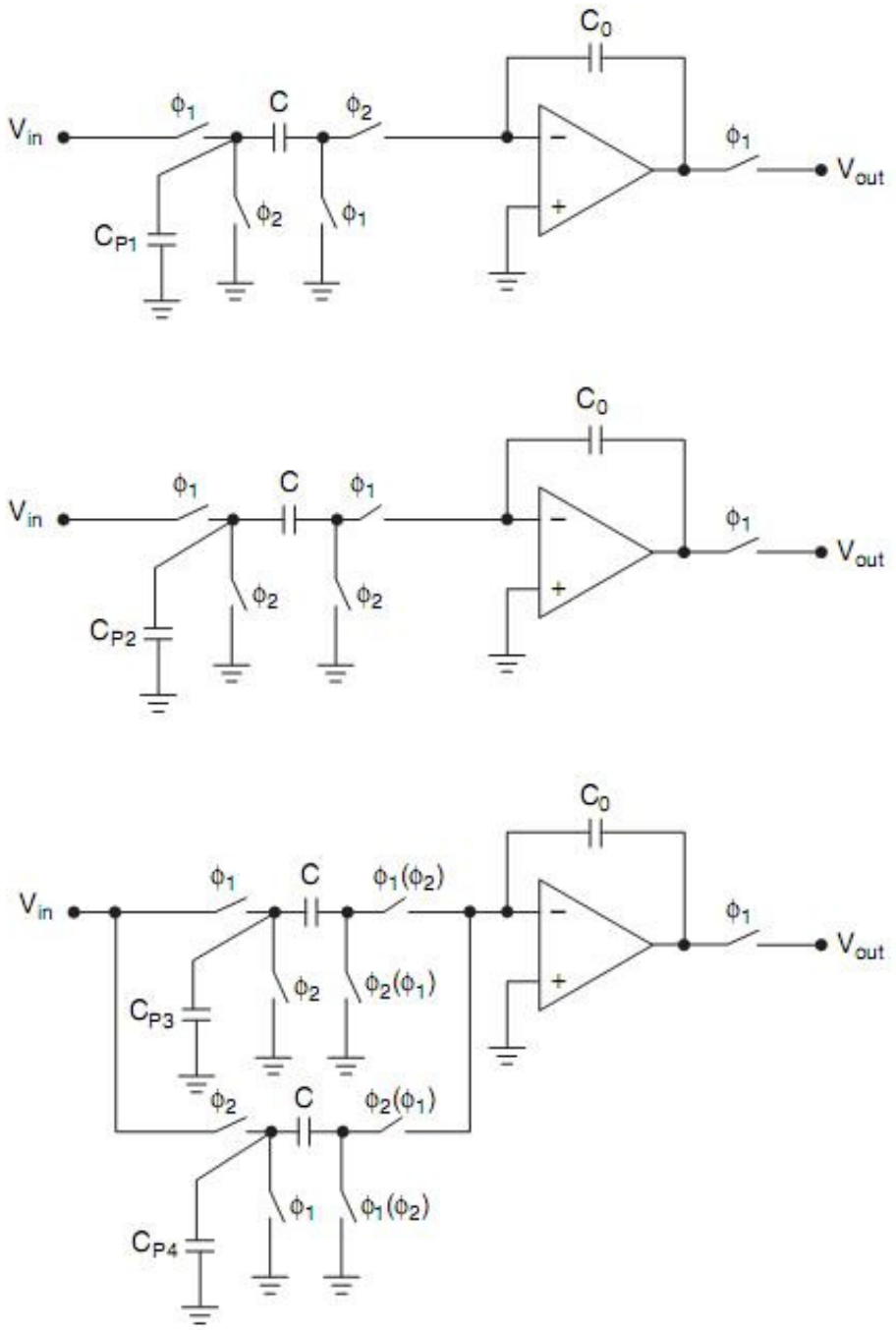

Figure 4.3. Parasitic-insensitive SC integrators [11]

Thus far all the SC integrators given are single-ended. Despite being economical, they suffer from non-ideality effects which can degrade the performance.

However, the usage of fully differential integrators overcomes this problem. These fully differential integrators are discussed in the following section.

4.1.3. Fully Differential Switched-Capacitor Integrators

Fully differential SC integrators improve the circuit's common-mode noise performance and facilitate the sign changes for transfer functions through simple wire-crossing operations. That is why they are more popular than the single-ended ones in modern SC circuits.

In Figure 4.4, a standard fully differential Euler SC integrator is given which is composed of the first integrator in Figure 4.3 and its horizontally flipped-over duplicate. Thus, a fully differential SC integrator is parasitic-insensitive by default because of being a combination of two or more parasitic-insensitive single-ended subcircuits.

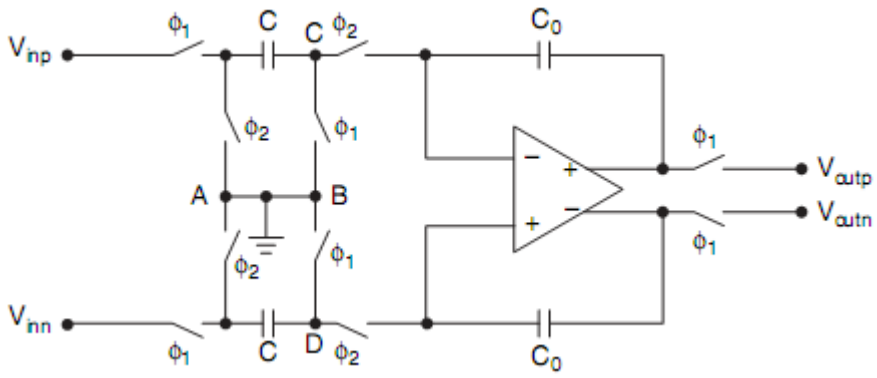

Figure 4.4. Fully differential Euler SC integrator [11]

If both the input and output are sampled when $\Phi_1 = 1$ the resulting transfer function will be given by Equation (4.6). If the output is sampled when $\Phi_2 = 1$, the delay element (z^{-1}) in the numerator of Equation (4.6) will be removed. In other words, depending on the sampling moments of the input and output, the circuit in Figure 4.4 may realize either a forward- (FEI) or backward-Euler integrator (BEI). These are given in Figure 4.5, respectively.

In Figure 4.4, the nodes A and B are connected to the ground or with each other, but in practice node A is divided into two nodes. One of them is connected to a positive reference voltage and the other one to a negative reference. The voltage difference between the inputs is sampled by the capacitors C. The differential reference specifies the dynamic

range requirement of the circuit. Node B is connected to a voltage source V_{CM} which can be adjusted by a biasing circuit.

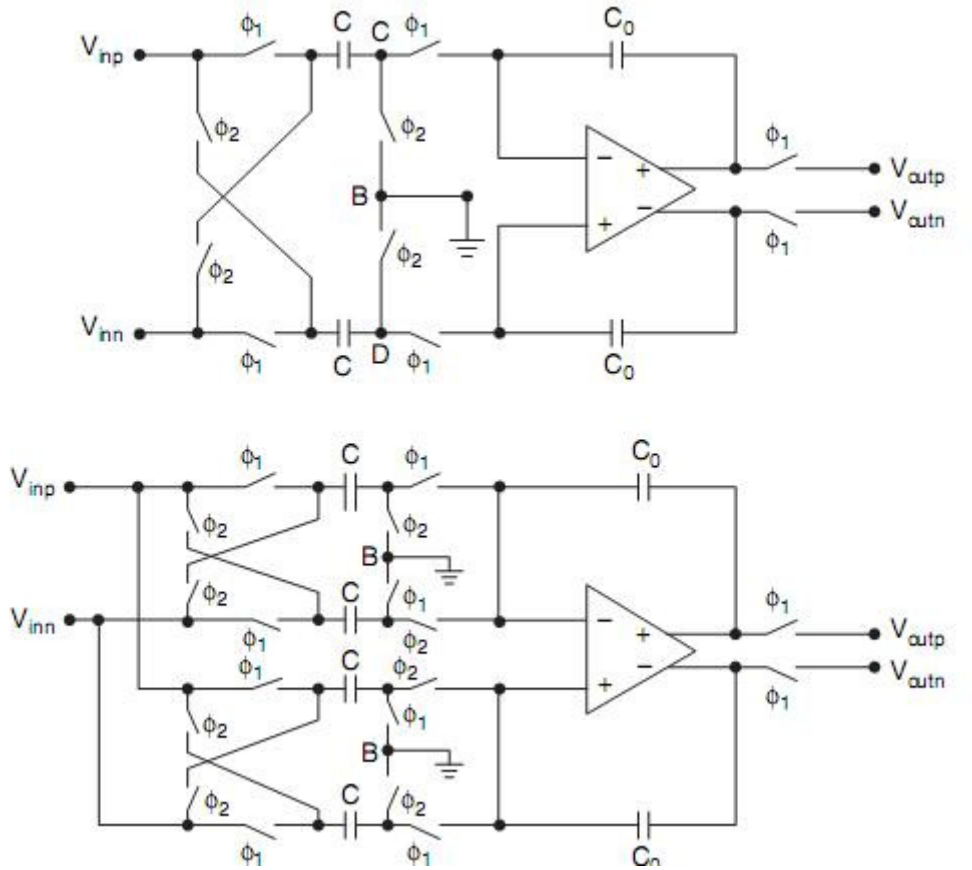

Figure 4.5. Fully differential bilinear/forward- Euler SC integrator and double-sampled bilinear Euler SC integrator [11]

Compared to the integrator in Figure 4.4, the first integrator in Figure 4.5 is more desirable for its capability of realizing both parasitic-insensitive bilinear and forward-Euler integrators. If both the input and output are sampled when $\Phi_1 = 1$ it realizes a bilinear SC integrator, if the input and output are sampled when $\Phi_2 = 1$ and $\Phi_1 = 1$, respectively then the forward-Euler transfer function is

$$H(z) = \pm\frac{2C}{C_0}\frac{z^{-1}}{1-z^{-1}} \tag{4.9}$$

and if the input and output are sampled when $\Phi_1 = 1$ the transfer function of the second integrator in Figure 4.5 is

$$H(z) = -\frac{C}{C_0}\frac{1+z^{-1}}{1-z^{-1}} \tag{4.9}$$

To ensure low power, the clock frequency has to be reduced. By duplicating the SC input stage of the first integrator in Figure 4.5 and connecting it to the original one forms the second integrator in Figure 4.5. This circuit is double-sampled so that the input is sampled at $2f_{clk}$ despite the actual clock frequency being only f_{clk}.

Various types of SC integrators are presented here including parasitic-sensitive/insensitive single-ended integrators and fully differential integrators, but there are many other SC integrators such as damping (lossy) SC integrators and very-large-time-constant (VLTC) SC integrators. These are used to resolve different design issues [11].

4.2. Power Optimization of the SC Integrators

As explained in the previous section, switched-capacitor circuits make use of one basic building block, namely the integrator. It is constructed of an opamp, a switch, and a capacitor, and with these a variety of integrator functions can be realized. Operational amplifiers used in SC circuits consume most of the power which makes them the most important part in the power considerations.

4.2.1. Operational Amplifier Design

Some operational amplifiers have been designed previously [22, 23] which can be used in low-voltage SC circuits. In high accuracy SC circuits, opamps must drive high capacitive loads especially when operating from a low supply voltage. Also, they have to settle within a definite short time period in high-speed applications. Class A operational amplifiers need high dc current in order to achieve large slew-rate as well as high unity-gain bandwidth.

However, in class AB amplifiers since the slew rate does not depend on the quiescent current and large currents are generated during slewing, a fast settling circuit is achieved with low static power dissipation [12].

4.2.1.1. Class A folded-cascode operational amplifier. A conventional folded-cascode operational amplifier is used first to show that its power consumption in an SC integrator is high.

As described in the previous section, there a number of different SC integrator architectures. The first one used in the design is a fully differential integrator and its block diagram is given in Figure 4.6. Fully differential integrators are chosen because of the advantages explained.

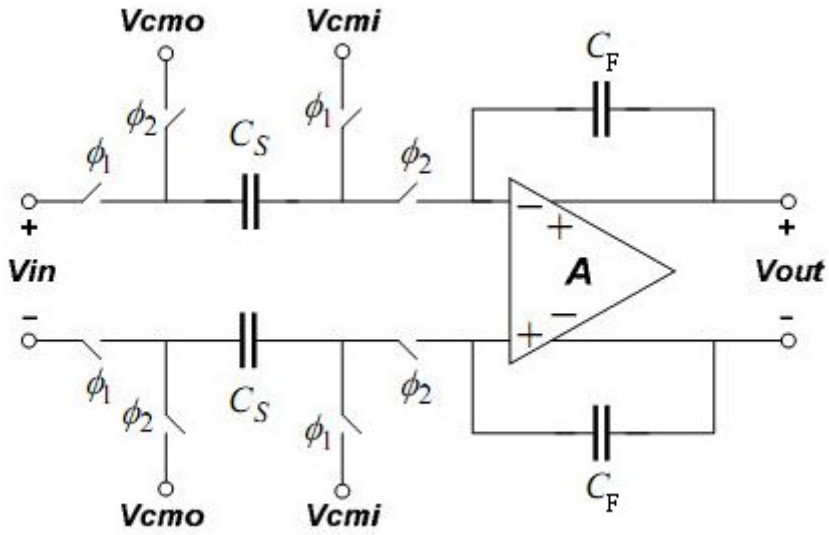

Figure 4.6. First order switched-capacitor integrator used in the design

The capacitors C_S and C_F are the sampling and feedback capacitors, respectively. V_{cmi} and V_{cmo} represent the common-mode voltages. Since the topology is fully differential, the class A folded-cascode operational amplifier used in the design is a fully differential amplifier, too and is shown in Figure 4.7. The difference between the common-mode voltage and the positive and negative inputs is sampled on C_S and is transferred to C_I. Then, a factor of the difference is realized where the factor is the ratio of C_S / C_F and called the gain factor.

The HSPICE simulation results showing the integrator positive and negative input and output differences are given in Figure 4.8. The capacitance values used in the simulation are C_S = 1 pF , C_F = 2 pF. The load used in this circuit is a capacitive load of C_L = 3.5 pF. The transistors in the circuit are sized properly to ensure low static power

dissipation. Thus, the measured power is as low as possible providing the correct integration operation.

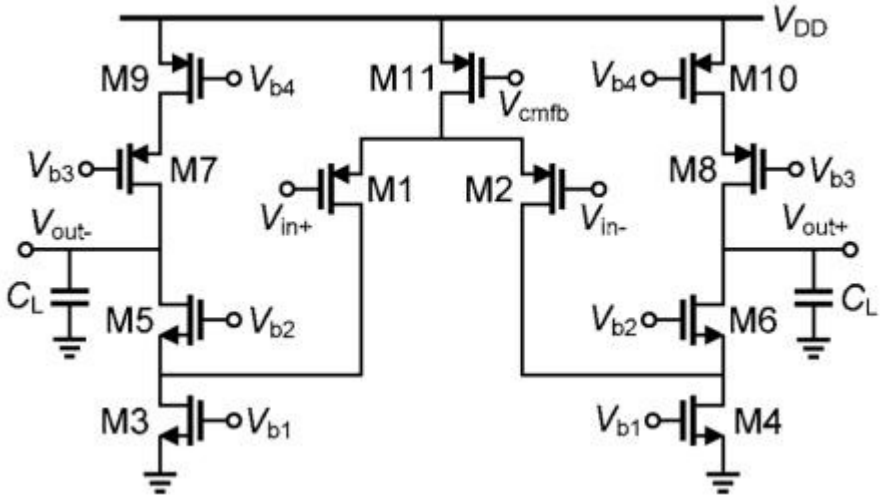

Figure 4.7. Class A folded-cascode operational amplifier

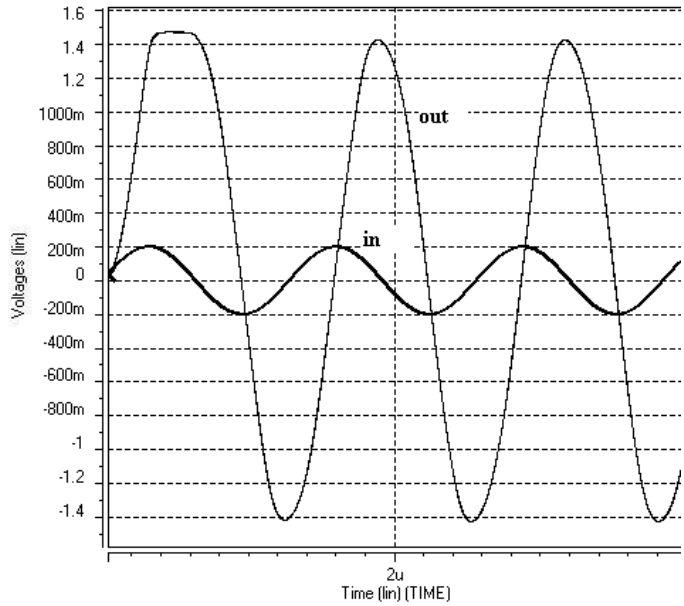

Figure 4.8. First order integrator input and output differences using class A opamp

The power consumed in this circuit is measured to be 221 µW. Further minimization in transistor sizes of the opamp causes the integrator to operate problematically. The sampling rate in this circuit is OSR = f_{in} / f_{clk} = 100 MHz / 0.78125 MHz = 128.

The simulation results of a second order integrator built using class A folded-cascode opamp are omitted because of the high power consumption of the first order integrator. The simulation results of the second order integrator built with the designed class AB folded-cascode opamp will be included below.

4.2.1.2. Class AB folded-cascode operational amplifier. The general structure of a class AB output stage is shown in Figure 4.9. A floating DC voltage source is connected between the gate terminals of transistors M1 and M2 operating as common source amplifiers. In this circuit, when a small input signal is applied, both transistors operate at the saturation region and hence the effective transconductance is $g_{m1} + g_{m2}$. Therefore, both DC gain and unity-gain bandwidth of a class AB output stage amplifier are greater than those of a class A output stage amplifier by $(1 + g_{m2} / g_{m1})$ ratio with the same static power dissipation.

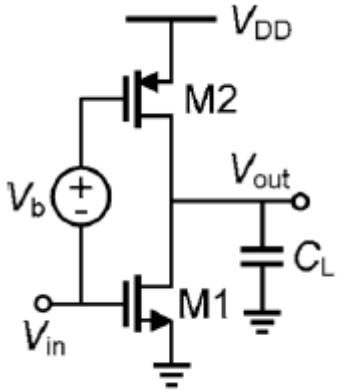

Figure 4.9. The general structure of a class AB output stage

The high current driving capability during slewing is the main advantage of a class AB amplifier. When a large input signal is applied to the circuit in Figure 4.9, the bias current of one of the output transistors is considerably increased and the other transistor turns off. So the load capacitor is discharged by a current that is much greater than the quiescent current of the amplifier.

An extra circuit to realize the floating DC voltage source is needed in the class AB output stage. The circuit given in Figure 4.10 is one of the alternatives and here the gate of

M2 is connected to a bias voltage and a capacitor is used to implement the floating voltage source when the amplifier is idle. However, in SC circuits amplifier is not idle in any of clock phases, thus the circuit in Figure 4.10 cannot be used in them.

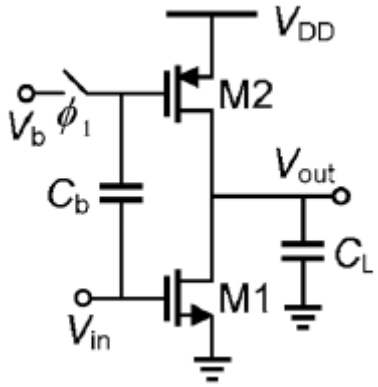

Figure 4.10. A switch and a capacitor realization of a class AB output stage

Another alternative called dynamic level shifting is given in Figure 4.11. In this circuit, to realize the floating DC voltage source the capacitor C_{b1} is used. A simple SC circuit consisting of the capacitor C_{b2} and the switches controlled by two non-overlapping clock phases, Φ_1 and Φ_2 define and refresh the DC voltage across the capacitor C_{b1}. This circuit can be employed in SC circuits, but an extra capacitor and two non-overlapping clock phases are needed.

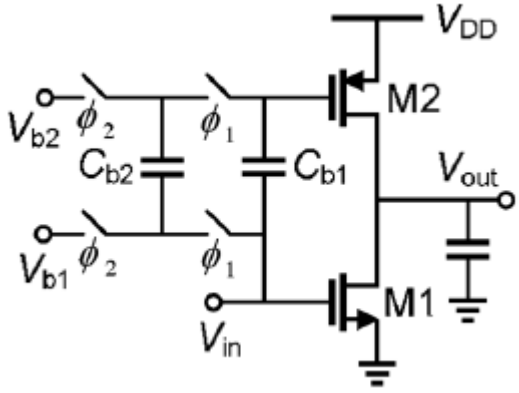

Figure 4.11. Dynamic level shifting

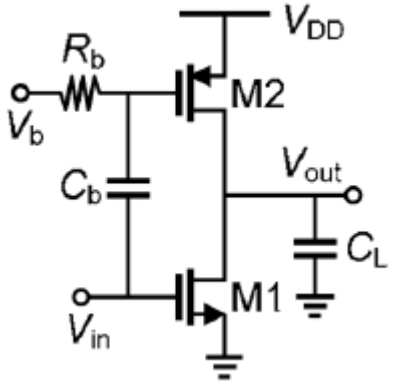

Figure 4.12. A large resistor and a capacitor realization of a class AB output stage

To define the gate DC voltage of M2 a large resistor can be used as shown in Figure 4.12. The gate bias voltage of M2 is always connected to V_b because there is no DC current through R_b. The DC voltage across the capacitor C_b is properly defined. Large resistor R_b prevents any signal attenuation from V_{in} to the gate of M2.

The circuit in Figure 4.12 is used to build the class AB operation. The topology built accordingly is shown in Figure 4.13. It is a single-stage class AB folded-cascode amplifier. The input signal is coupled through capacitors C_{b1}, C_{b2}, C_{b3} and C_{b4} to the gate of both NMOS and PMOS output current source transistors.

The gate bias voltage of output current source transistors are determined by connecting them to the proper bias voltage sources through large resistors. These resistors are realized by diode-connected PMOS transistors Mr1-Mr4 which are biased in the cut-off region to provide a very large resistor. Also, these transistors have a small aspect ratio.

The class AB folded-cascode operational amplifier has a very large slew-rate that is independent of the bias current. The bias voltages V_{b1} – V_{b4} determine the current of the input and cascode transistors under the quiescent conditions. Large and small input signal changes are directly coupled to the gate of the output current source transistors almost without any delay because between there is an equivalent lossy capacitive divider network consisting of the capacitors C_{b1} – C_{b4} paralleled with very large resistors realized by transistors Mr1 – Mr4. Since these resistors are very large, the frequency response of the circuit is flat beyond a few hertzs.

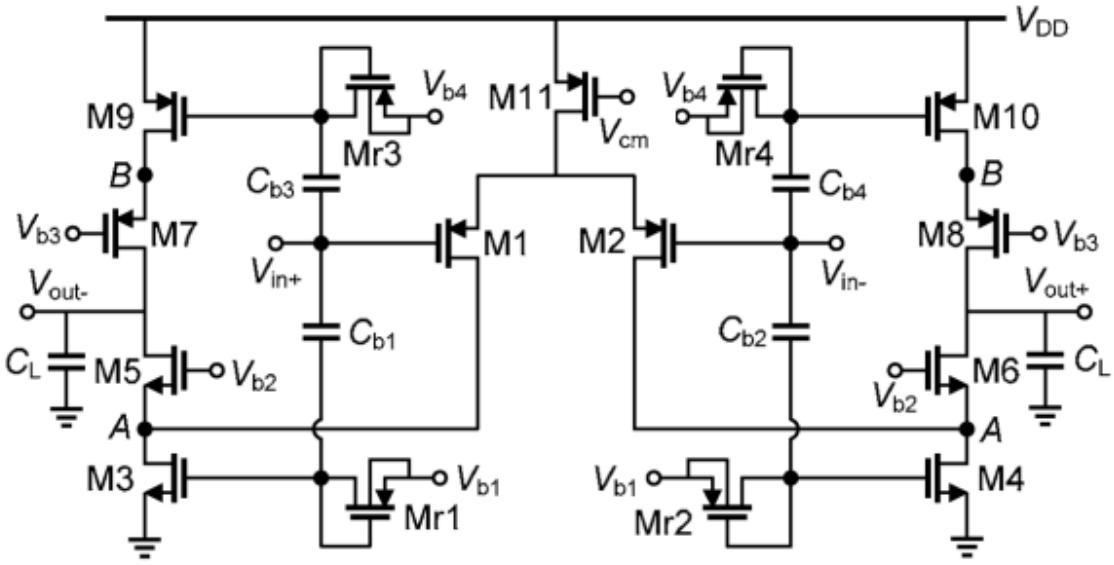

Figure 4.13. Class AB folded-cascode operational amplifier [12]

Thus, the output nodes change similar to the gate terminals of output current source transistors, but with a ratio determined by the feedback factor of the closed-loop circuit which uses the amplifier [12].

The power supply voltage requirement of the class AB folded-cascode operational amplifier is the same as the class A folded-cascode one.

To reveal the low power consumption of the class AB folded-cascode opamp, HSPICE simulations were performed using a 0.18-µm BSIM3v3 level 49 mixed-signal CMOS technology. The amplifier is used in a first order switched-capacitor integrator with sampling and feedback capacitors of 1 pF and 2 pF, respectively. The load capacitor is 3.5 pF in transient closed loop simulations. These capacitor values are selected to be the same with the ones in the class A opamp for a fair power consumption comparison. The transistors are properly sized to ensure low power without affecting the integration operation.

The first order integrator positive input and output are given in Figure 4.14. Again, the sampling rate in this circuit is OSR = f_{in} / f_{clk} = 100 MHz / 0.78125 MHz = 128.

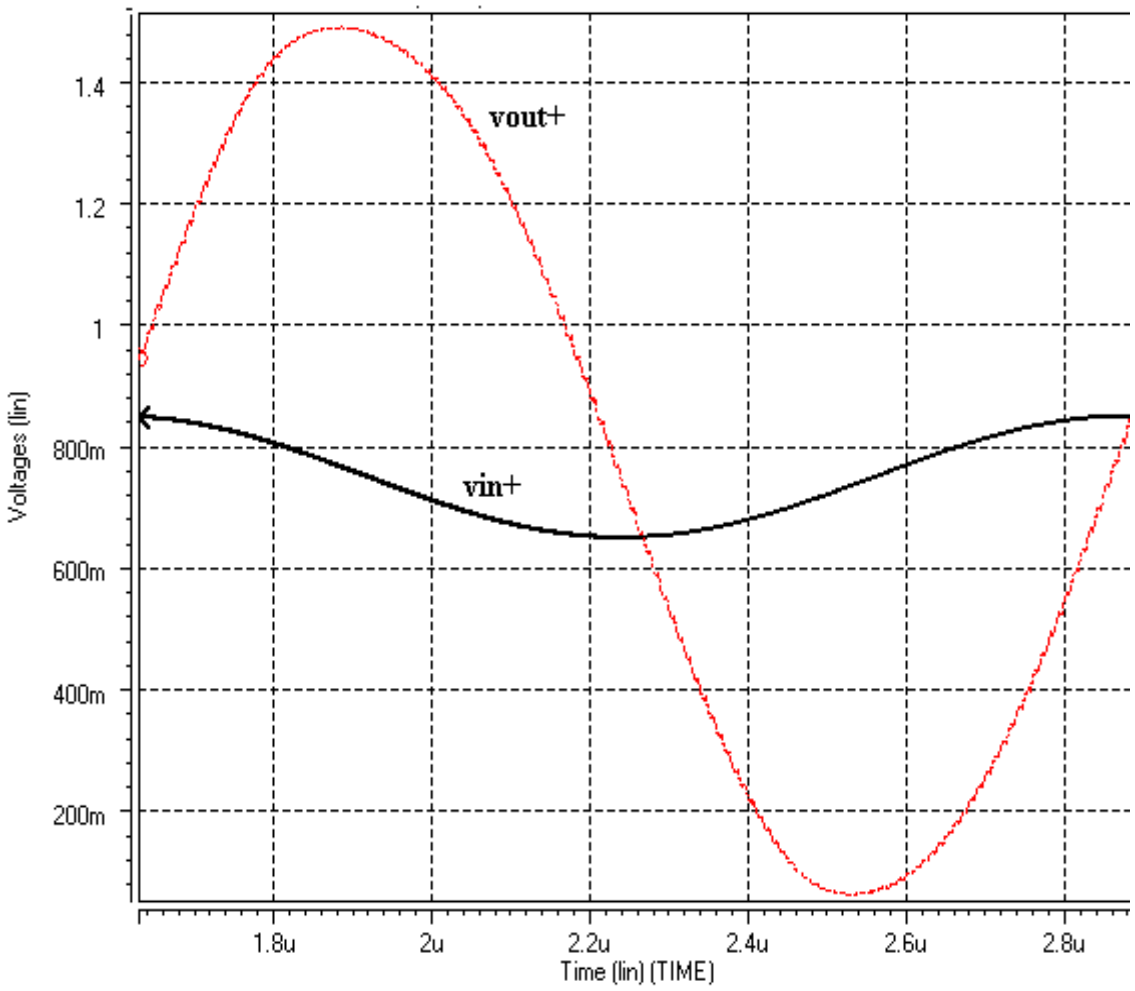

Figure 4.14. First order integrator positive input and output using class AB opamp

The static power dissipation of this circuit is measured to be 102 µW which is approximately half of that of the class A opamp.

The second order switched-capacitor integrator built with the designed class AB folded-cascode opamp is also presented below with the simulation results. The block diagram of a second order integrator is shown in Figure 4.15.

The second order switched-capacitor integrator is used with sampling and feedback capacitors of 1 pF and 2 pF, respectively. The load capacitor is 3.5 pF in transient closed loop simulations. These capacitor values and the transistors dimensions are selected to be the same as the ones in the first order integrator.

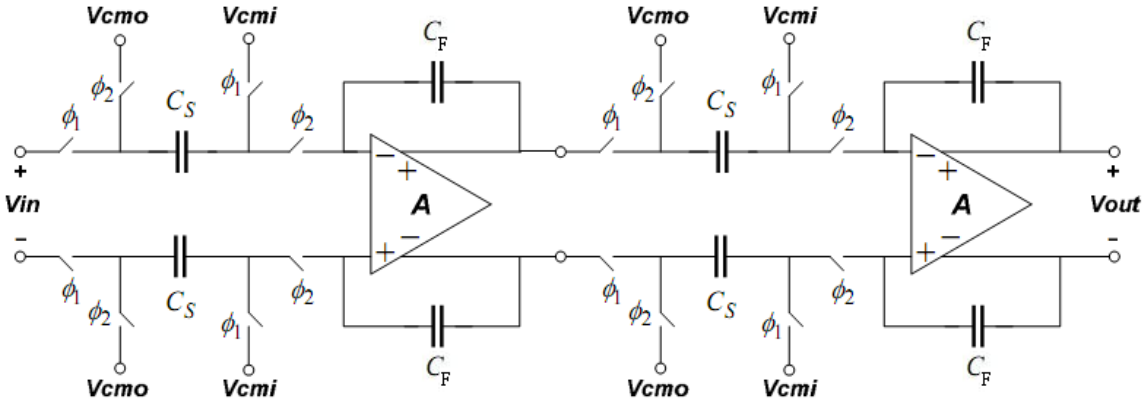

Figure 4.15. Second order switched-capacitor integrator used in the design

The second order integrator positive input, first integrator positive output, and second integrator positive output are given in Figure 4.16. Again, the sampling rate in this circuit is the same with the previous one, that is OSR = 128.

Because the exact same values with the previous integrator are used and because there is no DAC connection in this integrator, the second integrator output is clipped at its peaks. This affects the power consumption. Therefore, the static power dissipation of this circuit is measured to be 245 µW which is less than expected. That is because of the malfunctioning of the circuit at the output of the second integrator.

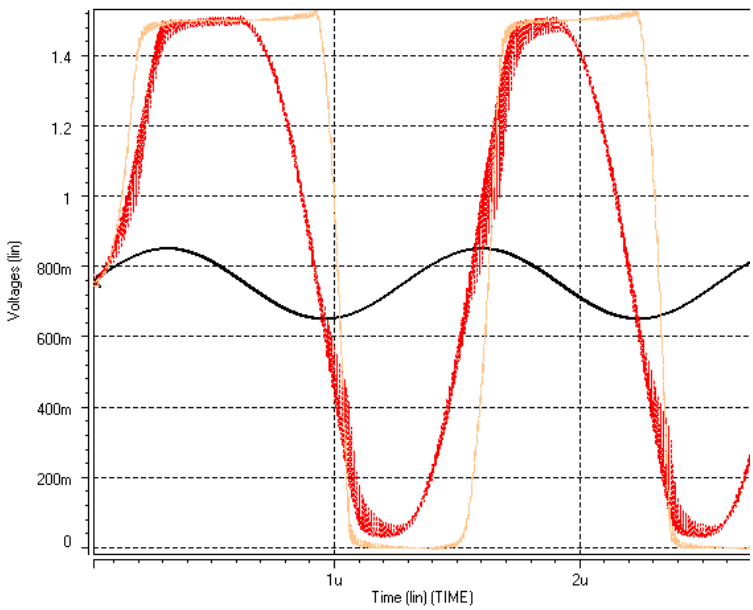

Figure 4.16. Second order integrator positive input and first and second integrator output

4.3. Histogram Based Power Analysis of the Second Order ΔΣ modulator

In order to see the power consumption of the circuit above in a ΔΣ loop, a quantizer and two DACs are included. There are two DACs because of the fully differential SC integrator. This feedback path forms a second order ΔΣ modulator which is shown in Figure 4.17 as a block diagram. The outputs of the second integrator are connected to a single-bit quantizer which is simply a comparator. When the clock signal is high, the circuit samples the input and changes its output values, and when the clock signal is low the circuit does not function. The quantizer gives 1.5 V and 0 V as outputs. The other component of the modulator is the DAC. Finally, the outputs of the DACs are connected to the nodes as shown in Figure 4.17. This completes the feedback path and the second order ΔΣ modulator.

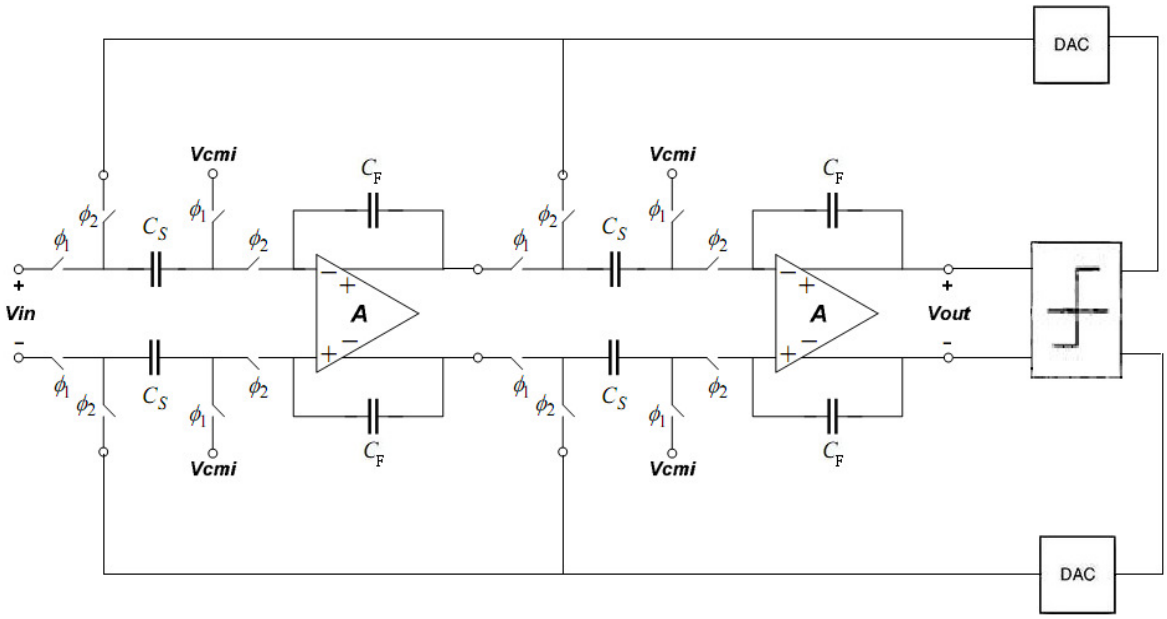

Figure 4.17. Block diagram of a second order ΔΣ modulator

The simulation results of the second order ΔΣ modulator is given below. The sampling and feedback capacitors of first integrator are chosen as 1 pF and 2 pF, respectively, whereas they are 2 pF and 1 pF in the second integrator. According to these capacitor values, the gains of the integrators are 0.5 and 1, respectively. Since the gain of the first integrator is 0.5, its output swing is reduced accordingly, while the gain of 2 for the second integrator compensates for the first integrator attenuation.

The second order ΔΣ modulator positive input, first integrator positive output, second integrator positive output and the positive DAC output are given in Figure 4.18. Again, the sampling rate in this circuit is same with the previous ones, that is OSR = 128.

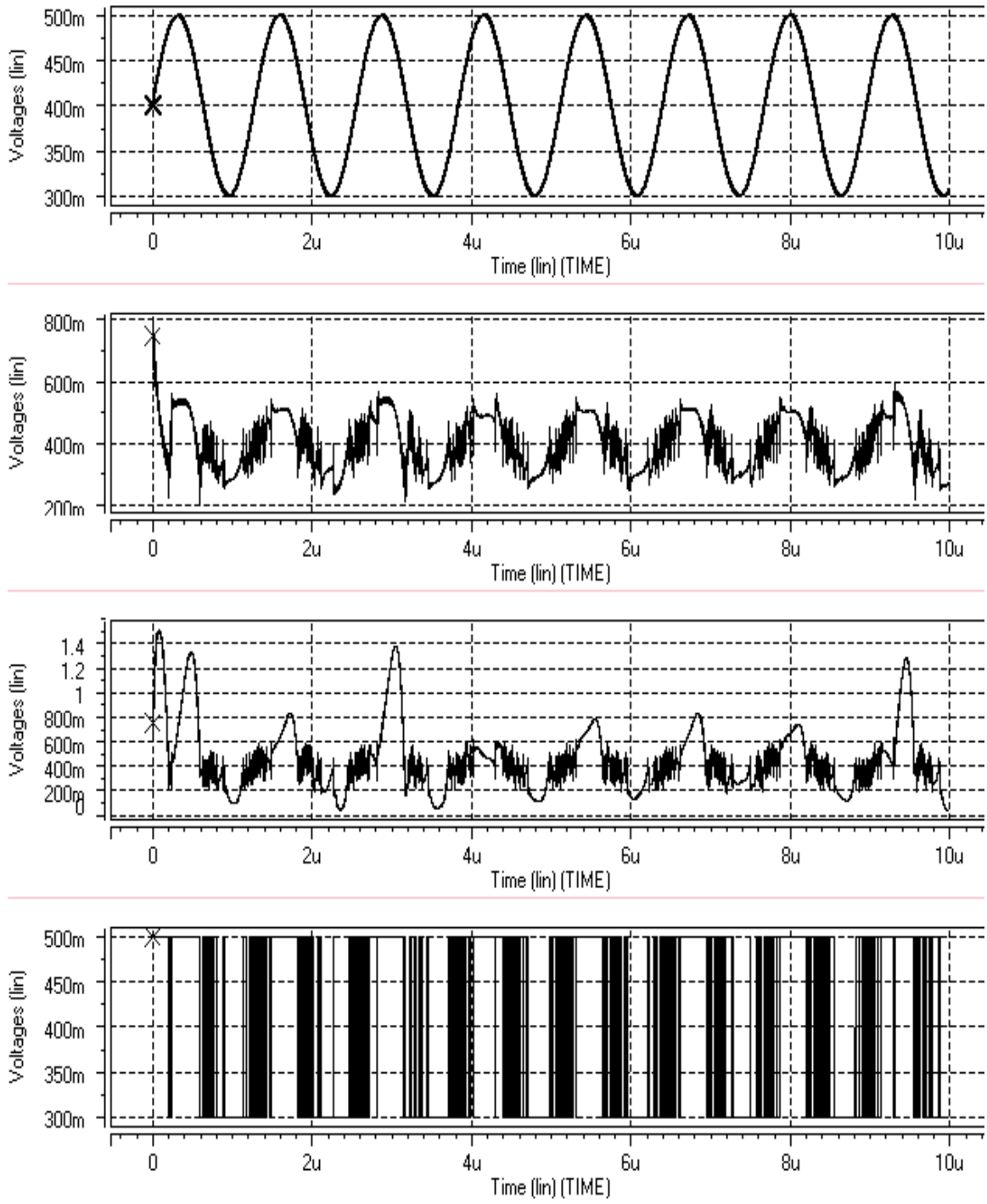

Figure 4.18. Simulation results of the second order ΔΣ modulator

With the feedback path included, the second circuit functions properly. This provides us to see the realistic power consumption. The static power dissipation of this circuit is measured to be 316 µW.

The input of the simulation in Figure 4.18 is sinusoidal. The effect of the input to the total power consumption can be observed by plotting the histograms of the first integrator output. The power consumption with sinusoidal input is simulated above and the power consumption is found as 316 µW. If triangular input is applied to the same system, the power consumption decreases to 309 µW. And, if a square wave input is applied, the power consumption decreases again and is measured to be 285 µW.

The histograms of the first integrator output are given in Figure 4.19, 4.20 and 4.21 when the inputs are sinusoidal, triangular and square wave, respectively. The histograms are obtained by using "HSPICE Toolbox for MATLAB". This toolbox is a collection of MATLAB routines that allows manipulating and viewing signals generated by HSPICE simulations [14].

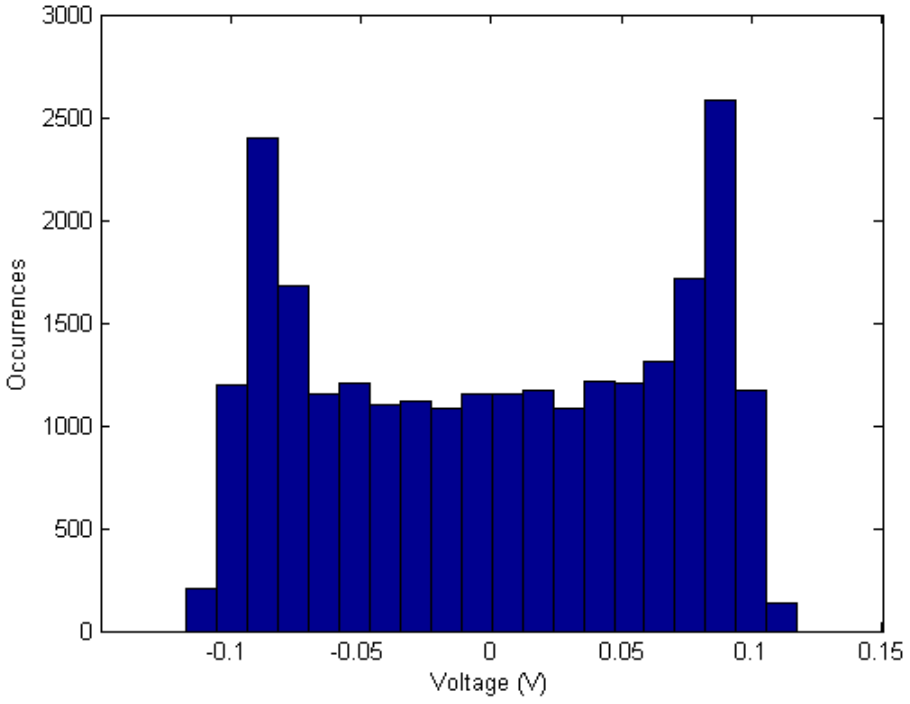

Figure 4.19. Histogram of the first integrator output when the input is sinusoidal

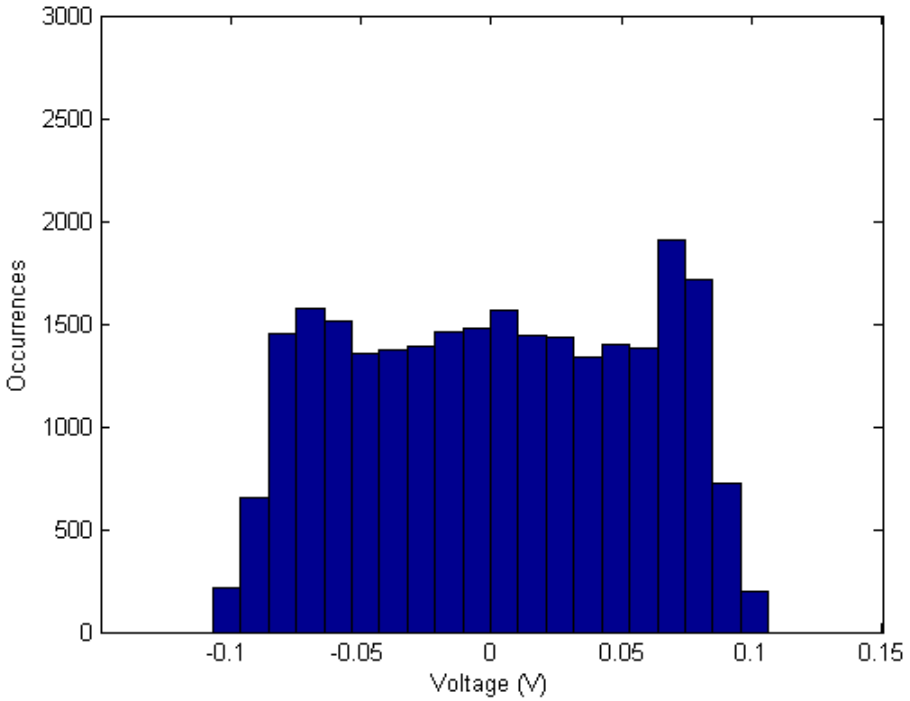

Figure 4.20. Histogram of the first integrator output when the input is triangular

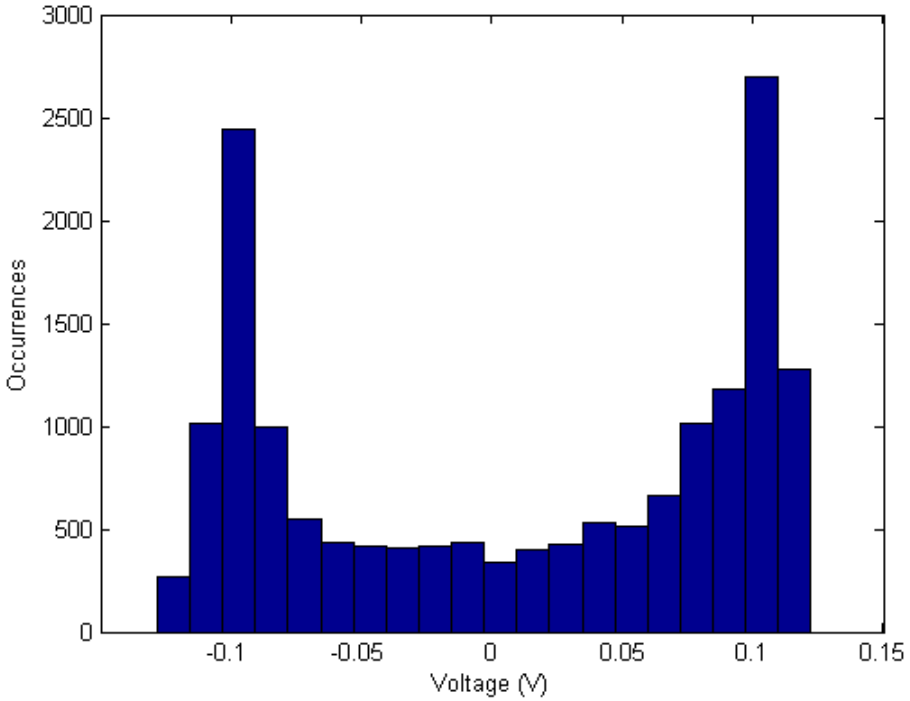

Figure 4.21. Histogram of the first integrator output when the input is square wave

The reason that $P_{sin} > P_{tri} > P_{squ}$ can be explained with the help of the histograms. As one can observe from the figures, the histogram of the first integrator output when the input is a square wave contains less occurrences which causes the power consumption to decrease eventually. However, the decrease in power consumption is not big; so, one can say that the shape of the input signal does not affect the total power consumption significantly.

5. POWER MODELING OF SWITCHED-CAPACITOR INTEGRATORS

In this chapter, power modeling of the switched-capacitor integrators that are used in ΔΣ modulators is presented. First, the power aspect of the design of ΔΣ modulators is treated and expressions for SC integrator power consumption are given. Then, the simulation results obtained from HSPICE simulations of the previous chapter are compared with the ones that are obtained from the power model. The comparison is performed by observing the change of power consumption with respect to the capacitance values in the SC integrator. And finally, after both results are compared, some examples which employ various second order ΔΣ modulator architectures and parameters are given, again looking at the change of power consumption in these circuits.

5.1. Expression for Switched-Capacitor Integrator Power Consumption

Some previous analysis in the literature assumes an infinite efficiency of the active part of the circuit and takes only the power that is dissipated when charging and discharging the functional capacitor into account. However, this assumption of no power consumption in the active circuitry yields a power consumption orders of magnitude below real implementations. Including a simple model for the active parts gives a more realistic result. This model is similar to [24] but the expression for SC integrator power consumption is developed from [10]. The settling process of an integrator is an exponential settling with a time constant τ that has a time dependent settling error ε_s of

$$\epsilon_s = e^{-t/\tau} = e^{-N_\tau} \tag{5.1}$$

The settling error is $\varepsilon_s = 2^{(-B)}$ for B bits of resolution and the number of necessary time constants (N_τ) is

$$N_\tau = \ln(2^B) = B\ln(2) \tag{5.2}$$

In a SC integrator, during the integration phase, the available time to settle is half a clock period T / 2 = N_τ. The time constant is determined by the transconductance g_m of the amplifier used in the SC integrator and the effective load capacitance $C_{L,eff}$,

$$\tau = \frac{C_{L,eff}}{g_m} \tag{5.3}$$

which leads to

$$g_{meff} = Bln(2)C_{L,eff}2f_S \tag{5.4}$$

Capacitance $C_{L,eff}$ is dependent on all the capacitors in the network and defined as:

$$C_{L,eff} = C_S + C_{CM} + C_{FB} + \frac{C_L + C_{CMS,eq}}{\mathcal{F}_{dc}} \tag{5.5}$$

$$\mathcal{F}_{dc} = \frac{C_{INT}}{C_S + C_{FM} + C_{CM} + C_{INT}} \tag{5.6}$$

In general, the capacitance $C_{L,eff}$ can be expressed as capacitance C_S of the sampling capacitor multiplied by an excess capacitance factor N_C,

$$C_{L,eff} = N_C C_S \tag{5.7}$$

C_S is determined by the integrated kT / C noise power

$$P_N = N_N \frac{kT}{C_S} \tag{5.8}$$

where N_N is the noise excess factor which includes noise sources.

The transconductance of a MOS transistor is expressed as

$$g_m = \frac{2I}{V_{ov}} \quad \text{with} \quad V_{ov} = V_{GS} - V_T \tag{5.9}$$

For a sinusoidal signal the maximum signal power can be expressed as,

$$P_S = \frac{V_S^2}{2} \tag{5.10}$$

and dynamic range is

$$DR^2 = \frac{P_S}{P_N} \tag{5.11}$$

The dynamic range can be defined as a function of bits of resolution B. The maximum signal power for a sinusoidal signal and for a step size of Δ is

$$P_S = \frac{1}{2}(2^B - 1)^2 \left(\frac{\Delta}{2}\right)^2 \tag{5.12}$$

and the random noise with unifom amplitude distribution between ±Δ / 2 is

$$P_N = \frac{1}{3}\left(\frac{\Delta}{2}\right)^2 \tag{5.13}$$

which leads to

$$DR^2 = \frac{3}{2}(2^B - 1)^2 \tag{5.14}$$

$$DR_{db} = 10\log(DR^2) = B \cdot 6dB + 1.76dB \tag{5.15}$$

where B is derived as

$$B = \frac{1}{2}\frac{\ln\left(\frac{2}{3}DR^2\right)}{\ln(2)} \tag{5.16}$$

Finally, by solving for the current I in equation (5.9) and multiplying it by the power supply voltage V_{DD}, an expression for the power is obtained as

$$P = N_N N_c kTV_{ov}V_{DD} \ln\left(\frac{2}{3}DR^2\right)\frac{DR^2}{P_S}BW \tag{5.17}$$

which shows that more power is required with the increasing dynamic range or bandwidth.

Equation (5.17) defines the power necessary to settle to an accuracy of B bits for an input signal with power P_S, but only including the g_{meff} of the amplifier. That means only the current of the input stage is included [10].

5.2. Comparison of the Power Model with the Real Implementations

The model given above is adapted to the implementation of the second order ΔΣ modulator built using class AB folded-cascode opamps. The effective load capacitance $C_{L,eff}$ given in equation (5.5) is modified according to the SC circuit used in the integrators. It is expressed as

$$C_{L,eff} = N_C C_S = \left(1 + \frac{(C_L)(C_S + C_F)}{C_S C_F}\right) C_S \tag{5.18}$$

The power consumption of the standard second order ΔΣ modulator was discussed in the previous chapter. Here, the HSPICE simulation results revealing the change of power consumption of these circuits with respect to the various capacitances in the circuit are given.

At first, the change of power dissipation with respect to the value of the load capacitance is observed. The values of the capacitances are changed using transient sweep analysis in HSPICE. The simulation output is given in Figure 5.1.

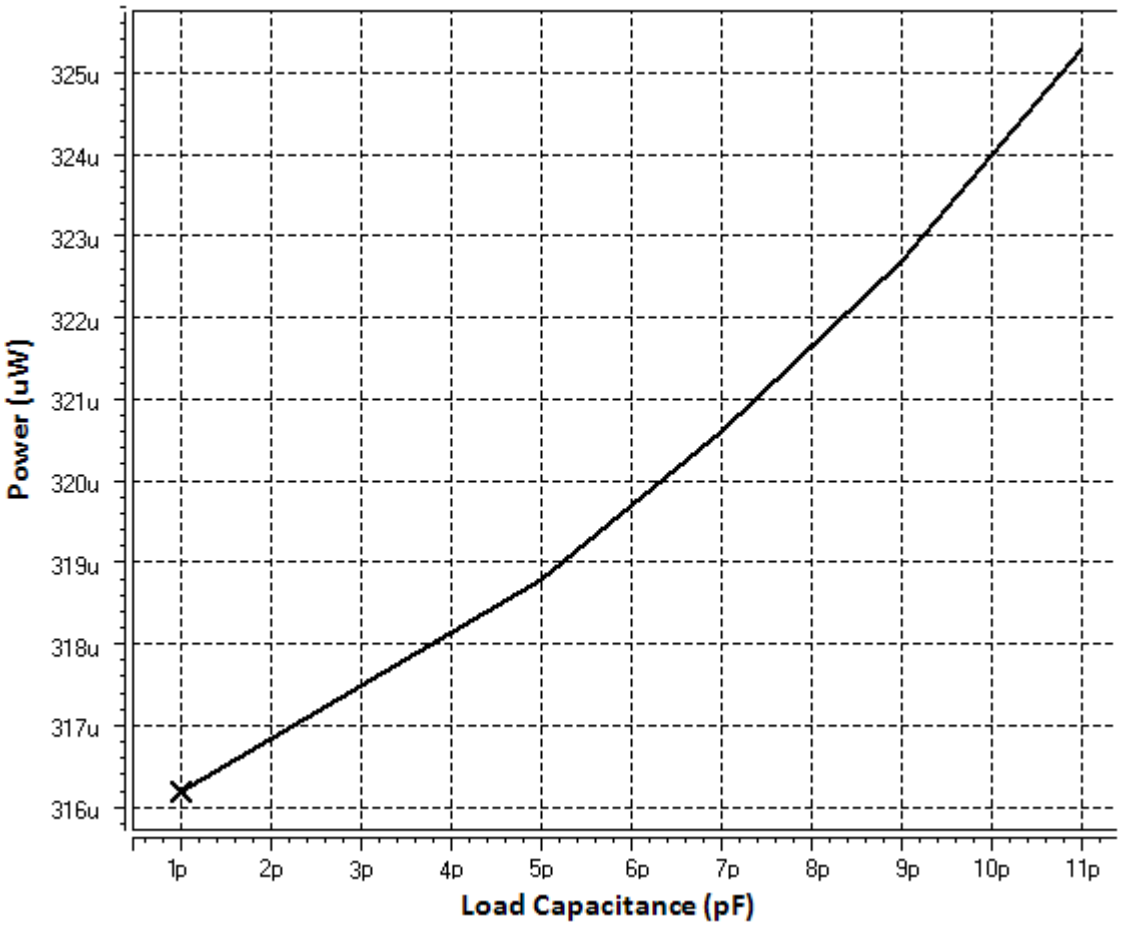

Figure 5.1. The change of the power consumption with respect to the load capacitances

As expected, the power of the circuit is increased with the increasing load capacitance. The value of the capacitance is swept from 1 to 11 pF. In this interval, the circuit does not malfunction. The values of the sampling and feedback capacitances are 1 pF and 2 pF, respectively.

Second, the change of power dissipation with respect to the value of the sampling capacitances in the circuit is given in Figure 5.2.

The power of the circuit is increased with the increasing sampling capacitances. The value of the capacitance is swept from 1 pF to 11 pF. Again, in this interval the circuit does not malfunction. The values of the feedback capacitances are 1 pF in this simulation and the load capacitances are chosen to be 3.5 pF.

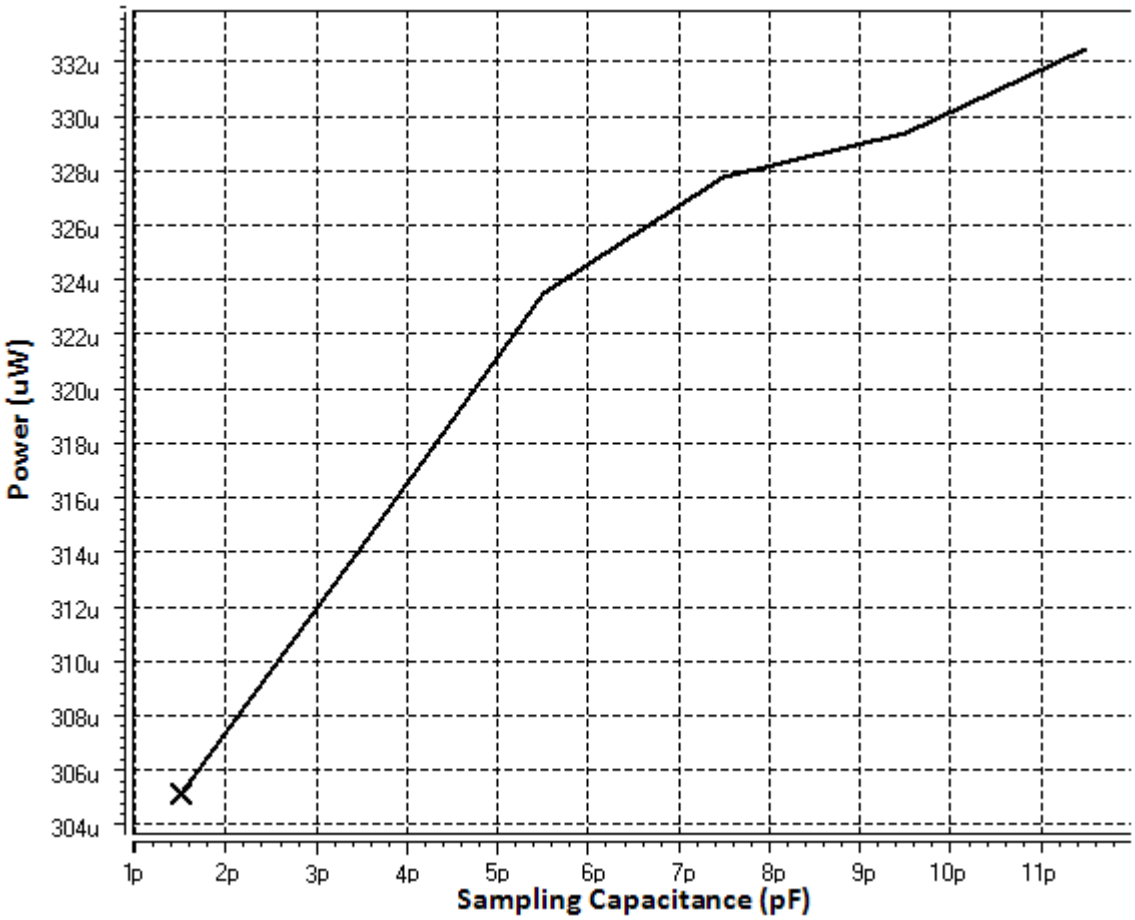

Figure 5.2. The change of the power consumption with respect to the sampling capacitances

Looking at the simulation results, it should be noted that the dynamic power dissipation of the circuit is very low with respect to the static power dissipation of the circuit. This has been emphasized in the previous chapters that the static power dissipation forms most of the total power dissipated in the circuit.

Now, having obtained the power consumption simulation results, they can be compared with the power model which is based on [10] as explained in the previous section.

The required parameters for the power model are shown in Table 5.1. The design automation tool in Chapter 3 is used to generate the second order ΔΣ modulator architectures which will be used in the power consumption simulations. Below there are comparative figures which show the HSPICE and MATLAB simulation results together.

Table 5.1. The parameters of the standard 2nd order modulator

Parameter	Value
f_S	100 MHz
V_{ov}	73.8 mV
Δ	1.5 V
V_S	100 mV

A netlist, containing the input and output nodes of the all possible path gains, integrators, adders, and noise blocks of a second order ΔΣ modulator shown in Figure 3.1, is given to the automatic architecture generator tool explained in Chapter 3. It takes the desired NTF and STF from the user and finds solutions.

Out of this solution set, the standard second order ΔΣ modulator shown in Figure 3.4 is selected to compare its power consumption with the real implementation. As given in Table 5.1 the sampling frequency is 100 MHz and the input is sinusoidal with peak amplitude of 100 mV.

Firstly, the comparison of the power dissipation with respect to the load capacitances is given in Figure 5.3. The values of the sampling and feedback capacitances are 1 pF and 2 pF, respectively which are the same with the ones of the simulation in Figure 5.1. The comparison of the HSPICE and MATLAB simulations are given together in Figure 5.3.

The power dissipation result obtained from the power model is slightly greater than the one of the real implementation. However, the increase of the power is alike in both of them proving that the power model developed is consistent with the real implementation.

The comparison of the power dissipation with respect to the sampling capacitances is given next. The values of the feedback and load capacitances are 1 pF and 3.5 pF, respectively which are the same with the ones of the simulation in Figure 5.2.

The comparison of the HSPICE and MATLAB simulations are given together in Figure 5.4.

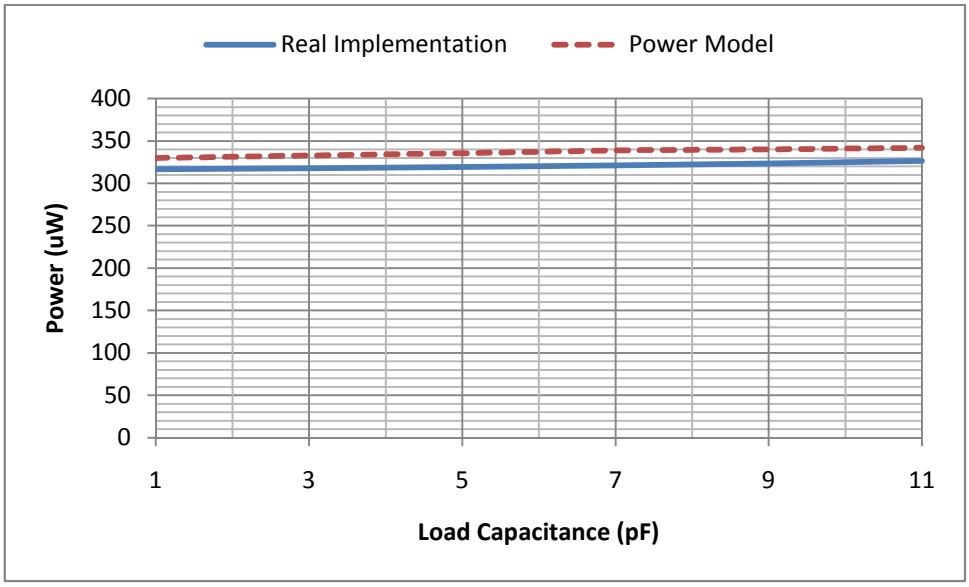

Figure 5.3. Comparison of the power consumption with respect to the load capacitances

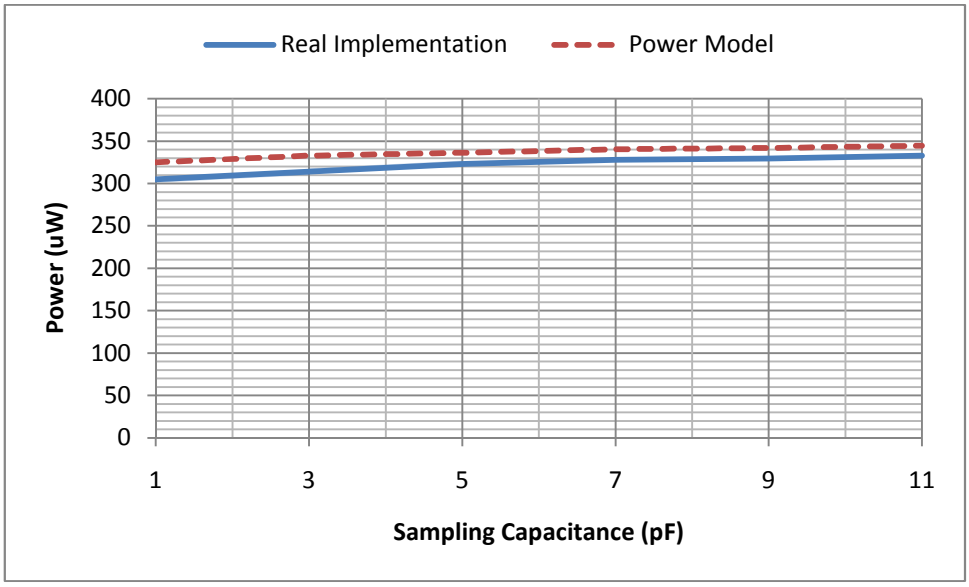

Figure 5.4. Comparison of the power consumption with respect to the sampling capacitances

Again, the power dissipation result obtained from the power model is slightly greater than the one of the real implementation. However, the increase of the power is alike in both of them again proving that the power model developed is consistent with the real implementation. In the next section, some more examples are given using the power model.

Most of the power is dissipated at the first stage because of the class A opamp. The HSPICE simulation results given below confirm this. Figure 5.5 and Figure 5.6 show the power consumption of the circuit after the power consumption of the first stage is subtracted from the total power.

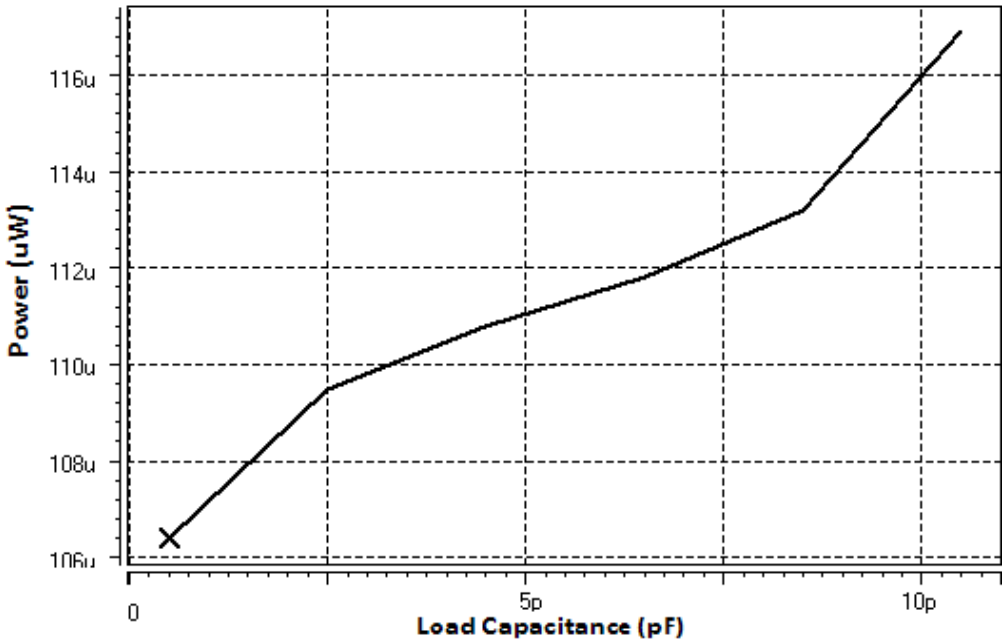

Figure 5.5. Power consumption vs. C_L after the power of the first stage subtracted

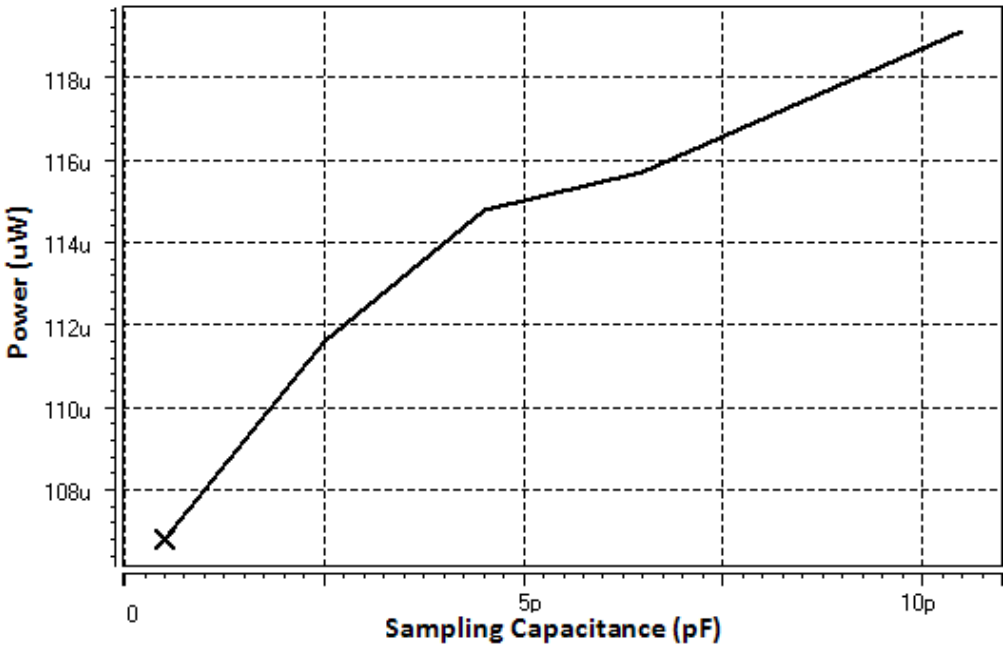

Figure 5.6. Power consumption vs. C_S after the power of the first stage subtracted

As one could observe from Figure 5.5 and Figure 5.6, most of the power is consumed at the first stage. By subtracting the power consumption of the first stage from the total power, the change of power with respect to the load and sampling capacitances is observed more clearly.

5.3. Examples Using Different Parameters and Architectures

The power model is shown to be consistent on the standard second order modulator using the parameters given in Table 5.1 in the previous section. In this section, some more examples are given which use the power model on some different ΔΣ modulator architectures and with different parameters.

Figure 5.7 shows the comparison of the power dissipation with respect to the load capacitances; but this time the sampling frequency is 50 MHz. The values of the sampling and feedback capacitances are 1 pF and 2 pF, respectively which are the same with the ones of the simulation in Figure 5.1.

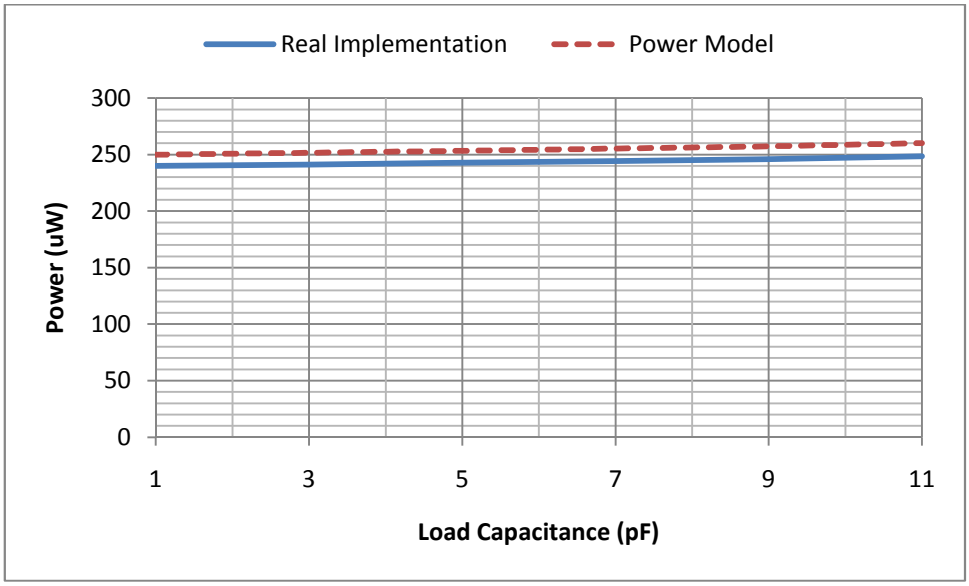

Figure 5.7. Power consumption vs. load capacitances (f_s = 50 MHz)

Figure 5.8 shows the comparison of the power dissipation with respect to the sampling capacitances and again the sampling frequency is 50 MHz.

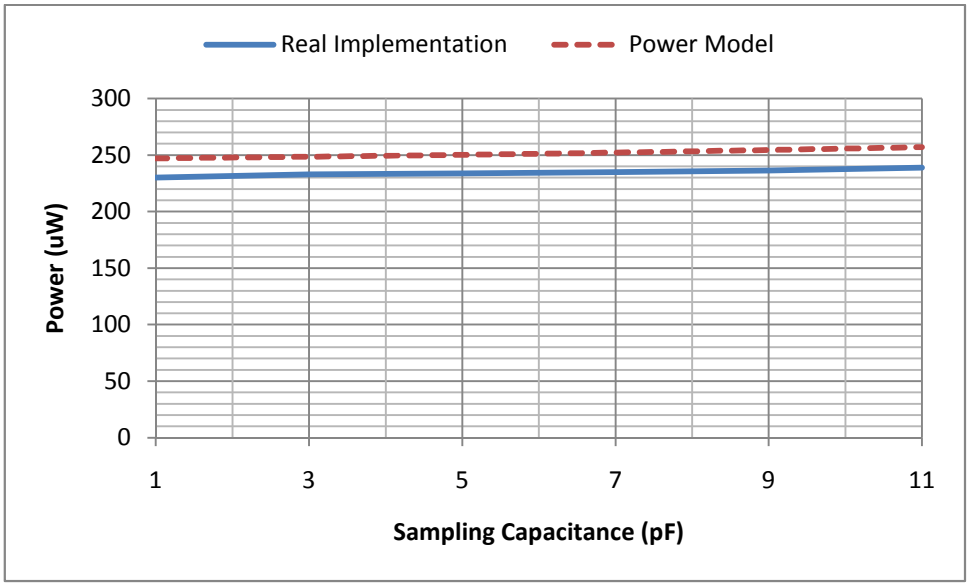

Figure 5.8. Power consumption vs. sampling capacitances (f_s = 50 MHz)

The power consumption is decreased in the case of 50 MHz but again the results are close to each other.

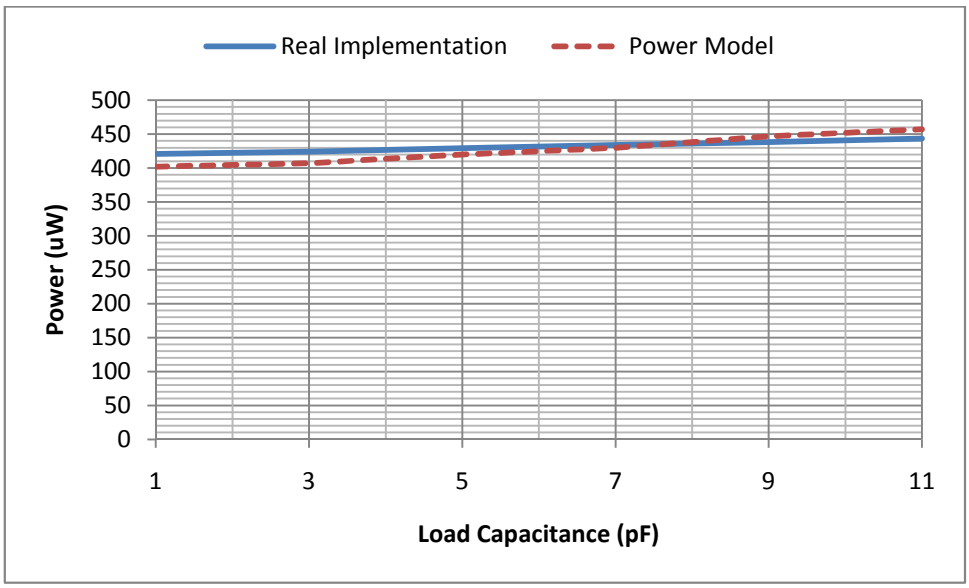

Figure 5.9. Power consumption vs. load capacitances (f_s = 200 MHz)

Figure 5.9 and 5.10 shows the comparison of the power dissipation with respect to the load and sampling capacitances. This time the sampling frequency is chosen to be 200 MHz.

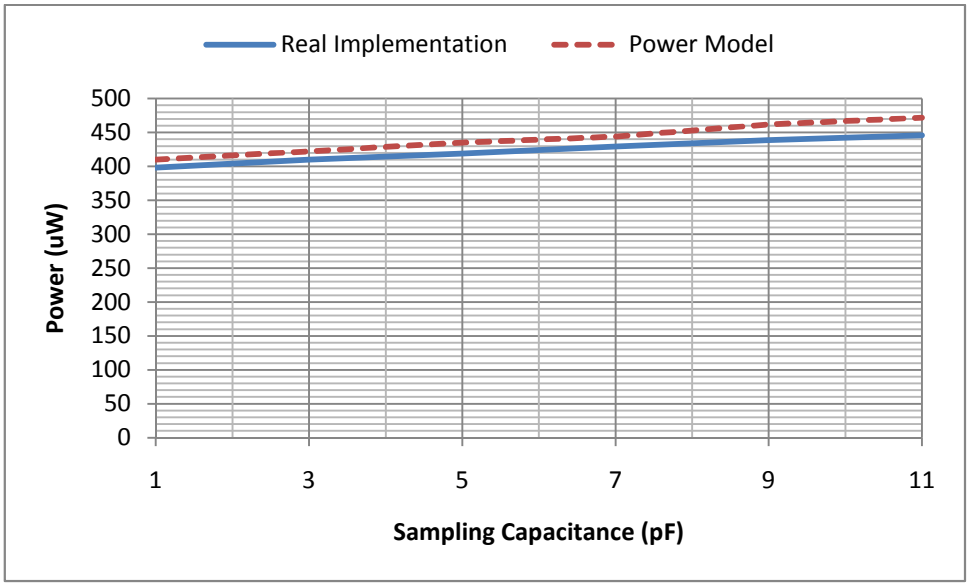

Figure 5.10. Power consumption vs. sampling capacitances (f_s = 200 MHz)

The power consumption is increased in the case of 200 MHz but again the results are close to each other.

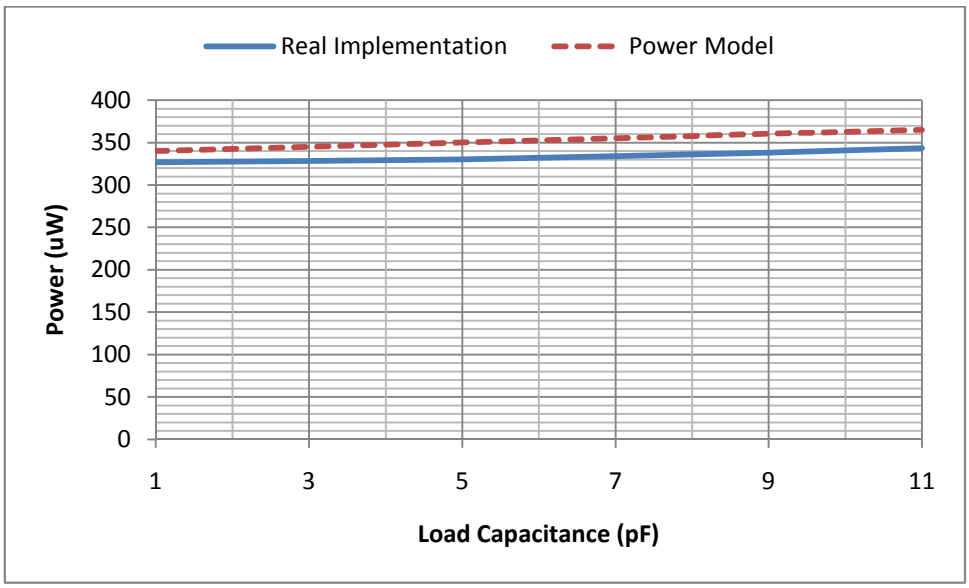

Figure 5.11. Power consumption vs. load capacitances (Vs = 200 mV)

Figure 5.11 and 5.12 shows the comparison of the power dissipation with respect to the load and sampling capacitances, respectively. This time the input amplitude is changed and chosen to be 200 mV.

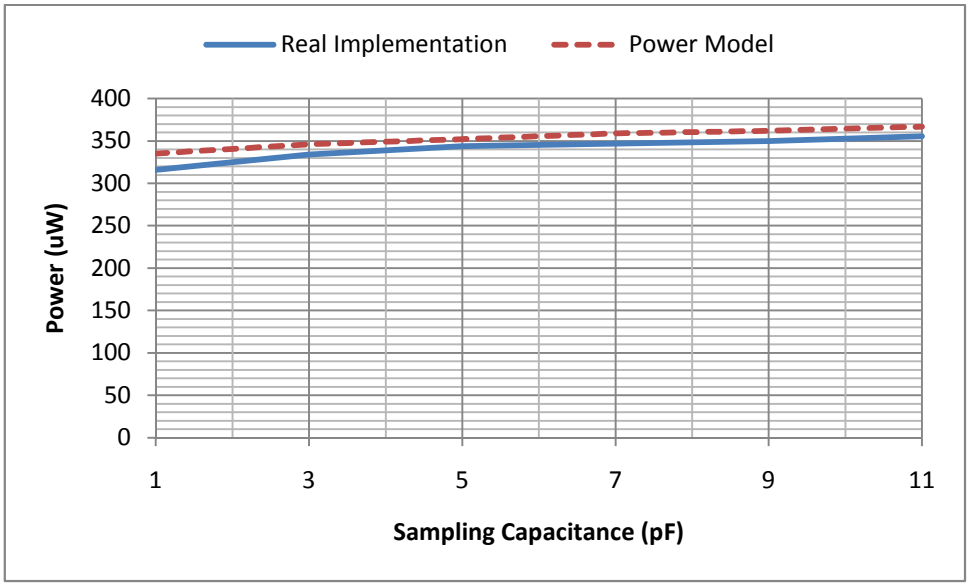

Figure 5.12. Power consumption vs. sampling capacitances (Vs = 200 mV)

In Figure 5.13 and 5.14 the input amplitude is chosen as 500 mV.

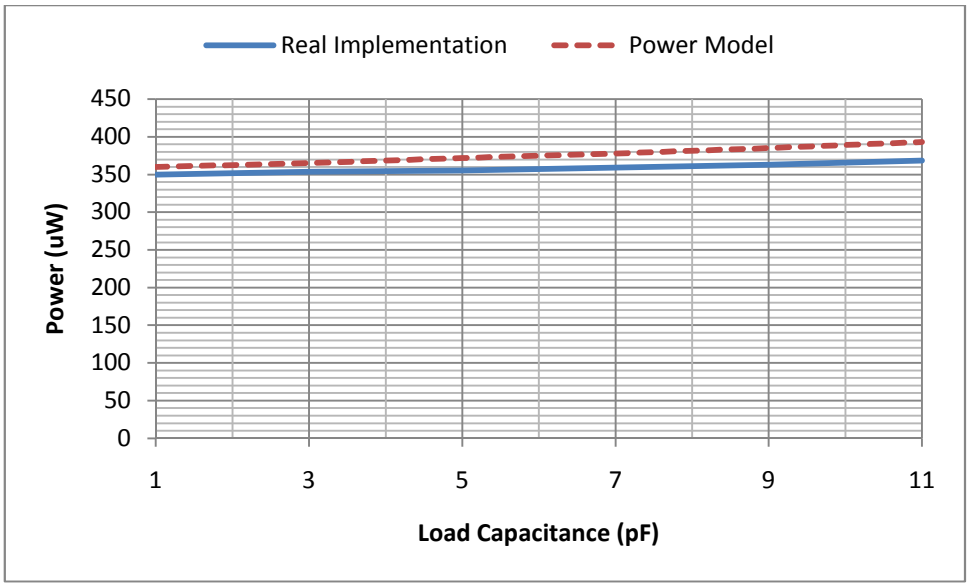

Figure 5.13. Power consumption vs. load capacitances (Vs = 500 mV)

The power consumption is increased in both of the cases of 200 mV and 500 mV, and the results obtained are consistent again.

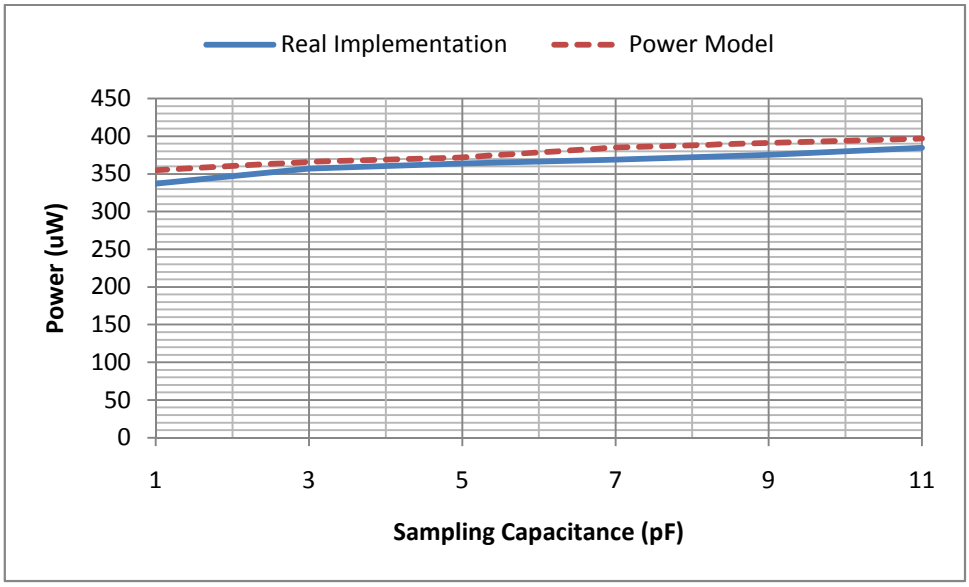

Figure 5.14. Power consumption vs. sampling capacitances (Vs = 500 mV)

The previous comparisons are made using the 2nd order standard modulator architecture given in Figure 5.15.

The power model is tested finally on the modulator architectures given in Figure 5.16 and 5.17. The real implementations of these architectures are realized in accordance with the details given in [9]. The paths in the architectures are realized using SC networks.

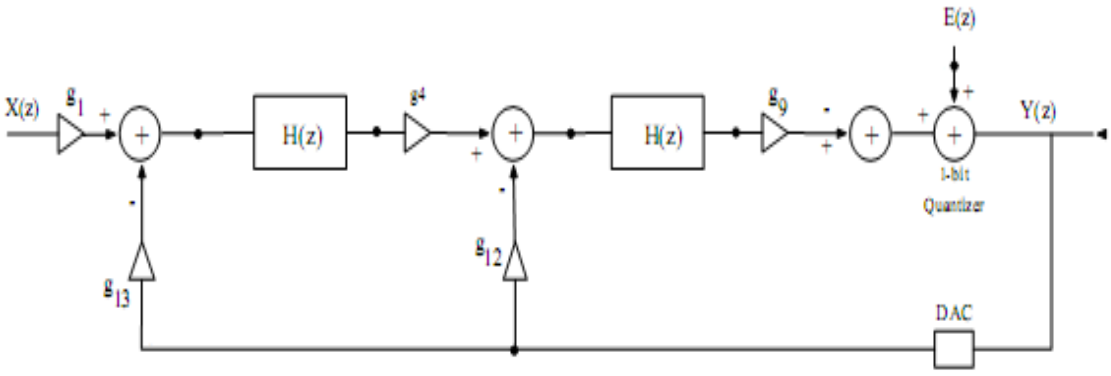

Figure 5.15. 2nd order standard modulator architecture

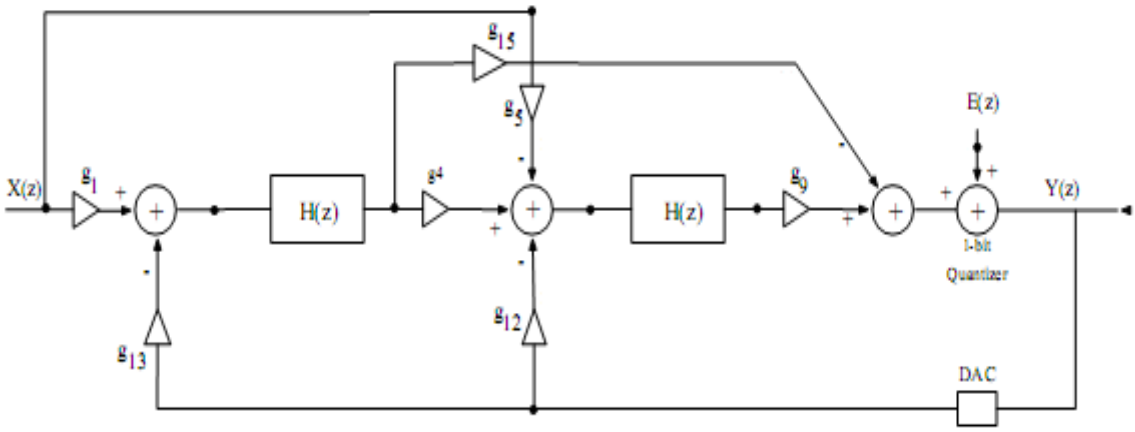

Figure 5.16. First architecture

Figure 5.17 shows the comparison of the power dissipation with respect to the load capacitances using the first architecture given in Figure 5.16.

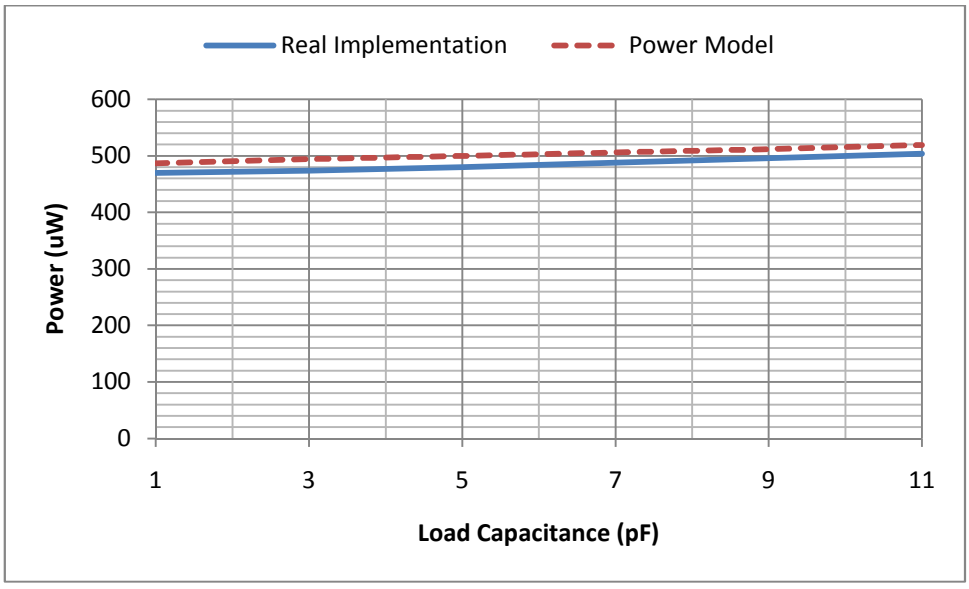

Figure 5.17. Power consumption vs. load capacitances (1st Architecture)

The power consumption is increased in the case of the first architecture and the results obtained are consistent again. Here, f_s = 100 MHz and Vs = 100 mV.

Figure 5.18 shows the comparison of the power dissipation with respect to the sampling capacitances using the first architecture given in Figure 5.16.

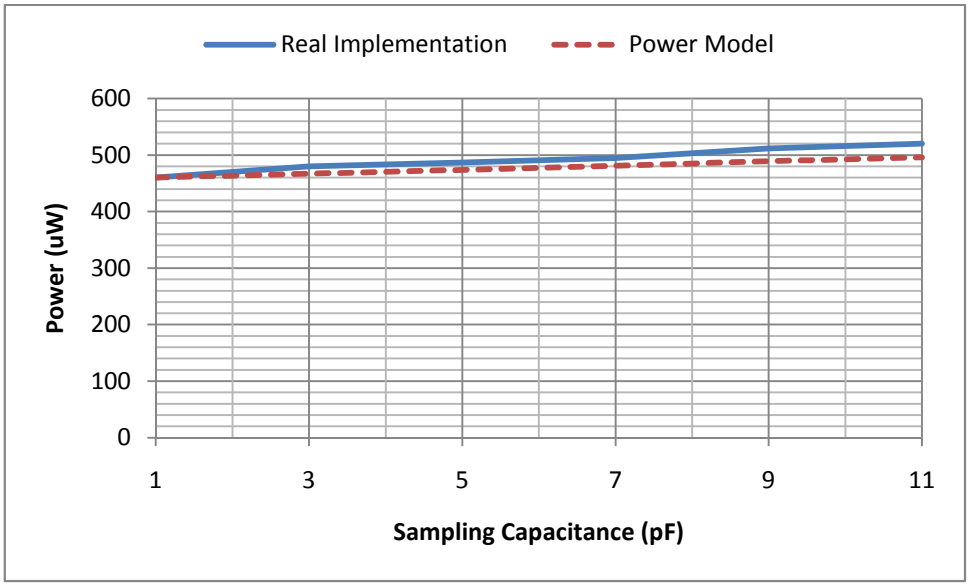

Figure 5.18. Power consumption vs. sampling capacitances (1st Architecture)

Figure 5.20 shows the comparison of the power dissipation with respect to the load capacitances using the second architecture given in Figure 5.19.

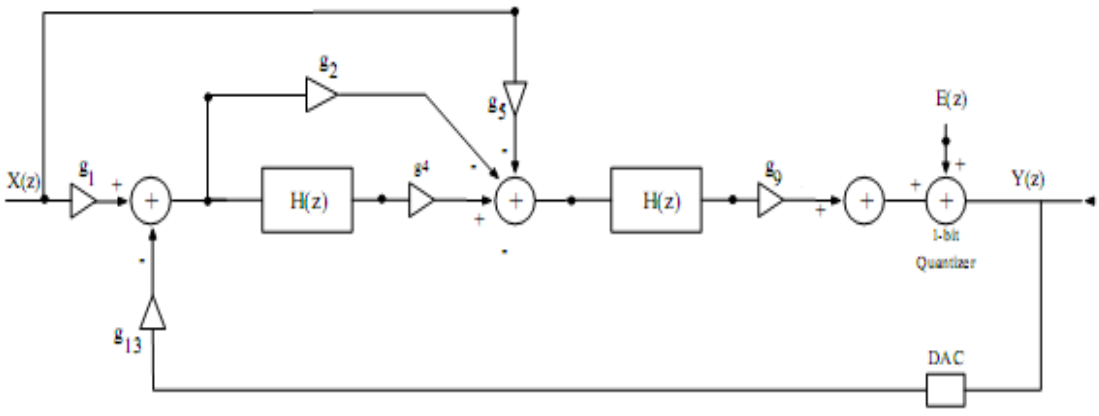

Figure 5.19. Second architecture

Finally, Figure 5.21 shows the comparison of the power dissipation with respect to the sampling capacitances using the second architecture given in Figure 5.19.

The results are consistent with each other again.

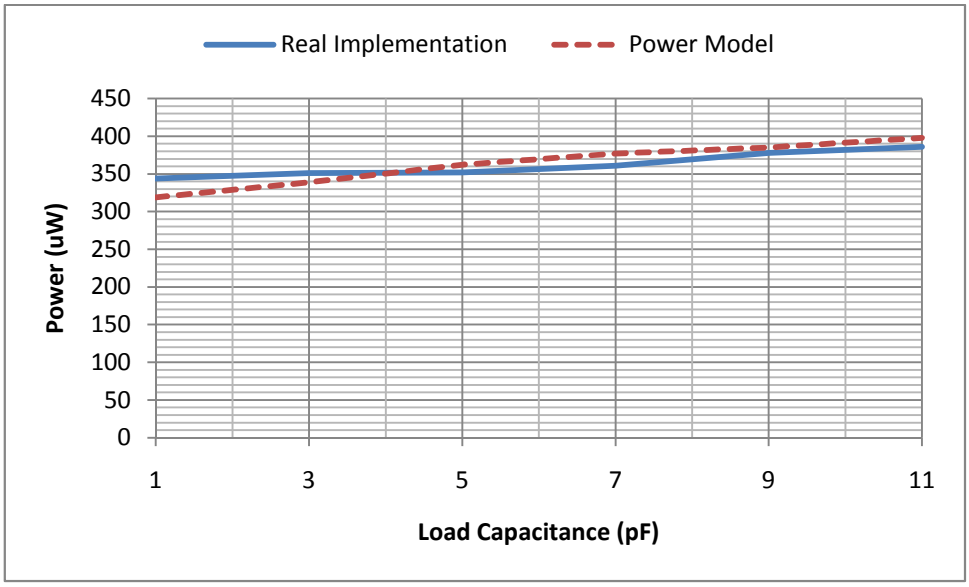

Figure 5.20. Power consumption vs. load capacitances (2nd Architecture)

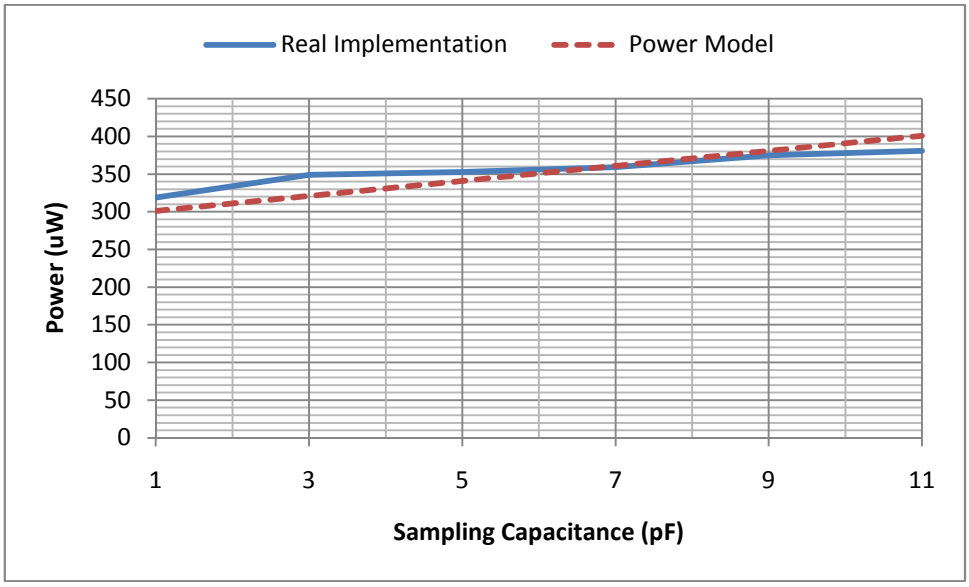

Figure 5.21. Power consumption vs. sampling capacitances (2nd Architecture)

6. CONCLUSIONS

In modern signal processing, conventional ADCs are not adequate to fully satisfy the high resolution and dynamic range requirements because of the limitations in their implementation. The sampling rate plays a significant role in achieving high resolution if it is higher than the Nyquist rate. This is called oversampling and the Delta-Sigma (ΔΣ) modulators are one of the most important electronic devices which employ oversampling. They have attracted the interest of many researchers recently.

Several different ΔΣ modulator architectures exist each one having its own advantages and drawbacks. Automated design of ΔΣ modulators is very important because of this variety in modulator architectures. An automatic architecture generator tool demonstrated in Chapter 3 generates quite a few topologies by taking the block diagram of the ΔΣ modulator as a netlist input file and the desired transfer functions from the user.

The implementations of sampled-data ΔΣ modulators are based on the Switched-Capacitor (SC) technique because of several reasons. First of all, the SC integrators are easily built as an integrated-circuit and they have high accuracy in determining the coefficients with capacitor ratios. In addition, the sampling rate does not change the value of these coefficients.

From the power consideration point of view, the most important part of a ΔΣ modulator is the SC integrator and the key component of an SC integrator is the operational amplifier it uses. Conventional class A operational amplifiers need a high dc current in order to achieve large slew-rate as well as high unity-gain bandwidth. Nevertheless, in class AB operational amplifiers a fast settling is achieved with low static power dissipation since the slew rate does not depend on the quiescent current. Regarding these, the power optimization of SC integrators is presented in Chapter 4. The class AB folded-cascode operational amplifiers reduce the power consumption drastically.

Having the power-optimized SC integrators, the second order ΔΣ modulator is built using them. Afterwards, a power model for SC integrators is introduced and the results of

the standard second-order ΔΣ modulator and some more examples using different architectures and parameters are compared with the real implementations. Consequently, the comparison proved the approach of the power model.

The power optimization and modeling of SC integrators together lead to a high quality data conversion at low power. However, the power optimization may not always be in the designer's interest because it is a trade-off with the settling performance. This situation can always be interchanged, for example by resizing the dimensions of the devices in the operational amplifier or by increasing the number of the output stages of it. For this reason, the power modeling provides the designer to easily decide how the design might flow before actually designing the circuit.

As a future work, the power model can be tested on higher order and cascade configurations after improving the tools given in Chapter 3. Also, power optimization can be further improved by designing a better operational amplifier which might have some other topology.

APPENDIX A: THE NETLIST OF THE SECOND ORDER ΔΣ MODULATOR WITH THE DESIGNED CLASS AB OPAMP

```
2nd Order Delta-Sigma Modulator with Class AB Opamp

.lib './mix018'  TT
.temp  27


**Opamp1

M1     2       in1p     1     1      pch     W=8u      L=0.18u
M2     3       in1n     1     1      pch     W=8u      L=0.18u

M3     2       vb1          ss     ss      nch     W=6u      L=0.18u
M4     3       vb1       ss     ss      nch     W=6u      L=0.18u

M5     out1n     vb2      2      ss      nch     W=4u      L=0.18u
M6     out1p     vb2      3      ss      nch     W=4u      L=0.18u

M7     out1n     vb3      6      dd2     pch     W=6u      L=0.18u
M8     out1p     vb3      7      dd2     pch     W=6u      L=0.18u

M9     6       vb4      dd2    dd2     pch     W=6u      L=0.18u
M10    7       vb4      dd2    dd2     pch     W=6u      L=0.18u

M11    1       vcm      dd2    dd2     pch     W=10u     L=0.20u



**********************************************************************
***
```

```
**SC Integrator1

gs1    vin+    im1     vcr   pwl(1) ph1  0   0.0v,100meg 1.5v,500
gs2    vin-    im2     vcr   pwl(1) ph1  0   0.0v,100meg 1.5v,500

gs3    im3     in1-    vcr   pwl(1) ph2  0   0.0v,100meg 1.5v,500
gs4    im4     in1+    vcr   pwl(1) ph2  0   0.0v,100meg 1.5v,500

gs5    im3     vcmi    vcr   pwl(1) ph1  0   0.0v,100meg 1.5v,500
gs6    im4     vcmi    vcr   pwl(1) ph1  0   0.0v,100meg 1.5v,500

gs7    im1     vcmp    vcr   pwl(1) ph2  0   0.0v,100meg 1.5v,500
gs8    im2     vcmn    vcr   pwl(1) ph2  0   0.0v,100meg 1.5v,500

Cs1    im1     im3     1p
Cs2    im2     im4     1p

Cf1    out1+   in1-    2p
Cf2    out1-   in1+    2p


*************************************************************************
***
**Opamp2


M1b    20      in2+    10    10    pch    W=8u     L=0.18u
M2b    30      in2-    10    10    pch    W=8u     L=0.18u

M3b    20      40      ss    ss    nch    W=6u     L=0.18u
M4b    30      50      ss    ss    nch    W=6u     L=0.18u

M5b    out-    vb2     20    ss    nch    W=4u     L=0.18u
```

```
M6b    out+    vb2     30    ss    nch    W=4u     L=0.18u

M7b    out-    vb3     60    dd    pch    W=6u     L=0.18u
M8b    out+    vb3     70    dd    pch    W=6u     L=0.18u

M9b    60      80      dd    dd    pch    W=6u     L=0.18u
M10b   70      90      dd    dd    pch    W=6u     L=0.18u

M11b   10      vcm     dd    dd    pch    W=10u    L=0.20u


Mr1b   40      40      vb1   vb1   pch    W=1.0u   L=2u
Mr2b   50      50      vb1   vb1   pch    W=1.0u   L=2u
Mr3b   80      80      vb4   vb4   pch    W=1.0u   L=2u
Mr4b   90      90      vb4   vb4   pch    W=1.0u   L=2u


Cb11b in2+     80      0.2p
Cb12b in2+     40      0.2p
Cb13b in2-     90      0.2p
Cb14b in2-     50      0.2p
**********************************************************************
***
*SC Integrator2

gs9    out1+   im5     vcr   pwl(1)  ph1   0   0.0v,100meg  1.5v,500
gs10   out1-   im6     vcr   pwl(1)  ph1   0   0.0v,100meg  1.5v,500

gs11   im7     in2-    vcr   pwl(1)  ph2   0   0.0v,100meg  1.5v,500
gs12   im8     in2+    vcr   pwl(1)  ph2   0   0.0v,100meg  1.5v,500

gs13   im7     vcmi    vcr   pwl(1)  ph1   0   0.0v,100meg  1.5v,500
gs14   im8     vcmi    vcr   pwl(1)  ph1   0   0.0v,100meg  1.5v,500
```

```
gs15    im5     vcmp     vcr    pwl(1)  ph2   0    0.0v,100meg  1.5v,500
gs16    im6     vcmn     vcr    pwl(1)  ph2   0    0.0v,100meg  1.5v,500

Cs3     im5     im7      1p
Cs4     im6     im8      1p

Cf3     out+    in2-     2p
Cf4     out-    in2+     2p

*********************************************************************************
***
*DAC


E1 vcmp vcmi dacp vcmi max=0.1 min=-0.1 100k
E2 vcmn vcmi dacn vcmi max=0.1 min=-0.1 100k


gs20    out+    dacp     vcr    pwl(1)  ph1   0    0.0v,100meg  1.5v,5
gs21    out-    dacn     vcr    pwl(1)  ph1   0    0.0v,100meg  1.5v,5
csw1    dacp    ss       1p
csw2    dacn    ss       1p

Clp     out+    ss       3.5p
Cln     out-    ss       3.5p

*********************************************************************************
***

vvb1    vb1     0        dc 550m
vvb2    vb2     0        dc 817m
vvb3    vb3     0        dc 545m
vvb4    vb4     0        dc 890m
```

```
vvcm     vcm     0       dc 870m

vdd2     dd2      0          dc       1.5
vdd      dd       0       dc     1.5
vss      ss       0       dc     0
vcmi     vcmi     0       dc     0.4

vip      vin+     im3p    sin(0  0.1 0.78125Meg 0.0u)
vin      vin-     im3n    sin(0 -0.1 0.78125Meg 0.0u)
vin1     im3p     0       dc=0.4
vin2     im3n     0       dc=0.4


vph1      ph1      0     pulse(0     1.5    0        0.5n  0.5n   4n    10n)
vph2      ph2      0     pulse(0     1.5    5n       0.5n  0.5n   4n    10n)

*********************************************************************************
***

.end
```

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