FAST AND HIGH EFFICIENCY HYSTERETIC BUCK CONVERTER

by

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ABSTRACT

FAST AND HIGH EFFICIENCY HYSTERETIC BUCK CONVERTER

Mobile battery powered platforms have to focus on high efficiency to increase their on times. In addition to high efficiency, their components have to work under a varying battery voltage to obtain stable operation. To answer these needs switching DC-DC converters are used to produce a stable voltage output needed by mobile platforms and its peripherals with high efficiency to increase standby time. Also as a main design target, the converter should respond to the load variation as fast as possible to produce a reliable output voltage. Hysteretic converters are known to have fast load variation responses and a hysteretic converter scheme is utilized for the design in this thesis. Another important target of mobile platforms is that to decrease bill of materials as much as possible to reduce total price of the device in a challenging competitive market condition. This thesis introduces a hysteretic buck converter to produce two different output voltages utilizing a single inductor. Also, using a single inductor, the cost of one inductor is reduced from the total budget. However, to produce two separate voltage outputs with a single inductor has a drawback of cross talk between outputs which is called cross regulation. This single inductor double output (SIDO) hysteretic buck converter focuses mainly on increasing efficiency and reducing the cross regulation for better regulation of the outputs. After a brief description of the DC-DC converters, the designed SIDO hysteretic buck converter and its sub blocks are explained in detail. Finally, top level post-layout simulation results are compared with state of art SIDO buck converters.

ÖZET

HIZLI VE YÜKSEK VERİMLİ HİSTERİSİSLİ BUCK ÇEVİRİCİ

Bataryalı mobil platformlar cihazın açık kalma süresini uzatmak için yüksek verimliliğe odaklanmak zorundadır. Yüksek verimliliğe ek olarak içerisindeki yapıların değişen batarya gerilimiyle düzgün bir şekilde calışması gerekmektedir. Hem yüksek verimlilik hem de düzenli çıkış gerilimi sunmasından dolayı DC-DC çeviriciler bu ihtiyaçları karşılayarak uzun batarya çalışma süresi sunarlar. Önemli bir tasarım hedefi de çeviricinin çıkış yük değişimine tepkisinin hızlı olması gerekmektedir. Histeresisli dönüştürücüler çıkış yük değişimine hızlı cevap vermesinden dolayı histeresisli dönüştürücü mimarisi kullanılmıştır. Mobil platformlar için önemli bir diğer nokta ise rekabetin ön planda olduğu bir pazarda bileşen sayısının mümkün olduğunca azaltılmasıdır. Bu tez, tek endüktör iki çıkışlı histeresisli bir DC-DC çevirici yapısını anlatmaktadır. Ayrıca, tek bir endüktör kullanılarak mobil cihazın üretim maliyeti de azaltılmış olur. Ancak, tek bir endüktörle iki çıkış sunmanın en büyük problemi iki çıkış geriliminin bir birbirini bozacak şekilde etkilemesidir. Bu histeresisli tek endüktörlü çift çıkışlı DC-DC çevirici, iki çıkışın birbirini etkilemesini azaltmaya yoğunlaşarak aynı zamanda yüksek bir verimlilik amaçlamaktadır. Tezin başlangıcında var olan DC-DC çevirici yapıları anlatılarak tasarlanan çeviricinin iç blokları ayrıntılı bir şekilde sunulmuştur. Son bölümde ise serim sonu benzetim sonuçları şimdiye kadar yapılan diğer çalışmalarla karşılaştırılmıştır.

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LIST OF SYMBOLS

C_{out}	Output Capacitor
D	Duty cycle
f_s	Switching frequency
kHz	Kilo Hertz frequency unit
M	Input to Output Voltage Conversion ratio
MHz	Mega Hertz frequency unit
V_{in}	Input Voltage
V_{out}	Output Voltage
T	Temperature

LIST OF ACRONYMS/ABBREVIATIONS

CCM	Continuous Conduction Mode
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DCM	Discontinuous Conduction Mode
DLL	Delay Lock Loop
EMI	Electro Magnetic Interference
FOM	Figure of Merit
IC	Integrated Circuit
NMOS	N type Metal Oxide Semiconductor
OPAMP	Operational Amplifier
PLL	Phase Lock Loop
PMOS	P type Metal Oxide Semiconductor
PSR	Power Supply Rejection
PVT	Process Voltage Temperature
SIDO	Single Inductor Double Output
SIMO	Single Inductor Multiple Output

1. INTRODUCTION

1.1. Motivation and Methodology

DC-DC converters have become the dominant voltage converter architecture due to increasing efficiency requirements of mobile platforms to increase the battery life time. Low drop out (LDO) architecture is another option for producing a stable voltage output from a variable supply voltage; however, there is a constant voltage drop at the output switch device which reduces efficiency substantially. DC-DC converters use the inductor as a voltage to current converter and then as a current to voltage converter, achieving efficiency figures above 90 %. Furthermore, there is no static voltage drop unlike LDOs. Thus, DC-DC converters are used in almost every mobile platform due to this widespread use and different requirements. Every architecture has pros and cons from the control and load regulation point of view. Voltage mode converters are known to be slow for load response with low load regulation performance, whereas current mode architectures have a relatively fast load response with better load regulation performance. Hysteretic converter (even being voltage mode control) has a fast load response since waiting for a synchronization clock is not required. Thus, the hysteretic converter architecture can be used to design a buck converter which has a fast load response.

Another important requirement for mobile applications is to decrease the bill of materials as much as possible. Single input double output (SIDO) and single input multiple output (SIMO) architectures are attractive from this point of view as they reduce the number of inductors. In these architectures, the same inductor is used to regulate two or more outputs. The main drawback of using the same inductor for more than one output is, that the design becomes complicated and the load regulation of one output can affect the other output which is called cross regulation. Thus, SIDO and SIMO architectures generally suffer from cross regulation which results in decreasing the regulation control of outputs. A SIDO architecture offering improved cross-regulation is desirable due to reduced bill of materials.

To design a SIDO hysteretic buck converter a single output hysteretic buck converter is built initially with sub blocks which incorporate ideal opamps, comparators and ideal digital gates. Then, this model hysteretic converter is simulated for different circuit parameters such as different inductor and output capacitor values to understand the behavior of the converter. Then, this single output hysteretic buck converter is changed to a SIDO buck converter. Similarly, simulations have been carried out to understand the behavior of the SIDO hysteretic buck converter and simulation results pointed that cross regulation becomes the dominant issue to be dealt with. Various solutions have been tried like changing the hysteresis dynamically and adding current feedback inside the control loop. However, cross regulation performance has not improved much with these solutions. Then the delay lock loop (DLL) based idea has been implemented and it has presented promising results improving the cross regulation with slow load performance. Then, a load balance algorithm was developed using a frequency counter to speed up the load response while accommodating the delay lock to fine tune the regulation. Then, each block which was built with ideal elements was designed using actual transistor based schematics. Due to the non idealities from actual transistor based designs, some challenges such as output voltage comparator delay were encountered. Solutions like faster comparators were implemented. Another issue was having a kickback due to main output voltage comparators on the DAC outputs and this issue was solved by adding a RC filter at the outputs of the DAC blocks.

1.2. Buck Converter

Buck converters are used to down convert a DC supply voltage to a DC output voltage with the help of a control mechanism to produce a stable voltage level even for different load conditions. This control can be done by directly measuring the output voltage and regulating it by comparing it with a target voltage and modifying the duty cycle to reach that target voltage (voltage control mode), or by indirectly controlling the inductor current (current control mode). Voltage mode control compared to current mode is slower for load variation response; and also its DC (static) regulation is not as good as current mode control. Both control modes also have a variety of different

control mechanisms. In its most simple form, a buck converter can be formed by two switches (one to supply connection and one to ground connection), one inductor, one output capacitor and a controller that controls the on and off of the two switches. Figure 1.1 depicts the simplified buck converter diagram with the load being modeled by a current source.

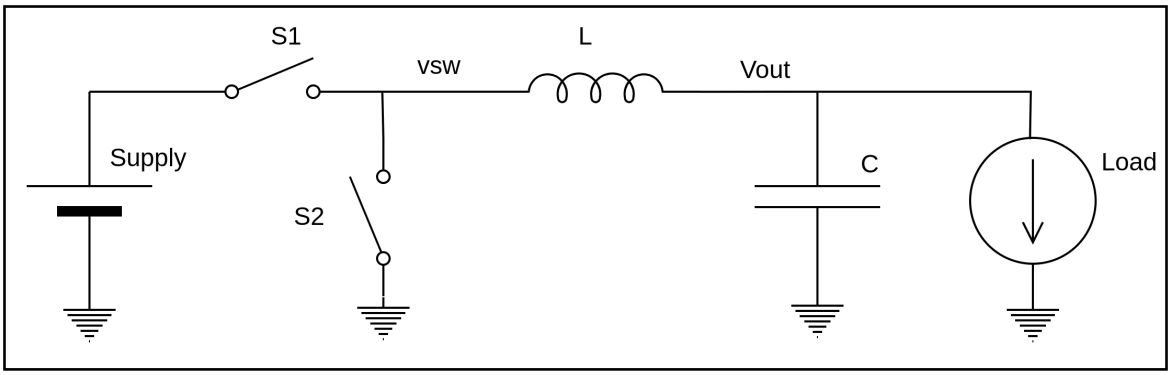

Figure 1.1. Buck Converter simplified circuit diagram.

To understand the functionality of a buck converter, mathematical expressions should be derived from the physical behavior. First, assume that output current load demand is high enough to prevent the buck converter inductor current from reaching 0A. The inductor conducting current being either by connected to the supply or to ground is called continuous conduction mode (CCM). Figure 1.2 shows the inductor current for CCM operation. The other operation mode is called discontinuous conduction mode (DCM). In DCM mode, load current is relatively low such that, inductor current can reach to 0A and output load can still be regulated by the inductor. Figure 1.3 shows the inductor current for DCM operation. [1] gives detailed mathematical expressions about the buck converter behavior. Some expressions to be used in this thesis will be derived from the detailed calculations given in [1].

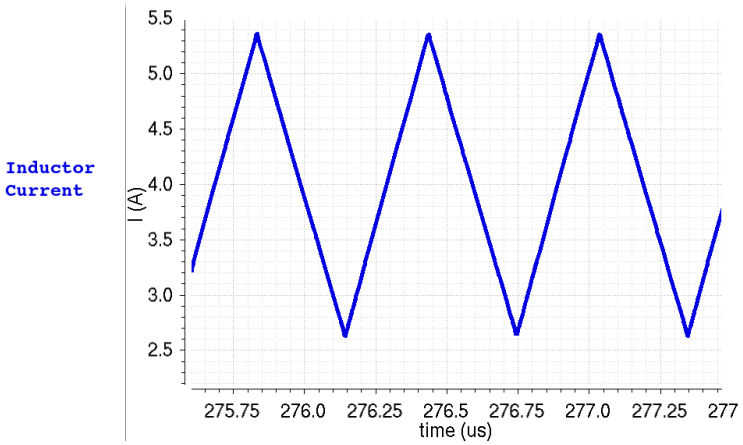

Figure 1.2. Inductor Current at CCM operation.

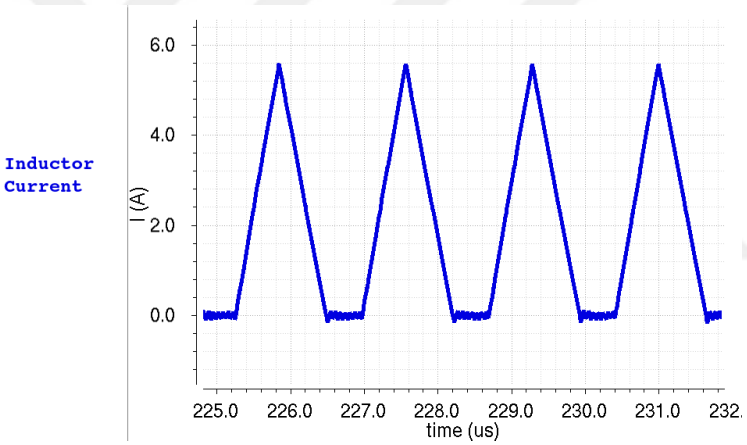

Figure 1.3. Inductor Current at DCM operation.

The main inductor equation is expressed as

$$\triangle V = L\frac{\triangle I}{\triangle t}, \tag{1.1}$$

both for charging (magnetizing) and discharging (demagnetizing) of the inductor current. It can be arranged as

$$\triangle V \triangle t = L \triangle I, \tag{1.2}$$

which is another representation of the same equation that will be used later. To find the output voltage to input voltage ratio, equation can be rearranged as

$$V_{in} - V_{out} = L\frac{I_{peak}}{DT_{sw}} \tag{1.3}$$

$$V_{out} = L\frac{I_{peak}}{(1-D)T_{sw}} \tag{1.4}$$

$$(D(V_{in} - V_{out})T_{sw} - V_{out}(1-D)T_{sw})\frac{1}{T_{sw}} = 0 \tag{1.5}$$

$$M = D = \frac{V_{out}}{V_{in}} \tag{1.6}$$

This main inductor equation is used to understand the switching converters. Assume that the inductor is working at the borderline of the CCM and DCM which means inductor minimum current is 0A and the current reaches 0A, the inductor immediately charges from the supply. Since it is charging or discharging all the time; switching frequency and period relation can be written as F_{sw}=$1/T_{sw}$. When the inductor is charging from the supply, the inductor equation can be written as in (1.3). This equation also shows that the input supply and output voltage relation defines the inductor charging slope. For instance, the supply voltage being much higher than the output voltage results a very sharp inductor charging slope.

For DCM operation, output to input voltage conversion ratio is given as

$$M = \frac{2}{1 + \sqrt{1 + \frac{8L}{D^2 R T_{sw}}}}, \tag{1.7}$$

more detailed information about this derivation can be found in [1].

D is the duty cycle of the inductor charged from the supply and $1 - D$ is the inductor discharging duty cycle. When the inductor is discharging to the output, (1.4)

can be written. Inductor discharging equation also shows that when the output voltage is high inductor discharging slope becomes sharper.

The change in current in the positive and negative directions must be same as shown in (1.3) and (1.4). The same applies to the product (1.2). Arranging (1.2), (1.3) and (1.4) gives (1.5) which can be simplified to find a duty cycle relation with supply and output voltage as (1.6). This equation shows that inductor charging duty cycle is related to only supply and output voltage. M is the conversion ratio, which is the output voltage divided by the input voltage. For CCM operation, the conversion ratio (M) is equal to the duty cycle (D).

$$R_{transition} = 2F_{sw}L\frac{V_{in}}{V_{in} - V_{out}} \tag{1.8}$$

$$I_{transition} = \frac{V_{out}}{R_{transition}} \tag{1.9}$$

The point that at which the buck converter changes mode between CCM and DCM is also important. Assuming the borderline condition with inductor minimum current being 0A and by equating DCM and CCM equations, the load resistor at the transition point can be calculated. (1.8) is obtained from the DCM and CCM equations. $R_{transition}$ is the transition resistor value and (1.9) shows $I_{transition}$ as the transition load current to change mode between DCM to CCM and vice versa. Similar approach can be applied to find the inductor value for transition, as well.

1.3. Boost Converter

Boost converters are used to increase the output voltage to higher values than its supply voltage. Similar to buck converters, their control mode can be voltage control mode or current control mode. Figure 1.4 demonstrates the simplified boost converter circuit diagram including the load current. Initially, S1 switch turns on and charges the inductor through the supply voltage. At the next cycle, S1 turns off and S2 turns on. The output voltage is the sum of the supply voltage and the inductor voltage. This way the output voltage will go to higher than the supply voltage.

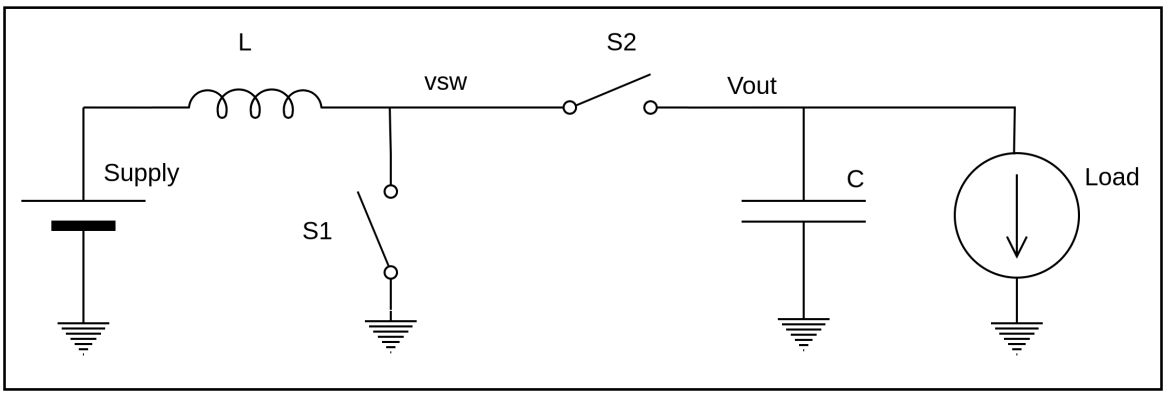

Figure 1.4. Boost Converter simplified circuit diagram.

Boost converter output to input voltage conversion ratio is expressed as

$$M = \frac{V_{out}}{V_{in}} = \frac{1}{1-D}. \tag{1.10}$$

Unlike the buck converter, the inductor on time duty cycle inversely affects the output voltage for the boost converter. Decreasing the duty cycle increases the voltage conversion ratio. In theory the conversion ratio can be infinite; however, in practice it is limited by the physical design parameters since controlling a very small duty cycle becomes really cumbersome.

1.4. Buck-Boost Converter

Buck-Boost converter can be a buck or a boost converter depending on the controller as the name implies. Buck-Boost converters are generally used to provide a freedom to choose the output voltage or to produce a stable output with changing supply voltages like in mobile platforms. Figure 1.5 demonstrates the simplified buck-boost converter circuit diagram with the load current. Depending on the supply and output conditions, S1 and S2 turn on and off duty cycles determine the output voltage setting.

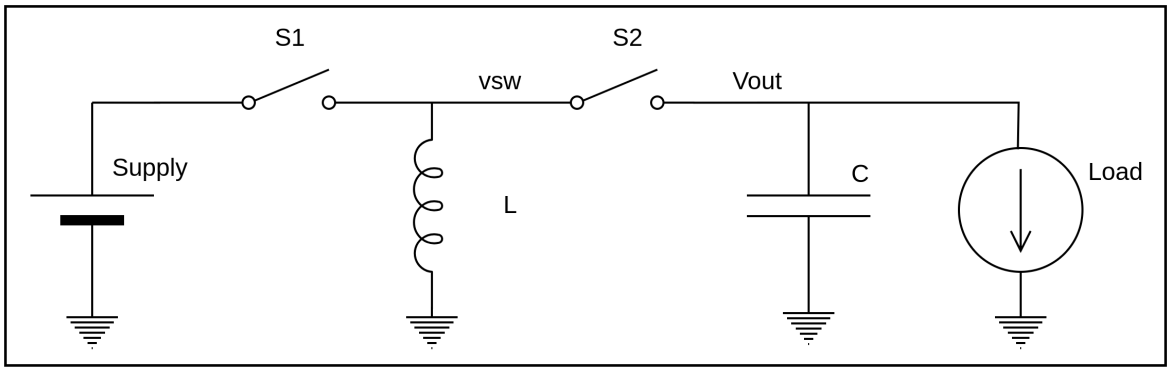

Figure 1.5. Buck-Boost Converter simplified circuit diagram.

Buck-boost converter output voltage to input voltage conversion ratio can be expressed as

$$M = \frac{V_{out}}{V_{in}} = -\frac{D}{1-D}. \tag{1.11}$$

Since it can be a buck converter or a boost converter, duty cycle ratio defines the conversion ratio and mode of operation.

1.5. Hysteretic Buck Converter

Every buck converter architecture has advantages and disadvantages regarding DC regulation performance, load transient response, and efficiency. Despite the improved load transient response of voltage control mode, it is difficult from a compensation point of view, and stability is a concern for voltage mode control. On the other hand, hysteretic control is known to be unconditionally stable [2], [3], [4] unlike the other voltage mode control architectures. Thus, it makes hysteretic control a better candidate for a buck converter. The major drawback of hysteretic control is that its switching frequency is related to the load and it can cause a wide switching frequency spectrum [5]. If the switching frequency of the converter is controlled within a certain spectrum, then the advantages of the hysteretic converter outweigh the problems. To control the switching spectrum, Phase Locked Loop (PLL) and Delay Locked Loop (DLL) control schemes have been used [6], [7], [8]. In this study, the DLL based idea is used to control the switching spectrum with the help of a switching frequency counter

as coarse control and delay locking as fine control to achieve a better regulation for both outputs. In this way, its load response will be faster compared to pure PLL or DLL controllers.

$$f_s = \frac{D(1-D)}{\tau_{RC}(V_H/V_{IN}) + \tau_D} \tag{1.12}$$

$$f_s = \frac{D(1-D)}{\tau_{RC}(V_H/V_{IN}) + \tau_D + \triangle\tau} \tag{1.13}$$

Since hysteretic converters do not have a synchronization clock signal, their switching frequency is determined by the system device parameters, whose values must be known to have a better insight about the functionality of the hysteretic buck converters. [9] gives a mathematical function of the switching frequency f_s represented in (1.12). D is the duty cycle at CCM operation, τ_{RC} is the product of the feedback network time constant, V_H is the hysteresis window, V_{IN} is the supply voltage and finally τ_D is the controller and driver summed inner total delay. [6] adds a delay which is used for a DLL hysteretic architecture such that f_s is modified to the expression in (1.13) for DLL hysteretic architectures. $\triangle\tau$ is the delay due to the delay line of the DLL. The main aim of hysteretic converters is to control this expression with different ideas applied at various architectures.

To reduce the cost of a DC-DC converter implementation, the same inductor is employed to regulate two or more outputs. Eliminating one or more inductor offers reduced bill of materials with the expense of design complexity at the expense of cross talk between outputs. To control two outputs (which have different voltage settings and load currents) by utilizing a single inductor, there must be a control mechanism which monitors both outputs and adjusts one output operation with respect to the other. Inherently, usage of the same inductor in a time multiplexed manner causes cross regulation issues, whereby one output affects the other one, and at worst case scenario, can cause loss of regulation. Different architectures have been proposed in the literature to reduce cross regulation. The adaptive switchable continuous conduc-

tion mode and discontinuous conduction mode technique utilizes a five input cross-talk reduction error amplifier in [10] to minimize the cross regulation and increase power delivery. A continuous gate-drive modulation (CGDM) scheme is proposed in [11] to minimize the cross regulation when outputs have large load transition. Dual switching frequency technique is used to enhance the response time and cross regulation in [12]. In [13], adaptive pseudo continuous conduction mode (PCCM) is used for reducing the cross regulation and being adaptive also increases efficiency [14]. The design in [15] operates in pseudo-continuous conduction mode (PCCM) with single freewheel phase to reduce the switching loss and minimize the cross regulation. The proposed solution in [16] was to use a freewheeling capacitor. Another idea to reduce the cross regulation was to use a PLL and auto-phase allocation algorithm [14] , [17]. [18] propose dual-mode energy delivery methodology which reduces both steady-state and transient cross regulation in load transient response. The design in [19] focuses on constant charge control to regulate each output and reduce the cross regulation issues. The proposal in [20] introduces a scheme with adaptive adjustment of the load dependent peak-current control technique and hysteresis mode to minimize the cross regulation. Another important approach to reduce the cross regulation was to improve the response of the feedback loop or feed forward technique [21] , [22]. In this way when the feedback response is improved consequently the cross regulation is reduced. Ripple based adaptive off-time control method in [23] focuses reducing the cross regulation for multiple output. For multiple output systems the cross regulation issue could be more severe since accumulative error increases with increasing number of outputs.

In this study, another solution is presented to improve the cross regulation further. In this proposed architecture, load balancing scheme adjusts one output with regard to the other by continuously monitoring load demands of both outputs and then prioritizing the inductor current delivery with an iterative process to improve the transient response and cross regulation. In addition, a frequency counter is utilized to enhance the transient response further and delay locked loop is utilized to enhance the static regulation.

1.6. Single Inductor Double Output (SIDO), Single Inductor Multiple Output (SIMO) Converters

To reduce the bill of materials, single inductor can be used to regulate two or more outputs. Single inductor double output (SIDO) converter utilizes the same single inductor to regulate double outputs. Single inductor multiple output (SIMO) utilizes the same single inductor to regulate more than two outputs. In this architectures, the same inductor is used in a time multiplexed manner to regulate all different output voltages for different load conditions. SIDO/SIMO idea is used for buck, boost or buck-boost converters to reduce one inductor. Figure 1.6 depicts the basic idea of SIMO architecture showing switches and three outputs.

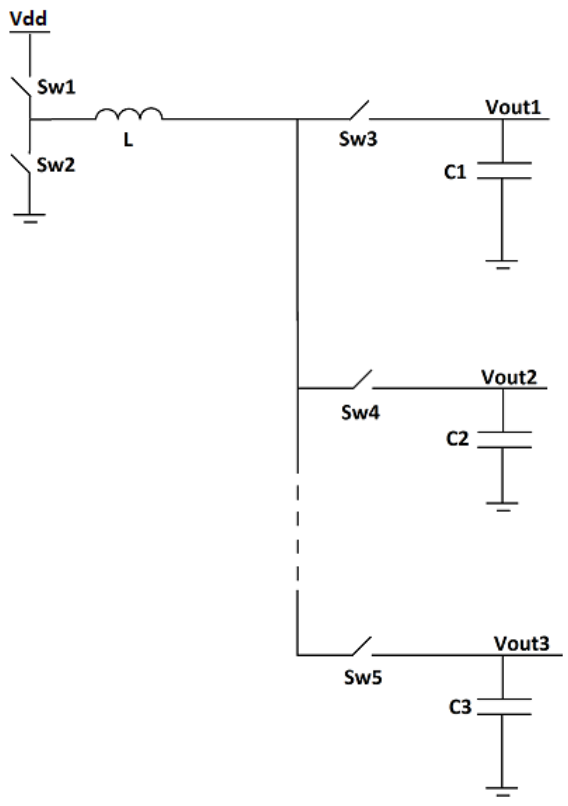

Figure 1.6. SIMO architecture.

Different techniques are used for the regulation of SIDO converters. [30] uses capacitor current and voltage to regulate both outputs, [31] uses hysteretic current and charge control to regulate outputs. [32] uses average current control, [34] uses

digital control to regulate both outputs, [35] uses to change duty of the comparator to regulate outputs, [36] uses charge control of each output to regulate all outputs.

Since SIMO converters have more outputs, its design complexity increases with increasing number of outputs. Most designs are achieved by utilizing the inductor in a strict time multiplexing mode and, as a result, output load transient performance is heavily affected by the time multiplexing. Since, a load can be applied to one output at any time instant, it will take some time for the inductor to be connected to that output and higher load drop for that output will be inevitable. Various architectures are present in literature to regulate more than two outputs. [36] uses charge control scheme for each output voltage to regulate all outputs. [37] uses digital driven control to regulate all outputs. [35] changes the comparator by duty regulation to maintain all outputs regulation. [47] introduces a new pulse width modulation scheme assisted by digital to produce stable outputs.

1.7. Thesis Organization

This document is organized as follows:

Chapter 1 provides details about the motivation of this work and the main design methodology followed. Then, the chapter introduces the DC-DC converter and main DC-DC converter architecture types, followed by brief information about buck, boost, and buck-boost architectures. Then, Single Inductor Double Output (SIDO) and Single Inductor Multiple Output (SIMO) architectures are introduced.

Chapter 2 gives an overview of the designed architecture and Chapter 3 introduces the main architecture proposed in this work and gives details about each sub block. These blocks are; Up/Down switch, output switch, current bias block, digital to analog converter (DAC), output comparator, current limiter block, active diode comparator, bottom current comparator, charge pump, always on block, digital gates, frequency counter, pulse delay block, delay lock block and finally the core of this work as load balancing controller. Each block is explained in detail with some figures giv-

ing information about the functionality of the block and also showing some simulation results to support the main idea.

Chapter 4 shows the top level simulation results for different test purposes. Power-up and start-up simulations demonstrate the initialization of the SIDO hysteretic buck converter. Load and line transient simulation results give the main transient performances of the buck converter, which are the key design aspects evaluated in every DC-DC converter. Then, the dependency of the inductor switching frequency on the load and output voltage is shown, which is a specific case for hysteretic buck converters. Finally, cross regulation simulation results are provided and compared with prior art. Cross regulation is the key design goal of this work.

Chapter 5 concludes the paper with final remarks and then introduces some ideas to enhance the performance further.

1.8. Thesis Contribution

This thesis presents a novel Single Inductor Double Output (SIDO) Hysteretic Buck converter which balances one output with respect to the other by continuously monitoring the load demands of both outputs and then aligning the outputs such that each output regulates its load with minimal disturbance to the other. Load balancing prioritizes the inductor current delivery in the case of a large load current request. The controller aims to finalize the ongoing regulation of the recent output in a prompt manner and then directs the inductor current to the steep load demand output and afterwards returns to the initial output regulation in an iterative way. In conjunction with iterative duty cycle adjustment of outputs, a frequency counter is utilized to accelerate the iteration process to enhance the transient response further. In addition, a delay locked loop fine tunes the duty cycle further to reduce the steady state cross regulation and also limits the switching frequency spectrum. Consequently, both static cross regulation and transient cross regulation performance are further improved compared to previous SIDO architectures. Post-layout simulation results indicate that this architecture has a static cross regulation of 0.0009 mV/mA and transient cross regu-

lation of 0.0063 mV/mA. This SIDO buck converter outperforms the previous studies with a total power delivery capability by supplying 3A load current at each output and 10W of total power with a peak efficiency of 93.7 %.

2. ARCHITECTURE OVERVIEW

The overall architecture is formed by a current bias block, Digital to Analog Converter (DAC), active diode, current limiter, output voltage comparators, charge pump, input and output select switches, and controller block. The controller block includes sub blocks such as frequency counter, pulse delay, delay lock block, and control logic to process the relevant internal signals. Since it has NMOS and PMOS switches at the input side and two output select switches, the controller basically drives four switches. The simplified circuit diagram of the designed buck converter includes four switches, one inductor, two output capacitors and a main control unit which is shown in Figure 2.1. The inductor is 220nH and the output capacitor for each output is 50μF. Output switches are driven by a charge pump for low power supply and/or for high output voltage settings. All building blocks inside the peripheral blocks and the load balancing controller are depicted in Figure 2.2. All building blocks will be briefly discussed in the following chapter, and finally controller and main functionality will be explained in detail.

Briefly the main control functionality can be described as both output voltage comparators (comparator 1 and comparator 2 in Figure 2.2) monitoring the output initially. When there is a voltage drop due to a load demand, that output voltage comparator causes the inductor to charge through the supply. Then, depending on the other output load demand, controller also regulates the other output as well. Controller tries to find an optimum duty cycle for each output with regard to the other output and changes the duty cycle accordingly. Duty cycle adjustment is performed by measuring the switching frequency of each output via counting the switching cycles when inductor is supplying current to that output. Then, a delay time is produced which will define the ON time of that output (using inductor for that output for current supply) with regard to the other output. Delay lock block fine tunes the duty cycle for each output further. Load balance algorithm tries to regulate both outputs to their load currents and finds an optimum operation point for both outputs.

DAC blocks are used to produce a reference voltage for the output voltage comparators. Charge pump is used to drive output switches for low input voltage and/or high output voltage setting. Current limit comparator is used as a protection mechanism for not saturating the inductor current and also preventing high current for the input side PMOS switch. Bottom current comparator is used to push inductor into CCM operation if possible for better load transient response. Active diode is used in DCM disabling the inductor current going beyond zero.

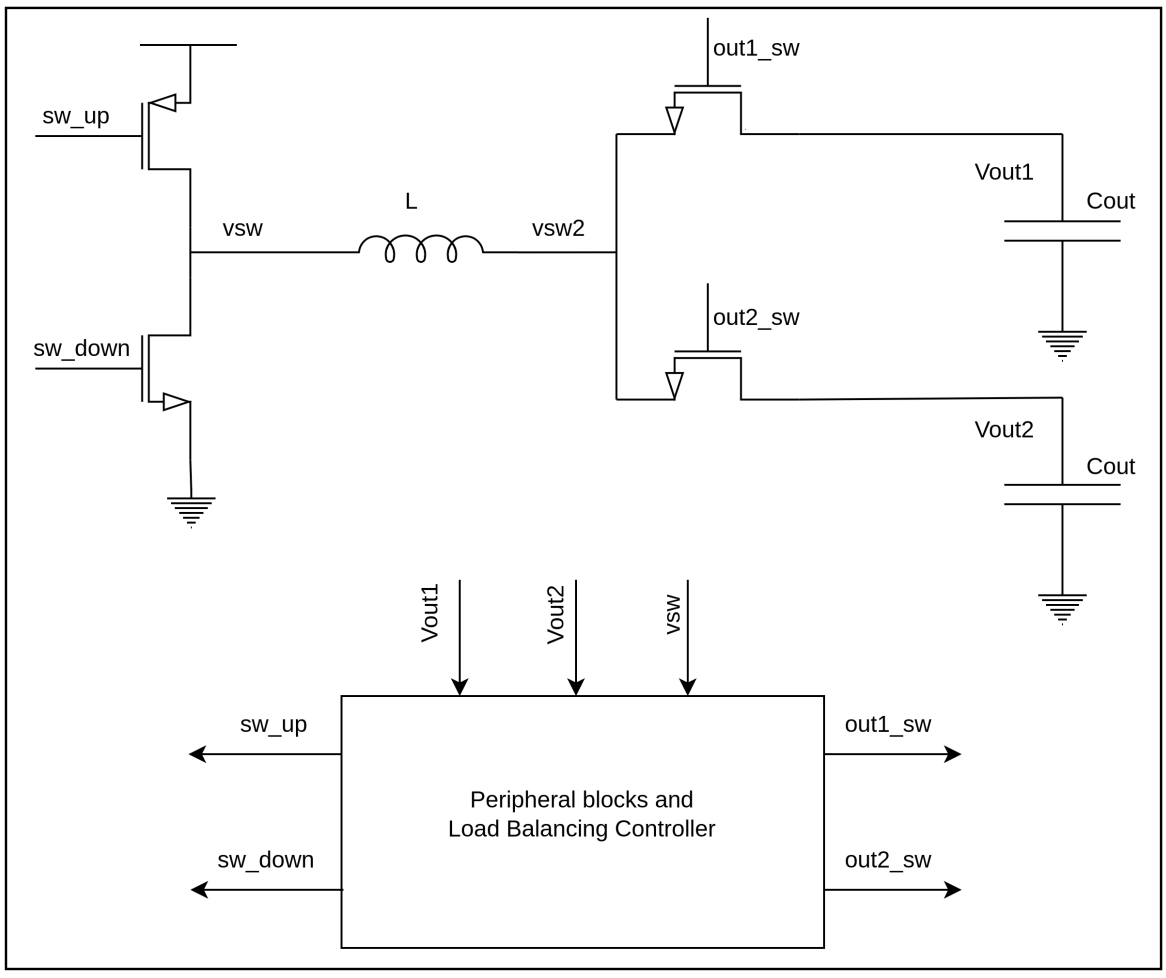

Figure 2.1. Single inductor double output hysteretic buck converter circuit diagram.

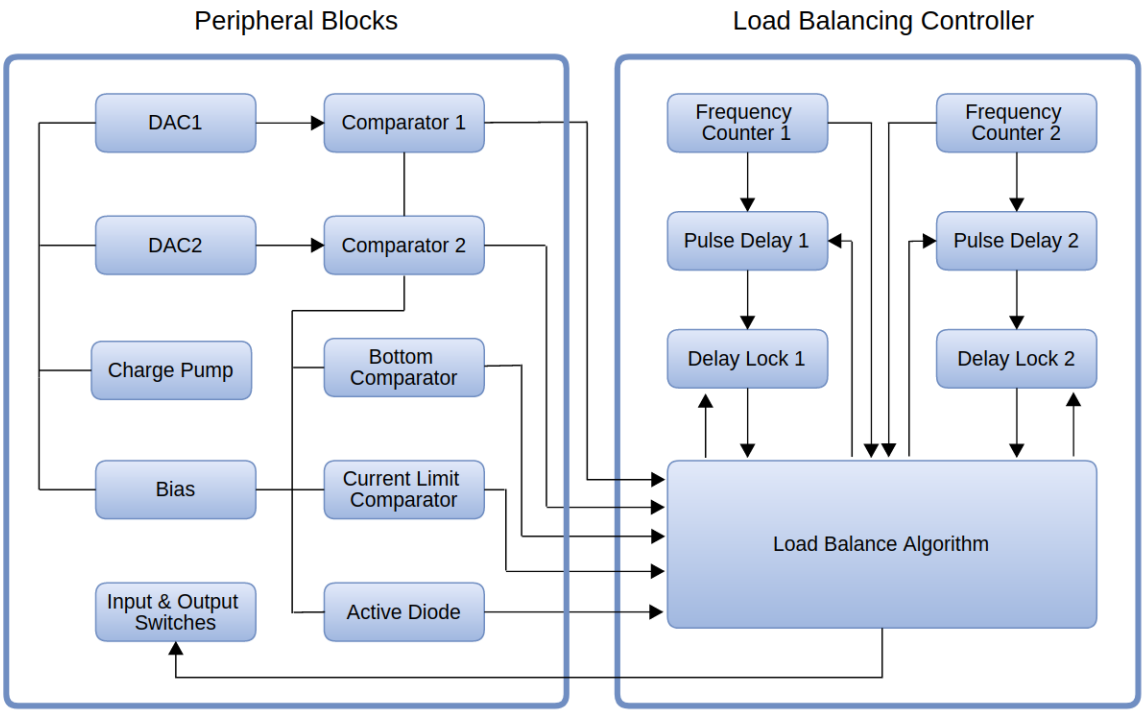

Figure 2.2. Main architecture showing peripheral blocks and load balancing controller.

3. MAIN ARCHITECTURE

3.1. Up/Down Switch

Up/Down switch is used charge the inductor through the supply voltage and discharge the inductor to ground. PMOS transistors are used for the up switch and NMOS transistors are used for the down switch. To have better conductivity and faster switching, these PMOS and NMOS switches have to have low resistance values. Thus, these MOS transistor sizes are very large and they occupy a big portion of the chip area. Another crucial design characteristic of these switches is that they must never be ON at the same time; otherwise, there will be a short circuit current which can damage the switch transistors and also cause huge loss of power. As a result, having non overlapping clocks to these PMOS and NMOS transistors is really crucial. Figure 3.1 depicts the input up/down switch simplified block diagram. The leftmost gates in this figure provide non-overlapping logic to guarantee the non-overlapping PMOS and NMOS gate signals to be used for the *up_switch* and *down_switch* signals. Then, inverter stages are adjusted such that propagation delay from input to output is minimized. To size each inverter stage and also to find the optimum number of inverter stages to drive the PMOS and NMOS switches with low propagation delay,

$$f = \sqrt[N]{C_{out}/C_{in}} \tag{3.1}$$

is used in [38]. f is the sizing factor, N is the number of the stages and C_{out} is the output capacitor which is the gate to source capacitance of the switch MOS and C_{in} is the gate to source capacitance input inverter. Sizing calculations done separately for PMOS and NMOS to find the optimum number of stages and inverter sizes.

A simulation has been run to check the input to output propagation delays both for PMOS up switch and NMOS down switch. Table 3.1 shows the PVT simulation result of input switch PMOS and NMOS input to output rise and fall delays. At the same simulation setup PMOS and NMOS on switch resistances are also calculated and listed in Table 3.2.

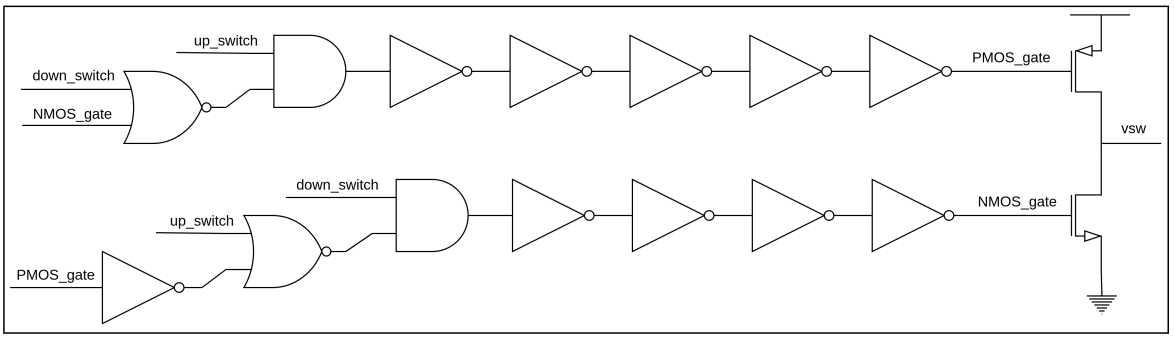

Figure 3.1. Up/Down switch block diagram.

Table 3.1. Up/down switch input to output propagation delay.

	Typ. (ns)	**Min. (ns)**	**Max. (ns)**
PMOS rise delay	3.4	2.3	6.5
PMOS fall delay	1.9	1.4	3.5
NMOS rise delay	3.3	2.2	6.5
NMOS fall delay	1.8	1.3	3.3

Table 3.2. Up/down switch PMOS and NMOS switch resistance PVT results.

	Typ. (mΩ)	**Min. (mΩ)**	**Max. (mΩ)**
PMOS resistance	12.8	7.9	24.7
NMOS resistance	7.7	4.4	17.3

3.1.1. Layout Design of The Up/Down Switch

Up down switch layout design is crucial since the ON resistance of these switches affect the efficiency. To increase the efficiency, the ON resistance of the switches must be low which will increase the silicon area. Also, when MOS transistor sizes increase, their gate capacitance will increase and the switching loss will increase due to gate capacitance. Thus, there is a trade-off while choosing the right size of the switch devices. PMOS switch size is almost double the NMOS switch size due to electron hole mobility ratio. Layout design of the input Up/Down switch is shown in Figure 3.2.

PMOS switch is at the top and NMOS switch is located below. Left bottom is the non overlap logic and driver of the PMOS devices and right bottom side is similarly non overlap logic and driver of NMOS switch. To reduce the layout related parasitic resistance which is added on top of actual switch resistance, all metal layers are utilized and the number of via contacts is chosen as high as possible. The layout dimensions of the block are 1350μm to 920μm.

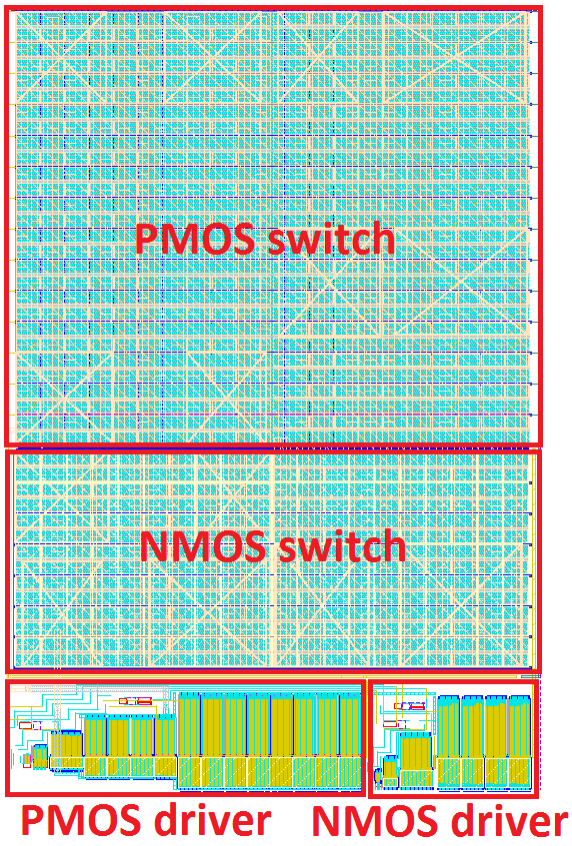

Figure 3.2. Layout design of Up/Down input switches.

3.2. Output Switch

To control two outputs with the same inductor, two extra switches are needed to connect the inductor, to the outputs. The output switches serve two purposes; to connect the inductor to the outputs and also to isolate one output from the other. To have a better switch conductivity, its switching resistance must be as low as possible. The switch can be implemented using PMOS or NMOS devices. Since NMOS has a

better conductivity compared to PMOS due electron mobility being high compared to hole mobility, output switch is formed by NMOS devices. Figure 3.3 shows the simplified block diagram of the output switch. The gate signal of NMOS switch transistors are driven by the charge pump voltage for two main reasons. The first reason is to have lower switch resistance. The second reason is that when the output voltage is set to 2.5V and the supply is at lowest value of 3V there will be 0.5V of gate to source over drive voltage which is less than the threshold voltage of the NMOS transistor. Overdrive voltage being less than the threshold voltage results in the NMOS transistor being OFF and conductivity being too small. To overcome this overdrive voltage issue, charge pump voltage is used to drive the logic and switch NMOS transistors. Charge pump produces a 5V stable output voltage regardless of the supply as long as it is in the range 3V to 5V. Input switch on signal named *out_sw_on* is level shifted to the charge pump voltage by the input signal level shifter. Another important design highlight is that two NMOS transistors are connected back to back. This is done to have two back to back body diodes; otherwise, one output voltage will leak into the other output through the body diode. With current back to back diode connection, two outputs will be totally isolated from each other and each output can be selected without limitation. Otherwise, single inductor double output architectures will have some limitation choosing the output voltages. Since the inductor can serve one output only at given time, it must be guaranteed that only one output switch is ON and the other one is OFF. To ensure that only one output switch is ON, the gate signal of the other switch pass device gate signal is used to mask the input switch signal. It was already mentioned that the ON resistance is very important to serve as a switch; a PVT simulation with addition of output voltages of being 3V and 5V has been run to check the ON resistance of the switches. Table 3.3 lists the ON resistance for typical, minimum, and maximum ON resistance values. For the same simulation setup, switch rise and fall delays are also calculated since it is crucial that ON and OFF times must be as low as possible to have a faster operation. Input to output rise and fall delays are listed in Table 3.4. Note that inverter stages which are used to drive the actual NMOS switch transistor sizing is performed similarly to the up-down switch design.

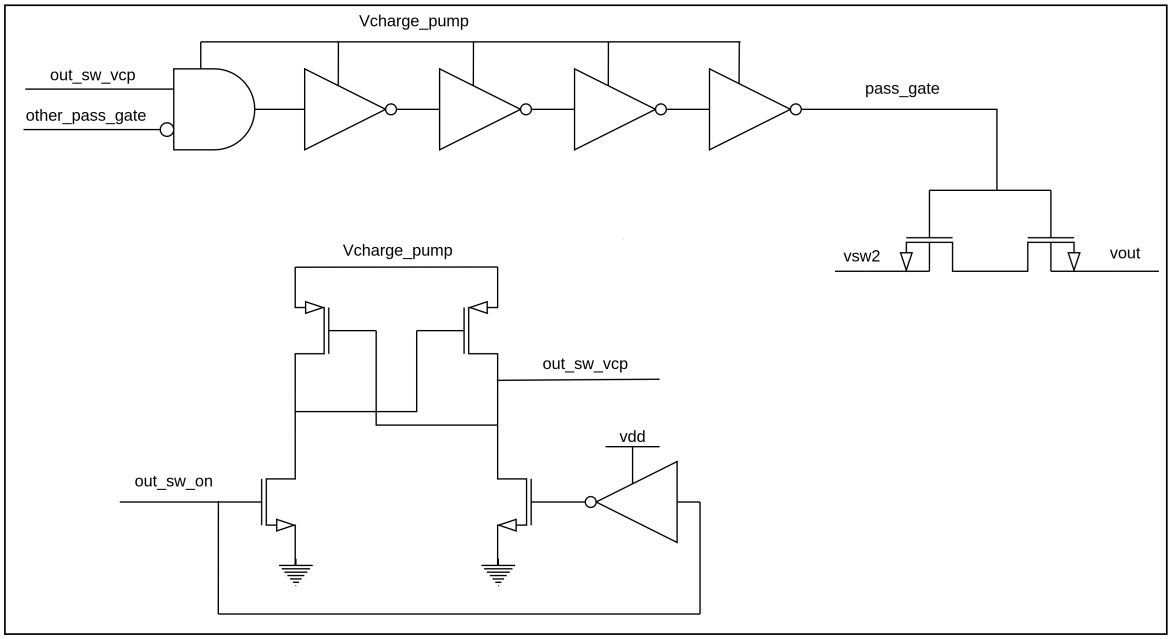

Figure 3.3. Simplified block diagram of output switch.

Table 3.3. Output switch resistance PVT simulation results.

	Typ. (mΩ)	**Min. (mΩ)**	**Max. (mΩ)**
Output switch resistance	8.7	5.3	15.1

Table 3.4. Output switch rise and fall delays for PVT simulation results.

	Typ. (ns)	**Min. (ns)**	**Max. (ns)**
Output switch rise delay	1.9	1.5	2.6
Output switch fall delay	1.9	1.5	2.7

3.2.1. Layout Design of The Output Switch

The ON resistance of the output switch must be as low as possible. However, such a low resistance switch requires a huge silicon area. Thus, there is a trade-off between silicon area and conductance. Another important physical design aspect is that; the resistance of the metal connections in the layout must be as low as possible to reduce parasitic resistance which is added to the actual switch resistance. To reduce layout

parasitic resistance, all metal layers are used in addition to many via connections. Figure 3.4 demonstrates the final layout of the output switch. Almost all of the area of this blocks layout is occupied by the actual NMOS switches. Non overlap logic and driver is shown below the figure. The layout dimensions of the block are 1360μm to 1220μm.

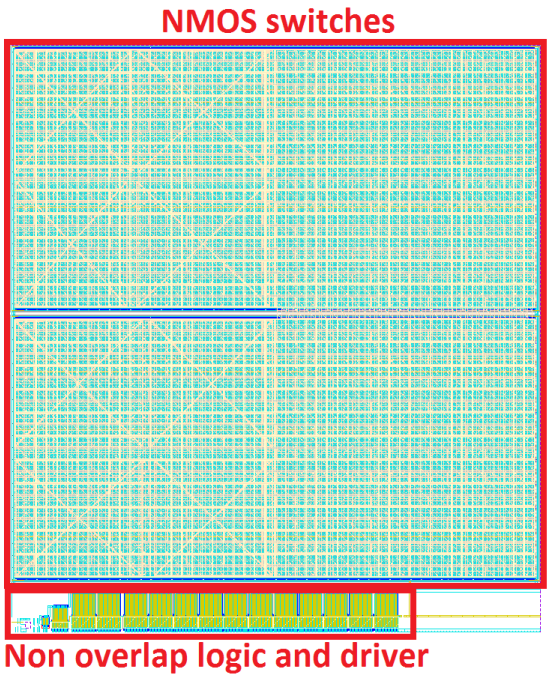

Figure 3.4. Layout design of output switch.

3.3. Current Bias Block

Most analog building blocks need a stable current source as a reference to operate at a predictable DC condition. This current reference is produced by a block called current bias. For this thesis, a current bias block is designed by using an accurate external resistor with an accurate voltage source. Initially, a 0.4V voltage reference is obtained by a resistor divider with the help of a 1.2V band-gap voltage reference. Then, an opamp is used to buffer this 0.4V voltage reference to an accurate 800k external resistor. The current which flows through this resistor is used as a reference current to produce both NMOS and PMOS bias currents. Figure 3.5 shows the simplified block diagram of the current bias block. The current bias block has current sources of

three different values of current sources as; 0.5μA, 1μA, and 10μA. Five 0.5μA output current sources, ten 1μA, and twelve 10μA bias currents are fed to the internal blocks.

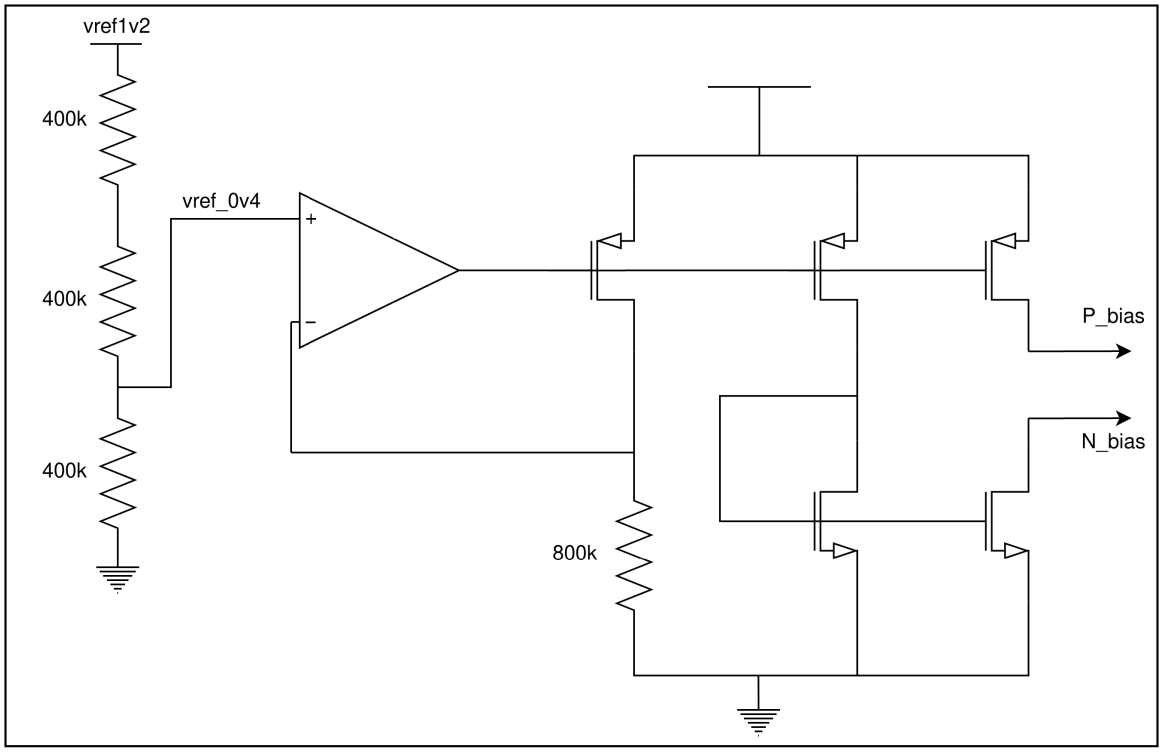

Figure 3.5. Simplified current bias block diagram.

The voltage buffer used to replicate the 0.4V voltage reference is designed as folded cascode architecture. Figure 3.6 shows the designed folded cascode voltage buffer. $Vinp$ input of the buffer is connected to $vref0v4$ resistor division node. $Vinn$ input of the buffer is connected to 800kΩ external resistor. Output of the voltage buffer is connected to the PMOS which drives current to the external 800kΩ resistor. Since the voltage of the resistor is precisely adjusted to 0.4V, if the resistor value is accurate, then the current through this resistor must be precise. Note that other building blocks use current sources driven by the bias block. However, the voltage buffer of the bias block also needs a bias current. This bias current of the voltage buffer is formed by the crude current bias generator shown at the left side of Figure 3.6. The basic idea is to use a resistor with an NMOS diode transistor. This way when the power supply is ramped to its final value there will be a roughly known current source which is enough for the voltage buffer. The drawbacks of this crude current bias generator is that its

value is not precise and it can cause increased power consumption in this block.

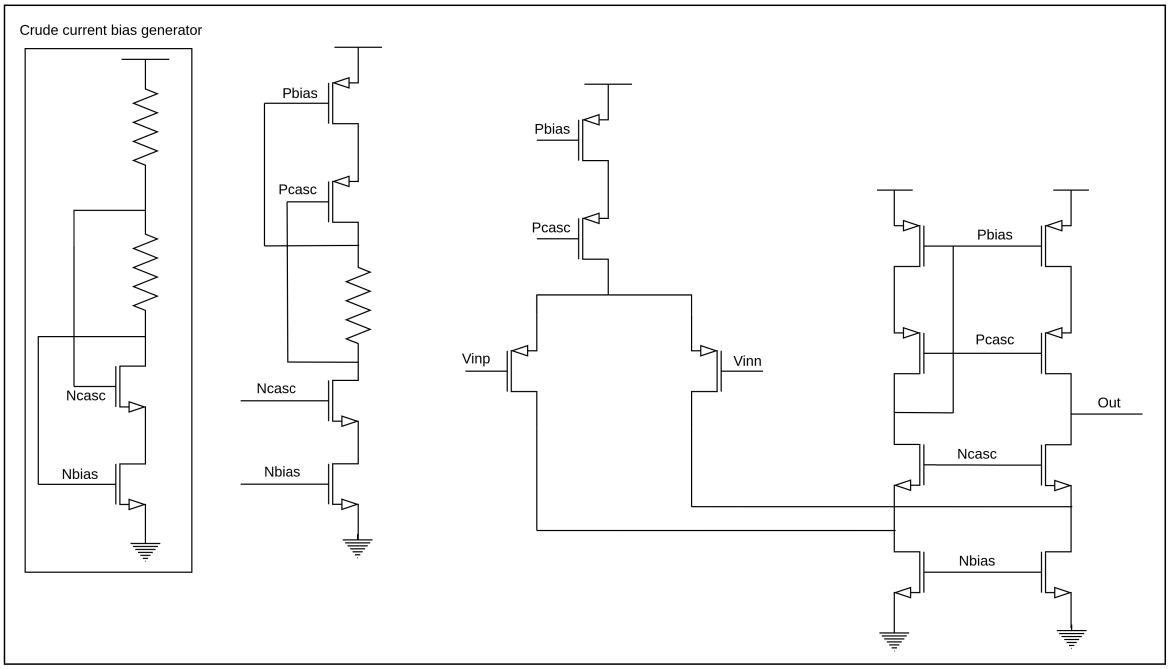

Figure 3.6. Voltage buffer design of the current bias block.

3.3.1. Current Bias Block Simulation Results

The first simulation is run by ramping up the supply to check that the current bias block settles as expected and *bias_ok* signal flag with current output values are as expected. Vdd supply voltage is ramped up from 0 to 4V with a rise time of 1μs. Then, all different current outputs are observed in addition to the voltage on the external 800kΩ resistor. Figure 3.7 shows this simulation run. *bias_ok* signal rises at 17μs and current values should be stable after this flag. I_1uA is one of the 1μA output and I_10uA is one of the 10μA output. V_800k is the top node of the external 800kΩ resistor showing how its voltage is close to 0.4V.

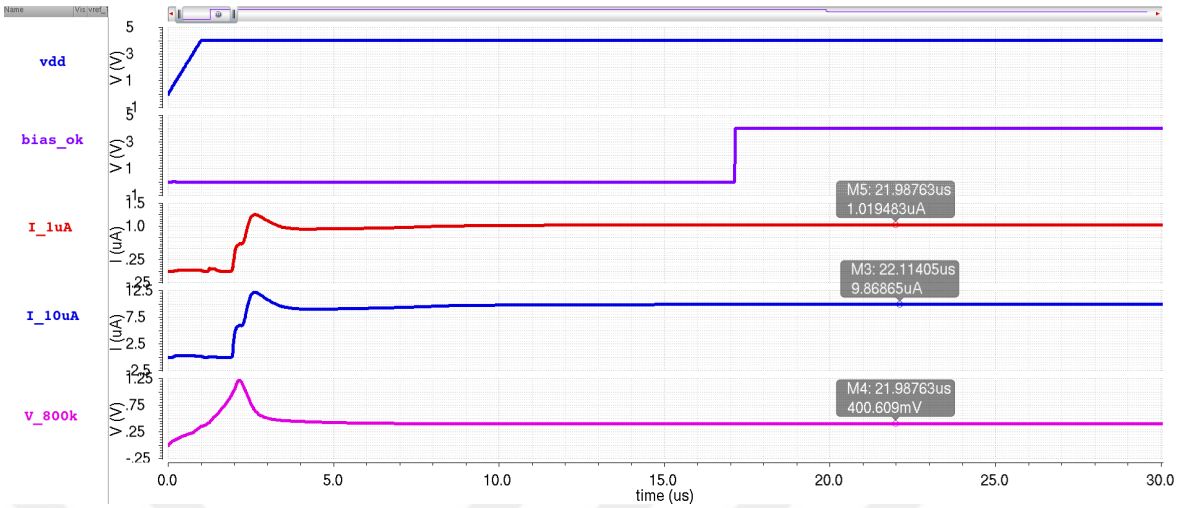

Figure 3.7. Current Bias block settling with supply ramp-up.

To test the current bias block functionality with simulation, AC simulation has been run to check the stability of the closed loop configuration. Then, 1.2V voltage reference is changed abruptly at a full PVT transient simulation to see if there is ringing at the current outputs to ensure the stability of the output currents. Figure 3.8 depicts this PVT transient simulation results. 1.2V voltage source is changed abruptly to 1.3V and then reverted back to 1.2V abruptly. The used settings for full PVT analysis are; for process ss, ff, sf, and fs active device corners, 3V and 5V supply and -40°C and 125°C for temperature. As can be seen from the waveform, there is no oscillation or ringing at 10μA bias current output. DC simulation also has been run for full PVT to check the current values at corner conditions. Table 3.5 shows the 1μA current output results for typical, minimum and maximum values seen from this PVT simulation. Results indicate that output current is accurate enough to use as a current bias.

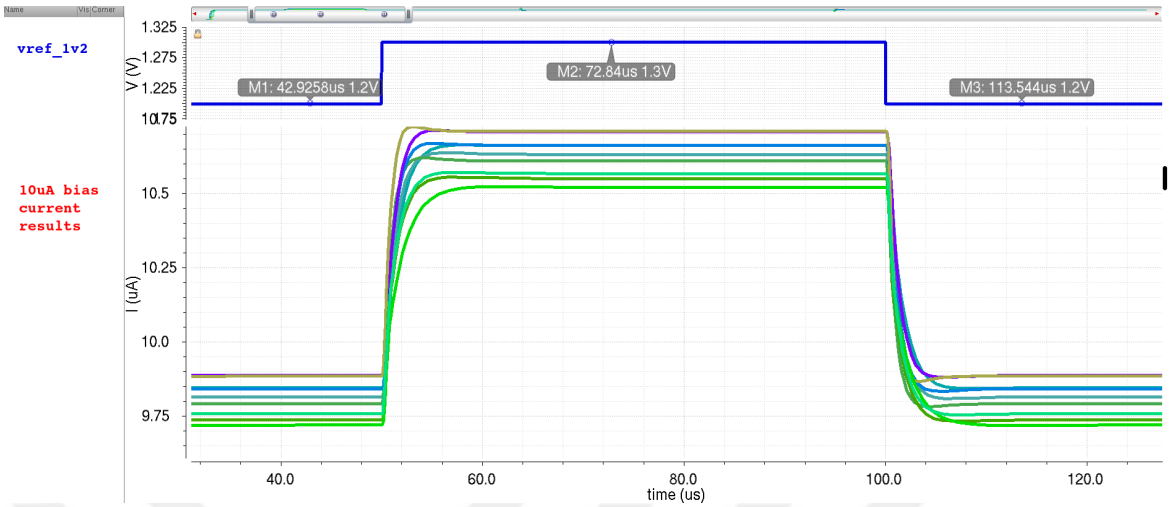

Figure 3.8. Bias current output for full PVT with reference voltage change.

Table 3.5. 1μA current output PVT simulation results.

	Typ. (μA)	**Min. (μA)**	**Max. (μA)**
1μA current output value	1.026	0.985	1.060

Power supply rejection is also a very important design goal for a current bias block because when there is a noise at supply the reference bias currents must not be affected from supply variation. To test the power supply rejection (PSR) of the bias block, the test setup has been modified and a simulation has been run. Figure 3.9 shows the PSR simulation result. Applied signal frequency is changed from 1Hz to 10GHz. For very low frequencies (1Hz) the PSR is -87.6dB and it increases with increasing frequency and its value is -23.6dB for 1MHz. Another simulation is also run to check the power supply rejection with transient analysis. Figure 3.10 shows the simulation result of power supply rejection with transient simulation. In this simulation supply voltage is changed abruptly from 4V to 5V and then reverted back to 4V and the 10μA current output is observed to see the power supply effect at the bias output current. For 1V of supply voltage change only 115nA is changed from 10μA current output. Note that 1V of supply change is an exaggerated situation which won't happen in actual operation.

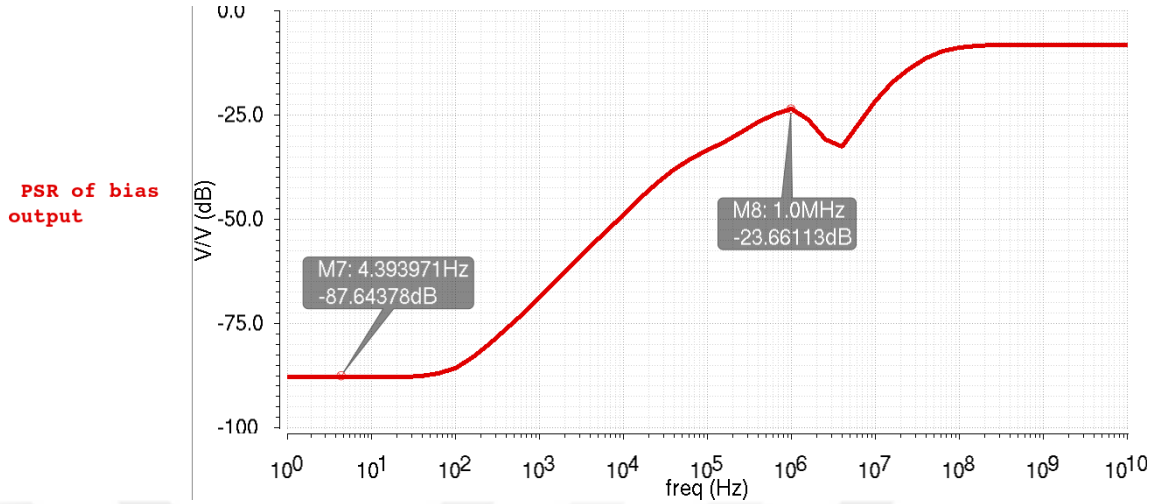

Figure 3.9. PSR simulation of bias block.

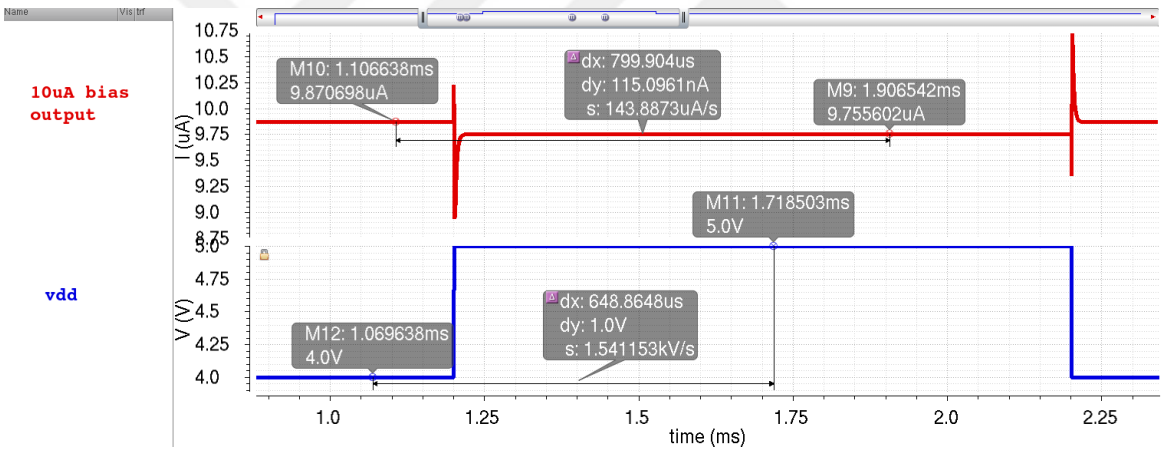

Figure 3.10. Power supply rejection simulation result showing one of the output.

3.3.2. Layout Design of The Current Bias Block

Current bias block supplies current to almost all internal blocks as reference and its outputs must be stable since the performance of the other blocks will be affected by these currents. As a result, great care has been taken out to isolate the internal signals during layout design. Figure 3.11 depicts the layout design of the current bias block. At the left top side, the opamp which is used as a buffer is placed. At the right of this block is the compensation part. Power on reset section is located top right of the layout which is used by charge pump block. The bottom part contains the output bias current generators, which are used by other internal blocks. The layout dimensions of

the block are 130μm to 840μm.

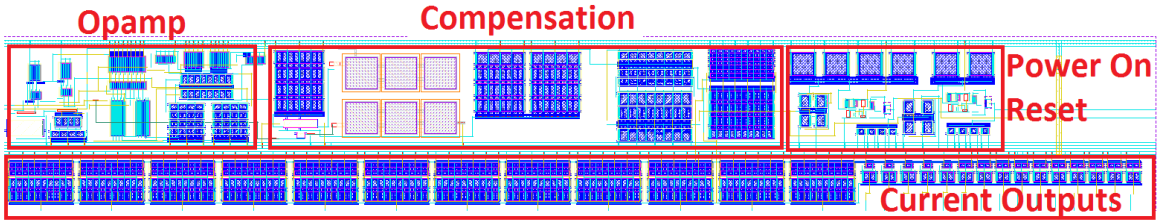

Figure 3.11. Layout design of the current bias block.

3.4. Digital to Analog Converter (DAC)

The DAC output is used as reference voltage for comparing the output voltages by the comparators. A stable and adjustable reference voltage is the key element of a DC-DC voltage converter. A folded cascode opamp is used with a variable resistor ladder to obtain a reference voltage. Figure 3.12 shows the simplified block diagram of the DAC design. Two voltage outputs are created, namely, "*dac_high*" and "*dac_low*". The "*dac_high*" is used as the upper voltage reference to detect when the output voltage reaches its maximum value. The "*dac_low*" is the lower voltage reference to detect that the output voltage is below the reference. The voltage difference between the two DAC outputs is the hysteresis voltage. The top resistor value is changed by switches to change the hysteresis and the ripple voltage. The middle resistor in the ladder is used to define the main DAC voltage and can be adjusted between 100kΩ to 2100kΩ. This resistor can be adjusted such that the output voltage can vary between 0.5V and 2.5V with a 6 bit digital setting. Table 3.6 shows the different hysteresis values for 3 bit digital code.

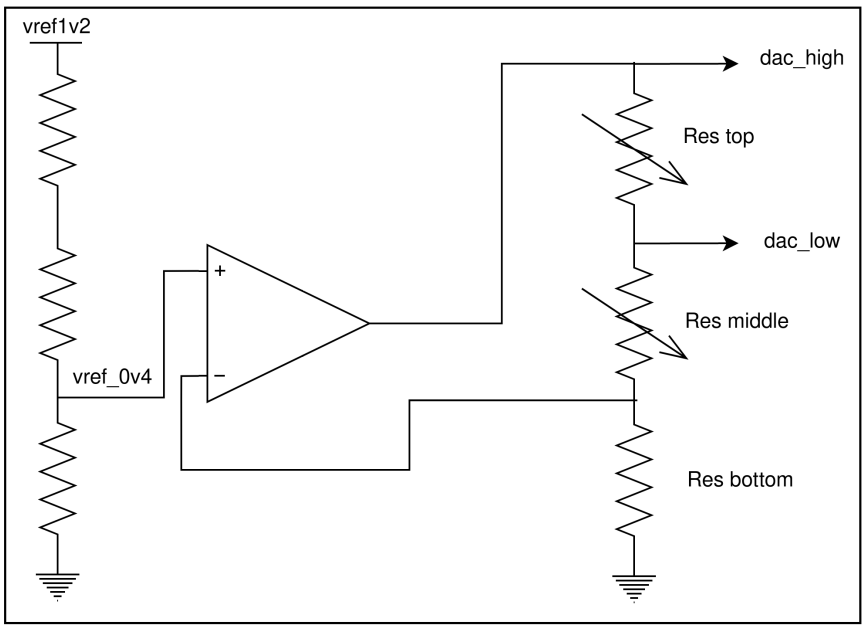

Figure 3.12. Simplified Digital to Analog Converter (DAC) as voltage reference.

Table 3.6. DAC decimal code and hysteresis settings.

Code	**Hysteresis (mV)**
0	5
1	8
2	10
3	13
4	16
5	19
6	22
7	24

Table 3.7 shows different voltage output values for 6 bit digital code settings. Note that code values are shown as decimal values for simplicity.

Table 3.7. DAC code and output voltage settings.

Code	**DAC Out (V)**	**Code**	**DAC Out (V)**	**Code**	**DAC Out (V)**	**Code**	**DAC Out (V)**
0	0.50	16	1.01	32	1.52	48	2.02
1	0.53	17	1.04	33	1.55	49	2.06
2	0.56	18	1.07	34	1.58	50	2.09
3	0.60	19	1.10	35	1.61	51	2.12
4	0.63	20	1.13	36	1.64	52	2.15
5	0.66	21	1.17	37	1.67	53	2.18
6	0.69	22	1.20	38	1.71	54	2.21
7	0.72	23	1.23	39	1.74	55	2.25
8	0.75	24	1.26	40	1.77	56	2.28
9	0.79	25	1.29	41	1.80	57	2.31
10	0.82	26	1.33	42	1.83	58	2.34
11	0.85	27	1.36	43	1.87	59	2.37
12	0.88	28	1.39	44	1.90	60	2.40
13	0.91	29	1.42	45	1.93	61	2.44
14	0.94	30	1.45	46	1.96	62	2.47
15	0.98	31	1.48	47	1.99	63	2.50

3.4.1. DAC Buffer

Inside the DAC block, there is an opamp which is used as a voltage buffer to produce a stable output. This buffer needs to have high gain and low quiescent current, and more importantly, a stable AC characteristic. Since this buffer is used in a closed loop configuration, it needs to be compensated properly in the frequency domain; otherwise, any noise could cause oscillation in the buffer. If the buffer causes oscillation, then the DAC outputs will oscillate and buck converter will not regulate its output as expected. So it is really crucial that whole DAC must function properly for different output settings, supply voltage, bias change, temperature, and all active corner cases it must function properly. Figure 3.13 shows the designed folded cascode opamp used as voltage buffer.

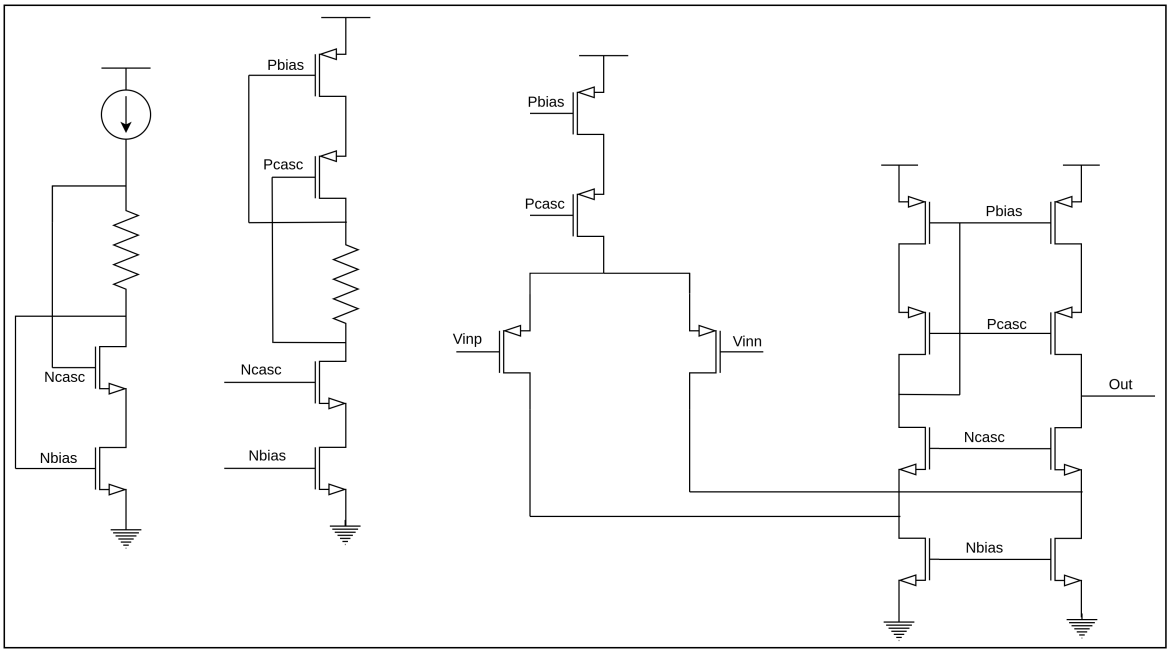

Figure 3.13. Simplified folded cascode DAC buffer.

3.4.2. DAC AC Behaviour

Closed loop configuration of the DAC buffer is compensated by using a nullifying resistor between input and output stage. To see that the DAC buffer is always compensated enough not to cause any oscillation, AC simulation has been performed. In this configuration, the feedback loop is AC wise cut with a 1H inductor and a 1F capacitor to block AC frequency but obtain the correct DC value. Figure 3.14 shows the typical AC simulation result of the DAC buffer with resistor string output attached. Phase margin is 89.8 degrees and Gain margin is -40.7dB. It is accepted that more than 45 degree of phase margin is enough for proper operation without any oscillation behavior.

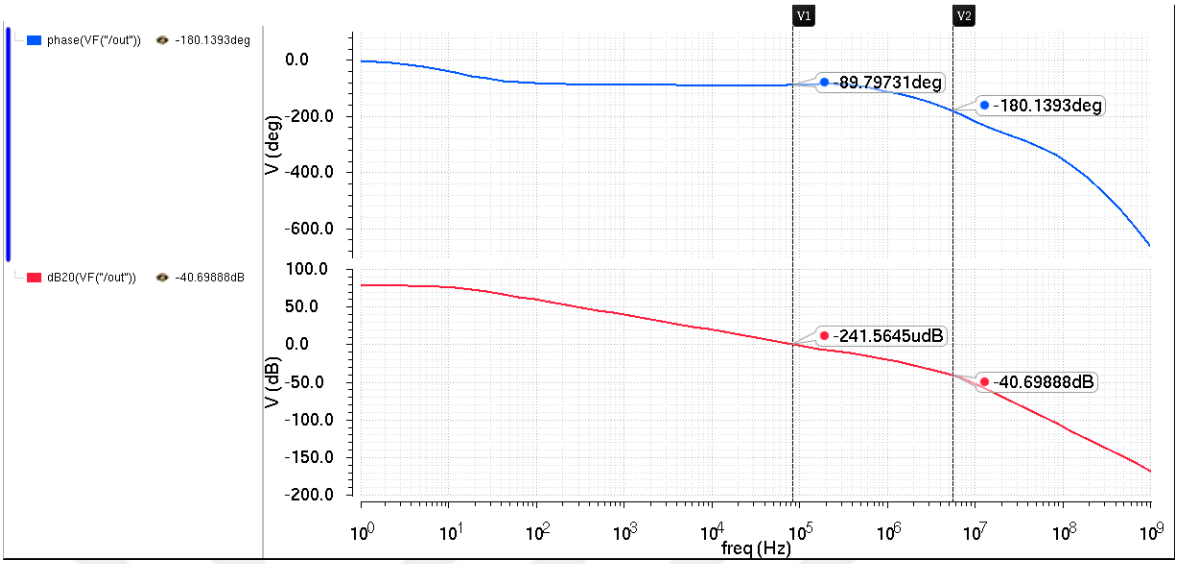

Figure 3.14. DAC buffer AC simulation showing gain and phase margin.

To test the DAC buffer AC behavior for all corner conditions, the typical bias current of 500nA is changed to 450nA and 550nA, the typical supply voltage of 4V is changed to 3V and 5V, 27°C typical temp is changed to -20°C and 100°C and all active corners as, ss, ff, sf, fs are also used. Table 3.8 shows the minimum and maximum values of gain margin and phase margin of this AC corner simulation.

Table 3.8. DAC buffer gain and phase margin results.

	Min.	**Max.**
Gain Margin (dB)	-67	-41
Phase Margin (deg.)	80	101

Also a step response transient simulation has been run to verify the AC simulation results. In this simulation 1.2V band-gap reference voltage is changed to 1.3V abruptly and output voltage is observed. Figure 3.15 shows the PVT corner simulation result for 0.5V output voltage setting and Figure 3.16 shows similar results for 2.5V output voltage setting.

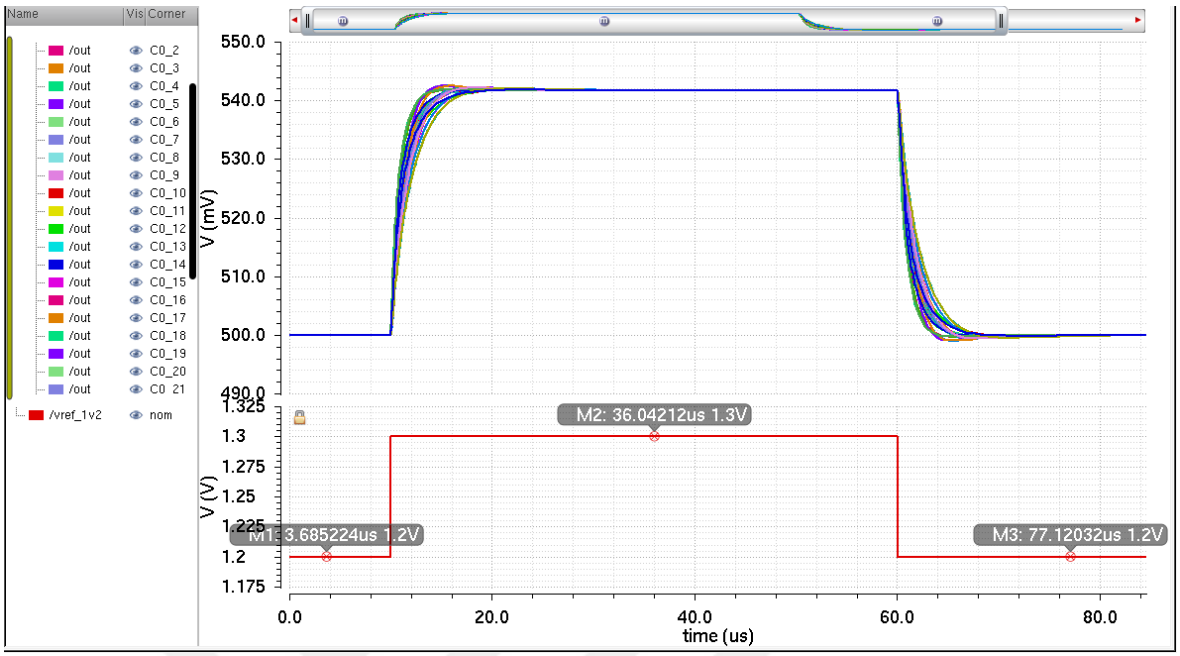

Figure 3.15. Step response of the DAC buffer for 0.5V output voltage.

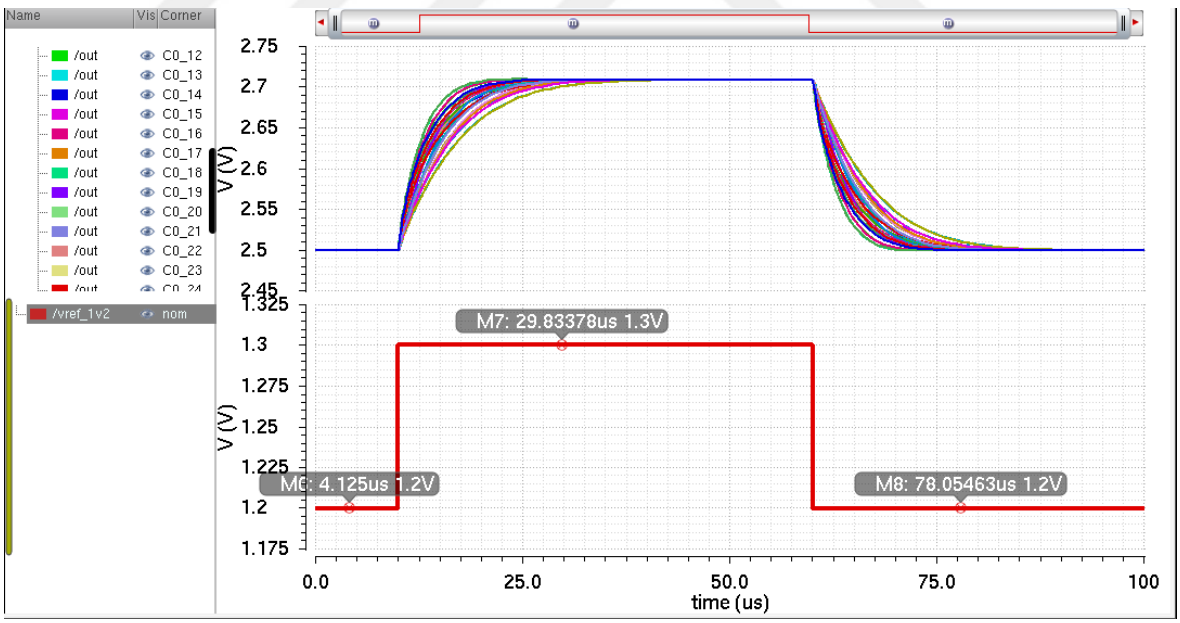

Figure 3.16. Step response of the DAC buffer for 2.5V output voltage.

3.4.3. DAC Corner Simulation Results

The DAC has been simulated at block level for corner cases. The used corner values are; vdd=3V, 5V, temperature -20°C, 100°C, bias current=450nA, 550nA , and active corners ss, ff, sf, fs and Table 3.9 shows results of this run.

Table 3.9. DAC PVT corner simulation results for minimum and maximum output.

	Min. (mV)	**Typ. (mV)**	**Max. (mV)**
DAC 0.5V output setting	499.8	500	500.3
DAC 2.5V output setting	2499	2500	2501

3.4.4. DAC Monte Carlo Simulation Results

Monte Carlo simulations have been run to see the effects of process and mismatch. For each output voltage setting as 0.5V and 2.5V, two MC simulations have been run. It has been seen that process variations do not affect the output voltage accuracy; however, mismatch is very effective. This is expected due to mismatches in the resistor string and in the DAC buffer. These mismatches will shift the output voltage DC level; however, there is a digital setting and it can be changed to compensate these variations so there will be no need of extra trimming. Note that 200 Latin Hypercube runs have been simulated both for process and mismatch. Table 3.10 shows the Monte Carlo simulation result for process variations and Table 3.11 shows the Monte Carlo simulation result for mismatches.

Table 3.10. DAC Monte Carlo 200 run for process.

	Min. (mV)	**Max. (mV)**	**Mean (mV)**	**Standard deviation (mV)**
DAC 0.5V output setting	500.1	500.2	500.1	0.01
DAC 2.5V output setting	2500	2500	2500	0.04

Table 3.11. DAC Monte Carlo 200 run for mismatch.

	Min. (mV)	**Max. (mV)**	**Mean (mV)**	**Standard deviation (mV)**
DAC 0.5V output setting	495.2	504.1	500.1	1.7
DAC 2.5V output setting	2467	2528	2500	10

3.4.5. DAC Power Supply Rejection Simulation Results

DC-DC converters produce a lot of switching noise which can deteriorate the functionality of some internal building blocks which share the same power supply. The DAC block is one of the key blocks of the buck converter because it creates the reference voltages for the buck converter. To test the power supply rejection of the DAC block, the simulation setup has been modified to run a PSR simulation. In this simulation an AC noise is applied to the supply whose frequency is varying from 1Hz to 10GHz to see the PSR of the block in broad frequency band. Figure 3.17 shows PSR simulation results of the DAC block. PSR value at DC (1Hz) is -57.8dB and it shows that the DAC block has a good power supply rejection. Highest PSR value is obtained at 248kHz and its value is -50.4dB which is still good enough to reject the noise. Also a transient simulation has been run to check the power supply rejection. Figure 3.18 shows this transient power supply rejection simulation result. In this simulation, initially the supply voltage is set to 4V and then it is abruptly changed to 5V. Then supply voltage is reverted back to 4V similarly. For a 1V supply voltage change, only 987μV change is observed at the DAC output. Note that 1V of supply voltage change is an exaggerated situation and is used just to measure the change at the output. For a 1V of supply change we get 987μV of change which corresponds to -60.1dB of rejection. When the transient simulation power supply rejection result is compared with the AC PSR simulation result of -57.8dB it can be seen that the two values are very close. AC PSR result of -57.8dB translates as 1288μV at transient and it is close to 987μV of transient simulation result. The slight voltage difference between two results could be due to the fact that the -57.8dB PSR result is at 1Hz (DC) whereas the transient simulation

utilises a pulse whose actual frequency value is somewhere in the range of kHz to MHz.

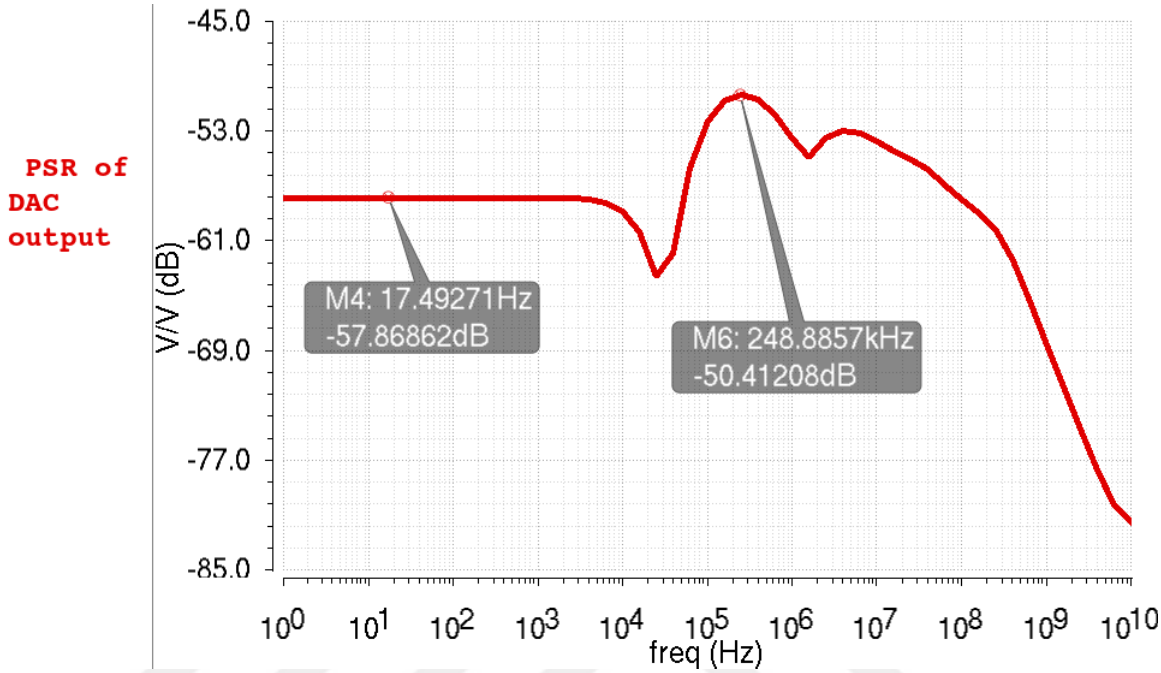

Figure 3.17. DAC block PSR simulation result.

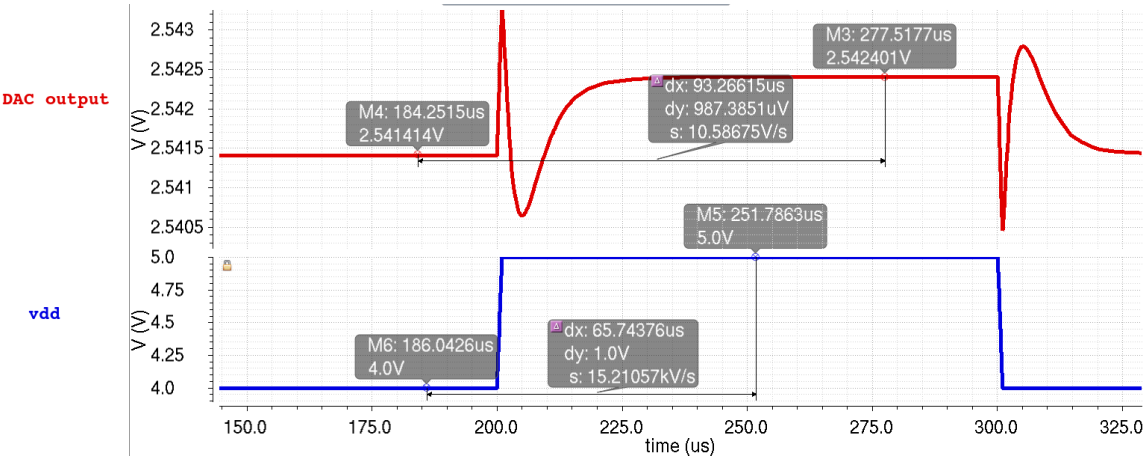

Figure 3.18. DAC power supply rejection transient simulation result.

3.4.6. DAC Top Level Simulation Results

To see the DAC behavior in the the actual Buck converter, the DAC model is removed and replaced with the actual DAC block. It has been seen that due to kick-back of the output comparators there is some switching noise at the DAC outputs.

Figure 3.19 shows two DAC high output voltages at the top level simulation run.

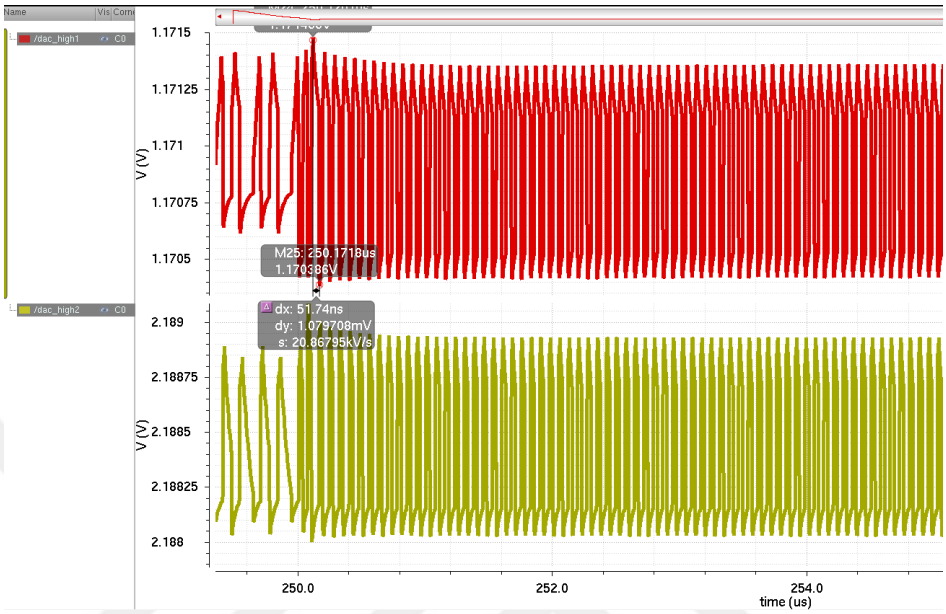

Figure 3.19. Top level simulation result of DAC outputs.

It has been seen that due to kickback from the output comparators, the DAC voltage has roughly 1mV peak to peak switching noise. It is less than the hysteresis voltage; however, it will deteriorate the output regulation. Thus, to reduce the kickback from the output comparators, an RC passive filter is used at the two outputs of the DAC. Then, this noise is almost reduced by 7 times (150μV) with the trade off at adding a resistor and a capacitor for each output. Figure 3.20 shows the DAC top level buck simulation results with RC filters at the outputs.

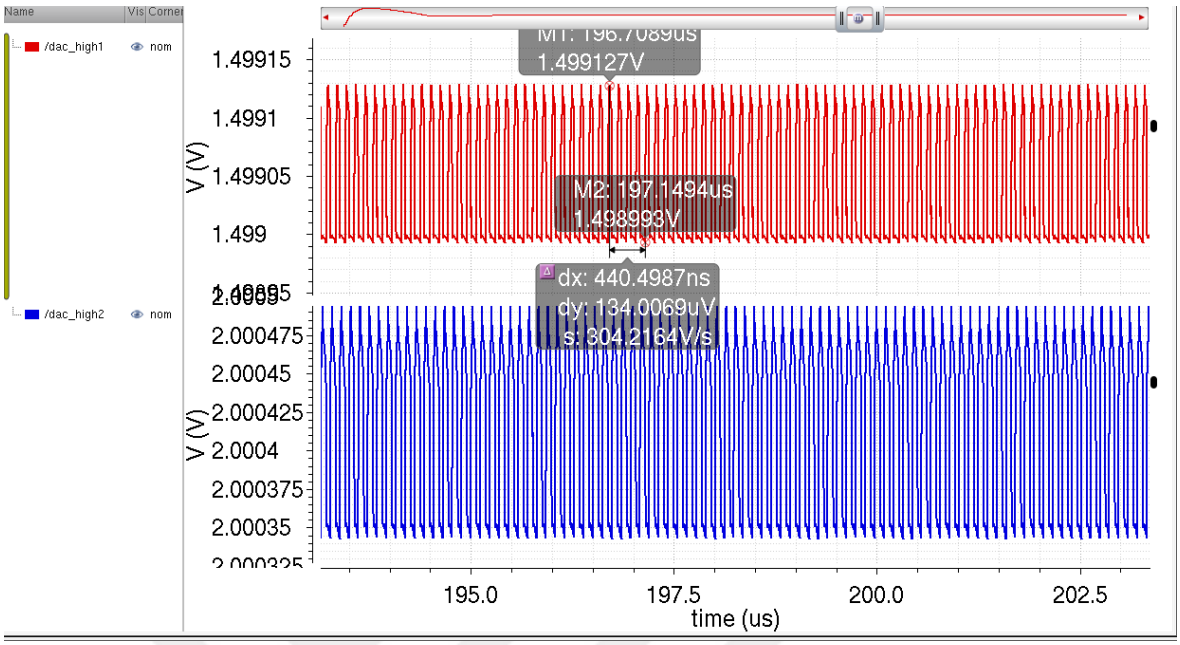

Figure 3.20. Top level simulation result of DAC outputs with RC filter.

3.4.7. Layout Design of DAC

Figure 3.21 depicts the layout design of the DAC block. Top left part is the folded cascode buffer, bottom part is the resistor ladder and the switches to choose the proper DAC voltage. At the right side part, the resistor ladder continues and above there are MIM capacitors used for compensation. Since MIM capacitors are formed by the top and the one below it, they can be placed above the MOS devices, to utilize layout area more efficiently. The layout dimensions of the block are 540μm to 120μm.

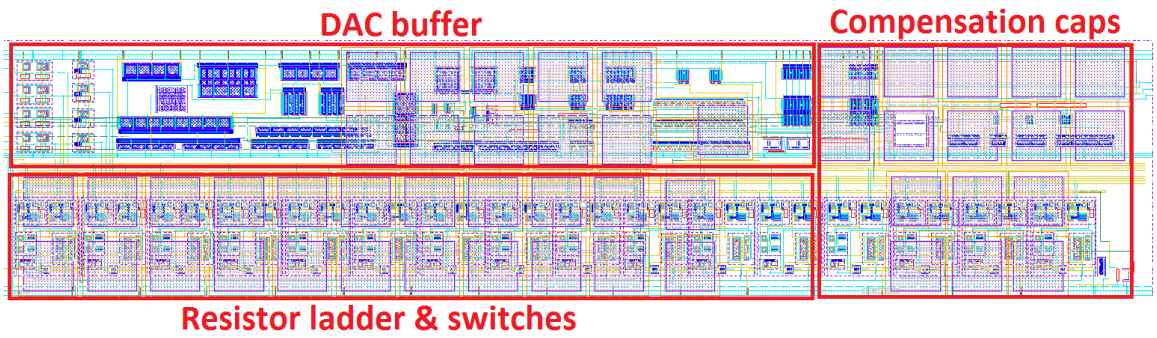

Figure 3.21. Layout design of the DAC block.

3.5. Output Voltage Comparator

Output voltage comparators monitor two output voltages and flag low and high signals when output voltages reach upper and lower thresholds. In the event of an abrupt load current demand, output comparator should be fast enough to detect the output voltage drop and the whole buck converter response time will be determined by this voltage drop. As a necessary consequence, output voltage comparators have to be as fast as possible with high enough gain to accurately detect that the output reaches a threshold value. The simplified circuit diagram of designed comparator is shown in Figure 3.22. The output voltage of the buck converter can be adjusted from 0.9 to 2.5V and the power supply voltage is between 3V and 5V. The input stage must ensure functionality for these input DC level and power supply conditions. To guarantee that input transistors are in saturation, resistor loads are used rather than PMOS transistors. The second stage is used as a level shifter by source followers to step down the DC level for the next stage. The third stage is the first gain stage and formed by PMOS diode and cross coupled diodes. To secure that the load impedance is positive, diode transistor sizes are larger than those of the cross coupled diodes. The second and third gain stages are similar to the first gain stage. The last stage is used to convert the differential signal to a single ended signal and also to add some extra gain. Note that, inside each output comparator block, the core is used twice; one for low threshold and one is used for high threshold comparison.

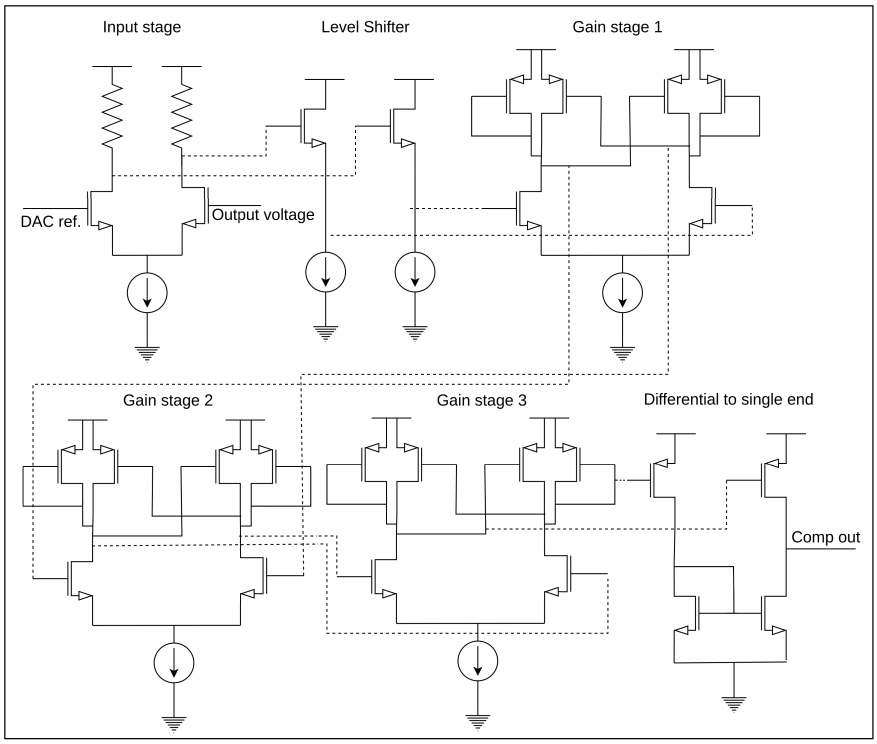

Figure 3.22. Output voltage comparator design.

The delay of the output voltage comparator is crucial for the performance of the buck converter because there will be extra under and over shoots at the output in the case of delays in the response time. Thus, several design iterations have been carried out to improve the comparator latency. During the analysis of the design iterations, it has been seen that increasing the open loop gain of the comparator doesn't help much to reduce the comparator delay. At each stage due to the input capacitor of the next stage and also self loading of the inner capacitors have to charge, and this is the root cause of the comparator delay. It starts with ramp and continues exponentially as classical voltage charge of a capacitor. As a reminder, a 1pF capacitor charging over a 100kΩ resistor from a 4V pulse voltage source is shown in Figure 3.23. At the top waveform is the output voltage of the capacitor and the below waveform is the derivative of this output voltage. The slope of the ramp is 40MV/s in the beginning and decays to asymptotically to 0MV/s. Initially, capacitor is charged faster and charging speed decreases when time passes.

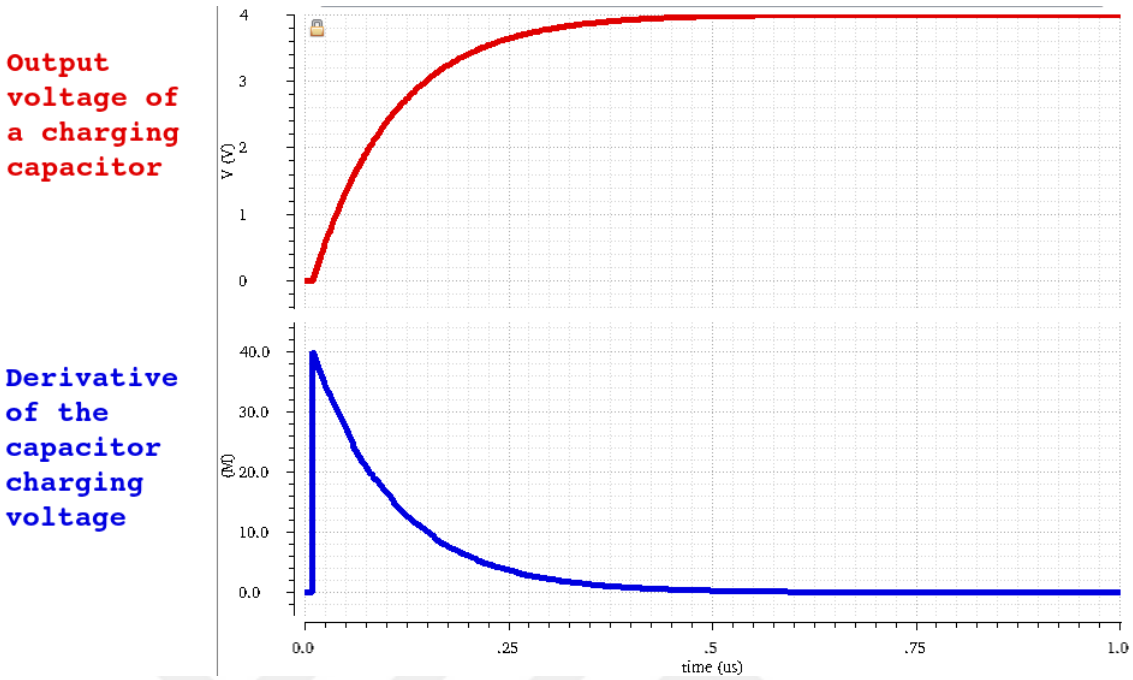

Figure 3.23. Capacitor charging showing output voltage and its derivative.

When same idea is applied to the comparator and analyzed with the same methodology, the results look similar. Figure 3.24 shows the simulation plot of the applied input as the top waveform, the one below is the differential output voltage of the first stage and the bottom waveform is the derivative of the first stage output differential voltage. The figure demonstrates that the charging starts with a steep ramp with slope 175M V/s and decreases to almost 0 V/s exponentially. If the steep ramp portion is used, then it will result in a rapid charging. Thus, 6 gain stages are cascaded to use the steep portion as much as possible. The total open loop gain of the 6 stages is more than 90dB which is more than needed; however, this gain is used to leverage the charging speed. In theory, if the number of the stages increases, it should decrease the settling time with the increasing number of stages. However, in reality, due to the delay of each stage this doesn't help much more than 6 to 8 stages. Figure 3.25 shows the output voltage derivative of the designed comparator for each stage. The first plot is the applied differential input signal, below are the output voltage derivatives of each stage and the bottom waveform shows the final output.

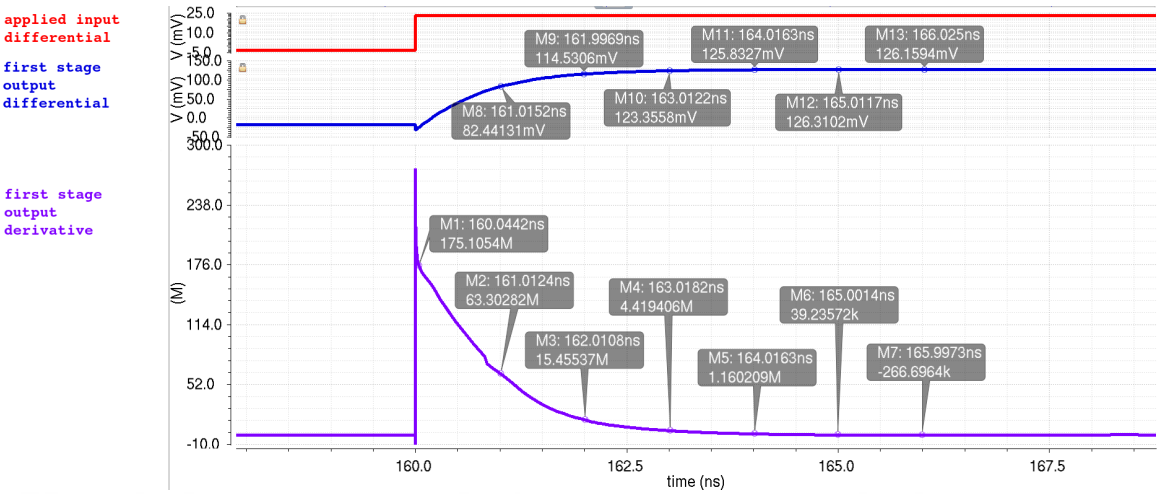

Figure 3.24. Comparator first stage charging graph with outputs derivative.

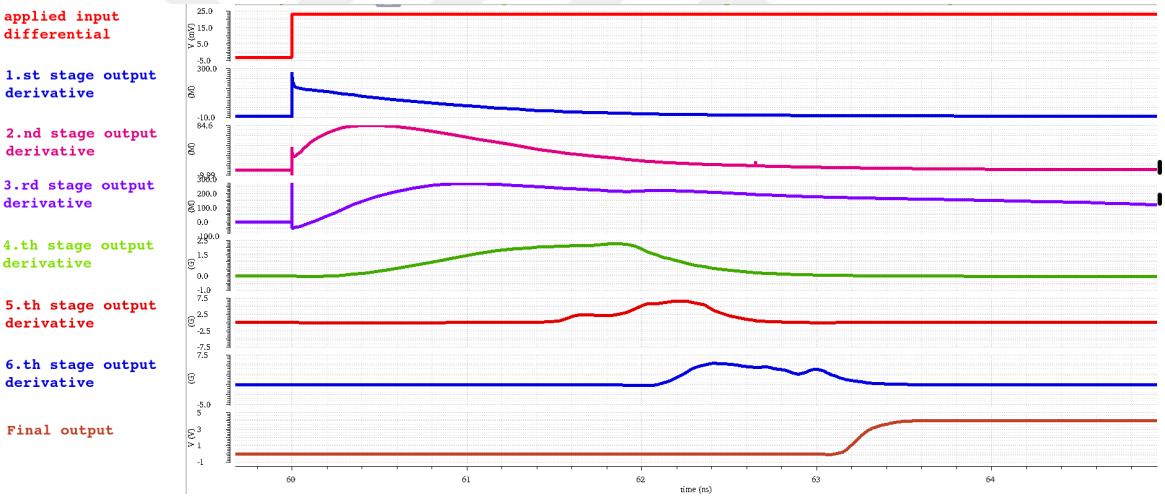

Figure 3.25. Comparator all stages output voltage with derivatives.

A simulation has been run with the designed output voltage comparator in a separate test bench to check rise and fall delays. Figure 3.26 shows the delay for low and high comparator outputs. At the top of the plot upper threshold is DAC high voltage threshold named as *dac_high*, lower threshold is DAC low voltage threshold and named as *dac_low*, and $Vbuck$ is the buck output voltage. Middle waveform is the *out_low* which is the output voltage comparators output flagging that output is below the lower threshold and bottom waveform is *out_high* which is the output voltage comparators high output flag signal. This result is for typical simulation conditions such as vdd 4V, all active devices are typical, all passive resistors are typical, and

10μA bias current is also typical. Low output delay is 7.29ns and high output delay is 7.25ns. A PVT simulation has been run for all four active device corners such as ss, ff, sf and fs; vdd either 3V or 5V; the outputs are either 0.5V or 2.5V; and the bias current is either 9μA or 11μA. Figure 3.27 shows all corner outputs for this corner run simulation. Low and high output delays are listed in Table 3.12.

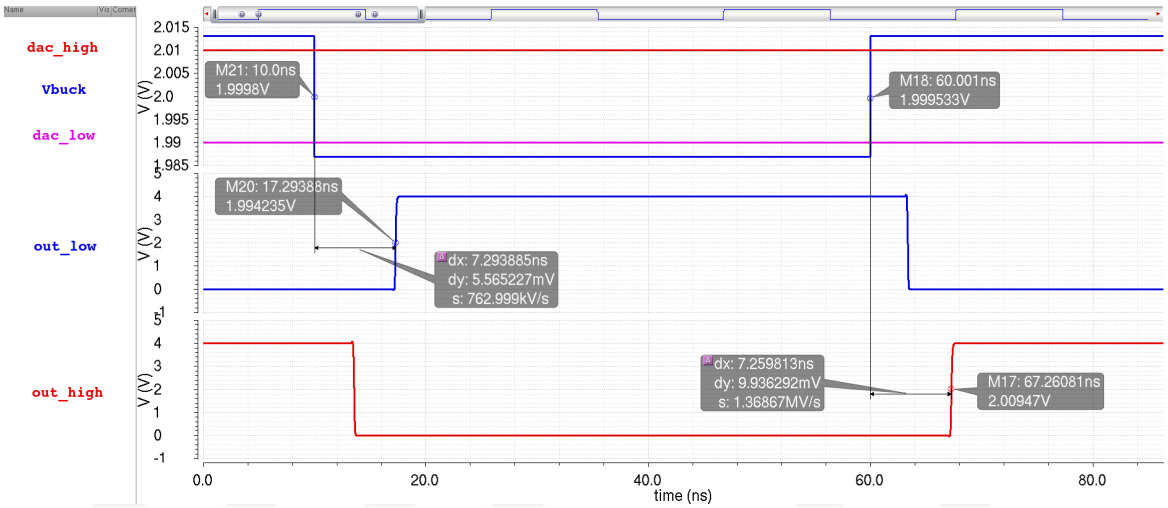

Figure 3.26. Output voltage comparator simulation result for typical.

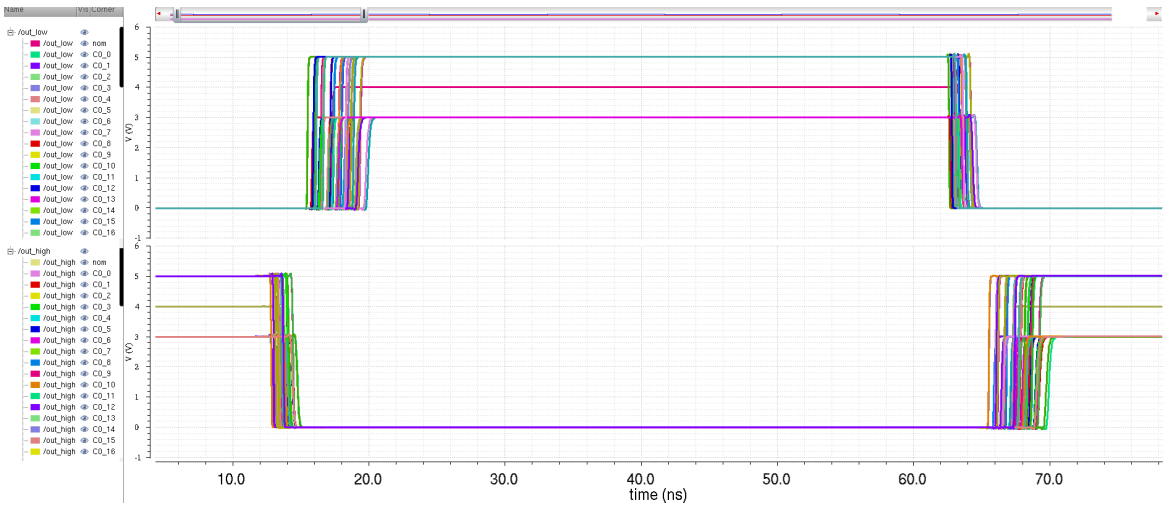

Figure 3.27. Output voltage comparator simulation result for PVT, output and bias corners.

Table 3.12. Output voltage comparator delay results for PVT run.

	Min. (ns)	**Typ. (ns)**	**Max. (ns)**
Comparator low out delay	5.4	7.3	9.8
Comparator high out delay	5.5	7.3	9.9

3.5.1. Layout Design of output voltage comparator

Figure 3.28 shows the designed output voltage comparator layout. At the left side current bias transistors are located, middle upper section is for the upper voltage threshold comparator, bottom one is the lower voltage threshold comparator. At the right side of the layout are the comparator output buffers since the outputs of this block are fed to many digital gates for logic processing. Buffering is required to prevent any loading effect and thus speed reduction. The layout dimensions of the block are 320μm to 70μm.

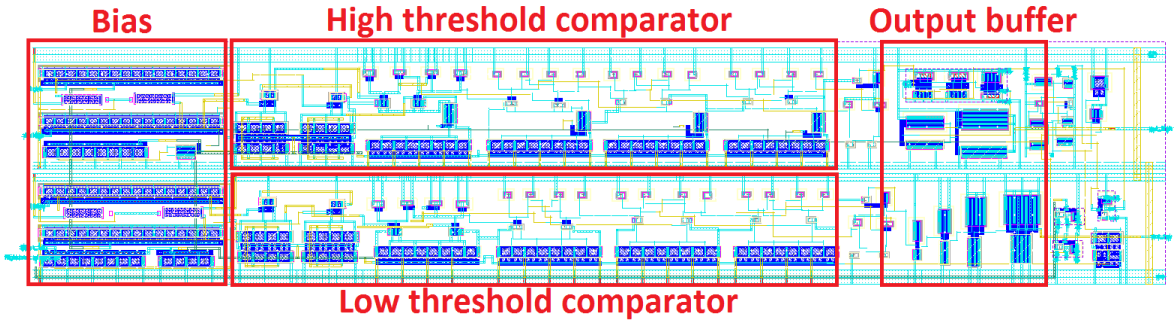

Figure 3.28. Layout design of output comparators.

3.6. Current Limiter Block

The current limiter block is generally used to limit the inductor and the input side PMOS switch current; otherwise, both the inductor and the PMOS switch could be damaged permanently. Figure 3.29 shows the block diagram of the current limiter block. In this design, a comparator compares the input PMOS switch drain as vsw node with respect to replica PMOS switch transistors (1 to 5000 ratio) with a current source to produce a similar voltage level. When the inductor current is increased to

a threshold level (which is defined by a 4 bit current DAC), the comparator flags the high current signal. Figure 3.30 shows the current limit of the comparator core. Input stage is formed with resistor loads to increase the input common mode range. The second stage is used to bring down the first stage voltage level. The third, fourth, and fifth stages are for gain and the last stage is used to convert differential signal to single ended signal and also add some extra gain.

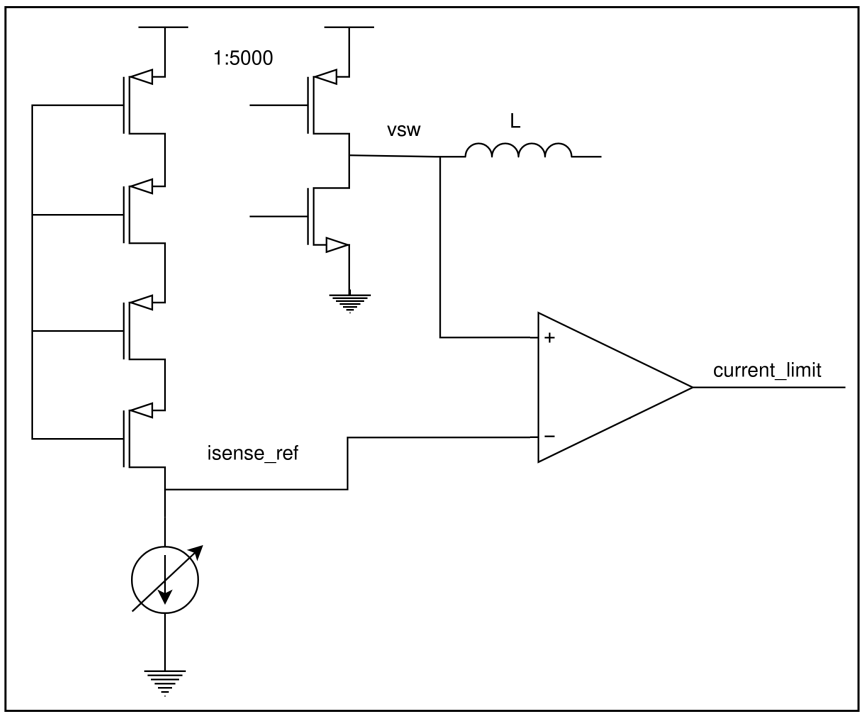

Figure 3.29. Current Limiter block diagram.

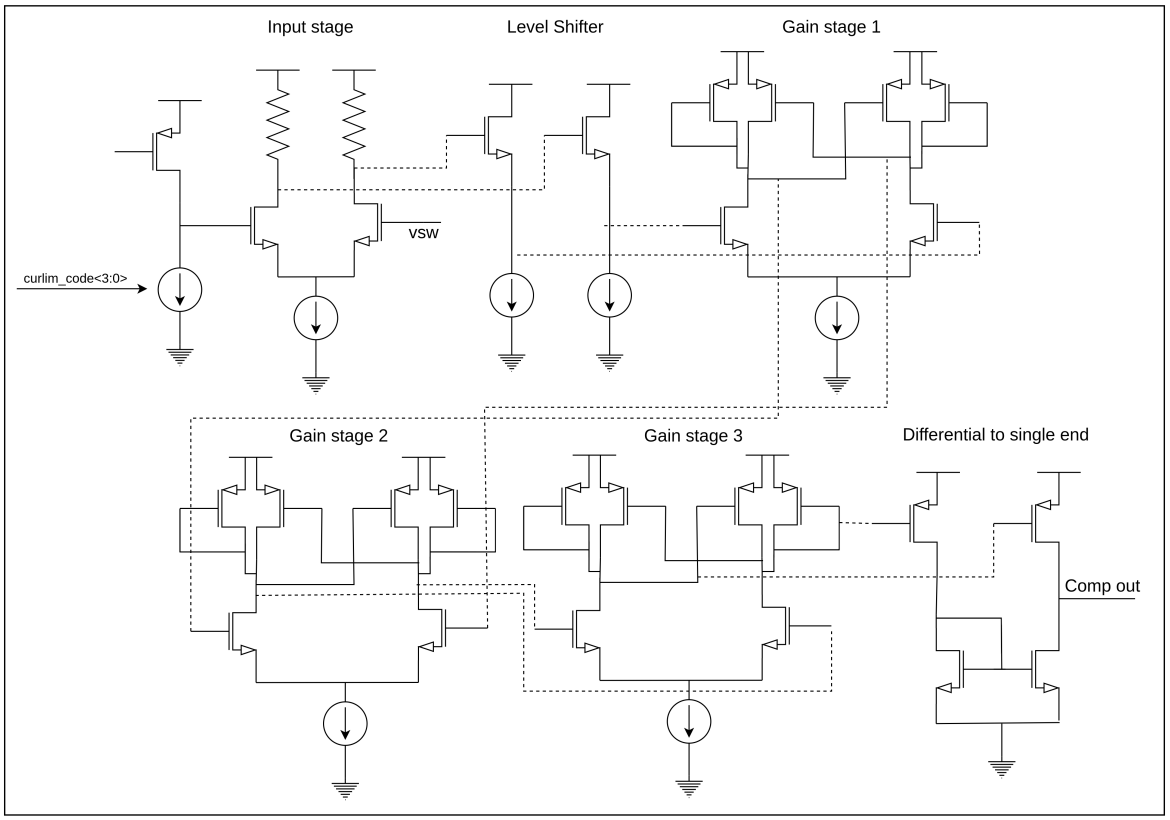

Figure 3.30. Current Limiter comparator core.

It is important to note that the offset current due to total internal delay will be different for different supply and output voltage settings. This offset current causes the inductor current to drift to higher values which results in an extra error for the current limit block. This is due to different inductor current slope for different input supply and output voltages. To calculate this offset value, the inductor behavior is written as

$$\triangle V = L\frac{\triangle I}{\triangle T}, \tag{3.2}$$

$$\frac{V_{in} - V_{out}}{L} = \frac{\triangle I}{\triangle T}. \tag{3.3}$$

$$\frac{V_{in} - V_{out}}{L}\triangle T = I_{offset} \tag{3.4}$$

$$For\ maximum\ inductor\ slope \Rightarrow \triangle I_{offset} = \frac{5V - 0.9V}{200nH} 10ns = 0.205A \tag{3.5}$$

$$For\ minimum\ inductor\ slope \Rightarrow \triangle I_{offset} = \frac{3V - 2.5V}{200nH} 10ns = 0.025A \tag{3.6}$$

When (3.2) is modified for the inductor being charged with the supply voltage, (3.3) is obtained. Finally, the expression is edited to find the offset current, and with (3.4) the offset current can be calculated. The highest inductor slope is for the case of V_{in} being highest (5V) and the output voltage V_{out} being lowest (0.9V). On the contrary, the lowest inductor current slope is formed by V_{in} being lowest (3V) and the output voltage V_{out} being highest (2.5V). Assuming that the total delay of the current limit comparator, controller, and driver delay is 10ns and the inductor value is 200nH. The inductor offset current is calculated for the highest and lowest inductor current slopes. (3.5) is the result of the offset current for highest inductor current slope and (3.6) is the result for lowest inductor current slope.

Simulations have been run to check the operation for the current limiter block. Figure 3.31 shows the typical (V_{in}=4V and V_{out}=1.8V) result of this simulation run. $isense_ref$ is the internal current reference signal and vsw is the switching node of the input PMOS and NMOS switch common drain node. When the current increases at both inductor and the PMOS switch, vsw node voltage is dropped due to the IR drop at the PMOS switch. When vsw node voltage reaches $isense_ref$ voltage, the current limit comparator output toggles, resulting in a high current flag signal.

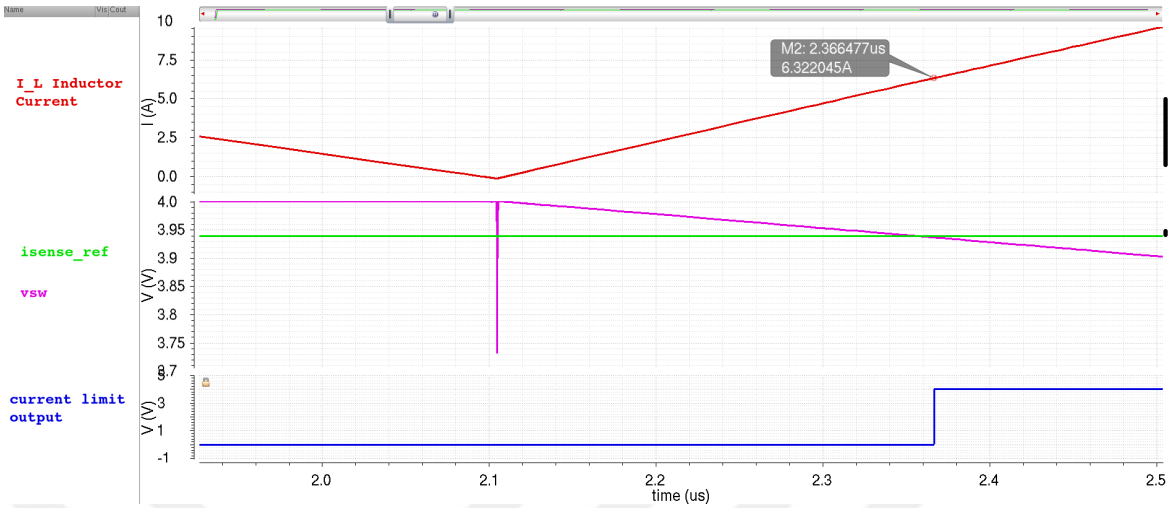

Figure 3.31. Current Limiter simulation result for typical.

Table 3.13. Current Limit code and set current settings.

Code	Current Limit (A)	Code	Current Limit (A)
0	2.86	8	5.26
1	3.12	9	5.65
2	3.40	10	5.96
3	3.64	11	6.20
4	4.06	12	6.61
5	4.30	13	6.84
6	4.60	14	7.15
7	4.84	15	7.38

The actual toggling values for the output of the current limiter are different than the set current limit values due to the delay in responding by the comparator. The comparator delay is multiplied by the current slope values, causing an offset in the current limit values. Furthermore, the supply voltage, output voltage, and inductor values change the inductor current slope. A PVT simulation has been run to calculate the comparator delays and to see the effect on the current limit value shift. Table 3.14 shows the typical, minimum, and maximum comparator delays.

Table 3.14. Current Limit comparator delay results for PVT run.

	Min. (ns)	**Typ. (ns)**	**Max. (ns)**
Comparator delay	8.3	9.6	14.1

PVT simulation has been run for each current limit code to see the minimum and maximum current values. Table 3.15 lists current values for each decimal code.

Table 3.15. Current Limit simulation results for PVT corners.

Current Limit decimal code	**Typ. (mA)**	**Min. (mA)**	**Max. (mA)**
0	2863	2711	3029
1	3098	2919	3297
2	3408	3240	3602
3	3643	3436	3868
4	4064	3867	4270
5	4300	4075	4536
6	4607	4377	4840
7	4841	4590	5106
8	5422	5202	5645
9	5655	5402	5912
10	5962	5712	6214
11	6195	5912	6480
12	6614	6345	6880
13	6846	6544	7145
14	7152	6851	7446
15	7384	7051	7712

A Monte Carlo simulation has been run to check the current limiter block for process and mismatch variation. 200 runs have been simulated both for process and mismatch. Table 3.16 shows process variation and Table 3.17 shows the mismatch related variation at the current limit results.

Table 3.16. Current Limit Monte Carlo 200 run for process.

	Min. (A)	**Max. (A)**	**Mean (A)**	**Standart deviation (A)**
Current limit setting for 8 code	5.42	5.5	5.45	0.015

Table 3.17. Current Limit Monte Carlo 200 run for mismatch.

	Min. (A)	**Max. (A)**	**Mean (A)**	**Standart deviation (A)**
Current limit setting for 8 code	4.65	6.24	5.45	0.31

3.6.1. Layout Design of Current Limiter Block

The layout design of the current limit block is depicted in Figure 3.32. Input bias transistor is located at the top left of the layout. Next is the replica PMOS switch devices used to mimic the input PMOS up switch. Right top portion is the offset current setting to change the current limit value if needed. Finally, the bottom part of the layout is the comparator core part. The layout dimensions of the block are 90μm to 190μm.

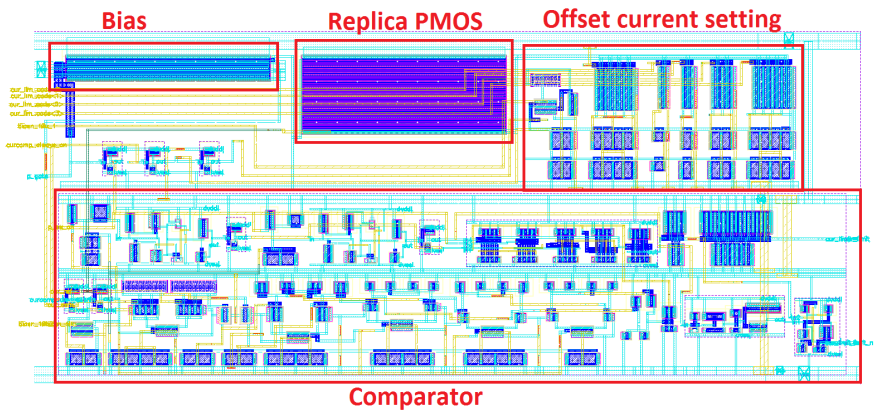

Figure 3.32. Layout design of the current limit block.

3.7. Active Diode Comparator

The inductor current must be monitored not to go beyond a maximum level and not to go below zero; otherwise, the inductor will discharge the output. To detect the inductor current reaching zero value, an active diode comparator is used. The input NMOS switch drain node named vsw is monitored and compared with a replica of the NMOS device (1 to 5000 ratio). Also, due to inherent delay of the blocks, inductor current must be detected with an offset value to compensate the turn off delay of the NMOS and inner blocks. A current DAC is used to change this offset value. Figure 3.33 shows the active diode comparator block diagram.

As expressed in section 3.6, there will be some offset current due to active diode comparator delay in addition to the controller and driver propagation delay. This will cause the inductor current to drift to negative values which will decrease the output voltage and efficiency. To find the inductor offset current, the inductor current formula is rewritten as

$$\triangle V = L\frac{\triangle I}{\triangle T}, \tag{3.7}$$

$$\frac{-V_{out}}{L}\triangle T = \triangle I_{offset}. \tag{3.8}$$

$$For\ maximum\ inductor\ slope \Rightarrow \triangle I_{offset} = \frac{-2.5V}{200nH}10ns = -0.125A \tag{3.9}$$

$$For\ minimum\ inductor\ slope \Rightarrow \triangle I_{offset} = \frac{-0.9V}{200nH}10ns = -0.045A \tag{3.10}$$

When (3.7) is arranged for the inductor being discharged we get (3.8). The inductor discharge slope is highest is for the highest output voltage and the inductor discharge slope is lowest for the lowest output voltage. When the inductor discharge current is

used to calculate the highest offset current we get the result in (3.9) for V_{out}=2.5V. The lowest inductor offset current is obtained as in (3.10) for V_{out}=0.9V.

Figure 3.34 shows the comparator core. The first stage is formed by PMOS diodes loaded with resistors. Second and third stages are similar to the output voltage comparator gain stages as NMOS input with diode and cross coupled diode PMOS loads. The last stage is used to convert the differential signal to a single ended signal also add some extra gain. Figure 3.35 shows the simulation result of the active diode comparator for typical settings (V_{in}=4V and V_{out}=1.8V). The top signal is the inductor current and the two signals below are vss as 0V and vsw node voltage. The bottom signal is the active diode comparator output signal. This simulation plot shows that the inductor current goes below zero current (-220mA) due to delays. To compensate for the comparator, controller logic, and NMOS turn off delays, an offset is used to increase the active diode current to positive values. When used with offset decimal code of 4, current goes to 20mA positive value which is shown in Figure 3.36.

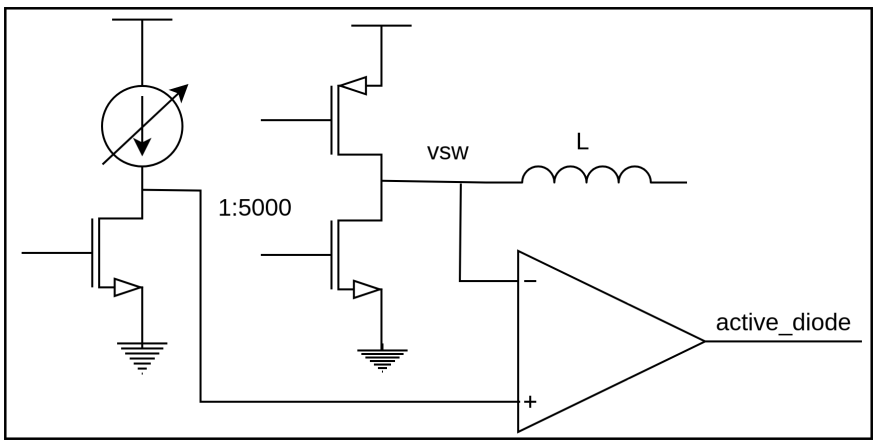

Figure 3.33. Active diode comparator block diagram.

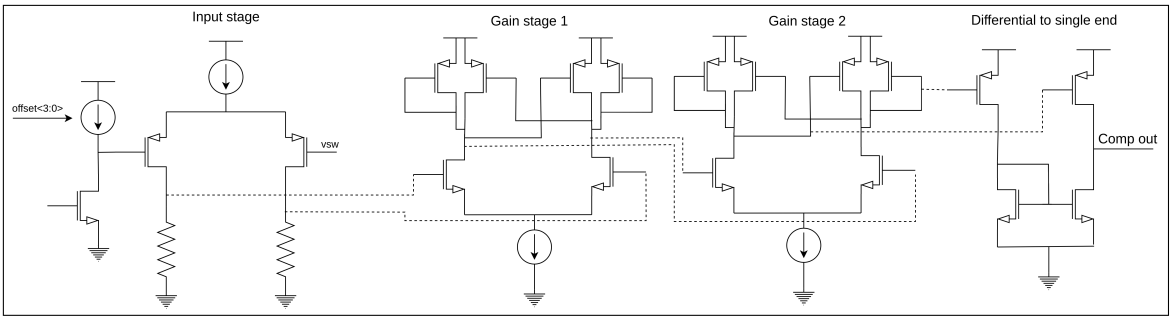

Figure 3.34. Active diode comparator core.

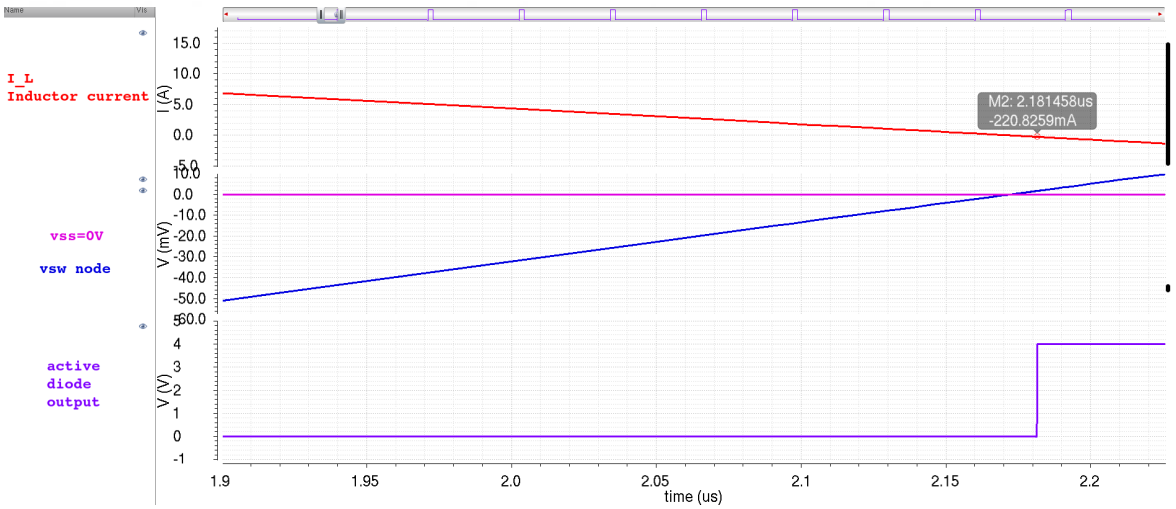

Figure 3.35. Active diode comparator simulation for offset code 0.

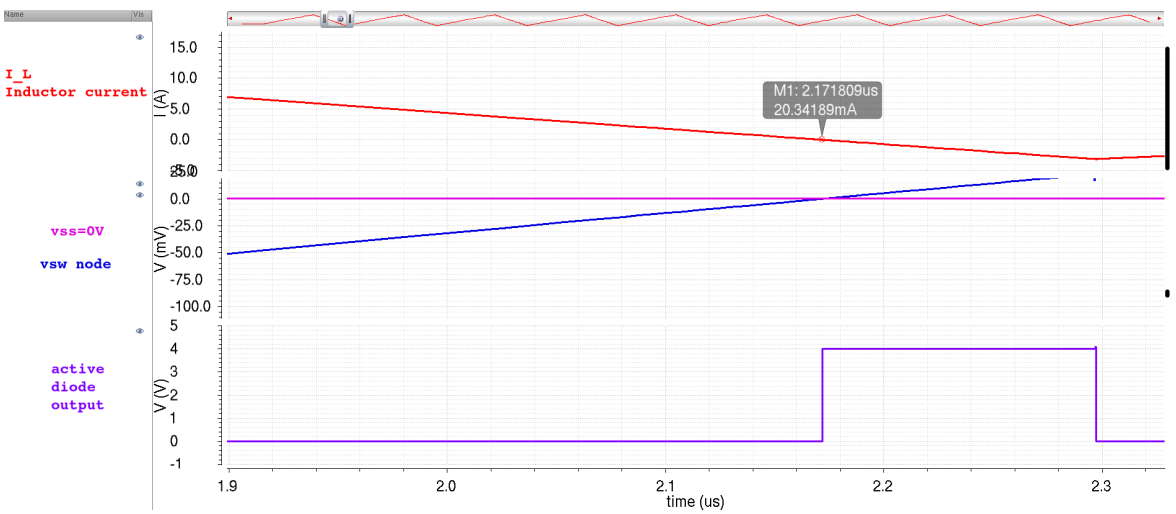

Figure 3.36. Active diode comparator simulation for offset code 4.

Table 3.18. Active diode offset code and current settings.

Code	**Current Limit (mA)**	**Code**	**Current Limit (mA)**
0	-220	8	254
1	-158	9	315
2	-97	10	376
3	-36	11	437
4	20	12	494
5	82	13	554
6	142	14	615
7	204	15	676

The response time of the active diode comparator is an important design goal since the inductor current can go to quite negative values and can discharge the output capacitors. A PVT simulation has been run to check the active diode comparator delay. Table 3.19 shows the comparator delay for typical, minimum, and maximum values.

Table 3.19. Active diode comparator delay results for PVT run.

	Min. (ns)	**Typ. (ns)**	**Max. (ns)**
Comparator delay	5.1	8.7	11.3

3.7.1. Layout Design of Active Diode Comparator

Figure 3.37 shows the layout design of the active diode comparator. The top part is the offset current setting to change the active diode setting if needed and also this portion includes the input NMOS switch replica device. The bottom part of the layout is the comparator core. The layout dimensions of the block are 70μm to 260μm.

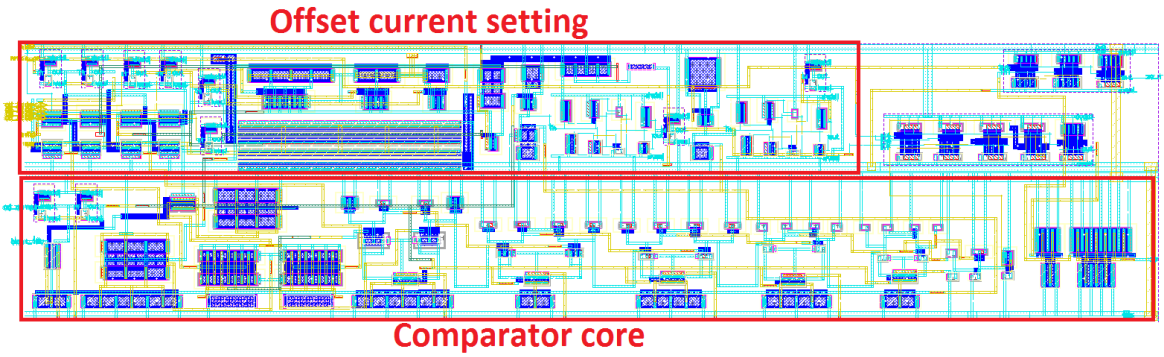

Figure 3.37. Layout design of the active diode block.

3.8. Bottom Current Comparator

The bottom current comparator is used to monitor the inductor current; if the current goes below a threshold value, this block creates a flag signal such that the controller uses this signal to push the operation as much as possible to Continuous Conduction Mode (CCM). At heavy load conditions, if the bottom current comparator is not used, the inductor current goes to its maximum limit, then discharges and stays at zero current for some portion of the time, which causes undesired frequency noise. Different architectures have been presented in literature for bottom current comparator [39], [40], [41].

In this study, bottom current comparator is formed by combination of current limit and active diode blocks with the addition of some offset at each block. A small control logic combines both comparator outputs and forms a single bottom current flag signal. Figure 3.38 shows the simplified circuit diagram of the bottom current comparator. It is necessary that both blocks will track every current value which could be present during the input PMOS or NMOS switch is on. Both active diode and current limit sub blocks track the sensed current values and both blocks threshold levels are adjusted with offset currents. Thus, when PMOS switch is on, current limit comparator will track the inductor current and decide if the inductor current is above or below the current limit threshold. Similarly, when NMOS switch is on, the active diode comparator will track the inductor current and decide whether the inductor current is above or below the current threshold. Both active diode and current limit

comparator output and inverted signals are used. The input polarity is arranged such that the comparator outputs of both blocks will flag the bottom current detection signal. Oppositely, both comparator inverted outputs will reset the bottom current detection signal. This is done by using two OR gates at the inputs of the SR latch. The output of the SR latch is the bottom current detection signal. Both blocks have 3 configuration bits to change the threshold values. This is achieved by changing the applied offset bias currents.

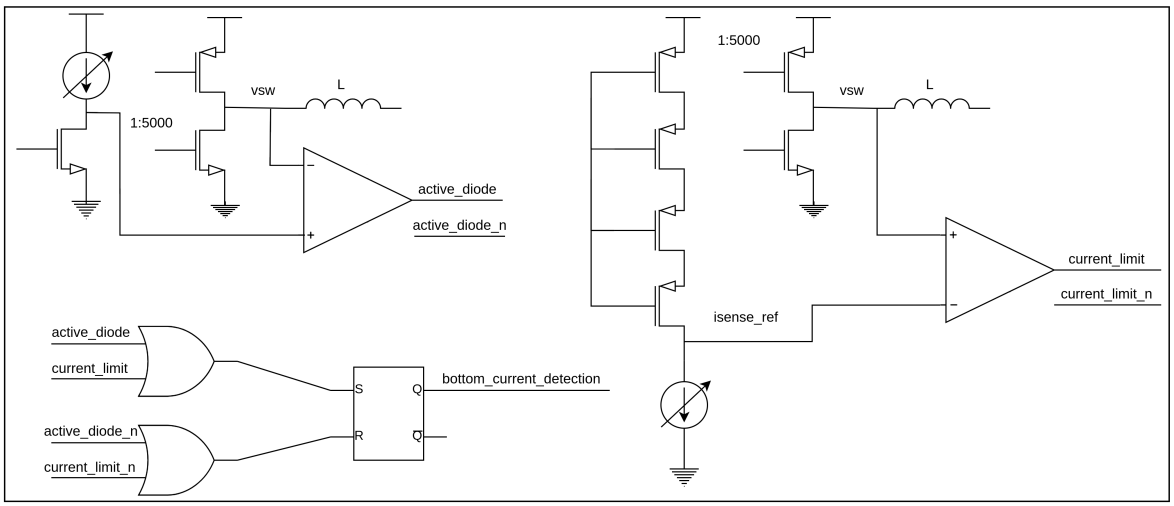

Figure 3.38. Bottom Current comparator simplified block diagram.

Block level simulation has been run to check the functionality of the bottom current comparator as shown in Figure 3.39 for decimal 4 offset code. The top waveform is the inductor current and the lower waveform is the bottom current detection. The final signals are the outputs of the inner active diode and current limit blocks. When the inductor current decreases and reaches 3.76A, the bottom current detection flags. When the inductor current increases and reaches 3.85A, then the inner current limit block flags that the current is above the limit and it turns off the bottom current detection flag. Note that at the lower inner block, there is a gap in the flag signals during change over from PMOS to NMOS switches. This is due to each block signal being masked with PMOS and NMOS gate signals. Thus, there is no glitch signal at the bottom current output signal. Another important point is that two thresholds are slightly different from each other because each block has some delay while the inductor

current is also changing. For active diode inner block, the inductor current decreases during comparator delay and for the inner current limit block, the inductor current increases during comparator delay. As a result, there is some delta value between the active diode rising flag and current limit falling flag which results in some offset value between the two block flag signals.

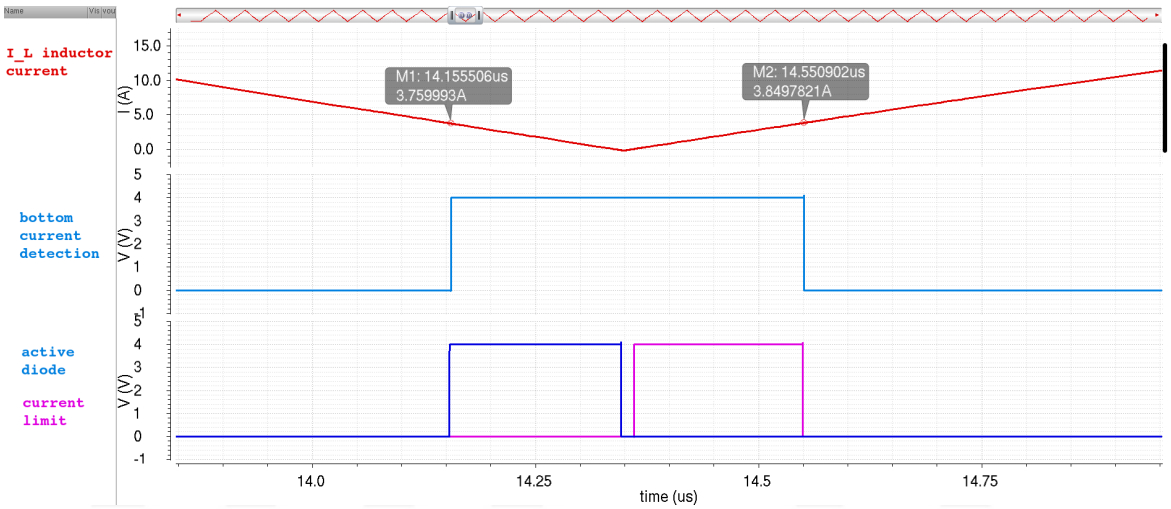

Figure 3.39. Bottom Current comparator simulation result for offset code 4.

A PVT and two output minimum and maximum voltage setting simulation has been run to check the active diode current bottom detection rise flag and the current limit fall flag. Table 3.20 lists all PVT and output combination simulation results for bottom current detection comparator.

Table 3.20. Bottom current comparator PVT simulation results for all offset codes.

	Typ. (mA)	**Min. (mA)**	**Max. (mA)**
Active diode rise for code 0	1775	1681	2005
Current limit fall for code 0	2038	1829	2376
Active diode rise for code 1	2038	1829	2376
Current limit fall for code 1	2301	2187	2548
Active diode rise for code 2	2793	2659	3059
Current limit fall for code 2	2888	2645	3248
Active diode rise for code 3	3314	3162	3597
Current limit fall for code 3	3272	3008	3651
Active diode rise for code 4	3759	3586	4062
Current limit fall for code 4	3850	3585	4221
Active diode rise for code 5	4278	4088	4598
Current limit fall for code 5	4233	3947	4625
Active diode rise for code 6	4765	4556	5103
Current limit fall for code 6	4696	4395	5097
Active diode rise for code 7	5281	5055	5635
Current limit fall for code 7	5079	4756	5502

3.8.1. Layout Design of Bottom Current Comparator

Figure 3.40 shows the layout design of the bottom current comparator. At the top left are the offset current setting for both active diode and current limit sub blocks. Active diode sub block is located at the bottom left of the layout. Current limit sub block is at the right bottom side of the layout and some digital logic is added to process both sub block signals and combine them to produce a single output signal. At the top middle is the replica devices of input PMOS and NMOS switches. The layout dimensions of the block are 110μm to 470μm.

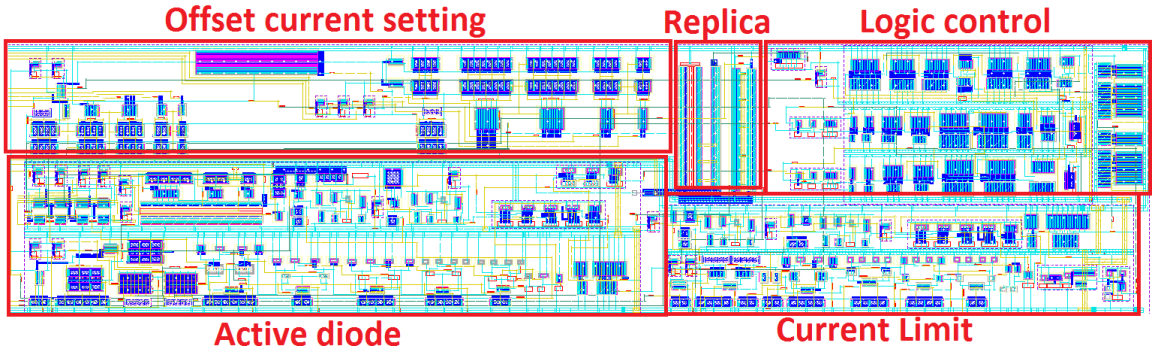

Figure 3.40. Layout design of the bottom current comparator.

3.9. Charge Pump Block

The buck converter outputs are selected between 0.5V and 2.5V and the supply the voltage can vary between 3V to 5V. When the output voltage is 2.5V and the supply voltage is 3V, the gate to source voltage of the output select switch will be 0.5V. This will cause the switch to exhibit a very high resistance, resulting in a poor current driving capability. To overcome this issue, a charge pump is used to boost the supply voltage to 5V and drive the output select switches. Figure 3.41 shows the simplified idea of the designed charge pump. Two comparators monitor the charge pump voltage and when the voltage goes below the lower threshold (4.9V), the comparator enables the ring oscillator and the charge pump core increases the voltage. When it reaches the upper threshold voltage (5V), the ring oscillator and the core cease operation.

Figure 3.42 gives a more detailed perspective of the designed charge pump. This configuration shows one extra comparator which is used to detect the charge pump start-up finalization and which goes to the main controller to produce the all_ref_ok signal. Charge pump functionality can be summarized as follows; initial charge pump starts with por_start signal. When cp_low flag is high and cp_high flag is low it means that the charge pump voltage is below the target threshold. Thus, these conditions enable the seven inverter stages oscillator by enabling the osc_enable signal. It starts the clk <1:7> signals which are used to drive the charge pump units. These charge pump units are the core of the design which produces the charge pump output voltage. The middle two blocks are used to select and produce nwell potential used at the charge

pump units. A comparator is used to compare the vdd supply voltage with the charge pump output voltage and produce two signals *vcp_big* and *vdd_big* signals which are the inverted versions of each other. Depending on these signals, the n-well selector PMOS switches connect the n-well pin of the charge pump units either to vdd or to charge pump output voltage. Charge pump units need the higher potential to drive the PMOS n-wells to this voltage level. Figure 3.43 shows the charge pump unit. Inside the charge pump, there is non overlap logic which is very crucial. Without the overlap logic, the efficiency would be degraded by the short circuit current through the two cross coupled inverters. The basic idea is that a capacitor charges with vdd supply voltage when the inverter output is at 0V and the inverter input is vdd. When the inverter input goes from vdd to vss, the output voltage goes to vdd and the capacitor bottom node becomes vdd. As a result, the capacitor top node becomes twice the vdd and this voltage results in a charge transfer from the pump capacitors to the bank capacitor (which is much bigger than pump capacitors). When the input signal toggles, other inverters transfer charges to the capacitor bank similarly. This operation continues until the capacitor bank voltage reaches 5V. Then, the comparator flags *cp_high* signal and *osc_enable* signal goes low and the charge pump ceases operation.

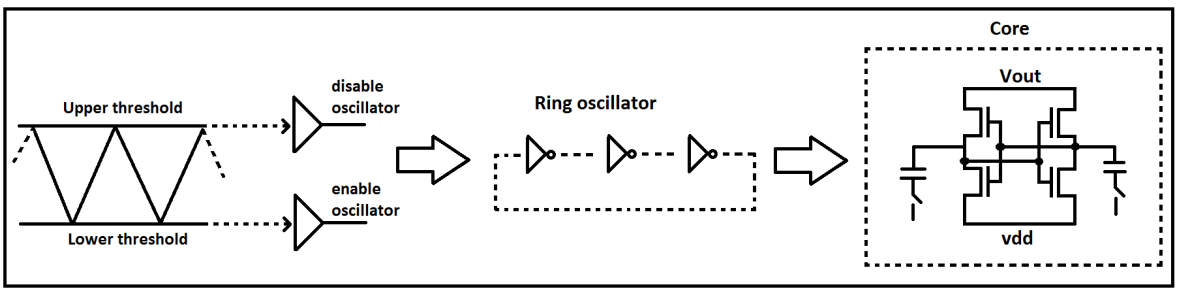

Figure 3.41. Charge pump simplified idea.

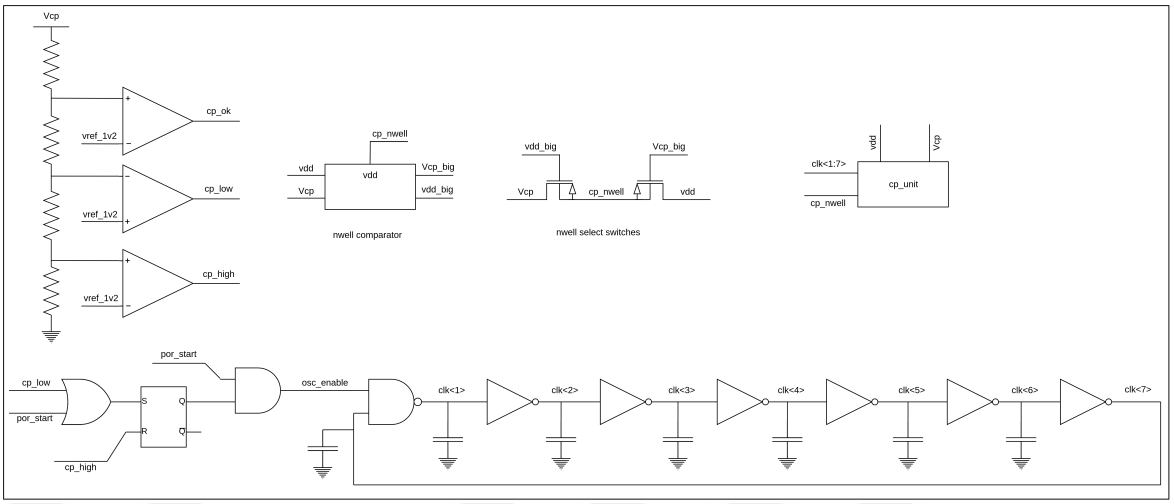

Figure 3.42. Charge pump block diagram.

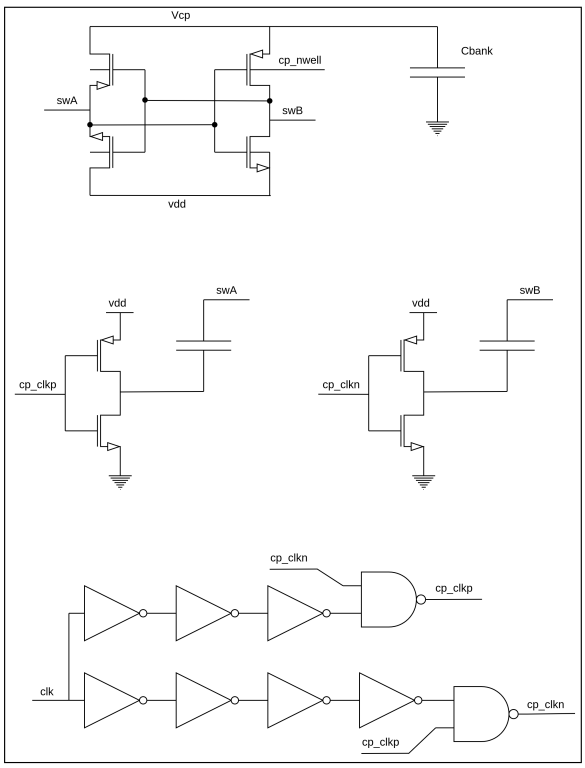

Figure 3.43. Charge pump unit simplified design.

Charge pump comparators are designed to have three stages since the charge pump comparator does not need to be too fast and have a high gain. It compares 1.2V band-gap with resistor division of the charge pump voltage. Figure 3.44 shows the simplified design of the charge pump comparator. The first and second stages have

NMOS input transistors and PMOS diode loads. The third and last stage is designed for differential to single end conversion and also some extra gain.

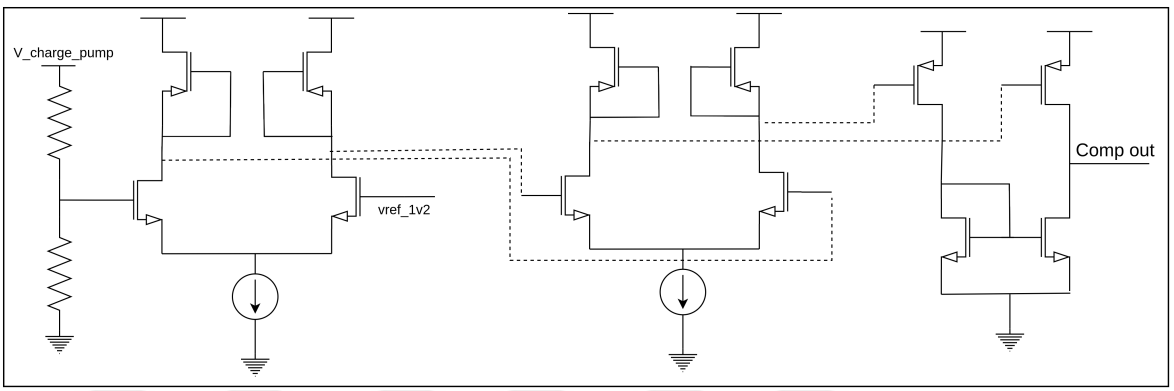

Figure 3.44. Charge pump comparator design.

3.9.1. Charge Pump Simulation Results

The designed charge pump is simulated to observe the functionality. Figure 3.45 depicts the startup simulation result of the designed charge pump with top level of the buck converter. It starts with *por_start* signal coming from the bias block. Since the charge pump output voltage is initially 0V, *cp_low* signal is high and *cp_high* signal is low. Thus, *osc_enable* turns high and the charge pump inverter oscillator stage turns on. Each charge pump unit pumps charge to bank capacitor and the output voltage starts to rise. At the lowest waveform, only one signal of the inverter oscillator clock is shown (clk <1>). Other clock signals have similar wave forms with only some phase shift with respect to each other. When the output voltage reaches 4.4V, *cp_ok* signal becomes high, which is used at the controller block to produce all_ref_ok signal. Note that, due to comparator delay, the voltage ok signal toggles at 4.424V. Then, with the increasing of the output voltage *cp_low* toggles from high to low when the output voltage reaches 4.94V and *cp_high* signal goes high when the output voltage reaches 5.06V.

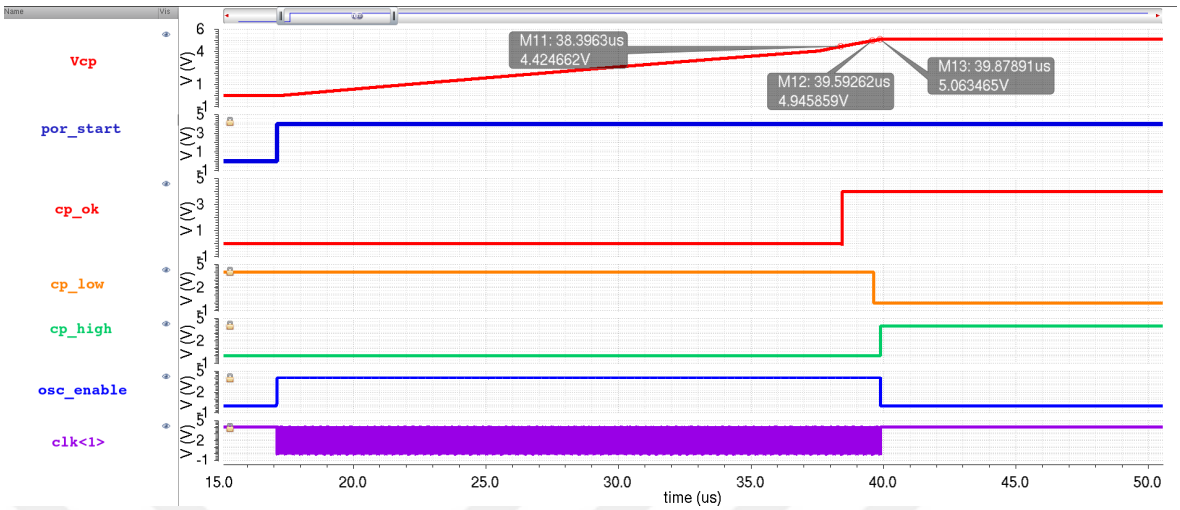

Figure 3.45. Charge pump start-up simulation result.

Another important functionality of the charge pump is to change the n-well potential from vdd to the charge pump voltage if needed. This behavior ensures that the n-well is always at the higher potential and does not cause any issues at the PMOS devices in the cross coupled pumping stages. During the startup, and also if needed, due to supply voltage change, nwell comparator compares vdd to the charge pump voltage and decides which one has the higher voltage. Then, after this decision Vcp_big or vdd_big goes high and selects the PMOS nwell switch regarding this comparison. Note that, these two signals are the inverted versions of each other. Figure 3.46 displays the n-well selection decision. Initially, when the charge pump starts from 0V, the n-well comparator gives the decision of vdd being high and as a result vdd_big output is high and Vcp_big is low. PMOS select switches connect the vdd to cp_nwell. Then, when the charge pump voltage is higher than vdd being 4V, both comparator outputs are toggled and n-well select switches connect Vcp to cp_nwell. Note that, due to switching noise cp_nwell has a switching noise, however it does not affect the operation.

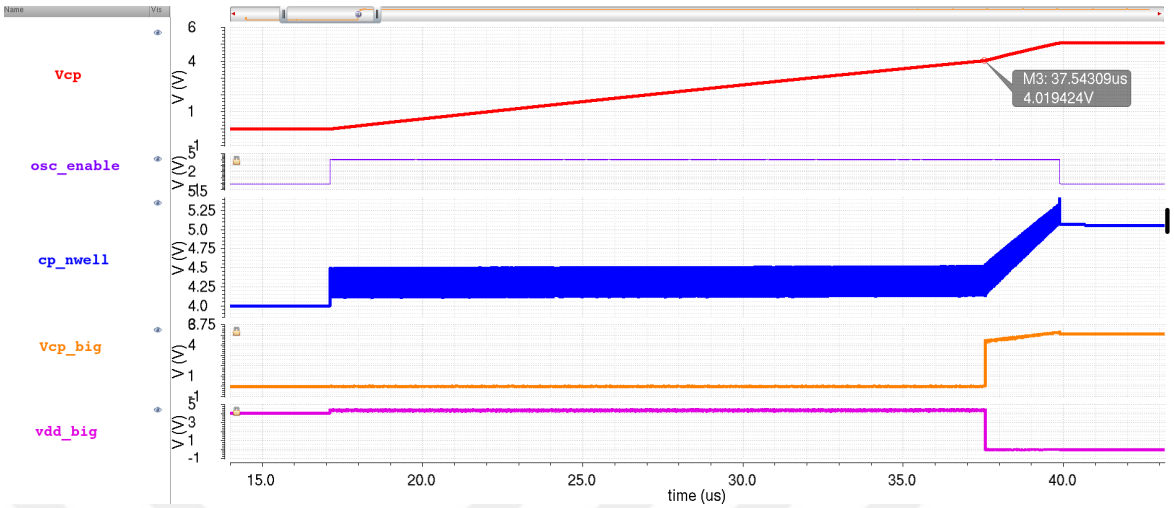

Figure 3.46. Simulation result showing the n-well selection.

To see the functionality of the charge pump at the mission mode, a load transient simulation has been run with the whole buck converter. Figure 3.47 depicts charge pump and relevant signals showing the functionality of the block. Due to switching of the output 1 and 2 switches, the charge and voltage on the charge pump bank capacitor depletes during the switching event. At some point, bank capacitor voltage decreases and reaches low voltage threshold and oscillator clock named clk <1> starts to toggle (only one oscillator clock is shown, other clocks are also toggling) and bank capacitor voltage increases and finally when it hits the high threshold it halts operation. This cycle repeats itself and bank capacitor voltage is kept between its lower and higher threshold.

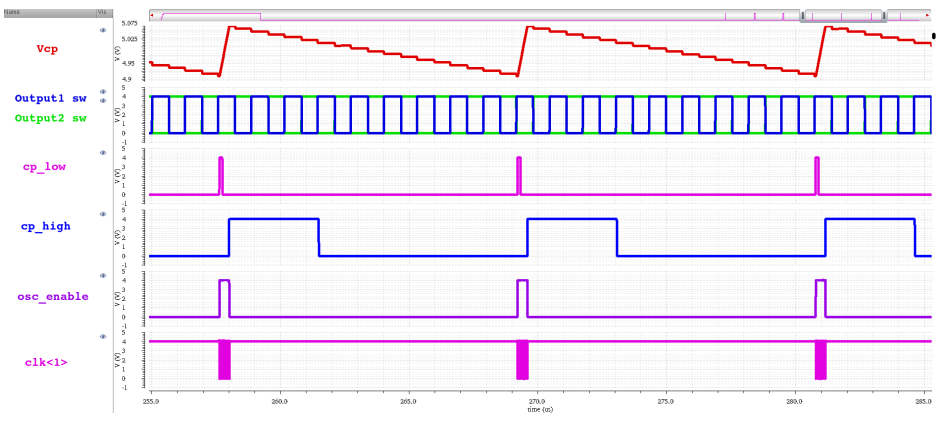

Figure 3.47. Charge pump simulation result with whole buck converter.

3.9.2. Layout Design of Charge Pump

Figure 3.48 shows the layout design of the charge pump block. Almost all layout area is occupied by charge pump units which are located inside the big rectangle. Comparators are located at the bottom left of the layout. Conditionally enabled ring oscillator resides at the middle bottom of the layout. Since charge pump block has relatively higher current values compared to other peripheral blocks, metal thickness and different metal layers are used at the charge pump unit outputs. The layout dimensions of the block are 840μm to 1180μm.

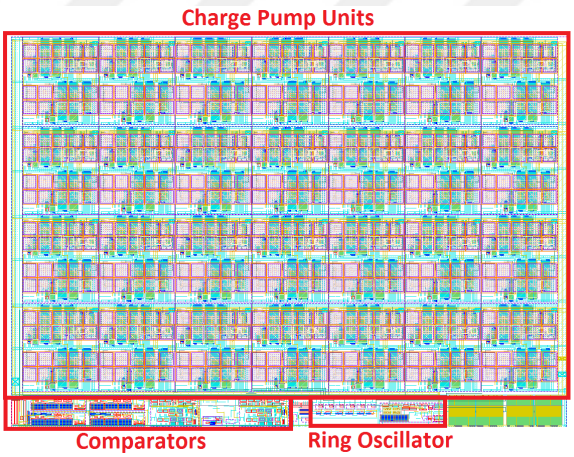

Figure 3.48. Layout design of the charge pump block.

3.10. Always On Block

This block is used to monitor comparator and switch signals. If there is no activity, then it turns off most of the blocks. If load current is detected then this block turns on all blocks to operate as always on mode. Figure 3.49 shows the simplified block diagram of the always on block. The main idea is that when there is activity low comparator and switching signals will be high and NOR output will be zero and PMOS will be on. As a result, Schmitt trigger output flags always on signal. Inversely, when there is no switching activity, the output voltage comparator low or switch up and down signals are zero and NOR output will be high. Discharging PMOS will be off and bias current charges the capacitor. After some time, depending on the bias current

and capacitor value, the bottom node of the capacitor will reach the Schmitt trigger threshold value and the Schmitt trigger toggles and activity on signal goes low. When always on signal goes low, some peripheral blocks are turned off to save power. This block is used to not to turn off the buck converter when there is a small load current at light loads.

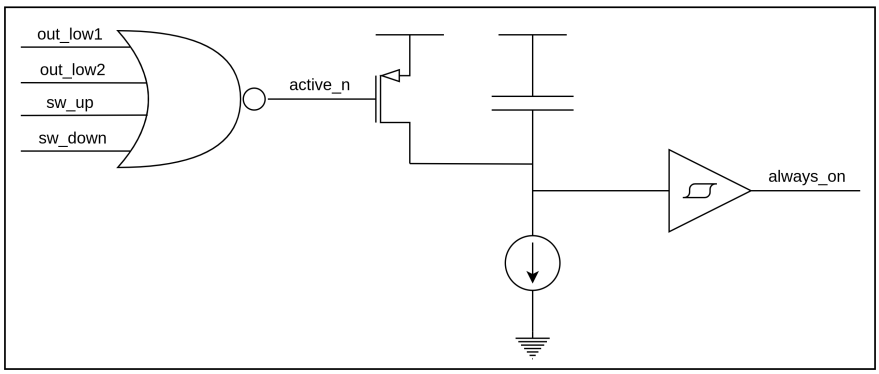

Figure 3.49. Always on block diagram.

Block level simulation is depicted in Figure 3.50. When *low_signal*1 goes high, always on signal immediately goes high as well. *cap_timer* is the the bottom node of capacitor and due to PMOS discharge switch it goes to 4V as vdd supply. When *low_signal*1 goes low, cap timer node starts to decline. When it reaches the threshold voltage of Schmitt trigger (1.67V) *always_on* signal goes low. The time between *low_signal*1 going to low and *always_on* going low is the time to let some blocks to settle before going to low power mode. A PVT simulation is run to check the settling time for all corner conditions and listed in Table 3.21.

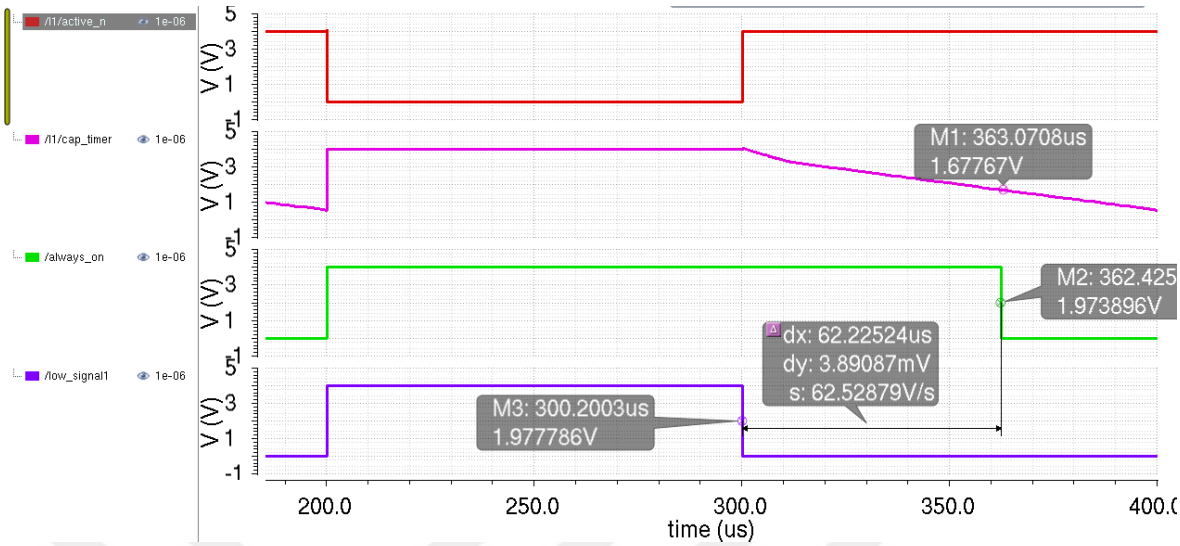

Figure 3.50. Always on block simulation result.

Table 3.21. Always on block PVT simulation results.

	Min. (μs)	**Typ.** (μs)	**Max.** (μs)
Settle time	36.6	62.2	90

3.10.1. Layout Design of Always On Block

Figure 3.51 shows the layout design of the always on block. PMOS capacitors are located at the top portion of the layout. The bias block is at the left middle and finally the Schmitt trigger, which is used as the comparator resides bottom middle of the layout. The layout dimensions of the block are 50μm to 90μm.

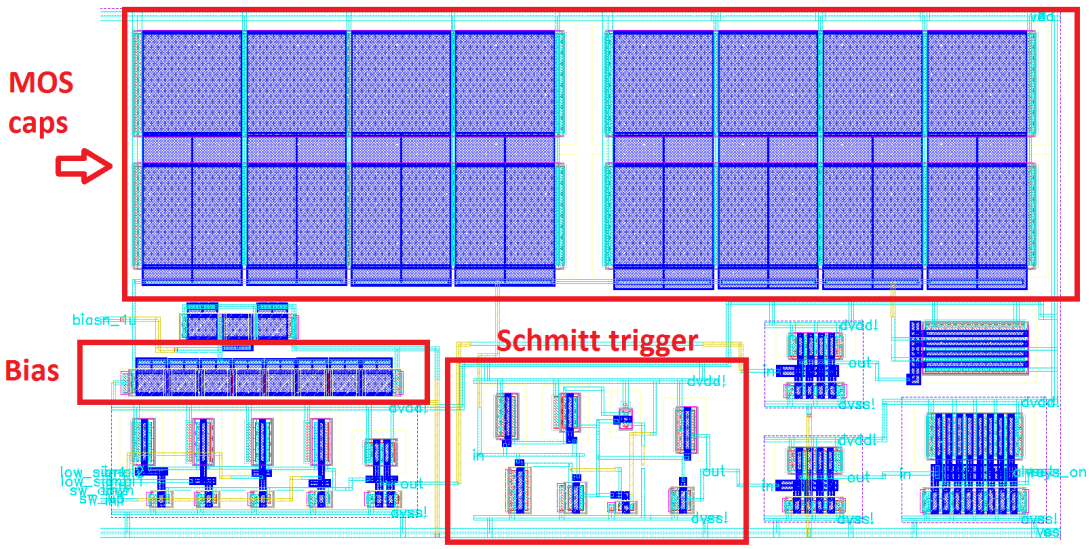

Figure 3.51. Layout design of always on block.

3.11. Frequency Counter Block

Frequency counter block is used inside the load balancing controller to measure the switching frequency of the inductor. Since the converter has two outputs two frequency counter blocks are used. Figure 3.52 shows the simplified circuit diagram of the frequency counter block. The operation can be summarized as follows; input up side switch (PMOS switch which connects the inductor to the power supply) gate signal is logical AND'ed with that output switch (connects the inductor to the selected output) on signal. Then, this signal is logical AND'ed with its 20ns delayed signal to produce a 20ns pulse signal. This 20ns pulse signal turns on the NMOS switch to charge a capacitor. Note that a parallel resistor is connected to the capacitor to change the decay of the voltage to adjust the voltage level. Then, this pulse voltage which is called as V_freq is measured by eight simple comparator blocks and converted to thermometric digital code outputs. Thermometric code is then converted to a three bit binary digital code which is fed to the load balancer block controller for further processing.

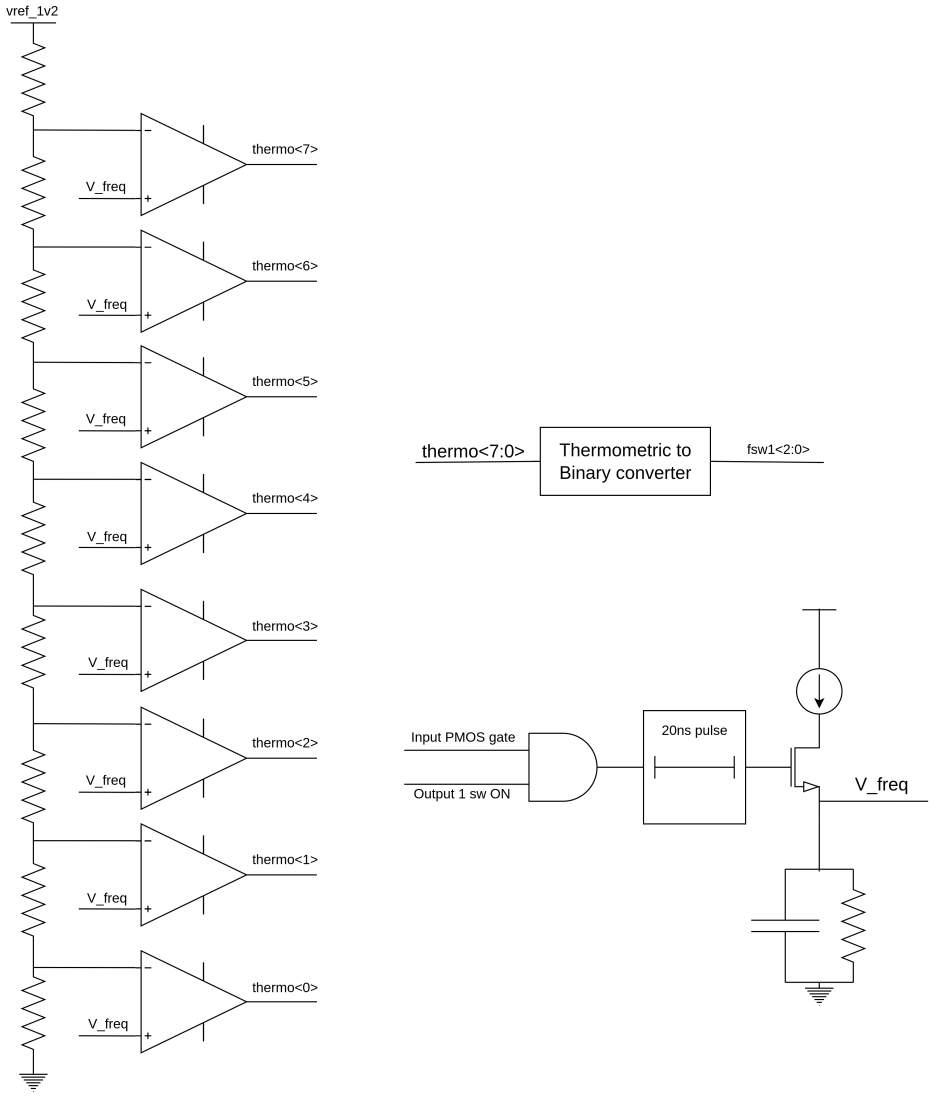

Figure 3.52. Frequency Counter block simplified circuit diagram.

Figure 3.53 shows the simulation result to illustrate the operation of the frequency counter. V_freq is the frequency voltage value and below is the counter value shown in decimal form for the sake of simplicity. This is done by applying the digital code to a Verilog-A block which converts the digital code to an analog voltage. Initially, the voltage is 0V and the code is zero (which is shown as voltage value). Then, voltage increases and digital code also increases. The decimal code value follows the analog voltage value by increasing step by step in the last part of the simulation waveform, the analog voltage reduces and the decimal code is changed from seven to six.

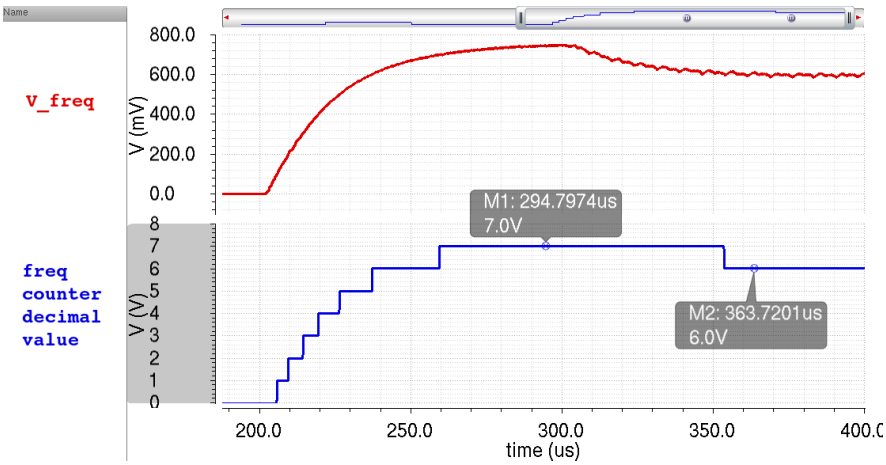

Figure 3.53. Frequency Counter functional simulation.

3.11.1. Layout Design of Frequency Counter Block

Figure 3.54 shows the layout design of the frequency counter block. Latches are placed at the top and right side of the layout. Comparators are placed in the middle of the layout and the resistor ladder is placed at the left side of the comparators. The layout dimensions of the block are 360μm to 490μm.

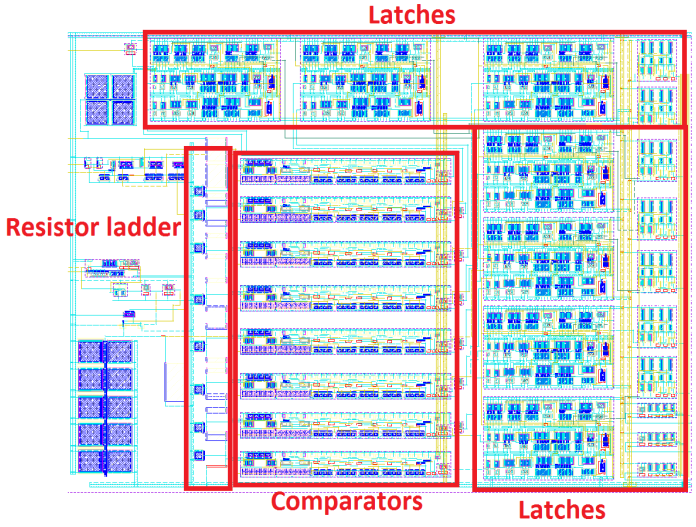

Figure 3.54. Layout design of frequency counter block.

3.12. Pulse Delay Block

The Pulse delay block is designed to produce an accurate delay which can be adjusted by digital codes. It is used to produce such a delay that the delay lock block compares the duty cycles and tries to adjust both outputs duty cycles such that the duty cycle of each output is enough to regulate its load current. To adjust the duty cycles, each delay lock block compares this delay with the low signal of the other output and tries to increase or decrease the delay time for each output to find an equilibrium point which suits both outputs. Figure 3.55 shows the simplified block diagram of the pulse delay block. In its simplest form, a capacitor is charged with a variable current source and when it reaches a threshold value, a comparator flags that it reached that target voltage. Primary coarse current source which is used to charge the capacitor is the output of the frequency counter and the secondary fine current source comes from the delay lock block. Both currents are summed and then used to switch if that output switch is on. When the output switch turns on, the summed current charges the capacitor and when voltage on the capacitor reaches 1.2V a comparator output toggles signaling that the timer value is reached. To produce a pulse waveform, an SR latch is used. The SR latch set pin is connected to output switch enable signal and the reset pin is connected to the comparator output. When the comparator reaches 1.2V, the SR latch is reset and the pulse waveform is obtained.

To prepare the pulse delay block for the next event, a discharge signal is used, which is a logical result of the inverted pulse signal AND'ed with that output switch enable or on signal. Pulse delay block has two outputs, one is named *delay*1 and other one is *delay*1_*plus*. *delay*1_*plus* output has a 2 bit digitally adjustable extra delay compared to the *delay*1 signal which will be explained in detail in the following section. Note that the actual design is much more complicated than the simplified block diagram as shown in Figure 3.55. Since each output has its own pulse delay block, a similar naming convention has been applied to output2 as; *delay*2 and *delay*2_*plus*.

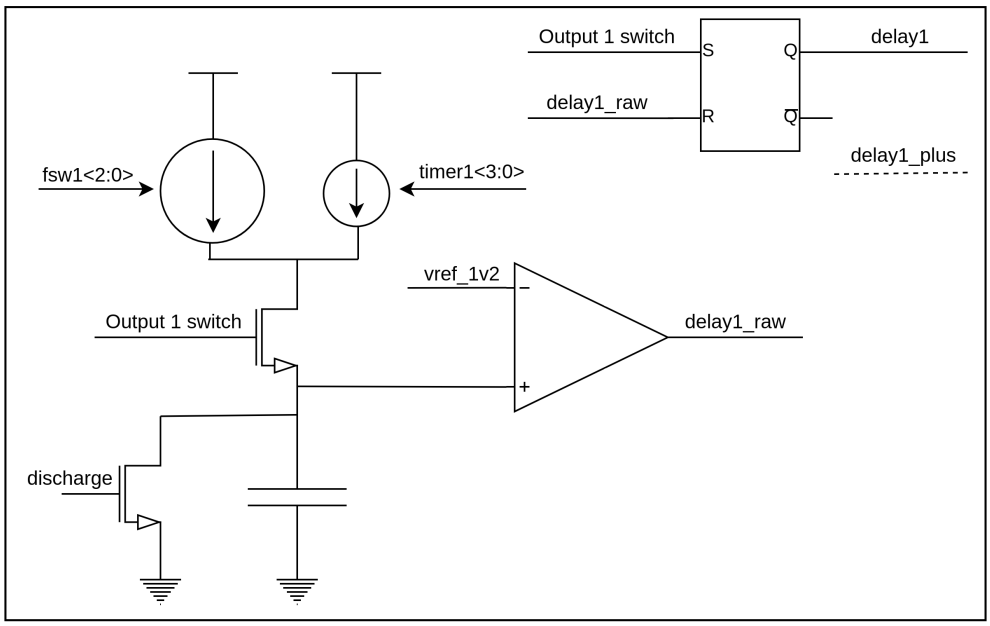

Figure 3.55. Pulse Delay block simplified circuit diagram.

To show the functionality of the pulse delay block, a simulation has been run and the results are depicted in Figure 3.56. V_cap is the capacitor voltage that charges with current, $vref_1v2$ is the 1.2V reference voltage for comparison. The waveform below is the output1 switch enable signal and the one below is the delay1 output signal and lowest signal is the discharge signal.

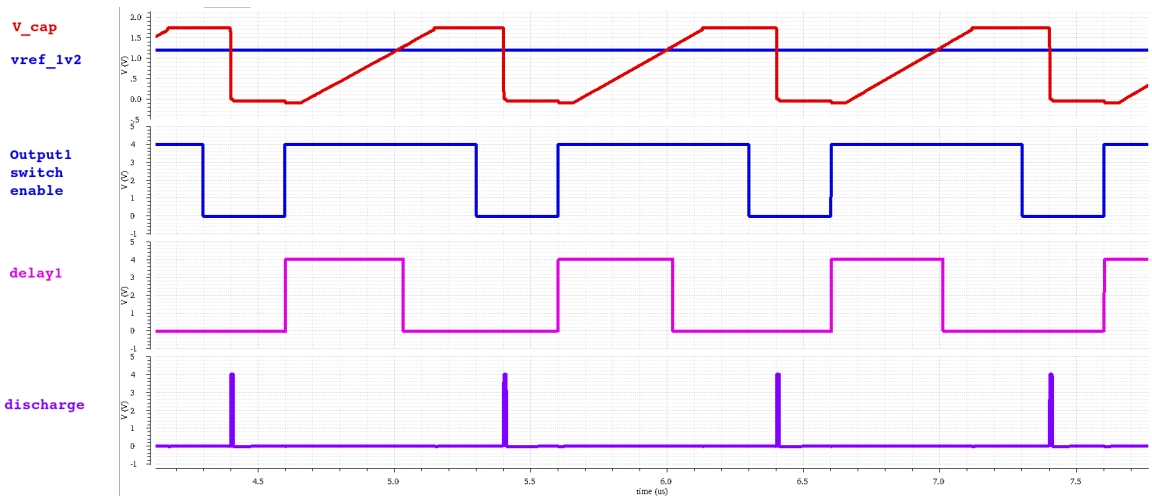

Figure 3.56. Pulse Delay block simulation result.

3.12.1. Layout Design of Pulse Delay Block

Figure 3.57 shows the layout of the pulse delay block. The area is mostly dominated by the bias current units which are placed in the top left section of the layout. Two discharge switches (one for *delay* and one for *delay_plus*) are placed at the right side of the layout. Two SR latches are placed at the bottom. The digital logic to process the signals is above the latches. The layout dimensions of the block are 540μm to 400μm.

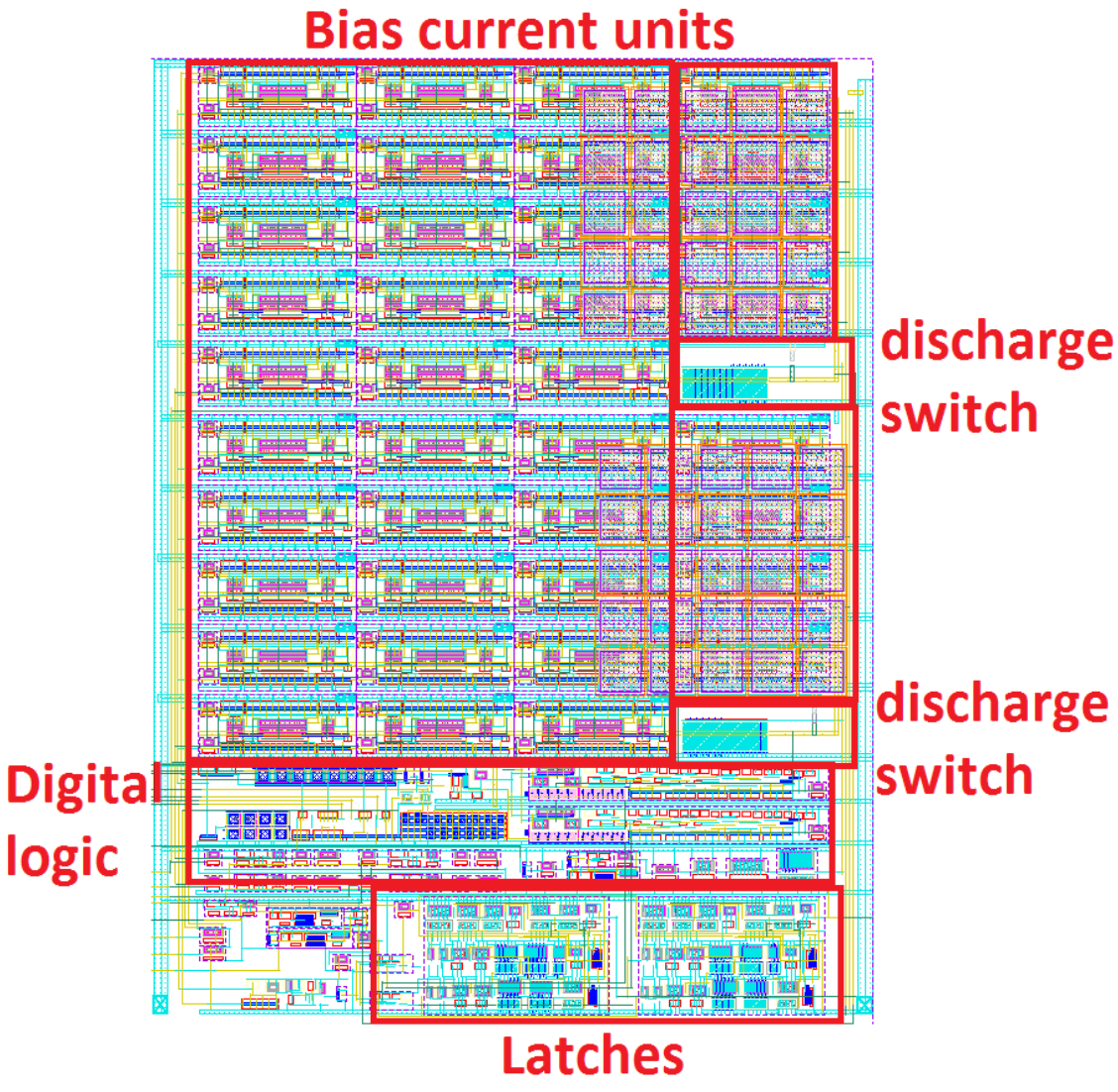

Figure 3.57. Layout design of pulse delay block.

3.13. Delay Lock Block

Delay lock block is used to fine tune the pulse delay timers. As a reminder, the pulse delay time has two digital inputs, one input coming from frequency counter and the other input is coming from delay lock block. The delay block produces a four bit digital timer code that fine tunes the pulse delay with an up/down counter. Additionally, this up/down counter also has a no code change mode. Figure 3.58 shows the simplified delay lock block diagram. The three main signals connected to the inputs of this block are; *delay*1, *delay*1_*plus*, and *output*2 low signal. Three logical comparisons are performed with these three signals; to check if the output 2 low signal is at the same time region of delay and *delay_plus* or in the low time region of these two signals. Figure 3.59 explains in detail the three comparison decisions. If delay1, *delay*1_*plus*, and *output*2 low signals are high it means that output2 load demand is higher than output1 and output1 pulse delay time must be decreased. If delay1 and *delay*1_*plus* are both low and output2 low comes to that time region it means that output2 load demand is lower than output1 and output1 pulse delay time can be increased to give some extra time to regulate its load better. The third time region occurs when output2 low signal coming from delay1 is low and *delay*1_*plus* is high, this means that both output1 and output2 pulse delay times are at equilibrium and output1 pulse delay time is ok and doesn't need to change the timer code. Note that the mentioned labels delay1, *delay*1_*plus* and *output*2_*low* are used for the delay lock block of the first output. Since the second output also has delay lock block dedicated to it, its labels will be similar as; *delay*2, *delay*2_*plus* and *output*1_*low*.

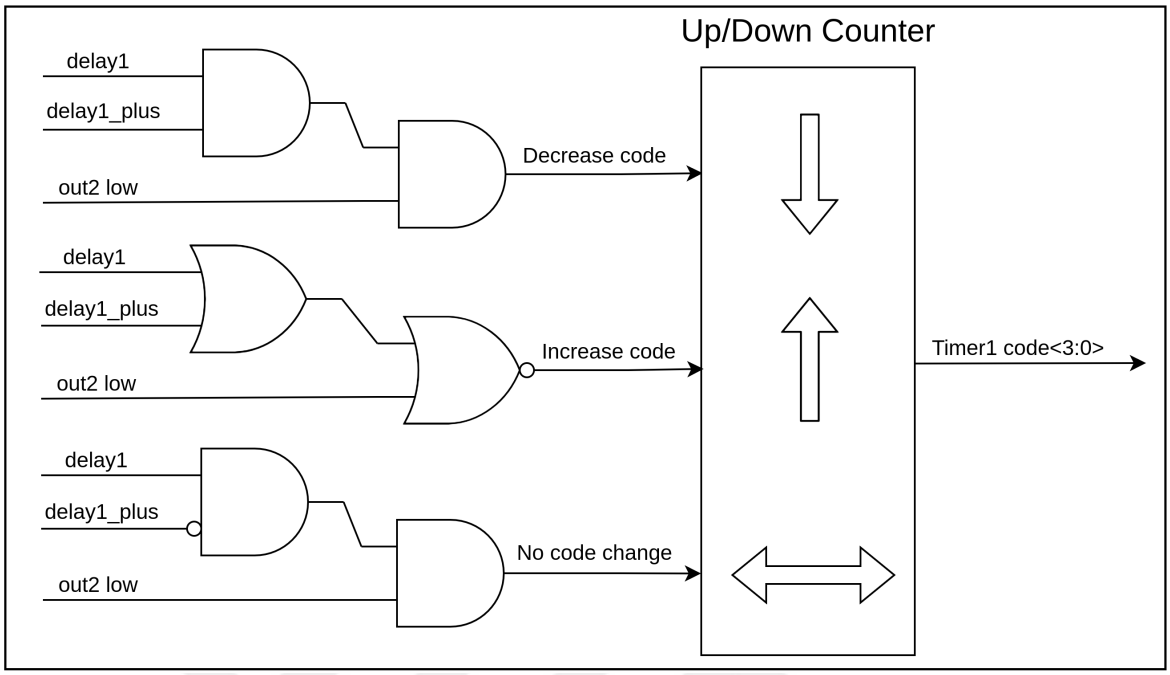

Figure 3.58. Delay lock block simplified diagram.

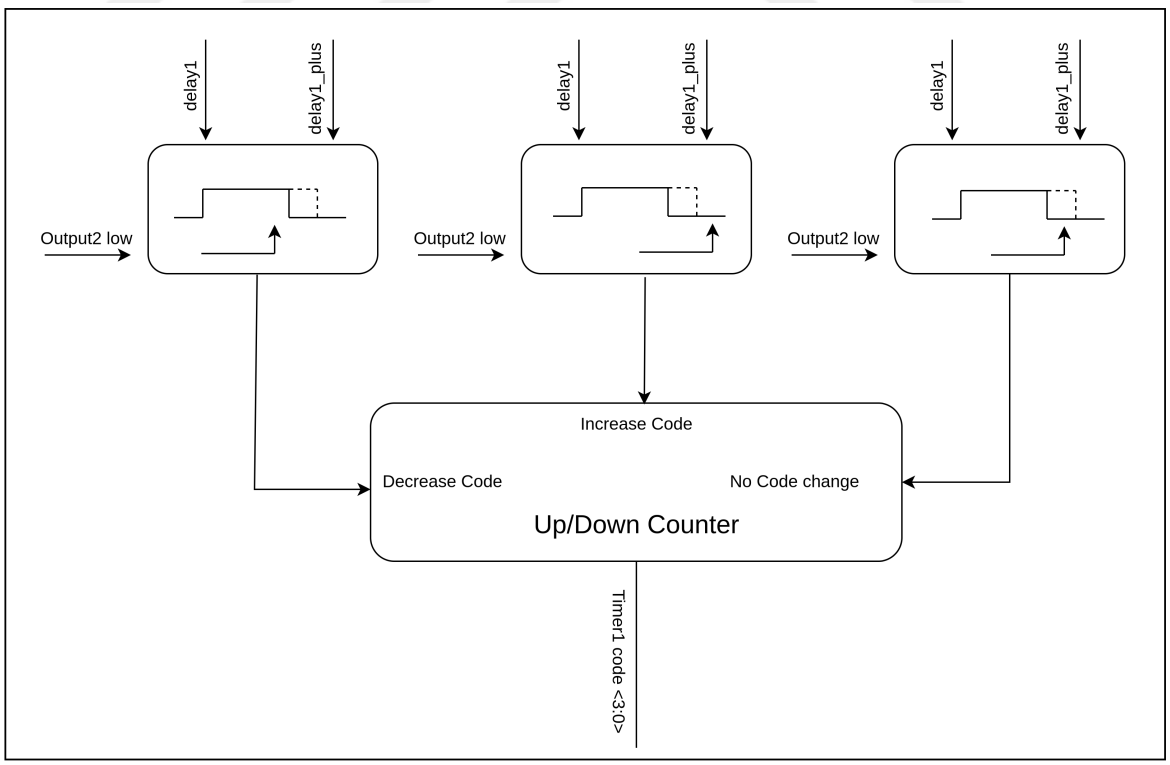

Figure 3.59. Delay lock block flow-chart.

The Up/Down counter is realized with D type latches since it has no clock for synchronization. Four D latches are needed for four bits and also some digital gates to process and initialize the up/down counter. Figure 3.60 shows the simplified diagram of the up/down counter block. Initially *delay*1 and *delay*1_*plus* signals are used with *output*2_*low* signal to produce *count_down* signal. When upper logical path is activated through its logic inputs, digital counter decreases code by one. When middle logical path is activated, digital counter increases code by one. Also to disable the counting *no_code_change* signal is used. *no_code_change* and *output*2_*low* signals are used to produce the trig signal which triggers all D latches to count up or down. Finally four bits of digital data is produced at every *output*2_*low* signal rise and D latches keep the data for the next event.

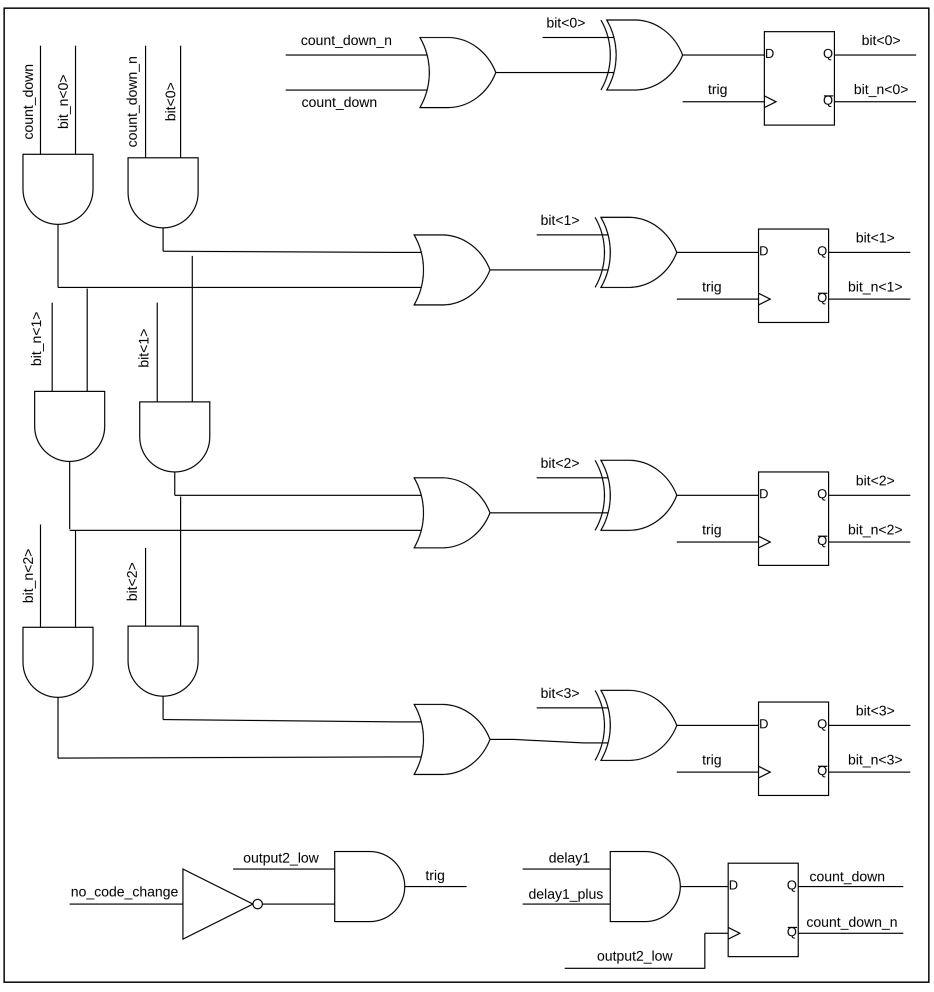

Figure 3.60. Up/Down counter simplified diagram.

Block level simulations have been run to check the functionality of the delay lock block. To change the direction of the counting at the test-bench level, two different output2 low signals have been used and logically enabled or disabled to mimic top level output2 low signal shifting with operation. Figure 3.61 shows the block level simulation result of delay lock block. timer1 code starts with a decimal code of 15 and output2 low signal is high when delay1 and *delay*1*_plus* signals are high, too. As designed, *count_down*1 signal goes high showing that it counts down. By each output2 low signal, timer1 code is decreased one by one and when timer1 code reaches 0, it stays at 0. Then output2 low signal is set high when both delay1 and *delay*1*_plus* are low which means the delay lock block should increase the timer1 code. Note that due to internal logic inside the delay lock block, *count_down*1 goes to zero which means it is a count up event. By every output2 low signal timer1 decimal code increases from 0 to 15. When it reaches to 15, it stays at that point.

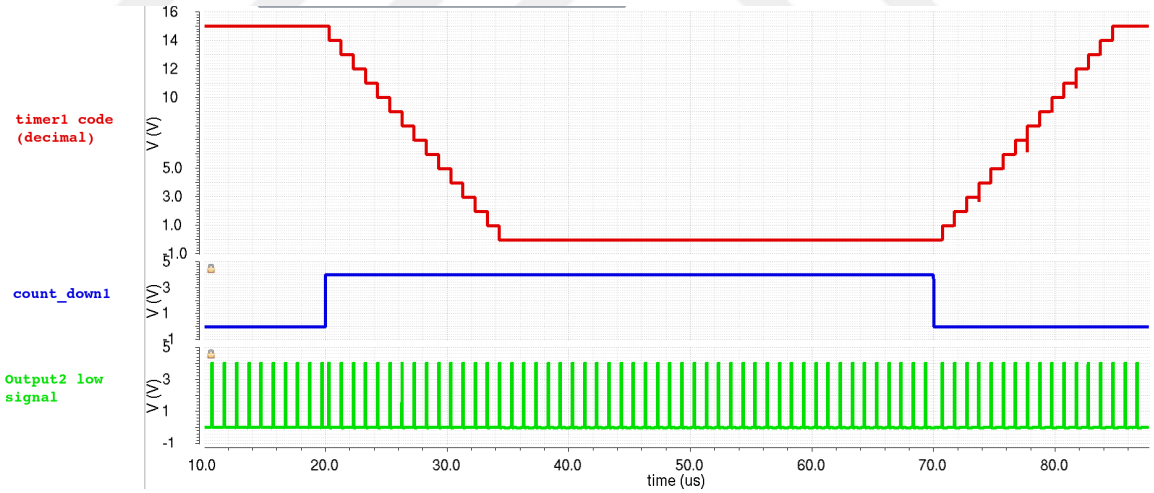

Figure 3.61. Delay lock block level simulation result.

3.13.1. Layout Design of Delay Lock Block

Figure 3.62 shows the layout of the delay lock block. The layout area is mostly dominated by the latches since each event change needs to be stored until the next event. Top and bottom sides are occupied by the latches and the core logic to process the signals is in the middle in the middle of the layout. The layout dimensions of the

block are 300μm to 510μm.

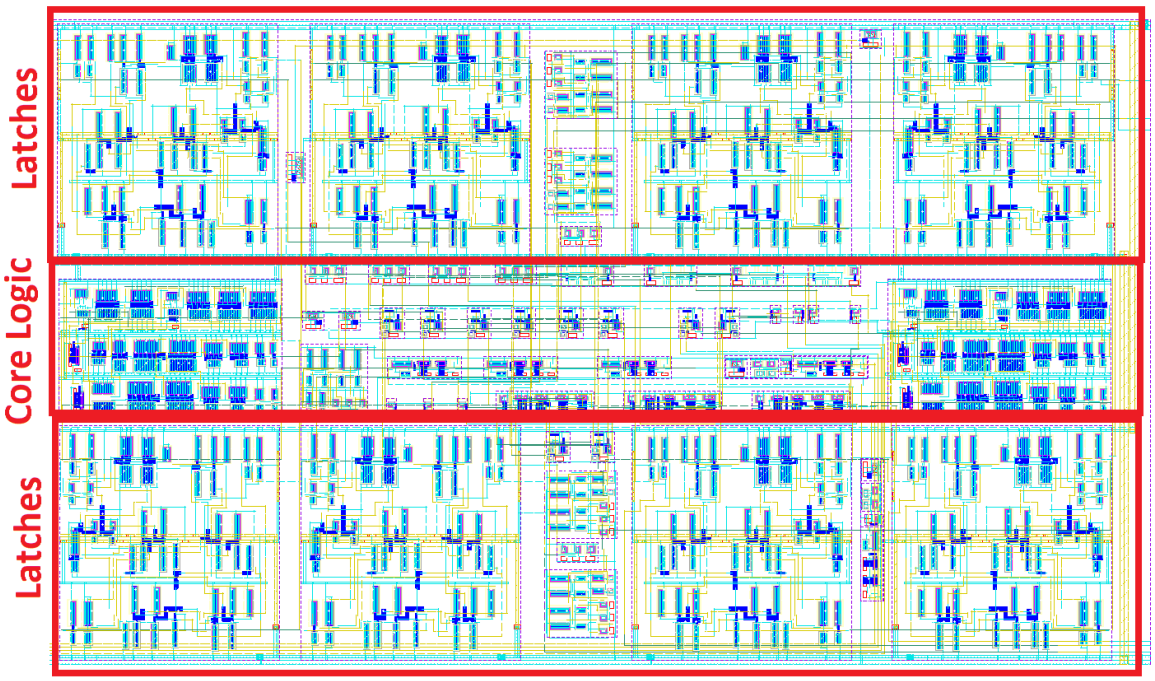

Figure 3.62. Layout design of delay lock block.

3.14. Load Balancing Controller and Functionality

The load balancing controller is the core of this architecture because all other block output signals are fed into this block, processed, and finally all four switch driver signals come out from this block. It is formed by the frequency counter, pulse delay, delay locked loop (DLL), and the load balancing core logic. The right side of Figure 2.2 shows the internal building blocks of the load balance controller and some needed input signals.

The operation can be described as follows; comparators monitor each output continuously and flag if the output voltage is lower than the allowed value; in that case, the controller block starts driving that output by controlling all four switches simultaneously. When the comparator of the other output flags a low voltage, the controller waits for the first output to finish; then, after some time depending on the control logic and the delay locked loop, the second output controller takes over the

control. This loop continues for every low signal by the controller trying to adjust each output to minimize the load drop. Note that for relatively heavy load conditions, the buck converter operates in the Continuous Conduction Mode (CCM). If the total load on both outputs is relatively low, the inductor current can go to zero and the converter operates in the Discontinuous Conduction Mode (DCM) and the active diode turns off the NMOS input switch in order not to discharge the output. Changing mode from CCM to DCM and vice versa is done automatically by the controller.

The controller can be divided into four main parts; frequency counter, pulse delay, delay locked loop (DLL), and the control core. The pulse delay block accepts a 4 bit code from the frequency counter as coarse control and an additional 4 bit code from the DLL as fine control. The main idea is that the ON time of both outputs is defined by the pulse delay unit time. Thus, adjusting the delay of one output with respect to the other adjusts the duty cycle of that output. As a result, the main controller of this buck converter tries to increase or decrease the duty cycle of that output to balance the load demand and regulate both outputs. To change and adjust the ON delay time of each output, the frequency counter and DLL core blocks increase or decrease the code of the pulse delay block. The frequency counter block counts the input switch PMOS on time and produces a 4 bit output data. When the load demand of that output is high, the controller inherently tries to increase the inductor switching frequency, whereby the frequency counter 4 bit code increases, and as a result, pulse delay time decreases. Inversely, when the load demand is low, the controller tries to decrease the inductor switching frequency, and the frequency counter 4 bit code decreases, and as a result pulse delay time also increases. The frequency counter produces 4 bits of data which is used as coarse data by the pulse delay timers. Also, the DLL block produces 4 bit data which is used as fine data for the pulse delay block. Consequently, the pulse delay block has 4 bit coarse and 4 bit fine as a total of 8 bits of control input data.

Changing the pulse delay time of each output with respect to the other also means changing the duty cycle of each output with respect to the other and a good load balancing is achieved whereby both outputs regulate the load harmoniously. The load balancing (duty cycle adjustment) idea is depicted in Figure 3.63, showing the

frequency counter and delay lock relation with total duty cycle and the duty cycle of each output.

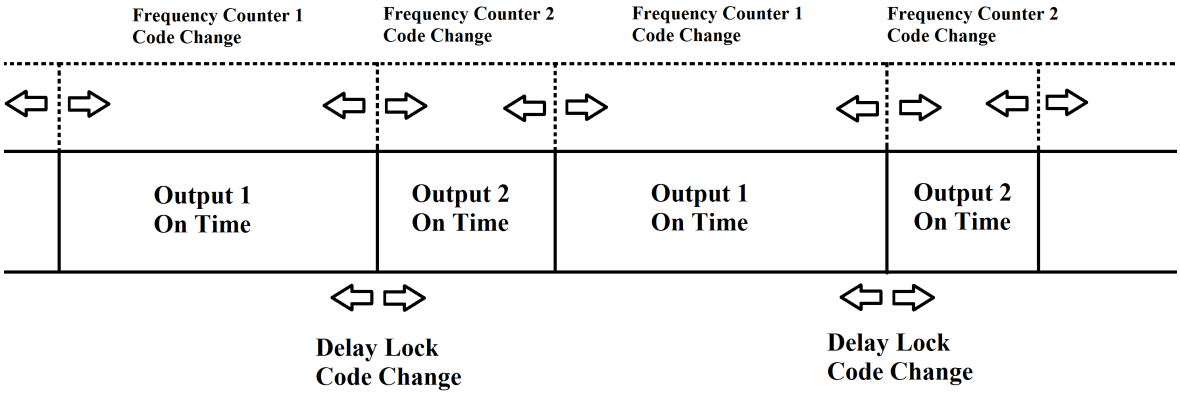

Figure 3.63. Frequency counter and delay lock code change and duty cycle relation.

Initially, the pulse delay unit value which defines the duty cycle of the corresponding output starts with 0000 coarse digital code and 1111 fine digital code for both outputs. Due to a sudden load demand, the buck converter tries to regulate both outputs and the inductor switching frequency increases. Coarse digital code changes from 0000 to 0001 and then increases bit by bit when needed. To fine tune the duty cycle of each output, the pulse delay unit is controlled by a delay locking mechanism. The main delay lock loop core algorithm which fine tunes the duty cycles of both outputs is depicted in Figure 3.64.

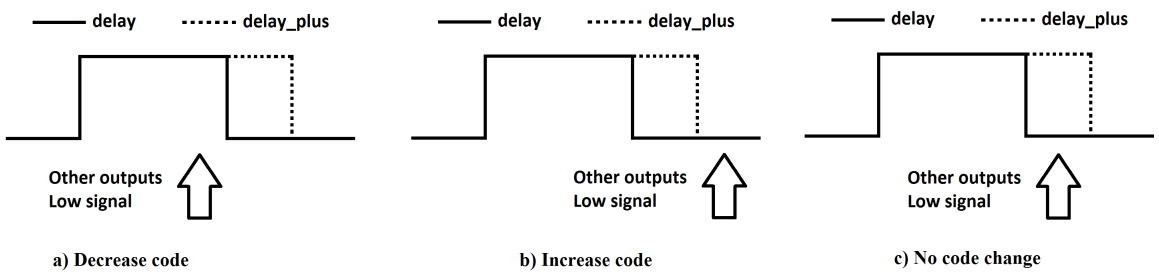

Figure 3.64. Delay lock fine tune algorithm.

A delay time is defined for both outputs by the delay unit, which also defines

the duty cycle of that output. Note that each delay unit also has a *delay_plus* time which will be explained later. Assuming that each output is at equilibrium initially and output 2 load demand is increased abruptly. Then, the output 2 low comparator is flagged showing the case depicted in Figure 3.64 (a). If the delay unit of output 1 is not finished and output 2 low comparator is flagged, then it means that delay unit 1 must decrease and delay unit 2 must increase. As a result, the duty cycle of output 1 will decrease and the duty cycle of output 2 will increase. For load decrease case, it is the opposite as shown in Figure 3.64 (b), then the delay unit code of that output must increase and the delay unit time will increase, and as a result, duty cycle of that output will increase. As shown in Figure 3.64 there is a *delay_plus* time in addition to delay time and this is used to define a "no code change zone" which means if low signal comes to this portion of the delay timer there will be no code change. This no code change zone is used to prevent code oscillation. If there is no dead time zone, for each cycle, the code will keep increasing and decreasing creating an unstable operation. Thus, to have a stable operation for both outputs, there must be a no code change zone. This is done by adding a *delay_plus* signal for both outputs additionally. This *delay_plus* time is also controlled by 2 control bits.

It has been mentioned that delay time is adjusted in a coarse manner by the frequency counter but the overall operation of both outputs has to be discussed. If the load demand increases for one output or for both outputs, the frequency counter code is increased and the delay timer is decreased which means increasing the switching frequency of that output to regulate it with a faster inductor switching.

Due to not having a clock signal and regulating two outputs at the same time, input PMOS and NMOS switches could be switching at a very high frequency. To prevent PMOS and NMOS input switches from operating at a very high frequency, minimum constant on times are defined for both PMOS and NMOS input switches. This way, converter stability is increased, and a decrease in efficiency due to high switching losses is prevented.

3.14.1. Top Level Simulation Results with Load Balancer Block

After finalizing the design of the load balancer block, top level simulations have been run to check the functionality of the controller block. After charging of the output capacitors with a start-up sequence, load currents are applied to both outputs. Initially, the delay lock timers for both outputs start from a decimal code of 15 which is the highest code for 4 bit digital. Then, the separate delay lock block of each outputs checks whether delay and *delay_plus* signals coincide with the low signal of other output voltage comparators. As a result, delay locking for each output is regulated by the low signal of the other output (load demand) resulting in a situation where two outputs control one another. Figure 3.65 shows the top level simulation result of the code change of the delay lock block. When output1 switch enable signal goes high, delay1 and *delay*1*_plus* timers are started, and timer1 code is decimal 12. Note that, timer codes are converted to decimal by the help of a Verilog-A code and decimal voltage values are shown for the sake of simplicity. Output1 comparator flags the low signal at the time region of both delay1 and *delay*1*_plus* are high. With the rising edge of output2 low comparator signal, timer1 code is decreased by one from 12 to 11. It means that output1 timers should decrease to reduce the duty cycle of the output1 compared to output2.

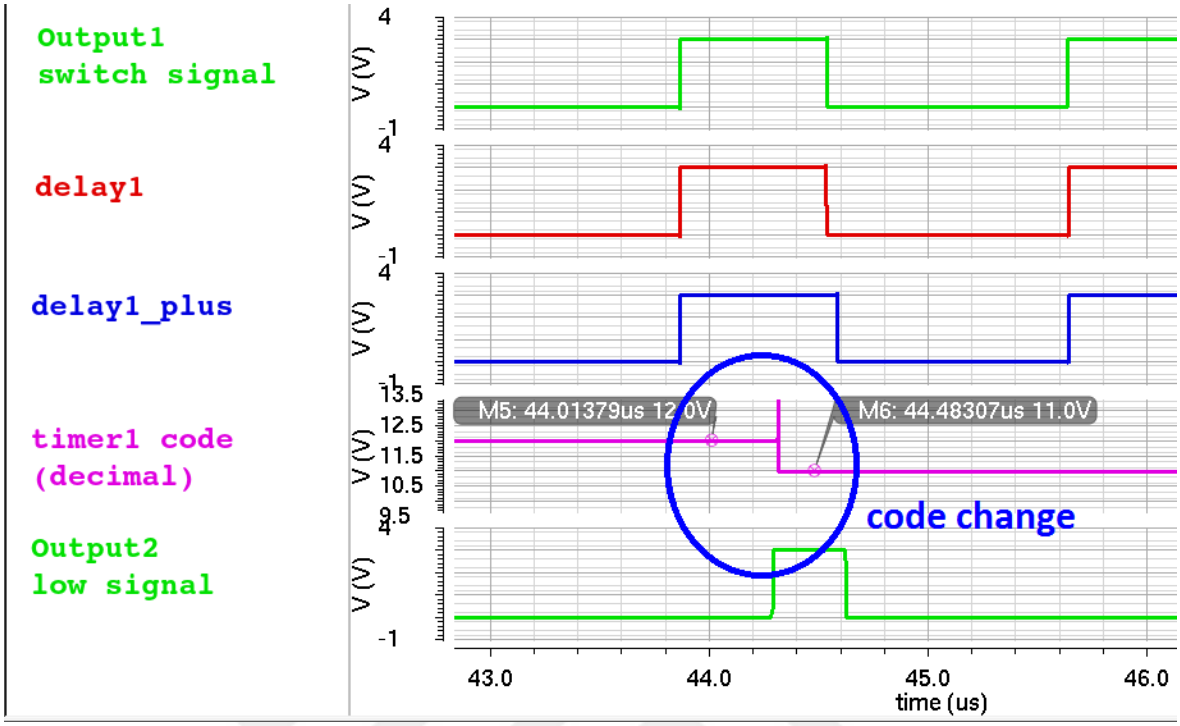

Figure 3.65. Top level simulation result showing delay lock block code change.

Figure 3.66 shows the timer code decimal values of both outputs voltages and the output voltages themselves. The timers for each output start with a decimal code of 15 and decrease. They may increase later due to the timer code change of the other output and finally both timers and output voltage settle to a stable point. For this simulation plot, both outputs have been set to the same value as 0.7V and also have the same load currents to observe the settling behavior of both output voltages related to timer codes. Another simulation has been run to check the load balancer functionality for two different output voltage settings also with two different load currents. Figure 3.67 shows the simulation result of two different output voltage settings with also two different load currents. Each output timer starts with a decimal code of 15 and then the code changes one by one. Due to changing of both output timers changing at the same time in the middle of the simulation time, output code increases then decreases again and after some time both output timers settles to their final values.

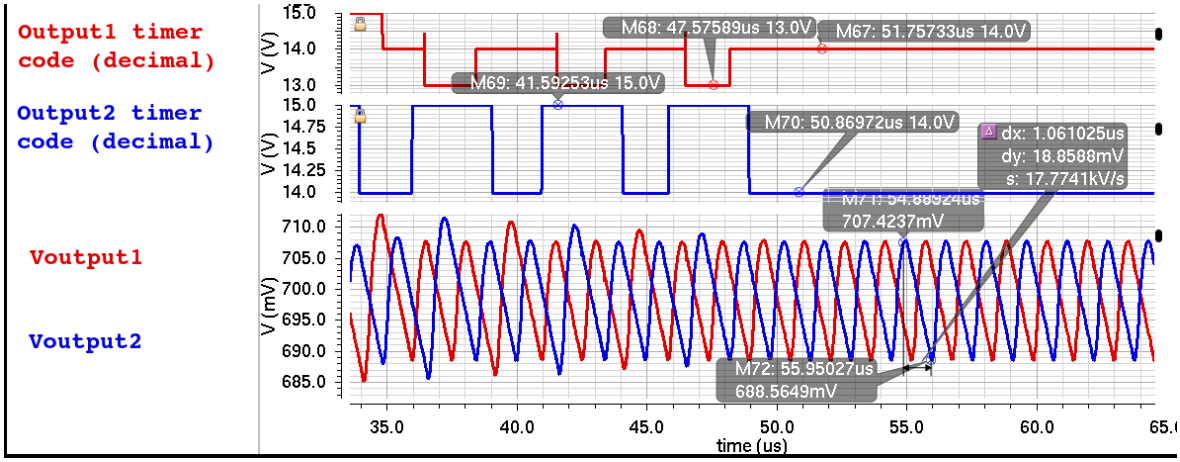

Figure 3.66. Top level simulation result showing both outputs timer codes and output voltages.

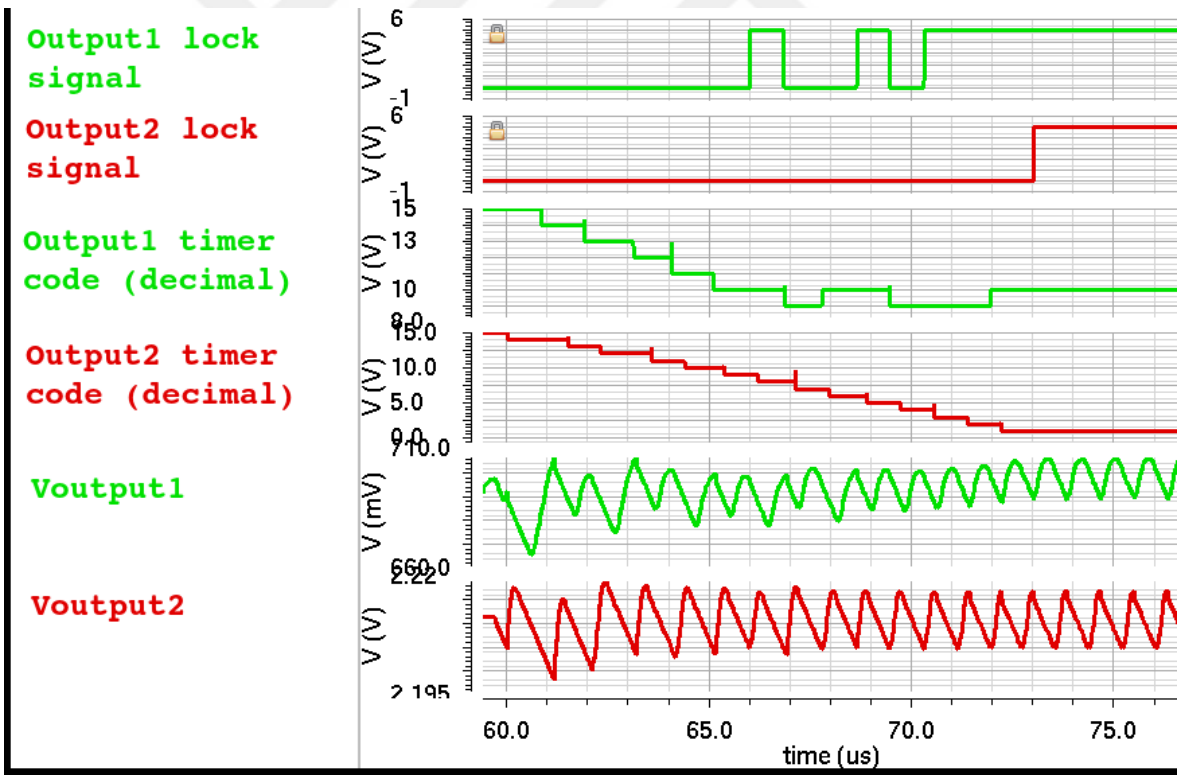

Figure 3.67. Top level simulation result showing both outputs timer codes, output voltages and lock signals.

3.14.2. Layout Design of the Load Balancing Controller

Figure 3.68 shows the layout design of the load balance controller block. At the left side there are two pulse delay internal blocks for each output. Delay lock block of output 1 resides at the top center of the layout and delay lock block of output 2 resides at the bottom center of the layout. At the right side are two frequency counters, one for each output. Finally, the core control logic which processes all the signals and drives the four switches is located at the center of the layout. The layout dimensions of the block are 1350μm to 920μm.

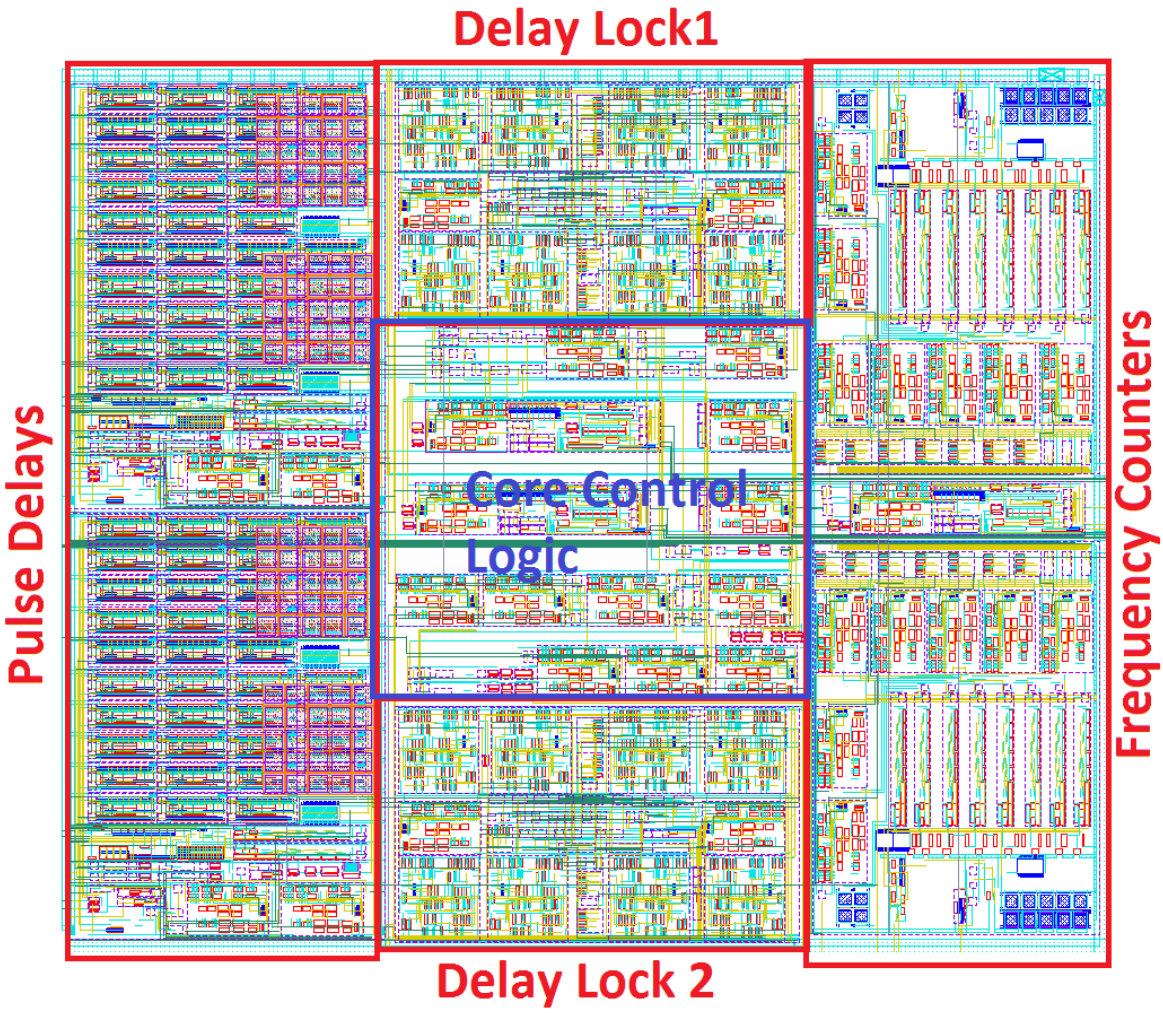

Figure 3.68. Layout of the load balance controller.

3.15. Top Level Layout

0.18 μm CMOS technology is used in the design, and every block is designed and verified individually before combining to form the top level and run the post layout simulations. The final design area is 3mm X 3mm. Figure 3.69 shows the final top level of the design with all blocks. All internal blocks can be listed as; Input up/down switches, 2 output switches, charge pump, bias, bottom comparator, current limit, active diode, output voltage comparators, DACs and main controller blocks.

Four big switch device layout has been designed such that all metal layer vias are been used extensively to reduce metal resistance. Also, increased number of vias help to reduce the risk of electromigration.

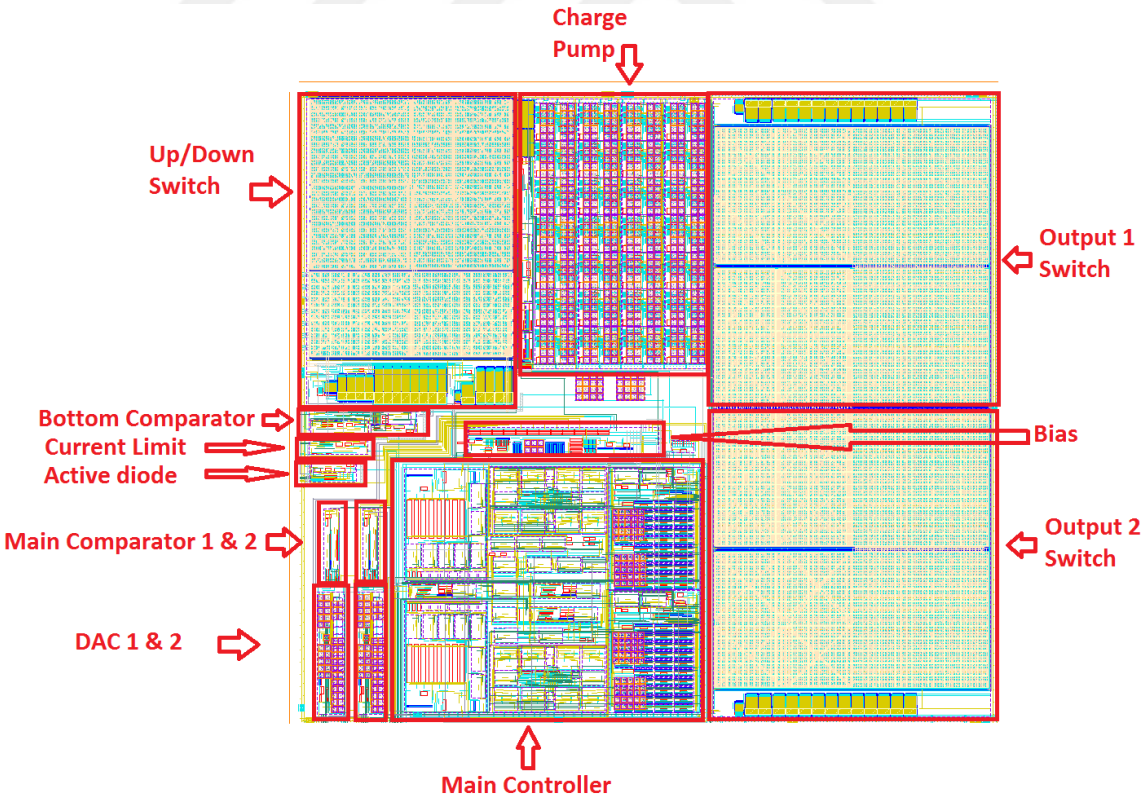

Figure 3.69. Top level layout showing all internal blocks.

4. TOP LEVEL SIMULATION RESULTS

An initial simulation is performed to observe the buck converter power-up and start-up behavior. In this simulation, the voltages on the output capacitors start from 0V and then each output settles to its defined DAC voltage value. To test the buck converter for load transient performance, the load at each output is changed independently and the outputs are observed. Then, to test for line transient performance, the supply voltage is changed to observe both outputs. Note that this buck converter has a 220nH inductor, 50μF output capacitors for each output and 4 internal switches. Simulations are performed with post layout R and C extracted parasitic. Each output can be changed separately from 0.9V to 2.5V with 6 bit DACs. Also, input supply can be between 3V and 5V to support both outputs.

4.1. Power-up Simulation Results

Integrated Circuits need a power-up sequence to properly load up to a known condition to be ready for the operation and this is called a power-up sequence. This sequence defines the ramp-up order of the building blocks with supply voltage. Current biases and some reference voltages which are used by the other building blocks must be ready before the relevant block starts its operation.

The power-up for the designed buck converter starts with current bias block initialization. Other building blocks such as DAC and charge pump also depend on the bias current. When the bias current increases during power-up, the DAC and charge pump blocks are also initialized. When the power supply is changed from 0V to 4V, $bias_ok$ goes high after some time depending on the internal settling. Then, the charge pump block initializes due to presence of supply and bias current. Charge pump starts to charge its bank capacitor with small pump capacitors. After some time cp_ok signal goes high when the charge pump voltage reaches its threshold voltage. Then, the DAC block settling is finished by DAC_ok signal. Finally, all_ref_ok signal goes high, signaling the controller that the power-up sequence is finalized. Figure 4.1 shows

the power-up sequence simulation result.

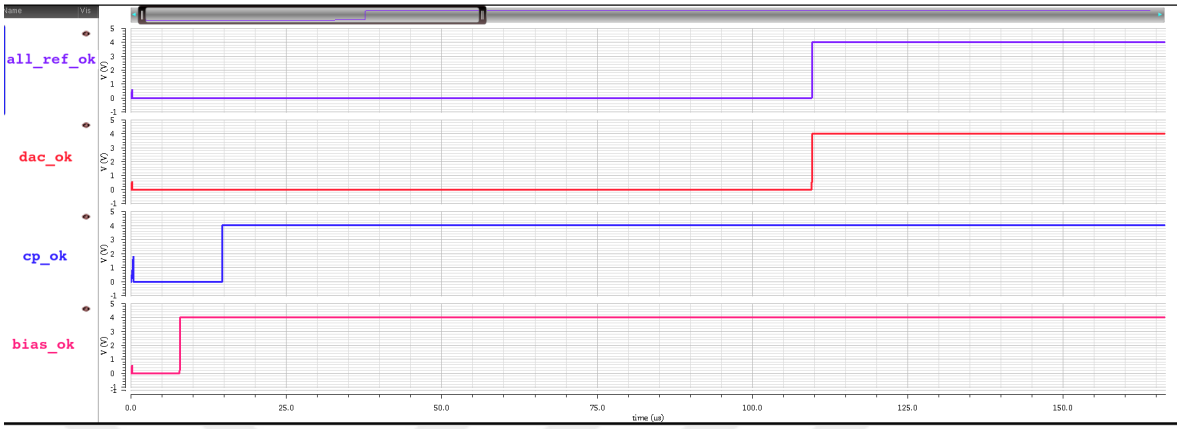

Figure 4.1. Power-up sequence of the buck converter.

4.2. Start-up Simulation Results

Initially all building blocks start from 0V voltage or 0A current. In this simulation, each output initially starts from 0V, and then the first output capacitor starts to charge to its DAC voltage level. Then, the second output capacitor starts to charge to its DAC voltage level. Inside the controller, the start-up section is separated from the main control logic. When start up is finalized, start-up flag signal goes high and the main regulation control loop takes over the control.

Figure 4.2 depicts the simplified start-up section inside the main controller and Figure 4.3 shows the simulation result with the necessary internal signals. Initially, all_ref_ok signal goes high after the power up and this signal turns on the input PMOS switch by enabling $startup_sw_up$ and the inductor charges from the input supply source. Then, when inductor current hits current limit threshold, $startup_sw_up$ goes low and $startup_sw_down$ goes high and enables the input NMOS switch to discharge inductor current to the output capacitor. When the inductor current reaches 0A, the active diode flag signal is generated and $startup_sw_up$ signal goes high to charge the inductor current from the supply. This cycle repeats itself until the high flag signal of the first output is generated producing $output1_ok$ signal. Then, the start-up event repeats in a similar manner for output 2. After output 2 output voltage comparator

flags high signal and *output2_ok* signal is generated, *startup_done* signal goes high which finalizes the start-up event and controller mode changes from startup mode to normal operation mode.

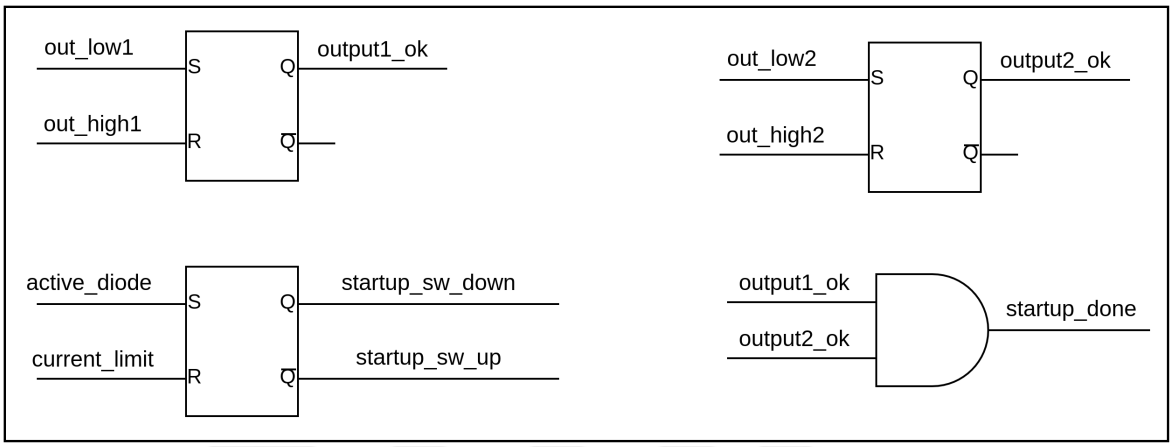

Figure 4.2. Simplified Start-up section inside the main controller.

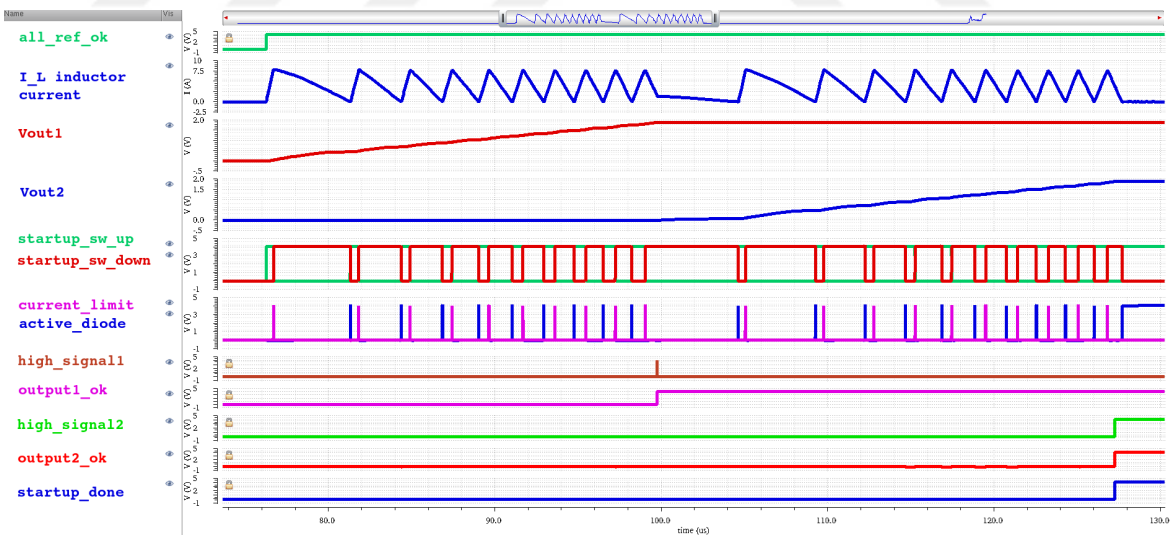

Figure 4.3. Start-up simulation showing internal signals.

4.3. Quiescent Current Simulation Results

To reduce the quiescent current of the whole buck converter when there is no load, the always on block activates or deactivates some blocks to save power. These power saved blocks can be listed as; bias block, charge pump block, active diode block,

current limit block, bottom current comparator block, and finally load balancer block. The power of these blocks are either turned off or reduced at standby mode. At normal operation their quiescent currents are reverted back to their default values. Figure 4.4 shows the quiescent currents of some blocks when the *always_on* signal goes from logic "0" to logic "1". Note that not all of the sub block quiescent currents are shown in the figure to avoid congestion. The quiescent currents of the load balancer block, active diode comparator, one of the DAC blocks, one of the output voltage comparator blocks, and the bias blocks are shown in the Figure 4.4. Two vertical markers are added left. One shows the quiescent current of each block when the *always_on* block is low (which means these blocks are at standby mode) and right vertical marker shows when *always_on* signal is high and the buck converter is active. The current for each block is listed in Table 4.1 both for standby mode when *always_on* signal is low and normal operation when *always_on* is high. The quiescent current of some blocks is increased due to activity at some portion of the time. Thus, these current values listed at table are calculated by averaging in a 100μs time window to increase accuracy.

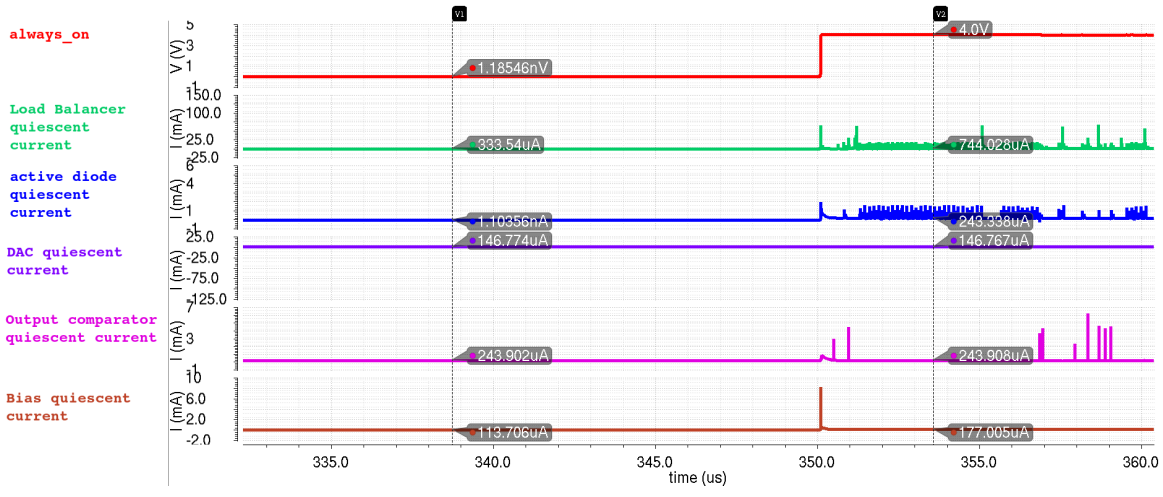

Figure 4.4. Quiescent current of some block with always on block activation.

Table 4.1. Quiescent Current simulation results for standby and normal operation.

Block name	**Normal operation current (μA)**	**Standby mode current (μA)**
Bias block	177	114
DAC1 block	147	147
DAC2 block	147	147
output voltage comparator1	244	244
output voltage comparator2	244	244
Charge Pump	49360	33
Active diode block	208	0
Current Limit block	317	0
Always on block	2	2
Bottom Current comparator	525	0
Load Balancer block	1852	334
Total Current	53223	1265

4.4. Load Transient Response Simulation Results

To test the single inductor double output (SIDO) hysteretic converter load transient response, a load transient is applied on the outputs. First, the load is changed for output 1, then the load is changed for output 2. Note that, due to start-up and also DLL loop to settle initially, the load transient pulse is repeated and the actual results will be after the initial settling of the DLL blocks. For simulation, output 1 is set to 1.45V and output 2 is set to 1.85V. The applied load changes from 1A to 2A for both loads. Figure 4.5 shows the load transient response for all four load current combinations for both outputs. The top (blue) waveform is the inductor current, the one below (red) waveform is the first output voltage and the second below (green) waveform is second output voltage. The two bottom (blue and pink) wave forms drawn on the same axis are output 1 and output 2 drawn load currents.

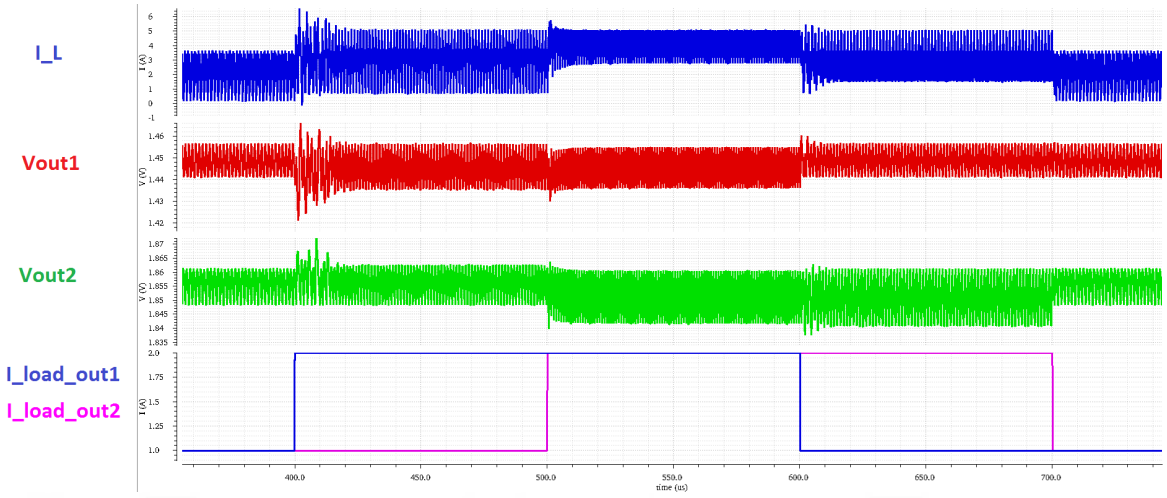

Figure 4.5. Load transient response showing both outputs with all 4 current load combinations.

For the first load transient event, the current transient section is zoomed to show the load transient responses clearly. Figure 4.6 zoomed simulation plot shows both outputs have 1A load current initially and then, the load current of output 1 rises from 1A to 2A with a rise time of 10ns. Output2 has 1A load current for this zoomed plot. The load transient response of output 1 is 19.8mV and the load transient response of output 2 is 6.3mV. The load transient response of output 2 is also the transient cross regulation value for this transient event.

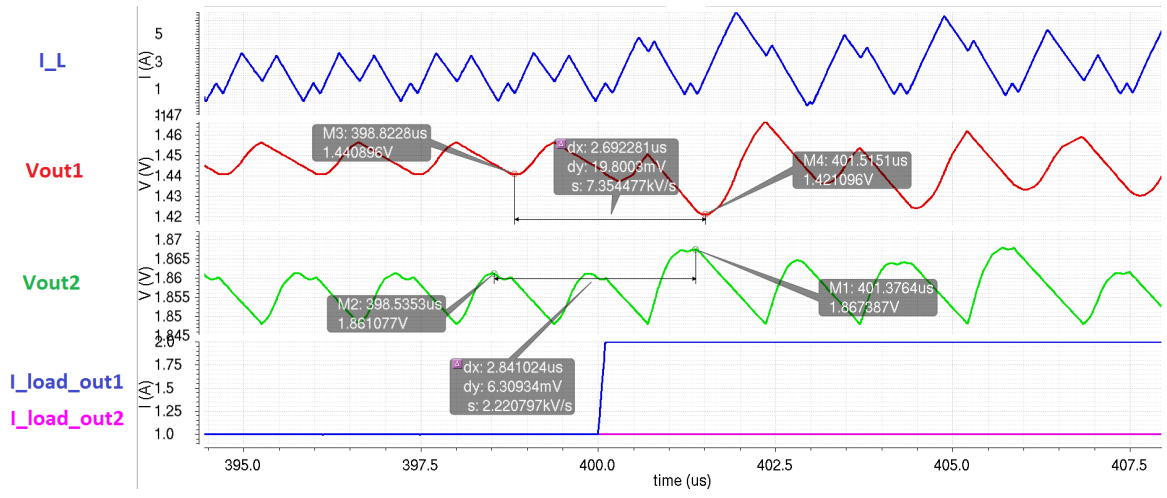

Figure 4.6. Load transient response results of output 1 going from 1A to 2A.

Figure 4.7 shows the case where output 1 has a load of 2A and output 2 load is changing from 1A to 2A. The load transient response of output 1 is 5.5mV and the load transient response of output 2 is 8.7mV. 5.5mV load transient response of output 1 is also transient cross regulation value for this load transient event.

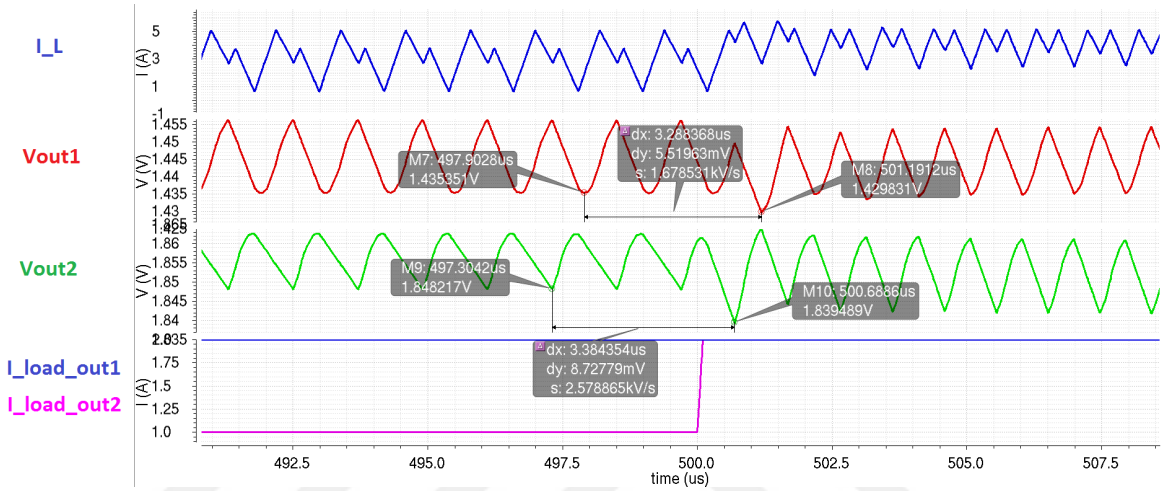

Figure 4.7. Load transient results of output 2 going from 1A to 2A.

Figure 4.8 waveform shows the case where both outputs initially have 2A load and then output 1 load current is changed from 2A to 1A. Load transient response of output 1 is 5.1mV and load transient response of output 2 is 2.9mV. Load transient response of output 2 is also transient cross regulation value for this load transient event.

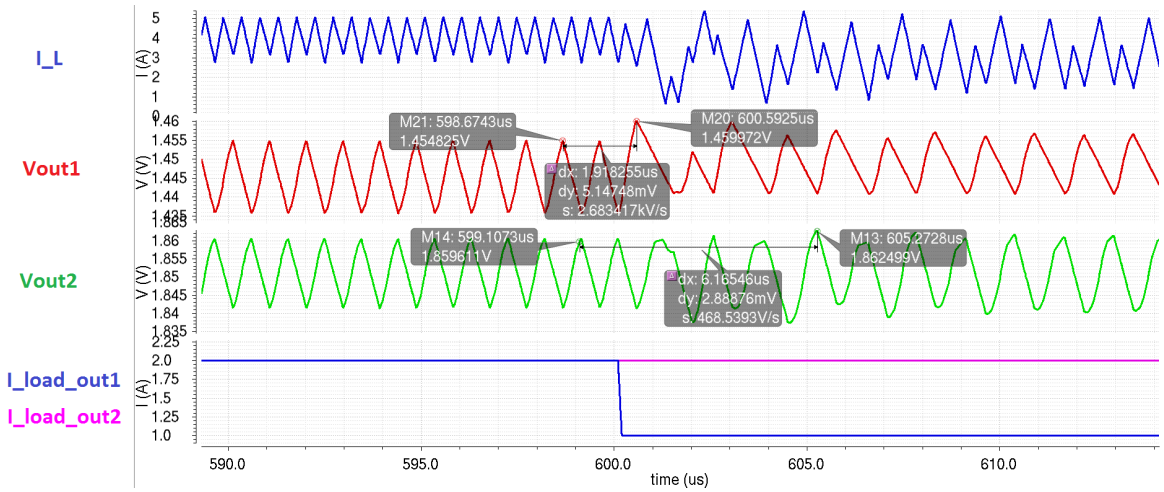

Figure 4.8. Load transient results of output 1 going from 2A to 1A.

Figure 4.9 shows the final load transient response where output 2 load current changes from 2A to 1A. Output1 has 1A load current for this zoomed plot. Load transient response of output 1 is 0.6mV and load transient response of output 2 is 7.4mV. Load transient response of output 1 is also transient cross regulation value for this load transient event.

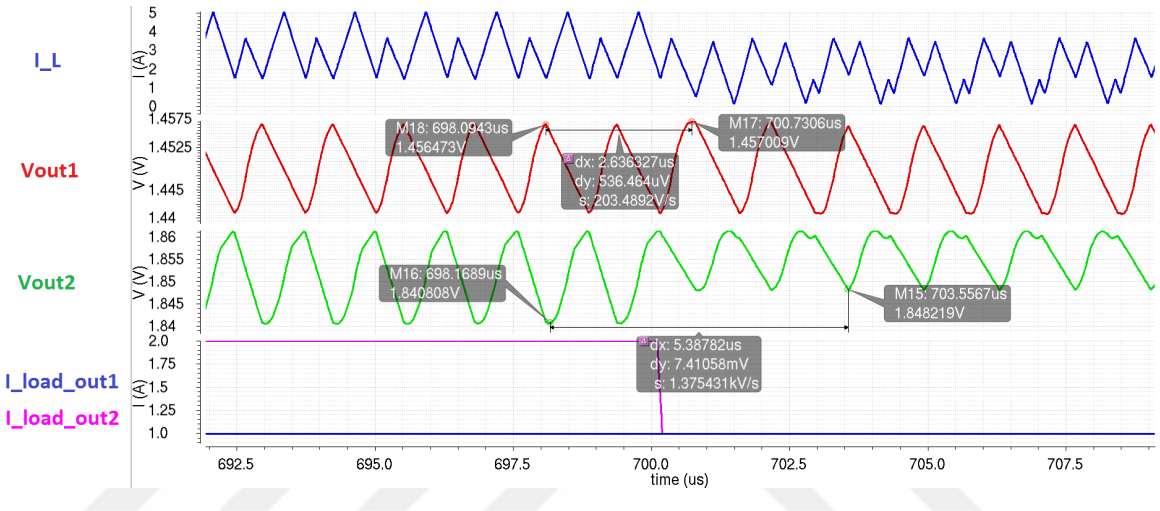

Figure 4.9. Load transient results of output 2 going from 2A to 1A.

All load transient response simulation results are tabulated in Table 4.2. Table shows that load transient response values are modest compared to vast load current change from 1A to 2A. The controller block immediately responds to minimize the load transient voltage drop by supplying current to that output in the best way possible.

Table 4.2. Load transient response simulation results.

Output 1 Load (A)	**Output 2 Load (A)**	**Output 1 Load Transient (mV)**	**Output 2 Load Transient (mV)**
1 ⇒ 2	1	19.8	6.3
2	1 ⇒ 2	5.5	5.5
2 ⇒ 1	2	5.1	2.9
1	2 ⇒ 1	0.6	7.4

4.5. Switching Frequency change with Load and Output Voltage

Hysteretic buck converters do not have a clock for synchronization of the internal blocks, and the inductor switching frequency is mainly related to the load current and also supply voltage and output voltage. Thus, the hysteretic buck converter needs a frequency spectrum control to have a better EMI affecting both the supply and the output. Due to load balancing achieved by this architecture, switching frequency does not change linearly with load current. Figure 4.10 shows the switching frequency (MHz) for different load currents and output voltage settings. The figure depicts the switching frequency being controlled in a narrow band with changing of the load current.

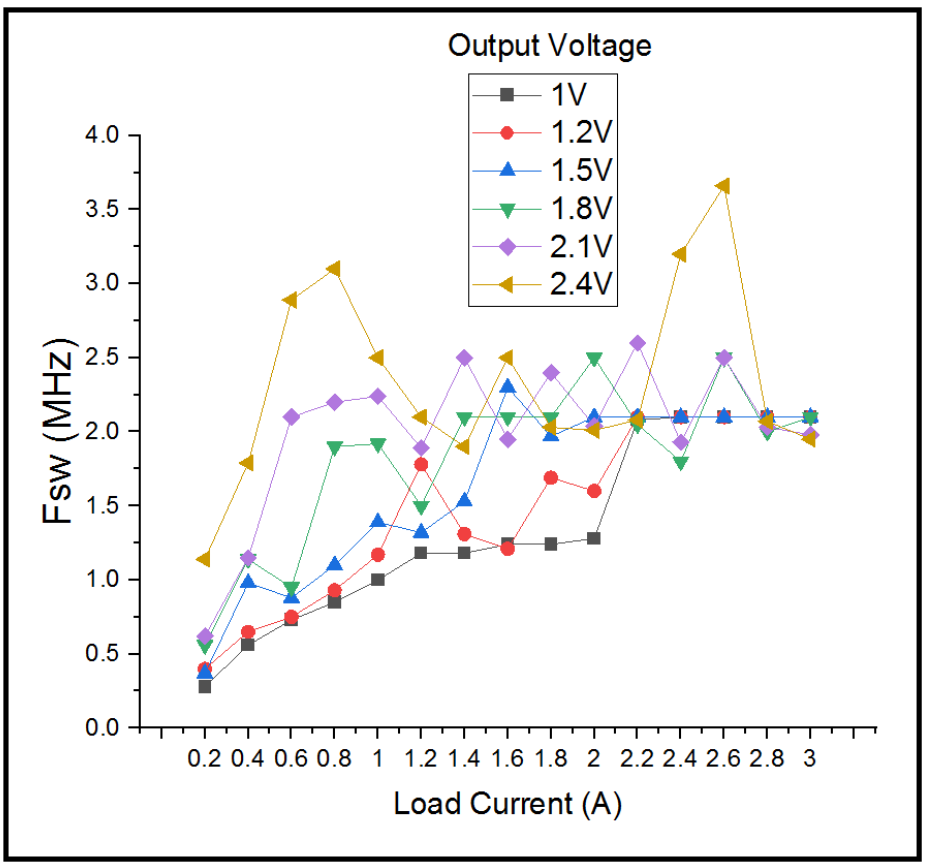

Figure 4.10. Switching frequency relation for different load currents and output settings.

4.6. Line Transient Response Simulation Results

To see the line transient response performance of the buck converter, 2A load is drawn from both outputs, and then the supply is changed from 4V to 5V and then to 4V again with rise and fall times of 200μs. Figure 4.11 is the result of this line transient response simulation. The line transient response is 5.8mV for output 1 and 8.6mV for output 2. It shows that even a large supply voltage change of 1V affects the output voltage slightly.

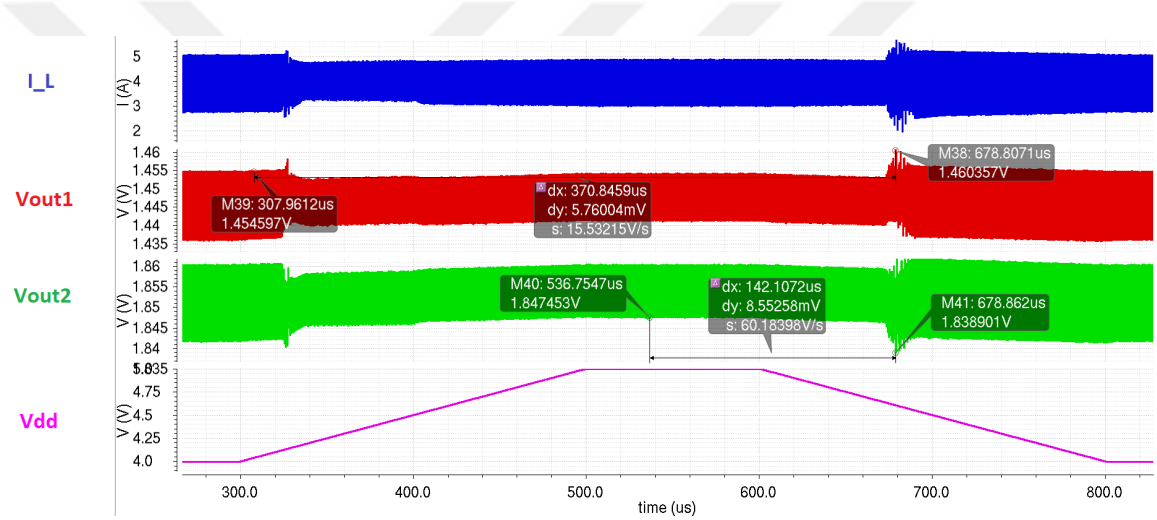

Figure 4.11. Line transient response simulation result.

4.7. Efficiency Simulation Results

Simulations have been run for different load currents and different output voltage settings for efficiency calculation. Initially, the converter is started with zero current. After some settling time for both outputs, input and output power values are calculated for a 200μs time window. Simulated load current values are incremented from 0.2A to 3A with 0.2A increments. The simulated output voltages are 1V, 1.2V, 1.5V, 1.8V, 2.1V, and 2.4V. The input power supply is 4V for all these simulations for the sake of comparison; however, power supply value could be between 3V and 5V. The efficiency results are from R and C parasitic extracted post layout simulations. The minimum efficiency is 78.8 % and the maximum efficiency is 93.7 %. Figure 4.12 shows the simulated efficiency results. Note that this buck converter is designed to have maximum

2.5A load current for each output; however, simulations have been performed for 3A maximum output current as well, showing proper behavior.

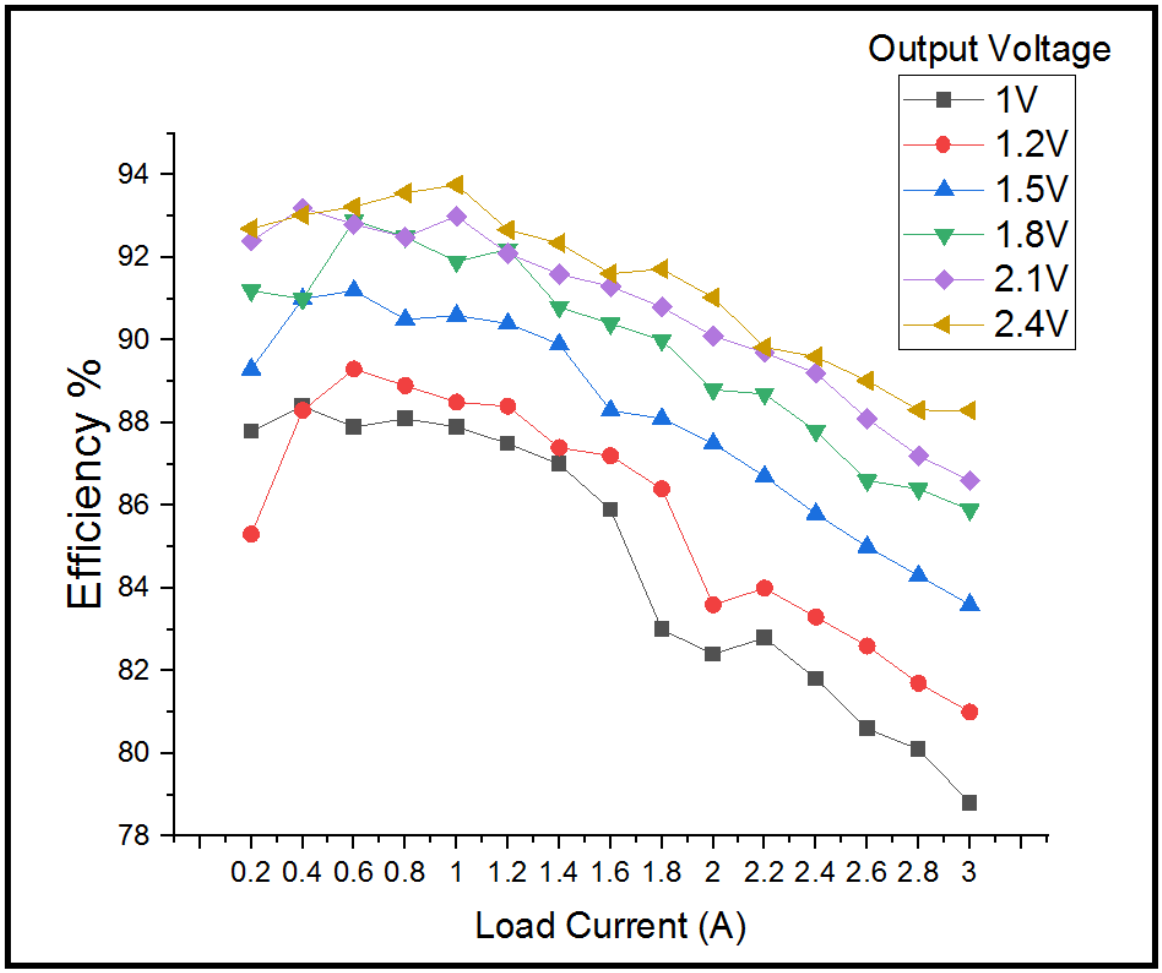

Figure 4.12. Efficiency simulation results.

4.8. Cross Regulation Simulation Results

Using a single inductor to regulate two outputs is a difficult task from regulation and isolation points of view. Each output must be isolated as much as possible from each other; otherwise, cross regulation occurs and the voltage and/or load conditions of one output could affect the other output, and both outputs could even run out of regulation. Thus, cross regulation is a very important figure of merit as a design goal for SIDO architectures. To measure the cross regulation for two outputs, 4 different load transients are applied and both outputs are observed. Figure 4.13 shows the case

when both outputs have 1A load current initially and then output 1 load current is increased to 2A. For this load transient case, output 1 has 2.2mV of static voltage change and output 2 has 0.3mV of static voltage change. Since output 1 load current is changing, static change of output 2, which is 0.3mV, is the static cross regulation value. Note that transient cross regulation results can be read from load transient results.

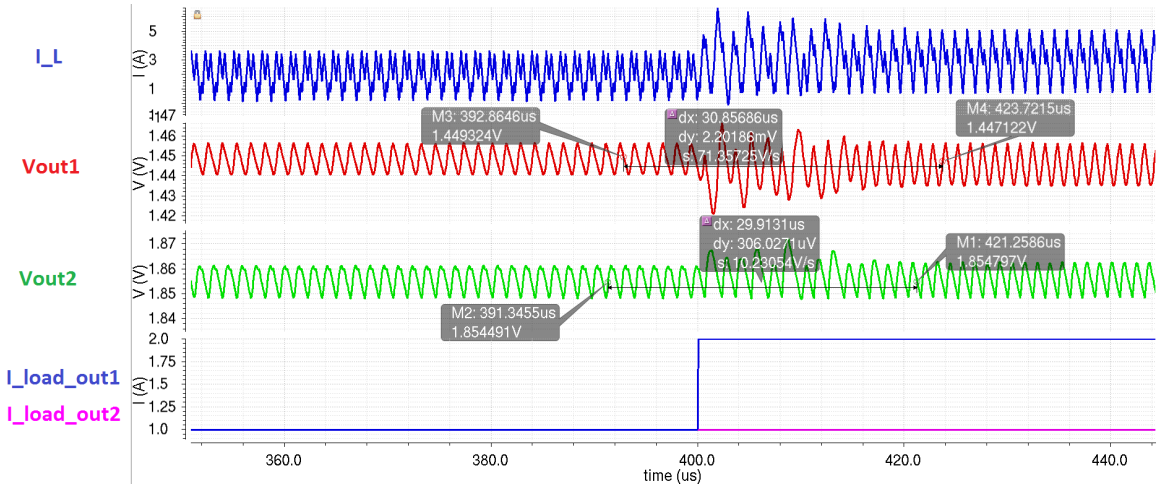

Figure 4.13. Cross regulation results for output 1 having load transient from 1A to 2A.

Figure 4.14 shows that output 1 has 2A load current and output 2 has a load transient from 1A to 2A. Output 1 has DC change of 0.5mV and output 2 has 4.1mV DC change. Thus, static cross regulation is 0.5mV for this transient event.

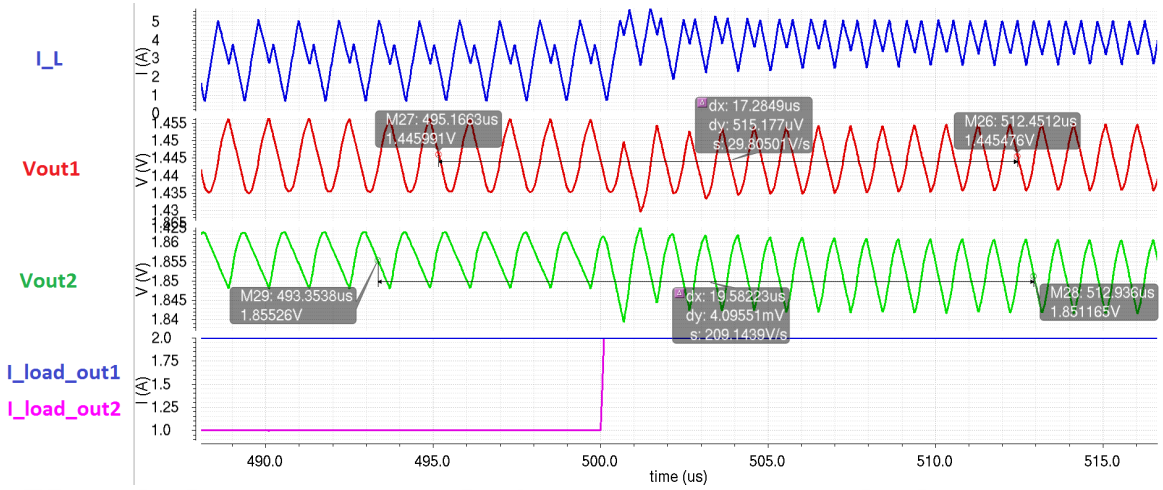

Figure 4.14. Cross regulation results for output 2 having load transient from 1A to 2A.

Figure 4.15 shows both outputs having 2A load current, then the load current of the first output is changed from 2A to 1A. Output 1 has 3.7mV DC change and output 2 has 0.4mV DC change. Static cross regulation for this transient event is 0.4mV.

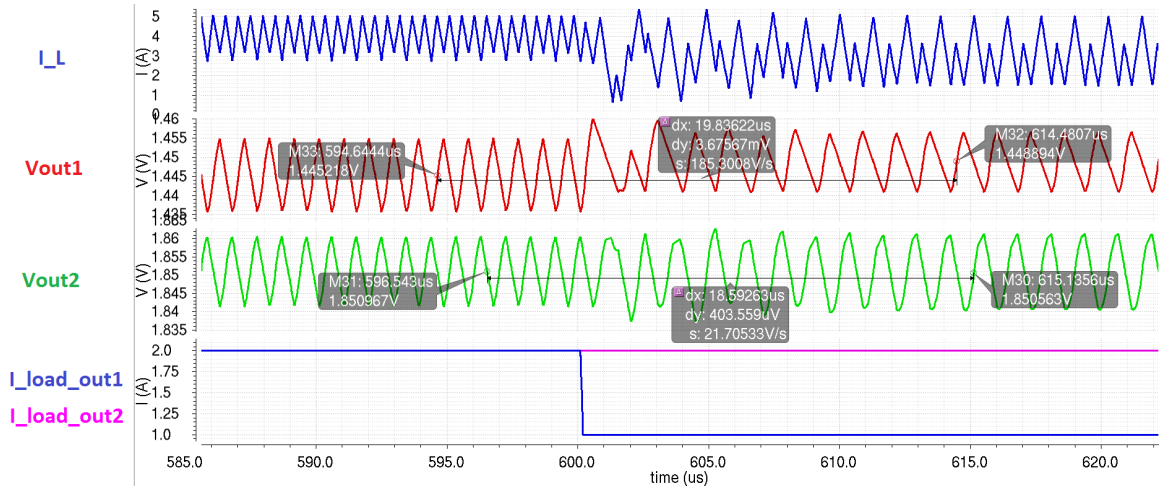

Figure 4.15. Cross regulation results for output 1 having load transient from 2A to 1A.

Figure 4.16 shows the last cross regulation simulation plot where output 2 has a load current change from 2A to 1A. Output 1 has 0.9mV DC change and output 2 has 3.5mV DC change. Static cross regulation for this transient event is 0.9mV.

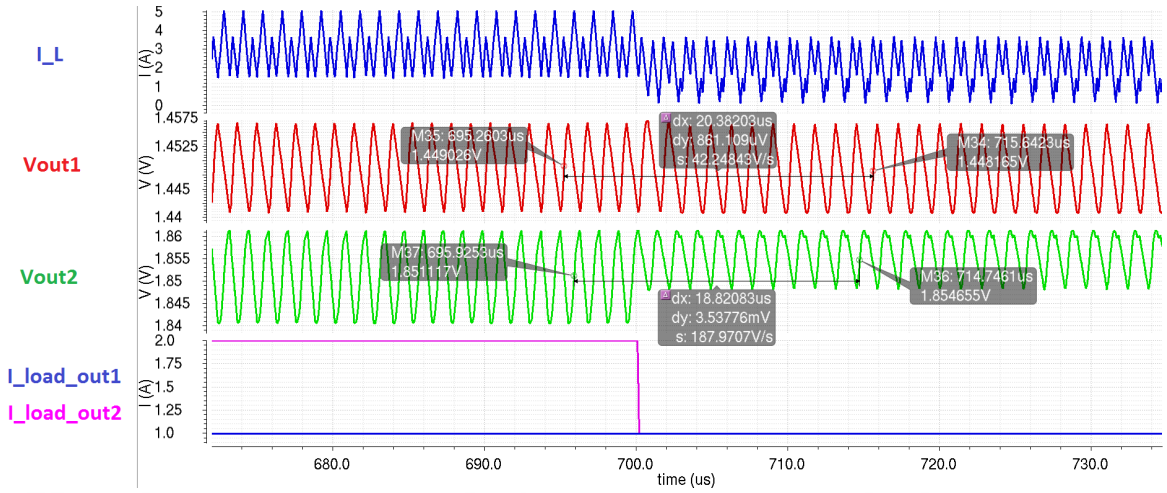

Figure 4.16. Cross regulation results for output 2 having load transient from 2A to 1A.

All four zoomed load transients showing static (DC) cross regulation and also transient cross regulation from load transient results are listed in Table 4.3. Note that cross regulation is defined as the change of the output voltage (mV) divided by the change in load current (mA) as Figure of Merit (FOM) for comparison. When the load current changes from 1A to 2A, the load current change is 1000mA. Maximum static voltage change for cross regulation is 0.9mV and this makes FOM 0.0009 mV/mA. Maximum transient voltage change for cross regulation is 6.3mV and this results in a FOM of 0.0063 mV/mA. As a result, maximum static cross regulation FOM is 0.0009 mV/mA and maximum transient cross regulation FOM is 0.0063 mV/mA.

Table 4.3. Cross regulation simulation results.

Output 1 Load (A)	**Output 2 Load (A)**	**Output 1 Cross Regulation Static (mV)**	**Output 1 Cross Regulation Transient (mV)**	**Output 2 Cross Regulation Static (mV)**	**Output 2 Cross Regulation Transient (mV)**
1 ⇒ 2	1	Undefined	Undefined	0.3	6.3
2	1 ⇒ 2	0.5	5.5	Undefined	Undefined
2 ⇒ 1	2	Undefined	Undefined	0.4	2.9
1	2 ⇒ 1	0.9	0.6	Undefined	Undefined

Many single inductor double output (SIDO) and single inductor multiple output (SIMO) designs have been presented in the literature. Table 4.4 shows the main parameters and some performance figures of this work compared with earlier works. The proposed design exceeds prior art by having 0.0063 mV/mA of cross regulation and 2.5A of current drive capability at each output with a peak efficiency of 93.7 %. The presented SIDO buck converter supports wide range of output voltage with broad supply voltage. Note that, comparison table is arranged in a chronological order to display the historical progress of SIDO and SIMO converters for some performance metrics.

Table 4.4. Comparison with prior art.

	Process (μm)	**Results from**	**Type**	**Supply (V)**	**Output Voltage (V)**	**Ind. (μH)**	**Cap. (μF)**	**Voltage Ripple (mV)**	**Load Current (max) (mA)**	**Cross Regulation (mV/mA)**	**Max. Eff. %**
This work	0.18	Post-layout Simulation	SIDO	3-5	0.9-2.5	0.22	50	$\leq$ 30	2500+2500	0.0063	93.7
JSSC 2022 [10]	0.15	Measurement	SIMO	1-5	0.8-3.6	2.2	10	$\leq$ 28	N/A	0.03	94.3
JSSC 2021 [11]	0.13	Measurement	SIDO	2.7-4.2	0.8-1.6	66	2.2	$\leq$ 20	600+600	0.01	89.5
CICC 2020 [12]	0.18	Measurement	SIMO	1.8	0.4-1.6	4.7	1.5	N/A	450	0.01	87.5
SPIES 2020 [13]	0.18	Simulation	SIDO	12	3.3-5	N/A	N/A	$\leq$ 120	500+500	0.066	86.32
PE 2019 [27]	0.25	Measurement	SIDO	4-5.5	1.8-3.3	4.7	4.7	N/A	400+400	0.015	94
ISCAS 2016 [15]	0.18	Simulation	SIDO	4	2-2.4	4.7	2.2	$\leq$ 20	200	0.58	87.32
PE 2016 [14]	0.35	Measurement	SIMO	1.8-2.9	1.8-3.3	3.3	10	N/A	34+156	0.013	89
JSSC 2015 [16]	0.35	Measurement	SIMO	5	N/A	10	10	$\leq$ 40	N/A	0.1	88.7
AICSP 2012 [17]	0.13	Measurement	SIMO	1.5	N/A	1	10	N/A	300	0.02	93.46
JSSC 2011 [18]	0.055	Measurement	SIDO	2.7-3.6	1.2-1.8	4.7	4.7	N/A	300+300	0.02	91
JSSC 2011 [19]	0.35	Measurement	SIDO	1.8-2.4	3-3.6	1	9.4	$\leq$ 200	1000	0.07	91.6
PE 2010 [28]	0.25	Measurement	SIDO	2.8-5	1.2-1.8	4.7	22	N/A	400+200	0.027	87
JSSC 2009 [20]	0.25	Measurement	SIMO	1.8-2.2	1.2-2.2	10	33	$\leq$ 22	N/A	0.035	93
CICC 2009 [26]	0.35	Measurement	SIDO	1.8-2.4	3-3.6	1	4.7	N/A	600	0.05	87.8
JSSC 2007 [24]	0.5	Measurement	SIMO	2.5-4.5	5-12	10	4.7	$\leq$ 160	110	0.01	80.8

5. CONCLUSION AND FUTURE WORK

This study introduces a novel Single Inductor Double Output (SIDO) hysteretic buck converter which aims to balance the load regulation of both outputs by constantly monitoring the outputs and then adjusting one output with respect to the other in an iterative way to enhance the operation. Load balancing scheme prioritizes the inductor current delivery for the output which has an abrupt load change and then returns back to the initial output, and this cycle repeats to minimize the voltage drop for both outputs. Consequently, the duty cycles of both outputs are adjusted in order to have less voltage drop and less cross regulation. In addition to iterative duty cycle adaptation, a frequency counter is incorporated to accelerate the transient response further. Moreover, a delay locked loop is utilized to fine tune the duty cycle to enhance the steady state cross regulation and also to limit the switching frequency spectrum. The proposed design outperforms similar designs in terms of cross regulation, while maintaining similar or better efficiency than most. Post-layout simulations demonstrate that this buck converter has a static cross regulation of 0.0009 mV/mA and transient cross regulation of 0.0063 mV/mA. Efficiency is also increased by load balancing of both outputs harmoniously and 93.7 % peak efficiency is reached. Power delivery capability is improved by driving 2.5A of load current at each output and 10W of total power which exceeds previous studies.

As future work some modifications could be done to improve the performance metrics. Load balance blocks fine tune digital bits which are coming from delay lock block could be increased to 5 or 6 bits and also counter could be modified to count 2 and 4 bits each time depending on the conditions to speed up the settling of the delay lock block for more bits.

Another possible improvement could be to change the bulk connection of the output switch device so that no need to second device and the connection of back to back. This way output switch device size could be reduced greatly, which will result in a reduction of the total chip area. However care must be taken not to turn on the

body diodes otherwise the load regulation will be severely affected.

Power consumption at no or low load conditions can be improved further by reducing some block currents. Output voltage comparators can be set to low quiescent current condition, where they are still functional but have tolerable delays. DAC block currents can also be reduced further by reducing their voltage buffer current consumption. Similar to the DAC block, current consumption of the voltage buffers in the bias blocks can be also reduced. Load balancer block quiescent current consumption can be reduced to a bleeding current, whereby the block is still functional but consumes less power at no or low load conditions.

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APPENDIX A: A MODEL OF HYSTERETIC BUCK CONVERTER

Basically, hysteretic converter can be modeled as a simple hysteresis comparator, two switches one inductor, one capacitor and one load resistor. Ideal hysteresis comparator is built with two comparators and a RS latch. Also to model the inductor current reaching zero at DCM, an ideal comparator is used to model the active diode comparator. The basic ideal model can be seen in Figure A.1.

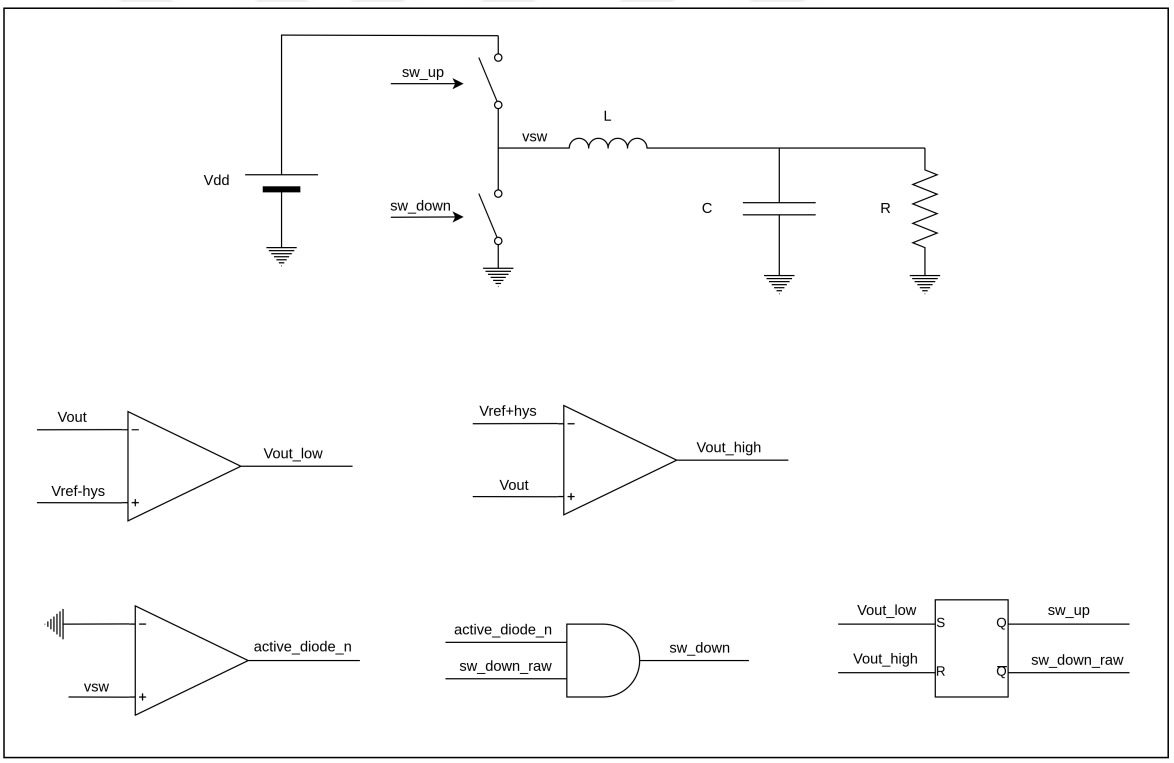

Figure A.1. Hysteretic buck converter build model with ideal elements.

Since there is one inductance and one capacitance in the circuit this circuits voltage and current equations will be second order exponential equations. In literature there are several models which are used with these second order exponential equations [29] and [42] which are mostly based on state space averaging method and hard to interpret the inter dependency of the circuit parameters. Also from going basic ideal

elements to actual design its complexity will increase due to added elements to model actual circuit. Thus, it's important to build a simple first order linear mathematical model which could be used to understand the behavior of the converter and also very beneficial for the design phase too. With this first order model, inter dependency of the converters parameters and relation between them will be easy to interpret.

$$V_L = L\frac{\mathrm{d}i}{\mathrm{d}t} \quad \text{for a linear interval we can write as} \quad V_L = L\frac{\triangle I}{\triangle t} \tag{A.1}$$

$$\text{after arranging} \quad V_L\triangle t = L\triangle I \quad \text{with average voltage we obtain} \quad \overline{V_L}\triangle t = L\triangle I. \tag{A.2}$$

Similar for the Capacitor equation

$$I_C = C\frac{\mathrm{d}v}{\mathrm{d}t} \quad \text{for a linear interval we can write as} \quad I_C = C\frac{\triangle V}{\triangle t} \tag{A.3}$$

$$\text{after arranging} \quad I_C\triangle t = C\triangle V \quad \text{with average current we obtain} \quad \overline{I_C}\triangle t = C\triangle V. \tag{A.4}$$

To be able to use a first order model, initially inductor and capacitor equations must be in the form of the first order which will give enough accuracy and be simple to use. Thus, from actual inductor and capacitor equations, first order equations of them are derived as; (A.1), (A.2), (A.3), and (A.4). Now we can use first order equations of inductor and capacitor rather than differential equations with the assumption of being linear in the interested region.

A.1. DCM Linear Equations

In this mode first inductor is connected to the input voltage to supply current to the load and also to charge the output capacitor and inductor. This charging continues until the output voltage is reached to the upper threshold of the hysteresis comparator. Upper switch in Figure A.2 is the switch which turns on for the on phase of the conduction mode. Then this switch turns off and active diode turns on automatically which is shown as bottom switch in the Figure A.1. Stored current in the inductor is used as energy source to supply current for both load and output capacitor and when the current inside inductor depletes output capacitor supplies current to the

load. Also output capacitors voltage decreases with sourcing current to the load and when its voltage reaches the lower threshold of the hysteresis comparator upper switch turns on and this cycle repeats itself.

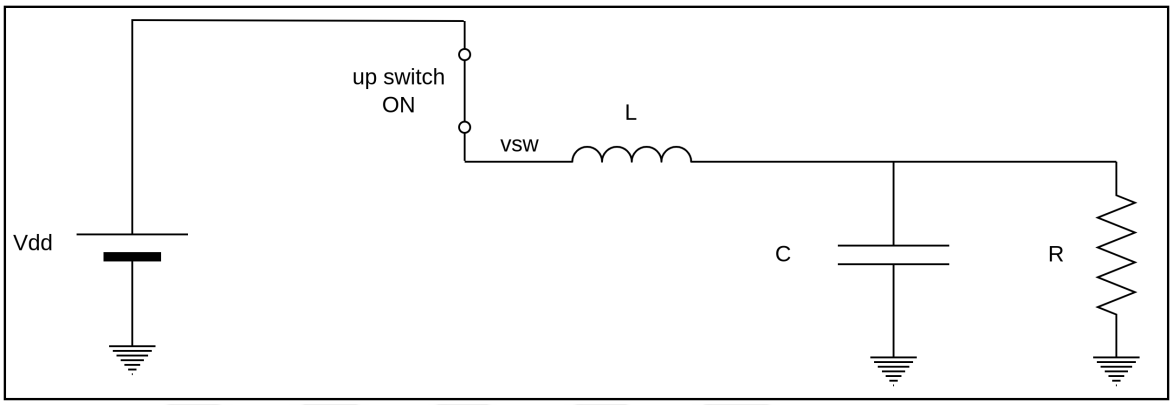

Figure A.2. Charging of the inductor at DCM.

Charging of the inductor has two sub regions of operation. In the first sub region output voltage is not ramped up instantly because inductor current does not rise immediately as the natural behavior of the inductor. Thus, in the first sub region the time which the inductor current reaches to the output load current is calculated. Then after this first sub region output voltage rises with the increased inductor current and second sub region is ended with the time of output voltage reaching the upper threshold of the comparator.

In the first sub region with the help of the linear equation the time which inductor current goes from zero to two times of the load current is calculated. Two times of the load current means that one load current is send to load and the other one load current stores in the inductor which then the net current to the load is more than the load pulling. From this point output voltage increase. Thus, writing the equation with the help of first order inductance equation becomes as

$$\frac{V_1 + V_2}{2} \triangle t_1 = L * I_1. \tag{A.5}$$

For the sake of clarity, equations which are used will present the main idea with simplified equations to not be confused with the detailed mathematical long equations.

Also, at actual equations, switch resistances are taken into account which will increase complexity. Here V_1 is the voltage of the inductor at the starting point of this operation region and similarly V_2 is the voltage of the inductor at the end of this operation region.

$$\frac{V_2 + V_3}{2} \triangle t_2 = L(I_2 - I_1) \qquad \frac{I_2 + I_3}{2} \triangle t_2 = C(V_3 - V_2) \tag{A.6}$$

At the second sub region (A.6) of the inductor charging phase, delta time is the time between the sub region 1 to the reaching the point of upper threshold of the hysteresis comparator.

Next phase is the inductor current discharging both to the load and the output capacitor which is shown at Figure A.3. Also in this phase there are again two sub regions. First one is started with the turning of the upper switch and at the same time turning on of the active diode. It ends with a maximum output voltage going beyond the upper threshold of the hysteretic control voltage (A.7).

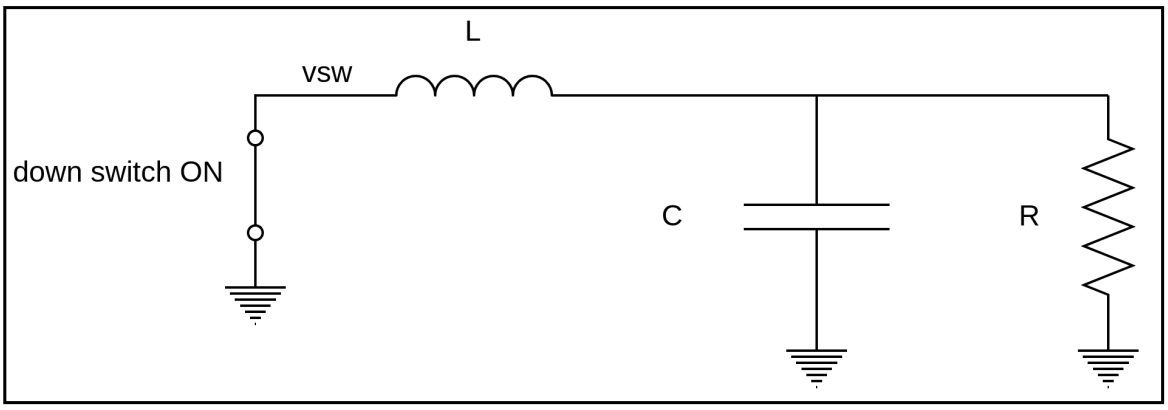

Figure A.3. Discharging of the inductor at DCM.

Inductor voltage can be written with discharging current to find the values

$$\frac{V_3 + V_{max}}{2} \triangle t_3 = L(I_3 - I_2) \qquad \frac{I_3 + I_4}{2} \triangle t_3 = C(V_4 - V_3). \tag{A.7}$$

Next sub region is the time frame starting with the maximum output voltage time to the inductor current depletes to zero time and it can be solved by

$$\frac{V_{max} + V_4}{2} \triangle t_4 = L * I_3. \tag{A.8}$$

Last phase of the DCM is the region when output capacitor goes to lower threshold of the hysteresis comparator and it can be expresses as

$$\frac{I_4 + I_5}{2} \triangle t_5 = C(V_6 - V_5), \tag{A.9}$$

$$\frac{I_4 + I_5}{2} \triangle t_5 = C(V_6 - V_5). \tag{A.10}$$

Figure A.4 shows that output capacitor is discharging at load resistor R (A.10).

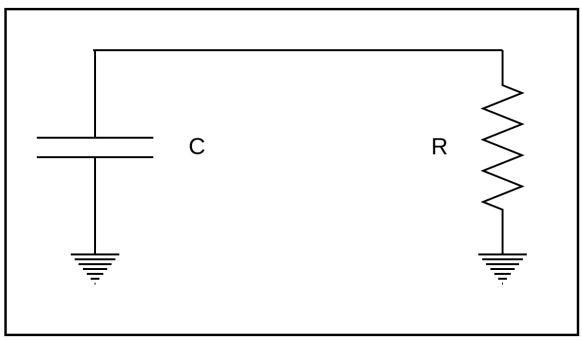

Figure A.4. Discharging of the capacitor to load resistor at DCM.

A.2. CCM Linear Equations

Mainly CCM has two phases inductor charging and discharging phases. At charging phase upper switch is on which connects inductor to the power supply and at discharging phase down switch is on which connects the inductor to the ground. Figure A.1 shows the main used model as a reminder. In inductor charging phase like in DCM mode there are also two sub regions. The first sub region starts with hysteresis

comparators lower threshold reach signal and ends with current polarity change of the output capacitor.

$$\frac{V_1 + V_2}{2}\triangle t_1 = L(I_2 - I_1) \qquad \frac{I_1}{2}\triangle t_1 = C(V_2 - V_1) \tag{A.11}$$

Second sub region of the inductor charging starts with the ending of the sub region 1 and to the upper threshold of the hysteresis comparator. Equations are similar like in the sub region 1.

$$\frac{V_2 + V_3}{2}\triangle t_2 = L(I_3 - I_2) \qquad \frac{I_2}{2}\triangle t_2 = C(V_3 - V_2) \tag{A.12}$$

Discharging phase of CCM starts with the upper threshold hysteresis comparator's signal, charging switch turns off and active diode turns on. Discharging phase also has two sub regions like charging phase. First sub region ends with the current polarity change of the output capacitor like in the charging phase of CCM.

$$\frac{V_3 + V_4}{2}\triangle t_3 = L(I_4 - I_3) \qquad \frac{I_3}{2}\triangle t_3 = C(V_4 - V_3) \tag{A.13}$$

Second sub region of discharging starts with end of the first sub region and ends with the lower threshold reach signal of the hysteresis comparator (A.14).

$$\frac{V_4 + V_5}{2}\triangle t_4 = L(I_5 - I_4) \qquad \frac{I_4}{2}\triangle t_4 = C(V_5 - V_4) \tag{A.14}$$

A.3. CCM-DCM Transition

Mainly current demand of the output load decides the mode of the converter as CCM or DCM. Since at DCM mode output load is relatively small and at some portion of the period output capacitor's stored energy will be enough to supply the output load. However, in the CCM mode current demand is high and inductor is in always conducting currents to the load. Thus, to find out at which value of the output load converter changes its mode, inductor current can be used. If we assume the minimum inductor current as zero at CCM mode and we solve CMM equations we can find the minimum load for the mode transition between CCM to DCM.

A.4. Comparison of The Linear Mathematical Model With Actual Results

Prepared equations for DCM, CCM and CCM-DCM transition are solved with mathematical solvers. Initially, step by step equations compared with actual results and then whole equations for four different cases are solved and results are compared with actual circuit simulation results which are obtained by ideal model of the hysteretic buck converter. Generally duty cycle of the charging switch and switching frequency is used as comparison criteria however currents and voltages are compared too. For each DCM and CCM two different sets of model parameters and for the CCM-DCM one different set of model simulation results are compared. For these sets inductor, capacitor, load resistor and hysteresis values are changed. Table A.1 shows the comparison of four different sets both for simulation and mathematical model results for duty cycle of the inductor and switch frequency of the inductor.

Table A.1. Comparison of mathematical model with simulation results.

	Model Duty Result (%)	**Simulation Duty Result** (%)	**Duty Error** (%)	**Model Frequency Result (kHz)**	**Simulation Frequency Result (kHz)**	**Frequency error (kHz)**
DCM-1	33.07	32.97	-0.1	400.5	398.4	-2.1
DCM-2	22.67	22.34	-0.33	283.4	275.8	-7.6
CCM-1	41.18	41.34	0.16	160.5	164	3.5
CCM-2	50.94	50.93	-0.01	154.1	167	12.9

As can be seen from CCM-2 values frequency error is relatively huge. For CCM, 8 different first order equations have been tried to solve with mathematical solver functions and this huge error is related to solvers un-satisfied convergence. Several different solvers are used however some even gave worst results. A comparison is also made for the transition resistor load value which hysteretic buck converter changes from DCM to CCM and vice versa. Table A.2 shows the transition resistor load both from simulation result and mathematical model result.

Table A.2. DCM-CCM Transition load mathematical and simulation result.

	Simulation Result (Ω)	**Model Result (Ω)**
DCM-CCM Transition Load	0.76	0.72

As conclusion, hysteretic buck converter first order equations are used to find the operating point for the duty cycle and frequency for the given circuit specifications. Three different set of equations are used for one for DCM, one for CCM and also one for CCM-DCM transition. For the DCM, difference between circuit simulator and mathematical model results seems reasonable however, for one CCM case due to the convergence problems error is increased for some calculations. For transition load resistor circuit level simulations are very close to the mathematical model result.