AGING IN CMOS CIRCUITS AND CIRCUIT DESIGN ROBUST TO AGING PHENOMENA

by

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ABSTRACT

AGING IN CMOS CIRCUITS AND CIRCUIT DESIGN ROBUST TO AGING PHENOMENA

The subject of aging in CMOS circuits has been examined and some reliability simulations have been run for analog CMOS circuits in order to observe the effects of this phenomenon on the reliability of CMOS circuits in this work. Electronic circuits also have a useful lifetime as everything in the nature. This time can be defined as a regular period where the circuit is able to work properly and do its function accurately. Despite the fact that rapid advances in semiconductor technology brings many advantages, there are also some drawbacks. One of these negative consequences is reduction of reliability of circuits. Aging isn't a new trend for the CMOS circuits but, after the iteration of Moore's law which pushed the transistor channel length to under 180 nm, the subject of aging has been elevated from an academic exercise to a growing, and perhaps a detrimental concern which the foundries have focused on. In order to understand the physical mechanisms and create solutions to this phenomenon, reasons should be manifested clearly by both researchers and foundries. There are a number of physical failure mechanisms affecting the reliability of a CMOS ASIC. Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI), Time Dependent Dielectric Breakdown (TDDB) and Electromigration are the most common failure mechanisms. The physical causes are investigated and a number of aging models of these mechanisms were discussed in the initial chapters. In addition to this theoretical study, three diverse CMOS Cross-Coupled Differential LC Oscillators (NMOS, PMOS, and CMOS) were designed to observe the aging effects on phase noise of each structure, reliability simulations were run for each structure, and the study is completed by evaluating all of these results.

ÖZET

CMOS DEVRELERDE YAŞLANMA VE YAŞLANMAYA DAYANIKLI DEVRE TASARIMI

Bu çalışmada, CMOS devrelerde yaşlanma sorunu araştırılmış ve bu sorunun CMOS devrelerin dayanıklılığına olan etkisi bir analog devre üzerinde güvenilirlik testleri gerçekleştirerek incelenmiştir. Doğada bulunan herşey gibi elektronik devrelerin de bir ömrü vardır. Bu süreyi, devrenin fonksiyonunu hatasız bir biçimde gerçekleştirebildi-ği zaman aralığı olarak tanımlayabiliriz. Yarı iletken teknolojisindeki hızlı ilerlemeler yanında bir çok yarar getirdiği gibi aynı zamanda bazı sorunlar da oluşturmaktadır. Bu olumsuz sonuçlardan birisi de devrelerin dayanıklılığının azalmasıdır. Yaşlanma olayı CMOS devreler için yeni bir kavram olmadığı halde, özellikle transistor kanal boyunun 180 nm'nin altına indirilmesi ile yaşlanma sadece bir araştırma konusu olmaktan çıkmış, aynı zamanda üretici firmaların da yakından ilgilendiği önemli bir sorun haline gelmiştir ve bu konuda gerek üretici firmaların gerekse araştırmacıların çözümler ortaya koymaları gerekmektedir. Bu yüzden bu calışmada, CMOS devre-lerde yaşlanmaya sebep olan 4 farklı fiziksel olay (Sıcak Taşıyıcı Enjeksiyonu, Negatif Tabanlı Sıcaklık Kararsızlığı , Zamana Bağlı Yalıtkan Bozulması ve Elektron Göçü) araştırılmış ve bu araştırmaya ek olarak üç farklı yapıda çapraz baglı farksal CMOS osilatör devresi tasarlanarak, yaşlanma olayının her bir osilatörün faz gürültüsüne etkisi incelenmiş, güvenilirlik benzetimleri yapılmış ve çalışma tüm bu sonuçların yorumlanmasıyla tamamlanmıştır.

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LIST OF SYMBOLS

$E_{\perp}$	Vertical Electric Field
$E_{\parallel}$	Parallel Electric Field
E_{ox}	Oxide Electric Field
g_{m}	Transconductance of a MOSFET
I_{d}	Drain current of MOSFET
I_{g}	Gate current of MOSFET
I_{sub}	Substrate current of MOSFET
I_{submax}	Maximum substarte current of MOSFET
J_{avg}	Average Current Density
J_{peak}	Peak Value of Current Density
J_{rms}	RMS value of Current Density
q_{bd}	Charge Breakdown
R_{g}	Post Breakdown Resistance
$T_{\mathrm{B}}(E_{\mathrm{ox}})$	Tunnel probability of hot electrons
V_{d}	Drain voltage of MOSFET
V_{ds}	Drain to source voltage of MOSFET
V_{dsat}	Drain voltage of MOSFET at saturation
V_{g}	Gate voltage of MOSFET
V_{gs}	Gate to source voltage of MOSFET
V_{th}	Threshold voltage of MOSFET
$\Delta \mathrm{N}_{\mathrm{it}}$	Interface Trap Density
φ_s	Surface potential
ϕ_{b}	Energy barrier
ϕ_{it}	Critical energy for device damage
γ	Noise factor of a FET
μ_0	Mobility of MOSFET

LIST OF ABBREVIATIONS

CHC	Channel Hot Carrier
CHE	Channel Hot Electron
CAD	Computer Aided Design
CDCCO	CMOS Differential Cross Coupled Oscillator
CMOS	Complementary Metal Oxide Semiconductor
DAHC	Drain Avalanche Hot Carrier
EM	Electro Migration
FN	Fowler-Nordheim
HBD	Hard Breakdown
GIDL	Gate Induced Drain Leakage
HCI	Hot Carrier Injection
LEM	Lucky Electron Model
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTTF	Mean Time To Failure
MVE	Multiple Vibrational Excitation
NDCCO	NMOS Differential Cross Coupled Oscillator
NBTI	Negative Bias Temperature Instability
NMOSFET	N Channel Metal Oxide Semiconductor Field Effect Transistor
PBTI	Positive Bias Temperature Instability
PMOSFET	P Channel Metal Oxide Semiconductor Field Effect Transistor
SBD	Soft Breakdown
SEM	Scanning Electron Microscope
SGHE	Secondary generated hot electron
SHE	Substrate Hot Electron
SHH	Substrate Hot Hole
SILC	Stress Induced Leakage Current
SoC	System on Chip
TDDB	Time Dependent Dielectric Breakdown

VCO	Voltage Controlled Oscillator

1. INTRODUCTION

Thanks to the rapid developments in semiconductor technology, circuit properties such as speed, power consumption, supply voltage, and chip area can now be improved easily. As the dimensions are scaled down, supply voltages also decrease as a result transistors have lower threshold voltages. Power consumption and chip area also decrease with developing technology. Besides these advantages, there are also some drawbacks considering the concept that 'every gain has a loss'. The subject of aging is one of the disadvantages which can be considered as a consequence of the advanced technology. Aging of circuits refers to the degradation of circuit performance over time. Circuits lose their functionality with time and run out at the end of the life period. The length of proper operation is changed from a few years to a few months with respect to worst-case conditions. Considering all of these, reliability has become a crucial concept for foundries because consumers always prefer the product which is more reliable and has longer lifetime. At this point, designers should take into consideration reliability concerns in order to provide their consumers with more robust and durable products. They should research all the reasons causing reliability problems, examine the effects on circuit performance, model the physical phenomena and create accurate solutions to overcome to this issue.

It can be argued that transistors have always aged. However, this aging wasn't significant until the iteration of Moore's law which pushed the channel length of the transistor to 0.18 μm. Under 0.18 μm channel lengths, reliability has become more significant concern in IC world. The simultaneous use of extremely small channel lengths and higher operating frequencies has elevated circuit aging from an academic exercise to a growing, and perhaps detrimental, concern for system-on-a-chip (SoC) designs. Reliability of a circuit is directly proportional to the amount of failure rate of its function and studies on the subject of aging have clearly showed that the electrical properties of circuits change over time. The curve shown in Figure 1.1 called "Bathtub Curve" which is used for reliability in engineering can also be used to illustrate the relationship between the failure rate and time.

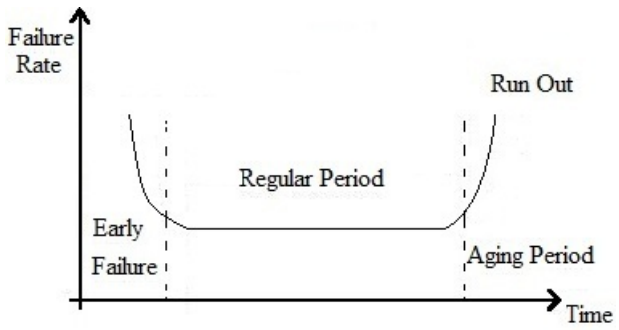

Figure 1.1. Bathtub Curve represents the circuit life period as three different slots: Early Failure, Regular Period, and Aging Period.

According to this curve, there are mainly three distinct sections: early failure, regular period, and aging period for ICs. The first section (the left side of the curve) is only related to the foundries. The products in this area as a result of faulty production have high failure rates and would never reach the normal operating period in their lifetime. Thereby, IC providers should catch these devices before they come on the market. The second section (the center of the curve) called "Regular Period" represents the products which successfully passed the burn in tests and offered to the market. Regular period should be the longest period among all life period of products because the efficiency of the product reaches the maximum value at this period. Furthermore, the object of research which strives to increase the reliability of a product is to extend this straight line as much as possible. At last, circuits which pass the first and second sections, reach the part of the curve called "Aging Period". Circuits start to lose their functionality at the beginning of this section and finally complete their life at the end of the curve which is called "Run Out".

Reliability can also be defined as the length of the useful lifetime, thus the longer the regular slot, the more reliable the devices are. In order to achieve more reliable circuits, physical reasons of the aging must be clearly exhibited and solutions must be offered. In this sense, physical causes of aging in CMOS circuits will be a main subject of this study.

Aging in CMOS circuits stems from four major physical phenomena: Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), Time Dependent Dielectric Breakdown (TDDB), and Electromigration (EM). HCI affects NMOS transistors and is effective only while transistors are conducting current. NBTI (Negative BTI) affects PMOS transistors and is effective when the transistor is on; however, PBTI (Positive BTI) seen in NMOS transistors isn't as effective as NBTI, so its effects can be neglected compared to the other reliability issues. While aging affects digital circuits during the switching time, analog circuits are affected during the whole operation period. Both NBTI and HCI effects manifest themselves as a reduction in the drain current as the devices age which causes timing violations in digital circuits and transconductance reduction in analog circuits. TDDB on the other hand, causes the dielectric to break down and become electrically shorted after some operation time. Another aging mechanism occurring in CMOS circuits is Electromigration, which is an interconnect degradation phenomenon and can be avoided by limiting current density in the wires to safe limits. All of these causes will be covered in this thesis within a physical background part. However, studying and understanding the reasons of aging are not sufficient to analyze the aging phenomena. Experiments should be performed and results should be examined to clarify the subject of aging. In this context, a couple of CMOS Differential Cross-Coupled LC oscillator circuits were designed in order to understand the aging effects in analog circuits.The oscillator is a nonlinear circuit, and even small changes in voltages or currents at any node may cause great deviations at the outputs. Due to the fact that aging leads to changes in transistor current and transconductance, the oscillator will show irregular behavior when it ages. Therefore, oscillator circuits have been simulated with both fresh and old transistors and phase noise has been examined for both situations. All results were evaluated at the conclusion and robustness of oscillators were compared and the most reliable structure was determined according to the their phase noise behaviors over time.

In summary, aging is an increasingly important phenomenon for CMOS circuits due to the scaling down of device dimensions. This study provides a review including the most important reliability issues for CMOS circuits. Moreover, a general insight

of the effects of aging on CMOS circuits can be observed thanks to the aging analysis of LC oscillators whose design procedure was explained, reliability analysis was performed, and consequences were evaluated in Chapter 4, 5, and 6 respectively.

2. PHYSICAL BACKGROUND

Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), Time Dependent Dielectric Breakdown (TDDB), and Elecromigration (EM) are the most known mechanisms which cause aging in CMOS circuits. Each of these mechanisms is quite complicated and requires a profound knowledge of solid state physics. The aim of this section is to provide an overview of the knowledge accumulated regarding these physical phenomena rather than discussing the details of all the underlying mechanisms.

2.1. Hot Carrier Injection

The term "hot carriers" refers to either holes or electrons (also referred to as "hot electrons") that have gained very high kinetic energy after being accelerated by a strong electric field in regions with high field intensities [1]. Because of high energy, hot carriers get injected and trapped in regions of the device where they do not normally exist, forming a space charge, causing the device to become unstable. The term "hot carrier effects", therefore refers to device deterioration or instability caused by hot carrier injection.

Over the years, as MOS dimensions scaled down to sub-micron levels, electric fields have increased, resulting in increasingly substantial HCI effects. In NMOS transistors, the primary impact ionization can take place at the drain edge, where the carriers reach the saturation velocity [2]. The electrons are collected by the drain and the holes join the substrate and cause the substrate current. Furthermore, the holes can ionize again the atoms of the substrate and second ionization occurs, generating electrons, which are then accelerated towards the gate by the vertical field of the depletion zone. They acquire sufficient energy to penetrate into the gate, thus resulting in a gate current. The maximum hot carrier damage has traditionally been associated with the peak I_{sub} region approximately $V_{\text{gs}} \approx V_{\text{ds}}/2$ due to the creation of interface states and the substrate current is exponentially proportional to $V_{\text{ds}} - V_{\text{dsat}}$ [3]. The longitudinal electric field responsible for primary impact ionization generates hot car-

riers with energy around 1.5 eV, whereas secondary impact ionization generates hot carriers with energy values of 3to3.5 eV. Various experiments were run on a 0.18 μm and a 0.1 μm technology [2, 3, 4].

Traditionally, it had been assumed that HCI was negligible in p-channel devices [5]. This was due to their lower hole mobilities. Measurements were performed for similar n and p transistors [5, 6] to verify this assumption. The data obtained show that not only are hot electrons present in the PMOS device, but in the avalanche bias region ($V_{\rm ds} >> V_{\rm gs}$), the gate current is larger than the NMOS device. It should be noted that the n-channel device is more efficient in generating hot carriers (about 3 times) as can be measured from the bulk currents. However, when biased in the active mode, the gate appears positive with respect to the drain in PMOS transistors (thus attracting electrons), whereas appearing negative for the NMOS transistors (thus repelling electrons, and attracting holes). The effects of gate and drain voltage waveforms on the hot carrier induced MOSFET degradation are studied in [7]. According to results of [7], the pulsing of drain voltage is shown to introduce no perceivable difference in device degradation. It has been found that the falling edge of the gate pulse in the presence of high drain voltage is a main source of the enhanced degradation rates [7]. Moreover, it was noted that the degradation rate under AC stress is predictable from the expected substrate current waveform in a straightforward manner.

There are four common hot carrier injection mechanisms. These are: Drain Avalanche Hot Carrier injection (DAHC), Channel Hot Electron injection (CHE), Substrate Hot Electron injection (SHE), and Secondary Generated Hot Electron injection (SGHE). In the following sections, physical backgrounds of these mechanisms will be discussed. The order of these mechanisms has been arranged from the most important to the least.

2.1.1. Drain Avalanche Hot Carrier

Drain avalanche hot carrier (DAHC) injection occurring at the maximum substrate current condition ($I_{\rm submax}$) is serious in NMOS devices [8] where interface trap

generation decreases the drain current [9, 10, 11]. At stress conditions with higher V_{ds} and lower V_{gs}, the drain avalanche hot-carrier (DAHC) injection becomes important [12]. This occurs if a high voltage is applied to the drain under non-saturated conditions ($V_d > V_s$) and results in very high electric fields near the drain, which accelerate channel carriers to the drain region.

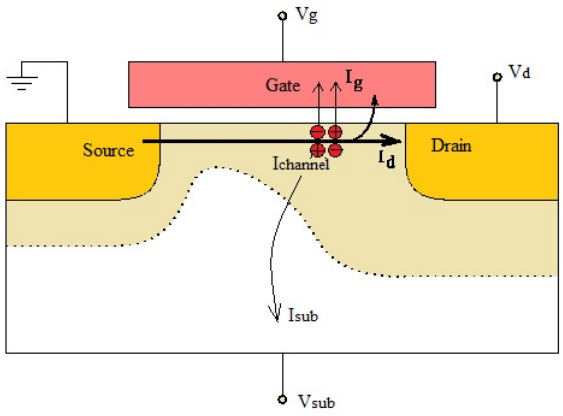

Figure 2.1. Hot carriers lead to impact ionization generating electron-hole pairs. In DAHC, hot electrons and hot holes are injected into the dielectric and some holes form a bulk current.

The acceleration of the carriers causes them to collide with silicon atoms, creating electron-hole pairs. This phenomenon is known as impact ionization, shown in Figure 2.1, with some of the displaced electron-hole pairs also gaining enough energy to pass over the electric potential barrier between the substrate and the gate oxide [1]. In NMOS transistors, the primary impact ionization can take place at the drain, where the carriers achieve the saturation velocity [2]. Under the influence of drain-to-gate field, hot carriers that surmount the substrate-gate oxide barrier get injected into the gate oxide. Hot carriers can be trapped at the Si/SiO_2 interface (hence referred to as "interface states") or within the oxide itself, forming a space charge that increases over time as more charges are trapped [1]. These trapped charges cause shifts in some of the characteristics of the device, such as threshold voltage (V_{th}) and mobility (μ_0).

2.1.2. Channel Hot Electron Injection

When the gate voltage is equal to the drain voltage, the channel hot-electron (CHE) regime reaches the maximum value [1]. Figure 2.2 shows this condition where "lucky electrons" [13, 14] which are attracted by the high gate voltage by means of gaining sufficient energy from the electric field across the channel to overcome to the Si/SiO_2 barrier at the drain [15].

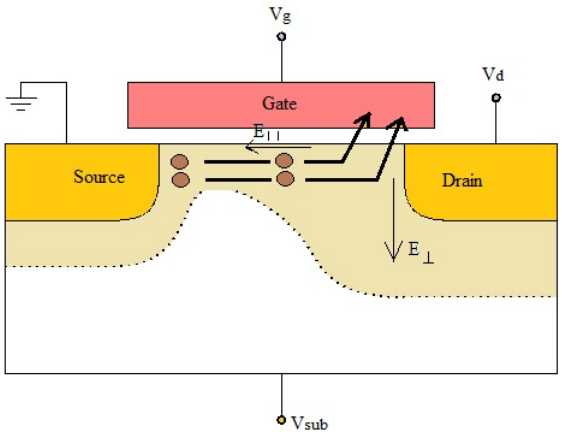

Figure 2.2. Channel Hot Electron (CHE) injection regime in NMOS. $E_{||}$ denote the lateral electric field at the drain side.

The effect of the drain voltage (V_d) on the surface potential (φ_s) reduces the conductivity of the channel near the drain side, thus increasing the lateral potential drop in the drain region [1]. Therefore, $E_{||}$ presents a larger value in proximity of the drain diffusion and the channel electrons reach very high energy values at the end of the channel [16]. As depicted in Figure 2.2, the hot electrons near the drain region have enough energy to pass over the Si/SiO_2 energy barrier (ϕ_b = 3.15 eV) and they are injected into the floating gate, accelerated by the oxide electric field E_ox [1]. Moreover, the channel hot electrons produce electron-hole pairs by means of Impact Ionization events in proximity of the drain edge of the channel. The generated secondary holes are collected by the substrate and they cause the substrate current I_sub [16, 17]. The secondary electrons have enough energy to penetrate into the gate

oxide, thus applying a small additional contribution to the gate current I_g. Therefore, the gate and the substrate currents have a common source, namely the electrons accelerated while traveling along the channel [1]. The injection efficiency, strongly based on the lateral electric field, that heats the channel electrons, and on E_{ox} in proximity of the drain, that influences the tunnel probability ($T_B(E_{ox})$) for the hot electrons [1]. Near the drain region, the V_d influence on φ_s reduces the available potential drop in the oxide (V_{ox}), hence E_{ox} and $T_B(E_{ox})$ [1].

2.1.3. Substrate Hot Electron/Hole Injection

SHE/SHH is commonly used to investigate the insulator qualities and for reliability tests [18, 19]. The benefit of this is that the energetic carriers at the interface are uniformly distributed along the channel contrary to the injection mechanisms described above, where the maximum of the injection is near the drain. As the surface potential ϕ_s is pinned, the oxide field is only controlled by the gate voltage. The potential drop in the substrate is determined by the substrate voltage V_{sub}.

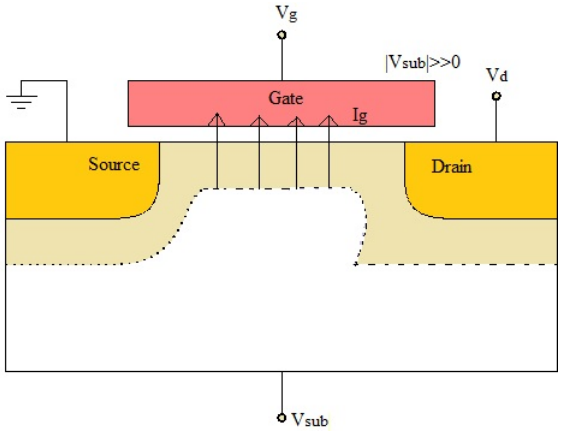

Figure 2.3. SHE injection involves trapping of carriers from the substrate to SiO_2.

According to Figure 2.3 showing the SHE mechanism, injection is a consequence of a high positive or negative bias at the substrate V_{sub} [12]. This causes to carriers in the substrate penetrate to the Si/SiO_2 interface. The substrate carriers are either

generated by optical generation or by electrical injection from a buried p-n junction. These carriers can eventually overcome the energy barrier at the interface and are injected into the oxide.

2.1.4. Secondary Generated Hot Electron Injection

SGHE includes the generation of hot carriers from impact ionization involving a secondary carrier that was created by an earlier incident of impact ionization [1]. This occurs under conditions similar to DAHC, i.e., the applied voltage at the drain is higher than the voltage at the gate side, which is the driving condition for impact ionization. The main difference occurs due to the influence of the substrate's back bias in the hot carrier generation [1]. This back bias results in a field that tends to drive the hot carriers generated by the secondary carriers toward the surface region, where they further gain kinetic energy to overcome the surface energy barrier [1]. Figure 2.4 represents the SGHE injection mechanism.

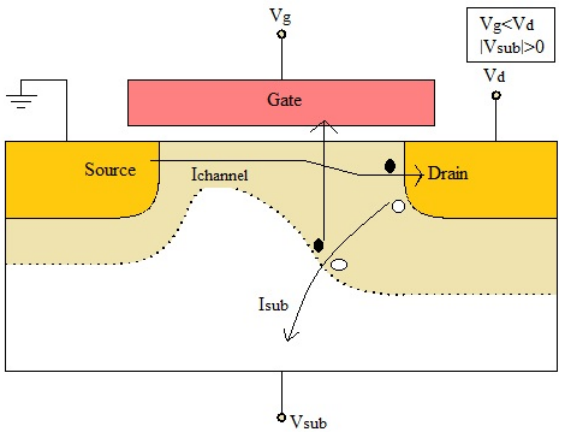

Figure 2.4. SGHE injection involves hot carriers generated by secondary carriers.

In summary, there are four different mechanisms causing hot carrier injection. When the drain voltage is higher than the gate voltage, DAHC occurs due to impact ionization and if an additional bias is applied to the substrate, SGHE occurs as well. On the other hand, if the drain voltage is around the gate voltage, CHC occurs and

reaches the maximum value when the gate voltage is equal to drain voltage. Lastly, SHH or SHE is used for reliability tests. A negative or positive bias voltage is applied to the substrate to direct the carriers to the interface state. All these conditions are summarized at the Table 2.1.

Table 2.1. Summary of HCI Mechanisms conditions.

Mechanism	Condition
DAHC	$V_{\mathrm{ds}} > V_{\mathrm{gs}}$
CHE	$V_{\mathrm{g}} \approx V_{\mathrm{d}}$
SHE/SHH	$\lvert V_{\mathrm{sub}} \rvert > 0$
SGHE	$V_{\mathrm{d}} > V_{\mathrm{g}}, \lvert V_{\mathrm{sub}} \rvert$

2.2. Negative Bias Temperature Instability

Among various failure mechanisms, Bias Temperature Instability (BTI), in particular Negative Bias Temperature Instability (NBTI) occurring in PMOS transistors, is emerging as one of the main reliability issues in nano-scale technologies [20]. From the physical point of view, PBTI and NBTI are due to the generation of traps at the Si/SiO_2 interface in positively biased NMOS or negatively biased PMOS, respectively [21]. Typically, transistor thresholds V_{th} increase, and other electrical parameters, such as drive current I_{d} and transconductance g_{m}, are also affected. At typical operating fields of SiO_2 transistors, BTI is only significant for PMOS transistors with negative gate bias (NBTI). A typical set-up for the observation of negative bias temperature (NBTI) degradation of a PMOS is schematically depicted in Figure 2.5. The substrate, the source, and the drain are grounded, while the gate is negatively biased. These bias conditions are applied at elevated temperatures, typically ranging between 100° C and 200° C, for a certain period of time.

2.2.1. Failure Mechanism

The high electrical field across the gate oxide in combination with an elevated temperature leads to an electrochemical reaction in the interface region between silicon

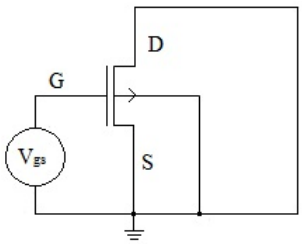

Figure 2.5. NBTI investigation set-up.

and gate oxide [22]. Figure 2.6 represents a schematic of the interface. Due to different lattice structures of monocrystaline silicon and the amorphous oxide, an interface region is occurred after gate oxide processing, which consists of only a few atomic layers and many dangling bonds and the open dangling bonds act as interface states [22]. They can catch carriers, trap them for a certain time and emit them back into the channel. Filled interfaces states shift the threshold voltage [22].

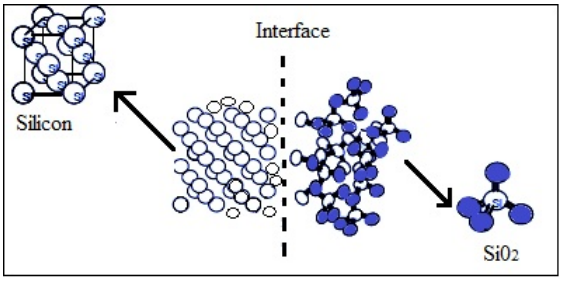

Figure 2.6. Schematic of the interface region of MOSFET.

There are two different mechanisms associated with BTI. One is the direct breaking of $Si-H$ bonds in the oxide. When a PMOS transistor is biased in inversion, the dissociation of $Si-H$ bonds along the silicon-oxide interface causes the generation of interface traps. The rate of generation of these traps is accelerated by temperature and the time of applied stress [20]. The process manifests itself as an increase in the threshold voltage (V_{th}) of the device, which results in a decrease of overdrive voltage, thus reduction of the driven current [20]. On the other hand, removal of the bias causes a reduction in the number of traps due to annealing.

The second event contributing to BTI is trapping. Besides of the interface states generation, some preexisting traps located in the bulk of the dielectric are filled with holes coming from the channel of the PMOS. Those traps can be emptied when the stress voltage is removed. This V_{th} degradation can be recovered over time.

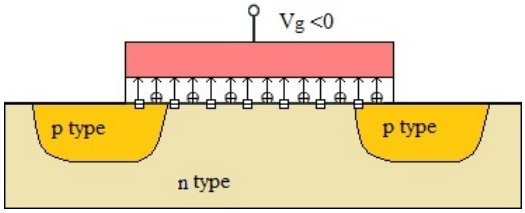

Figure 2.7. A cross-section of NBTI stressed PMOS.

Figure 2.7 shows a simplified cross-section of a NBTI stressed PMOS device. Positive oxide charges and filled donor-type interfaces are represented by circles and rectangles, respectively. NBTI has a pronounced process impact up to the passivation layer [22]. The process for gate oxide growing and the hydrogen inventory of the entire process influence the NBTI behavior [22]. $SiON$ gate oxides have enhanced NBTI, but the nitrogen fraction is necessary as a diffusion barrier in the gate oxide surface channel PMOS [22]. The barrier prohibits boron penetration from the p^+ doped poly-silicon into the channel [22].

Additionally, NBTI can also be categorized according to stress conditions: Static NBTI and Dynamic NBTI. Static NBTI corresponds to the case when the PMOS is under constant stress and this degradation can not be recovered. On the other hand, Dynamic NBTI corresponds to the case where the PMOS transistor undergoes alternate stress.

2.2.2. Recovery

Stress induced parameter degradation recovers very fast after the end of the stress. A peculiar property of the NBTI mechanism is the so called relaxation or re-

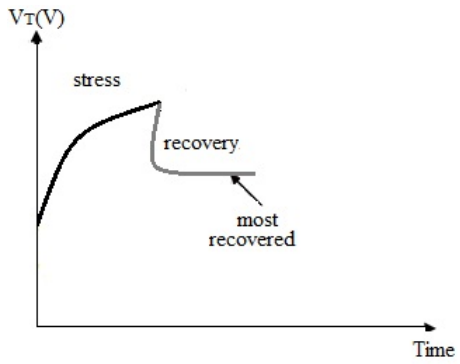

Figure 2.8. NBTI vs. time illustrating both degradation and recovery.

covery of the degradation immediately after the stress voltage has been reduced [23]. This greatly complicates the evaluation of NBTI, its modeling, and extrapolation of its impact on circuitry. The relaxation of the threshold voltage shift has been observed to have approximately a logarithmic time dependence and spanning times from microseconds to days [24, 25]. NBTI recovery is also expected to influence the response to AC stress [26]. It is clearly seen that NBTI degradation does not fully recover. Figure 2.8 shows a diagram of a typical PMOS NBTI degradation and recovery process reported in the literature. There is no consensus on the exact physical mechanism, but one of the leading models for PMOS NBTI recovery is the back diffusion of Hydrogen near the substrate/dielectric interface [27].

2.3. Electromigration

The material properties of the metal interconnects have a strong effect on the lifetime. The shape of the conductor, the crystallographic orientation of the grains in the metal, procedures of the layer deposition, heat treatment or annealing, characteristics of the passivation layer, and the interface to other materials affect the reliability of the interconnects. There are also serious differences with time dependent current: direct current or different alternating current waveforms cause different effects. Electromigration in the interconnects is the diffusion of metal atoms along the conductor in the direction of electron flow. This directional diffusion process occurs because of the

momentum transfer between the electrons and the metal atoms, which increases the probability that an metal atom will move in the direction of the electron flow shown in Figure 2.9 [28]. Since the mass of the electron is very smaller than the mass of the metal atoms, the transfer of momentum is only enough to have a statistical effect upon the diffusion of aluminum [28]. This diffusion process will preferentially fill metal ion vacancies placed in crystal defects, leaving a vacancy in the location from which the metal atom came [28]. All metal films have microstructural variations that lead to the

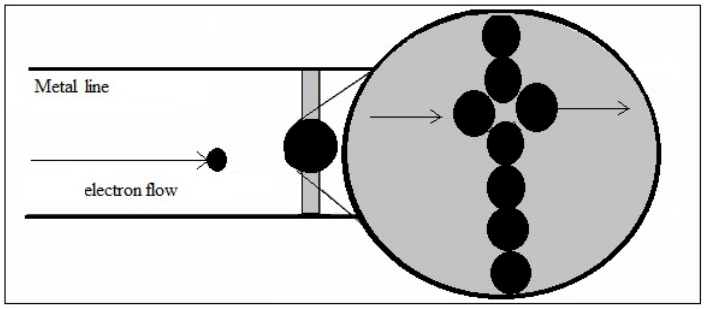

Figure 2.9. Momentum transfer between electron and metal ion.

atomic flow rates through them to be non-uniformly distributed. This non-uniform atomic flow rates through different sections of the conductor result in mass depletion which causes voids and mass accumulation causing small hills [29]. Figure 2.10 shows a void and a hillock placed on a metal wire [29]. There are two different scenarios for

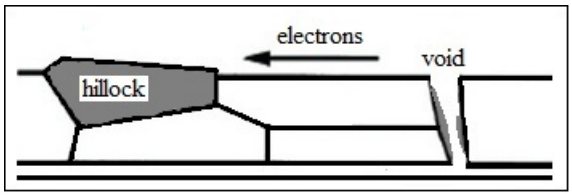

Figure 2.10. A void and a hillock which occurred due to electromigration.

metal wires after a long term electromigration degradation.

(i) An open circuit occurs when the voids formed in the metal line that becomes big enough to damage it.

(ii) A short circuit occurs when the small hills become long enough to behave as a bridge between the metal and another one neighboring to it.

Electromigration is actually not a function of current, but a function of current density [28]. It is also accelerated by elevated temperature. Thus, electromigration is easily observed in metal lines that are subjected to high current densities at high temperature over time [28]. There are two major driving factors that make electromigration happen:

(i) The direct effect of the electric field on the charged atoms or ions of the metal.

(ii) Frictional force or momentum exchange between the electrons and metal ions.

The total driving force is the sum of the effects of these two factors [30].

In Al films, the dominant mechanism of atomic migration is along grain boundaries and surfaces. Lattice mismatches (such as those between adjacent large and small grains or when three grain boundaries meet) can create grain boundary interconnections that provide shorter paths for the atoms, enabling the latter to move faster through the film [30].

Another important thing to note that how grain structures affect electromigration failure rates. Electromigration failure rates decrease with decreasing line widths, but up to a certain point only. It is obvious that a wider wire results in smaller current density, so the possibility of electromigration is less than the narrower wires Also, the metal grain size has a influence on electromigration; the smaller grains, the more grain boundaries and the higher likelihood of electromigration effects [30]. However, if you reduce wire width to below the average grain size of the wire material, the resistance to electromigration increases, despite an increase in current density [30]. This clear contradiction is caused by the position of the grain boundaries, which in such narrow wires as in a bamboo structure lie perpendicular to the width of the whole wire. Because the grain boundaries in these so-called 'bamboo structures' are at right angles

to the current, the boundary diffusion factor is excluded, and material transport is correspondingly reduced [30].

However, the maximum wire width for a bamboo structure is usually too narrow for large-magnitude currents in analog circuits or for power supply lines. In these circumstances, slotted wires are often used, whereby rectangular holes are carved in the wires [30]. Here, the widths of the individual metal structures in between the slots lie within the area of a bamboo structure, while the resulting total width of all the metal structures meets power requirements [30]. There is also a critical lower limit for the length of the metal line that allows electromigration to happen. It is known as the Blech length, any metal line having a length below this limit will not fail by electromigration. Thus, the Blech length should be considered while testing structures for electromigration.

The effect of temperature on electromigration becomes important only when a void has started to form. Prior to any void formation, the metal can still be under uniform thermal distribution. Once a void forms, however, the current density at the section where the void is present increases as a result of the reduced cross-sectional area of the conductor, leading to current crowding around the void [30]. The higher current density around the void cause localized heating and therefore it accelerate the growth of the void, which again increases the current density [30]. The cycle continues until the void becomes large enough to cause the metal line to fuse open as shown in Figure 2.11 [31]. Electromigration failure takes time to develop, and is therefore very difficult to detect until it happens. The best solution would be to design more robust circuits considering this phenomenon.

At last, electromigration can be prevented by

(i) Limiting the current densities in all metal lines.

(ii) Increasing the grain sizes of the metal lines.

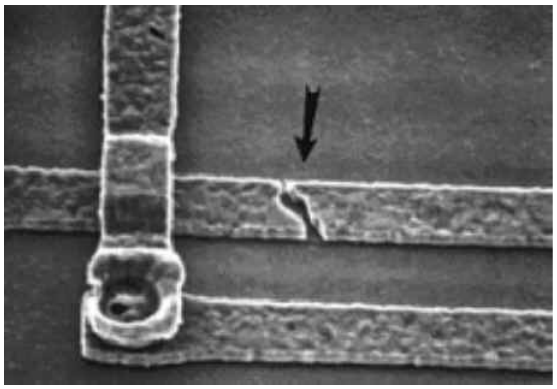

Figure 2.11. A SEM photo that capture the void causing fuse open due to electromigration [31].

(iii) Good selection and deposition of the passivation or thin films placed over the metal lines in order to limit extrusions caused by electromigration.

2.4. Time Dependent Dielectric Breakdown

Time-dependent gate oxide breakdown (or time-dependent dielectric breakdown, TDDB) is a failure mechanism in MOSFETs, when the gate oxide breaks down as a result of long-time application of relatively low electric field (as opposite to immediate breakdown, which is caused by strong electric field). The breakdown is caused by formation of a conducting path through the gate oxide to the substrate due to electron tunneling current, when MOSFETs are operated close to or beyond their specified operating voltages. Defects in the gate oxide are usually called traps; they are called traps because the degraded oxide can capture charges [32]. Traps are generally neutral, but quickly become positively charged near the anode, and negatively charged near the cathode [32].

Gate-oxide breakdown begins when the traps start to form in the gate-oxide. At the beginning, the number of traps is very low and conduction does not occur as shown in Figure 2.12 but as the number of traps increases, they start to create a conduction path [33]. Once these traps form a conduction path from the gate to the channel,

and breakdown shown in Figure 2.13 occurs [33]. This type of breakdown is called Soft Breakdown (SBD). Once there is conduction, new traps are generated by thermal damage, which allows increased conductance as depicted in Figure 2.14 [34]. The cycle of conduction causes excessive heat that results thermal runaway and finally to a lateral propagation of the breakdown spot [34, 35]. The Silicon within the breakdown place starts to melt, and Oxygen gets released, and a silicon wire is formed in the breakdown region [34]. This type of breakdown is called Hard Breakdown (HBD) as shown in Figure 2.15 [36].

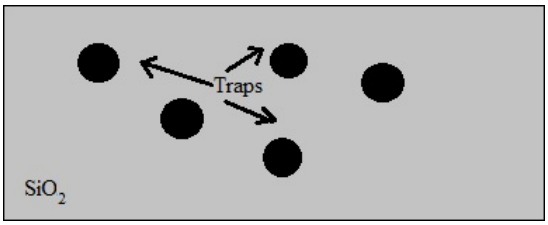

Figure 2.12. The beginning of oxide breakdown.

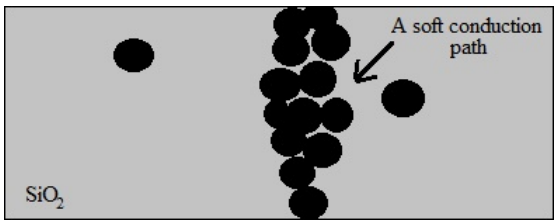

Figure 2.13. Soft breakdown of gate-oxide.

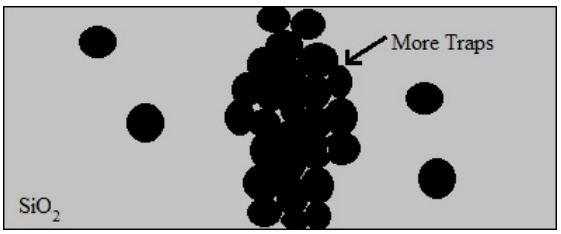

Figure 2.14. Increased traps in gate-oxide.

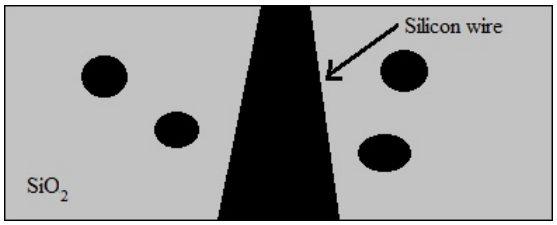

Figure 2.15. Hard breakdown of gate-oxide.

2.4.1. Soft Breakdown of Gate Oxide

Soft breakdown generally does not affect the performance of the transistor, except the increased leakage current of transistor's off state [36]. With technologies having thinner t_{ox} values, the gate tunneling leakage is quite large so that any increase in the gate current due to SBD in the transistor's on state may be not important [36]. However, when the transistor is off, and if SBD occurs near the drain there is an increase in Gate-Induced Drain Leakage (GIDL) of five orders of magnitude [37]. This increase in GIDL is due to the negative charge trapping in the oxide over the overlap region. SBD at other locations of the gate do not have any important effect on the operation of the transistor. Also, long-channel transistors are less affected by the SBD, due to the fact that the drain extension forms much smaller percentage of the total transistor length [36]. SBD affects circuit performance for transistors with low W/L. Since the gate area is very small, the SBD region can compose a considerable portion of the gate area[38]. Under such circumstance the transconductance, g_m of the transistor may drop by 50% and the saturation current fall to 30% of it's original value [38].

2.4.2. Hard Breakdown of Gate Oxide

A current path forms from the gate to the channel after HBD has occurred. The current path is generally symbolized by a gate post-breakdown resistance defined as $R_g = V_g/I_g$ [39]. I_g is the current through the gate. Thus modeling of the effects of HBD gains important to be able to find R_g. The dependence of R_g on the position of the breakdown along the length of the transistor has been pointed out in [39]. For

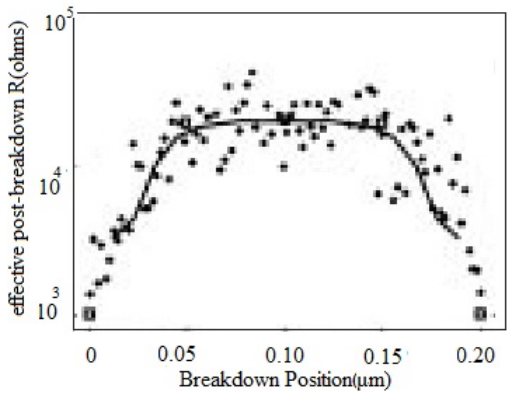

Figure 2.16. Post-breakdown resistance versus the position of the breakdown [38].

a $0,20$ μm long transistor, the post-breakdown resistance versus the position of the breakdown is shown in Figure 2.16 [39]. In the areas where the breakdown occurs around the source and drain extensions, R_{g} decreases linearly [39].

On the other hand, if the breakdown occurs over the channel, R_{g} is relatively constant [39]. The linear increase in R_{g} around the source/drain extensions can be illustrated by the resistance of the length of the n-doped region in the extension where the breakdown happened [39]. When the breakdown occurs around the channel, it is as if current is injected from the gate through the breakdown path into the channel which then continues to the drain and the source. Considering the magnitude of the current after HBD, [40] shows that after HBD near the source or drain, there is an increase of two orders of magnitude when the transistor is on, and an increase of six orders of magnitude when the gate voltage is near zero Volts. The specific increase in current depends on many factors including the size of the transistor, and the size and location of the breakdown [40].

3. MODELING OF FAILURE MECHANISMS

3.1. Motivation

Some physical mechanisms causing reliability issues in CMOS circuits were discussed in the previous chapter. However, this physical point of view is not sufficient to analyze aging phenomena and to make circuits robust to aging. It is obvious that modeling the aging mechanism is necessary to understand the problem analytically and create solutions before the realization of these performance faults. In addition, mathematics science is always used to clarify the physical events, so both sciences cannot be considered independently. In this context, modeling of device degradation ought to be a translation of the understanding of the physical mechanisms leading to degradation of device parameters. There are a lot of different models developed for each mechanism, but the most known, useful, and accurate models will be mentioned and explained in this chapter.

3.2. Hot Carrier Injection Modeling

HCI degradation occurs mostly due to interface trap generation and electron trapping in the gate oxide [16, 41, 42]. Many models for how hot carriers generate interface traps have been proposed [41]. It is probable that recombination of electrons with trapped holes generate interface traps, especially since bulk oxide electron traps can also be generated by this recombination [42]. Moreover, energetic electrons can break $Si-H$ bonds at the Si/SiO_2 interface and generate interface traps [16]. As a result of all of these events, there are some parameter shifts in the device parameters such as carrier mobility and threshold voltage.

$$\frac{d\Delta}{dt} = DG(\Delta)\left(\frac{I_{\mathrm{d}}H}{W}\right)exp(-\phi_{\mathrm{it}}/kT_{\mathrm{c}}) \tag{3.1}$$

Assuming that the rate of device degradation, $d\Delta/dt$, where Δ is ΔI_{d} or ΔV_{th} is proportional to the density of hot electrons having energy larger than some critical energy,

ϕ_{it}, for device damage (through either charge trapping or interface trap generation). W is the MOSFET width, where I_{d}/W represents the flow rate of electrons. $DG(\Delta)$ represents the dependence of the degradation rate on existing damage. For example, $d\Delta/d_{\mathrm{t}}$ may decrease with increasing Δ due to the depletion of breakable hydrogen silicon bonds, or a vertical field repelling hot electrons from the interface [43], or even a change in E_{m}, that reduces T_{c} [44].

Similarly, the substrate current due to impact ionization has been shown as [16]

$$I_{\mathrm{sub}} \propto I_{\mathrm{d}} exp(-\phi_{\mathrm{i}}/kT_{\mathrm{c}}) \tag{3.2}$$

where ϕ_{i} is a critical energy for impact ionization. If both equations are combined

$$d\Delta/dt = HG(\Delta)\left(\frac{I_{\mathrm{d}}H}{W}\right)\left(\frac{I_{\mathrm{sub}}}{I_{\mathrm{d}}}\right)^{\phi_{\mathrm{it}}/\phi_{\mathrm{i}}} \tag{3.3}$$

where H and D are constants in Equation 3.1 and 3.3 [45].

$$\int \frac{d\Delta}{G(\Delta)} \equiv F(\Delta) = \int \left(\frac{I_{\mathrm{d}}H}{W}\right)\left(\frac{I_{\mathrm{sub}}}{I_{\mathrm{d}}}\right)^{\phi_{\mathrm{it}}/\phi_{\mathrm{i}}} dt \tag{3.4}$$

$$\Delta = f\left[\int \left(\frac{I_{\mathrm{d}}H}{W}\right)\left(\frac{I_{\mathrm{sub}}}{I_{\mathrm{d}}}\right)^{\phi_{\mathrm{it}}/\phi_{\mathrm{i}}} dt\right] \tag{3.5}$$

Where f is the inverse of F (i.e. $y = f(x)$ if $x = F(y)$) [45]. Empirically, $f(x) \approx x^{\mathrm{n}}$. We call the integral in Equation 3.5 the 'age' of the transistor. For a given waveform $V_{\mathrm{s}}(t), V_{\mathrm{d}}(t)$, and $V_{\mathrm{g}}(t)$, the current $I_{\mathrm{d}}(t)$ is known. Also I_{sub} is known as [45]

$$I_{\mathrm{sub}} = A(V_{\mathrm{ds}} - V_{\mathrm{dsat}})I_{\mathrm{d}} exp(-B/V_{\mathrm{d}} - V_{\mathrm{dsat}}) \tag{3.6}$$

A and B, as well as the ratio of $\phi_{\mathrm{it}}/\phi_{\mathrm{i}}$ and the function f, are extracted from measured data for a given IC technology [46]. The remaining step before using the simulator is

to extract the MOSFET model parameters of the IC technology on the fresh MOSFET (age=0) and after DC stress under known conditions such as known $I_{\mathrm{d}}, I_{\mathrm{sub}}$ and stress time.

Since we know that the threshold voltage, mobility, transconductance and drain current shifts have a direct relationship to the amount of degradation has occurred from [16, 47, 48] this degradation can be expressed as [49]

$$Degradation \propto A.t^{\mathrm{n}} = \left[\frac{I_{\mathrm{d}}}{WH}\left(\frac{I_{\mathrm{sub}}}{I_{\mathrm{d}}}\right)^{\mathrm{m}}\right]^{\mathrm{n}} t^{\mathrm{n}} \tag{3.7}$$

Here H $(B/Degradation_{\mathrm{f}})$ was used rather than B to eliminate the dependence of degradation parameters on the criteria chosen to define device lifetime($t = \tau$=lifetime when $Degradation = Degradation_{\mathrm{f}}$) [49]. In this context

$$Degradation \propto Age^{n} \; where \; Age = \left[\frac{I_{\mathrm{d}}}{WH}\left(\frac{I_{\mathrm{sub}}}{I_{\mathrm{d}}}\right)^{\mathrm{m}}\right] t \tag{3.8}$$

To calculate the age of each device at a user-specified time T_{age}, it is assumed that circuit behavior is periodic with the period equal to length T of the SPICE analysis [49]. The age that each device would then have at T_{age} becomes

$$Age(T_{\mathrm{age}}) = Age(T)\left(\frac{T_{\mathrm{age}}}{T}\right) \tag{3.9}$$

An easier and more understandable model is given in the following equations including both under AC and DC stress for NMOS devices.

$$\Delta V_{\mathrm{th}} = \frac{q}{C_{\mathrm{ox}}}\Delta N_{\mathrm{it}} \text{ and } \; \mu = \frac{1}{(1+\alpha\Delta N_{\mathrm{it}})^{\mathrm{m}}}\,\mu_{\mathrm{eff}} \; (\alpha = 5 \text{ and } m = 1, 6) \tag{3.10}$$

where ΔN_{it} is density of created interface traps, C_{ox} is oxide capacitance.

For DC stress

$$\Delta N_{\mathrm{it}} = C_1 \left(\frac{I_{\mathrm{inj}}}{W} t \right)^{\mathrm{n}} \tag{3.11}$$

where I_{inj} is current injected into oxide and C_1 is parameter in lifetime model as function of V_{ds} and L_{eff}

$$I_{\mathrm{inj}} = C_2 I_{\mathrm{d}} e^{\left[\frac{-\phi_{\mathrm{ib}}}{q \lambda_{\mathrm{m}} E_{\mathrm{m}}} \right]} \tag{3.12}$$

ϕ_{ib} is total energy barrier, E_{m} is lateral electric-field peak and expressed as

$$E_{\mathrm{m}} = \sqrt{\left(\frac{V_{\mathrm{ds}} - V_{\mathrm{dsat}}}{\ell} \right)^2 + E_{\mathrm{c}}^2} \approx \frac{V_{\mathrm{ds}}}{\ell} \tag{3.13}$$

so ΔN_{it} can be expressed clearly by

$$\Delta N_{\mathrm{it}} = C_1 C_2 \left(\frac{I_{\mathrm{d}} e^{\left[\frac{-\phi_{\mathrm{ib}} \ell}{q \lambda_{\mathrm{m}} V_{\mathrm{ds}}} \right]}}{W} t \right)^{\mathrm{n}} \tag{3.14}$$

In order to derive a relationship for an AC stress on the drain, the assumption that HCI effect in NMOS may be approximately treated as a superposition of DC effects [50]. Intrinsic transient effects in the generation and injection of hot electrons and holes can be neglected for device operation frequencies [50]. In the following, it is assumed that interface trap generation ΔN_{it} is the major mechanism; $V_{\mathrm{gs}}(t)$ is assumed around max $I_{\mathrm{sub}}(V_{\mathrm{ds}}(t))$. Electron and hole trapping is not accounted for, as well as the DC sequence-effects due to hole/electron trapping and neutral electron traps [51, 52] . For the model derivation, the assumption that there are no transient effects in HCI degradation [50]. The damage-creation-kinetics depends on the pre-existing damage in the AC conditions like in the DC conditions. Using these assumptions, the total amount of accumulated damage may be expressed as

$$\Delta N_{\mathrm{it}} = C_1 \int_0^{\mathrm{t}} \left(\frac{I_{\mathrm{inj}}}{W} t \right)^{\mathrm{n}} dt \tag{3.15}$$

so the total interface density can be expressed clearly as

$$\Delta N_{\mathrm{it}} = C_1 C_2 \int_0^{\mathrm{t}} \left(\frac{I_{\mathrm{d}} e^{\left[\frac{-\phi_{\mathrm{ib}}\ell}{q\lambda_{\mathrm{m}} V_{\mathrm{ds}}}\right]}}{W} t \right)^{\mathrm{n}} dt \tag{3.16}$$

Consequently; HCI manifests itself as an increase in threshold voltage and the degradation of the carrier mobility for the NMOS transistor.

3.3. Negative Bias Temperature Instability Modeling

NBTI can be explained as the consequence of trap generation at Si/SiO_2 interface in negatively biased PMOS transistors at elevated temperatures. Absence of the stress can recover some of the interface traps resulting in a partial relaxation [53]. In order to transfer the effect of NBTI from the physics to mathematics, a number of models have been developed in literature. Since all the models can not be covered in this section, the most known models will be given to understand this physical event from the mathematics window.

The obvious consequence of the NBTI on PMOS transistor is the shift (increase) in the threshold voltage and it is directly proportional to interface density as modeled in [54, 55, 56].

$$\Delta V_{\mathrm{th}} = q\frac{N_{\mathrm{it}}}{C_{\mathrm{ox}}} \qquad C_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} \tag{3.17}$$

For a PMOS transistor, there are two phases of NBTI depending on its biasing condition. These two phases are depicted in Figure 3.1. Assume that the substrate is biased at V_{dd}. In the first phase, V_{gs} equals to $-V_{\mathrm{dd}}$ since the gate voltage is zero and thus positive interface traps are accumulated at the gate side over time due to H diffusing [53]. This stage is called as "Stress" and static stress of the PMOS occurred in this phase only as mentioned above. In the second phase, when gate voltage is equal to V_{dd}, V_{gs} goes to zero thus new holes are not present in the channel and instead of the generation of new interface traps, H diffuses back and anneals the broken $Si-H$ [53].

As a result, NBTI degradation is recovered due to the fact that number of interface traps are reduced. This stage is called as "Recovery" and has an important role for the circuits which includes dynamic switching at the PMOS devices.

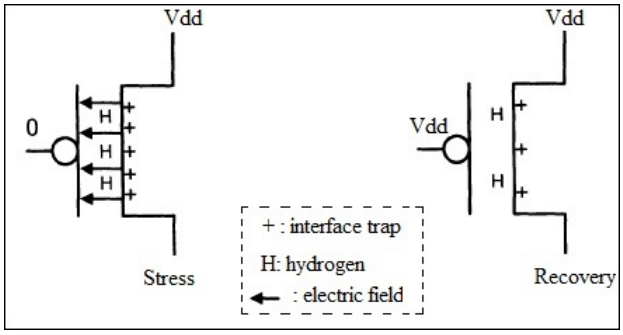

Figure 3.1. Two phases of PMOS NBTI ($V_{\mathrm{b}} = V_{\mathrm{dd}}$).

Briefly, there are two different mechanisms for the NBTI phenomenon if the stress quality is considered. Static stress occurs when a constant negative stress is applied to the gate of the PMOS and there is no relaxation, and degradation will be permanent. On the other side, if an AC signal is applied to the gate of the PMOS, the NBTI part should be examined in two stages: Stress and Recovery. In the light of this concept, two different models have been developed to explain the NBTI phenomenon.

3.3.1. Static NBTI

Interface traps are generated by the reaction to break $Si-H$ bonds and H atoms leave the SiO_2 interface through diffusion at PMOS under stress conditions. This can be described by reaction-diffusion process model [57]. The interface traps equation is

$$\Delta N_{\mathrm{it}} = \left(K^2 t^{1/2} + c^{1/2n}\right)^{2n} \tag{3.18}$$

where c is the number of interface traps at the beginning, n which is the signature of neutral diffusion, is about 0.25 for H diffusion model and 1/6 for H_2 [56, 57]. The equation can be calculated both H dominated diffusion and H_2 dominated diffusion

process by changing the n exponent.

Accounting for the reaction of breaking $Si - H$ bonds, the generation rate of interface traps, K, is linearly proportional to the hole density and exponentially dependent on temperature (T) and the electric field ($E_{\rm ox}$) [56, 55] shown as

$$K \propto \sqrt{C_{\rm ox}(V_{\rm gs} - V_{\rm th})} exp(E_{\rm ox}/E_0) exp(-E_{\rm a}/kT) \quad \text{where} \;\; V_{\rm ds} = 0 \tag{3.19}$$

$E_{\rm ox} = (V_{\rm gs} - V_{\rm th})/T_{\rm ox}$ and k is the Boltzmann constant at the above equation. E_0 and $E_{\rm a}$ are technology independent characteristics of the reaction [53]. The above equation is valid for $V_{\rm ds} = 0\ V$. If $V_{\rm ds}$ does not equal to zero (due to subthreshold leakage), $E_{\rm ox}$ at the drain is smaller than the source, which reduce NBTI stress [53]. The dependence of K can be expressed as

$$K \propto \frac{1 - V_{\rm ds}}{\alpha(V_{\rm gs} - V_{\rm th})} \tag{3.20}$$

3.3.2. Dynamic NBTI

Dynamic NBTI corresponds to the case where the PMOS transistor undergoes alternate stress ($V_{\rm gs} = -V_{\rm dd}$) and recovery ($V_{\rm gs} = V_{\rm dd}$) periods. Due to widely different diffusivity of H_2 in the oxide and polysilicon [58], the recovery becomes a 2-step process, with fast recovery driven by the H_2 in oxide followed by slow recovery of H_2 by back diffusion from polysilicon [58]. The gate voltage alternates between $-V_{\rm dd}$ and $V_{\rm dd}$. The PMOS is under stress while $V_{\rm g} = -V_{\rm dd}$ and interface traps are generated. However, during the switching of the gate from $-V_{\rm dd}$ to $V_{\rm dd}$, the stress is removed and the interface traps are annealed. This process depends on the diffusion of neutral H and thus has no field dependence [24]. Presuming the relaxation occurs at the time $t = t_0$ with $\Delta N_{\rm it} = \Delta N_{\rm it0}$, the change of interface traps can be modeled as [53]

$$\Delta N_{\rm it} = \Delta N_{\rm it0}[1 - \sqrt{\eta(t - t_0)/t}] \tag{3.21}$$

Modeling dynamic NBTI is very difficult due to complexity of stress and recovery process. Without losing generality, the impact of NBTI can be modeled as a constant δ [53].

$$Stress : \Delta N_{\mathrm{it}} = \sqrt{K^2(t-t_0)^{1/2} + \Delta N_{\mathrm{it0}}^2} + \delta \tag{3.22}$$

$$Recovery : \Delta N_{\mathrm{it}} = (\Delta N_{\mathrm{it}} - \delta)\left[1 - \sqrt{\eta(t-t_0)/t}\right] \tag{3.23}$$

If the the all of above equations are covered, an NBTI model shown in Table 3.1 can be obtained which provides us a solid basis for simulation studies and tool development.

Table 3.1. Summary of NBTI model.

Condition	ΔV_{th} under NBTI
Stress	$\sqrt{{K_{\mathrm{v}}}^2(t-t_0)^{0,5} + {\Delta V_{\mathrm{th0}}}^2} + \delta_{\mathrm{v}}$
Recovery	$(\Delta V_{\mathrm{th0}} - \delta_{\mathrm{v}})\left[1 - \sqrt{\eta(t-t_0)/t}\right]$
K_{v}	$At_{\mathrm{ox}}\sqrt{C_{\mathrm{ox}}(V_{\mathrm{gs}} - V_{\mathrm{th}})}\left[1 - V_{\mathrm{ds}}/\alpha(V_{\mathrm{gs}} - V_{\mathrm{th}})\right] exp(E_{\mathrm{ox}}/E_0) exp(-E_{\mathrm{c}}/kT)$

3.4. Electromigration Modeling

Electromigration is the movement of metal atoms in the direction of electron flow due to momentum transfer from electrons to the metal ions under thermal and voltage stresses. Over time, the resistance of the metal line may be changed. There are a number of electromigration lifetime models ranging from simple one dimensional models to more complex models. However, Black's formula [28] provides a useful insight into electromigration failure modeling. According to Black's formula, MTTF is inversely proportional to the rate of mass transport [59].

$$MTTF \propto \frac{1}{R_{\mathrm{m}}} \tag{3.24}$$

The mass transport, R_{m}, is proportional to the momentum transfer between thermally activated ions and conducting electrons [60].

$$MTTF \propto n_{\mathrm{e}},\ \Delta p N_{\mathrm{a}} \tag{3.25}$$

Where N_{a} is the density of thermally activated ions, Δp is the momentum transfer between electrons and metal atoms, and n_{e} is the density of conducting electrons. Moreover, both electron density and momentum transfer are directly proportional to the current density, j.

$$n_{\mathrm{e}} \propto j \quad \Delta p \propto \ j \tag{3.26}$$

N_{a} can be expressed as

$$N_{\mathrm{a}} \propto exp\left(\frac{E_{\mathrm{a}}}{kT}\right) \tag{3.27}$$

Finally mean time to failure can be modeled as

$$MTTF = \frac{A}{j^n} exp\left(\frac{E_{\mathrm{a}}}{kT}\right) \tag{3.28}$$

where A is a material constant dependent on structural and geometric properties of the conductor, n is a current exponent factor, J is the current density, E_{a} is the activation energy, k is the Boltzmann constant, and T is the absolute junction (chip) temperature. The activation energy for Al-Cu alloy is in the range of 0.76 to 0.86 eV [61], and the activation energy for Cu interconnections can vary widely from 0.7- to 1.0 eV. The lifetime of interconnects is decreased with the reduction of line width [62]. The accuracy of lifetime prediction is strongly dependent on the accuracy of the junction temperature measurement during the acceleration testing [63].

Furthermore, there are independent limits set for the average current density J_{avg} (under DC or pulsed DC conditions), the rms current J_{rms} (under Joule self-

heating stress) and the peak current J_{peak} (under high current pulse stress). While copper is well known for having better resistance against electromigration due to significantly higher activation energy and higher conductivity, continued scaling of wires and increased power density will cause electromigration effects to worsen due to higher current densities and Joule self-heating.

The most interesting fact is that the failure time tends to be proportional to the inverse square of the current density, even though mass transport due to electromigration had been shown to be linearly dependent on current density [60]. A recent work discussed the application of the modified Equation 3.28 and concluded that it may lead to significant errors in the lifetime extrapolation. These errors stem from the assumption that the fitting parameters A, E_{a}, and n obtained from the accelerated tests can be directly applied for the lifetime extrapolation [60]. As Lloyd [59] shows, the experimental measurement of the above parameters does not consider important additional temperature and also pre-existing stress dependencies, which yields incorrect parameter values and, consequently, lifetime extrapolation [60].

Failure mechanism based on the generation of massive damage occurs after the damage should first be nucleated and then it should grow to the point of failure [59]. If each of these two processes is driven by the same force, in this case electromigration, but offer different kinetics, the partition of the failure time would not only be a single function of the force, but since the failure time is the sum of two functions, would change according to the stress conditions [59]. Therefore, the failure time would follow

$$t_{50} = t_{\text{nuc}} + t_{\text{g}} = \left[\frac{AkT}{j} + \frac{B(T)}{j^2}\right] exp\left(\frac{E_{\text{a}}}{kT}\right) \tag{3.29}$$

where t_{nuc} and t_g are time periods which denote nucleation and growing process, respectively. A and B are constants including geometric information, such as the size of the void required for failure. $B(T)$ also has a temperature dependence that depends on which failure model is chosen. According to the above equation, the relative contributions of nucleation and growth will change as a function of the current

density regardless of the any values of A and B. At higher current densities the time to failure will proportionately be more related to growth than the nucleated one [59].

3.5. Time Dependent Dielectric Breakdown Modeling

This phenomenon occurs due to several mechanisms. One of them is dielectric breakdown where dielectric is typically oxide for CMOS technology. Oxide breakdown can be classified into two types; namely, intrinsic and extrinsic. The extrinsic breakdown happens in defects in the oxide and typically appears during the relatively short time burn-in testing. As far as aging of CMOS circuits is considered, the main subject will be intrinsic breakdown.

E and $1/E$ models are widely used for intrinsic gate-oxide reliability predictions for oxide thicknesses greater than 50Å. Both models have a physical basis. The E model is expressed as, [64]

$$t = Aexp(\gamma E)exp\left(\frac{E_{\mathrm{a}}}{kT_{\mathrm{j}}}\right) \tag{3.30}$$

where t is the time to breakdown, A is a constant for a given technology, γ is the field acceleration parameter, E is the oxide field, and E_{a} is the thermal activation energy. This model is based on a thermochemical foundation. Based on the E-model, increasing electric field across the gate oxide will decrease the time to break down [64]. On the other hand, if we assume that breakdown is a current-driven process, thus t should be dependent on the $1/E$ due to FN conduction, and it is called as '$1/E$ model' [64].

$$t = \tau_0 exp\left(\frac{G}{E}\right) exp\left(\frac{E_{\mathrm{a}}}{kT_{\mathrm{j}}}\right) \tag{3.31}$$

where τ_0 and G are constants. The $1/E$ model represents that the dielectric does not degrade in the absence of electric field. The $1/E$ model ignores important thermal/diffusional processes that are known to degrade all materials over time, even in

the absence of an electric field [64]. Both models are derived from physical foundations, and both reflect an exponential reduction of lifetime with increasing electric field.

Experimental measurements of oxides in modern devices show that these two conventional models cannot provide the necessary accuracy leading to the proposal of a new TDBB model [65, 66]. Experiments show that the generation rate of Stress-Induced Leakage Current (SILC) and charge to breakdown (q_{bd}) in ultra thin oxides is controlled by the gate voltage rather than the electric field.

$$T_{\mathrm{BD}} = T_0 exp\left[\gamma(\alpha T_{\mathrm{ox}} + \frac{E_{\mathrm{a}}}{kT_{\mathrm{j}}} - V_{\mathrm{g}})\right] \tag{3.32}$$

where γ is the acceleration factor, T_{ox}, the oxide thickness acceleration factor is constant for a given technology, and T_0 is also a constant for a given technology, and T_{j} is the average junction temperature [64].

To explain the mechanism in extremely thin oxides, researchers proposed two different approaches, the anode hole injection model [67, 68], and the electron trap generation model [69]. According to the former, injected electrons generate holes at the anode that can tunnel back into the oxide. Intrinsic breakdown occurs when a critical hole concentration Q_{BD} is reached. The latter model claims that a critical density of electron traps generated during stress is required to trigger oxide breakdown. Based on this model, the breakdown event is presented as the formation of a conductive path of traps connecting the anode to the cathode interface. A newer model relating these two hypotheses allows us to calculate the critical density N_{crit} of defects per unit area at breakdown conditions as a function of t_{ox} as,

$$N_{\mathrm{crit}}^{\mathrm{BD}} = \frac{t_{\mathrm{ox}}}{{\alpha_0}^3} exp\left[-\frac{\alpha_0}{t_{\mathrm{ox}}} ln\left(\frac{A_{\mathrm{ox}}}{{\alpha_0}^2}\right)\right] \tag{3.33}$$

where α_0 is the lattice constant of a cubic structure in the oxide bulk and A_{ox} is the

oxide area. The time to breakdown can then be written as,

$$T_{BD} = \frac{qN_{\text{crit}}^{\text{BD}}}{P_{\text{g}} J_{\text{g}}} \tag{3.34}$$

where J_{g} is the tunneling current across the oxide and P_{g} is the injected electron density. Note that, this model is useful for transistors with very thin oxide where there is a considerable leakage current, and does not contain the gate voltage or electric fields. This model is in fact more accurate since it uses the gate current.

4. AN ANALOG DESIGN: 5 GHz CMOS DIFFERENTIAL CROSS-COUPLED LC OSCILLATOR

4.1. Motivation

In the previous chapters, physical mechanisms of aging were covered and their mathematical models were examined.In this chapter, an analog circuit will be used to demonstrate the aging effects. Thus, several MOS differential cross-coupled LC oscillators were designed because they are nonlinear circuits and even small changes in the oscillator properties may cause great deviations in the phase noise response of the circuit. It is also a well known fact that aging causes parameter degradation in CMOS circuits, so oscillator circuit will be a good example to show the aging effects on the analog circuits. As a result, three different CMOS Differential Cross-Coupled LC Oscillator(NMOS, PMOS, and CMOS) were designed and their phase noise analyzes were performed using both calculation and simulation steps as a preliminary study for the following chapter.

4.2. Introduction

CMOS LC oscillators are widely used in high performance PLLs and frequency synthesizers due to their relatively good phase noise and ease of design [70, 71, 72, 73, 74, 75]. There are lots of diverse architectures of differential pair LC oscillators (only NMOS, only PMOS, CMOS and Quadrature structure etc.). However, oscillators are nonlinear circuits and their phase noises are quite difficult to model. There are a number of phase noise models in the literature [76, 77, 78], but Abidi's phase noise model [76] was used in this study because it is quite accurate and easy to understand. In this chapter, three different types Differential Cross-Coupled LC Oscillators structures (NMOS, PMOS, and CMOS) whose oscillation frequency is 5 GHz have been designed using $0,13$ μm technology, their phase noise analyzes were performed, and their phase noise performances are discussed along with a comparison table including

both simulation and calculation results at the end of the chapter.

4.2.1. Methodology

An oscillator circuit must satisfy the Barkhausen criterion in order to sustain oscillation. For a positive feedback system, oscillation occurs when the loop gain has a zero phase shift with a magnitude of one at the oscillation frequency [70].

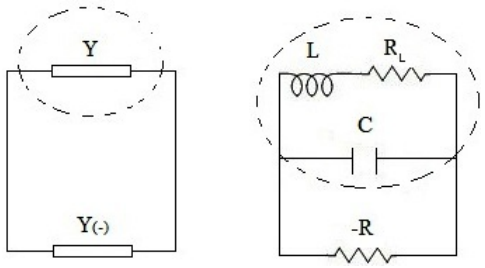

Figure 4.1. A general oscillator model and LC tank oscillator.

Figure 4.1 shows an oscillator model, where Y is the resonator admittance and $Y_{(-)}$ denotes a negative admittance which cancels out the energy loses in the resonator.

$$Y = G + jB \qquad Y_{(-)} = G - jB_{(-)} \tag{4.1}$$

To achieve steady-state of an oscillator, the phase condition requires the loop phase shift is zero.

$$B_{-} + B = 0 \tag{4.2}$$

When the oscillator achieves the steady state, phase shift will be zero and the oscillation frequency of oscillator, w_{osc} , is generally assumed to be the resonant frequency of LC pair, w_0 [70].

$$w_{\text{osc}} = w_0 = \frac{1}{\sqrt{LC}} \tag{4.3}$$

In order to design an oscillator, it is obvious that a circuit that produces a negative resistance should be added to the tank circuit to cancel out the resistance arisen from the LC part. Cross-coupled transistors are commonly used to produce a negative resistance in differential LC VCOs. Figure 4.2 is an NMOS cross-coupled pair.

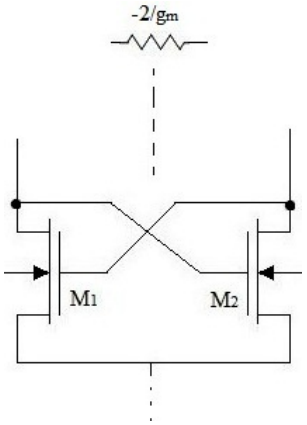

Figure 4.2. Cross-coupled NMOS for negative resistance.

If the LC tank circuit and cross-coupled part is combined, an NMOS LC oscillator circuit presented in Figure 4.3 can be obtained. The NMOS pair produces a negative resistance with value of $-2/g_{\mathrm{m}}$ (g_{m} is the transconductance of MOS) and this value should be equal to R_{p} (the resistance across the resonator circuit) to get oscillation in defined frequency. R_{s} represents the resistance of inductance and Q is the quality factor.

$$R_{\mathrm{p}} = R_{\mathrm{s}}(Q^2 + 1) \tag{4.4}$$

$$R_{\mathrm{s}} = \frac{w_{\mathrm{osc}} L}{Q} \tag{4.5}$$

The assumption was that

$$R_{\mathrm{p}} = \frac{-2}{g_{\mathrm{m}}} \tag{4.6}$$

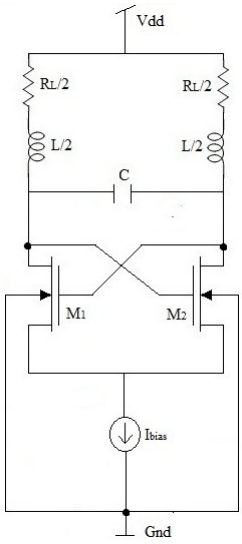

Figure 4.3. NMOS differential cross-coupled LC oscillator.

so that the g_{m} should be appropriately determined to provide us a resistance which is equal to R_{p} value. Equation 4.7 shows that the transconductance of MOS is directly proportional to the current flowing from the drain to the source and turn-on voltage of MOSFET.

$$g_{\mathrm{m}} = \frac{2I_{\mathrm{d}}}{V_{\mathrm{gs}} - V_{\mathrm{th}}} \tag{4.7}$$

and we know the I_d as

$$I_{\mathrm{d}} = \frac{1}{2}\,\mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{gs}} - V_{\mathrm{th}}) \tag{4.8}$$

This parameters are sufficient in order to start oscillator design showed in Figure 4.4. This structure is the well known tail current biased differential LC Oscillator.

In the steady state, the differential pair switches the tail current into LC tank. As a result of the filtering in LC circuit, the square wave of current creates a sinusoidal voltage across the resonator circuit and this voltage drives the differential pair ,thus a sustained oscillation is occurred.

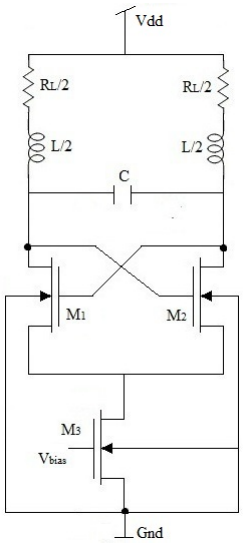

Figure 4.4. Tail current biased differential CMOS LC oscillator.

4.2.2. Calculations

As mentioned above, the oscillation frequency can be calculated by the resonant frequency of tank circuit.

$$w_{\text{osc}} = w_0 = \frac{1}{\sqrt{LC}} \tag{4.9}$$

Oscillation frequency has been determined 5 GHz, so if the f value is substituted at the Equation 4.9, component values are found as

$$LC = 1 \times 10^{-21} \Rightarrow L = 2 \text{ nH} \qquad \text{and} \qquad C = 0,5 \text{ pF} \tag{4.10}$$

Assuming the quality factor of the inductance Q=15, the serial resistance of the inductor can be calculated as

$$R_{\text{s}} = \frac{2\pi 5.10^{9}.2.10^{-9}}{15} \approx 4,2\ \Omega \tag{4.11}$$

Parallel resistance across the resonator circuit is calculated by

$$R_{\mathrm{p}} = 4,2(15^2 + 1) \approx 946\ \Omega \tag{4.12}$$

and the transconductance of MOSFET is calculated as

$$g_{\mathrm{m}} = \frac{2}{946} \approx 2,11\ \mathrm{mS} \tag{4.13}$$

The negative resistance produced by the transistors will have a $2,11$ mS transconductance, thereby, the MOSFET current is calculated by

$$V_{\mathrm{gs}} - V_{\mathrm{th}} \approx 1,2 - 0,44 = 0,76\ \mathrm{V} \quad \text{and} \quad I_{\mathrm{d}} = \frac{2,11.0,76}{2} \approx 0,8\ \mathrm{mA} \tag{4.14}$$

According to results of above equations, dimensions of transistor can be figured out by using the appropriated current value of each MOSFETs.

$$0,810^{-3} = 208.10^{-6}\frac{W}{L}(1,2 - 0,44)^2 \quad \Rightarrow \frac{W}{L} \approx 30 \tag{4.15}$$

As mentioned at the beginning of the part, the technology (130 nm) allows the minimum transistor length $0,12\ \mu$m, so the width of transistor will be

$$L = 0,12\ \mu\mathrm{m} \qquad \text{and} \qquad \mathrm{W} = 3,6\ \mu\mathrm{m} \tag{4.16}$$

4.2.3. Phase Noise in CMOS Differential Cross-Coupled LC Oscillators

Phase noise is defined as the instantaneous change at the oscillator output [79]. This noise is originated from three sources of the oscillator parts: LC resonator, differential pair and tail current part [79]. However, phase noise modeling has become a challenge for designers because of the nonlinearity effects. The first successful idea of the phase noise model has been developed by Leeson [77] and over the years, lots of

studies about phase noise analysis based on Leeson's formula have produced results. Nevertheless, these analyses have not produced accurate prediction of noise because all of them were based on a linear model of an LC resonator in steady-state oscillation and did not include the noise produced by MOSFETs. In this sense, MOSFET non-linearity effects have a crucial role in order to estimate the phase noise response and more recent research have focused on the modeling of the phase noise of MOSFET. A recent work is presented in [76] is easy to use and quite accurate to predict the phase noise in oscillator.

According to [76], the noise sources of an cross-coupled NMOS oscillator can be expressed respectively as

$$L(w_{\mathrm{m}}) = N_1 N_2 \frac{kTR}{V_{\mathrm{o}}^2} \left(\frac{w_0}{2Qw_{\mathrm{m}}} \right)^2 \tag{4.17}$$

In this formula, $N_1 = 2$ denotes the number of loss sources (left and right resonators) and $N_2 = 4$ due to uncorrelated quadrature noise originating at $w_0 + w_{\mathrm{m}}$ contributes to SSB phase noise at offset w_{m} [76].

The phase noise of tail current caused by thermal noise is

$$L(w_{\mathrm{m}}) = \frac{32}{9} \gamma g_m R \frac{kTR}{V_{\mathrm{o}}^2} \left(\frac{w_0}{2Qw_{\mathrm{m}}} \right)^2 \tag{4.18}$$

where γ is the noise factor of a single FET, R is the resonator parallel resistance, V_{o} is the output swing of the differential output [76].

and finally the last term in the phase noise is the differential pair noise is

$$L(w_{\mathrm{m}}) = \frac{32 I_{\mathrm{T}} R \gamma}{\pi V_{\mathrm{o}}} \frac{kTR}{V_{\mathrm{o}}^2} \left(\frac{w_0}{2Qw_{\mathrm{m}}} \right)^2 \tag{4.19}$$

The first and the second term also have been obtained by [78], but the last expression has been derived only by Rael and Abidi [76]. Combination of all of these equations,

Leeson's formula takes the form

$$L(w_{\mathrm{m}}) = \frac{4FkTR}{V_{\mathrm{o}}^2}\left(\frac{w_{\mathrm{o}}}{2Qw_{\mathrm{m}}}\right)^2 \tag{4.20}$$

where F denotes the noise factor. It is obtained by summing the expressions for resonator noise, differential pair noise and tail bias current noise, respectively. Consequently, the differential oscillator noise factor is

$$F = 2 + \frac{8\gamma RI_{\mathrm{t}}}{\pi V_{\mathrm{o}}} + \gamma\frac{8}{9}g_{\mathrm{mbias}}R \tag{4.21}$$

where g_{mbias} is the transconductance of the tail FET. In the light of these two equation, all nonlinear effects have been captured and an accurate phase noise analysis can be obtained.

4.2.4. Design Procedure

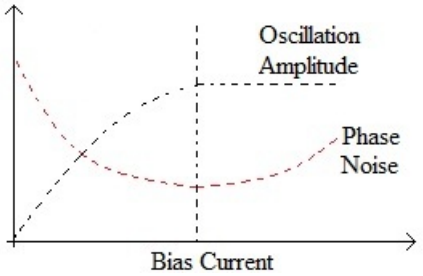

Figure 4.5. Phase Noise vs. Bias Current curve.

All values found in calculation step were used initially at the design step and some simulation results were observed. Then some modifications were carried out based on simulation results. Meanwhile, it should be noted that the tail current and phase noise curve shown in Figure 4.5 should be interpreted correctly to get accurate operating current. Increasing tail current first causes amplitude to rise until limited by supply. Phase noise diminishes with rising amplitude, then worsens due to higher noise factor. As a consequence, the operating point should be chosen at dashed line point.

In the light of this idea, some simulations have been run for different tail current values and the optimal current values have been detected nearly to be 3 mA. All component values are given in Table 4.1 for all oscillator designs.

Table 4.1. Component values of oscillators.

Structure	W/L(Tail)	W/L(Diff.)	R_{bias}	C/L	R_s	V_{bias}	V_{supply}	I_d
	[μm/ μm]	[μm/ μm]	[Ω]	[pF]/[nH]	[Ω]	[V]	[V]	[mA]
NMOS1	—	8/0.12	—	0.45 / 1	2.1	—	1.2	3
NMOS2	60/0.12	8/0.12	—	0.45 / 1	2.1	0.5	1.2	3
NMOS3	60/0.12	8/0.12	240	0.45 / 1	2.1	1.2	1.2	3
PMOS1	—	20/0.12	—	0.45 / 1	2.1	—	1.2	3
PMOS2	60/0.12	20/0.12	—	0.45 / 1	2.1	0.5	1.2	3
PMOS3	60/0.12	20/0.12	240	0.45 / 1	2.1	0.5	1.2	3
CMOS1	—	20-8/0.12	—	0.45 / 2	4.2	—	1.5	1.5
CMOS2	60/0.12	20-8/0.12	—	0.45 / 2	4.2	—	1.5	1.5
CMOS3	60/0.12	20-8/0.12	300	0.45 / 2	4.2	1.5	1.5	1.5

After the determination of component values, different oscillator structures have been designed and optimizations have been done to get a clear oscillation. All oscillator structures are schematically depicted in Figure 4.6, 4.7, and 4.8 ,respectively. Each structure involves three different biasing types: constant bias (a), tail MOS bias (b), and current mirror bias (c). Each oscillator has been renamed in order to make easy to use them at the next parts. These new names can be seen from the explanations of the Figures 4.6, 4.7, and 4.8.

An important difference can be clearly seen from the component values is that the drive current is decreased by 2 times for CMOS structures, because there are two differential parts which produces two negative resistance, so transconductance of transistors should be half of the other oscillators.

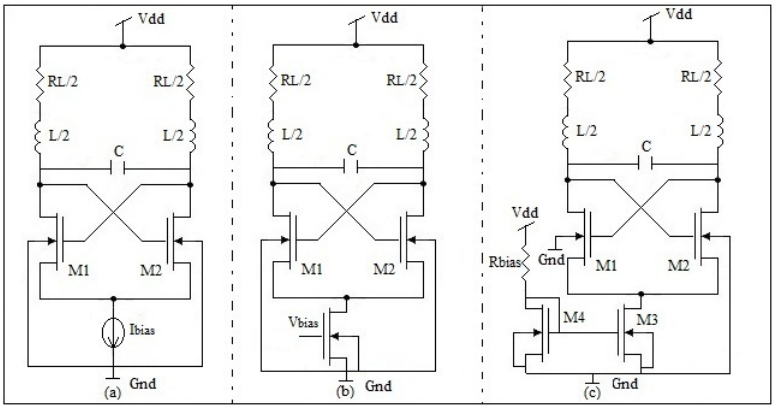

Figure 4.6. NMOS oscillators: (a) NMOS1, (b) NMOS2, (c) NMOS3.

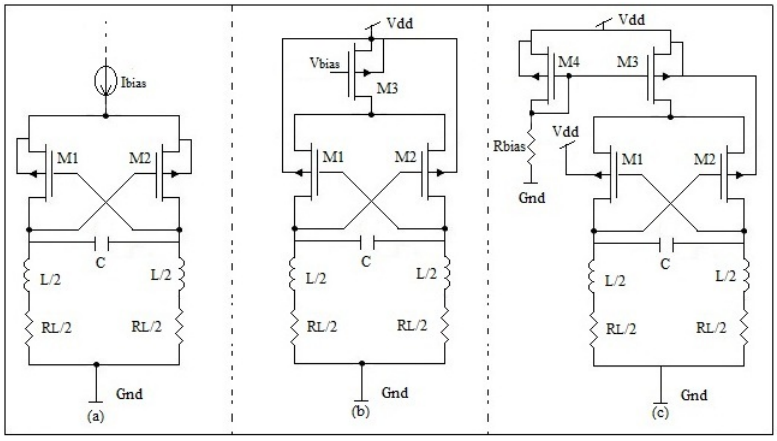

Figure 4.7. PMOS oscillators: (a) PMOS1, (b) PMOS2, (c) PMOS3.

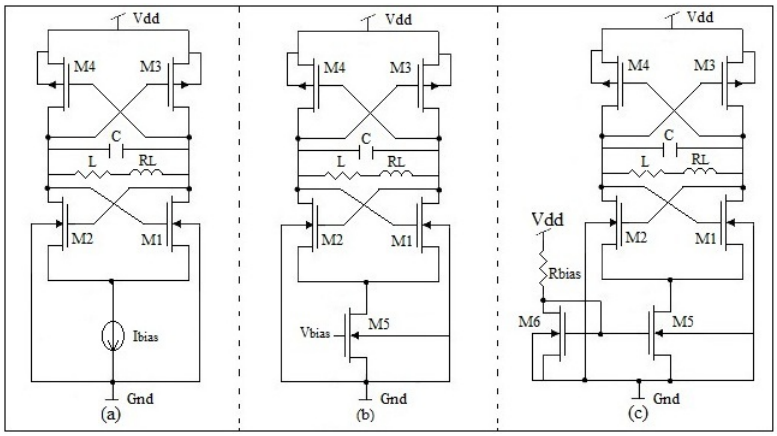

Figure 4.8. CMOS oscillators: (a) CMOS1, (b) CMOS2, (c) CMOS3.

4.2.5. Analyses and Results

Mentor and Eldo have been used during the design process and all simulations have been run by using UMC013 technology model parameters. Phase noise analyses have been calculated using Equation 4.20 and Equation 4.21 and these results are compared to results generated by the eldo simulation. The results of comparison process are given in Table 4.3.

Some parameters have to be assumed as approximated values while the calculation progress. For example; the noise factor, γ, for NMOS has been estimated 1,1 and the quality factor of inductance has been assumed 15. Moreover, the noise equation has to be changed for the CMOS structure for an accurate calculation. For this reason, the noise factor of differential pair is multiplied by 2, thus, Equation 4.21 takes form

$$F = 2 + \frac{8\gamma R I_{\mathrm{t}} 2}{\phi V_{\mathrm{o}}} + \gamma \frac{8}{9} g_{\mathrm{mbias}} R \tag{4.22}$$

Moreover, the formula used for phase noise also has been changed at some calculation steps. For example, the first circuits of all oscillators have not any tail MOS, so the tail noise figure should be taken '0'. Another important point is that, Abidi's formula represents only the NMOS pair noise, but the second and the third oscillators include PMOS devices, thereby, the noise figures should be re-calculated using updated formulas.

Phase noise of all oscillator structures have been calculated by using Equation 4.20, 4.21, and 4.22 and simulated by using Eldo. The oscillator output is shown in Figure 4.9 and the phase noise results at 1MHz offset frequency are given in Table 4.3. According to the results, calculation and simulation results are mostly in agreement with each other, the model used for calculation is quite accurate. According to the phase noise responses, the best phase noise response has been observed in PMOS oscillators, because PMOS transistors are less noisy devices than NMOS devices. On the other hand, NMOS structures are better than the CMOS ones according to their phase noise responses. However, the tail current reduced by 2 times, so the power

consumption is better for CMOS oscillators compared to the others.

The most important result of this part is summarized in Table 4.2. It shows the noise figures of each part of an oscillator for all structures. As seen from the table, the tail noise figure is always dominant for all oscillators. As a result, it can be concluded that aging of tail part devices will degrade the circuit performance at most. Moreover, the differential noise figure includes the drive current and the output voltage terms and these values are directly proportional to the performance of tail devices, so any degradation in tail will alternate the differential noise figure.

Consequently, a brief tutorial including both calculation and simulation parts has been prepared to how to design an CMOS LC oscillator. Furthermore, NMOS, PMOS, and CMOS differential cross-coupled LC oscillators whose frequency is 5 GHz have been designed using 0.13 μm technology and all design procedure has been explained step by step. Basic information about phase noise modeling has been covered and phase noise analyses have been performed for different oscillator structures by using phase noise formulas proposed by Rael and Abidi.

Table 4.2. Phase Noise factors.

Structure	F_{tail}	$F_{resonator}$	$F_{differential}$
NMOS1	0	2	2.815
NMOS2	13.41	2	2.815
NMOS3	13.41	2	2.815
PMOS1	0	2	4.06
PMOS2	8.15	2	4.06
PMOS3	8.15	2	4.06
CMOS1	0	2	2.14
CMOS2	4.97	2	2.14
CMOS3	4.97	2	2.14

Table 4.3. Phase Noise results at 1 MHz offset frequency.

Structure	Calculation[dB]	Simulation[dB]
NMOS1	-124.1	-122.23
NMOS2	-117.6	-117.3
NMOS3	-117.6	-116.24
PMOS1	-125.1	-124.25
PMOS2	-119.3	-119.42
PMOS3	-119.3	-118.52
CMOS1	-118.9	-117.22
CMOS2	-115.4	-114.93
CMOS3	-115.4	-114.35

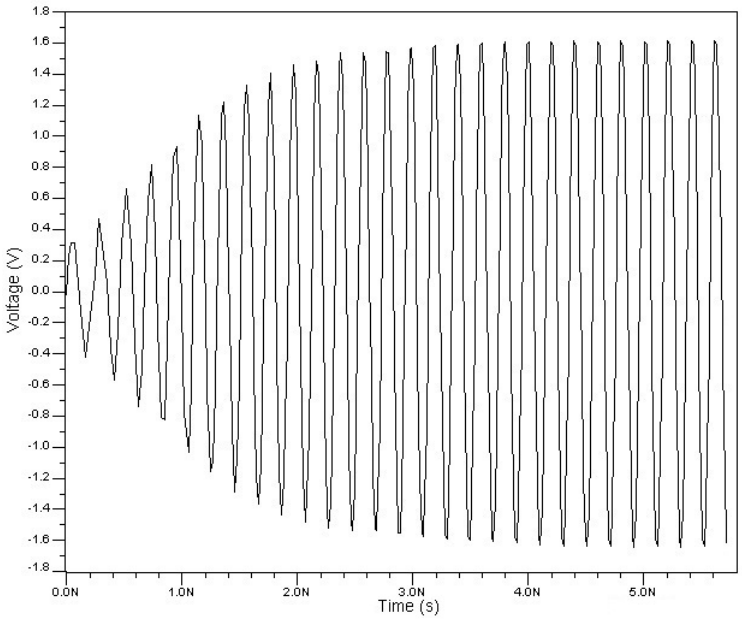

Figure 4.9. Oscillator output: $f_{\text{osc}} = 5$ GHz.

5. AGING ANALYSIS OF OSCILLATOR CIRCUITS

5.1. Introduction

The previous chapters have covered the background for aging analysis of oscillators. Physical mechanisms, reliability modeling, a sample analog design and phase noise analysis have been studied for better understanding of the aging process. Initially, a brief information about the reliability simulation tool which was used for aging simulation will be given. Aging models which were used through both simulation and calculation sections will be presented and finally, simulation and calculation results obtained by both fresh and aged components will be given and results will be discussed.

5.2. A CAD tool for aging simulation: User Defined Reliability Modeling

As mentioned above, Mentor Graphics software was used for all simulation steps. Eldo is a featured simulator tool in Mentor having a lot of specific simulation functions (i.e. post-layout simulation, optimization, reliability simulation etc.). A specific tool of Eldo, User Defined Reliability Tool (UDRM), was used for aging simulations in this study. In order to make understandable the simulation process, a brief description of UDRM simulation schemes will be provided in the following part.

5.2.1. Reliability Simulation Scheme in Eldo

The aim of reliability simulation is to be able to model the degradation occurring in the devices in a certain design causing deterioration in the performance of the design [80]. It is required to evaluate the amount of degradation occurring in a certain period of operation and examine the circuit performance after this period. A general view of reliability simulation in Eldo is shown in Figure 5.1 [80].

The amount of damage each transistor encounters depends on the bias conditions

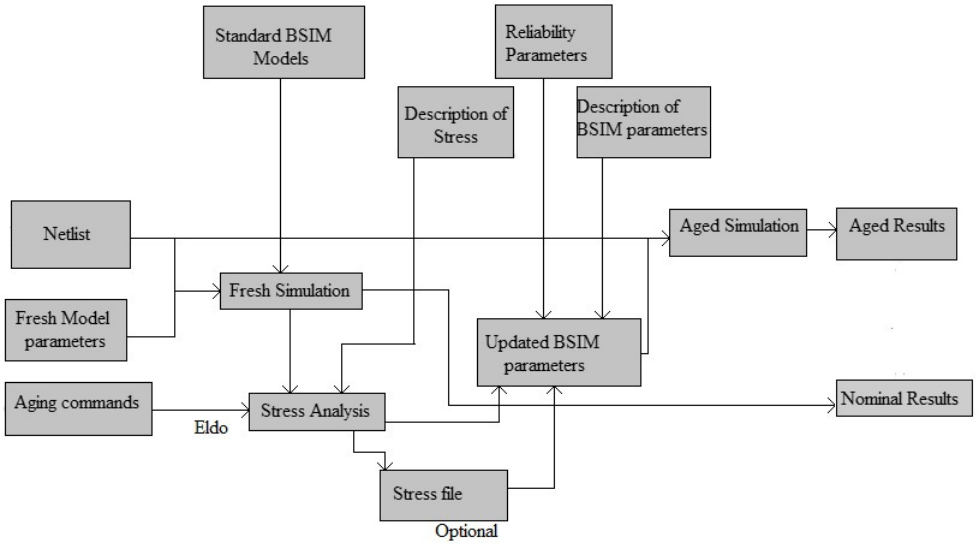

Figure 5.1. Reliability simulation in Eldo.

applied on that transistor and the time period through which this bias was applied. A quantity called "Stress" represents the extent of the damage where "Stress" is the integration of the instantaneous stress applied to the transistor. The integration is carried out from a certain time T_{start} (ideally zero), until the final age, T_{age} (usually after several years), where the characteristics of the design is to be evaluated [80].

This integration progress could be evaluated by running a transient simulation from T_{start} to T_{age}. However, it is very long to run such a transient simulation. Also it will not be possible to model the gradual change of characteristics and its effect on the damage rate [80]. Instead of this, a short transient simulation is run as a sample of the operating conditions, assumed to repeat over and over through the device's lifetime. At this situation "Stress" can be defined as

$$Stress = Stress_{\text{Int}} \times \frac{T_{\text{age}}}{T_{\text{tran}}} \tag{5.1}$$

5.2.2. Long-Term Reliability Simulation Scheme

There are two methods for long-term reliability simulation in the UDRM. These are: Two simulations scheme and Repetitive scheme. A flow chart of two simulations reliability simulation is shown in Figure 5.2 [80].

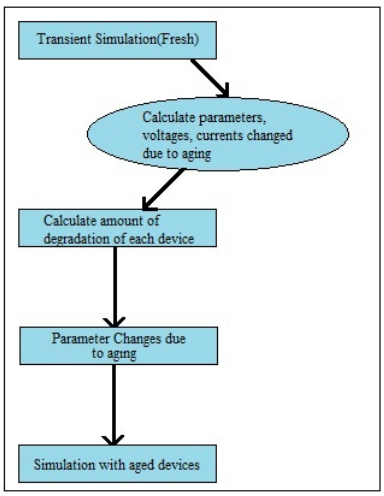

Figure 5.2. A flow chart of two simulations scheme.

This flow can be explained as, a transient simulation with the 'fresh' transistors is run. At the end of the fresh simulation, the stress of each transistor is calculated according to the amount of damage. Then, the transistor models are updated according to the calculated stress and the equations specified in the user defined reliability functions and finally a new transient simulation is run with the aged transistors [80].

In the repetitive scheme, on the other hand, the long period T_{age} is divided into smaller time slots T_{i} (where $T_{\text{age}} = \sum T_i$) and the same steps in the two simulations scheme are followed, except steps 2 to 4 are repeated NBRUN times, where NBRUN is the number of time intervals [80]. The calculation of the stress is updated at the end of every time interval using formula as

$$Stress = Stress + Stress_{\text{Int(i)}} \times \frac{T_{\text{i}}}{T_{\text{tran}}} \tag{5.2}$$

This loop will continue until $t = t_{age}$. This approach is more accurate due to accounting for the gradual bias changes in devices. Figure 5.3 represents the flow chart of the repetitive scheme.

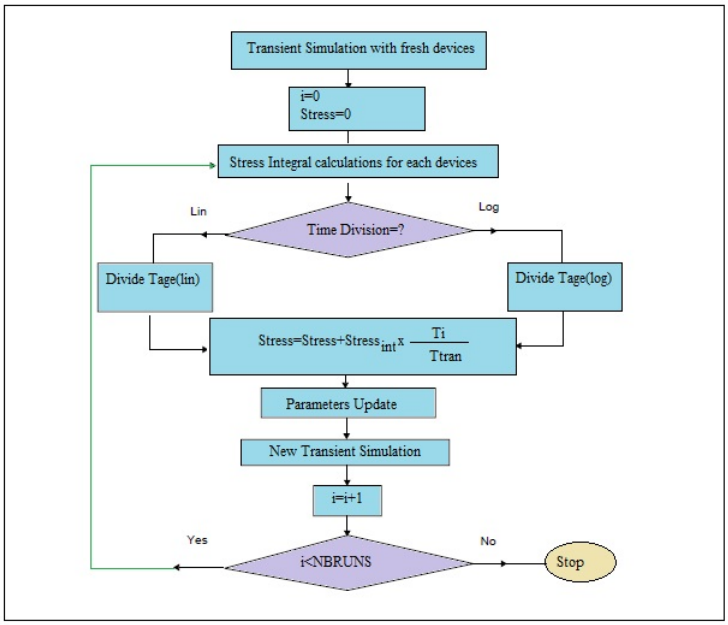

Figure 5.3. Flow chart of repetitive scheme.

According to [80], the simulation process is started by a transient simulation with fresh devices, the stress of each transistor is calculated, during the time division, using the equations in the UDRM. Afterwards, T_{i} is calculated to determine the next timing at which the aged simulation will be run. If linear time interval is specified, equal time periods will be considered, but, if a logarithmic time division is specified, the time divisions will be crowded at the beginning and get larger as T_{age} is approached. The calculated stress vector during T_{i} is then multiplied by a factor $T_{\mathrm{i}}/T_{\mathrm{tran}}$, where T_{tran} is the period of simulation. The above vector is added to the previous stress vector values. After updating the stress vector, it is used to change the parameters of the model file for each device in the circuit according to the reliability models. Now, the circuit is ready for a new aged transient simulation. This process is repeated NBRUNS times until reaching $t = T_{\mathrm{age}}$, where a final transient simulation is done and the performance of the circuit is examined.

5.3. Reliability Modeling in UDRM

UDRM introduces some aging models for HCI and NBTI. Although these models are not sufficient to observe accurate data, they can be used to get a general picture of the aging effects.

5.3.1. Hot Carrier Injection Model

The instantaneous stress due to HCI on any device is defined as a function of I_{ds} and I_{sub} as

$$HCI_{\mathrm{Stress}}(\mathrm{t}) = \frac{I_{\mathrm{ds}}(\mathrm{t})}{W.H}\left[\frac{I_{\mathrm{sub}}(t)}{I_{\mathrm{ds}}(\mathrm{t})}\right]^{m} \tag{5.3}$$

where W width of the transistor's channel, H technology dependent parameter which can be used for fitting and m parameter that can also be used for fitting. Ideally, m equals $(\phi_{\mathrm{it}}/\phi_{\mathrm{i}})$ where ϕ_{it} and ϕ_{i} are the critical energies for interface damage and impact ionization respectively.

5.3.2. Negative Bias Temperature Instability Model

The instantaneous stress on any device exposed to NBTI defined as a function of V_{gs}, such that the stress has value only when V_{gs} is negative as

$$NBTI_{\mathrm{Stress}}(t) = m\left[\frac{1}{2}(|V_{\mathrm{gs}}(\mathrm{t})| - V_{\mathrm{gs}}(\mathrm{t}))\right]^{H} \tag{5.4}$$

Where H is a technology dependent parameter. It can be used for fitting and m is a model parameter also used for fitting.

5.3.3. Model Parameter Update Methodology

In order to update the model parameters shifted due to the aging phenomena, UDRM uses a simply model

$$dP = \frac{P - P_0}{P_0} \tag{5.5}$$

where P is the parameter value at time t, and P_0 is the parameter value extracted at $t = 0$ s.

The value of dP is calculated as a function of the stress Integral(s), and the reliability model parameters. In the case, where there are more than one type of degradation, a separate parameter change value is calculated for each of them, then the total parameter change (dP) is their superposition.

$$dP = dp_{\mathrm{HC}} + dp_{\mathrm{NBTI}} \tag{5.6}$$

The parameter update are examined into two different trends: the power law and the saturated power-law. A linear relationship governs the parameter shift and stress according to power-law approach. On the other hand, this linearity is saturated after a definite stress amount in the saturated behavior approach. Figure 5.4 represents both these degradation patterns.

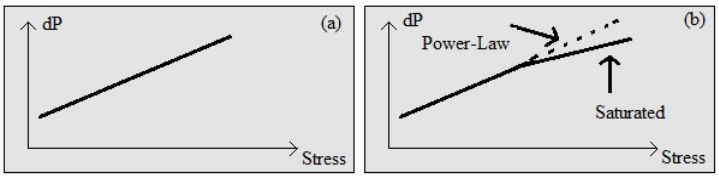

Figure 5.4. Parameter degradation patterns (a) Pure power-law degradation and (b) Saturated power-law degradation.

HCI parameter shift model can be expressed for power-law behavior as

$$dP_{\mathrm{HC}} = A \times HC_{\mathrm{S}}^{\mathrm{n}} \tag{5.7}$$

where A is the degradation constant, n is the degradation rate. On the other hand, if saturated-law is considered, the parameter shift equation takes form as

$$dP_{HC} = B \times [ln(1 + C \times HC_S)]^n \tag{5.8}$$

where B is a degradation constant, C is stress scaling constant and n is degradation rate. MOSFET parameters are listed according to their degradation patterns in Table 5.1.

Table 5.1. Degradation patterns of parameters.

Pattern	Parameter
Power-Law	VTH0, VOFF, NFACTOR
Saturated Power-Law	U0, UA, UB, VSAT, ETA0, AO, PCLM, PDIBCL2

UDRM provides a basic power-law model for NBTI which predicts a change in the parameter PMOS zero bias threshold voltage. The degradation pattern is expressed as

$$dP_{\mathrm{NBTI}} = A \times \mathrm{NBTI}_{\mathrm{Stress}}^{n} \times e^{\left[\frac{E_{\mathrm{a}}}{KT}\right]} \tag{5.9}$$

where A is the degradation constant, n degradation rate, E_{a} is thermal activation energy, K is Boltzman constant and T is temperature in degrees Kelvin.

5.3.4. Aging Model of Time Dependent Dielectric Breakdown

UDRM provides some reliability models only for HCI and NBTI, however there is no model for TDDB degradation. Thereby, a different method will be used to

simulate the TDDB effects. TDDB causes a short circuit between the gate and the channel over time. Firstly, soft breakdown occurs, however, this would not change the circuit behavior when the transistor is on state. On the other hand, due to the acceleration effect of temperature, SBD worsens and the hard breakdown occurs. The narrower path starts to behave as a wire between the gate and the channel, because the width of the path expends with time, so the resistance of the wire decreases. Figure 5.5 shows the post breakdown behavior versus the breakdown location.

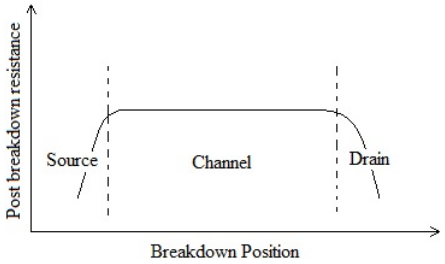

Figure 5.5. Breakdown resistance vs breakdown location.

As can be seen from the figure, the resistance value of wire reach the maximum value at the drain and the source extensions because of high electric field. On the other hand, if the breakdown occurs along the channel, the resistance would be higher, so this would not cause any important degradation. Figure 5.6 represents a method to test TDDB effect.

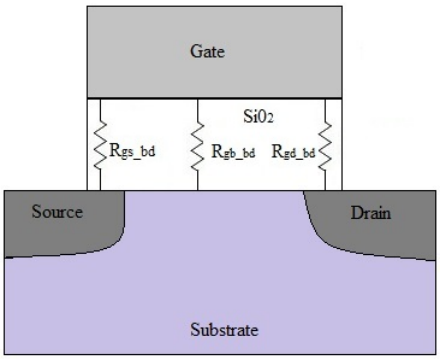

Figure 5.6. A cross-section of MOSFET with breakdown resistances.

There would be three different possibilities of resistance location(the drain, the source, and the gate). R_{gs}, R_{gb}, and R_{gd} denote the gate to the source resistance, the gate to the bulk resistance, and the gate to the drain resistance, respectively. These resistance values change from a few to a few hundred kilo ohms. R_{gs} and R_{gd} would be lower than the R_{gb}, because HBD occurs more heavily at these sides of transistor. Briefly, due to the absence of a reliability model of TDDB in UDRM, a simple method was proposed to test the circuits against to TDDB. According to this method, some post-breakdown resistances are added to design schematics, thus, circuits are aged, and simulations are performed again with aged transistors.

5.4. Aging Analysis

The aim of this section is observing the aging effects (HCI, NBTI, and TDDB) on phase noise of oscillators which were designed in Chapter 4. There were mainly three different oscillator structures: NMOS, PMOS, and CMOS and each structure had 3 different biasing methods: constant current source, tail NMOS biasing and current mirror biasing. Phase noise response of each structure was shown in Table 4.3 obtained by simulating fresh transistors. In this section, each part (tail and differential) of oscillators will be aged separately and the effects on phase noise of these degradations mechanisms will be determined. Therefore, it is necessary to remind the phase noise equation used in Chapter 4 in order to evaluate the results accurately.

Phase Noise of Differential pair LC Oscillator was given as

$$L(w_{\mathrm{m}}) = \frac{4.F.k.T.R}{V_{\mathrm{o}}^2}\left(\frac{w_{\mathrm{o}}}{2Q.w_{\mathrm{m}}}\right)^2$$

where

$$F = 2 + \frac{8\gamma R I_{\mathrm{t}}}{\pi V_{\mathrm{o}}} + \gamma\frac{8}{9}g_{\mathrm{mbias}}R$$

for NMOS and PMOS structures, and

$$F = 2 + \frac{8\gamma R I_t 2}{\pi V_o} + \gamma \frac{8}{9} g_{mbias} R$$

for CMOS.

It is important to note that, HCI and NBTI manifest themselves degradation in threshold voltage of either NMOS or PMOS. Moreover, the mobility is reduced as a result of HCI in n type transistors. In this sense, NMOS and PMOS structures shown in Figure 4.6 and 4.7 may be affected by HCI and NBTI, respectively. Furthermore, the CMOS oscillators may be exposed to both HCI and NBTI due to including both NMOS and PMOS. On the other hand, TDDB may cause degradation on phase noise of all oscillator structures.

Initially, if the first circuit (NMOS1) is considered, there are only two NMOS transistors at differential part, so only HCI may affect the circuit performance over time. According to the previous sections, HCI manifests itself degradation in threshold voltage and mobility of NMOS. In this sense, V_{th} and μ_0 parameters of each NMOS were changed in a certain interval and phase noise results were observed through simulations. Figure 5.7 and 5.8 show the phase noise results. Noise1 and Noise2 denote the phase noise response of the oscillator whose transistors were aged independently and equally, respectively. As can be seen from the results, the differential part of the oscillator does not have any considerable effect on the phase noise. This case can be explained by using Table 4.5 which involves the phase noise factors. The phase noise factor of differential part is about 7 times smaller than the tail noise factor, thus, any degradation in this part would not cause a visible change on the phase noise. In addition, some aging calculations were performed by using equations provided by UDRM and the results were added to outputs showed by black-bold lines in Figures 5.7 and 5.8.

On the other hand, if a tail MOSFET is placed to the NMOS1 structure (NMOS2), the tail will also age over time. Figure 5.9 and 5.10 exhibit the results of aging of tail MOSFET due to HCI.

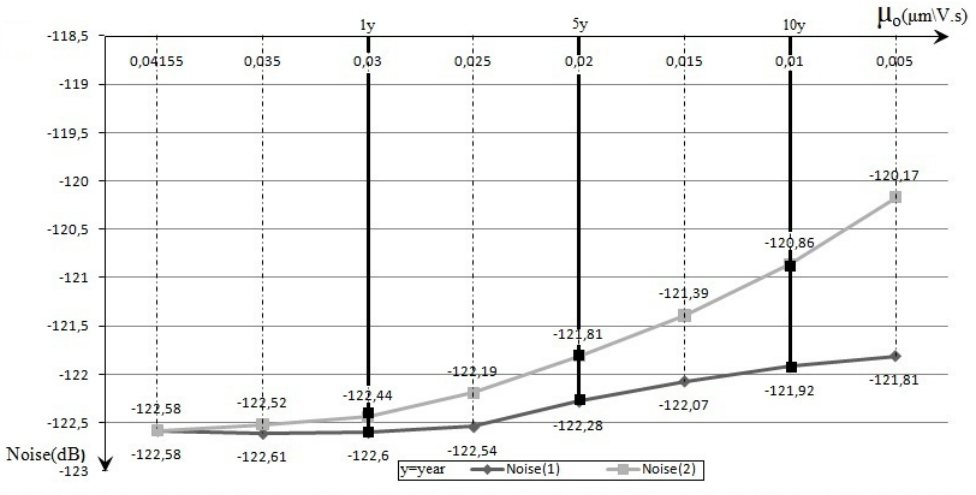

Figure 5.7. Mobility degradation results of NMOS1 (HCI).

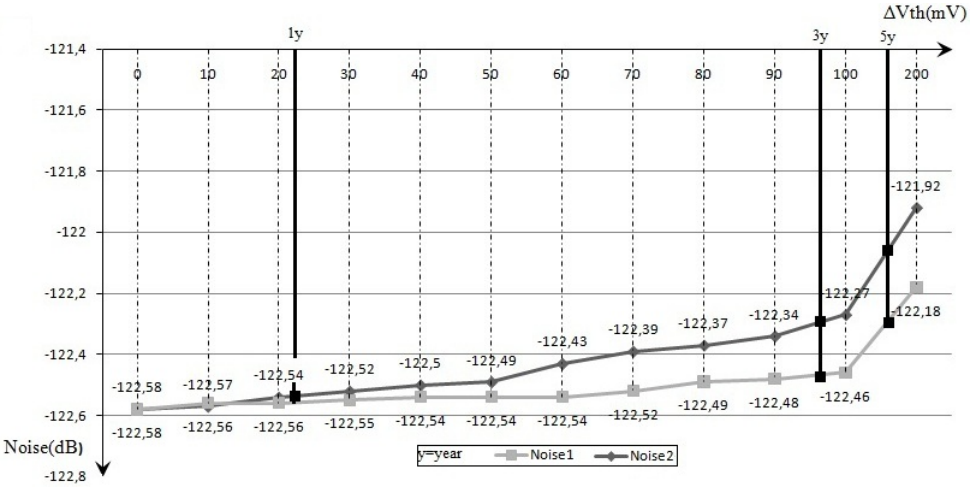

Figure 5.8. Threshold voltage degradation results of NMOS1 (HCI).

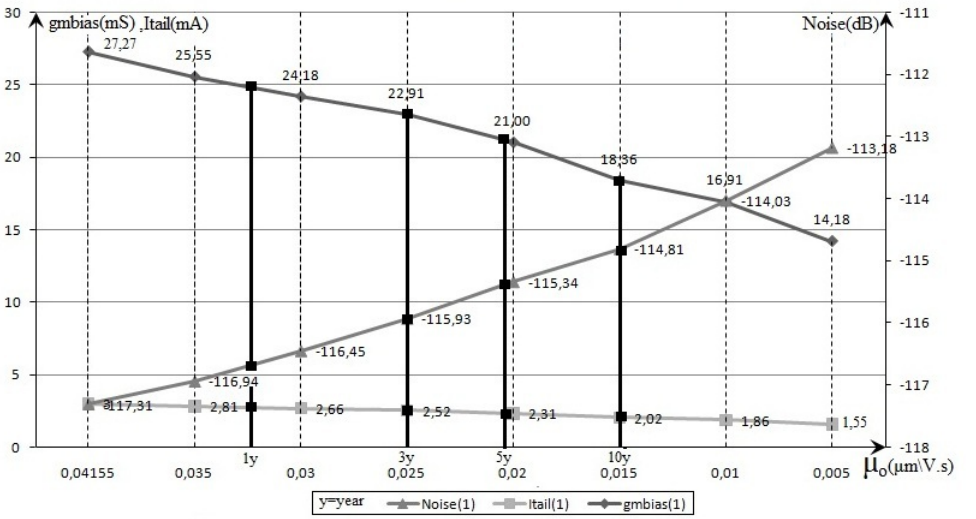

Figure 5.9. Mobility degradation results of tail transistor of NMOS2 (HCI).

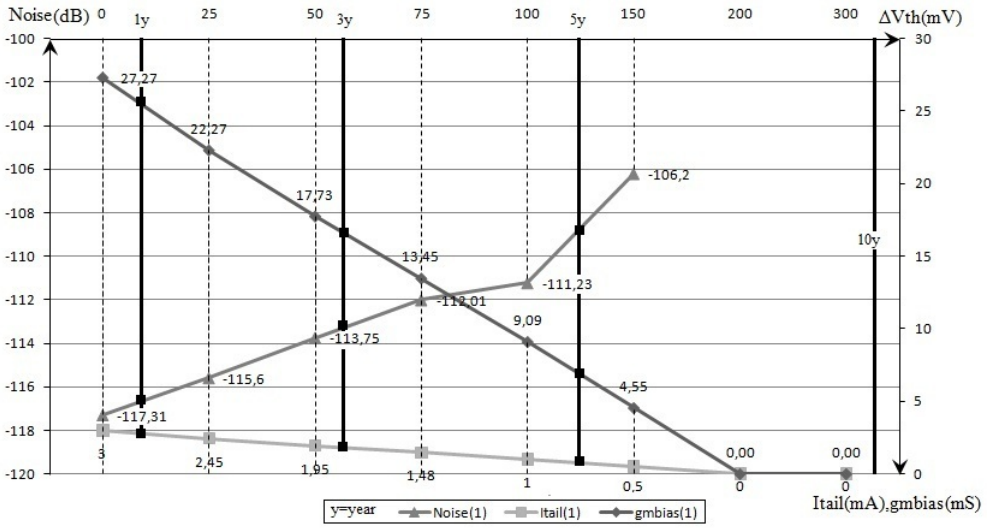

Figure 5.10. Threshold voltage degradation results of tail MOSFET of NMOS2 (HCI).

Considering the reliability simulation results of NMOS2, the tail MOSFET degradation affects the phase noise behavior negatively. Figure 5.9 represents the phase noise response versus mobility after HCI degradation. The phase noise increases from -117 dB to -114 dB at the end of 10 years working period. Another aging analysis was performed for threshold voltage degradation. Figure 5.10 shows the phase noise behavior versus shift in V_{th} due to HCI. The phase noise increases from -117 dB to -109 dB after 5 years working period. Both V_{th} and μ_0 degradations cause reduction in tail current and these changes result with worsening phase noise response. According to Equation 4.21, the tail current and transconductance were directly proportional to the noise factor of tail part. In addition, it has been pointed out that the tail MOSFET is the most noisy part of the oscillator, so any change in tail current will dramatically increase the phase noise response. Furthermore, the tail current will also affect the differential part noise as can be seen from Equation 4.21. The tail current and the transconductance of tail MOSFET changes are also shown in Figure 5.9 and 5.10.

Next, the tail MOSFET was replaced by an NMOS current mirror (NMOS3). There can be derived a number of combination of the tail current degradation due

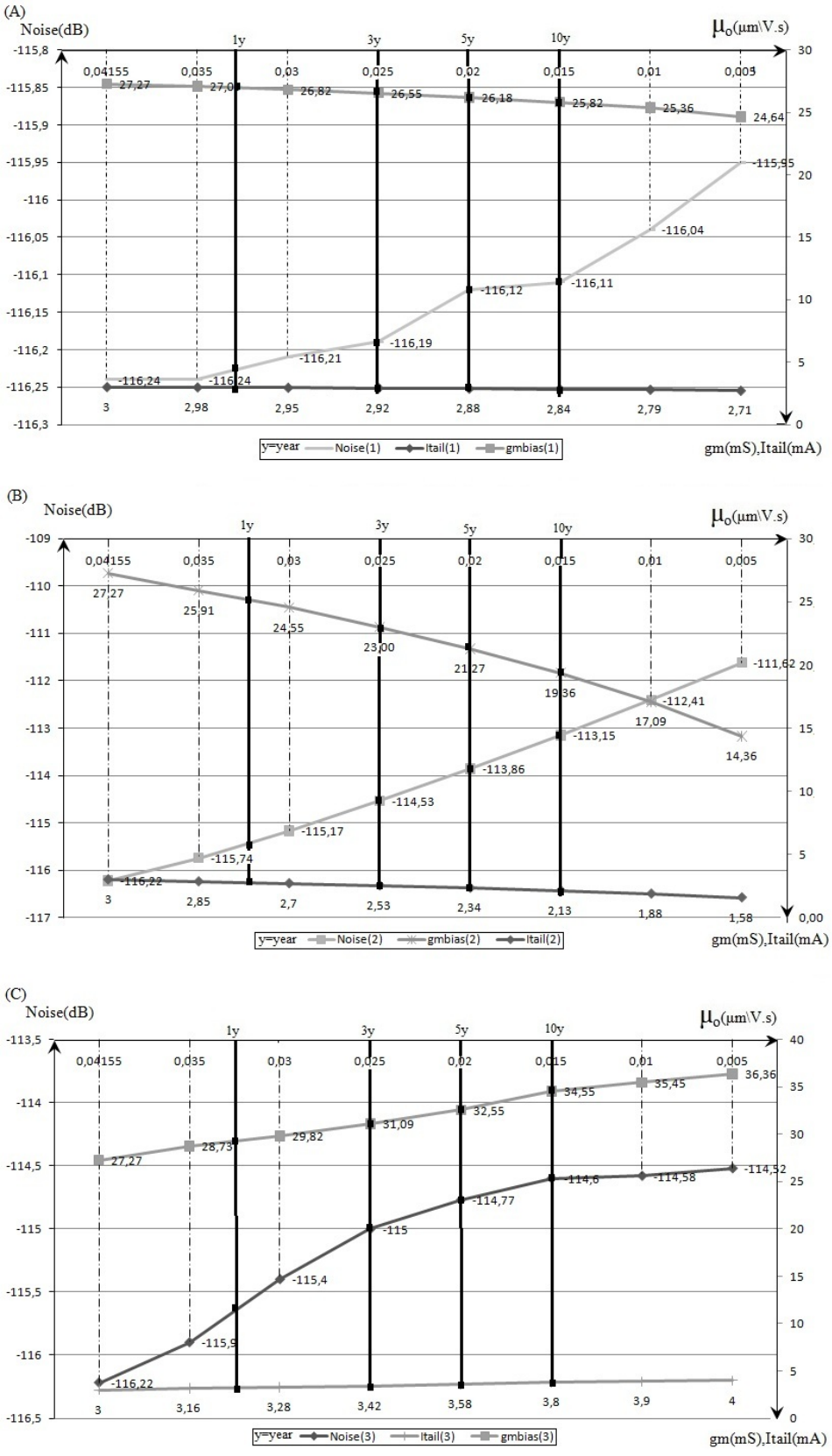

Figure 5.11. Mobility degradation results of tail MOSFET of NMOS3 (HCI).

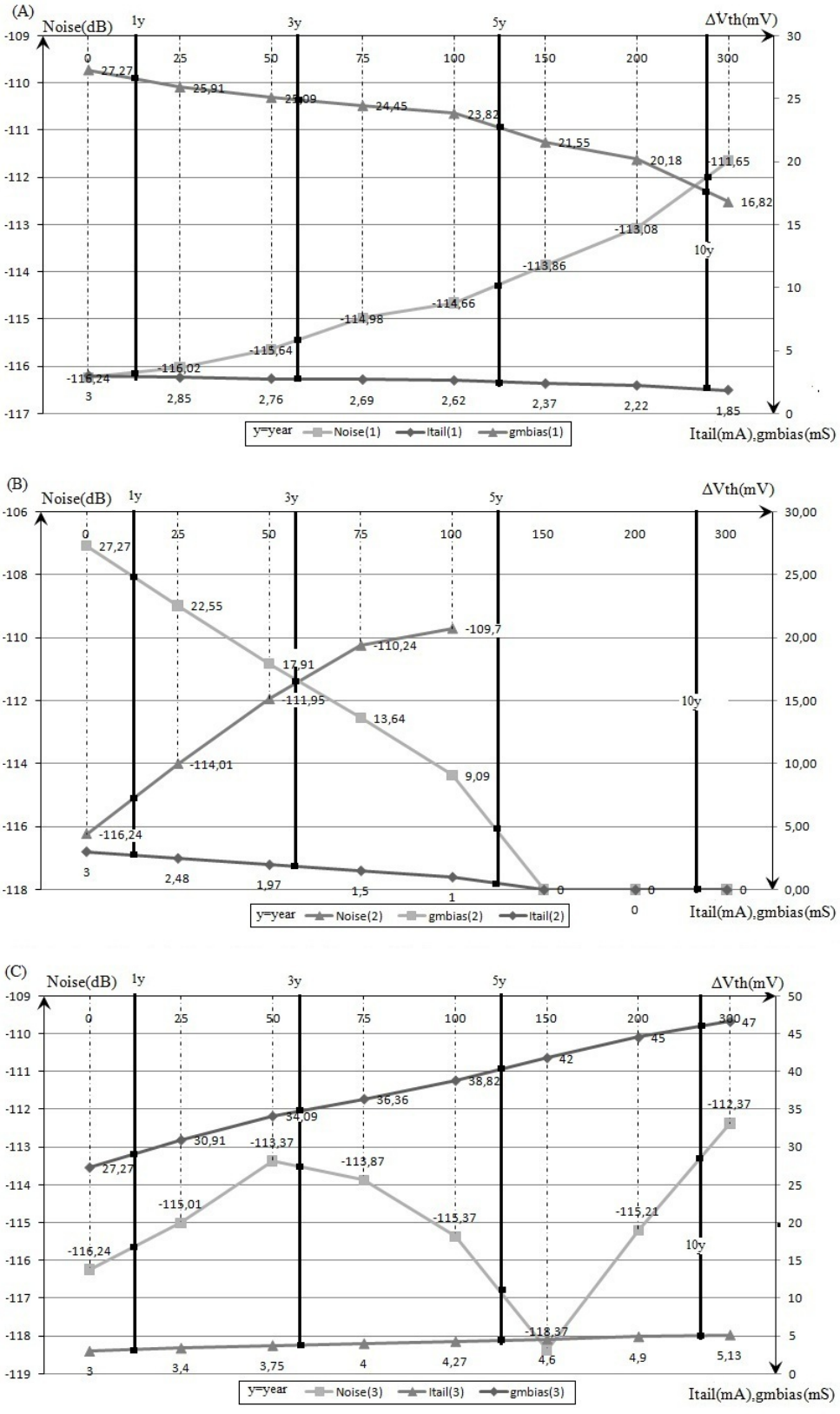

Figure 5.12. Threshold voltage degradation results of tail MOSFET of NMOS3 (HCI).

to HCI. The biasing part and the mirror part of the tail circuit may age either independently or together, therefore, the phase noise results will vary due to several aging possibilities of the tail part. At first, if the tail NMOS devices were exactly matched, HCI would affect these devices equally. On the other hand, if transistor properties are different for each device, degradation amount for each device would be different from each other, and so either the biasing NMOS would age more than the mirror MOSFET or vice versa. All of these possibilities have been simulated and results were given in Figure 5.11 and 5.12. According to the results, if both transistors were exactly matched, the phase noise response would show the minimum variation and the circuit would maintain its regular function for a long time. However, if the mirror MOSFET ages more, the reliability of the circuit would worsen over time, because the balance of the mirror would be degraded due to the difference of parameters of two devices. After a long working period, the threshold voltage will increase and the mobility will decrease, thus, the tail current and the transconductance will considerably decrease and transistor will turn off when the threshold voltage shift reaches hundreds levels. On the other hand, if the biasing MOSFET ages more, the phase noise would have an unstable response for short time degradation, because switching transistors would start to circulate between cut-off, saturation, and triode mode while oscillator operates under current limited mode [81], however, for long term, it would also be degraded. The variation of tail current and transconductance were also given in Figure 5.11 and 5.12. Reliability calculation results (black bold lines) were also added to the output figures.(A) represents the case at which transistors are aged equally, (B) represents the case at which the mirror MOSFET is aged more, and (C) shows the case at which the biasing MOSFET is aged more.

The other structures designed in Chapter 4 are PMOS type oscillators. Since there are no PMOS transistor in the NMOS type oscillators, NBTI effects were not considered. However, in PMOS oscillators, NBTI may occur and manifest itself at the output of the circuits. The methodology is the same that used in HCI analyses, however, in contrary to HCI, NBTI only causes threshold voltage degradation. In order to observe the degraded parameters due to NBTI, the below equations were used

through all calculations. Table 5.2 shows the parameter values that were obtained from literature.

$$\Delta V_{\mathrm{th}} = K_{\mathrm{v}} \beta^{\frac{1}{4}} T^{\frac{1}{4}} \left[1 - (1 - \sqrt{n(1-\beta)})^{2n-2} \right]^{\frac{1}{2}} \tag{5.10}$$

$$K_{\mathrm{v}} = A T_{\mathrm{ox}} \sqrt{C_{\mathrm{ox}}(V_{\mathrm{gs}} - V_{\mathrm{th}})} exp\left(\frac{E_{\mathrm{ox}}}{E_{\mathrm{o}}}\right) \left[1 - \frac{V_{\mathrm{ds}}}{\alpha(V_{\mathrm{gs}} - V_{\mathrm{th}})} \right] exp\left(-\frac{E_{\mathrm{a}}}{kT}\right) \tag{5.11}$$

Table 5.2. Parameter values of V_{th} degradation.

Parameter	A	E_0	E_{a}	t_{ox}	α	η	δ_{v}	V_{th}
	[mV/nm/C$^{0.5}$]	[mV/cm]	[eV]	[nm]	[—]	[—]	[mV]	[mV]
Value	1.8	2.0	0.13	2.25	1.3	0.35	5.0	216

where n is number of cycles, β is duty cycle and T is temperature degrees in Kelvin.

Initially, if the first structure has been examined, since bias current is supplied by a constant current source, only differential part will age over time. Simulations were performed by using degraded threshold voltage values, however, the results were similar with the simulation results of NMOS1, so threshold voltage shifts at differential part have no visible effect on the phase noise. Moreover, an approximate V_{th} degradation have been calculated using the above formula at elevated temperature (350 Kelvin). Although the amount of threshold voltage shift is nearly 95mV, the phase noise behavior was not alternated considerably. After that, a PMOS was added to PMOS1 to generate the bias current (PMOS2), and same analyses were performed for this design. Since NBTI causes increase in threshold voltage, the bias current and the transconductance of biasing part decreases, and this case causes to worsening phase noise response over time. Figure 5.13 represents the phase noise, tail current,

and transconductance of tail PMOS behavior versus shifts in threshold voltage due to NBTI.

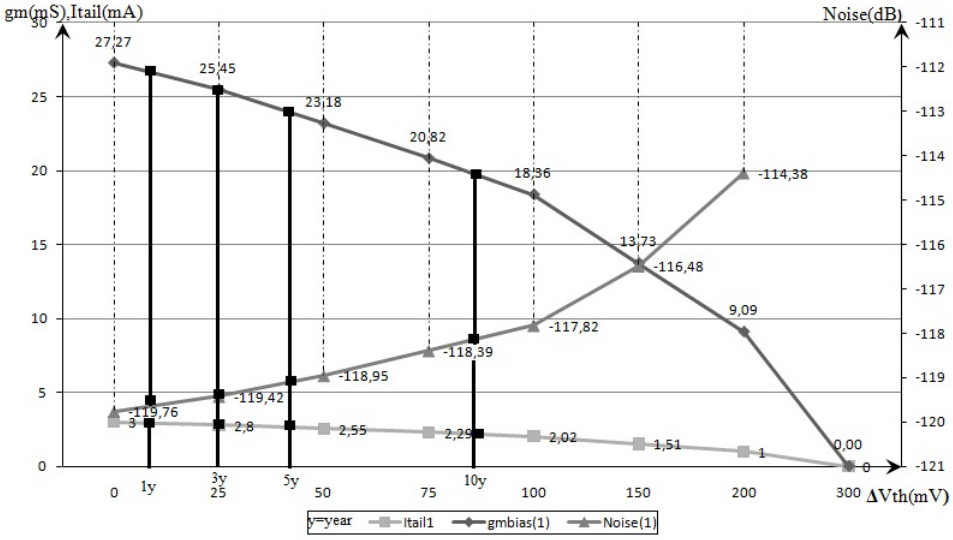

Figure 5.13. Threshold voltage degradation results of tail MOS of PMOS2 (NBTI).

The next PMOS circuit was PMOS3 which involves a PMOS current mirror circuit instead of the tail PMOS device. All simulation and calculation steps mentioned before were performed again for this circuit. As obtained before, the tail part of the oscillator has the most dominant role on the phase noise response. The current mirror structure involves two PMOS devices and these devices may age either equally or independently. Simulations have been performed considering all these possibilities and results were given in Figure 5.14. (A) shows the results at which transistors are aged equally, (B) shows the results at which the mirror PMOS is aged more, and (C) shows the results at which the biasing MOS is aged more. After 10 years working period, threshold voltage would increase up to nearly 100 mV, but, the phase noise responses would not alternate as compared to the other structures, so it can be easily said that PMOS oscillators are more robust to aging than the other structures.

At last, the CMOS oscillators were tested and reliability simulations were performed as well as the other structures. Figure 5.15 shows the results of reliability

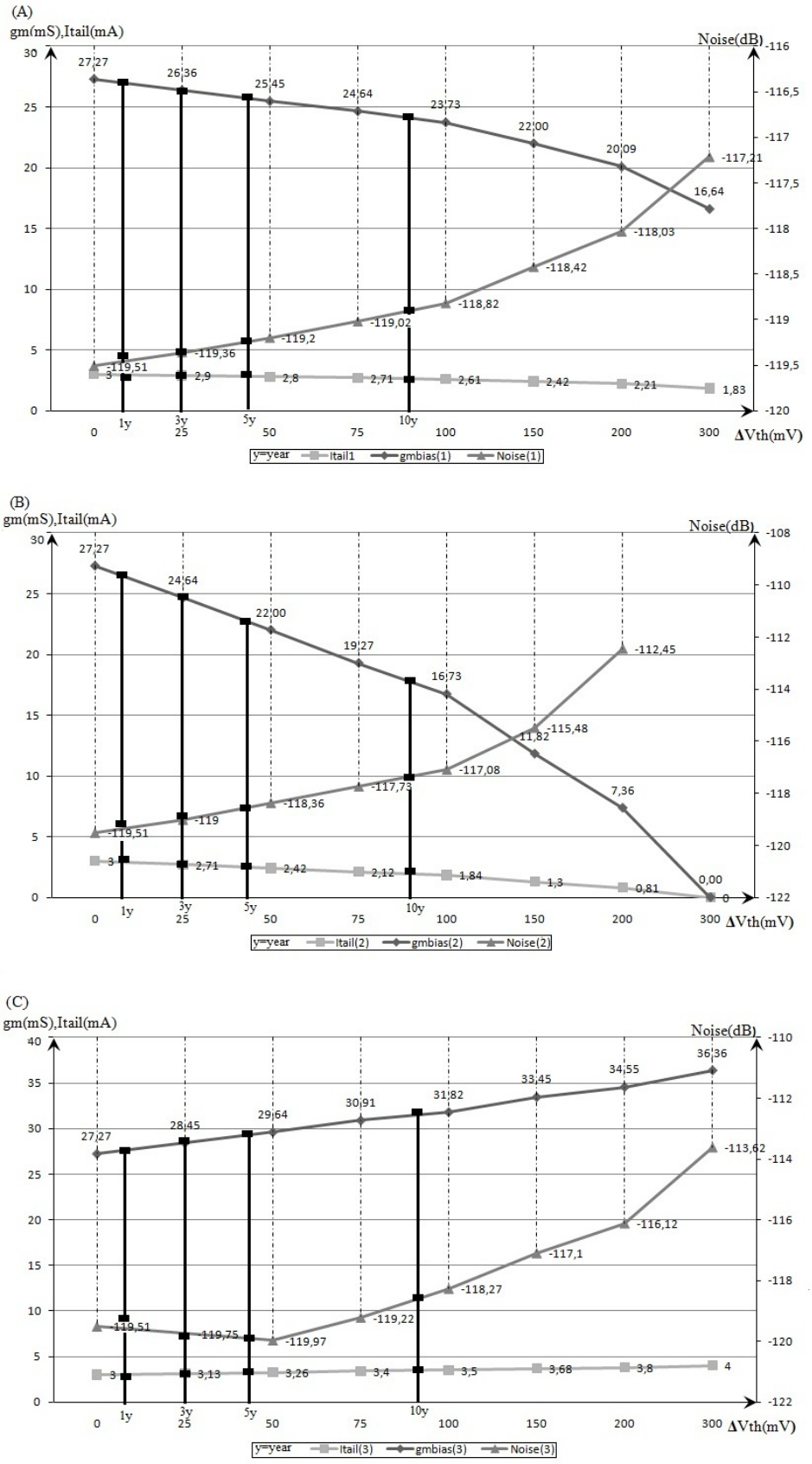

Figure 5.14. Threshold voltage degradation results of tail MOS of PMOS2 (NBTI).

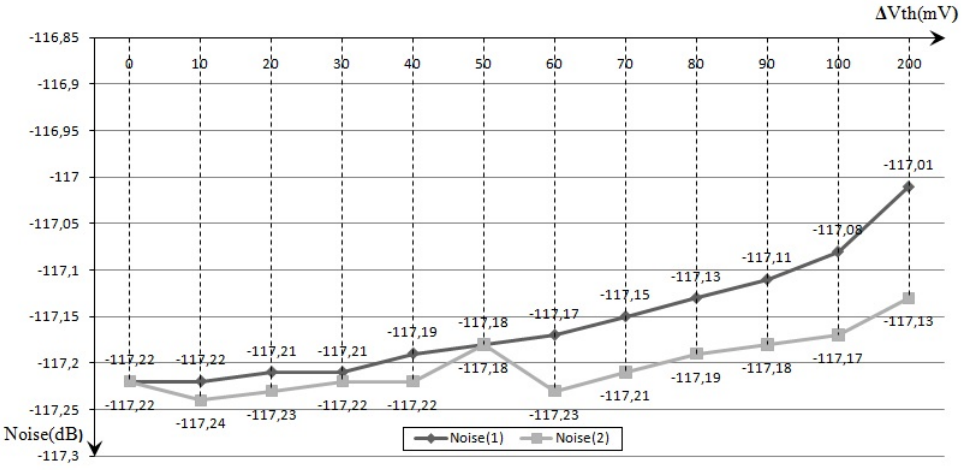

Figure 5.15. Threshold voltage degradation results of CMOS1: Noise1 denotes the degradation of NMOS part and Noise2 denotes the degradation of PMOS part.

analysis of CMOS1. The design includes two differential part and the bias current is supplied by a constant current source, thus, the effect of aging can only be monitored at the differential parts. According to the results, aging of differential parts does not cause any visible increase in phase noise as well NMOS and PMOS structures whose bias currents were also supplied by constant sources.

A tail NMOS was placed to the tail of the CMOS oscillator and this oscillator had named CMOS2. In contrary to CMOS1, an additional analysis was performed to observe the effect of tail part degradation on phase noise. As well as NMOS oscillators, HCI causes degradation at the tail MOSFET which leads to an increase in the threshold voltage and a decrease in the mobility of the device. These changes in device parameters cause reduction in tail current and transconductance which are directly proportional to the phase noise response. The reliability analysis results of CMOS2 are given in Figures 5.16 and 5.17.

Finally, the last oscillator (CMOS3) was examined and the same reliability simulations were performed. A current mirror produces the bias current at this oscillator, so the HCI effect exists on the tail part. On the other hand, HCI and NBTI effects

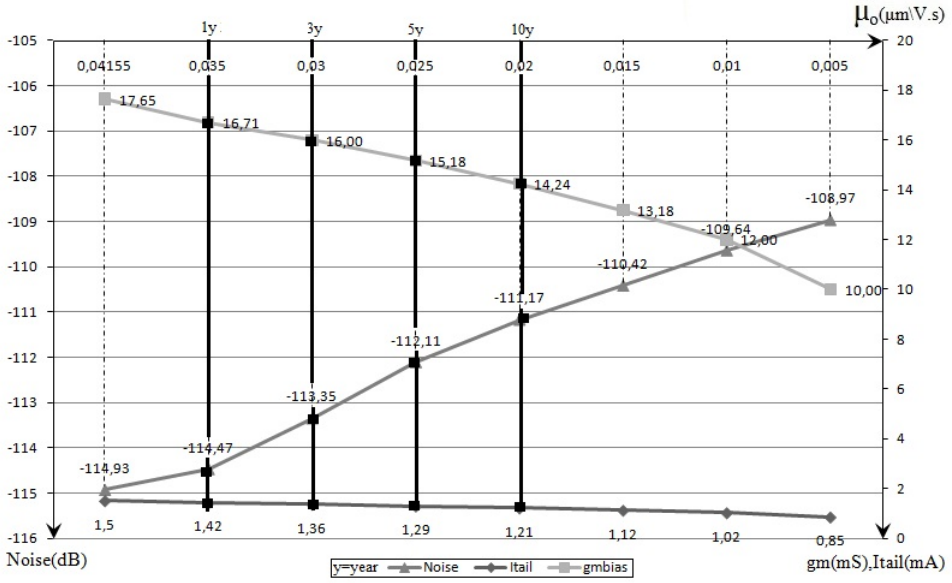

Figure 5.16. Mobility degradation results of tail MOSFET of CMOS2 (HCI)

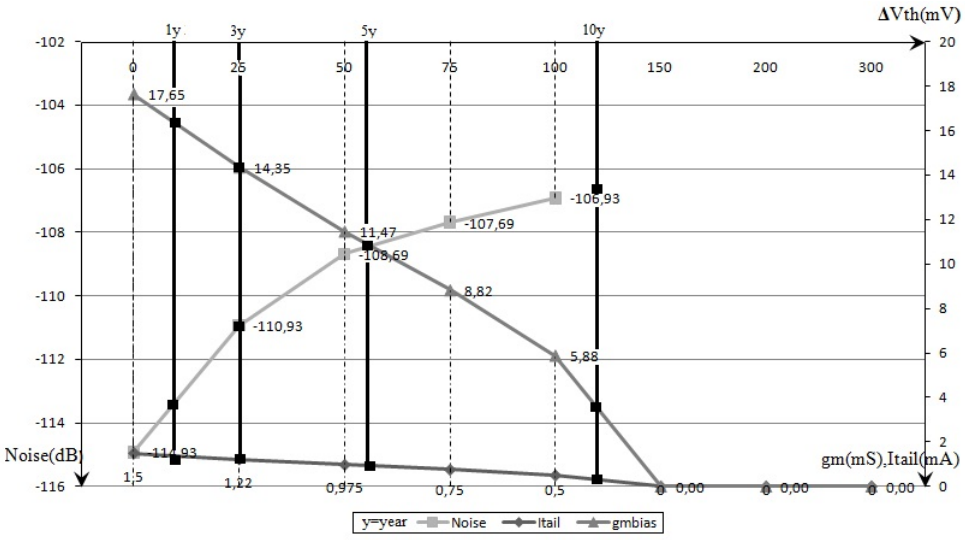

Figure 5.17. Threshold voltage degradation results of tail MOSFET of CMOS2 (HCI).

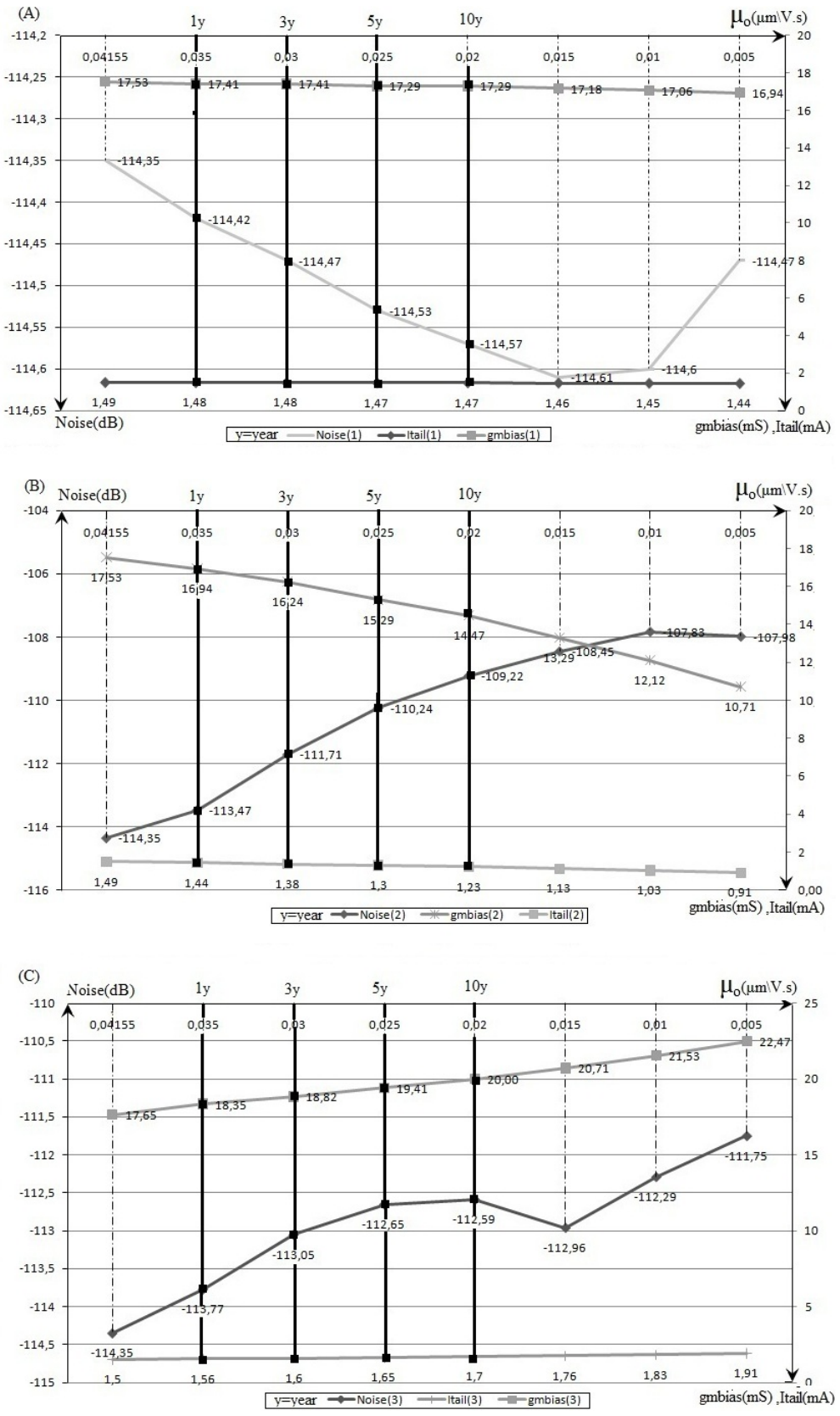

Figure 5.18. Mobility degradation results of tail MOSFET of CMOS3 (HCI).

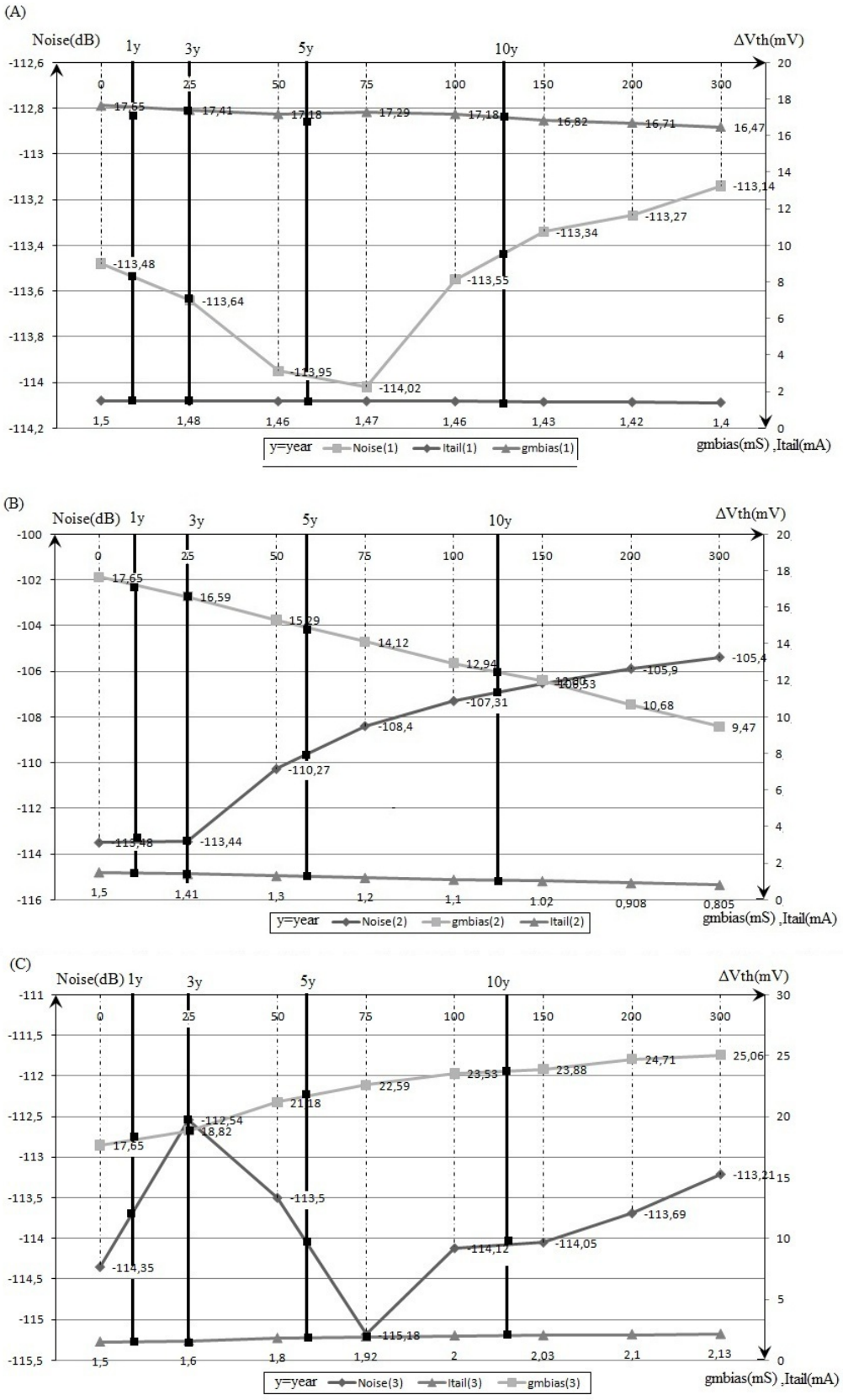

Figure 5.19. Threshold voltage degradation results of tail MOSFET of CMOS3 (HCI).

were also examined for differential parts, however, the results have been observed as similar as NMOS3 and PMOS3 results, so differential part effect can be neglected contrary to tail part effect. All possibilities of aging of tail part mentioned before were simulated and the results were given in Figure 5.18 and 5.19. (A) shows the results at which transistors are aged equally, (B) shows the results at which the mirror NMOS is aged more, and (C) shows the results at which the biasing MOS is aged more. In addition to simulation results, reliability calculation results were also added to these results illustrated by dark-bold lines. If the transistors age equally, the effect of degradation on phase noise would not be as visible as the results of CMOS2. On the other hand, if the mirror ages more, the degradation would cause a considerable increase in phase noise as can be seen from the figures. Lastly, if the bias MOSFET ages more, the phase noise would have a unstable response until current increases up to transition region from to current limited mode to voltage limited mode, and the phase noise would start to show a stable increase.

HCI and NBTI reliability simulations were performed by using UDRM provided by Eldo, however, UDRM does not include any model for TDDB. The method proposed in the previous section was used to observe TDDB effects on phase noise response of oscillators. The method can be summarized that several post-breakdown resistances are added to transistors according to the location of breakdown. The hard breakdown occurs either the gate to the channel or the gate to the drain or the source. It is a well known fact that dielectric breakdown occurs near the higher electric fields and is accelerated by elevated temperatures. The highest electric field occurs at the drain extensions for the oscillator design, because the maximum voltage swing (approximately $2V_{\mathrm{dd}}$) is encountered between the gate and the drain nodes due to cross-coupled structure. While one transistor is conducting current, the other one is off state and the output of one transistor is coupled to the gate side of the other transistor, thus, the voltage swing between the gate and drain may reach to $2V_{\mathrm{dd}}$. Although the maximum electric field occurs at the drain side, all possibilities were tried during simulations and effects of all of these were illustrated clearly. The assumption was that when the breakdown occurs at drain or source extensions, the post-breakdown resistance reaches

the minimum value and exhibits a linear increase or the breakdown occurs through to the channel and the resistance reaches the maximum value and show a constant behavior. All resistances used to observe TDDB effects were chosen pessimistically, considering the curve shown in Figure 5.5. The simulation results are shown in Table 5.3.

Table 5.3. Simulation results after TDDB.

Structure		Phase Noise[dB]		
	[$R_{gd} = 2$ kΩ]	[$R_{gb} = 10$ kΩ]	[$R_{gs} = 2$ kΩ]	[Initial]
NMOS2	-113.13	-117.035	-114.96	-117.31
PMOS2	-112.24	-119.49	-117.35	-119.76
CMOS2(NMOS)	-110.76	-113.91	-112.85	-114.93
CMOS2(PMOS)	-110.76	-114.32	-112.48	-114.93
		Output Voltage[V]		
NMOS2	0.9	1.72	1.3	1.8
PMOS2	0.8	1.55	1.15	1.6
CMOS2(NMOS)	0.95	1.3	1.2	1.35
CMOS2(PMOS)	0.95	1.3	1.1	1.35
		Negative Resistance[Ω]		
NMOS2	540	881	790	961
PMOS2	436	770	714	800
CMOS2(NMOS)	440	555	528	571
CMOS2(PMOS)	440	568	537	571

As mentioned in Chapter 2, when the breakdown occurs through the channel, the breakdown resistance would be higher with respect to occurring at the drain side or the source side. Therefore, the gate to bulk resistance was chosen 10 kΩ and this resistance was added to transistors of differential parts for NMOS2, PMOS2 and CMOS2 oscillators, respectively. As can be seen from the results, even this pessimistic resistance could not change the oscillator behavior, because the output voltage and the negative resistance did not exhibit a considerable change. In addition, higher

resistances were added to the same structures to observe the TDDB aging which occurs at the source extension. The effect of TDDB would be more remarkable when the breakdown occurs at the source side, because the negative resistance and the output voltage would alternate and this case would cause an increase in the phase noise. Finally, the post-breakdown resistances were added to drain side of the oscillators and simulations were performed again. As can be seen from simulation results, the most considerable degradation was observed when the breakdown occurs at the drain side of the oscillators. The phase noise was described as the instantaneous change at the output and the output nodes of the oscillator circuits at the drain sides of differential parts, thereby, the output voltage decreases and the transconductance of the differential part.

5.5. Results and Discussion

The first structures of each oscillator architecture include differential part transistors and tail currents are supplied by constant current sources. Therefore, reliability analyses were performed only for the transistors placed on the differential parts. Simulation results illustrate that aging of differential part due to HCI and NBTI has no considerable effect on phase noise. Taking into consideration the phase noise formula and noise factors of each part, it is not an unexpected result, because aging does not cause any degradation in drive current and transconductance which are the dominant parameters for phase noise calculation. Moreover, the phase noise factor of this part isn't as effective as the noise figure of tail part. In short, both HCI and NBTI cause degradation in some transistor parameters, however, aging of differential part does not lead to a visible deterioration on the phase noise.

The second structures have a tail MOSFET instead of the constant tail source, so the aging of tail part gains importance for this configuration. N type tail MOSFET was used for NMOS and CMOS oscillators, thus, HCI effects were considered while transistors were aged. The mobility and the threshold voltage were changed regarding the formulas provided by UDRM. Simulation results show that aging of tail MOSFET causes increase in phase noise due to degradation of drive current and transconductance

of tail MOSFET which are significant values for noise factor of tail MOSFET. On the other hand, PMOS transistor was used in PMOS structures to constitute the bias current, so NBTI was considered for this structure. The same comments could be repeated for NBTI, however, NBTI only degrades threshold voltage while HCI causes reduction in the mobility. Furthermore, HCI causes about 120 mV shift in V_{th} after 5 years while NBTI causes 40 mV, thus, it can also be concluded that the damage caused by NBTI degradation is less significant than that of HCI degradation.

Another possible alternative to produce the bias current is current mirror architecture (NMOS3, PMOS3, and CMOS3). A basic current mirror includes two transistors and the balance of the mirror is directly proportional to matching of these two transistors. If the amount of stress on these transistors are accepted equal, the degradation of parameters would be equal, so the balance of the mirror would not exhibit great deviations after aging period. Therefore, aging may not cause considerable changes at the output. However, if the transistors age independently, the equilibrium would be affected, so drive current and transconductance would be degraded. Therefore, these structures have two different possibilities, either the bias transistor ages more or the mirror ages more. Simulations and calculations were performed considering all these possibilities. According to the results, if the transistors were exactly matched, aging would not cause great increase in the phase noise. Furthermore, when the mirror transistor ages more than the other, the aging effect would be similar with the aging of single tail MOSFET so decrease in the drive current and transconductance causes increase in the phase noise. However, the most interesting results were obtained for the third probability. Phase noise behavior showed an unstable behavior when the bias MOSFET is aged more. The expected phase noise trend after the increase in the tail current due to aging was the increase in the phase noise as shown in Figure 4.5. However, the phase noise response was different from the expected one. It increased at first up to a certain current value and then, it started to behave as estimated. This difference could be explained by using a newer curve shown in Figure 5.20 instead of the conventional one.

Oscillator operates under current limited mode and differential part transistors

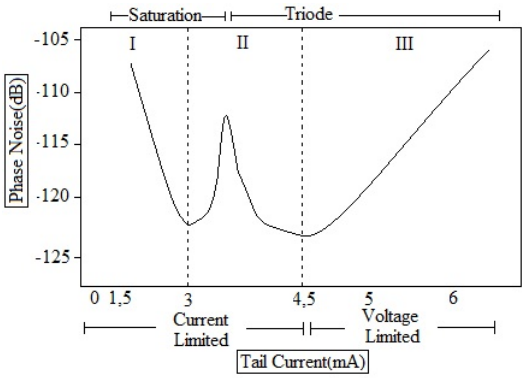

Figure 5.20. Phase noise vs tail current (a newer model).

switch between cut-off and saturation mode at the first section of the curve. The flicker noise of tail transistors is the dominant source of noise [81]. In region two, differential transistors circulate between cut-off, saturation, and triode mode operations while transistor still operates under current limited mode and the noise of tail continues to dominate total of noise [81]. However, in region three, $1/f$ noise of differential part is the main source of increased phase noise caused by second harmonic mechanisms [81]. In this context, the phase noise shows a different trend as shown in figure contrary to conventional one. Therefore, the results of aging bias MOSFET should be evaluated regarding this curve. When the bias MOSFET ages more, the balance of current mirror is degraded and the drive current increases over time. The phase noise decreases until the voltage limited mode and it increases due to second harmonic modulation.

At last, considering Time Dependent Dielectric Breakdown simulations, three different probabilities were considered through simulations and resistances were added to the differential part transistors only, because electric field is much higher at this part due to the higher voltage amplitude across to the gate and the drain. When the breakdown occurs at the channel, this would not cause a visible effect on phase noise. On the other hand, if it occurs at the drain or side, the resistance of the conductive path would be smaller, because of the higher electric field effect. Furthermore, although the same post-breakdown resistances were placed to the drain and the source, the breakdown of drain side oxide causes more degradation in phase noise due to the more

alternation of output voltage and transconductance.

Table 5.4. Phase Noise Results at 1 MHz offset frequency after aging($\Delta V_{\text{th}} = 100$ mV).

Structure	After HCI Stress[dB]		After NBTI Stress[dB]	
	Calculation	Simulation	Calculation	Simulation
NMOS2	-111.5	-111.23	—	—
NMOS3	-110.9	-109.7	—	—
PMOS2	—	—	-111.8	-113.22
PMOS3	—	—	-111.1	-111.85
CMOS2	-110.05	-108.98	—	—
CMOS3	-109.85	-107.42	—	—

In addition, as a novel study, phase noise calculations were re-performed after the circuits were aged and the results are shown in Table 5.4. The phase noise simulation and calculation results are obtained considering 100 mV shift in the threshold voltage. Although there are also some small differences between the calculation and simulation, Abidi's formula preserves its accuracy after circuits aged.

A performance comparison table is shown in Table 5.5. All structures were evaluated according to drive current, voltage supply, phase noise and robustness. According to the Table 5.5, the PMOS oscillators are the less noisy structures, because NMOS is much more noisy than the PMOS device. Furthermore, since the robustness is considered, PMOS oscillators are better, because only NBTI mechanism affects these structures and the degradation amount of NBTI is less compared to the HCI in the same aging period.

On the other hand, CMOS oscillators are the worst structures regarding the robustness due to combination effects of NBTI and HCI on the phase noise of these

Table 5.5. Performance comparison table of oscillators.

Structure	Drive Current	Voltage Supply	Phase Noise	Reliability
NMOS	2nd	1st	2nd	2nd
PMOS	2nd	1st	1st	1nd
CMOS	1st	2nd	3rd	3st

oscillators. Furthermore, phase noise analysis show that CMOS type oscillators shows the worst phase noise response. Actually, CMOS would be better than the NMOS, because the tail current of CMOS structures were chosen arbitrary. The assumption was that the negative resistance produced by differential part increased two times for CMOS oscillator, so the tail current should be reduced by half, however, simulation results illustrate that this assumption isn't accurate and the tail current for the optimum oscillation is obtained at higher values through some extra simulations($\approx$ 2 mA), but, the performance comparison was performed regarding 1.5 mA results. Furthermore, the conventional type oscillator (NMOS type) has an average performance regarding phase noise and reliability among all structures.

6. CONCLUSION AND FUTURE WORK

6.1. Conclusion

This study can be mainly summarized under three titles;

(i) Physical background and mathematical models of aging mechanisms occurring in CMOS circuits.

(ii) Design of several CMOS differential cross-coupled LC oscillator structures and phase noise analysis.

(iii) Aging analysis of oscillators and the aging effects on phase noise of the oscillators.

Four different degradation mechanisms causing aging in CMOS, Hot Carrier Injection in NMOS, Negative Bias Temperature Instability in PMOS, Time Dependent Dielectric Breakdown in both NMOS and PMOS, and Electromigration in metal interconnects, were examined at the first two parts of the study. A literature survey was performed and an overview including physical background and mathematical models of all of these phenomena was prepared to increase the comprehensibility of the next parts. Although all of these mechanisms were not explained in full detail because of complexity of each mechanism in itself, it is sufficient to understand the basics of aging in CMOS and perform reliability analyses. A CMOS LC oscillator design procedure was explained in detail at the next part of the study. Several oscillator architectures were designed and phase noise analyses were performed for all oscillator structures through both calculation and simulation. At the final part, aging analyses of these oscillators were performed and the results were discussed. As a summary of the results, aging cause degradation on the phase noise response of CMOS oscillators. In addition, PMOS oscillators are the less noisy and the most robust circuits against to aging, because it is only affected by NBTI and the effect of NBTI is less compared

to HCI. On the other hand, NMOS oscillators show an average performance while CMOS oscillators are the least robust circuits, because both NBTI and HCI degrades the phase noise performance of CMOS oscillator over time.

6.2. Future Work

Although circuit design against to aging problem is an individual study, some suggestions can be made. Firstly, the biasing part of the oscillator should be designed considering the aging because this component dominates the phase noise response of oscillators. For example, PMOS transistors can be used rather than NMOS because they are more robust. Another possible solution is using the mirror structures to produce the tail current. It was demonstrated that if the transistors at the mirror and they were exactly matched, aging effect would be less effective. On the other hand, as a general solution, using bigger transistors at the design process may decrease the negative effects of aging. All of these and the other possible solutions to design more robust circuits could be collected under a title and this could be a promising future work.

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