ULTRA-LOW POWER SAR ADC DESIGN

by

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Ms.c., Electrical and Electronics Engineering, University of Tabriz, 2012

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Doctor of Philosophy

Graduate Program in Electrical and Electronics Engineering
Boğaziçi University

2024

ACKNOWLEDGEMENTS

To my beloved family, especially to my mother, whose influence and encouragement have been the guiding light in every step I take.

I am profoundly thankful to Professor Günhan Dündar, my supervisor, and Professor Hakan Doğan, my co-supervisor. Their guidance and insight have been a constant source of inspiration and have driven me to achieve my best throughout this research.

I extend my sincere thanks to the members of my thesis committee: Prof. Arda Deniz Yalçınkaya, Assist. Prof. Ahmet Tekin, Assist. Prof. Okan Zafer Batur, and Assoc. Prof. Engin Afacan. Their feedback and support have been invaluable.

A special thank you to the members of BETA laboratory. Your friendly and invaluable support has made a significant impact on this work. I am grateful to Merve Albayrak, Zeynep Duygu Sutgol, and former BETA members Semih Ramazanoglu, Oguz Kagan Erden and many others. Additionally, I cherish the friendships I made during my time at Boğaziçi University. To Mehdi Ghorbani Hokmabad, Ata Sarrafinezhad, Alireza Ahmadi Asl, and Negin Kazemi, your unwavering help and companionship have been truly appreciated.

Lastly, I express my heartfelt gratitude to Selçuk Bayraktar for his generous financial support of the chip fabrication.

ABSTRACT

ULTRA-LOW POWER SAR ADC DESIGN

Analog-to-Digital Converters (ADCs) find applications in various fields. In portable applications such as the Internet of Things (IoT), power efficiency is a critical consideration. Deploying IoT devices in challenging environments introduces additional concerns, including reliability, the operating temperature range, and etc. ADCs typically serve at the front-end of an IoT device, playing a pivotal role in sensing various environmental parameters, such as temperature, pressure, and many others. The acquired data can then be processed with a Digital Signal Processor (DSP). Effectively tackling these challenges is crucial to transform theoretical concepts into tangible designs, ultimately enriching the overall user experience. Additionally, achieving high yield necessitates circuits that are robust in terms of Process, Voltage, and Temperature (PVT).

In this thesis, we develop two ultra-low-power Successive Approximation Register ADCs (SAR ADCs) suitable for IoT devices in harsh environments, such as the automotive sector. Operating at sampling frequencies of 100kHz and 1MHz with V_{DD} values of 0.7V and 1.2V, respectively, both ADCs demonstrate high robustness in the presence of PVT variations. Designed in the 65nm UMC CMOS process node, the ADC with a 0.7V supply voltage consumes only 1.55μW, while the ADC with V_{DD}=1.2V consumes 248μW. These developments contribute to the advancement of efficient and reliable ADCs for demanding IoT applications.

ÖZET

ULTRA DÜŞÜK GÜÇLÜ SAR ADC TASARIMI

Analogdan Dijital Dönüştürücüler (ADC'ler), çeşitli alanlarda uygulama bulmaktadır. Taşınabilir uygulamalarda, örneğin Nesnelerin İnterneti (IoT) gibi, güç verimliliği kritik bir düşünce haline gelmektedir. IoT cihazlarının zorlu ortamlarda kullanılması ek endişeleri beraberinde getirir, bunlar arasında güvenilirlik, işletme sıcaklık aralığı gibi konular yer almaktadır. ADC'ler genellikle bir IoT cihazının ön uçlarında hizmet verir, çeşitli çevresel parametreleri algılama konusunda kilit bir rol oynar, bunlar arasında sıcaklık, basınç ve diğer birçok parametre bulunmaktadır. Elde edilen veriler daha sonra bir Dijital Sinyal İşlemcisi (DSP) ile işlenebilir. Bu zorlukların etkili bir şekilde ele alınması, teorik kavramları somut tasarımlara dönüştürmek açısından önemlidir ve nihayetinde genel kullanıcı deneyimini zenginleştirmeye katkı sağlar. Ayrıca yüksek verimliliğe ulaşmak, süreç, voltaj ve sıcaklık (PVT) açısından sağlam devreler gerektirir.

Bu tezde, 100kHz ve 1MHz örnekleme frekanslarında çalışabilen ve sırasıyla 0.7V ve 1.2V V_{DD} değerlerine sahip iki ultra düşük güç SAR ADC (Sıralı Yaklaşım Kayıt ADC) geliştirmekteyiz. Her iki ADC de PVT değişimleri mevcutken yüksek sağlamlık sergilemektedir ve otomotiv sektörü gibi zorlu ortamlarda kullanıma uygun hale getirilmiştir. 65nm UMC CMOS işlem düğümünde tasarlanan 0.7V besleme voltajına sahip ADC, sadece 1.55µW güç tüketirken, V_{DD}=1.2V'ye sahip ADC 248µW tüketmektedir. Bu gelişmeler, talepkar IoT uygulamaları için etkili ve güvenilir ADC'lerin ilerlemesine katkıda bulunmaktadır.

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LIST OF SYMBOLS

C_u	Unit Capacitance
$F(.)$	Dawson Function
K	Boltzman Constant
V_{CM}	Common Mode Voltage
V_{REF}	Reference Voltage
V_T	Thermal Voltage
μ	Mobility
σ^2	Jitter Variance
$\mathcal{L}$	Phase Noise
$\Sigma\Delta$	Sigma Delta

LIST OF ACRONYMS/ABBREVIATIONS

ADC	Analog to Digital Converter
BSU	Bit Slice Unit
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
ENOB	Effective Number Of Bits
FoM	Figure of Merit
INL	Integral Non-Linearity
IoT	Internet of Things
PVT	Process Voltage Temperature
SAL	StrongArm Latch
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio

1. INTRODUCTION

Data converters serve as bridges between real-world signals and digital signal processing (DSP) units. Real-world signals, initially continuous-time continuous-amplitude signals, require conversion to the digital domain for processing by the DSP block. The analog-to-digital converter (ADC) plays a crucial role in facilitating this conversion. The digital outputs produced by the ADC undergo processing within the DSP unit before being converted back into an analog signal through a digital-to-analog converter (DAC). In Figure 1.1, the system-level block diagram illustrates the interaction of a general ADC with real-world signals [1]. Prior to entering the ADC, the analog input signal undergoes initial filtration to eliminate high-frequency components and prevent aliasing. The ADC then compares this signal to a reference signal, expressing its magnitude in relation to a binary number. This fundamental procedure is known as *quantization* or *quantizing*.

Various types of ADCs exist, mostly falling into categories such as Nyquist-rate (Flash, Pipeline, and SAR) and oversampled (Sigma-Delta) ADCs. Within each of these categories, different architectures can be chosen based on the intended application and required specifications. In general, ADCs encompass a broad spectrum of characteristics, spanning from very low to very high bandwidth and from low to high resolution. This diversity caters to a multitude of applications across fields such as biomedical applications, audio/video signal processing, communication, and etc.

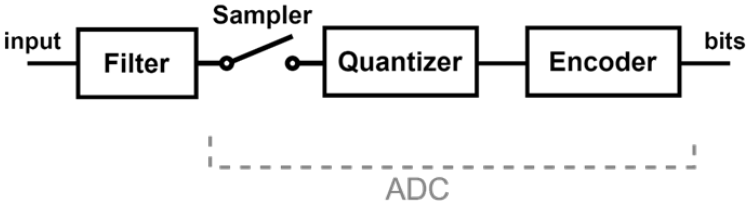


Figure 1.1. A general use of ADC in a system

ADCs possess three key attributes that define their utility: conversion speed, resolution, and power consumption.

- Resolution: Number of quantization "bits" that the ADC employs, dictating measurement precision.
- Sampling Rate: Measurement frequency influencing the ADC's effective signal bandwidth.
- Power Consumption: Amount of power consumed during the ADC operation.

1.1. ADC Kinds

ADCs can generally be classified into several architectures, with four fundamental: Flash, Pipeline, Sigma-Delta, and SAR (Successive Approximation Register). Each architecture is ideally suited for a specific trade-off between bandwidth and resolution.

Flash: The flash ADC architecture is most suitable for high-bandwidth, low to medium resolution applications. A basic example of this architecture is illustrated in Figure 1.2. To complete the entire conversion in one clock cycle, the traditional flash architecture employs 2^N -1 comparators in parallel, each referencing a distinct voltage from a reference ladder. The maximum sampling rate of the converter is determined by the comparator's aperture time. The outputs of all the comparators collectively form a thermometer-coded word, subsequently converted into binary. While flash ADCs excel in lower-resolution applications, the exponential relationship between increasing resolution and the number of comparators is demanding. Moreover, achieving a stable reference ladder at high speeds, especially with resolutions equal to or surpassing the overall converter capability, presents substantial challenges. This limitation constrains the extension of the flash architecture's resolution beyond the range of 6-7 bits [2].

Pipeline: The pipeline ADC architecture is best suited for applications requiring moderate to medium resolution and medium to high bandwidth. A conceptual diagram is shown in Figure 1.3. Although it may not achieve the same bandwidth as flash ADCs, the pipeline ADC achieves higher resolution by dividing the conversion process

into multiple stages that operate sequentially; the output of one stage serves as the input to the next [3]. Once the input is sampled by the first stage of the ADC and the initial partial conversion is performed, the residue (or "leftover" un-quantized input) is amplified back up to the initial voltage range of the input. It is then further quantized with subsequent stages using sub-ADCs and multiplying DACs with high-gain residue amplifiers.

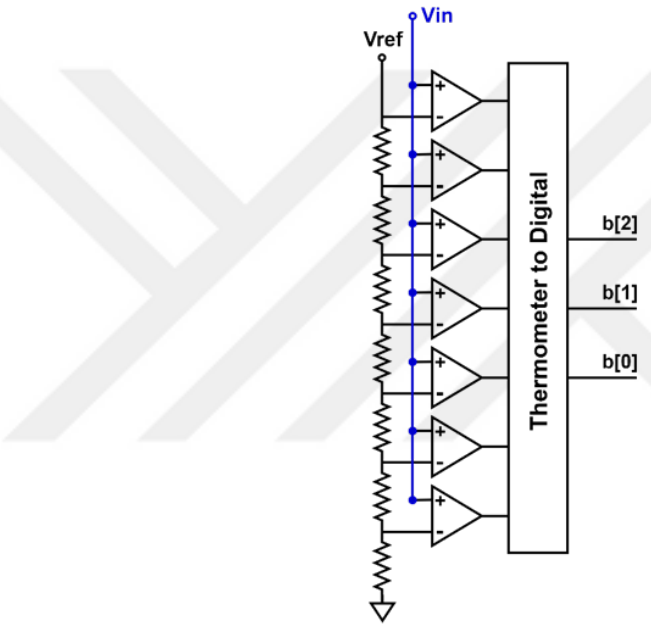


Figure 1.2. A general 3-bit flash ADC

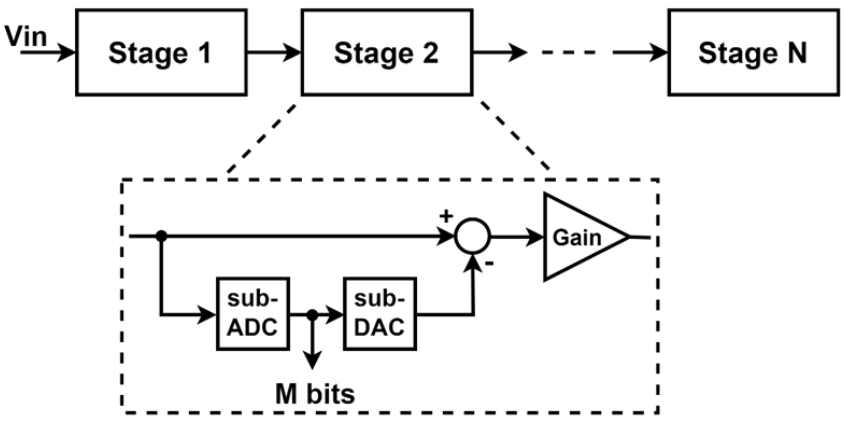


Figure 1.3. A general pipeline ADC

The pipelining process can be repeated as many times as desired, but the total resolution is limited by the accuracy of the first stage. Even if the first stage only quantizes the initial 3 most significant bits (MSBs) of a 10-bit converter, it still needs to be 10-bit accurate. Pipeline ADCs are commonly chosen for systems requiring 12 to 16 bits with high bandwidth. While parallelism is the constraining factor for flash ADCs, the finite gain error from each stage's residue amplifier and the accuracy of the first stage are the primary challenges in designing pipeline ADCs.

Sigma-Delta: The Sigma-Delta $\Sigma\Delta$ architecture achieves the highest resolution among all converter types by employing oversampling and noise shaping. Oversampling sacrifices converter bandwidth for increased resolution. In contrast to Nyquist ADC architectures, where the quantization bandwidth is half the sampling rate $f_s/2$, $\Sigma\Delta$ ADCs provide only a limited usable quantization bandwidth, either at DC (low-pass $\Sigma\Delta$) or at some intermediate frequency below the sampling clock (band pass $\Sigma\Delta$). Noise shaping effectively "pushes" the quantization noise and other non-linearities outside the conversion bandwidth of interest [1]. A block diagram of a first-order $\Sigma\Delta$ modulator is depicted in Figure 1.4. With a high oversampling ratio (OSR), it becomes possible to achieve +16 bits of resolution even with a 1-bit quantizer. While increasing loop order or quantizer resolution improves the theoretical performance of $\Sigma\Delta$ ADCs, it is important to note that noise shaping primarily affects blocks in the forward path, making the performance of the feedback DAC a limiting factor. Additionally, as loop order increases, the performance of integrators becomes progressively challenging, with considerations for finite gain error, slew rate, and dynamic range.

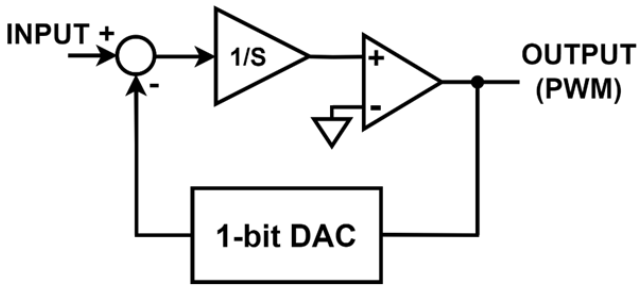


Figure 1.4. A 1st order 1-bit $\Sigma\Delta$ modulator

SAR: The Successive Approximation Register (SAR) architecture derives its name from the utilization of a DAC in a feedback loop, conducting a recursive search on the input voltage after sampling. This iterative process is commonly referred to as successive approximation [3]. Figure 1.5 presents a simplified block diagram of a single-ended SAR ADC, and Figure 1.6 depicts a 3-bit example of a binary-weighted SAR algorithm [4]. This algorithm is referred to as "binary weighted" because it halves the search space between each successive step.

In binary logic, each step corresponds to a decreasing power of two. Initially, the input signal (depicted by the red line) is compared against a DAC voltage of $V_{REF}/2$. The result of this comparison yields either a "true" (1) or "false" (0) outcome, indicating whether $V_{IN} > V_{REF}/2$. Subsequently, the second decision either adds or subtracts $1/4{\times}V_{REF}$ to the DAC's previous value, contingent upon the result of the first decision. Given that the first result is a "1", $1/4{\times}V_{REF}$ is added, leading to a comparison between V_{IN} and $3/4{\times}V_{REF}$. This comparison concludes with a logical "false" (0), affirming that $V_{IN} < 3/4{\times}V_{REF}$. Moving on to the third and final comparison, the search space is once again reduced by a power of two, resulting in a deduction of $1/8{\times}V_{REF}$ from the DAC value. This final comparison involves V_{IN} and $5/8{\times}V_{REF}$, culminating in another "0" result from the comparator. The outcome of this 3-bit conversion is an output code of "100". This code, within the 3-bit code space of "000" to "111", is the 5th out of 8 possible codes.

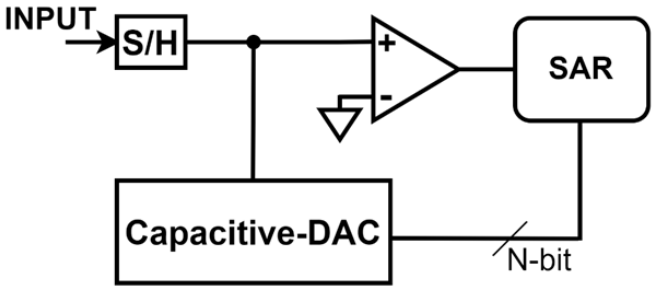


Figure 1.5. A general SAR ADC

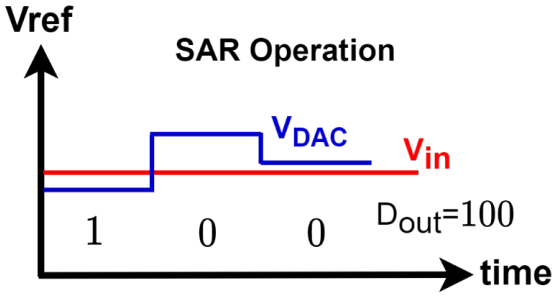


Figure 1.6. SAR operation with a 3-bit binary-weighted DAC

1.2. Methodology

In the last decade, SAR ADCs have attracted significant attention, primarily due to their inherently scalable and predominantly digital architecture. However, their popularity extends beyond just their architecture. Notably, several key innovations have further refined the SAR architecture, evolving into widely adopted design techniques. Some of these advancements can be categorized into the following areas of improvement:

Energy-efficient DAC switching: The method by which the capacitors in the DAC are switched, plays a crucial role in determining how a successive approximation is carried out during a SAR conversion. While various approaches can lead to a linear transfer function, the selection of the DAC switching scheme significantly impacts power consumption [5–9]. Figure 1.7 shows a conventional 10-bit fully differential SAR ADC. Considering only the positive side of the DAC, with sampling phase enabled, V_{IP} charges the bottom plates of the capacitors, while the top plates reset to the common-mode voltage V_{CM}. Following this, the largest capacitor, C_1, is switched to V_{REF}, with the remaining capacitors switched to ground. The comparator then executes the initial comparison. If V_{IP} surpasses V_{IN}, the most significant bit (MSB) B_1 becomes 1; otherwise, it is 0, and the largest capacitor is reconnected to ground. The process repeats with the second-largest capacitor, C_2, being switched to V_{REF}, and the comparator performing another comparison. This sequence continues until the

least significant bit (LSB) is determined. Despite the simplicity and intuitiveness of the trial-and-error search procedure, it is not an energy-efficient switching scheme [9]. In the monotonic switching scheme illustrated in Figure 1.8, the input signal is sampled on the top plates while, simultaneously, the bottom plates of the capacitors are reset to V_{REF}. Subsequently, once the ADC deactivates the sampling switches, the comparator directly executes the first comparison without the need for capacitor switching. Based on the comparator output, the largest capacitor C_1, positioned on the higher voltage potential side, is switched to ground, while the other capacitor on the lower side remains unchanged. This procedure repeats iteratively until the determination of the least significant bit. Since, each bit cycle involves only one capacitor switch, the charge transfer within the capacitive DAC network is reduced, resulting in smaller power dissipation. For an N-bit ADC, the number of unit capacitors in the capacitor array amount to 2^N-1, a half of the conventional approach in Figure 1.7.

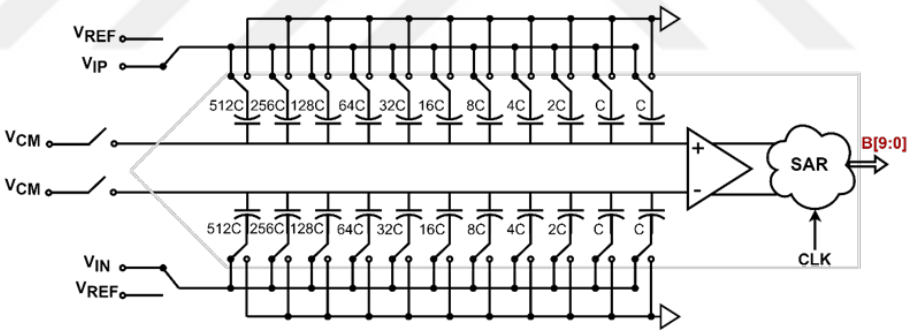


Figure 1.7. SAR ADC: conventional DAC switching method

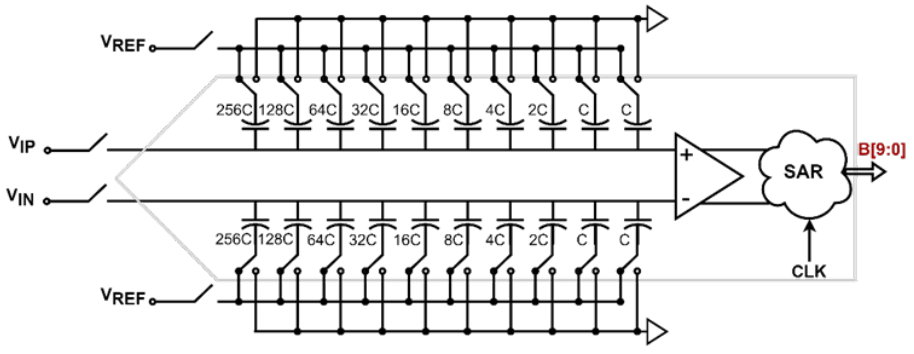


Figure 1.8. SAR ADC: monotonic DAC switching method

Tunable comparator performance: In conventional SAR ADCs, comparators are so designed to maintain the input-referred noise voltage below half of the LSB size. The primary objective is to minimize noise while adhering to specified power consumption levels [8]. In a study conducted by Harpe [10], a tunable comparator is introduced, providing the flexibility to adjust internal capacitance and tail current. This adjustability enables targeted enhancement of the input-referred noise, depending on the specific SAR decisions being made. Harpe's approach leads to a significant 50% reduction in comparator power, allowing for lower noise performance during the initial N-2 trials. Subsequently, in the final three comparisons, which include an additional error-checking decision, the noise performance is intentionally heightened.

Asynchronous operation: SAR ADCs are distinguished by their system clock frequency rather than their sampling clock frequency. The system clock acts as the trigger for each successive step in the SAR cycle and is usually a multiple of the effective sampling clock. For instance, if a SAR ADC requires N system clock periods to complete a conversion, the sampling rate f_S can be expressed as f_S/N. In SAR ADCs, consistent step durations ensure that the comparator has equal time for each decision-making process. Nevertheless, it is important to note that regenerative comparators, commonly employed in SAR ADCs, show an exponential relationship between clock-to-output time and input voltage. This aspect is not fully capitalized upon in SARs using a fixed system clock. By aligning the entire timing of the SAR ADC around the worst-case comparator input voltage of LSB/2, valuable time is often lost. This time could be harnessed to improve the sampling rate and input bandwidth. A strategy introduced in [11] involves allowing the comparator to "clock itself," resulting in increased speed. This concept has been widely embraced and has found its way into many recent SAR ADC designs. Considering the concept of metastability, asynchronous design also outperforms its synchronous counterpart [12, 13]. However, care should be taken in allocating proper time for settling of the DACs.

Non-binary radix conversion: The interplay between conversion speed and DAC settling time is significantly refined in non-binary radix SAR approach [14]. Most SAR ADCs adopt groupings of capacitors with a radix of 2, resulting in binary-weighted groupings. Consequently, the search space diminishes by half in each SAR trial. However, in non-binary radix SARs, a radix less than 2 is utilized. As a result, the search space in each SAR trial is less than half. This deviation from halving the search space implies that part of the prior trial's search space carries over to the subsequent decision.

Others: Error-correction via extra decisions [15, 16], residue shaping [17], dithering [18], time-domain comparison [19], and utilization of tunable capacitors [20] to shift the noise outside of the desired frequency band are some of the existing techniques in design of SAR ADCs.

The objective of this thesis is to contribute to the ongoing refinement of the SAR architecture and explore innovative circuit design techniques. The upcoming sections of the thesis are outlined as follows:

Chapter 2 delves into the developed SAR ADC design, introducing a novel resetting technique aimed at further diminishing power consumption. Two ADCs are designed, with the first sampled at 100kHz and a 0.7V supply voltage, and the second sampled at 1MHz with a 1.2V supply voltage. In chapter 3, the focus shifts to the design of sample and hold and BSU as ADC's building blocks. Chapter 4 covers the design of comparators. In chapter 5, a novel insight is presented to deal with the jitter in the sampling clocks. Chapter 6 is devoted to the performance of the ADCs. This chapter presents simulation results. Chapter 7 concludes the thesis.

2. PROPOSED SAR ADC

With evolution of CMOS technology, Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) can go well above several hundred MS/s and still provide outstanding energy-efficiency. Among the building blocks of a SAR ADC, the capacitive DAC used to consume a significant portion of the total power, primarily influenced by the switching scheme and the total capacitance of the capacitor array which is usually used as a sampling capacitor in a top plate sampling structure. Thanks to technology scaling, using small unit capacitors with C_u as small as 0.25fF, sampling capacitance has decreased to 280fF for a 10-bit 80kHz ADC [21]. However, noise and matching requirements complicate the design of ADCs with more than 10bits using such small unit capacitors. For reduction of switching energy, various switching schemes have been proposed to improve the power efficiency. The monotonic scheme saves up to 81% of the average energy compared with the conventional method [9]. The average switching energy in conventional scheme, the monotonic scheme, the V_{CM}-based scheme, the switching-back scheme, and merged capacitor switching (MCS) scheme in a 10-bit ADC are $1363.3{CV_{REF}}^2$, $255.5{CV_{REF}}^2$, $170.2{CV_{REF}}^2$, $127.5{CV_{REF}}^2$ and $84.7{CV_{REF}}^2$, respectively. The improvements made to the DAC switching scheme, as a consequence, have resulted in the power consumption of other blocks, particularly the comparator, becoming nearly comparable to the overall power of the ADC.

In this thesis, a reset-efficient hybrid switching algorithm for the DAC design is proposed. The hybrid switching method, initially introduced in [22], has substantially decreased the switching energy to $15.8{CV_{REF}}^2$, resulting in a 93.8% reduction on average compared to the monotonic scheme. However, this technique encounters reset energy, nearly double its switching energy, at $31.2{CV_{REF}}^2$. Moreover, the conventional hybrid scheme primarily draws current from the V_{CM} reference during either the conversion cycle or the reset time slot. This may introduce offset in the V_{CM} reference. With the developed technique, the reset energy in the conventional hybrid switching is reduced by 26%. This reduction directly alleviates perturbations in the V_{CM} reference, making it robust and appealing for the design of ultra-low-power and $>$ 10-bit ADCs.

2.1. Hybrid DAC Switching Method

The conventional binary-weighted hybrid switching scheme for a 4-bit DAC is illustrated in Figure 2.1. In the sampling phase, the bottom-plates of the capacitors are initially loaded with the sequence of [V_{CM}, 0, 0], where V_{CM}=V_{REF}/2. Simultaneously, the top plates sample the differential inputs V_{IP} and V_{IN}. During the conversion phase, the top plates of the capacitors are disconnected from the inputs, and with the first rising edge of the comparator clock, the initial comparison is performed directly and the MSB is obtained with zero switching energy. If $V_{IP} > V_{IN}$, MSB equals '1'. In this case, the voltage on all capacitors at the positive side remains the same, while the voltage on the negative side increases by V_{CM} (by switching V_{CM} to V_{REF} and GND to V_{CM}). Conversely, if $V_{IP} < V_{IN}$, MSB equals '0', and the capacitors at the negative side remain unchanged, while the voltage on the positive side increases by V_{CM} in the same manner. Since the voltage on the bottom-plates of the capacitors increases by the same value, here V_{CM}, the DAC consumes "zero" energy to move to the next state.

When the second comparison cycle is triggered, the MSB-1 bit is determined. In case $V_P > V_N$, MSB-1 equals '1' and the voltage on the positive side drops down by V_{CM}. As a result, the voltage on positive side decreases by V_{REF}/4 for the next comparison. V_P and V_N are the positive and negative input pins of the comparator, respectively. The same procedure occurs if $V_P < V_N$. Upon the third rising edge of the comparator, the MSB-2 is derived again with no energy consumed. From this state onward, the voltage on the bottom plate of the next-right capacitor increases by V_{CM}, in response to the preceding output bit, and the DAC begins to consume energy. With the next rising edge of the comparator, the last bit (LSB) is attained, and the DAC returns to the sampling phase.

The efficiency of this scheme during conversion cycles lies in the fact that, in conventional binary-weighted SAR ADCs, the DAC dissipates approximately 87.5% of its switching energy to detect the first three bits. However, due to the absence of energy consumption during the first three comparison cycles in hybrid switching, this scheme demonstrates remarkable energy efficiency, outperforming many existing schemes.

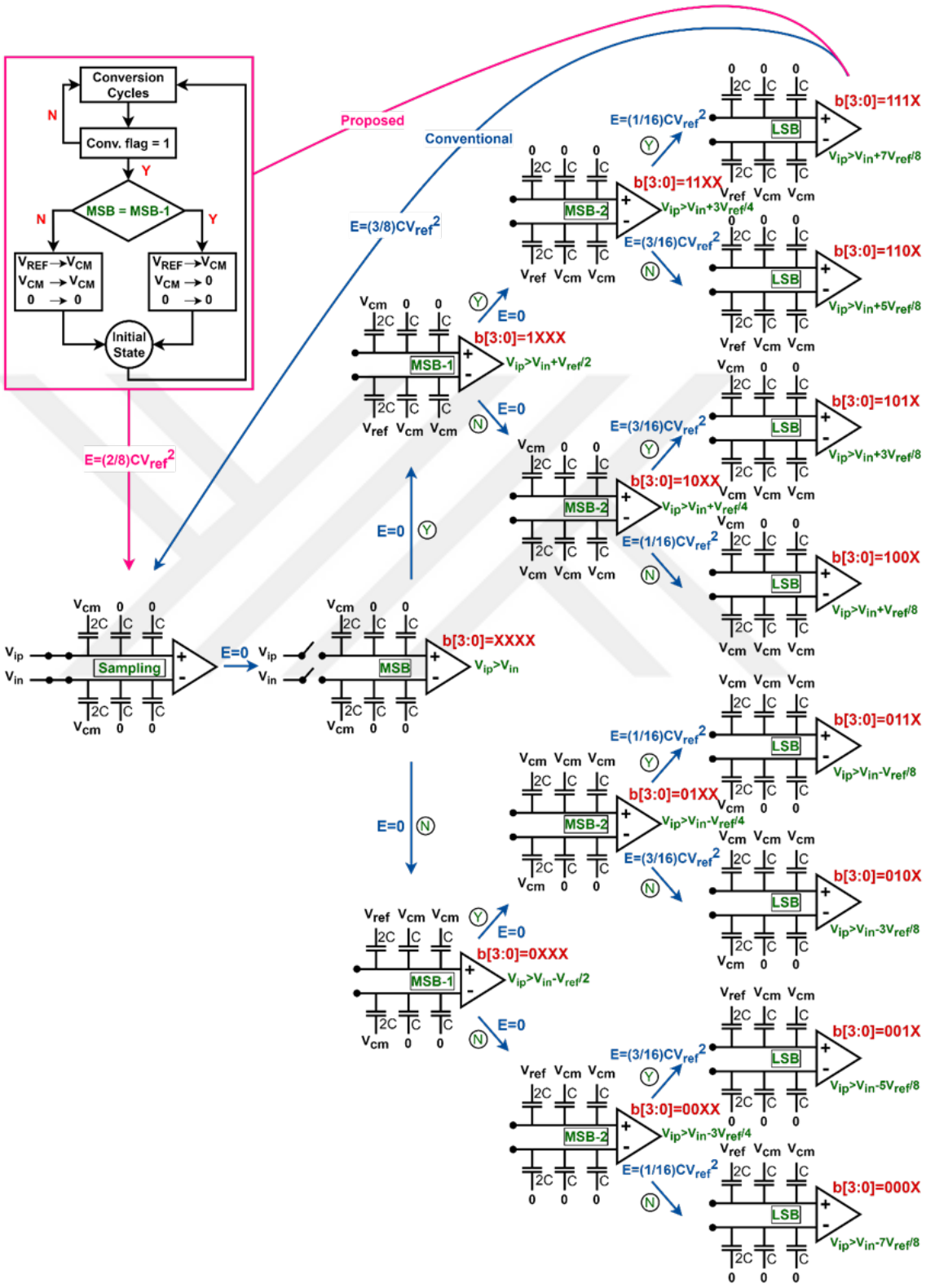


Figure 2.1. 4-bits hybrid switching DAC with/without proposed reset-efficient path

Nevertheless, as previously stated, this technique suffers from reset energy, which is twice the conversion switching energy. Another significant aspect of the hybrid scheme is that it reduces the area by 50% compared to its monotonic counterpart. It should also be noted that, in the hybrid switching scheme, the common mode input voltage of the comparator varies during conversion. This variation can compromise the linearity of the ADC and requires careful design considerations of comparator. Table 2.1 compares the switching energy of the hybrid scheme with some other techniques.

Table 2.1. Switching energy performance

Switching scheme	avg. energy CV^2_{REF}	avg. energy saving	avg. reset energy CV^2_{REF}	total energy saving	area saving
Monotonic	255.5	Ref.	0	Ref.	Ref.
VCM-based	170.2	33.4%	0	33.4%	0
Switching-back	127.5	50.1%	128	0	0
MCS	84.7	66.7%	0	66.7%	0
Hybrid	15.8	93.8%	31.2	81.6%	50%

2.2. Proposed Reset-Efficient Switching Scheme

The issue of high reset energy in the conventional hybrid scheme arises from the necessity to load the bottom plates of the capacitors with the sequence [V_{CM}, 0, 0, . . . , 0] in every cycle. In the proposed reset method, the DAC capacitors are not immediately loaded with that sequence. Instead, they first enter an intermediate state where the capacitors are charged based on the state of the MSB and MSB-1 bits. On the next rising edge of the clock, they subsequently transition to the initial state of [V_{CM}, 0, 0, . . .]. The efficient resetting process is highlighted in Figure 2.1. When the conversion flag equals '1', signifying the completion of the conversion for one sampled data, the following steps occur:

1. If MSB equals MSB-1, any V_{REF} at the bottom plates of any capacitor, both the positive and negative sides, drops down to V_{CM}, and all others are reset to ground.

2. If MSB is not equal to MSB-1, then V_{REF} drops down to V_{CM}, and the voltage on bottom-plates of other capacitors remain unchanged.

To further elaborate on the states of the DAC, we assume that the output code follows the pattern 110x ('x' being either '1' or '0') represented in Figure 2.2. As the last bit is attained in state 4, the DAC returns to the sampling phase and consumes,

$$E_r = -2CV_{CM}\left[\left(-\frac{V_{CM}}{2} - \frac{V_{CM}}{4}\right) + \left(-\frac{V_{CM}}{2} + \frac{V_{REF}}{4}\right)\right] = \frac{3}{8}CV_{REF}^2. \tag{2.1}$$

In the proposed technique, schematically illustrated in Figure 2.3 using the same example where the output code was 110X), since MSB and MSB-1 are equal, the initial action is for V_{REF} to reduce to V_{CM}, while all other capacitors are connected to ground. Afterwards, the subsequent sampling phase will take place. This way, the energy drawn from the DAC is,

$$E_{r1} = -2CV_{CM}\left(\frac{V_{CM}}{2} - V_{CM} - \left(\frac{3V_{REF}}{4} - V_{REF}\right)\right) = 0 \tag{2.2}$$

$$E_{r2} = -2CV_{CM}\left(\frac{V_{CM}}{2} - V_{CM} - 0\right) = CV_{CM}^2 \tag{2.3}$$

$$E_{rt} = E_{r1} + E_{r2} = CV_{CM}^2 = \frac{1}{4}CV_{REF}^2. \tag{2.4}$$

Comparing equation (2.4) with equation (2.1), a 33.3% reduction in reset energy is achieved through this transition.

To ensure a fair comparison with the original hybrid scheme [22], the behavioral simulation of the reset-efficient scheme is carried out in MATLAB for a 10-bit DAC.

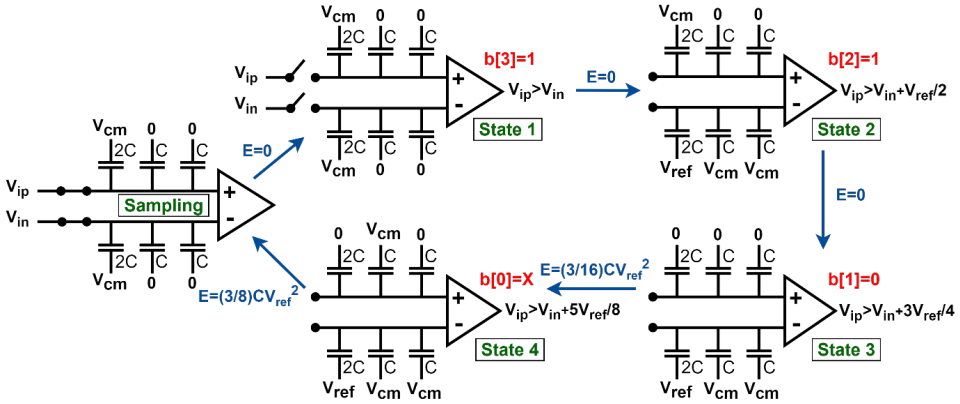


Figure 2.2. Conventional hybrid DAC when the output is 110X

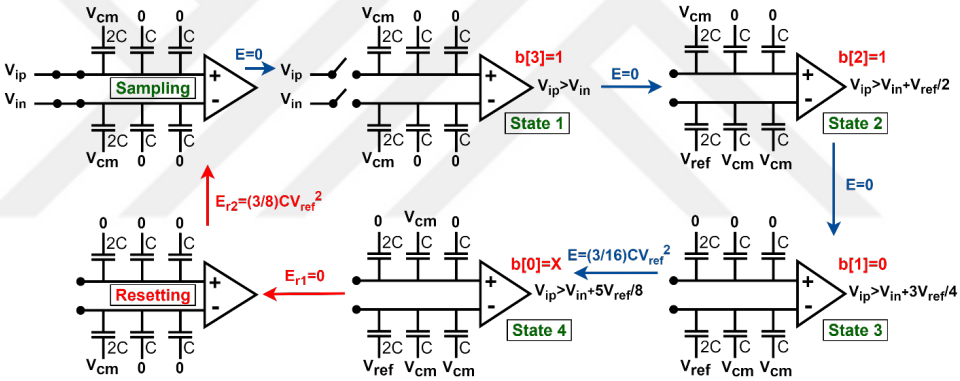


Figure 2.3. Reset-Efficient hybrid DAC when the output is 110X

As shown in Fig. 2.4, the reset energy in the proposed method varies across the complete range of output codes and maintains an average lower than that of [22]. This results in an overall reduction in the DAC's switching energy. The effectiveness of the proposed reset method on the DAC's energy consumption is further evident in Table 2.2. In ultra-low power design, V_{CM} is usually generated using a voltage divider [11]. Due to the current drawn from the V_{CM} reference, this voltage can exhibit variations. It is crucial to maintain the average deviation to be less than one LSB for better performance. With the proposed method, the average energy drawn from V_{CM} is reduced by 26%. This reduction contributes to easing the design of the V_{CM} generator.

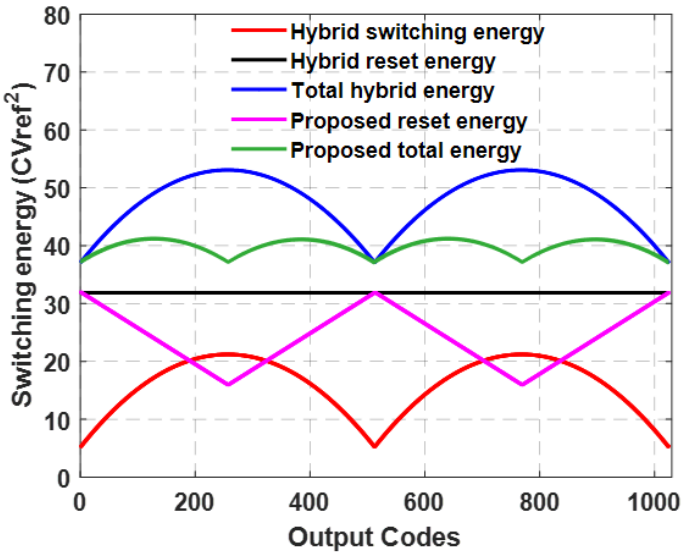


Figure 2.4. Energy consumption of the conventional and the proposed DAC

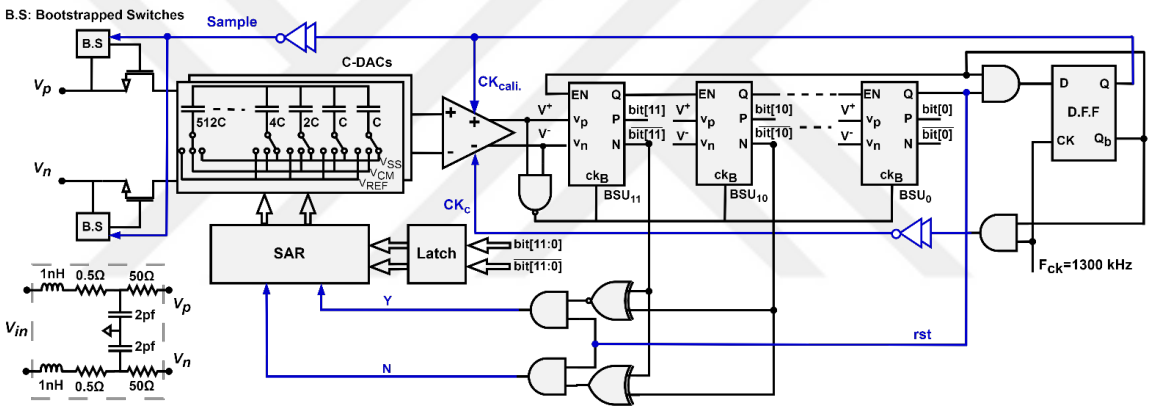
Table 2.2. Performance summary of the DAC switching schemes

switching method	avg. energy (CV^2_{ref})	avg. reset energy	reset energy saving	tot. energy (CV^2_{ref})	tot. energy saving
hybrid [1]	15.8	31.2	reference	47	reference
proposed	15.8	23.2	26%	39	17%

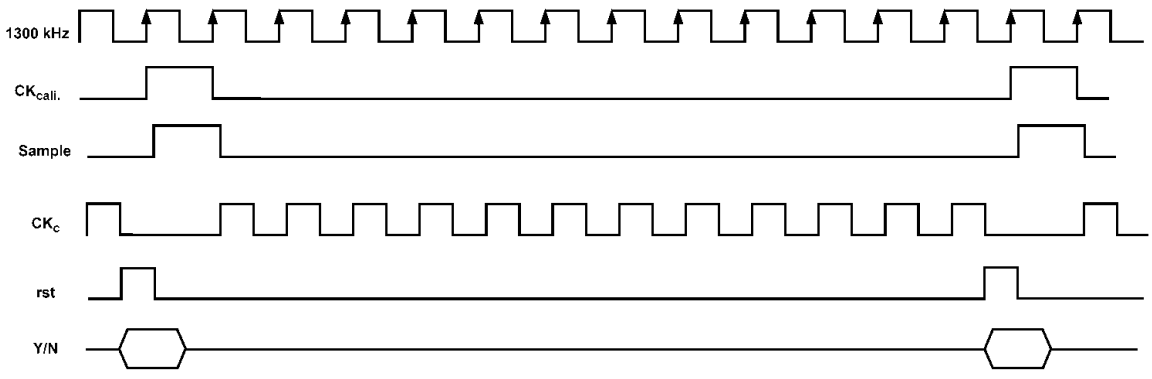
2.3. The Structure of the Proposed ADC

Two ultra-low-power ADCs are designed in this study: one with a V_{DD} of 0.7V sampled at 100kHz and another with a 1.2V supply voltage sampled at 1MHz. Both ADCs exhibit high robustness to Process, Voltage, and Temperature (PVT) variations. The synchronous SAR ADC, featuring the proposed reset-efficient technique, is illustrated in Figure 2.5(a), and its corresponding timing diagram is provided in Figure 2.5(b). This architectural design is employed for both ADCs, however, some of their building blocks differ. The input signal passes through a network comprising a 50Ω internal resistance, a 1nH inductor simulating wire bonding, and a 2pF capacitor representing ESD parasitic effects.

For a 12-bit and 100kS/s ADC, an external clock with a frequency of 1.3MHz governs the sampling and conversion processes. Upon the rising edge of the clock, the input signal is sampled on the capacitive DACs (C-DAC), which also serve as the sampling capacitors, through bootstrapped switches. The sampling phase, lasting one clock cycle, is initiated at intervals of 10µsec. Simultaneously, the inputs of the comparator are disconnected from the DACs, and the comparator undergoes calibration over a duration equivalent to the sampling phase (770nsec). Subsequent clock cycle reconnects the comparator inputs to the DACs, concluding the sampling phase. In the meantime, the sampled data undergoes comparison, and MSB is obtained.



(a)



(b)

Figure 2.5. Proposed SAR ADC (a) the structure and (b) timing diagram

To ensure proper functionality, slight delays are introduced in the sampling and the comparator clocking signal. With each rising edge of the comparator clock, the output bit is determined, initiating the SAR algorithm. The algorithm iteratively settles one of the DACs with a new voltage, progressively approaching the other one. This process continues until all 12 bits are obtained. On the falling edge of the 12th comparator clock, the reset signal *rst*, associated with the signal Q in the last Bit Slice Unit (BSU_0), is activated and it lasts for half a cycle, $\sim 385nsec$. Immediately after the activation of the *rst* signal, the DACs are pre-reset based on the states of the MSB and MSB-1. Following this, the sampling phase begins and the comparator undergoes calibration while disconnected from the DACs. This cyclic process of activation, resetting, and calibration continues consistently, in accordance with the predefined operational sequence.

For the second ADC design, the external clock frequency is 13MHz. Consequently, the duration of the sampling phase and calibration phase of the comparator are both equal to 77nsec. The analysis and design of the building blocks for both ADCs will be addressed in the subsequent chapters.

3. SAMPLE AND HOLD AND BSU DESIGN

Two of the ADC's building blocks, sample and hold (S/H) and bit-slice-unit (BSU), are analyzed and designed in this chapter.

3.1. Sample and Hold

Sampling of the time-varying input signal typically marks the initial stage in the design of SAR A-to-D converters. The linearity of the frontend S/H circuit significantly influences the overall performance of the ADC [23]. While a single MOS transistor can serve as a sampler, it often contends with imperfections such as charge injection, clock-feedthrough, non-constant on-resistance, and leakage current. To mitigate these issues, a CMOS switch, comprising an NMOS in parallel with a PMOS, can be employed for sampling purposes, making charge injection and clock-feedthrough less severe. Nevertheless, the non-linear signal-dependent on-resistance of the switch still introduces harmonic distortion.

In addressing the aforementioned challenges, a bootstrapped switch was introduced in [24] and later modified in [25] for Sigma-Delta modulators. With the bootstrapped switch, the gate-source voltage of the sampling transistor is fixed to a value approximately equal to the supply voltage. This reduction in on-resistance modulation enhances the linearity of the S/H. Additionally, channel charge injection error becomes a constant value, treated simply as an offset.

In modern CMOS technology, although the speed of the sampling switches is increased, the adverse effect of leakage current persists and limits the linearity of bootstrapped sampling switches, especially in low-speed paradigms. Despite several proposed methods to further improve linearity, they often suffer from either increased area [26] or design complexity [27].

3.1.1. Conventional Bootstrapped Switch

The conventional bootstrapped sampling switch is depicted in Figure 3.1(a), where "in" represents the input signal being sampled, and "out" is the output node connected to the capacitor array of the DAC, denoted as C_L. When the sampling clock is '0' (ϕ=0 and ϕ_b=1), M_5 and M_6 pull node V_a to ground, and the sampling switch M_1 is off. In this state, capacitor C_S is charged by the current passing through M_3 and M_4 until it reaches the supply voltage V_{DD}. Meanwhile, M_{10} is turned off by M_7, and V_a is isolated from the voltage over C_S, V_b. If the sampling clock goes high, M_4 turns off, and M_8 connects the gate of M_{10} to the bottom plate of C_S. As a result, M_{10} turns on, connecting the top plate of C_S to the gate of the sampling switch M_1 through M_{10}, and the bottom plate is connected to the source of M_1 through M_2. This way, the gate-source voltage of the sampling switch M_1 is fixed to V_{DD}, generating a voltage close to V_{in}+V_{DD} at node V_a [23]. A fixed V_{GS} greatly improves linearity; however, modulation of the input voltage into the on-resistance through the threshold voltage V_{TH} still produces harmonic distortions. Charge injection noise also has a V_{in}-dependent term that worsens linearity. The bulk switching technique could be used to solve the problem [28], but care should be taken into consideration that the source–body and drain–body junctions of the main switch will remain off. Clock feedthrough error is usually a constant value. However, since the rising edge of the bootstrapped clock phase depends on V_{in}, there is a second-order signal-dependent clock feedthrough term. A cross-connected capacitance is introduced in [29] to alleviate this noise.

Another issue concerning the conventional bootstrapped switch is the leakage current. When a transistor is in its off state, a small current pass through its terminals. This current is directly proportional to the area of the transistor [30],

$$I_{off} = KWe^{-V_{TH}/V_T}\left(1 - e^{-V_{DS}/V_T}\right), \tag{3.1}$$

where V_{DS} is the drain-source voltage, V_T is the thermal voltage, and K is a constant. The switch leakage significantly affects the S/H circuit performance in low-speed SAR

ADCs. Considering an N-bit ADC, during the hold mode, the voltage change, ΔV, on the sampling capacitor C_L caused by the leakage current $I_{leakage}$ is given as $\Delta V = I_{leakage} / (2F_S.C_L)$, where F_S is the sampling rate of the ADC. The least-significant-bit (LSB) of the N-bit ADC is defined as LSB=$V_{REF}/2^N$, in which V_{REF} is the reference voltage. Assuming $\Delta V <$ (LSB/2) is the condition under which the ADC resolution is not affected by the leakage current, we have [31],

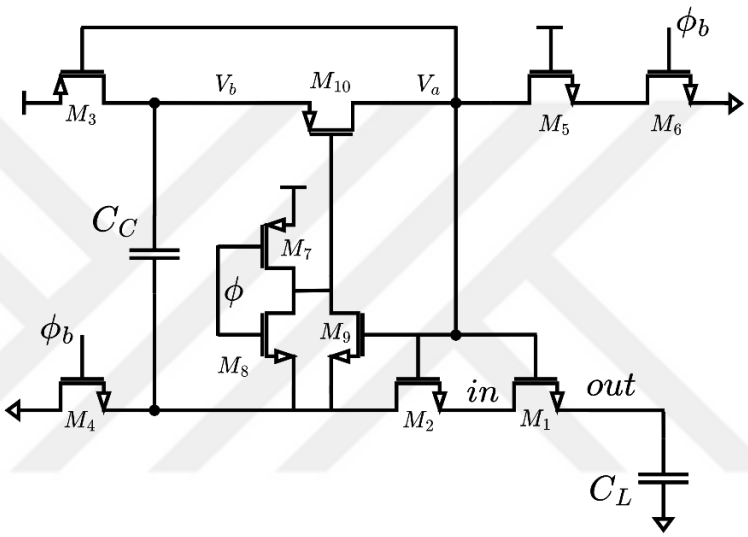
$$I_{\text{leakage}} < \frac{V_{\text{ref}}}{2^N} F_S C_L. \tag{3.2}$$

Considering equation (3.2), low leakage current becomes crucial in the case of high-resolution, low sampling rate, and a small on-chip sampling capacitor. To address this issue, two sampling switches, as depicted in Figure 3.1(b), are connected in series. With the stacked structure, the leakage current is significantly reduced [32]. According to equation (3.1), in addition to being temperature-dependent, the off current is also an exponential function of V_{DS}. The drain-source voltage of a sampling switch in an S/H circuit, at the hold mode, is a function of the time-varying V_{in}. In a SAR ADC, V_{out} is also changing due to the conversion process. This makes the leakage current an input-output dependent value and deteriorates switch linearity, especially in modern CMOS technology. Simulation results represented in Figure 3.2 show that the stacked topology further isolates input and output voltages, attenuating the dependency to some extent. Figure 3.3 shows the FFT results of both switches with $f_s = 1MHz$, $f_{in} \sim$ Nyquist, $C_L = 13pF$, and $V_{DD} = 1.2V$ at ff corner with temperature of +125°C. The Signal to Noise and Distortion Ratio (SNDR) and Spurious Free Dynamic Range (SFDR) are increased by 10dB and 9dB, respectively, in switch type II compared to the conventional switch type I.

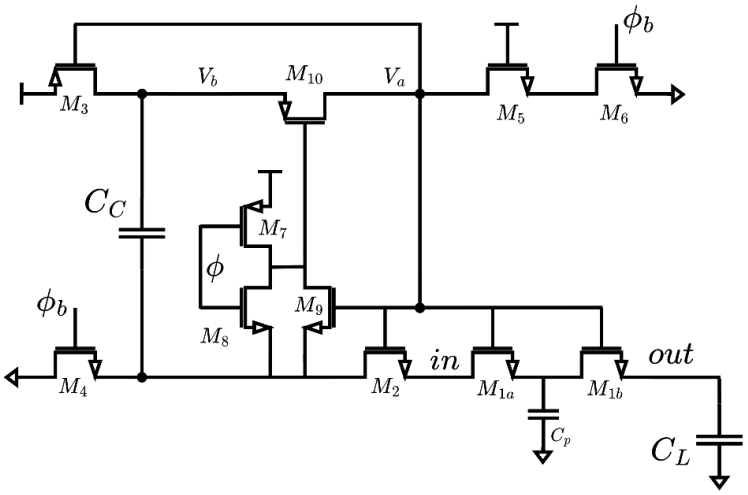
It is worth noting that two identical MOS transistors configured in series are equivalent to a single MOS transistor with the length doubled. Using a single MOS with the length being doubled instead of stacked configuration would not benefit in reduction of leakage current. This is due to the fact that, as equation (3.1) reveals, a

single MOS still experiences a full V_{DS} change. In addition, with length being doubled, the threshold voltage V_{TH} will decrease, making the leakage current more severe.

As another remedy to minimize the leakage current, the gate of the sampling switches can be connected to a negative voltage [11]. This increases the threshold voltage in equation (3.1) and makes the circuit more effective in reducing off-leakage.



(a)



(b)

Figure 3.1. Bootstrapped switch (a) type I (b) type II

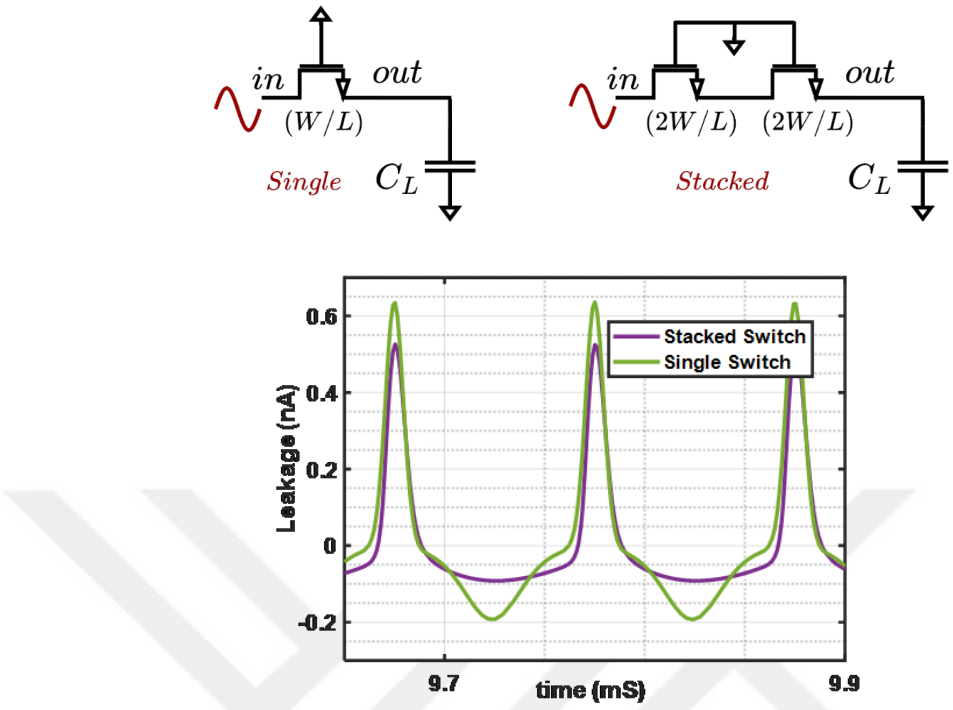


Figure 3.2. Leakage current in single and stacked transistors

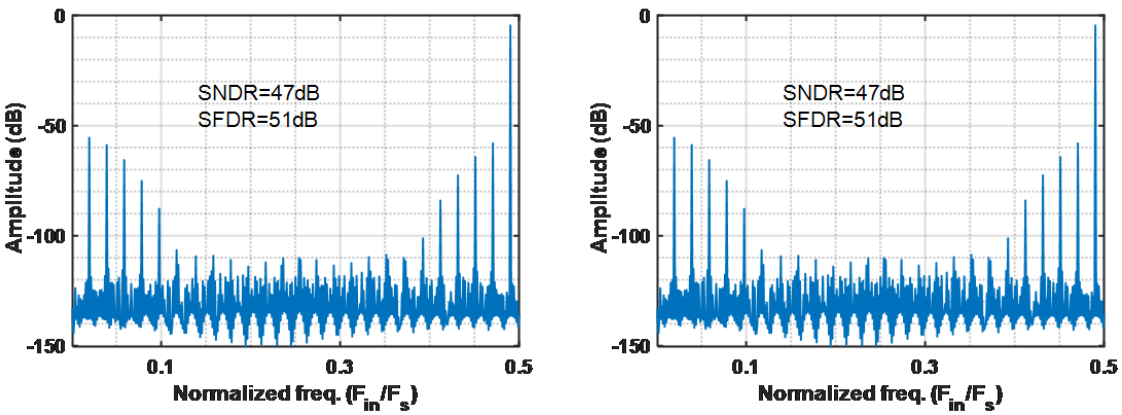


Figure 3.3. FFT simulations of the bootstrapped switch (a) type I (b) type II

3.1.2. Design of Sampling Switch for 1MHz ADC

The proposed bootstrapped sampling switch for 1MHz ADC is depicted in Figure 3.4, comprising a stacked transistor, which is $\times n$ times the main switch, and a PMOS transistor MP. In a conventional stacked topology, type II, switch sizes are doubled to achieve equal on-resistance as the single switch. According to Eq. (3.1), doubling

transistor size will also double its leakage current and its drain-bulk capacitance. In top-plate sampling SAR ADCs, the input signal is typically sampled onto the same node as the comparator inputs. This implies that any nonlinear capacitance at either the drain of the sampling switch ($C_{DB,sw}$) or the input gates of the comparator ($C_{GS,comp}$) will affect each sampled voltage. As the input voltage and, consequently, the voltage across $C_{DB,sw}$ vary, its nonlinear voltage-dependent capacitance will fluctuate, introducing harmonics [4]. In the proposed method, we maintain the main sampling switch M_1 size equal to its single-switch counterpart and increase the stacked transistor size. This approach ensures that the on-resistance of the sampling switch is,

$$R_{on}^{-1} \propto \mu_n C_{ox}(\frac{W}{L})(V_{DD} - V_{th})(1 + 1/n). \tag{3.3}$$

By selecting a large value for n, the bandwidth is preserved; however, it increases the parasitic capacitance C_p at the gate of the main switch. To conserve area and achieve a similar C_p as that of the conventional stacked switch, n is chosen to be 3. This choice would slightly decrease in bandwidth. In the hold mode, the transistor MP shorts the middle node to ground through M_{5-6} to further isolate the input and output nodes. In other words, it prevents the input voltage from being transferred to the sampling capacitor through leakage current. With the low-resistance path created by the transistor MP, channel charge in either of the stacked switches will be dispersed to the middle node, thereby improving linearity. Nevertheless, this node is continuously charged and discharged through the leakage current of M_1, influenced by variations in either output voltage or input voltage during the conversion phase. The low-impedance path created by the transistor MP is preserved only for a brief duration when the voltage in the middle node is higher than V_{THP}. Afterwards, the transistor MP turns off. This ensures that the impedance seen by the output and input nodes remain very high. During the conversion phase, the middle node is directly connected to the ground or V_{REF} [28]. Although these techniques better short the middle node, the output voltage is now directly applied to the drain-source of the sampling switch. This introduces a dependency of the leakage current on the changes in the output voltage.

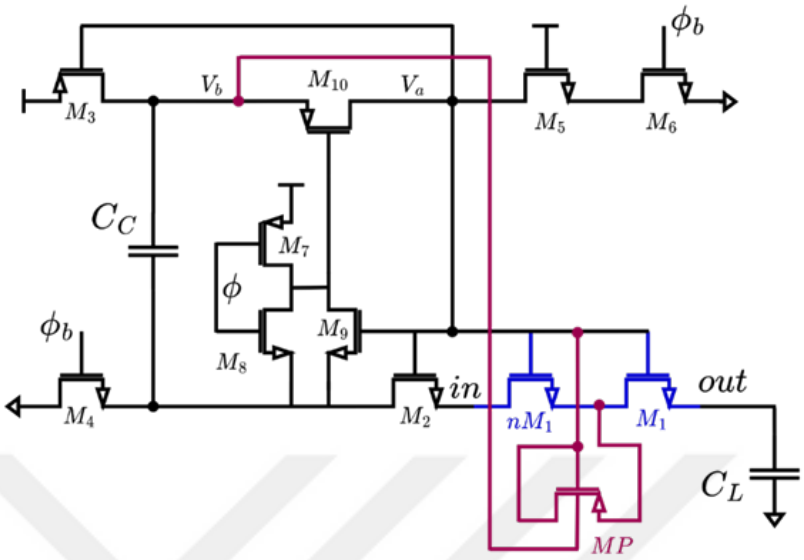


Figure 3.4. Proposed bootstrapped switch for 1MHz ADC

A sinusoidal input at the Nyquist frequency is sampled using the bootstrapped switches type I and II, and the proposed switch of Figure 3.4. The decay in the hold is less severe in the proposed bootstrapped switch, as illustrated in Figure 3.5. The FFT result, shown in Figure 3.6, further demonstrates the effectiveness of the proposed solution, with SNDR and SFDR being greatly improved compared to the conventional type I and II switches.

In the conventional bootstrapped sampling switches in Figure 3.1, charge sharing arises from the parasitic capacitance of transistors M_{1-2}, M_{5-6} and M_{9-10}, resulting in a decrease in V_{GS} voltage during the sampling phase as opposed to reaching V_{DD}. In the proposed switch shown in Figure 3.4, the addition of the parasitic capacitance of transistor MP further contributes to the overall increase in parasitic capacitance. While this effect is typically negligible with a sufficiently large C_C, it becomes a significant factor compromising switch linearity as the input frequencies rises. [33] presents a modified sampling switch to tackle the challenges in high-frequency ADC design. The proposed modifications depicted in Figure 3.4 can be incorporated into the switch introduced in [33], enhancing its suitability for high-speed sample and hold designs.

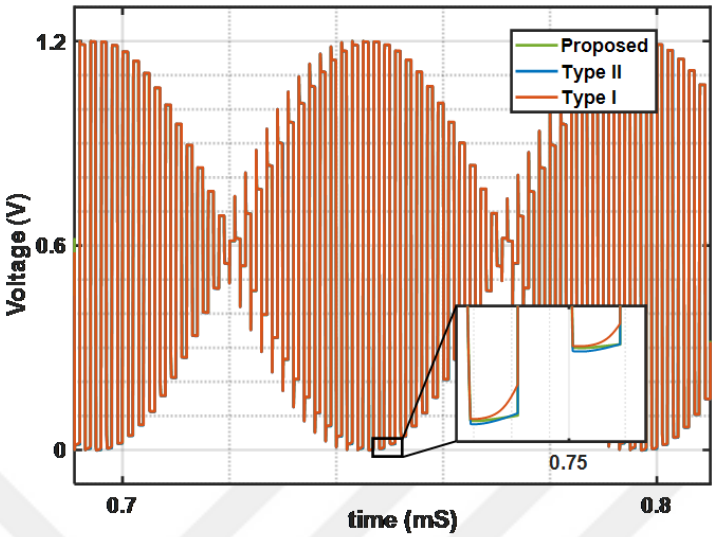


Figure 3.5. Transient response of the switches in ff corner and +125°C temp.

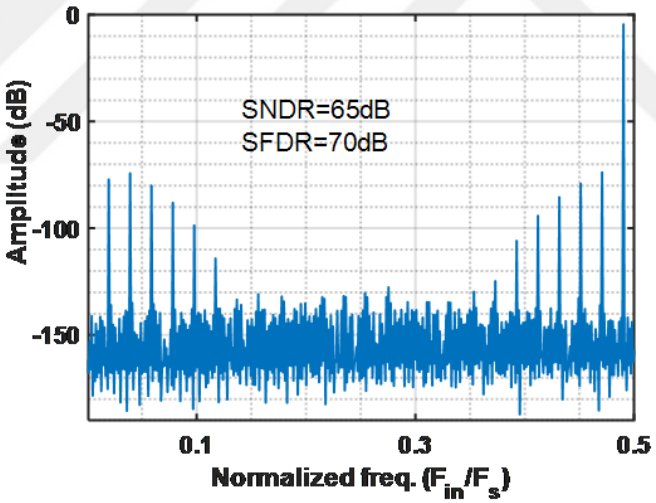


Figure 3.6. FTT result of 1MHz switch at ff corner and +125°C temp.

3.1.3. Design of Sampling Switch for 100kHz ADC

As previously explained, one method to decrease MOSFET leakage current is by connecting the gate voltage to a negative value. This increases the switch's off-resistance, better isolating the output. However, leakage current still depends on the drain-source voltage if a single MOSFET is used. In the 0.7V 100kHz ADC design, a conventional type II bootstrapped switch is modified as shown in Figure 3.7. When ϕ_b is low, the capacitor C_N is charged to V_{DD} through the NOT gate and M_{11-12}. In this

state, the gate of M_{11} is at least V_{DD} and at most $2V_{DD}$, so it is turned ON. When ϕ_b goes high, the right-side of capacitor C_N is shorted to ground, and the left-side holds the voltage $-V_{DD}$. This negative voltage is connected to the gate of M_1 through M_{5-6}. The gate of the transistor M_{11} is connected to its drain through M_{5-6} to keep it in the off-state during the hold mode. The FFT results of the designed switch is presented in Figure 3.8. In S/H circuits, the worst performance usually occurs at the ss corner and high temperatures. In a low-speed design, since the leakage current is usually the main limiting factor, the design in the ff corner becomes more challenging.

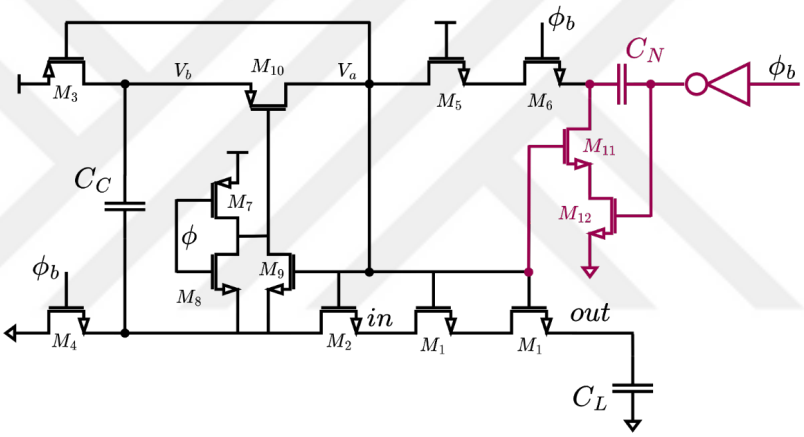


Figure 3.7. Proposed bootstrapped switch for 100kHz ADC

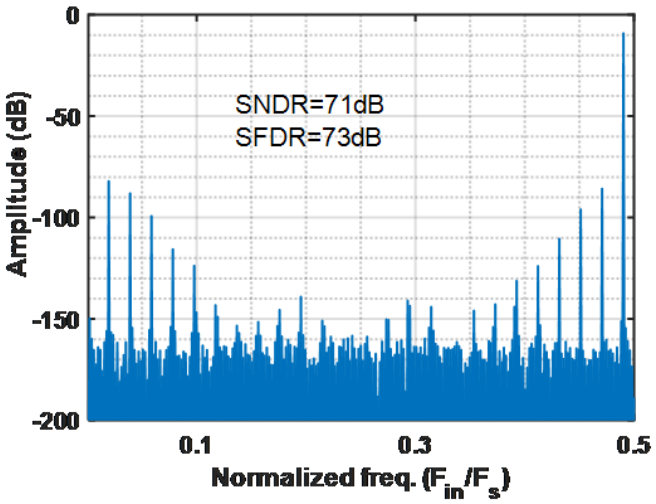


Figure 3.8. FFT result of 100kHz switch at ff corner and +125°C temp.

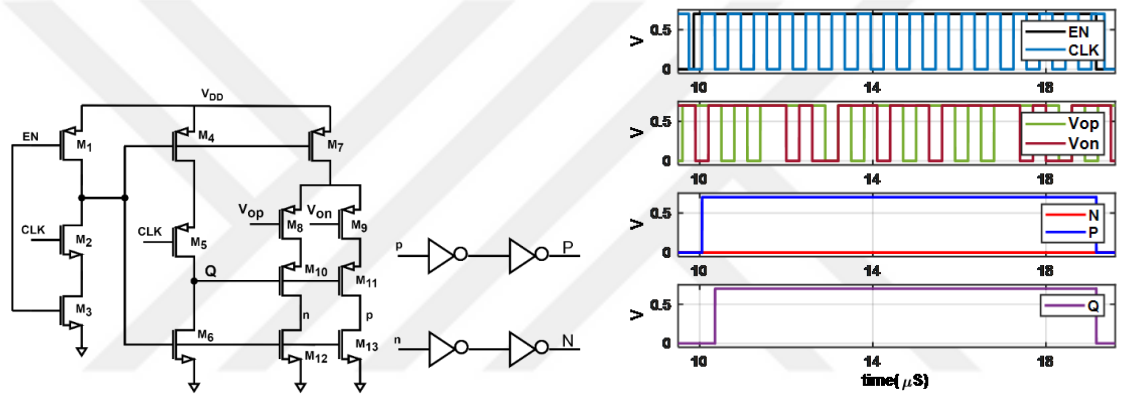
3.2. Bit-Slice-Unit (BSU)

The outputs of the comparator, V_+ and V_-, are fed into Bit Slice Units (BSUs). A conventional BSU circuit and its waveforms are shown in Figure 3.9. Right before the start of conversion phase, the enable signal EN associated with B_{11} is set to zero, resulting in Q being equal to zero. Since the Q signal of any BSU serves as the EN for the subsequent BSU, it follows that all BSUs will be reset to ground. Consequently, both and will be maintained at low level.

When the enable signal (EN) of B_{11} transitions to 1, the conversion process begins. At the rising edge of the BSU clock (CLK), bit[11] is acquired based on the values of V_{op} and V_{on}, where V_{op} and V_{on} signify the comparison results obtained from the comparator. The BSU clock is triggered once V_{op} and V_{on} are settled, ensuring the reliable processing of the result. During the reset phase of the comparator, V_{op} and V_{on} are both pre-charged to V_{DD}. This action causes the CLK signal associated with all BSUs to go low through the NAND gate. Consequently, Q switches to 1, enabling the subsequent BSU. This sequential process continues until B_0 establishes bit[0] and resets the ADC. One primary limitation of the conventional BSU circuit in Fig. 3.9 is its sensitivity to PVT variations. As shown in Figure 3.10(a), when the temperature rises, the internal node n experiences continuous charging toward V_{DD} due to the off-current in its path. Moreover, due to the fact that all BSUs share the same V_{op} and V_{on} signals of the comparator, the values of V_{on} and V_{op} undergo changes during each conversion cycle. Thus, preceding BSUs must retain their respective outputs. However, as depicted in Fig. 3.10(b), the conventional BSU demonstrates vulnerability to mismatches and is also sensitive to temperature variations.

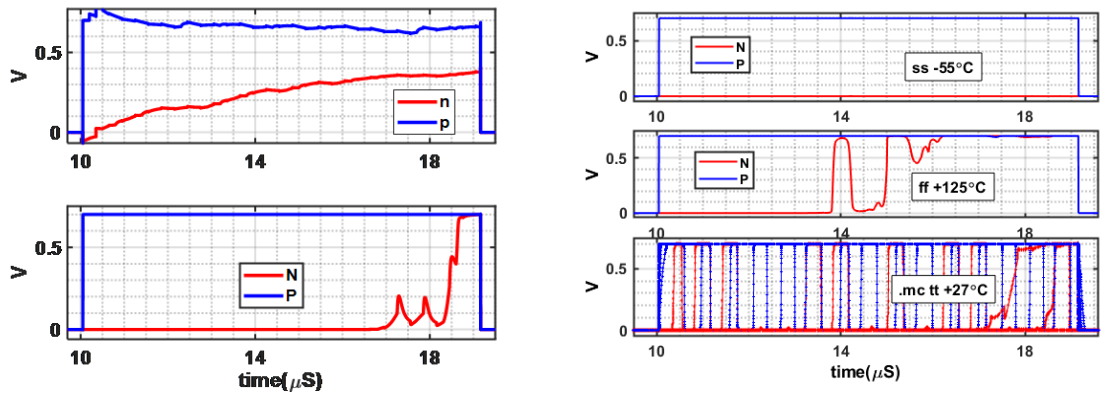
The proposed BSU circuit is shown in Figure 3.11(a). During the reset phase, Q_b is set to 1, and both internal nodes and outputs are grounded through S_0-S_3. When EN is equal to 1, at the rising edge of the CLK, Q_b transitions to zero, and M_7 connects the sources of M_9 and M_{10} to V_{DD}. Due to the latched structure of the proposed method, nodes n and p are immediately settled based on the values of V_{op} and V_{on}, determining the output voltages P and N. Apart from its faster operation compared to

the conventional counterpart, the proposed circuit is more reliable in preserving output values. In scenarios where V_{op} and V_{on} change every cycle or the temperature rises, internal nodes n and p are effectively maintained with the assistance of transistors M_{P1-3}. For instance, if the off-current in M_9 attempts to charge node n through M_{11}, M_{P2} provides a short resistance path to the ground, allowing the off-current of M_9 to flow through M_{P2} rather than M_{11}. This ensures the retention of node n. In addition, M_{P3} and M_{P4} serve as an extra feedback path to enhance the preservation of internal nodes.



(a) (b)

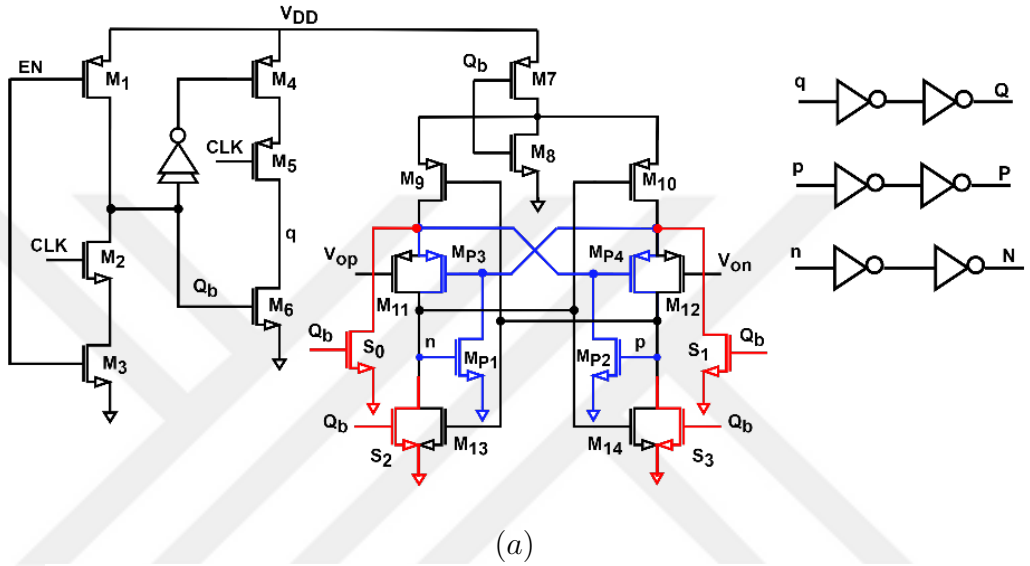
Figure 3.9. (a) Conventional BSU circuit and (b) its waveforms



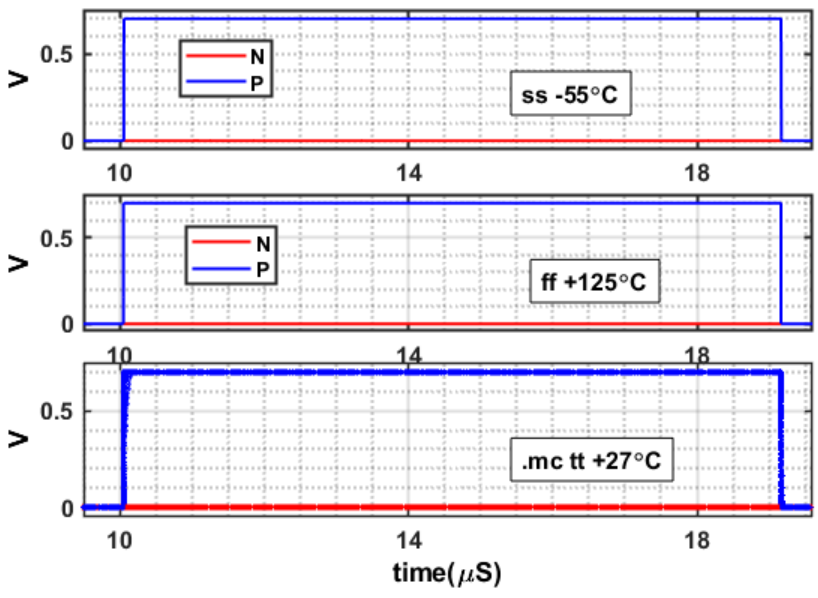
(a) (b)

Figure 3.10. Conventional BSU: (a) charge/discharge of internal nodes (b) variations in the presence of PVT

Figure 3.11(b) shows the simulation results of the proposed circuit under various corners, temperatures, and in the presence of mismatch (30 .mc run). The results demonstrate the superiority of the proposed BSU compared to the conventional one. This structure is used in both ADCs.



(a)



(b)

Figure 3.11. (a) Proposed BSU circuit (b) its waveforms in the presence of PVT variations

4. COMPARATOR

Dynamic comparators are essential components in SAR ADC designs. Unlike OpAmp based static comparators, dynamic comparators have no static current consumption, which makes them highly suitable for low-power systems. These comparators also excel in speed due to their rapid charging and discharging capabilities, resulting in reduced delays and improved responsiveness. The high-speed functionality, combined with efficient energy usage, makes dynamic comparators preferable in scenarios where rapid and power-efficient signal processing is crucial. The StrongArm Latch (SAL) as an example of a widely used dynamic comparator is shown in Figure 4.1(a). Its performance is extensively explored in literature concerning noise, gain, offset, and several other factors. When the clock (CLK) is low, the internal nodes are pre-charged to V_{DD} by means of switches S_0-S_3, referred to as the reset phase. As CLK goes high, S_0 to S_3 turn off, and the comparator enters into the decision phase. At the outset of the decision phase, transistors M_1 and M_2 turn on, resulting in a differential current proportional to V_{in} being continuously drawn from the capacitors C_C. This allows V_{x-y} to increase and potentially surpass V_{in}, thus providing voltage gain [34]. This phase is referred to as the sampling phase and continues until the capacitor C_C drops by one threshold voltage, V_{thN}, whose duration is defined as

$$T_S = \frac{C_C V_{thN}}{0.5 I_0}, \tag{4.1}$$

where I_0 and V_{thN} are the tail current and threshold voltage, respectively. The dynamic amplification of the input voltage on C_C over T_S serves as the initial condition for the subsequent phase; the propagation phase. During the propagation phase, M_3 and M_4 are turned ON, resulting in the output voltage V_{out} being discharged by V_{thP} to activate the cross-coupled PMOS pair M_5-M_6. Over this phase, the transistors M_3-M_4 act as a charge-transfer amplifier between the capacitors C_C and C_L, allowing for the current

and voltage to ramp down in unison [35]. This phase lasts for

$$T_P = \frac{(C_C + C_L)V_{thP}}{0.5I_0}. \tag{4.2}$$

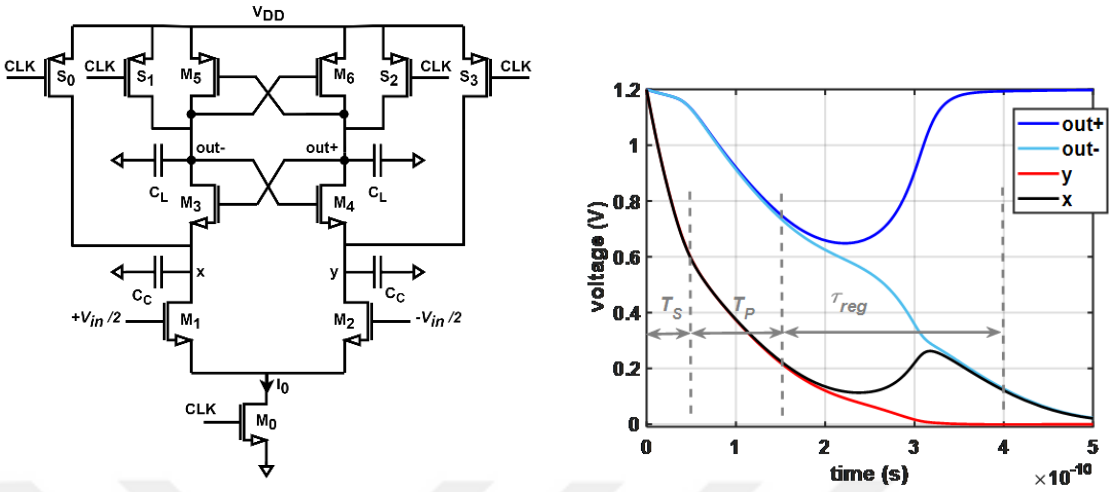
Following the propagation phase, the cross-coupled PMOS pair, M_5-M_6, is activated and, due to its sources being connected together, it continually regenerates the initial differential voltage V_{int} on C_L. This phase is called the regeneration phase and it lasts for

$$\tau_{reg} = \frac{C_L}{G_m} \ln \frac{V_{DD}}{V_{int}}. \tag{4.3}$$

For simplicity, V_{DD} is chosen to be the acceptable voltage level for logic "1". G_m is the net trans-conductance of the cross-coupled inverters. The contribution of the inverters to the net transconductance G_m varies across the regeneration phase, ranging from g_{m5-6} at the beginning to $g_{m5-6} + g_{m3-4}$ later when M_1 and M_2 are driven into the deep triode region [35, 36]. If the input pair M_1 and M_2 operate in the saturation region prior to the commencement of the regeneration phase, the input noise voltage (due to thermal noise) and the gain in Figure 4.1(a) are calculated by Equations (4.4) and (4.5) [35], as

$$A_V = \begin{cases} \frac{C_L+2C_C}{C_L-C_C} \cdot \frac{2V_t}{V_{DSAT1,2}} & \text{if } C_L \geq 2C_C \\ \frac{C_L+3C_C}{C_C} \cdot \frac{V_t^2}{V_{DSAT1,2}V_{DSAT3,4}} & \text{if } C_L \approx C_C \\ \frac{2V_t+V_{DSAT3,4}}{V_{DSAT1,2}} \cdot e^{\frac{2V_t}{V_{DSAT3,4}}} & \text{if } 2C_L \leq C_C \end{cases} \tag{4.4}$$

$$v_n^2(t) = \frac{4kT\gamma V_{DSAT1,2}}{V_t} \begin{cases} \frac{1}{2}\frac{1}{2C_C+C_L} & \text{if } C_L \geq 2C_C \\ \frac{1}{3C_C+C_L} & \text{if } C_L \approx C_C \\ \frac{1}{C_C\left(2+V_{DSAT3,4}/V_t\right)} & \text{if } 2C_L \leq C_C. \end{cases} \tag{4.5}$$



(a) (b)

Figure 4.1. (a) StrongArm Latch circuit and (b) its simulation results

In a typical design, M_1 and M_2 are the dominant contributors to the input offset voltage. Since the amplification phase provides voltage gain through the flow of charge from C_x and C_y (the total capacitance at nodes x and y), asymmetry can be created by making C_x unequal to C_y, thus cancelling the circuit's offset [34]. In the perspective of speed, the maximum achievable speed in a StrongArm Latch is determined by the delays in the sampling phase, propagation phase, regeneration phase, and the acceptable metastability error rate, which dictates the minimum clock period as a multiple (n) of the regeneration time constant [35],

$$\tau_{\text{delay}} = T_S + T_P + n\tau_{\text{reg}}. \tag{4.6}$$

As highlighted in Figure 4.1(b), T_S, T_P, and τ_{reg} are 50 psec, 100 psec, and 250 psec, respectively. While SALs have been thoroughly discussed in various papers, there remains a lack of comprehensive analysis concerning their speed characteristics. We will attempt to fill this gap and present ways to enhance the speed of SALs. We will show that, in contrast to conventional wisdom, the smaller value of transconductance G_m of cross-coupled inverters leads to improved comparator performance during the initial regeneration phase. An in-depth analysis, supported by circuit simulation results, will be conducted to validate this assertion.

4.1. Design of Comparator for 100kHz ADC

The accuracy of the comparator in a SAR ADC is crucial for optimal ADC performance. While a conventional StrongArm Latch (SAL) is well-suited for ADCs with fewer than 10 bits, it encounters challenges, particularly in terms of common-mode offset and noise. A comprehensive study on StongArm Latches has been conducted in [35]. However, for ADCs requiring more than 10 bits, a single SAL may prove insufficient. To address this, a common strategy involves employing a pre-amplifier followed by a SAL. This configuration mitigates non-linearity and noise in the SAL by leveraging the gain of the pre-amplifier, simplifying the overall design. On the other hand, in a low-voltage design, the pre-amplifier typically undergoes offset calibration to ensure a high dynamic range. The proposed comparator structure, shown in Fig. 4.2, integrates a calibrated pre-amplifier preceding a non-calibrated SAL.

Its operation is as follows: During the calibration phase, the input transistors M_1 and M_2 are isolated from the inputs and connected to the common voltage V_{CM} through the calibration switches S_1-S_2. These switches are activated by $CK_{Cali.}$. signal illustrated in Figure 2.5(b). Simultaneously, the current source I_{SS} flows through the signal path, involving transistors M_{1-4} and the load resistors R. When the signal $CK_{Cali.}$ goes low, the switches S_3-S_4 are activated and any errors in this path are sampled on the capacitors C_C. Due to the low value of V_{CM} compared to the threshold voltage, transistors M_{1-2} are forced to operate in weak inversion. Thus,

$$I_D = I_0 e^{\frac{V_{GS}-V_{th}}{V_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) = \frac{I_{ss}}{2}, \quad I_0 \propto \mu_n C_{ox} \frac{W}{L}, \tag{4.7}$$

where V_T is the thermal voltage. Given the assumptions listed in Eq. (4.8), the offset voltage at the output of the pre-amplifier is calculated,

$$\begin{cases} V_{th1} = V_{th} + \frac{\Delta V_{th}}{2} \\ V_{th2} = V_{th} - \frac{\Delta V_{th}}{2} \end{cases} \quad \begin{cases} I_{01} = I_0 + \frac{\Delta I_0}{2} \\ I_{02} = I_0 - \frac{\Delta I_0}{2} \end{cases} \quad \begin{cases} R_1 = R(1 + \frac{\Delta R}{2}) \\ R_2 = R(1 - \frac{\Delta R}{2}). \end{cases} \tag{4.8}$$

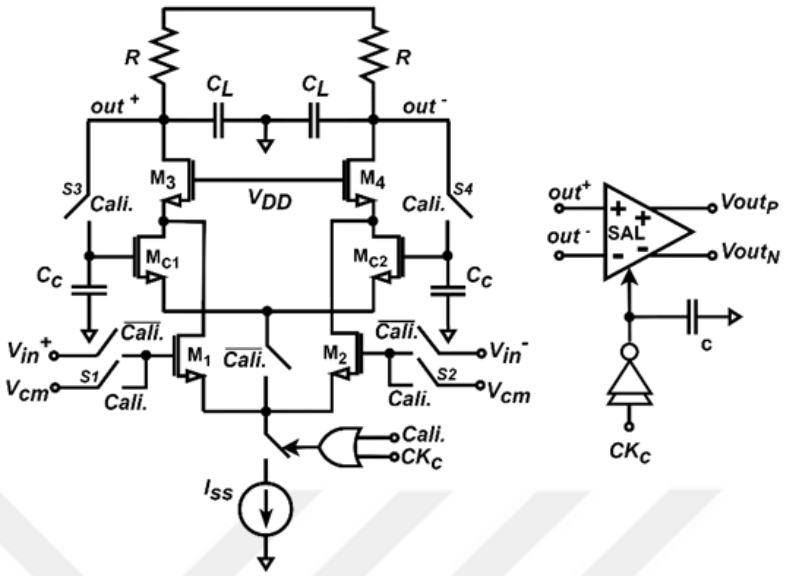


Figure 4.2. Proposed comparator circuit for 100kHz ADC

The output offset resulting from variations in the threshold voltage, V_{th}, and I_0 of the input transistors, as well as the mismatch due to the load resistors R is found using Equations (4.9), (4.10) and (4.11), respectively. And, the total offset at the output is given by Equation (4.12) as

$$\Delta V_{out_{\Delta V_{th}}} = R(I_{D1} - I_{D2}) = RI_0 \left[e^{\frac{V_{GS}-V_{th}-\frac{\Delta V_{th}}{2}}{V_T}} - e^{\frac{V_{GS}-V_{th}+\frac{\Delta V_{th}}{2}}{V_T}} \right] \approx -\frac{RI_{ss}\Delta V_{th}}{2V_T} \quad (4.9)$$

$$\Delta V_{out_{\Delta I_0}} = \Delta I_0 R e^{\frac{V_{GS}-V_{th}}{V_T}} \approx \Delta I_0 R \quad (4.10)$$

$$\Delta V_{out_{\Delta R}} = \frac{I_{ss}}{2}\Delta R \quad (4.11)$$

$$(\Delta V_{OUT})^2 = \left(\frac{RI_{ss}}{2}\right)^2 \left[\left(\frac{V_{th}}{V_T}\right)^2 \left(\frac{\Delta V_{th}}{V_{th}}\right)^2 + \left(\frac{\Delta I_0}{I_0}\right)^2 + \left(\frac{\Delta R}{R}\right)^2 \right]. \quad (4.12)$$

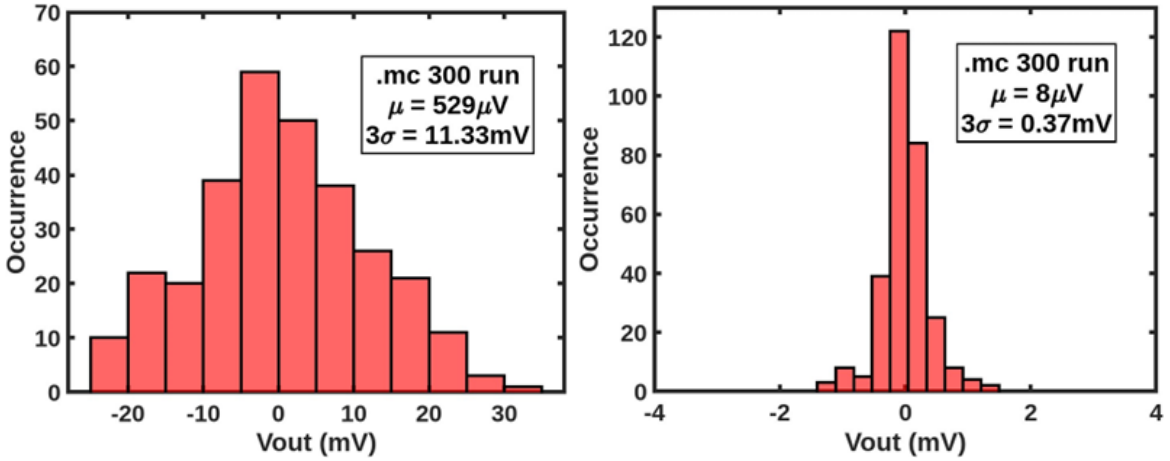
Indeed equation (4.12) describes the overall output offset of the pre-amplifier during the calibration phase activation. As the calibration signal goes low, M_1-M_2 reconnect to the inputs, and M_{C1}-M_{C2} pair is configured in parallel with the input transistors M_1-M_2. As a result, M_{C1} and M_{C2} draw currents in response to the offset voltage specified in Eq. (4.12), sampled on the capacitors C_C. This setup ensures an equal output voltage for each branch. Thus,

$$\Delta V_{out_{\Delta V_{OUT}}} = RI_c \left[e^{\frac{V_{GS}-V_{th}-\frac{\Delta V_{OUT}}{2}}{V_T}} - e^{\frac{V_{GS}-V_{th}+\frac{\Delta V_{OUT}}{2}}{V_T}} \right] \approx -\frac{RI_c \Delta V_{OUT}}{V_T}, \tag{4.13}$$

where I_c represents the current drawn from M_{C1}-M_{C2} pair. On the other hand, the sum of I_{c1} and I_1 should equal I_{SS} once the calibration phase is complete. This implies that I_{SS} in Eq. (4.11) is now a fraction of its previous value (denoted as $\alpha \Delta V_{OUT}$). To eliminate the offset, $\alpha \Delta V_{OUT}$ should be equivalent to Eq. (4.13). Given that I_1 is αI_{SS}, the value of I_c would be $(1-\alpha)I_{SS}$. So, we have,

$$\alpha \approx \frac{\frac{RI_{ss}}{V_T}}{1+\frac{RI_{ss}}{V_T}}. \tag{4.14}$$

In the preceding calculations, we disregarded the effect of mismatch in M_{C1}-M_{C2} pair. For the sake of simplifying the design, we set the current of M_{C1}-M_{C2} pair to be less than 10% of the I_{SS} so that the mismatch in M_{C1}-M_{C2} is not a critical factor. Thus, we chose α to be 0.9. Using Eq. (4.14) and with $V_T \sim 25$ mV, RI_{SS} is found to be 225 mV. In addition, long-channel devices are employed for M_{C1}-M_{C2} to decrease their offset and flicker noise. While the mismatch in load capacitors C_L is not highly critical in the first order, it often dictates the need for sufficient settling time. Moreover, C_L determines the noise limitations of the amplifier. The mismatch in the capacitors C_C is not crucial, as they simply retain the offset in the calibration phase for one cycle period. The Monte Carlo analysis of the proposed pre-amplifier is shown in Figure 4.3 for $V_{OUT} = out^+ - out^-$. The 3-sigma deviation in the pre-amplifier decreases significantly from 11.3mV when the calibration is off to 370μV when it is on. The mean values are denoted with in both cases.



(a) (b)

Figure 4.3. mc analysis of the proposed pre-amplifier when calibration is (a) off (b) on

4.2. Design of Comparator for 1MHz ADC

The 1MHz ADC operates with a core voltage of 1.2V. With a 12-bit resolution and a reference voltage equal to the supply voltage of 1.2V, the LSB is approximately 300μV. In the design of this comparator, calibration is not applied to the preamplifier, and the preamplifier is biased with a constant bias current. Represented in Figure 4.4, a static preamplifier ensures that the offset remains a constant value, simplifying its treatment as it can be easily canceled out in the measurement setup. The input common-mode voltage of the comparator is varied from $(1/2)V_{REF}$ to $(3/4)V_{REF}$. The 3-sigma offset of the comparator in Figure 4.4 is shown in Figure 4.5, with the input common mode voltage changing from $V_{CM} = 0.6V$ to $V_{CM} = 0.9V$. As expected, the offset remains nearly constant and only changes by approximately 40μV due to variations in the common-mode voltage.

4.3. Speed Analysis of StrongArm Latch Based Comparators

In the context of speed, dynamic comparators may restrict the operating speed of the ADC in two ways. 1) The net delay of the comparator, "the output delay", and 2) The poles associated with the input parasitic capacitance of the comparator C_p, "the input delay".

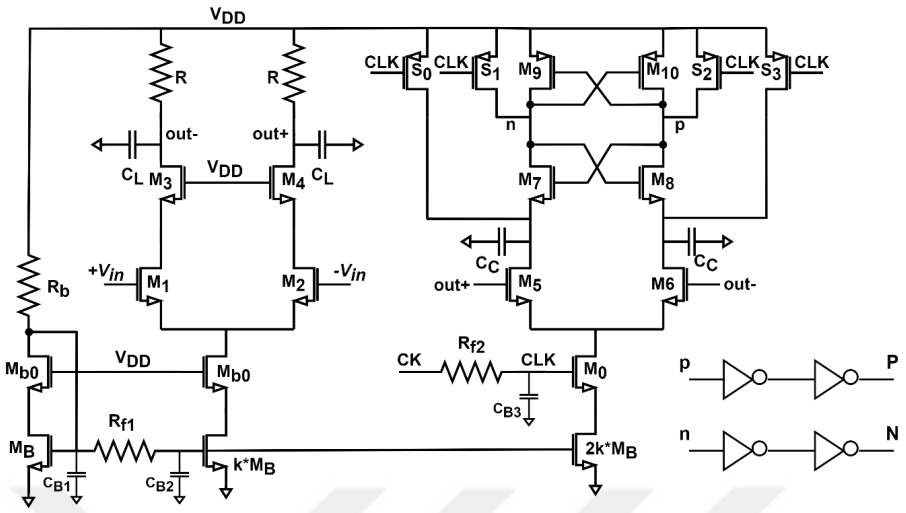


Figure 4.4. The comparator circuit for 1MHz ADC

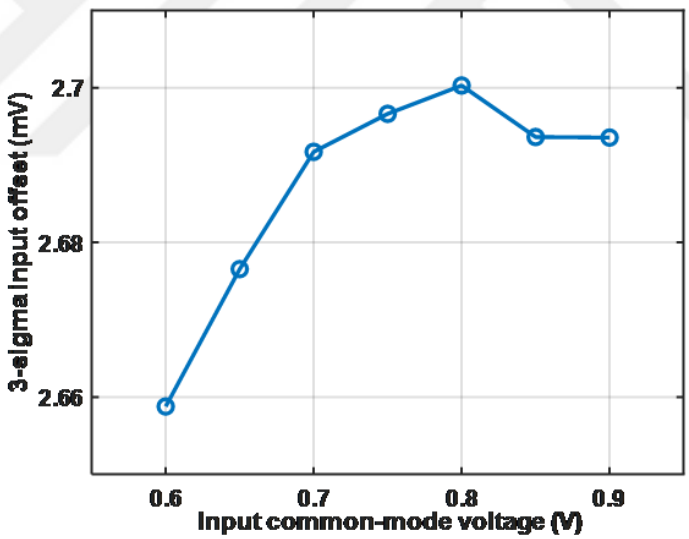


Figure 4.5. 3-sigma offset of the comparator in 1MHz ADC with varying CM input

As previously discussed in this chapter, the highest speed attained in a StrongArm Latch is directly influenced by the delays outlined in Eq. (4.6). On the other hand, the poles linked to the input capacitance of the comparator are also relevant in some applications. For instance, in the case of a SAR ADC, the input capacitance of the comparator can introduce gain error and impose limitations on the overall dynamic range. As another example, a StrongArm Latch as a sense-amplifier contributes to

the loading of column and row lines in SRAM arrays. Therefore, a comparator with a short delay and a small input parasitic capacitance is of interest. Equation (4.6) can be expressed as,

$$\tau_{\text{delay}} \approx \frac{(2C_C + C_L)V_{th}}{0.5I_0} + \frac{nC_L}{G_m} \ln\left(\frac{V_{DD}}{V_{int}}\right). \tag{4.15}$$

If a minimum value for C_C and C_L are set for the purpose of offset calibration and the noise requirement (see Equations (4.4) and (4.5)), I_0 would be the only factor to decrease the net delay at Eq. (4.15). On the other hand, if the size of the input pair M_{1-2} is limited to lower the input parasitic C_p, further increasing the value of I_0 to reduce the net delay would somehow impede any potential for speed enhancement. Consider the common practice of 1:1:1 FET sizing in a classic StrongArm Latch of Figure 4.1(a) with $(W/L)_{1-6} = 6\mu m/60nm$ and $C_{C,L} = 20fF$, with $V_{DIFF} = 1mV$ and $V_{CM} = 600mV$. The net delay from when $CLK = High$ to when output crosses $0.5V_{DD}$ is 346psec, 331psec and 321psec with $(W/L)_0$ of $16\mu m$, $32\mu m$ and $160\mu m$, respectively. Thus, as the size of the input pair is fixed, as shown in Figure 4.6, the enhancement in the speed is not appreciable.

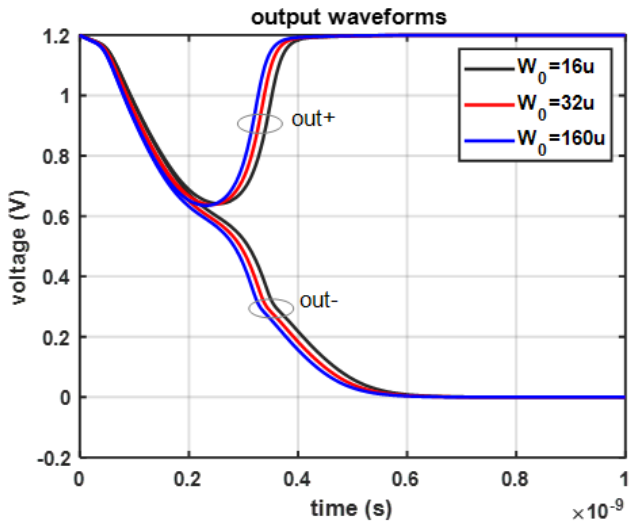


Figure 4.6. The outputs of the conventional SAL in Figure 4.1(a) with different widths for M_0

4.3.1. Negative Capacitance Approach

Consider the back-to-back inverter shown in Figure 4.7 with its regeneration time equation. In order to mitigate the delay in regeneration time, three options are possible.

(i) Increase the initial voltage V_{int} on C_L. This requires the preceding amplifier to have a larger gain. The larger the gain, the higher the amplification time period $T_S + T_P$.
(ii) Decrease C_L. The output capacitor C_L is usually limited by the input capacitance of the following stage as well as the requirements for the noise and offset.
(iii) Use larger devices to increase G_m, which add parasitic capacitance to the output node, thus limiting the speed.

As mentioned earlier, T_S and T_P determine the gain and the noise of the overall circuit. Thus, our initial analysis focuses on the circuit during the regeneration phase, and we aim to minimize its delay based on this analysis. The impedance seen by C_L during the propagation phase, as shown in Figure 4.8, is calculated as,

$$Z = \frac{2\left(r_{o3}z_x(g_{m3} + C_{gs3}S) + r_{o3} + z_x\right)}{1 - r_{o3}(g_{m3} + C_{gs3}S) + 2C_{gs3}S(r_{o3} + 2Z)} \approx \frac{2}{-g_{m3} + C_{gs3}S} - \frac{2r_{o1}}{r_{o1}C_cS + 1}, \quad (4.16)$$

where r_{o1} stands for the drain-source resistance of the input pair M_{1-2} and $z_x = r_{o1}/(r_{o1}C_cs + 1)$. Figure 4.9(a) shows Z with practical values of $r_{o3} = r_{o1} = 5k\Omega$, C_{gs3} = 5fF, C_C = 20fF, and g_{m3} =2mA/V. In a certain frequency band (0.1GHz-10GHz), the impedance Z acts like a negative capacitor, while at lower frequencies it behaves as a negative resistor. This circuit is widely used as a negative capacitance in design of operational amplifiers which drive large capacitive loads [37]. The negative capacitance value seen by C_L is also shown in Figure 4.9(b) with different values of r_{o1}. As r_{o1} becomes larger, the impedance seen by C_L is mostly capacitive and equals to $\sim C_{C/2}$. Suppose C_L=20fF. Around 2GHz, the impedance seen by C_L in Figure 4.9(b) is -16fF, so that, the total capacitance at the output node becomes only 4fF. Consequently, the bandwidth is widened, and the speed is enhanced.

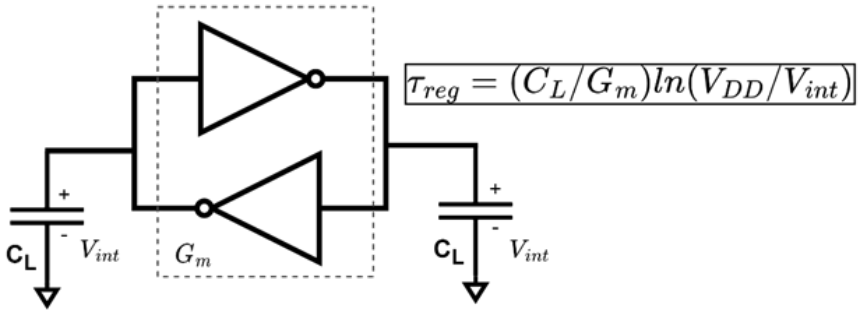


Figure 4.7. Back-to-back inverter structure

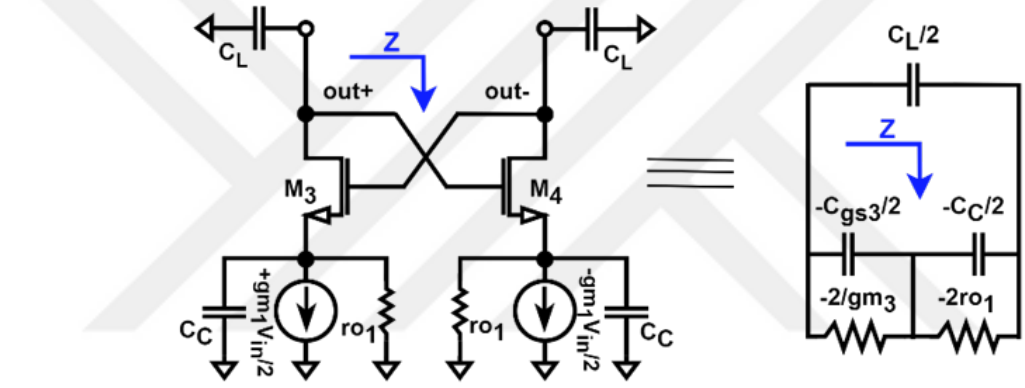
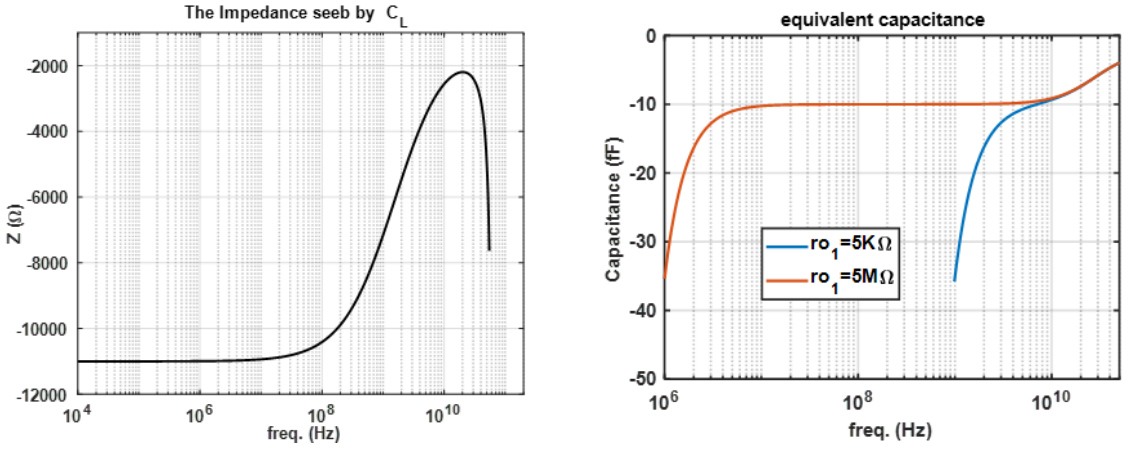


Figure 4.8. StrongArm latch in propagation phase



(a) (b)

Figure 4.9. (a) Magnitude of the impedance Z (b) Z with r_{o1}=5$k\Omega$ and 5$M\Omega$

In other words, one can decrease the total capacitance at the output nodes with appropriate sizing of devices and capacitors at a specified frequency. Nevertheless, care should be taken to avoid oscillation. Negative capacitance can be conceptualized as an inductance; thus, the circuit is prone to oscillate if loaded accordingly. As demonstrated in 4.10, when PMOS pair M_5 and M_6 are replaced with a positive resistance of R, the output oscillates. This is an important result. The impedance of the PMOS cross-coupled M_{5-6} in a StrongArm Latch is

$$R_{\text{eq}} = \frac{2}{(r_{oP})^{-1} - g_{mP}} \approx \frac{-2}{g_{mP}}, \tag{4.17}$$

where r_{oP} is usually neglected and the output impedance assumes a negative value. For any reason, if $(r_{oP})^{-1} \geq g_{mP}$, then R_{eq} becomes positive and the circuit is likely to oscillate. As in large signal systems, these analyses apply only at the beginning of the regeneration phase; the transition point from propagation to regeneration. The overall circuit, with an applied differential input voltage of V_{in}, is configured as in Figure 4.11(a). For the sake of simplicity, C_{gs3} is ignored and G_m is the total transconductance of the back-to-back inverters. As the regeneration time progresses, the input transistors enter the triode region and r_{o1} approaches zero; thereby, eliminating the effect of C_C and leaving C_L as the only factor contributing to the regeneration time delay. We normalize the circuit with that shown in Figure 4.11(b) with the factors of

$$\mu = g_{m3}/G_m \qquad \alpha = C_c/C_L \qquad \beta = G_m \cdot r_{o1}.$$

The equivalent impedance is now,

$$Z_{eq} = \frac{(-\alpha\beta S + \beta\mu + 1)}{(-\alpha\beta S^2 + (\beta\mu - \alpha\beta - \alpha\beta\mu + 1)S + \beta\mu + \mu + 1)}. \tag{4.18}$$

The impedance Z_{eq} is optimized for the maximum normalized bandwidth in MATLAB. Figure 4.12 illustrates a family of curves representing various factor values.

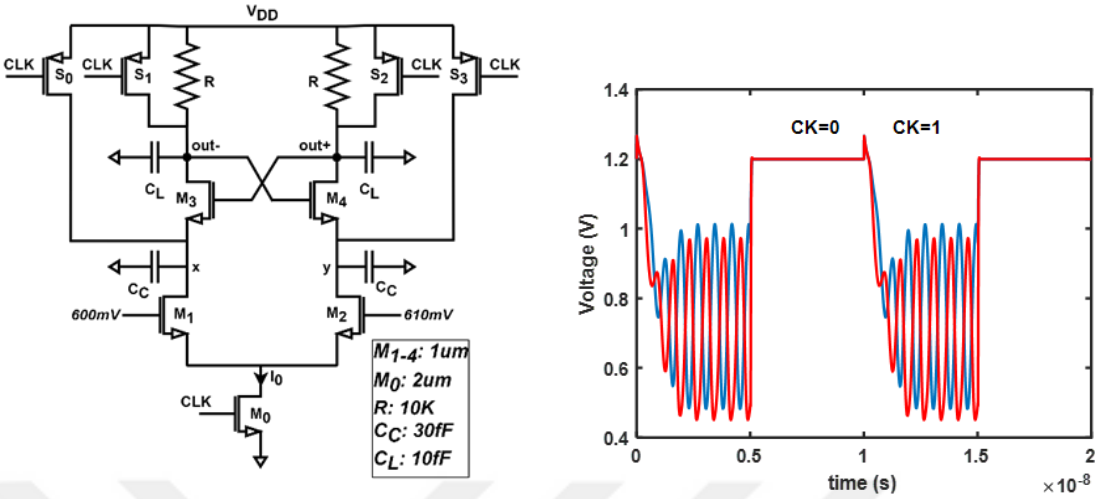
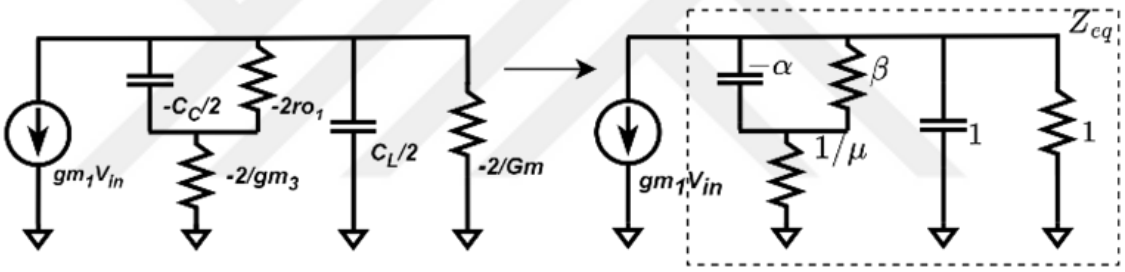
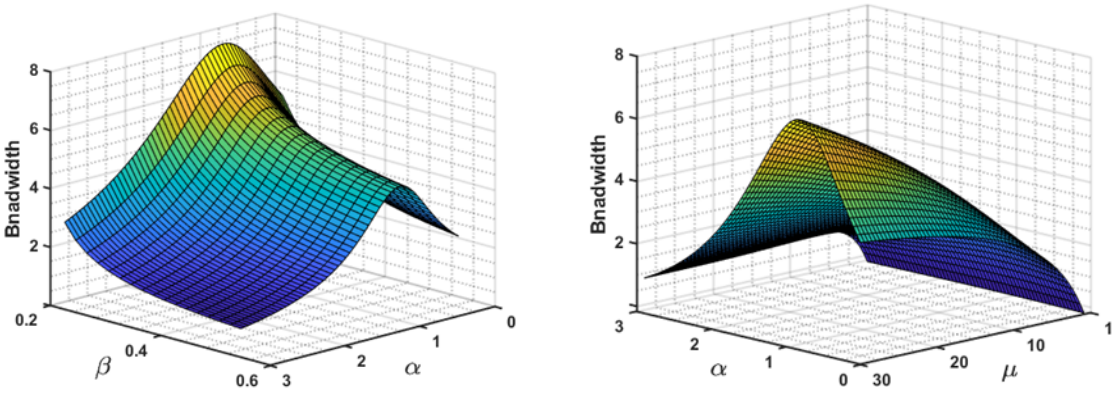


Figure 4.10. An example of oscillation possibility in StrongArm Latch



(*a*) beginning of the regeneration time (*b*) the normalized version

Figure 4.11. SAL in differential mode; beginning of the regeneration phase



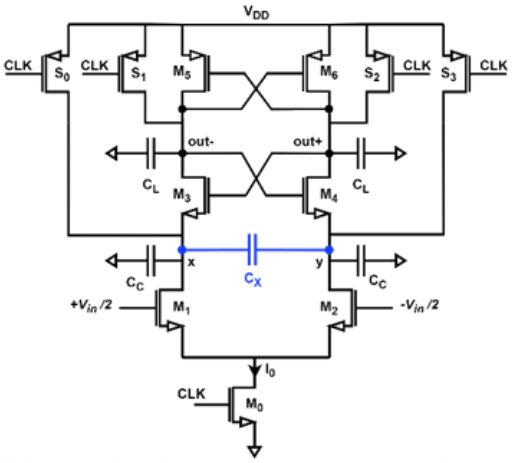
$\mu = 20$ $\beta = 0.2$

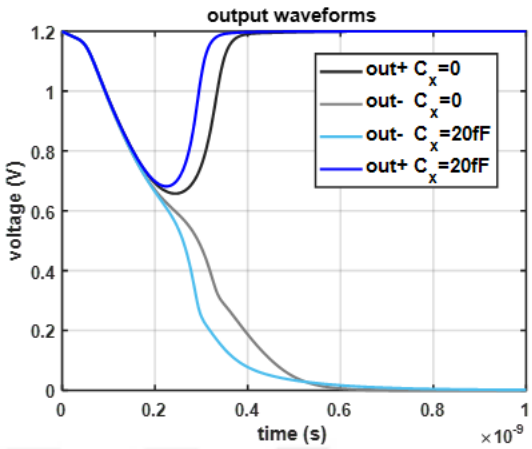
Figure 4.12. Normalized bandwidth of Z_{eq}

The figures reveal that, a higher value of μ and a lower value of β correspond to a broader bandwidth. In other words, at the point where regeneration phase starts, larger g_{m3}/G_m and smaller $G_m r_{o1}$ are of interest. If these two conditions are met, sweeping $\alpha = C_c/C_L$ would lead to an extended bandwidth. This could also be observed intuitively in the circuit of Figure 4.11(b). The higher values of μ will ground the minus side of the resistor β and the capacitor -α. As a result, the bandwidth will become $[(1 - \beta)\ (1 \parallel \beta)]^{-1}$. Therefore, a smaller value of $\beta = G_m r_{o1}$ is desirable in order to achieve a wider bandwidth. However, it is important to ensure that the value of α is kept smaller than 1. Otherwise, the pole will shift to the right-hand side of the complex plane, leading to a phase flip during the decision-making time period. In the case of StrongArm Latch, G_m=g_{m5-6} which is already a small value at the beginning of regeneration time. Therefore, by simply adjusting α, the bandwidth is extended. To preserve the values T_S and T_P, a differential addition of C_x is employed as illustrated in Figure 4.13(a). With C_x=20fF, the total capacitance at the output node is reduced during regeneration period, resulting in increased speed, Figure 4.13(b). Nevertheless, it is expected that the reduction in differential capacitance at the output nodes, will have a negative impact on the noise performance. With transient noise enabled in Spectre, the comparator is clocked at f_{CLK} = 500MHz with V_{DIFF} and V_{CM} of 0.6V. The node 'out+' is depicted in Figure 4.14 for various values of C_x. Out of a total of 50k cycles, 23 and 76 cycles are found to be incorrect when C_x=0 and C_x=20f, respectively. As C_x increases, the input referred noise tends to increase as well.

4.3.2. Smaller G_m Approach

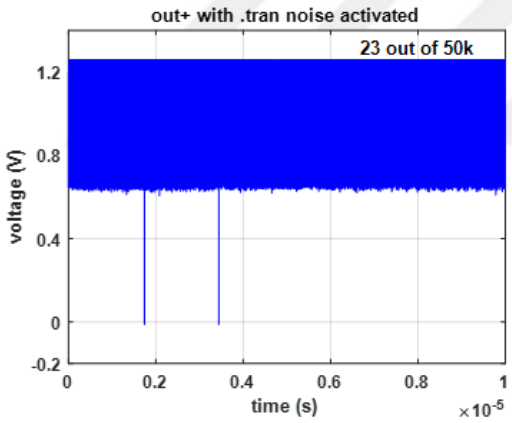
As stated earlier, higher values of g_{m3-4} increase the bandwidth. However, increasing the width of transistors M_{3-4} for larger g_{m3-4} adds parasitics to the output nodes, limiting bandwidth improvement. Decreasing β will also increase the bandwidth, however, G_m needs to be sufficiently high to regenerate output logic immediately after the cross-coupled pair acts. As a remedy, the resistor -2/G_m in Fig. 4.11(a) is replaced with a separate back-to-back inverters as in Fig. 4.15(a). This way, μ and β can be set free from each other. $T_S + T_P$ in Figure 4.1(b) was measured to be 150psec. To match this delay, the buffer B is set to 150psec, and the result is shown in Figure 4.15(b).



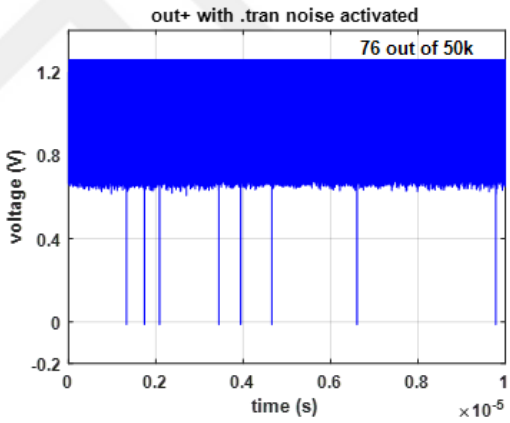


(*a*) decreasing the load capacitance by C_x (*b*) the resulting waveforms

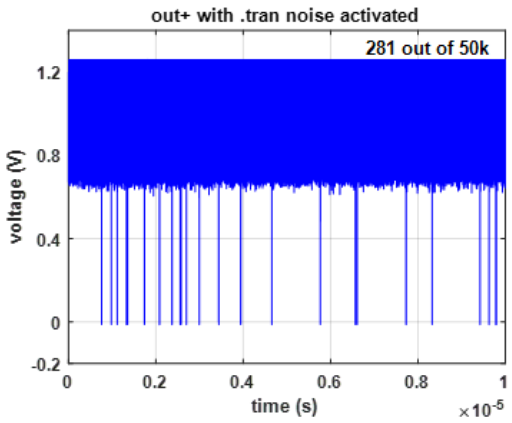
Figure 4.13. Speed enhancement; the negative capacitance approach



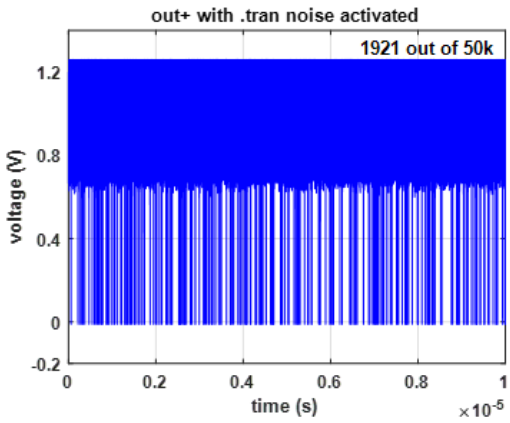
(*a*) $C_x = 0$



(*b*) $C_x = 20$fF



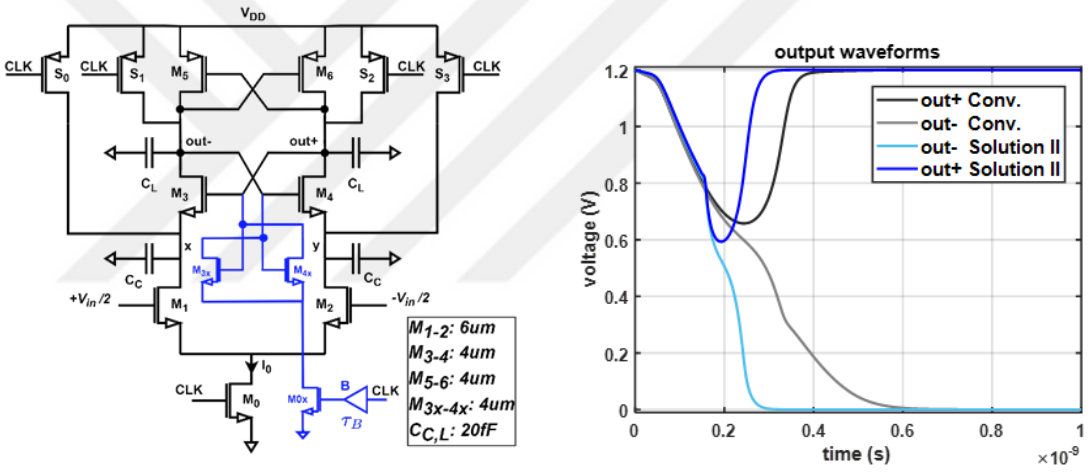
(*c*) $C_x = 40$fF



(*d*) $C_x = 100$fF

Figure 4.14. A snapshot of node 'out+' in Fig. 4.13 with different values for C_x

Right after the regeneration phase starts, the NMOS cross-coupled pair now incorporates an additional contribution from g_{m3x}. In contrast, the width of the transistors in the PMOS cross-coupled g_{m5-6} is reduced. Thus, μ becomes larger and G_m becomes smaller; further reducing the regeneration time delay. During the $T_S + T_P$ interval, the circuit remains unchanged, and therefore the input referred noise follows Eq. (4.5). Combining the approaches depicted in Figure 4.13 and 4.15, we compare the result with that of a conventional SAL. Shown in Fig. 4.16, the conventional SAL fails to achieve a complete response at $f_{CLK} = 1GHz$. To further increase the speed, $T_s \leq \tau_B \leq T_P$ could be selected, at the cost of reduced gain and increased noise.



(*a*) increasing μ and decreasing β (*b*) the resulting waveforms

Figure 4.15. Speed enhancement; smaller Gm approach

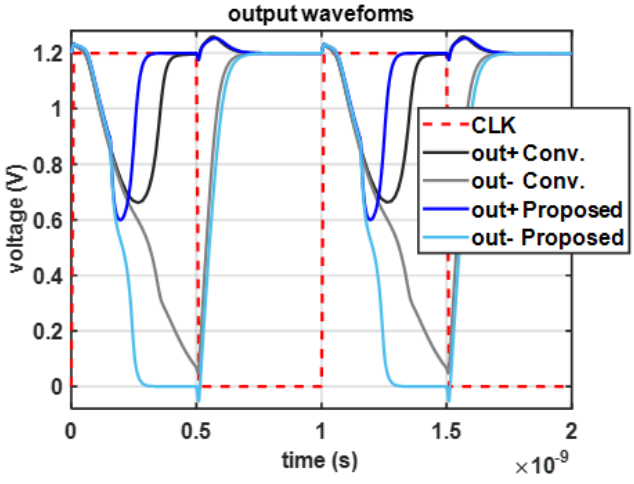


Figure 4.16. Comparison of the modified and conventional SAL

5. JITTER IN SAMPLING CLOCKS

When designing the clocking network for an ADC, one of the most critical parameters is jitter. The extent of established clock jitter will define the upper limit of the achievable Signal-to-Noise Ratio (SNR) for a specific input frequency. While clock jitter primarily holds significance in high-speed ADC design, its impact becomes crucial in a high-resolution ADC as well. The relationship between SNR and jitter is expressed as follows,

$$\mathrm{SNR} = -20\log\left(2\pi f_{\mathrm{in}} t_j\right), \tag{5.1}$$

where f_{in} is the frequency of the input signal, and t_j is the rms-jitter of the clock [38]. The Equation (5.1) indicates the maximum achievable SNR. For a high-frequency input signal and a constant amount of jitter, the maximum SNR will decrease. This is due to the fact that a faster slewing signal will exhibit a higher voltage error with the same amount of jitter. For input signals with relatively low-frequency content, say under 1MHz, clock jitter becomes less critical only if the resolution of the ADC is not very high. As an example, if f_{in}=1MHz and t_j=1psec, the ADC's SNR does not exceed 104dB (17-bits, in the best case). Nevertheless, when the frequency of the input signal reaches several hundred-megahertz, clock jitter becomes the dominant source of error and acts as the limiting factor for SNR.

An N-bit SAR ADC typically requires a minimum of N+1 cycles to digitize a continuous input signal. The initial cycle is usually designated for input sampling, while the subsequent N cycles are used for the conversion process. Although jitter during the conversion cycles do not affect the SAR ADC's performance, any inaccuracies during the sampling phase would directly impact the overall performance of the ADC. The clock synthesizer will not be designed or discussed. However, a supplementary analysis of jitter in the Ring Oscillator (RO) block will be presented for future work.

In general, ROs are the main contributors to the jitter in most RO-based frequency synthesizers. In the discussion that follows, we prove that for a CMOS inverter, the variance of the jitter is quadratically proportional to the period of the signal when flicker noise is dominant. Further, we show that consuming much power would not necessarily result in a better phase noise. For a given oscillation frequency of f_0, and a current consumption I, increasing supply voltage V_{DD} will deteriorate the close-in phase noise; a point of contrast to far-out phase noise where it is improved by larger V_{DD}s. The results are confirmed by means of circuit simulations.

5.1. Jitter in Ring Oscillators

Due to their ease of integration, compact layout, wide tuning range, and ability to generate multiple-phase outputs, Ring Oscillators (ROs) find applications in various scenarios [39]. One application of ROs is their use in Phase Locked Loop (PLL) based clock generations. Thus, the noise performance of these oscillators, namely jitter, is one of the primary concerns for the design. Examining the instantaneous phase perturbations, which is often done in phase domain, the phase noise is derived [40–42]. Time-domain analysis of noise requires autocorrelation function of the noise sources [43]. Basically, phase noise is the instability of the frequency expressed in frequency domain; while jitter is fluctuation of the signal waveform in the time domain. Although phase noise is rapidly preferred in radio frequency communications, in digital systems, jitter is favored. The simplest way to calculate the equivalent jitter is to obtain the integrated phase noise power over the desired range of frequency i.e., the area of the phase noise curve. However, studying the jitter directly in time domain is more natural since it is a time domain phenomenon.

In a RO-based clock generator, the RO is almost always integrated within the PLL where low frequency components of the phase noise, namely up to $1/f^3$ (phase noise corner f_c), are usually inside the loop bandwidth so that their contribution is filtered out by the loop filter [44]. In other words, thermal noise is typically assumed to be the only contributor to the overall jitter or phase noise. Nevertheless, in the latest deep submicron processes, this assumption is no longer valid as the corner frequency

of ring oscillators is pushed to tens and even hundreds of megahertz [39]. On the other hand, the lock time is inversely proportional to the loop bandwidth in most PLL types. Even though the corner frequency f_c in phase noise plot can be lowered partly by improving waveform symmetry [45], the applicability is limited to current-starved ring oscillators [42]. Therefore, even with a reasonable attenuation by the loop filter within the PLL bandwidth, up-conversion of the flicker noise may become apparent as feature size shrinks.

If the oscillator is in open-loop configuration, any uncertainty in an earlier transition affects all the following transitions, and its effect persists indefinitely. In other words, jitter accumulates [45]. Figure 5.1(a) shows the accumulated jitter (long-term jitter) versus the time elapsed on a log-log plot. In the region containing the line with slope of 1/2, jitter grows with the square of the time where the thermal noise of the devices usually matters the most. On the other region where the slope of the line is 1, jitter increases linearly with time and the flicker noise is predominant. κ and ζ are called proportionality constants [45, 46]. The jitter in a ring oscillator due to thermal noise sources is calculated and the relationship between κ and the phase noise is derived in [40, 45]. Further, they obtain the phase noise with 1/f noise sources; however, no analytical model was provided to calculate ζ. This is because the integral describing the link between jitter and phase noise is not readily solvable for 1/f noise sources.

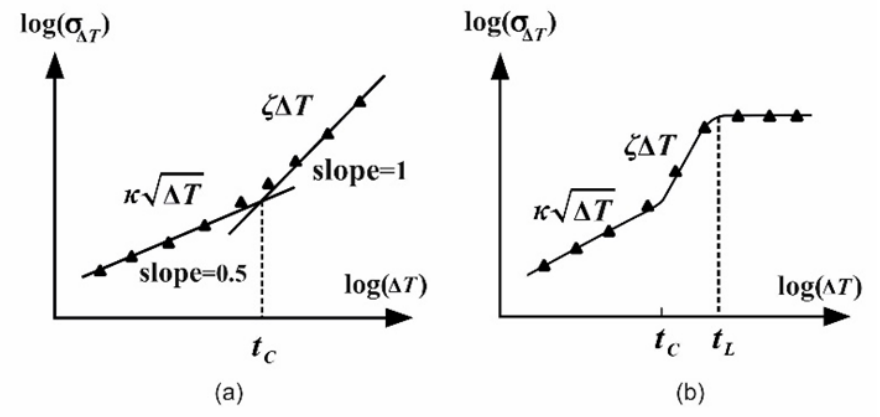


Figure 5.1. RMS jitter in a) open-loop RO b) closed-loop RO with $f_L < f_c$

A measurement-based solution is presented in [46] to particularly solve ζ and using this solution, [47] establishes the link between phase noise and jitter when flicker noise is dominant. Nevertheless, the theory supporting the measurement is still missing. As discussed above, in the case that the PLL loop bandwidth f_L is lower than the phase noise corner frequency, low frequency components of the noise are not sufficiently attenuated. f_c and f_L in the frequency domain correspond to t_c and t_L in the time domain, respectively. As shown in Figure 5.1(b), if $f_L < f_c$, then $t_L > t_c$ and the jitter due to $1/f$ noise is non-negligible. This effect is expected to become more pronounced as feature sizes scale down.

5.2. Time Domain Analysis of Noise

A time domain analysis of noise problems, either stationary or nonstationary, proves beneficial to determine timing jitter since the variance of the output noise is a function of time, and jitter can be measured from the rms value of the noise at the output. To perform such an analysis, the auto-correlation function R_{xx} (t_1,t_2) of the input noise process is needed where t_1 and t_2 are arbitrary time points in the noise signal. An example of low frequency noise signal is shown in Figure 5.2 where it is often assumed that $0 \leq t_1 \leq t_2$ [43, 48]. For a circuit with impulse response of $h(t)$, the auto-correlation function at the output is given by

$$R_{yy}(t_1, t_2) = h(t_1) * R_{xx}(t_1, t_2) * h(t_2). \tag{5.2}$$

The asterisk denotes the convolution operation. This gives the noise variance for the zero-state response. With initial conditions statistically independent of the noise sources, their effect is considered independently and then superposition is applied to perform a complete time-domain noise analysis. The variance of the output noise as a function of the auto-correlation is

$$\sigma_y^2 = E[y(t)y(t)] = R_{yy}(t_1, t_2)\Big|_{t_1=t_2=t}. \tag{5.3}$$

So, the output noise is obtained by first calculating $R_{yy}(t_1, t_2)$ and then substituting $t_1 = t_2 = t$. For a white noise step input, which is a stationary process, the input auto-correlation is a delta function $R_{xx}(t_1, t_2) = (1/2)S_x\delta(t_1 - t_2)$, where S_x is the one-sided white noise power spectral density (PSD) of the underlying noise process and the delta function signifies that the noise at different times is uncorrelated. The output variance then simplifies to

$$\sigma_y^2 = \frac{1}{2}S_x \int_0^t |h(\alpha)|^2 d\alpha. \tag{5.4}$$

Therefore, to solve for the output voltage variance due to the white noise in a rectangular time window from 0 to t, all that is required is the input white noise spectrum and the impulse response of the system [43].

Figure 5.3(a) demonstrates an inverter-based RO that consists of three inverter stages whereas Figure 5.3(b) depicts the model of M_1 where C denotes C_L plus all other parasitics from output to the ground and R denotes the output resistance. The charge (or discharge) current and the noise current are designated with I_0 and I_n, respectively. The input and output waveform for a single inverter are shown in Fig. 5.3(c). As V_{in} exceeds V_{th} at t_0, the NMOS transistor turns on, and the output starts to decrease from V_{DD}. The propagation delay t_d is defined as the time between the instants when V_{in} and V_{out} cross $V_{DD}/2$, i.e., $t_d = t_3$ - t_1. From t_0 to t_2, the NMOS transistor operates in its saturation region and continuously injects increasing flicker noise and thermal noise into the capacitor. Afterwards, the NMOS enters the triode region, reducing the flicker noise current. Meanwhile, the thermal noise current decreases from $4KT\gamma_n g_{mN}$ to a slightly lower value, $4KT/R$, where R denotes the channel resistance of the NMOS with V_{GS}=V_{DD}. Prior to the NMOS fully turning on, the PMOS transistor is in deep triode, acting like a resistor and depositing KT/C noise across C [41].

To calculate the overall noise voltage on the capacitor, an accurate estimate of the integration time window in Equation (5.4) is vital. Abidi [40] uses the propagation delay as the noise integration time window by approximating the PSD of the injected noise current to be constant during the transition time. However, this approach may

overlook some of the injected noise occurring between t_0 to t_1 and from t_3 onwards. This is because the area under the rectangle window t_d does not precisely match the practical noise envelope shape. A modified approach for selecting the starting time of the noise injection is introduced in [41]. One can characterize the detailed transition of noise current PSD by the ISF function, first introduced by Hajimiri [45], and predict the same result as in [41].

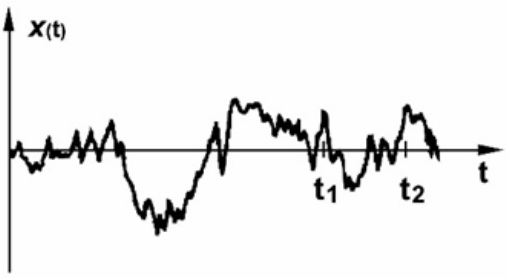


Figure 5.2. A low frequency noise signal x(t)

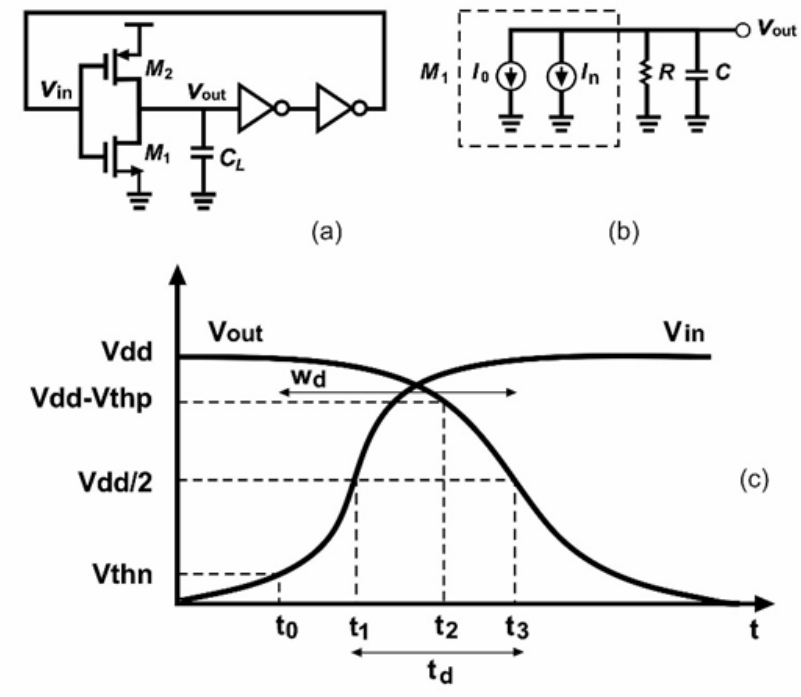


Figure 5.3. a) Inverter-based RO b) circuit model and c) its waveforms

In the analysis provided here, we make the following approximations:

1. We define the rectangular window in Eq. (5.4) as $w_d = t_3 - t_0$ to highlight the importance in choosing the integration time window.
2. Pull-down and pull-up currents are equal $I_P = I_N = I$).
3. Propagation delays of NMOS and PMOS devices are equal ($t_{dPMOS} = t_{dNMOS} = t_d$).
4. Switching point of the inverter is supposed to occur at $V_{DD}/2$. Thus, $t_d = CV_{DD}/2I$ and

$$f_0 \approx \frac{1}{2Mt_{\mathrm{d}}} = \frac{I}{CMV_{\mathrm{DD}}}. \tag{5.5}$$

Further, as in [40,41], we assume the spectrum S_x is constant over the integration time window. If the noise voltage variations are small at the switching point, the standard deviation of the noise voltage projects back to timing jitter by the slew rate (I/C)

$$\sigma_t^2 = \left(\frac{v_n}{I/C}\right)^2. \tag{5.6}$$

In a ring oscillator, Eq. (5.6) will continue to accumulate noise as it circulates around the loop.

5.2.1. Thermal Noise Components

The impulse response from the input to the output in Figure 5.3(b) is

$$h(t) = \frac{1}{C}\exp\left(\frac{-t}{RC}\right). \tag{5.7}$$

Considering only thermal noise source, Eq. (5.7) quantifies the output noise voltage in a w_d time interval as

$$v_{n_w}^2(t) = \frac{S_w}{2C^2}\int_0^{w_d} |e^{-t/RC}|^2 dt = \frac{S_w R}{4C}\left(1 - e^{-2w_d/RC}\right), \tag{5.8}$$

where $S_w = 4KT\gamma_n g_{mN}$. The noise integration time window, w_d, is composed of two parts. As shown in Figure 5.3(c), in $t_0 - t_1$, V_{in} is being charged by the pullup transistor of the previous stage, so that $t_1 = RCln(2 - 2V_{TH}/V_{DD})$. Thus, w_d is calculated as

$$w_d \approx t_d + RC \ln\left(2 - \frac{2V_{TH}}{V_{DD}}\right), \tag{5.9}$$

where R denotes the PMOS (of the previous stage) channel resistance in the triode region with V_{SG}=V_{DD} and V_{SD}=$V_{DD}/2$. Consequently, C equals C_L plus parasitic capacitance of the node V_{in} in Figure 5.3(a). Note that the value of the current I in t_0, t_1, t_2 and t_3 are not the same, however, we presume all to be equal for ease of calculation.

We summarize Eq. (5.8) such that the exponential part is used as an approximate boundary between the three cases.

- $w_d \ll RC/2$. This condition is satisfied if the NMOS transistor still operates in saturation at the toggle point t_3. That is, V_{DD} needs not to be much greater than $2V_{TH}$. Then $w_d \sim t_d$ in Eq. (5.9) and it follows that

  $$v_{nw}^2(t) = \frac{S_{xw}}{2C^2} t_d. \tag{5.10}$$

  It indicates that the integrated thermal noise can be treated as a random walk with time segments of t_d [41].
- $w_d \sim RC/2$. This is very likely to happen if V_{DD} is relatively greater than $2V_{TH}$. Hence, w_d is given by Eq. (5.9). Nevertheless, even in the worst case when $V_{DD} \gg 2V_{TH}$, the leakage caused by NMOS in the triode region is about $\sim$2dB [40].
- $w_d \gg RC/2$. For the time period sufficiently higher than the toggle point, the NMOS transistor goes into the deep triode region and as previously stated, the thermal noise current is now $4kT/R$.

Considering the initial noise deposited by the pullup transistor to the capacitor C as KT/C and using Equations (5.6) and (5.7), the jitter due to thermal noise is

$$\sigma_{\tau w}^2 = \frac{2kT}{I}\left(\frac{\gamma_N + \gamma_P}{V_{DD} - V_{TH}}\frac{w_d}{t_d} + \frac{1}{V_{DD}}\right)\left(\frac{1}{f_0}\right). \tag{5.11}$$

Assuming $w_d \sim t_d$, it reduces to [40, 47]

$$\sigma_{\tau w}^2 = \frac{2kT}{I}\left(\frac{\gamma_N + \gamma_P}{V_{DD} - V_{TH}} + \frac{1}{V_{DD}}\right)\left(\frac{1}{f_0}\right). \tag{5.12}$$

5.2.2. Flicker Noise Components

Flicker noise is a non-stationary random process, but it is usually modeled by a "stationary" and colored stochastic process for practical purposes with PSD given by $S_{1/f} = \alpha/f$. Treating $1/f$ noise as a non-stationary random process would eventually give rise to an autocorrelation function approximated in [48] as

$$R_{(1/f)}(t_2, \tau) = \ln\left(\frac{4t_2}{|\tau|}\right)u(\tau) \quad \text{only if} \quad t_2 \gg \tau, \tag{5.13}$$

where t_2 is the time elapsed since the noise process has started and the observation time $\tau = t_2 - t_1$ is much shorter than t_2. Observing the process for a finite interval will always yield a finite variance. In effect, Equation (5.13) is approximately stationary. Nevertheless, this would not be applicable to our case since we observe the noise from where it begins at t_0 to the toggle point t_3.

On the other hand, $1/f$ noise as a stationary process is not well-defined since it becomes non-finite at $f \sim 0$. However, in physical devices, as the frequency decreases, the dynamics of the flicker noise change slowly when compared with the time of observation, so that it is considered static for practical purposes [48]. In other words, as frequency decreases, from a point on, the spectrum deviates from $1/f$ and it attains nearly a finite value at $f = 0$. This point is called the flicker noise cutoff frequency Υ_c [49]. This would give rise to a well-defined stationary stochastic process model for

flicker noise. Using the following integral representation for a one-sided $S_{1/f}(f)$,

$$S_{1/f}(f) = \alpha \cdot \frac{1}{f} = \alpha \int_0^\infty \frac{4}{x^2 + (2\pi f)^2} dx. \tag{5.14}$$

By introducing the cutoff frequency Υ_c in Equation (5.14), we have

$$S_{1/f}(\omega) = \alpha \int_{\Upsilon_c}^\infty \frac{4\,dx}{x^2 + (2\pi f)^2} \tag{5.15}$$

$$= \alpha \left[\frac{2\pi}{|j\omega|} - \frac{4}{\omega} \tan^{-1}\left(\frac{\Upsilon_c}{\omega}\right) \right], \tag{5.16}$$

where $\omega = 2\pi f$ and $S_{1/f}(\omega)$ has now a finite value at zero, $S_{1/f}(0) = 4/\Upsilon_c$. [49] uses numerical methods to first compute the variance corresponding to the integral in Eq. (5.15) and then estimate the phase noise. Although the numerical methods are suitable for circuit simulators, they often involve too complicated calculations and bring little insight into the behavior of the circuit. We propose here a straightforward approach that gives a clear insight to deal with flicker noise in ring oscillators. Together with time domain analysis, the output voltage noise is estimated.

Observing carefully the spectrum in Equation (5.16), the first term inside the brackets estimates the magnitude of a half-order low pass filter. One may write the spectrum of the flicker noise as [50],

$$\frac{2\pi}{|j\omega|} \quad \longleftrightarrow \quad \alpha\frac{1}{f} \quad \longleftrightarrow \quad 2\pi\alpha \left| \frac{1}{\sqrt{j\omega}} \right|^2. \tag{5.17}$$

On the other hand, the second term in Equation (5.16) simply defines the cutoff frequency Υ_c. The integral in Equation (5.15) then simplifies to

$$S_{x1/f}(s) = 2\pi\alpha \left| \frac{1}{\sqrt{s + \left(\frac{\pi\Upsilon_c}{2}\right)}} \right|^2, \tag{5.18}$$

where $s = j\omega$. Depicted in Figure 5.4, with $\Upsilon_c = 10kHz$ and $\alpha = 1$, we recognize that Equations (5.16) and (5.18) are practically identical. This proves the observation we made above. For an increase of a decade in frequency above Υ_c, the magnitude drops by 10dB, resembling a half-order low pass filter. Recall from the basics of the noise problems in the frequency domain, Eq. (5.18) reminds us of white noise with a power spectral density of $2\pi\alpha$ applied to a filter whose transfer function is

$$F(s) = \frac{1}{\sqrt{s + \pi\Upsilon_c/2}}. \tag{5.19}$$

In this case, the output spectrum $S_{1/f}(s)$, assumes the shape of the filter's frequency response [44]. That is, to solve for the flicker noise, we will presume a white noise spectrum with PSD of $2\pi\alpha$ applied to a filter whose transfer function is

$$G(s) = F(s) \cdot H(s), \tag{5.20}$$

where $H(s)$ is the Laplace representation of Eq. (5.7).

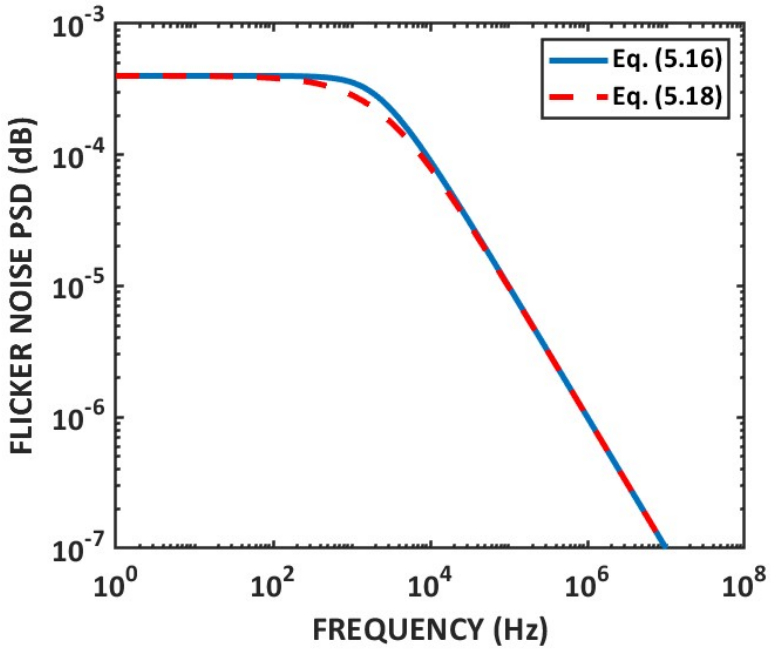


Figure 5.4. Flicker noise PSD approximation

The conceptual schematic of the overall approach with $1/f$ noise sources is shown in Figure 5.5. This observation is beneficial since Eq. (5.18) still has an acceptable form even for Υ_c=0. To solve for the output noise variance, we first find the time domain representation of Eq. (5.19) and then apply Eq. (5.20). Inverse Laplace transformation of $F(s)$ can be found as

$$F(s) = \frac{1}{\sqrt{s + \pi\Upsilon_c/2}} \quad \rightarrow \quad f(t) = \frac{1}{\sqrt{\pi t}} e^{-\frac{\pi}{2}\Upsilon_c t}. \tag{5.21}$$

Next, $h(t)$ and $f(t)$ are convolved for t>0

$$g(t) = \int_0^t f(\tau) \cdot h(t-\tau) d\tau. \tag{5.22}$$

The integral is often presented with limits of positive and negative infinity. However, since $f(\tau)$ and $h(t-\tau)$ are zero for $t < 0$, and $g(t)$ would later be applied only in a time span of w_d, we limit the integral from 0 to t. We have,

$$g(t) = \int_0^t \frac{1}{\sqrt{\pi\tau}} e^{-\frac{\pi}{2}\Upsilon_c \tau} * \frac{1}{C} e^{-\frac{(t-\tau)}{RC}} d\tau = \frac{e^{-\frac{t}{RC}}}{\sqrt{\pi C}} \int_0^t e^{(\frac{1}{RC} - \frac{\pi\Upsilon_c}{2})\tau} \frac{d\tau}{\sqrt{\tau}}. \tag{5.23}$$

Marking the index of the exponential term as u^2 and using the equivalent $(\sqrt{\pi}/2) - \text{erfi}(u) = \int e^{u^2} du$, Eq. (5.23) is calculated as

$$g(t) = \frac{2e^{-\frac{\pi}{2}\Upsilon_c t}}{C\sqrt{\pi}\sqrt{\left(\frac{1}{RC} - \frac{\pi}{2}\Upsilon_c\right)}} F\left(\sqrt{\left(\frac{1}{RC} - \frac{\pi}{2}\Upsilon_c\right) t}\right), \tag{5.24}$$

where $F(.)$ is called Dawson Function [51]. In practice, $\pi\Upsilon_c/2$ is much less than $1/RC$, then Eq. (5.24) reduces to

$$g(t) = \sqrt{\frac{4R}{C\pi}} e^{-\frac{\pi}{2}\Upsilon_c t} F\left(\sqrt{\frac{t}{RC}}\right). \tag{5.25}$$

One would reach the same result as in Eq. (5.25) with $\Upsilon_c = 0$ and solve the inverse Laplace transformation of $(\sqrt{s}.C(s + 1/RC))^{-1}$.

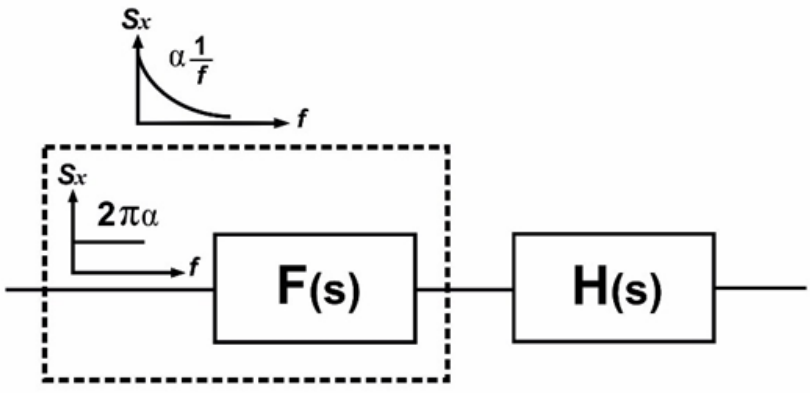


Figure 5.5. Conceptual schematic of the system with flicker noise PSD

As shown in Figure 5.6, the overall impulse response of the system would presume a Dawson function-like shape if flicker noise is considered, unlike with the thermal noise where it depends on exponentially decaying function (see Eq. (5.8)). The foregoing analysis reveals several useful insights. As a first boundary, if $t \ll RC$, then $F(\sqrt{x}) \approx \sqrt{x}$ [51]. In this case V_{DD} is not much greater than $2V_{TH}$, and then $w_d \approx t_d$. Using Eq. (5.8), the output noise voltage is

$$v_{n1/f}^2(t) = \frac{1}{2}(2\pi\alpha)\frac{4R}{C\pi}\int_0^{w_d} e^{-\pi\Upsilon_c t}|F(\sqrt{t/RC})|^2 dt \tag{5.26}$$

$$\approx \frac{2\alpha}{C^2}t_d^2\left[1 - \frac{\pi\Upsilon_c}{3}t_d + \frac{\pi^2\Upsilon_c^2}{16}t_d^2 - \frac{\pi^3\Upsilon_c^3}{240}t_d^3 + \cdots\right], \tag{5.27}$$

where $\alpha = K_f g_{mN}^2/WLC_{ox}$. This expression clearly indicates that the noise voltage (and consequently the jitter) attributed to flicker noise will grow with the square of elapsed time, consistent with the measurement findings presented in [46]. The implication is valid only if the observation time is way smaller than the RC time constant. When they become comparable, i.e., $t \sim RC$, the filter $g(t)$ reaches its maximum and thereafter starts decaying (see Figure 5.6), i.e., after a point in time, $v_{n1/f}^2(t)$ would not increase with the square of time. To further elaborate on this point, we numerically calculate the integral in Eq. (5.26), where we ignored the effect of Υ_c for simplicity. Depicted in Figure 5.7, when $t \ll RC$ the noise increases with the square of time shown

with gray dashed line. In the meantime, as the observation time gets closer to the time constant RC, the integrated noise deviates from what Eq. (5.27) predicts but it still increases. In other words, as time elapses, unlike the thermal noise where it eventually attains a constant value (see Eq. (5.8)), flicker noise deviates from a square shape but keeps rising somewhat logarithmically. Nevertheless, for times sufficiently higher than the time constant τ ($t \gg RC$), the NMOS is in deep triode and the flicker noise subsides due to lower bias currents [52].

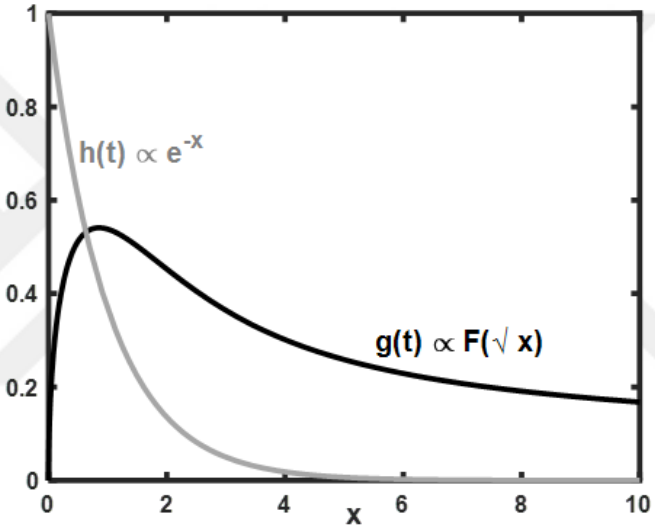


Figure 5.6. $h(t)$ and $g(t)$ with t normalized to $RC (x = t/RC)$

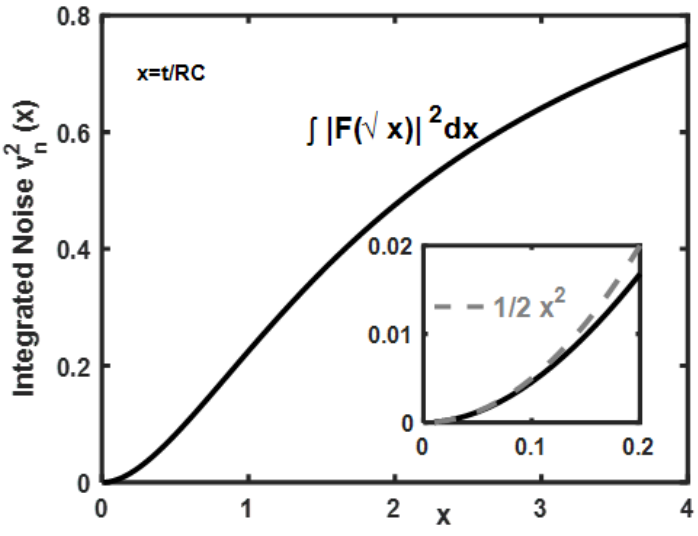


Figure 5.7. Integrated noise voltage with numerical integration

Similar to the solution for the thermal noise, the jitter due to flicker noise is obtained as

$$\sigma^2_{\tau_{1/f}} = \frac{K}{MI}\left(\frac{\mu_n K_{fn}}{L_n^2} + \frac{\mu_p K_{fp}}{L_p^2}\right)\left(\frac{1}{f_0^2}\right), \tag{5.28}$$

where K with $w_d \ll RC$ is

$$K \approx \left(\frac{w_d}{t_d}\right)^2 = \left(1 + \frac{RC}{t_d}\ln\left[2 - \frac{2V_{TH}}{V_{DD}}\right]\right)^2. \tag{5.29}$$

The jitter equation in Eq. (5.28) was not directly obtained in time domain so far. It was, however, predicted in previous work [47], based on the measurement results from [46], in which $K \sim 3$.

What Eq. (5.28) and Eq. (5.29) predict is, if V_{DD} is low ($V_{DD} \sim 2V_{TH}$), K falls to 1. Thus, the contribution of flicker noise on the overall jitter is minimal. However, if $V_{DD} \gg 2V_{TH}$, K attains a maximum value of $(1 + 0.7RC/t_d)^2$. This implies that the contribution of flicker noise to the overall jitter is now more pronounced. In other words, increasing V_{DD} exacerbates the jitter due to flicker noise, a contradict point to the white noise induced jitter.

5.2.3. Simulation Results

For a given oscillation frequency of f_0, t_d is fixed and the integrated noise across the capacitor C is minimum if the RC time constant is maximum. This holds for each of the noise types, i.e., $1/f$ or thermal noises. The fact is, with t_d and w_d far smaller than $\tau = RC$, the noise voltage increases linearly with time when thermal noise is dominant and quadratically with time when flicker noise is dominant. As long as the conditions above are met, output noise includes the factor w_d/t_d. The lower the integration time window w_d, the less the noise is being integrated. Thus, with $V_{DD} \sim 2V_{TH}$, the integrated noise voltage is further minimized. The jitter due to thermal noise sources in Equation (5.11), rising V_{DD} increases the factor w_d/t_d, however, the other factors are far more dominant so that they prevail the slight increase in w_d/t_d. For the case of

flicker noise, Equation (5.28) has no net dependence on V_{DD}. Rising V_{DD} will increase w_d/t_d, and consequently the jitter. In other words, the jitter with a thermal noise source benefits from higher V_{DD}, while it detriments the jitter with a flicker noise source. To verify the theory developed above, as a first setup, we design two inverter-based ring oscillators in a 180nm CMOS process where in both designs $M = 7$ and $L_n = L_p = 400nm$. To guarantee a fair comparison, the output frequency is fixed at 300MHz and the average current drawn from V_{DD} is $I = 1.64mA$.

With the sizing given as, 1) $W_p = 35\mu m$, $W_n = 6.4\mu m$, and $V_{DD} = 1.8V$, and 2) $W_p = 102\mu m$, $W_n = 18\mu m$, and $V_{DD} = 1.2V$, rise time and fall time would nearly be equal. The load capacitor C_L is chosen so that f_0 in each oscillator is 300MHz. Figure 5.8 shows the long-term jitter plot for both cases. Lowering V_{DD} increases jitter due to thermal noise while it decreases jitter due to flicker noise. For example; after 300 cycles, the jitter is 2psec lower with $V_{DD} = 1.2V$. In addition, since phase noise and jitter are different ways of quantifying the same phenomenon, the close-in phase noise should also be improved with lower V_{DD}. Figure 5.9 shows the phase noise of both oscillators where nearly 1.7dB improvement is achieved with lower V_{DD}. Note that none of the phase noise calculations in [39–42, 45–47] predict this.

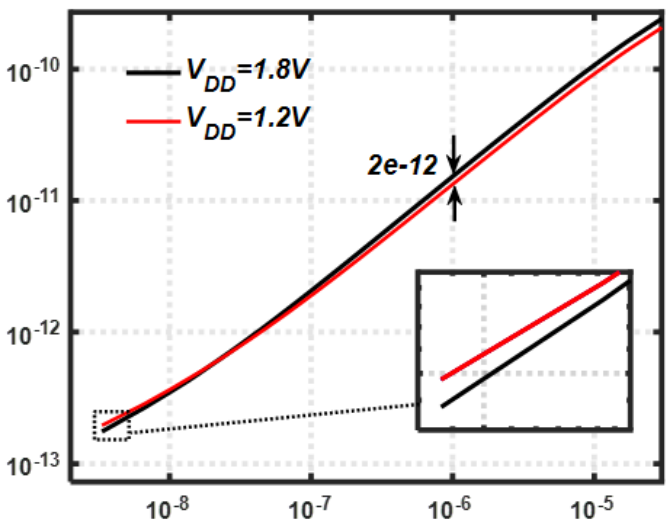


Figure 5.8. Accumulated jitter of both oscillators

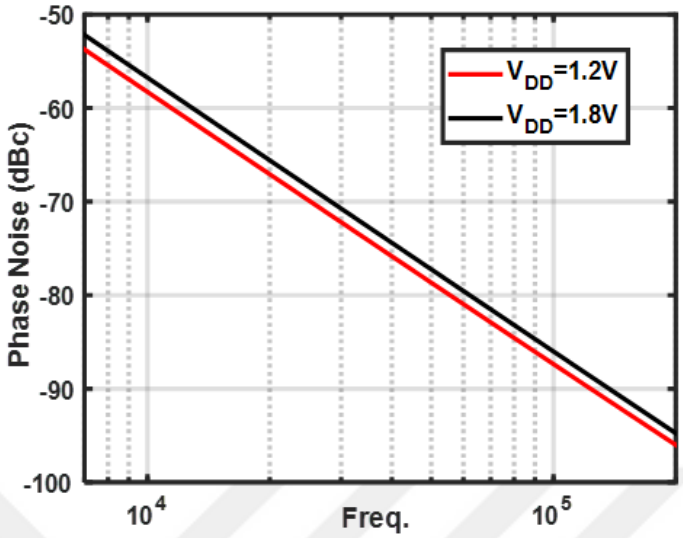


Figure 5.9. Flicker noise components of the phase noise

Thus far, we used long-channel approximations for the circuit parameters and PSD of each of the noise sources. Assuming velocity-saturated devices, our interpretations would still be valid with a slight deviation. The BSIM model of flicker noise spectrum $S_{1/f}$ in [52] has a weak dependency on the charge density at the source and at the drain with V_{GS} and V_{DS} voltages respectively. In simple terms, one may argue that the flicker noise factor K_f, which is assumed constant in long-channel devices, deviates with V_{GS} and V_{DS} for short channel devices. In other words, in a fixed current and geometry, the noise factor K_f is reduced when V_{DD} is lowered. To distinguish the reduction in phase noise with lower w_d/t_d from the reduction arising from K_f, we simulate the test circuit of Figure 5.10(a) as we set off all components' contribution to the output noise except M_1. We swept V_{DD} from 1.2V to 1.8V and measured the noise at 10KHz frequency with $W_1/L_1 = 6.4\mu m/0.4\mu$m. As Figure 5.10(b) shows, K_f is reduced by less than 5% when V_{DD} is lowered from 1.8V to 1.2V. That is about 0.2dB and can simply be ignored.

As for the second setup, we keep the device parameters constant and measure the close-in FoM. Designed in a 65nm CMOS process, for both RO circuits, $M = 7$, $L_n = L_p = 60nm$, $W_p = 9\mu m$, $W_n = 4\mu m$ and, 1) $C_L = 95fF$, with $V_{DD} = 1.2V$, and 2) $C_L = 25fF$, with $V_{DD} = 0.8V$.

For both conditions, the oscillation frequency $f_0 = 1.6GHz$. With V_{DD} of $1.2V$ and $0.8V$, the average current I drawn from the supply voltage is 1.6mA and 0.4mA, respectively. Figure 5.11 plots the simulated phase noise. Although low frequency components are increased by 4dB with $V_{\mathrm{DD}} = 0.8V$, the current consumption I is $4\times$ times decreased. This improves the FoM by 3.6dB. The reduction of K_f at 100kHz frequency offset with $L_{\min}$ was measured to be less than 7%, i.e., < 0.3dB.

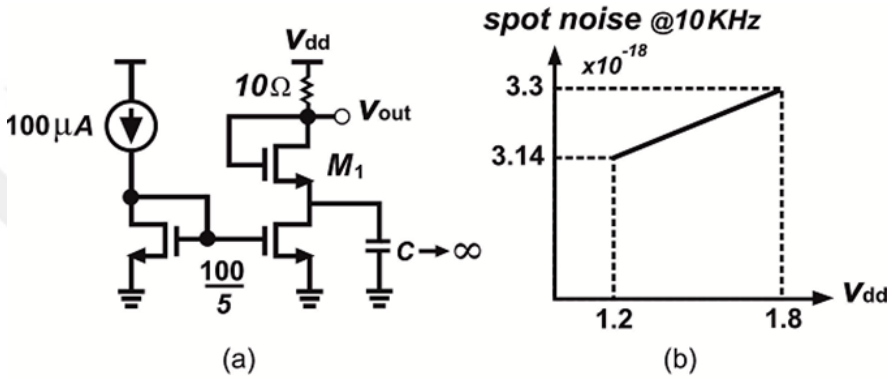


Figure 5.10. a) the test circuit with constant I and varying V_{DD}, b) spot noise @10kHz

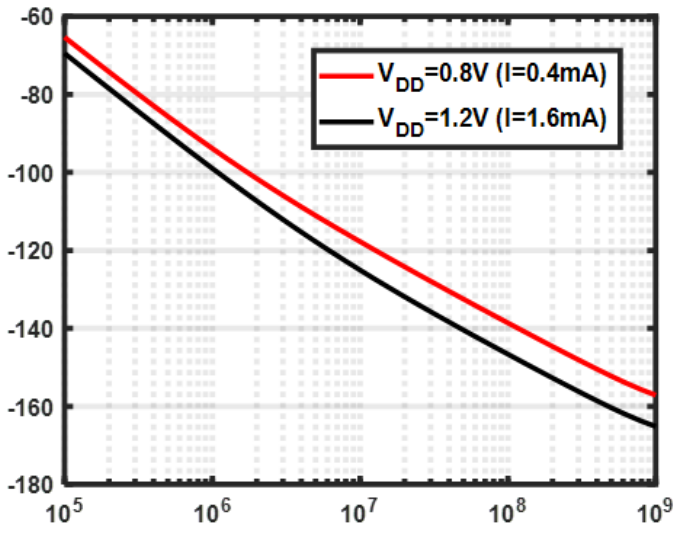


Figure 5.11. Phase noise plot of both oscillators in 65nm tech.

6. SIMULATION RESULTS

Two SAR ADCs have been designed in the 65nm UMC CMOS process node, operating at sampling frequencies of 100kHz and 1MHz, respectively. The ADC sampled at 100kHz operates with a V_{DD} as low as 0.7V, while the ADC sampled at 1MHz is powered by a V_{DD} of 1.2V. As mentioned in chapter 2, the area of the capacitive DAC in the hybrid switching scheme is greatly reduced compared to its conventional counterpart by 75%. This means that for a 12-bit ADC, only $1024C_u$ is needed to perform all 12 conversions [22]. Illustrated in Figure 2.5(a), the MSB capacitor is only $512C_u$, compared to the monotonic scheme with $1024C_u$ and the conventional scheme with $2048C_u$ as the MSB capacitor [9]. Typically, due to the high value of the capacitive DAC, thermal noise is not a significant issue, leaving mismatch as the main source of non-linearity in the DAC design. In other words, the C-DAC should surpass KT/C noise to a lesser value than the LSB size. For a V_{DD} of 0.7V and a resolution of 12 bits, the LSB equals $170\mu V$, and the quantization noise power is given by [1],

$$P_{q_n} = \frac{\Delta^2}{12} = 2.4 \times 10^{-9}, \tag{6.1}$$

where, Δ is the LSB voltage. To maintain a high SNR, we use the equation

$$\mathrm{SNR} = 10 \log \left(\frac{P_S}{P_{q_n} + \frac{KT}{C}} \right), \tag{6.2}$$

where P_S is the signal power. To attain 12-bit accuracy SNR should be 74dB or higher. From Equation (6.2), it is evident that C should be at least 0.5pF. Thus, with the hybrid switching scheme, C_u equals 0.5fF. This significantly decreases the area and noise.

In the 65nm UMC process, the minimum value for a MOM-cap and MIM-cap is approximately 2.63fF and 52fF, respectively. MIM caps typically have excellent immunity to mismatch, while MOM caps are denser and smaller in area. To benefit from the precise matching characteristics of MIM capacitors, we employ an array of MIM

capacitors in the capacitive DAC. Since the minimum value for a MIM-cap is relatively large at approximately 52fF, four MIM-caps are connected in series, resulting in an approximate unit cap value of 13fF. Figure 6.1 displays the 3-sigma error-bar plot of the SNDR of the designed ADC vs. unit capacitor with Monte Carlo analysis enabled. In the simulation, all other blocks were implemented by Verilog-A except the C-DAC. With an increased value in the MOM capacitor, the 3-sigma variation of the SNDR is reduced. However, with a MIM unit cap of 13fF (four 52fF caps being series), SNDR is the highest, and its variation is the lowest. With the hybrid switching scheme, the total sampling capacitor reaches nearly $\sim$ 13.3pF. Despite occupying a larger area, this configuration ensures effective thermal noise suppression and immunity to mismatch effects as well. The significant value of the sampling capacitor also contributes to the elimination of clock feedthrough in the bootstrapped switches [23]. All of these factors contribute to a better SNDR. The layout of the overall chip is shown in Figure 6.2.

On the other hand, the total resistance seen from the sampling capacitor is the series combination of the bootstrapped switch resistance, a constant 50Ω, and the resistance of the input signal source. It is crucial to maintain this resistance at a sufficiently low level to avoid impacting the settling time. In an RC-based sample and hold circuit, the sampling period (t_s) should be much larger than the RC time constant. It follows, $t_s \gtrsim RC \ln\left(2^N\right)$, where N is the number of bits.

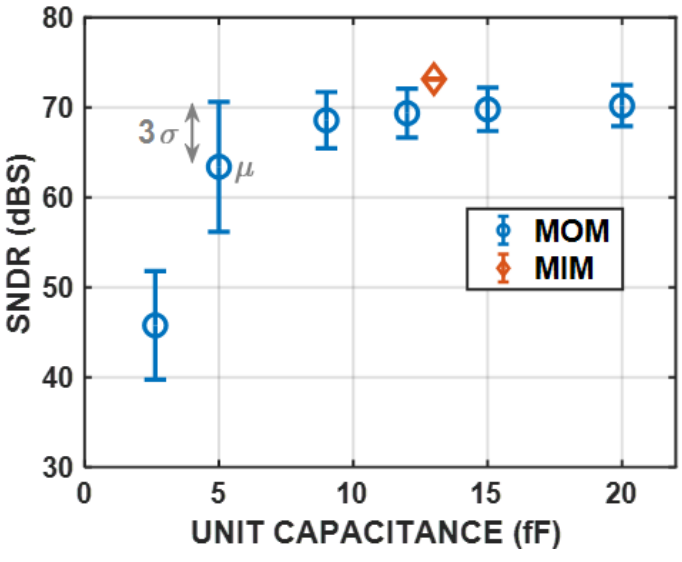


Figure 6.1. SNDR vs. unit capacitor

Figure 6.3 represents the minimum sampling time needed for N bits resolution. For 12-bit accuracy, the sampling period needs to be at least 8.3 times the RC time constant to settle to 99.98% of the input signal. This requirement dictates the value of the resistance R be less than 6kΩ and 600Ω, for 100kHz and 1MHz ADCs, respectively; a condition that can be easily fulfilled.

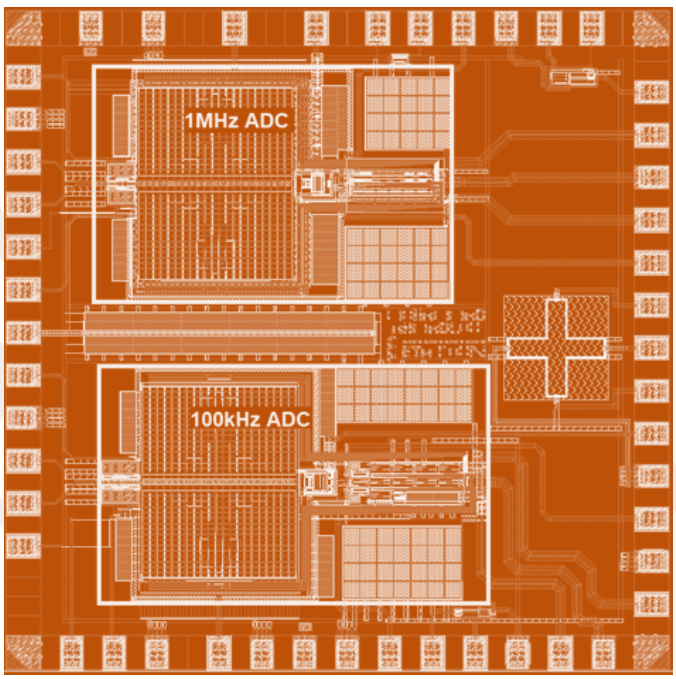


Figure 6.2. Layout of the overall chip (including both ADCs)

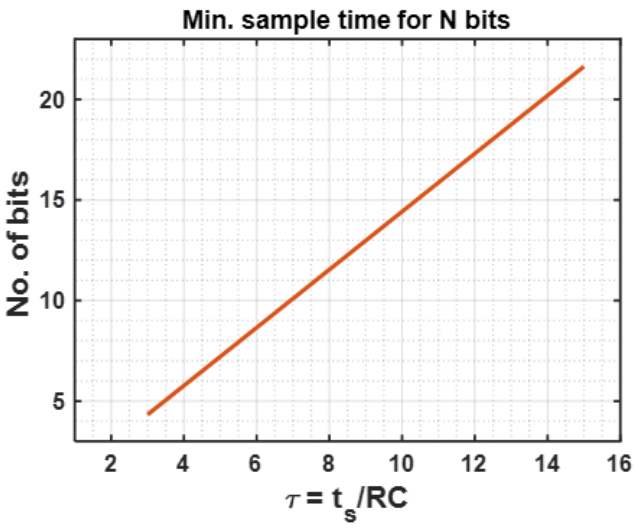


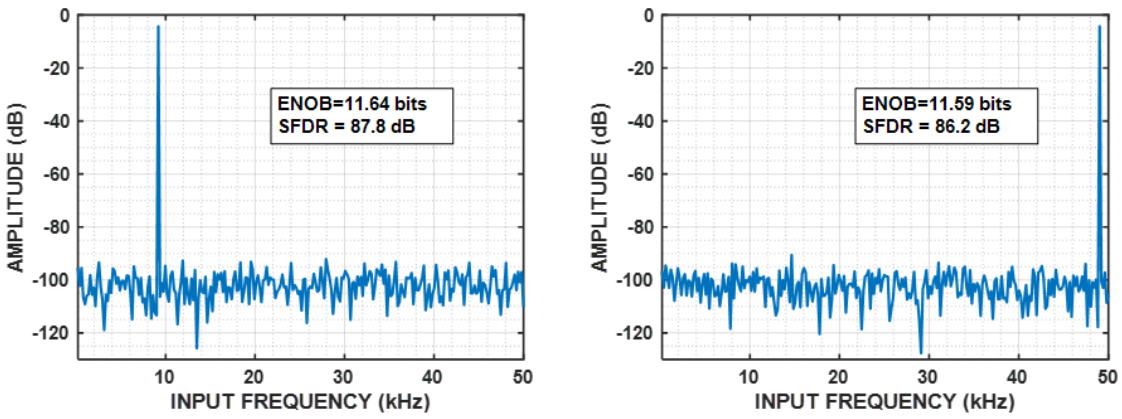
Figure 6.3. Sampling time vs. number of bits achieved in a S/H

6.1. Simulation Results of 100kHz ADC

Post-layout simulation results of the ADC sampled at 100 kHz are presented in this section. With V_{DD} set to 0.7V, Figure 6.4 displays the FFT result of the ADC at both low and Nyquist input frequencies. Due to the high input bandwidth, there is only a slight decrease at the Nyquist input compared to the low input frequency.

A family of curves in Figure 6.5 depicts the post-layout simulation results of the ADC under various corners, temperatures, and supply voltages. The results in Figure 6.4 and Figure 6.5 were obtained with transient noise enabled by setting $f_{\max}$ to 1 GHz and $f_{\min}$ to 200Hz.

SAR ADCs are predominantly digital; thus, variations in V_{DD} and temperature have minimal impact on their functioning, particularly at low speeds. Additionally, we developed a robust BSU that effectively handles PVT variations. Moreover, the preamplifier in the comparator is resistively loaded and biased with I_{SS}, resulting in a reasonable gain of approximately $G_{m1,2}R\left(\frac{I_{SS}R}{V_{DSAT1,2}}\right)$. This gain is largely independent of the supply voltage at the first order and has sufficient gain across all corners and temperature ranges. As a result, the overall ADC shows promising performance.



(a) (b)

Figure 6.4. FFT results of the 100kHz ADC (a) f_{in}= 9.179687kHz (b) f_{in}= 49.023437kHz

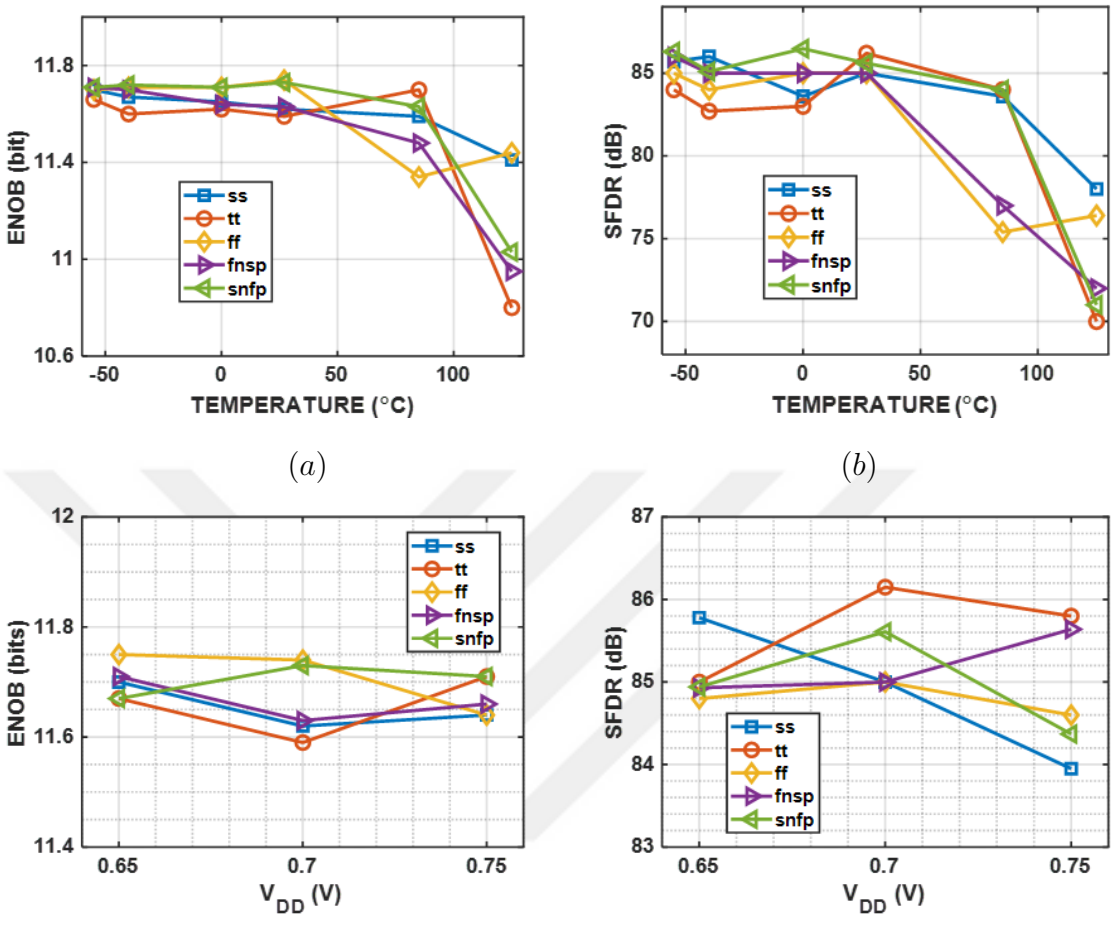


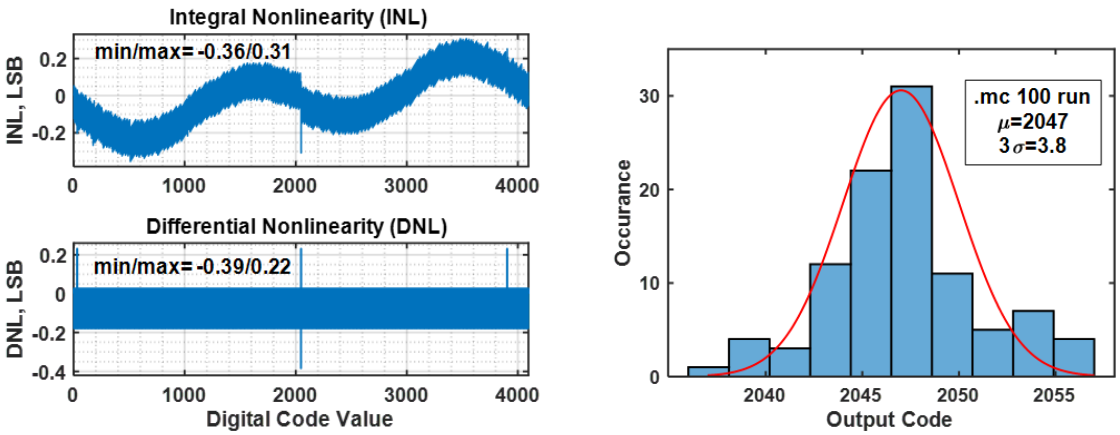
Figure 6.5. 100kHz ADC, (a) ENOB and (b) SFDR vs. Temperature with V_{DD}=0.7V. (c) ENOB and (d) SFDR vs. V_{DD} at 27°C

DNL and INL are two important metrics that describe the performance of an ADC when dealing with non-linearity. In a well-designed ADC, both INL and DNL should be below 1 LSB. Figure 6.6(a) presents the INL and DNL plots of the designed ADC. Thanks to the highly mismatch immune DAC structure and the low offset comparator design, DNL and INL are well below 1-LSB in magnitude, reaching the minimum and maximum values of -0.39/+0.22 for DNL and -0.36/+0.31 for INL. To assess the ADC's resilience against mismatch, Figure 6.6(b) illustrates the output code when the inputs are shorted to V_{CM}, and Monte-Carlo analysis is enabled with 100 runs. The common-mode voltage V_{CM} ($V_{REF}/2$) corresponds to the output code of 2048 in a 12-bit ADC. In the designed SAR ADC, the mean value is 2047, and in the case of mismatch, it

deviates from its mean by less than 4 LSB. This mismatch is mostly due to the 3-sigma deviation we previously measured in the pre-amplifier, being 370µV that is equivalent to around 2.2 LSBs. The results in Figure 6.5 through Figure 6.6 confirm the proposed ADC's high immunity to noise, distortion, and mismatch. Nevertheless, this advantage comes at the cost of a larger area.

The power consumption breakdown is shown in Figure 6.7 for +27°C and +125°C in the typical-typical corner. In ambient temperature, the comparator consumes almost 60% of the power. The SAR block occupies the smallest portion in the power consumption pie with 8%. As the temperature increases, SAR block corresponds to a significant portion, 42%, while the comparator uses 26% of the power.

The performance of the proposed ADC is compared with other works in Table 6.1. Even though the comparator is automatically calibrated in every cycle, the substantial value of the unit capacitor eliminates the necessity for additional calibration in the capacitive DAC against mismatch. The ADC, as summarized in Table 6.1, exhibits promising metrics. It operates over the widest temperature range (-55°C to +125°C), and achieves the lowest DNL/INL values. Although the power dissipated is not the lowest, its high SNDR results in a favorable Figure of Merit (FoM). Nevertheless, the large sampling and decoupling capacitors increase the area compared to other works.



(a) (b)

Figure 6.6. (a) INL and DNL plots of the 100kHz ADC (b) the output code with inputs shorted to V_{CM} in 100kHz ADC

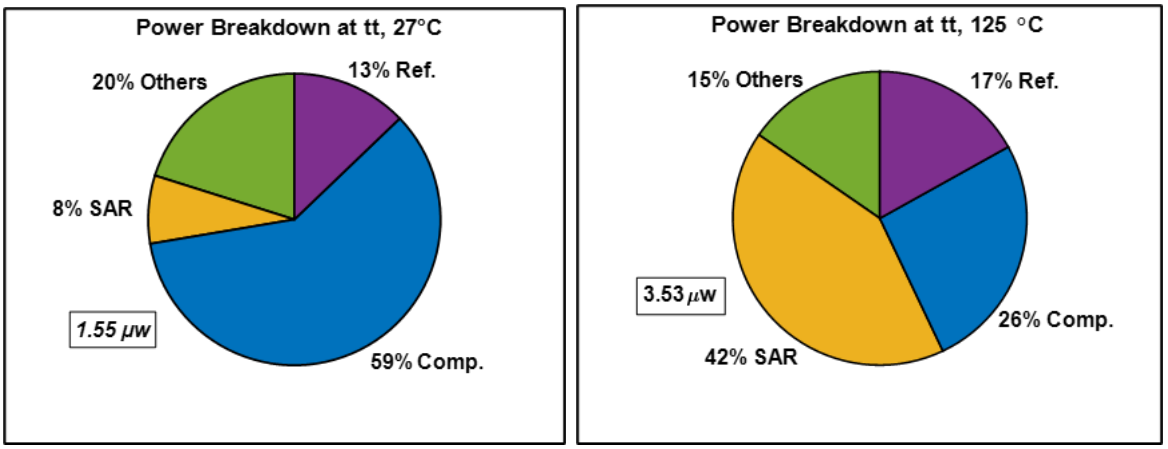


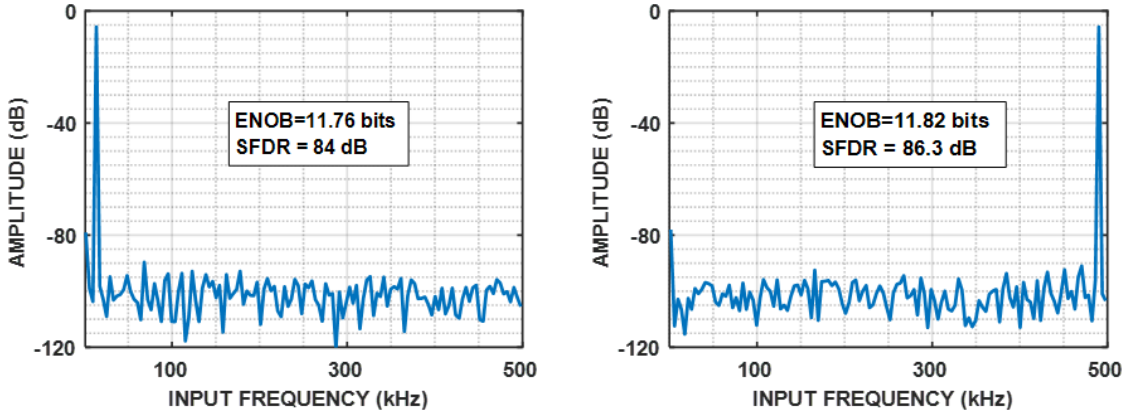
Figure 6.7. Power Breakdown of the 100kHz ADC

Table 6.1. Performance Summary of 100kHz

Parameter	**This Work 2023**	**[53] 2017**	**[21] 2016**	**[54] 2022**	**[55] 2020**	**[56] 2022**
Tech. (nm)	65	65	65	110	180	180
Sampling Freq. (kHz)	100	100	80	200	100	200
No. of bits	12	12	10	10	12	12
Sampling Cap. (pF)	13.3	1.056	0.256	–	0.95	–
VDD (V)	0.7	0.7	0.8	0.95	0.7	1.8 / 1
SNDR (dB)	72.4	64.5	56.6	58.4	63.7	67.4
SFDR (dB)	86	77	65	–	84	73.5
DNL/INL (LSB)	-0.39, +0.22 / -0.36, +0.31	±1 / -1.2, +1.6	0.94 / 0.6	–	±0.45 / -0.55, +0.65	–
Power diss. (µw)	1.55	0.6	0.106	2.24	1.15	5.05
Temp.	-55°C – +125°C	–	–	-40°C – +85°C	–	–
Area (mm2)	0.6	0.03	0.26	0.049	0.06	0.7
FoM (fJ/st.)	4.5	4.5	2.4	16.46	6.6	13.2
Calibration	No	Yes	No	No	Yes	Yes

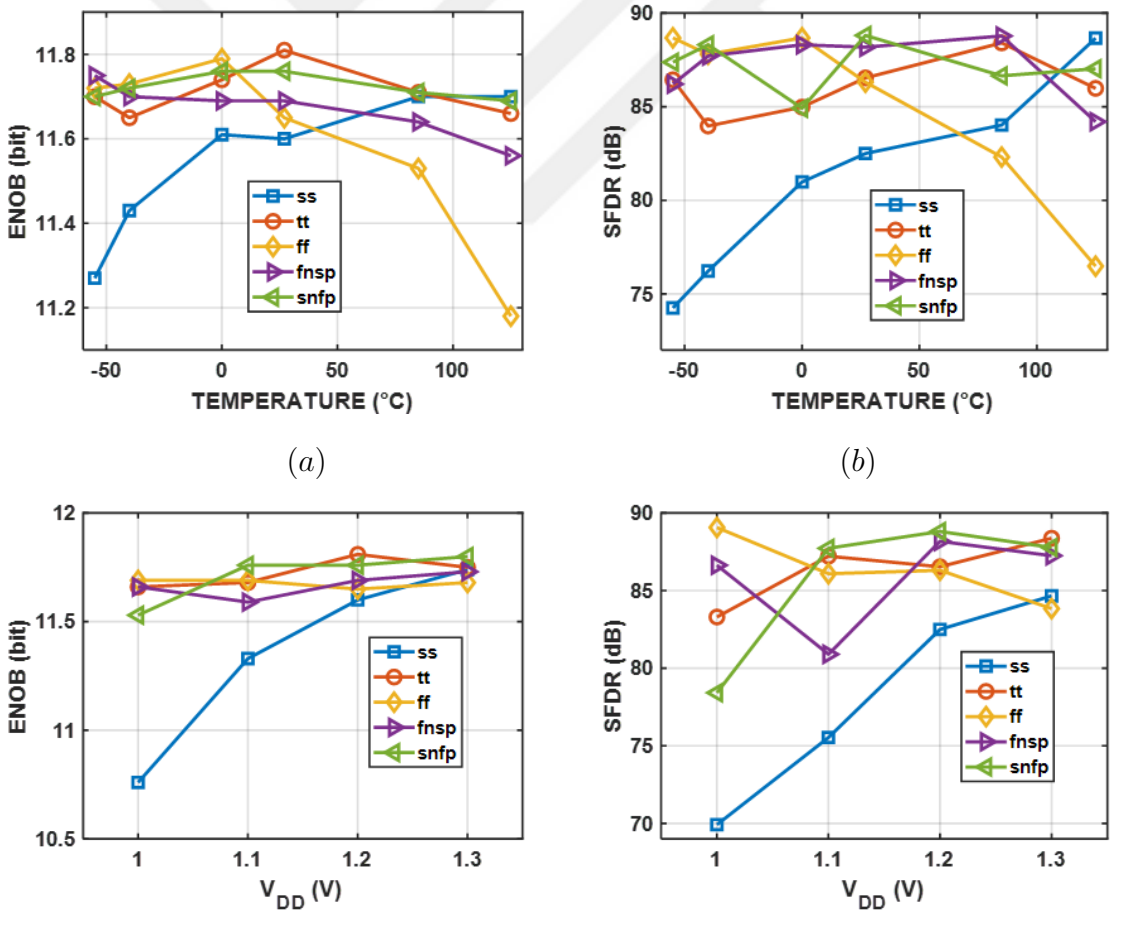
6.2. Simulation Results of 1MHz ADC

This section presents the post-layout simulation results of the ADC sampled at 1MHz rate with a V_{DD} of 1.2V. In Figure 6.8, the FFT results of the ADC are shown. To assess the robustness to PVT variations, Figure 6.9 displays a set of characteristic curves. The INL and DNL plots presented in Figure 6.10(a) confirm the linearity of the ADC, with both metrics consistently below 1 LSB. Specifically, INL ranges from -0.28 to +0.26, while DNL varies from -0.19 to +0.17.



(a) (b)

Figure 6.8. FFT result of the 1MHz ADC (a) f_{in}= 13.6718kHz (b) f_{in}= 490.2343kHz



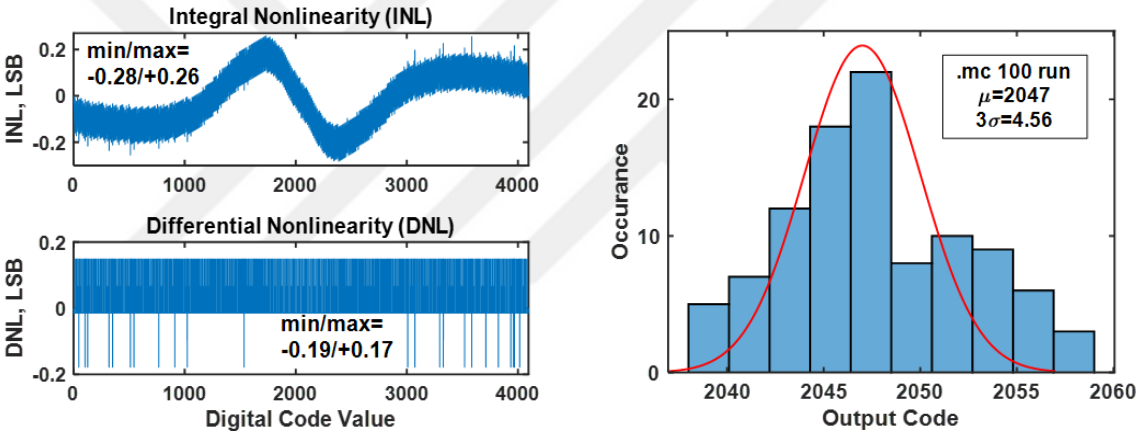
(a) (b)

(c) (d)

Figure 6.9. 1MHz ADC, (a) ENOB and (b) SFDR vs. Temperature with V_{DD}= 1.2V. (c) ENOB and (d) SFDR vs. V_{DD} at 27°C

Figure 6.10(b) demonstrates the ADC's resilience against mismatch through Monte-Carlo analysis with 100 runs, and inputs shorted to V_{CM}. This comprehensive evaluation underscores the ADC's robust performance across diverse operating conditions.

The power consumption breakdown of the 1MHz ADC is illustrated in Figure 6.11. The comparator accounts for about 82% of the power, largely due to the static nature of the preceding preamplifier. As temperature rises, power consumption in other blocks increases, while the comparator's consumption remains nearly constant, leading to a higher relative power share for other blocks.



(a) (b)

Figure 6.10. (a) INL and DNL plots of 1MHz ADC (b) Output code with inputs shorted to V_{CM} in 1MHz ADC

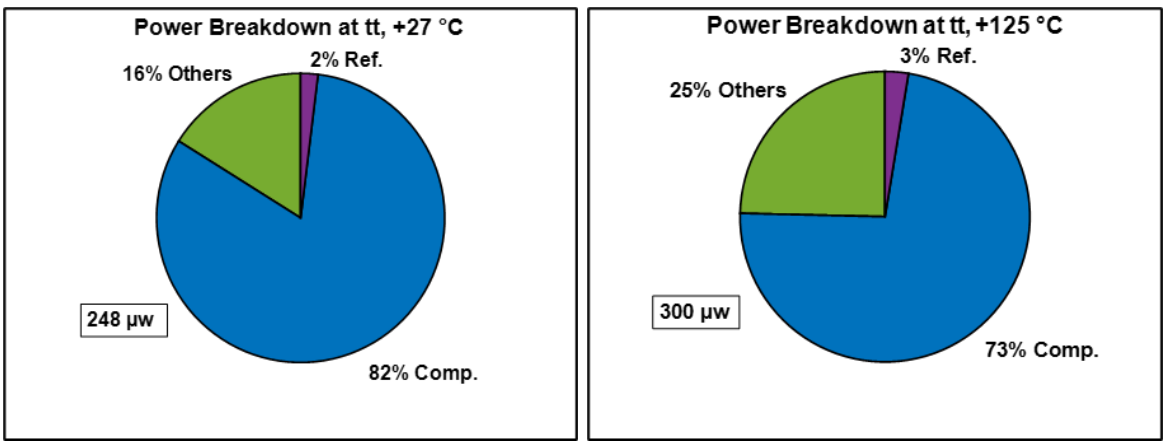


Figure 6.11. Power Breakdown of the 1MHz ADC

A comprehensive performance summary of the ADC is provided, comparing it with other works in Table 4.2.

Table 6.2. Performance Summary of 1MHz ADC

Parameter	**This Work (2023)**	**[57] 2019**	**[58] 2021**	**[59] 2019**	**[60] 2015**
Tech. (nm)	65	180	65	28	130
Sampling Freq. (MHz)	1	5	1-20	4	0.83
No. of bits	12	10	13	12	12
Sampling Cap. (pF)	13.3	2	2.048	–	–
VDD (V)	1.2	1.8	1.2	1.8	3.3
SNDR (dB)	72.85	56.7	68.8	70.1	60.2
SFDR (dB)	86.5	72.2	77.5	84.3	71.4
DNL/INL (LSB)	-0.19, +0.17 -0.28, +0.26	–	-0.79, +1.02 -2.28, +1.84	0.2 / 0.6 1.41 / 2.27	–
Power diss. (mW)	0.248	2.36	0.348	1.73	3.201
Temp.	-55°C – +125°C	–	–	up to +125°C	–
Area (mm2)	0.53	0.126	0.065	0.13	1.48
FoM (fJ/st.)	69	845	7.7	165.5	4600
Calibration	No	No	No	No	No

7. CONCLUSION AND FUTURE WORK

In this thesis, a reset-efficient DAC switching scheme is presented. Two SAR ADCs are designed in the 65nm UMC CMOS process node. The first ADC is sampled at 100kHz with $V_{DD} = 0.7V$, while the second ADC is sampled at 1MHz with V_{DD} set to 1.2V. The power consumption of the first and the second ADCs are 1.55µW and 248µW, respectively. Both ADCs demonstrate significant robustness to PVT variations. Post-layout simulations reveal the superiority of both ADCs in handling temperature variations ranging from -55°C to +125°C in all process corners. Each ADC withstands more than 10% of V_{DD} change. The linearity of both ADCs is confirmed through DNL and INL plots. These results establish the suitability of both ADCs for harsh environments and ultra-low power applications with a high yield. In the design of both ADCs, we have incorporated more than sufficient margins. Recognizing the comparator as the most power-hungry block, it is actually capable of comparing two input signals sampled at around ∼10MHz. The other blocks were designed in a similar manner. Limiting the design margin could reduce power dissipation. Below are some modifications and suggestions to enhance ADC performance efficiently:

1. Use a lower unit capacitor: C_u was chosen to be 13fF, which is relatively large. A smaller capacitor can be employed to significantly reduce the area and power consumption. However, the overall capacitance of the DAC should remain sufficiently large to suppress thermal noise. Smaller MIM-capacitors are not available in UMC CMOS technology. One could consider other technology nodes.
2. Explore a different architecture for the comparator: Various structures in the literature consume less power. Any reduction in the power dissipated by the comparator would have a significant impact on overall power consumption.
3. Optimize layout design: Typically, the layout of the digital part and the comparator is sandwiched between the two DACs, reducing the overall area. In this design, all blocks are arranged in series and the empty spaces were filled with decaps to minimize noise on the voltage lines. Any improvement in layout design would reduce the area.

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