DESIGN OF MAGNETIC SENSING MICROSYSTEM WITH HALL SENSORS

by

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ABSTRACT

DESIGN OF MAGNETIC SENSING MICROSYSTEM WITH HALL SENSORS

Magnetic sensors are transducers which convert magnetic field into electrical signals. A class of magnetic sensors is Hall Effect sensor where transportation of the electrons in the electrical device is affected by the presence of the external magnetic field to produce a voltage difference with a magnitude depending on the external magnetic field, Hall Voltage. Hall Effect sensors, formed by Hall element and signal-conditioning electronics integrated on the same integrated circuit fabricated in CMOS technology, include the advantages of small size, high speed, low cost, long life, and design flexibility. They are widely used in various industrial and automotive applications. This dissertation presents development of a compact cross-shaped Hall Effect sensor model and design of readout electronics for the magnetic sensing microsystem with Hall Effect sensor using UMC 130 nm CMOS technology. The presented technology allows sensing magnetic field with a low offset and low noise microsystem. The Hall Effect sensor is biased by a biasing circuit which implements dynamic offset cancellation method for cancelling sensor offsets due to fabrication imperfections and mechanical stress; and, Hall Voltage is amplified by an amplifier with a chopper technique realization for improving resolution of the microsystem and rejecting amplifier offset and low-frequency noise of the microsystem. The simulation results present a residual offset due to sensor offsets of 40 μV, corresponding to an input-inferred residual offset of 7.62 μT; and an input-inferred offset of 1.62 μV for a standard offset of 1 mV at amplifier input. Moreover, RMS noise voltage of 167 μV in the bandwidth of 1 Hz – 1 kHz at the microsystem output enables a microsystem resolution as low as 31.75 μT. Finally, the absolute sensitivity of the microsystem is 5.25 V/T.

ÖZET

HALL ALGILAYICILI MANYETİK ALAN ALGILAMA MİKROSİSTEMİ TASARIMI

Manyetik algılayıcılar manyetik alanı elektriksek işaretlere çeviren dönüştürücülerdir. Hall Etkisi algılayıcılar manyetik algılayıcıların bir sınıfıdır ve elektriksel aygıttaki elektron taşımacılığının harici manyetik alan varlığından etkilenmesi sonucu büyüklüğü harici manyetik alanın şiddetine bağlı Hall Gerilimi olarak isimlendirilen bir gerilim farkı oluştururlar. Hall Etkisi algılayıcılar aynı tümdevre üzerinde CMOS teknolojisi ile gerçekleştirilen Hall elemanından ve işaret iyileştirme elektroniğinden oluşur ve küçük boyutlu, yüksek hızlı, düşük maliyetli, uzun ömürlü ve esnek tasarımlı olmak gibi üstünlüklere sahiptir. Çeşitli endüstriyel ve otomotiv uygulamalarında Hall Etkisi algılayıcılar yaygın olarak kullanılırlar. Bu tez çalışmasında UMC 130 nm CMOS teknolojisi ile gerçekleştirilen yoğun çapraz-şekilli Hall Etkisi algılayıcı modeli gelişmesi ve manyetik alan algılama mikrosistemi okuma elektroniği tasarımı sunulmaktadır. Sunulan teknoloji manyetik alanın düşük ofsetli ve düşük gürültülü mikrosistem ile algılanmasını sağlamaktadır. Hall Etkisi algılayıcı, mikrofabrikasyon kusurlarından ve mekanik gerilmelerden kaynaklanan algılayıcı ofsetlerini gidermek amacıyla dinamik ofset giderimi yöntemi uygulayan bir kutuplama devresi ile kutuplanmaktadır. Hall Gerilimi, mikrosistem çözünürlüğünü iyileştirmek ve yükselteç ofseti ve mikrosistem düşük frekans gürültüsünü bastırmak amacıyla kıyım tekniğini uygulayan bir yükselteç ile yükseltilmektedir. Benzetim sonuçları, algılayıcı ofsetlerinden kaynaklanan 40 μV değerinde artık ofset ve 7.62 μT değerinde girdi-çıkarımlı artık ofset; ve yükselteç girişindeki 1 mV değerindeki ofsetten kaynaklanan 1.62 μV değerinde girdi-çıkarımlı ofset sunmaktadır. Mikrosistem çıkışındaki 1 Hz – 1 kHz bant genişliğine ait 167 μV etkin değerli gürültü gerilimi 31.75 μT değerinde mikrosistem çözünürlüğü sağlamaktadır. Son olarak, mikrosistem mutlak duyarlılığı 5.25 V/T olarak sunulmuştur.

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LIST OF SYMBOLS

B	Magnetic field
C	Capacitance
f	Frequency
G	Geometric correction factor
I	Current
k	Boltzman constant
L	Hall sensor length
n	Carrier concentration
$N_{A,sub}$	P-substrate doping concentration
$N_{D,nw}$	N-well doping concentration
n_i	Intrinsic carrier concentration
q	Electron charge
R	Resistance
R_H	Hall coefficient
r_H	Hall scattering factor
R_s	Sheet resistance
s	Hall sensor contact size
S_{Vn}	Voltage-noise spectral density
$S_{Vn\alpha}$	1/f voltage-noise spectral density
S_{VnT}	Thermal voltage-noise spectral density
S_I	Supply-current related sensitivity
S_V	Supply-voltage related sensitivity
t	Hall sensor thickness
T	Temperature
t_{nw}	N-well thickness
U_{pn}	Voltage across the pn junction
V	Voltage
V_D	Diffusion voltage of pn junction
V_H	Hall voltage

W	Hall sensor width
$w_{nw,sub}$	Depletion region thickness of pn junction
δR	Offset resistance
ϵ_{si}	Silicon absolute permittivity
μ_n	Electron mobility
σ_n	Semiconductor conductivity
θ_H	Hall angle

LIST OF ABBREVIATIONS

2D	Two Dimensional
3D	Three Dimensional
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
EDA	Electronic Design Automation
FEM	Finite Element Method
JFET	Junction Gate Field-Effect Transistor
NMOS	N-Channel Metal Oxide Semiconductor
PMOS	P-Channel Metal Oxide Semiconductor
RMS	Root-Mean-Square
SNR	Signal-to-Noise Ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
UMC	United Microelectronics Corporation
$\Delta\Sigma$	Delta-Sigma

1. INTRODUCTION

Magnetic sensors, being transducers which convert magnetic field into an electrical signal. Galvanomagnetic effects occur when a material carrying an electric current is exposed to a magnetic field. Lorentz defection and Hall Effect are two best known ones of these effects. While producing a current component perpendicular to the magnetic induction vector and the original current direction is called Lorentz defection, an electric field perpendicular to the magnetic induction vector and the original current direction is produced due to the Hall Effect. Semiconductor magnetic sensors exploit galvanomagnetic effects due to the Lorentz force on charge carriers in semiconductors as high mobility and low carrier concentration favor the galvanomagnetic effects. [1]

A class of magnetic sensors is Hall Effect sensor where the transportation of the electrons in the electrical device is affected by the presence of the external magnetic field. As the electrons are deflected in the electrical material, they cause a charge build up and a measurable voltage difference across the material. This voltage difference, which is a function of current density, magnetic field, charge density, and carrier mobility of the conductor, is called Hall Voltage. Since the output Hall voltage is typically on the order of microvolt to millivolt, due to being caused by galvanomagnetic effects, the conductive material needs to be paired with additional electronics to achieve useful voltage levels. Hall element and the signal-conditioning electronics, integrated on the same integrated circuit, form the basic Hall Effect sensor. [2]

The Hall plate is constructed from a thin sheet of conductive material and provided with four ohmic contacts. The Hall voltage appears between the output connections perpendicular to the direction of current flow,

$$V_H = \frac{R_H G I B}{t} \tag{1.1}$$

where R_H denotes the Hall coefficient, G denotes the geometric correction factor, B denotes the magnetic field, and t denotes the plate thickness. Hall coefficient, which is

favored by the low carrier concentration and high mobility, depends on the temperature and doping of the semiconductor material,

$$R_H = -\frac{\mu_n}{\sigma_n} = -\frac{r_H}{qn} \tag{1.2}$$

where r_H denotes the Hall scattering factor and n denotes the carrier concentration. Shape effects of the plate are described by the geometric correction factor, which depends on the length L and width W of the Hall plate, the contact size s, the position of the sensor contacts, and the Hall angle θ_H. It reflects the short-circuiting effects between the input and output contacts, having a value approaching unity in the limit of infinitely long plate. Diamond-shaped (with contacts at the four corners) and cross-shaped Hall plates (with contacts at the end of each cross) are more desirable in terms of reducing the short-circuiting effects. [1, 2]

Different types of sensitivities, which is the most significant factor for a Hall sensor, are defined based on the electrical supply signal type. The supply-current related sensitivity, Hall voltage per unit current and magnetic induction, is given in Equation 1.3.

$$S_I = \frac{V_H}{IB} = \frac{GR_H}{t} = -\frac{Gr_H}{qnt} \tag{1.3}$$

The transport of electrons is affected by the thickness of the material. The thicker the material, the easier it is for the electrons to transport in it. As a result, high supply-current related sensitivity is achieved by small carrier concentration and small plate thickness. The supply-voltage related sensitivity, Hall voltage per unit voltage and magnetic induction, is,

$$S_V = \frac{V_H}{VB} = \mu_n G \frac{W}{L} \tag{1.4}$$

where W and L denote the width and length of the device, respectively. Since the supply-voltage related sensitivity depends on the drift mobility, the material from which the Hall element is fabricated affects the sensitivity of the element. Higher relative

sensitivity is achieved for materials which have high carrier mobility. [1]

Noise, offset, temperature coefficient, and nonlinearity are the important factors that cause the deviations from the ideal Hall plate and limit the sensor performance and the precision of the magnetic field measurements. Since the measurement resolution is determined by the signal-to-noise ratio (SNR), noise severely limits the performance of the sensor. The noise voltage at the output of the Hall sensor can be caused by thermal noise (Johnson-Nyquist noise), 1/f noise, and generation-recombination noise (fluctuation of number of carriers) which is often negligible compared to 1/f noise. While 1/f noise becomes the dominant source of noise at low frequencies, thermal noise is the main noise source at high frequencies. The voltage-noise spectral density is,

$$S_{Vn}(f) = S_{Vn\alpha}(f) + S_{VnT} \tag{1.5}$$

where $S_{Vn\alpha}(f)$ denotes the voltage-noise spectral density due to 1/f noise and S_{VnT} denotes the thermal voltage-noise spectral density. The SNR in a narrow bandwidth Δf around f is given in Equation 1.6.

$$SNR = V_H(I, B) \times (S_{Vn}(f)\Delta f)^{-0.5} \tag{1.6}$$

Offset voltage, which strongly limits the resolution of the sensor, is a quasi-static output voltage of a Hall sensor in the absence of magnetic induction. The main cause of the offset voltage is the imperfections in the fabrication process like misalignments, nonuniformity of the material resistivity and material thickness. Piezoresistance effect by the mechanical stress and magnetoresistance effect activated by the magnetic induction can also produce offset at the output of the Hall sensor. Temperature coefficient determines the variations of the sensor sensitivity with temperature changes. The current related sensitivity is affected only by the temperature dependence of the scattering factor, r_H. However, the strong temperature dependence of the drift mobility dominates the temperature coefficient of the voltage related sensitivity. Although

Hall Effect is highly linear with the field strength with no saturation effects ranging to extremely high fields, nonlinearity appears as a source of deviation from the ideal case due to material and geometric causes. The material causes are reflected through the Hall coefficient while the geometry factor includes the geometrical ones. There is usually a quadratic relation between the nonlinearity and the magnetic induction such that nonlinearity is proportional to the B^2. [1–4]

Hall Effect can be implemented in standard complementary metal oxide semiconductor (CMOS) technology. Hall Effect sensors, formed by the Hall element and the signal-conditioning electronics integrated on the same integrated circuit fabricated in CMOS technology, include the advantages of small size, high speed, broad operation temperature range, low cost, long life, and design flexibility. [1, 2] Hall devices prove their versatility and general significance by being employed in different industrial and automotive applications like magnetometry, magnetic microbeads detection, magnetic resonance detection, current detection, contactless linear or angular position, displacement, or velocity detection. [1]

Integrating Hall sensors with permanent magnet microsystems will bring into existence a new set of micro devices for a variety of applications. To detect the magnetic field, hence the position of micro-scale permanent magnets, either a multi-axis force sensor with minimum 2-axis magnetic field sensing capability or a multi-point sensing device with an array of Hall sensors can be used.

The work presented in this thesis includes development of a compact cross-shaped Hall Effect sensor model and design of readout electronics for the magnetic sensing microsystem with Hall Effect sensor using UMC 130 nm CMOS technology. The presented technology allows sensing a magnetic field with a low noise and low offset microsystem. The electrical block diagram of the magnetic sensing microsystem, presenting the readout electronics, is shown in Figure 1.1. The Hall Effect sensor is biased by a biasing circuit which implements dynamic offset cancellation by periodic permutations of the input and output contacts. A chopper modulation stage is employed in between the sensor output and the amplifier to change the polarity of the signal at the sensor

output periodically. The signal is received by the amplifier which provides the amplification factor to increase the sensitivity of the system. A chopper demodulation stage is coupled to the amplifier to achieve low noise and offset figures by interchanging the polarity of the differential amplifier outputs. The whole readout electronics is designed to improve the signal-to-noise ratio of the system and reduce the offset caused by the imperfections and mechanical stress.

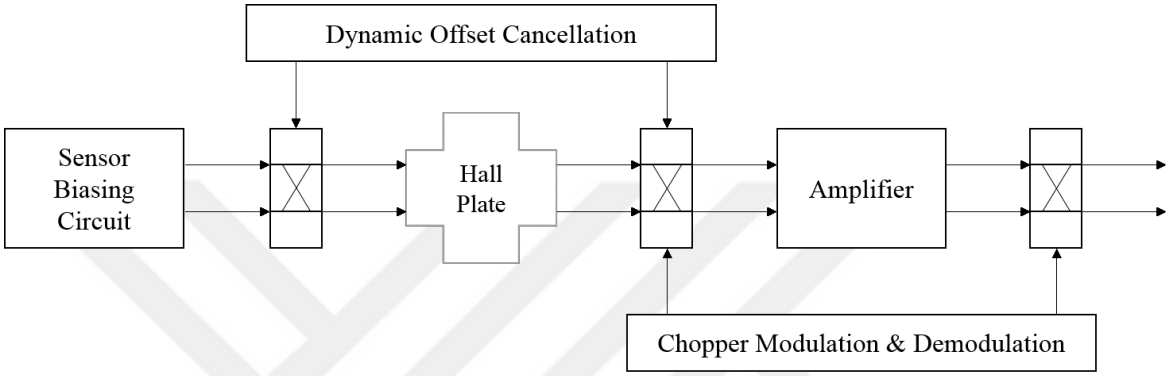

Figure 1.1. Electrical block diagram of the magnetic sensing microsystem.

2. COMPACT CROSS-SHAPED HALL SENSOR MODEL

Hall sensors are a group of magnetic sensors which can be implemented in standard complementary metal oxide semiconductor technology. Figure 2.1 presents a horizontal Hall plate which is fabricated as part of an n-type layer grown on a p-type substrate. It is generally used in the Hall sensors as the active region since n-type material has higher carrier mobility, favoring the voltage-related sensitivity. The plate is bounded by a lateral boundary of deep p-diffusion which serves as the isolation layer by providing a reverse-biased p-n junction. The contacts of the sensors are made by n+-diffusions, which correspond to the usual source and drain regions, to be used as the intermediate layer providing the ohmic contact between the semiconductor substrate and the metal layer. A shallow p-layer covers the surface of the whole Hall plate to shield the carriers from the interface, preventing the carrier scattering effect and reducing the flicker noise. [1]

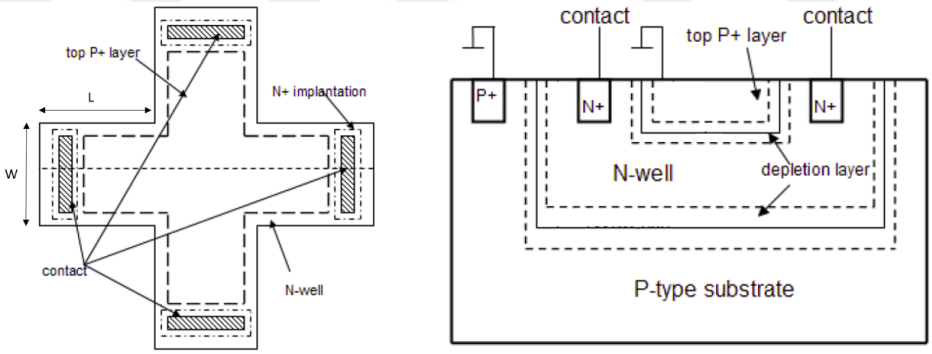

Figure 2.1. Structure of a Hall sensor fabricated using CMOS technology.

Since the cross-shaped Hall sensor is stated as the optimum plate to achieve the lowest noise, residual offset, and the best sensitivity; and the symmetrical design is stated to have the ability to provide immunity to imperfections in the fabrication process [3], it is preferred in the magnetic sensing microsystem.

As the signal-conditioning electronics is integrated on the same CMOS circuit with the Hall element, achieving high simulation accuracy in electronic design automa-

tion (EDA) tools is crucial for the proper design of signal-conditioning electronics. However, the EDA tool design-kits do not include the sensing Hall element, creating the necessity to develop a precise simulation model for the cross-shaped Hall sensor. The simulation model should describe the behavior of the Hall sensor accurately and be compact not to lead to long computation durations.

2.1. State of Art

A number of studies have presented simulation models for Hall sensors taking into account different effects such as nonlinearity, piezoresistance effect, temperature drift effect, and geometrical effect, frequency response, and noise behavior.

Some of the models are too complex to be used in SPICE-like EDA tools since they cause long simulation times. Dimitropoulos et al. presented a completely scalable lumped-circuit model which is composed of elementary rectangular Hall devices [5]. Each elementary cell includes two JFETs and two current controlled current sources, providing the ability to analyze temperature effects, dynamic response, and noise behavior through the included JFET model; and nonlinear conductivity, due to field-dependent mobility and sensor thickness modulation, and geometrical effects through the cell based structure of the model. Although the model provides high accuracy, it requires an accurate JFET device model which cannot be readily available in standard CMOS technology and causes long simulation times. 2D and 3D physical models, which were simulated in a FEM-like simulator, were proposed in [6]. The model is composed of eight current controlled current sources and eight nonlinear resistors, whose values are functions of the potential difference on their ends as the proportionality constants are defined by FEM simulations, to incorporate nonlinearity. Jankovic et al. proposed a symmetrical four-cell lumped element model whose electrical characteristics were simulated in 3D using a FEM-like simulator to analyze nonlinearity, temperature effect, and magneto-resistance effect [7]. They are modeled through a resistance equation which depends on the voltage across the resistor, temperature, and the magnetic field as their dependency parameters are extracted from the fitting with the 3D simulations. Four diodes and four connection resistors are also included in the model, together with

eight nonlinear resistors and eight current controlled current sources, for modeling the time response. Due to their long computation times to be used in SPICE-like circuit simulators, FEM models in [6, 7] are not usually preferred.

Schweda and Riedling proposed a behavioral model to include the nonlinearity caused by voltage dependency of the effective sensor thickness, transient effects caused by parasitics, and temperature effects caused mainly by the temperature dependency of charge carrier concentration and mobility but not geometrical and piezoresistance effects [8]. The model, which can be readily used in SPICE-like EDA tools, consists of a four-resistor Wheatstone bridge network with nonlinear and temperature dependent resistances, four voltage sources, and a diode and capacitance pair at each contact; however, the necessity of expanding the network in size and arrangement based on the experimental results is stated.

Xu and Zhao presented a simulation model architecture which takes into account nonlinearity, geometry, temperature effect and packaging stress in [9]. The model includes four resistors in Wheatstone bridge implementation to form the active region, two current controlled voltage sources in series with each resistor, eight nonlinear lumped capacitances for modeling the depletion capacitance between the n-well and p-substrate and the one between n-well and top p+ layer, and four resistor and capacitor pairs at the contacts to represent contact resistance and parasitic capacitances, respectively. However, the work does not present any equations for the electrical circuit elements based on physical and technology parameters or simulation fitting.

Xu and Pan developed a simulation model for Hall plates, shown in Figure 2.2, to cover voltage dependent nonlinear effects, geometrical effects, temperature effects, and packaging stress [10]. The model is composed of a network with eight nonlinear resistances for the body resistance of the Hall plate, four current-controlled voltage sources which are controlled by the current through the nearest contact to model the Hall voltage, and four parasitic capacitances to simulate the transient behavior. Nonlinearity caused by the variation of the effective device thickness with the voltage and temperature effect based on the temperature coefficient of sheet resistance, carrier

concentration of the n-well, and Hall factor are included in the model through the equations of resistance and sensitivity, whereas geometrical effect and piezo-Hall effect are modeled in the equation for sensitivity. However, the piezo-Hall and piezoresistive effects are pointed out to be too complex issues to be modeled accurately by a small number of physical and technological parameters. Lateral diffusion effect and junction field effect due to the lateral diffusion were also added to the model in the further work in 2012, [11]. However, the lateral diffusion effect is stated to be overestimated in small Hall plates based on the experimental results.

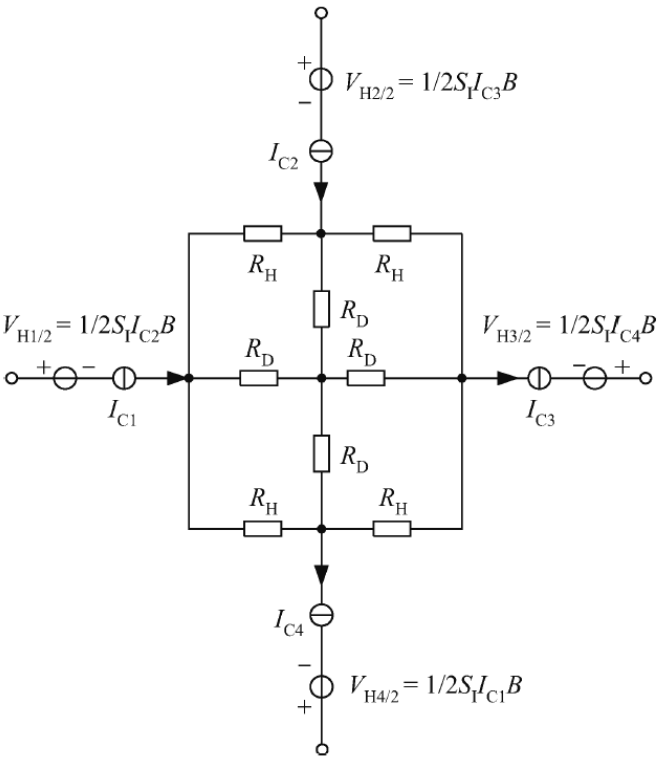

Figure 2.2. Simulation model for Hall plates, presented in [10] and [11].

A compact model of a cross-shaped Hall plate, which is composed of six resistors and four current controlled voltage sources, was presented in [12] by Madec et al. However, the model fails in taking into account effects such as temperature effect and mechanical stress effect, other than the nonlinearity effect by channel thickness modulation. The simulation model was improved with the inclusion of additional resistances to represent the offsets caused by the fabrication dispersions and mechanical stress [13]. The effect of channel thickness modulation is also detailed in the new model

as the voltage dependency is incorporated into the equations of the body resistance and sensitivity. The presented model in Figure 2.3 includes six nonlinear resistors connected between each pair of contacts, correction resistors in series with the nonlinear resistors, four current controlled voltage sources, and contact serial resistances. Madec et al. included thermal effects to the model [14]. It is reflected in the model through the temperature dependency of physical and technological parameters including electron mobility, carrier density, and scattering factor based on either the physical origins or fitting with the simulation results. However, the model lacks the coverage of dynamic behavior of the Hall device, which is important for the analysis of the frequency response of the magnetic sensing microsystem.

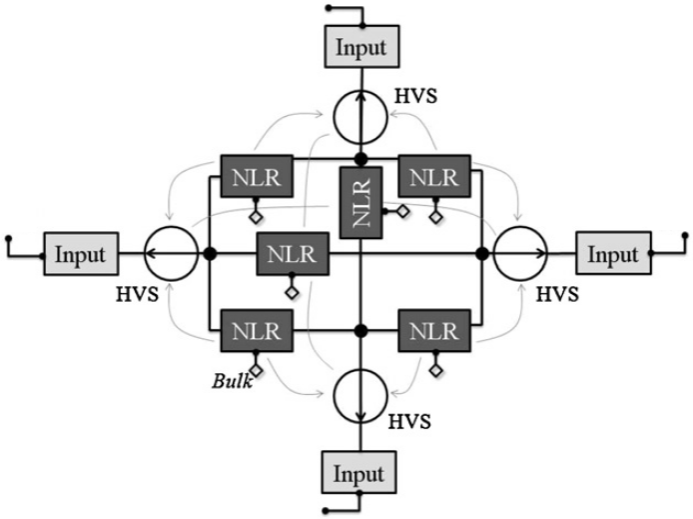

Figure 2.3. Simulation model for Hall plates, presented in [13] and [14].

2.2. Sensor Model Architecture

A simulation model for the Hall element in the magnetic sensing microsystem needs to be designed accurately to model nonlinearity, temperature drift effect, offsets due to fabrication dispersion and mechanical stress, geometrical effect, and frequency response, together with the Hall Effect. The model for the Hall element, whose accuracy is crucial for the proper design of the signal-conditioning electronics, is also required to be compact not to cause long simulation times.

2.2.1. Using Eight Resistors

Figure 2.4 presents the cross-shaped Hall sensor model, designed to fulfill these requirements. The model includes 8 resistors to represent the resistive behavior of the sensor body, 4 current controlled voltage sources to model the Hall voltage, and 4 parasitic capacitances to account for the sensor frequency response.

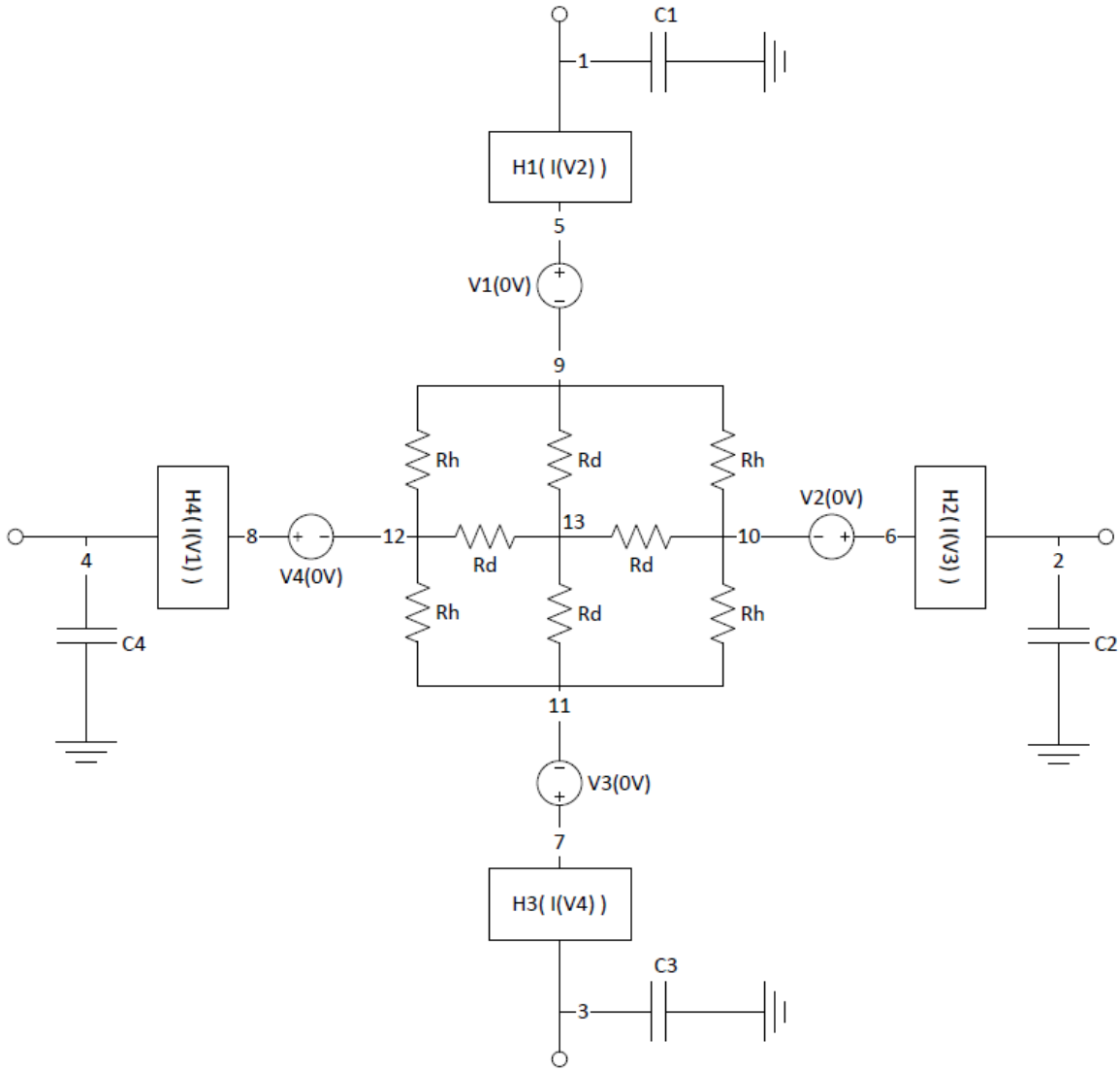

Figure 2.4. Compact cross-shaped Hall sensor model with eight resistors.

Conventional 4-resistor Wheatstone bridge implementation for resistive behavior of the Hall sensor fails in fulfilling the accuracy requirement since the current, flowing between the two adjacent contacts, crosses through the center region of the device,

which is ignored in a Wheatstone bridge configuration. Moreover, the offset caused by the piezoresistive effect, which generally results in compression along one of the two directions, cannot be accurately modeled using this configuration.

Hall plates with a symmetry of $\pi/2$, which are widely used for their immunity to fabrication dispersions, such as cross-shaped or square Hall plate can be represented by two types of resistances to model their electrical behavior. The resistances between two adjacent contacts and between two diagonal contacts are designated as R_H and R_D, respectively. Furthermore, they are defined as functions of sheet resistance of the n-well based on the Van der Pauw method [15] as the active region of the Hall element is fabricated in the n-well diffusion region. According to the Van der Pauw method, the potential difference between C and D per current flowing from A to B, $R_{AB,CD}$, is defined based on n-well sheet resistance in Equation 2.1.

$$R_{AB,CD} = \frac{ln(2)}{\pi} R_s \tag{2.1}$$

And, it is also defined in terms of R_H and R_D as,

$$R_{AB,CD} = \frac{R_H}{4} \times \frac{2R_D - R_H}{2R_D + R_H} \tag{2.2}$$

for the circuit architecture in Figure 2.4. Combining Equation 2.1 and 2.2, the resistances between the adjacent contacts, R_H, and between the diagonal contacts, R_D, are defined by,

$$R_H = R_s \times \frac{2}{\pi} \left(\left(2\frac{L}{W} + \frac{2}{3} \right) \pi - 2ln(2) \right) \tag{2.3}$$

$$R_D = R_s \times \frac{\left(\frac{2L}{W} + \frac{2}{3}\right) \times \left(\left(\frac{2L}{W} + \frac{2}{3}\right) \pi - 2ln(2) \right)}{\left(\frac{2L}{W} + \frac{2}{3}\right) \pi - 4ln(2)} \tag{2.4}$$

where R_s denotes the sheet resistance of the n-well, L and W denote the length and width of the sensor finger, respectively, as they are shown in Figure 2.1. The equations

depend purely on the dimensions of the sensor while $(2L/W + 2/3)$ is the effective number of squares of the n-well sheet resistance for the cross-shaped Hall sensor. The center square count is stated to be approximately reduced to 2/3 due to the parallel placement of two sensor fingers in [10].

It should be noted that the N+ contact resistances are ignored in the model since their resistance is very small in comparison to the sheet resistance of the n-well.

The Hall voltage is modeled by current controlled voltage sources at the contacts of the Hall sensor as they are controlled by the current flowing though the nearest contact. The Hall voltage in one of the measurement contacts is given by,

$$V_{H/2} = \frac{1}{2} S_I I(n1, n2) B \tag{2.5}$$

where $I(n1, n2)$ denotes the current flowing from the node $n1$ to node $n2$ as it is sensed by the current of the intentionally added zero-voltage voltage source. S_I is defined based on several technological and geometrical parameters in Equation 2.6 to form the multiplication factor of the current controlled voltage source, together with the parametrically defined magnetic field.

$$S_I = \frac{G r_H}{q N_{D,nw} \left(t_{nw} - w_{nw,sub}\right)} \tag{2.6}$$

$N_{D,nw}$ is the doping concentration of the n-well as its value is read from the foundry technological files and the effective thickness of the conduction channel is defined by the depth of the n-well, t_{nw}, and the thickness of the depletion region, $w_{nw,sub}$, which is formed between the n-well and the p-substrate due to the reverse-biased pn junction.

$$t_{nw} = \frac{1}{q \mu_n N_{D,nw} R_s} \tag{2.7}$$

$$w_{nw,sub} = \sqrt{\frac{2\epsilon_{si}}{q} \times \frac{N_{A,sub}}{(N_{A,sub} + N_{D,nw}) N_{D,nw}}} \times \sqrt{V_D} \tag{2.8}$$

The values of the n-well sheet resistance, the doping concentrations of n-well and p-substrate, and the diffusion voltage of the reverse-biased pn junction, denoted by V_D, are found in the foundry technological files.

2.2.2. Using Six Resistors

Figure 2.5 presents the second cross-shaped Hall sensor model, which includes 6 resistors to represent the resistive behavior of the sensor body, 12 current controlled voltage sources to model the Hall voltage as the Hall voltage at each contact depends on three different current flows, and 4 parasitic capacitances to account for the sensor transient behavior.

The model incorporates 6 resistors, each of them modeling the effective resistance between one pair of sensor contacts. In the ideal case, where there is not any fabrication imperfections or mechanical stress, Hall plate achieves a perfect symmetry of $\pi/2$ to be represented by two different resistances, R_A and R_O, as shown in Figure 2.5. The equivalent resistance between the adjacent contacts is calculated based on R_A and R_O as,

$$R_{12} = \frac{R_A R_O}{R_A + R_O} \tag{2.9}$$

and the one between the opposite contacts is given in Equation 2.10.

$$R_{13} = \frac{R_A(R_A + 3R_O)}{4(R_A + R_O)} \tag{2.10}$$

Since the conduction channel occurs in the n-well diffusion region, the resistance of a rectangular n-well resistor whose length and width are $2L+W$ and W, respectively, is defined as the reference resistance for calculation of R_A and R_O,

$$R_{ref} = \frac{1}{q\mu_n N_{D,nw} t_{nw}} \times \frac{2L + W}{W} \tag{2.11}$$

where q denotes the electron charge, μ_n and $N_{D,nw}$ denote the electron mobility and doping concentration in the n-well, and t_{nw} denotes the thickness of the n-well. It should also be noted that the n+ contact resistances are ignored in the model since they are very small in comparison to the sheet resistance of the n-well. The resistances of R_A and R_O are determined based on the geometry of the Hall device by α and β, as presented in Equation 2.12 and 2.13.

$$R_A = 2\alpha\,(2\beta - 1) \times R_{ref} \tag{2.12}$$

$$R_O = 2\alpha \frac{(2\beta - 1)}{(4\beta - 3)} \times R_{ref} \tag{2.13}$$

The coefficient, α, models the spread of current lines in the center of the device, the region where lateral arms cross, whereas β represents the short-circuit effect in the conduction channels. Their values depend purely on the dimensions of the Hall device,

$$\alpha = 1 - 0.0976 \times e^{-0.6631\frac{L}{W}} \tag{2.14}$$

$$\beta = 0.96 \times e^{0.003\frac{L}{W}} - 0.18 \times e^{-4.333\frac{L}{W}} \tag{2.15}$$

as the expressions are established from FEM simulations in [14].

Hall Effect is represented in the model by using current controlled voltage sources. The Hall voltage at each contact is controlled by the current flowing through three different branches,

$$\begin{aligned} V_{H1} &= \frac{1}{2} S_I\,(I_{2,1} + I_{1,4} + I_{2,4})\,B \\ V_{H2} &= \frac{1}{2} S_I\,(I_{3,2} + I_{2,1} + I_{3,1})\,B \\ V_{H3} &= \frac{1}{2} S_I\,(I_{4,3} + I_{3,2} + I_{2,4})\,B \\ V_{H4} &= \frac{1}{2} S_I\,(I_{1,4} + I_{4,3} + I_{1,3})\,B \end{aligned} \tag{2.16}$$

as numbering of the contacts is based on Figure 2.5, and gain of the current controlled voltage sources is set by magnetic field and current related sensitivity given by Equation 2.6.

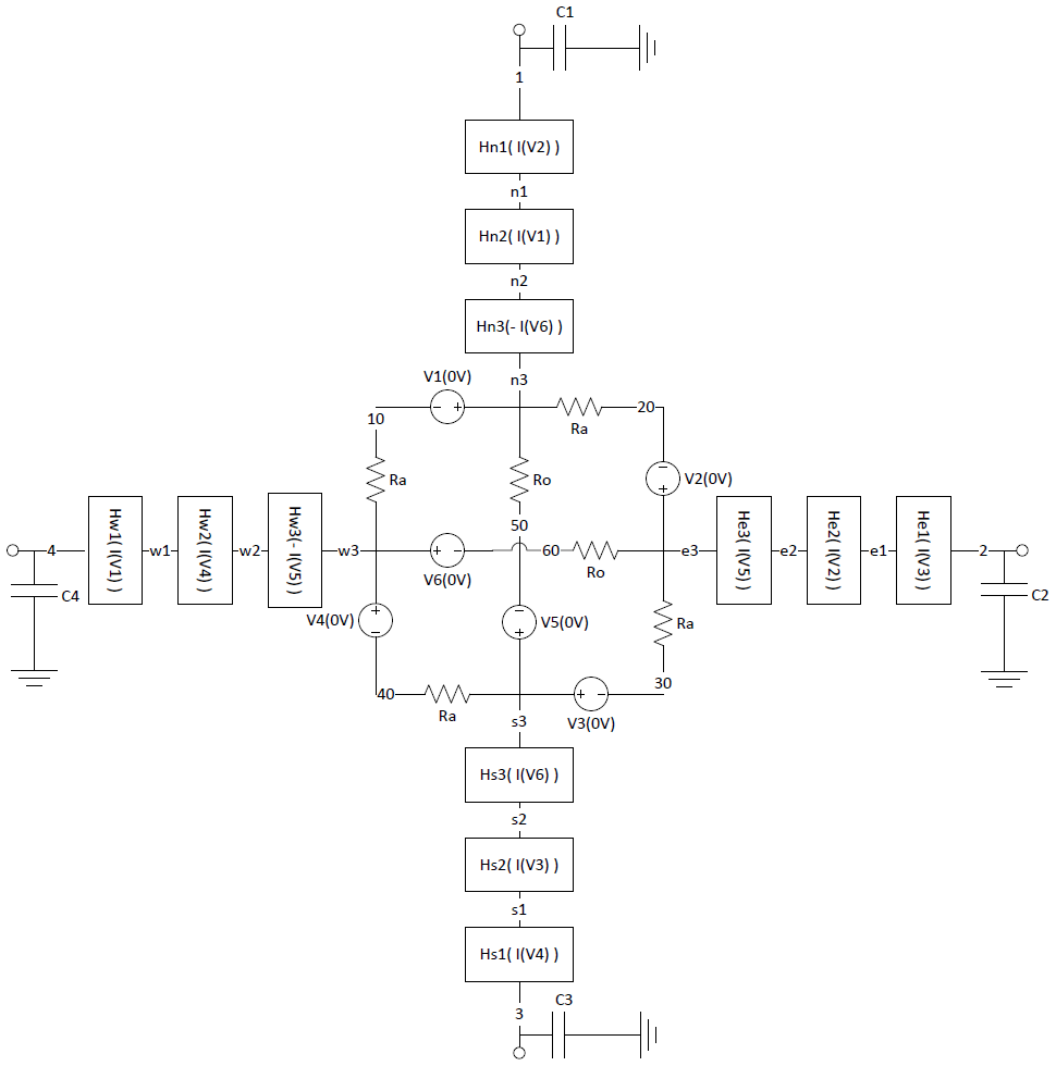

Figure 2.5. Compact cross-shaped Hall sensor model with six resistors.

2.3. Nonlinearity

The thickness of the conduction channel can be considered to be constant along the biasing direction if the voltage bias is small. However, the voltages, which will be used to bias the Hall element in the proposed microsystem, alter the voltage difference of the reversed biased pn junction between the n-well and p-substrate significantly. As a result, the thickness of depletion region around the junction changes with the voltage

difference according to Equation 2.17.

$$w_{nw,sub} = \sqrt{\frac{2\epsilon_{si}}{q} \times \frac{N_{A,sub}}{(N_{A,sub} + N_{D,nw})N_{D,nw}}} \times \sqrt{V_D - U_{pn}} \tag{2.17}$$

As the potential of the n-well changes along the biasing direction, the thickness of the conduction channel is modulated by the voltage bias through the change in the depletion region thickness, producing the strong nonlinear voltage dependency. The effect reflects in the sheet resistance and the current related sensitivity.

To include the effect of nonlinearity in the current related sensitivity, Equation 2.17 is substituted into Equation 2.6 replacing $w_{nw,sub}$. The new equation is extended by Taylor expansion up to the second order as a function of voltage difference to be able to include nonlinearity in the SPICE model.

$$S_I(U_{pn}) = S_{I0} + S_{I1} \times U_{pn} + S_{I2} \times U_{pn}^2 \tag{2.18}$$

$$S_{I0} = \frac{G \times r_H}{q \times N_{D,nw} \times \left(t_{nw} - \sqrt{k_1 \times V_D}\right)} \tag{2.19}$$

$$S_{I1} = \frac{1}{2} \times \frac{G \times r_H \times \sqrt{k_1}}{q \times N_{D,nw} \times \sqrt{V_D} \times \left(t_{nw} - \sqrt{k_1 \times V_D}\right)^2} \tag{2.20}$$

$$S_{I2} = \frac{1}{8} \times \frac{G \times r_H \times \sqrt{k_1} \times \left(3\sqrt{k_1 \times V_D} - t_{nw}\right)}{q \times N_{D,nw} \times V_D\sqrt{V_D} \times \left(t_{nw} - \sqrt{k_1 \times V_D}\right)^3} \tag{2.21}$$

where k_1 is defined in Equation 2.22.

$$k_1 = \frac{2\epsilon_{si}}{q} \times \frac{N_{A,sub}}{(N_{A,sub} + N_{D,nw})N_{D,nw}} \tag{2.22}$$

The multiplication factor of the current controlled voltage sources in Figure 2.4 and 2.5 is modified to be dependent on the voltage at the contact where they are placed, as the dependency factors are set by Equation 2.19 – 2.21.

The voltage dependence of the effective sheet resistance is represented by the inclusion of Equation 2.17 to Equation 2.23.

$$R_s = \frac{1}{q\mu_n N_{D,nw}\left(t_{nw} - w_{nw,sub}\right)} \tag{2.23}$$

For modeling of voltage dependence of the sheet resistance, Taylor expansion up to the second order is applied to achieve a sheet resistance definition as a function of voltage.

$$R_s(U_{pn}) = R_{s0} + R_{s1} \times U_{pn} + R_{s2} \times U_{pn}^2 \tag{2.24}$$

$$R_{s0} = \frac{1}{q \times \mu_n \times N_{D,nw} \times \left(t_{nw} - \sqrt{k_1 \times V_D}\right)} \tag{2.25}$$

$$R_{s1} = \frac{1}{2} \times \frac{\sqrt{k_1}}{q \times \mu_n \times N_{D,nw} \times \sqrt{V_D} \times \left(t_{nw} - \sqrt{k_1 \times V_D}\right)^2} \tag{2.26}$$

$$R_{s2} = \frac{1}{8} \times \frac{\sqrt{k_1} \times \left(3\sqrt{k_1 \times V_D} - t_{nw}\right)}{q \times \mu_n \times N_{D,nw} \times V_D\sqrt{V_D} \times \left(t_{nw} - \sqrt{k_1 \times V_D}\right)^3} \tag{2.27}$$

To be able to incorporate the nonlinear effect into the resistors of Figure 2.4 and 2.5, they are replaced with nonlinear resistors in Figure 2.6 whose control voltages are set to the voltage difference between the sensor contacts where the resistors are placed in between. The voltage controlled resistor is implemented by a voltage controlled current source which produces a current inversely and nonlinearly proportional to the voltage difference between the control nodes. The current at the output of the controlled source

is,

$$\frac{V(n_1, n_2)}{R_{s0} + R_{s1} \times V(nc_1, nc_2) + R_{s2} \times V(nc_1, nc_2)^2} \tag{2.28}$$

where R_{s0}, R_{s1}, and R_{s2} are defined parametrically. Therefore, the sub-circuit functions as a resistor whose resistance is controlled nonlinearly by the voltage difference between the control nodes.

Since the thickness of the depletion region between the p+ top layer and the n-well is smaller compared to the thickness of the depletion region between the n-well and p-substrate due to the high doping concentration of the p+ top layer, thickness variation of the former is not included in the model.

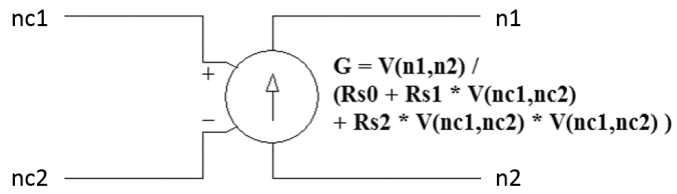

Figure 2.6. Voltage controlled resistor.

2.4. Temperature Drift Effect

Temperature drift has serious effect on the effective n-well resistance, magnetic field sensitivity, and the offset whereas it is caused mainly by the temperature dependency of electron mobility, carrier density, diffusion potential, and scattering factor, as well as packaging stress.

Instead of defining empirical temperature relations for the sheet resistance and sensitivity based on the results of experiments, the equations which represent the temperature dependency of the sheet resistance and sensitivity parameters are incorporated in the model since the parameters of the semiconductors have well defined temperature dependencies. Electron mobility, doping concentration, Hall scattering factor,

and diffusion potential are the temperature dependent parameters which determine the value of the sheet resistance and sensitivity whereas geometrical correction factor is a temperature independent parameter.

The mobility of carriers decreases with the increasing temperature since the vibrations of the crystal structure increased, reducing the mobility of the carriers. In the temperature range of interest, the temperature dependency of the mobility can be modeled by Equation 2.29.

$$\mu_n(T) = \mu_n(300K) \times \left(\frac{T}{300K}\right)^{-1.5} \tag{2.29}$$

Change of diffusion potential with temperature affects the sheet resistance and sensitivity through the thickness variations of the depletion region due to the reverse-biased pn junction. The well-known law for the diffusion potential [16] is incorporated to the model,

$$V_D(T) = \frac{k \times T}{q} \times ln\left(\frac{N_{D,nw} \times N_{A,sub}}{n_i^2}\right) \tag{2.30}$$

where k denotes the Boltzmann constant. The change of diffusion potential by temperature also affects the frequency response of the device by the dependency of the parasitic capacitance on the diffusion potential. Intrinsic carrier concentration, which is included in Equation 2.30, depends significantly on the temperature, as its mainly exponential dependence is also added to the model through Equation 2.31.

$$n_i = 7.3 \times 10^{21} \times T^{1.5} \times e^{\frac{-1.12}{2 \times 8.62 \times 10^{-5} \times T}} \tag{2.31}$$

Carrier density is also expected to change with temperature as the number of charge carriers in the conduction band increases with increasing temperature. However, the exact dependency of the carrier density on temperature is divided into three different regions: At low temperatures, there is not enough energy in the conduction

band to ionize all of the impurity atoms, resulting in an effective carrier density lower than the doping concentration, which is called freeze-out region. All of the impurity atoms are ionized with the increasing temperature, resulting in a constant carrier concentration equal to the doping concentration, which makes the region called as saturation region. At very high temperatures, the high energy level starts to ionize all of the semiconductor atoms, where the transition to intrinsic behavior is observed. For the n-well doping concentration used in this thesis and the temperature range of interest, the semiconductor can be considered in the saturation region of operation where the carrier density is equal to the doping concentration of the n-well based on [17] as the freeze-out region is noted to end around 250 K and the intrinsic behavior starts after 500 K.

Finally, temperature dependency of the Hall scattering factor is empirically included [18] and the value of r_{H0} is modified to fit with the results of the simulations as in Equation 2.32.

$$r_H = r_{H0} \times \left(\frac{T}{300K}\right)^{0.13} \tag{2.32}$$

The temperature effect on the device offset is caused mainly by the change of package stress with the temperature. Since the Hall element to be used in the magnetic sensing microsystem is not packaged, temperature drift effects due to the different temperature coefficients of the packaging materials and the silicon are ignored in this thesis.

2.5. Offset

Hall devices suffer from imperfections in the fabrication process like misalignments, nonuniform doping gradients, and nonuniformity of material thickness, and mechanical stress. Fabrication imperfections and mechanical stress cause an offset voltage at the output terminals of the Hall device under the zero magnetic field whereas the voltages of both terminals are the same in the ideal case, resulting in zero device offset.

It is important to cover all sources of offset in the model for the proper design of the offset cancellation circuit. Four different types of small resistors are added to the model to include the effect of offset caused by imperfection and mechanical stress:

- $\delta R1$ models the effect of shear stress on the Hall device by introducing a variation of the resistance along 1 – 4 and 2 – 3, and an opposite variation of resistance along 1 – 2 and 3 – 4. It can also be used to model the offset due to the misalignment of the contact pairs 1 – 3 and 2 – 4.
- $\delta R2$ includes the effects of fabrication imperfections along 1 – 3 like nonuniform doping gradient or material thickness along the direction and difference between the cross finger lengths. As the result of these types of imperfections, the resistance between terminal 1 and the center of the plate and the one between the center of the plate and terminal 3 become different.
- $\delta R3$ represents the same types of imperfections, which are covered by $\delta R2$, along the 2 – 4 direction. The imperfections cause a difference between the resistance between terminal 2 and the plate center and the one between the place center and terminal 4.
- $\delta R4$ covers the effect of the compression or expansion of the Hall plate along 1 – 3 or 2 – 4 directions with opposite variations of the mismatch resistance along 1 – 3 and 2 – 4.

After the small resistances are added to the model, the effective resistances between the sensor terminals become,

$$\begin{aligned} R_{1,2} &= R_A - \delta R1 + \delta R2 - \delta R3 \\ R_{2,3} &= R_A + \delta R1 - \delta R2 - \delta R3 \\ R_{3,4} &= R_A - \delta R1 - \delta R2 + \delta R3 \\ R_{4,1} &= R_A + \delta R1 + \delta R2 + \delta R3 \\ R_{1,13} &= R_O + \delta R4 \\ R_{2,13} &= R_O - \delta R4 \end{aligned} \tag{2.33}$$

in the sensor model architecture which includes six resistors, and,

$$\begin{aligned} R_{1,2} &= R_H - \delta R1 + \delta R2 - \delta R3 \\ R_{2,3} &= R_H + \delta R1 - \delta R2 - \delta R3 \\ R_{3,4} &= R_H - \delta R1 - \delta R2 + \delta R3 \\ R_{4,1} &= R_H + \delta R1 + \delta R2 + \delta R3 \\ R_{1,13} &= R_D + 0.5 \times \delta R4 \\ R_{2,13} &= R_D - 0.5 \times \delta R4 \\ R_{3,13} &= R_D + 0.5 \times \delta R4 \\ R_{4,13} &= R_D - 0.5 \times \delta R4 \end{aligned} \tag{2.34}$$

in the sensor model with eight resistors in the resistive bridge. Figure 2.7 and Figure 2.8 present the updated sensor model architectures with eight and six resistors, respectively.

The effects of $\delta R2$ and $\delta R3$ are to add a zero-field offset voltage to the sensor output when the sensor is biased with a voltage supply along 1 – 3 and 2 – 4 directions, respectively. However, the mismatch resistance $\delta R1$ shifts the sensor response significantly along the magnetic field axis and offset voltages with different polarities are generated at the output terminals of the Hall device under zero magnetic field. $\delta R4$ does not generate a significant change at the sensor output as shown in Figure 2.9 where the effects of different types of mismatch resistances are depicted.

2.6. Parasitic Effects

Due to the structure composed of layers with different voltage levels in CMOS realizations, undesirable parasitics are generated in the devices. They limit the performance of the offset reduction techniques like spinning current method since the parasitic capacitors need to be charged and discharged during the switching operation in implementation of the methods. Although the parasitic capacitances are on the order of femtofarads, they are big enough to limit the switching frequency of the offset

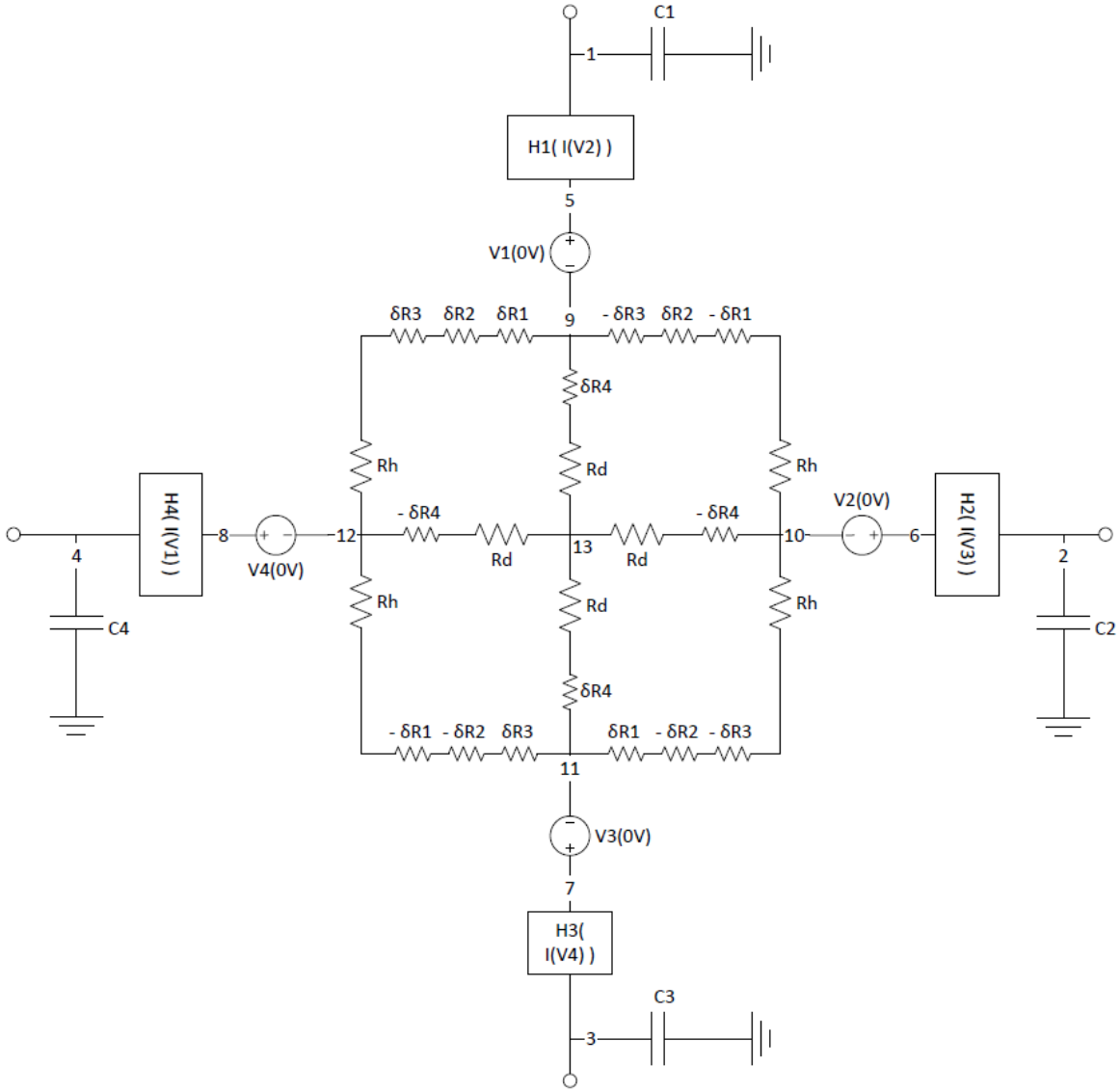

Figure 2.7. Offset inclusion to the compact cross-shaped Hall sensor model with eight resistors.

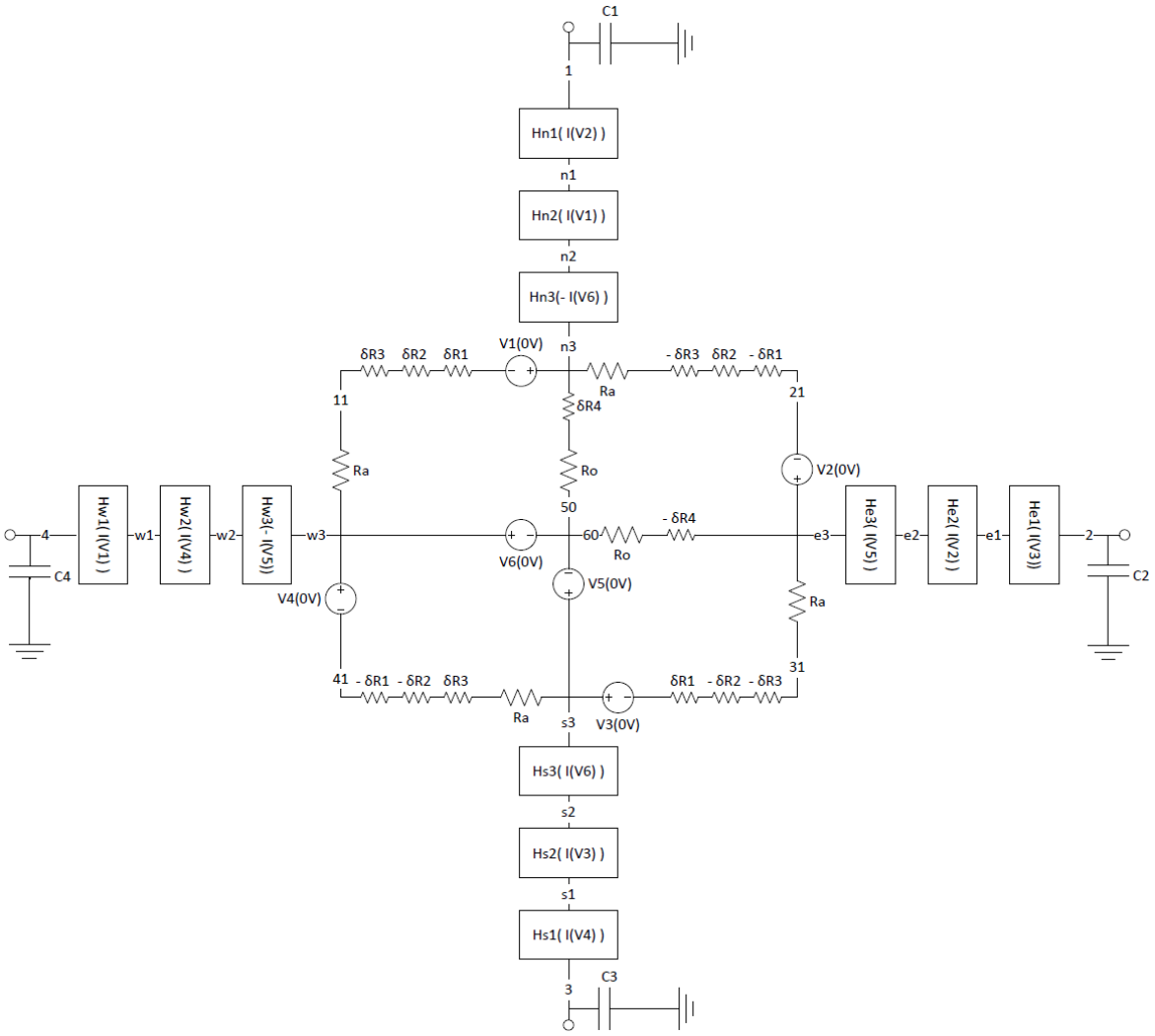

Figure 2.8. Offset inclusion to the compact cross-shaped Hall sensor model with six resistors.

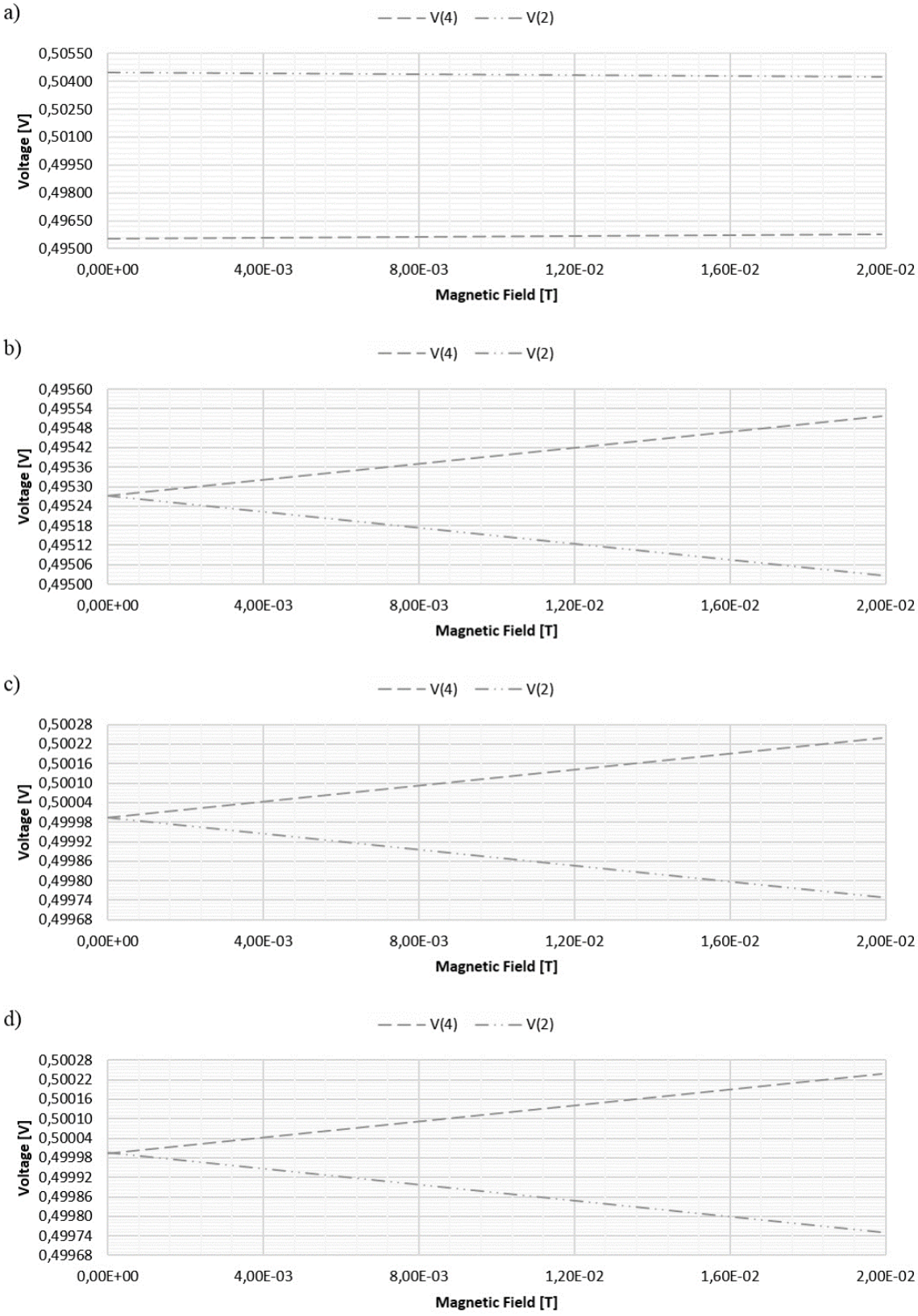

Figure 2.9. The voltage at the output terminals of the Hall device with mismatch resistances a) $\delta R1$, b) $\delta R2$, c) $\delta R3$, or d) $\delta R4$ under the biasing along 1 - 3 direction with 1 V voltage supply.

reduction methods. For the proper design of front end circuit which includes the offset reduction methods, the transient behavior of the Hall device should be accurately incorporated into the model.

The dominant source of parasitics in the Hall devices is the depletion capacitance of the pn junction between the n-well and the p-substrate. Since the depletion capacitance is distributed across the body of the Hall device, it is represented by four capacitors which are placed at the contacts of the Hall device. The value of the contact capacitors is defined based on the depletion capacitance per area equation,

$$C_{pn} = \sqrt{\frac{q\epsilon_{si}}{2} \times \frac{N_{D,nw} \times N_{A,sub}}{N_{D,nw} + N_{A,sub}} \times \frac{1}{V_D - U_{pn}}} \tag{2.35}$$

where V_D is defined by Equation 2.30. It should be noted that the depletion capacitance also depends on the voltage at the contact.

2.7. Geometrical Effects

Geometrical correction factor, which models the short circuit effects due to the sensor contacts, as well as the geometry of the device, is affected by the applied magnetic field although its change is relatively small for the low magnetic fields, as shown in Figure 2.10. Nevertheless, the dependency on the applied magnetic field is included in the model as the geometrical correction factor is defined to be dependent on the magnetic field parametrically using the equation for cross-shaped Hall device in [10].

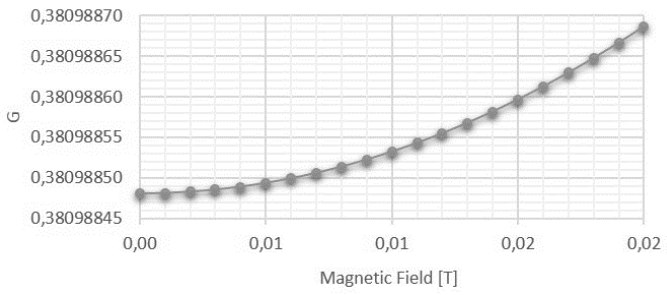

Figure 2.10. Dependency of geometrical correction factor on the magnetic field.

$$G = 1 - 5.0267 \times \frac{\arctan(\mu_n \times r_H \times B)}{\mu_n \times r_H \times B} \times e^{-\frac{\pi}{2} \times \frac{W+2L}{W}} \tag{2.36}$$

2.8. Conclusion

The presented compact cross-shaped Hall sensor model is designed to accurately model nonlinearity, temperature drift effect, offsets due to fabrication dispersion and mechanical stress, geometrical effect, and frequency response, together with the Hall Effect. Since strong magnetic fields will not be used in the magnetic sensing microsystem, magneto-resistance effect and carrier scattering effect are not included in the model. Also, considering the dimensions of the Hall plate in the microsystem, lateral diffusion effect is not significant to be included in the model.

With the adequate simplifications and assumptions, a compact model of the sensor is obtained without losing the required accuracy. Figure 2.11 presents the results of a finite element method (FEM)-based simulation of the cross-shaped Hall sensor to be used in the microsystem and compact SPICE model simulation as a voltage difference of 1 V is applied to two nonconsecutive terminals of the sensor. The presented sensor absolute sensitivity is 12.296 mV/T. The model relies only on the technological, physical, and geometrical parameters, enabling the use of the model for different Hall devices, as the parameters of the model are shown in Table 2.1. The values of the elements in the model are determined by technological and physical modeling instead of parameter fitting based on simulation results.

It is noticed that two sensor model architectures generate similar sensor response in terms of offsets, nonlinearity, and Hall Effect modeling. However, the model architecture with six resistors whose resistances are calculated based on equations with fitting parameters has a little smaller resistance and, as a result, smaller absolute sensitivity and noise than the model architecture with eight resistors for the parameters in Table 2.1. It should be noted that the sensor model architecture with eight resistors in the

resistive bridge is decided to be used in the remaining parts of this thesis, including the design of the front end circuit, since its resistances are calculated based on equations with purely technological, physical, and geometrical parameters.

Table 2.1. Parameters of the cross-shaped Hall sensor model.

Parameter	**Symbol**	**Value**	**Unit**
Electron charge	q	1.6E-19	C
Silicon absolute permittivity	ϵ_{si}	1.04E-10	F/m
Boltzmann constant	k	1.38E-23	$m^2kg/(s^2K)$
Intrinsic carrier concentration	n_i	1.49E+16	m^{-3}
N-well doping concentration	$N_{D,nw}$	1.7E+23	m^{-3}
P-substrate doping concentration	$N_{A,sub}$	3.41E+19	m^{-3}
Electron mobility	μ_n	4.16E-02	$m^2/(Vsec)$
PN junction diffusion voltage	V_D	6.20E-01	V
N-well thickness	t_{nw}	2.33E-06	m
Nw-Psub depletion region thickness	$w_{nw,sub}$	9.74E-10	m
Hall scattering factor	r_H	1.2	-
Geometrical correction factor	G	0.381	-
Sensor width	W	6.00E-06	m
Sensor length	L	1.00E-06	m

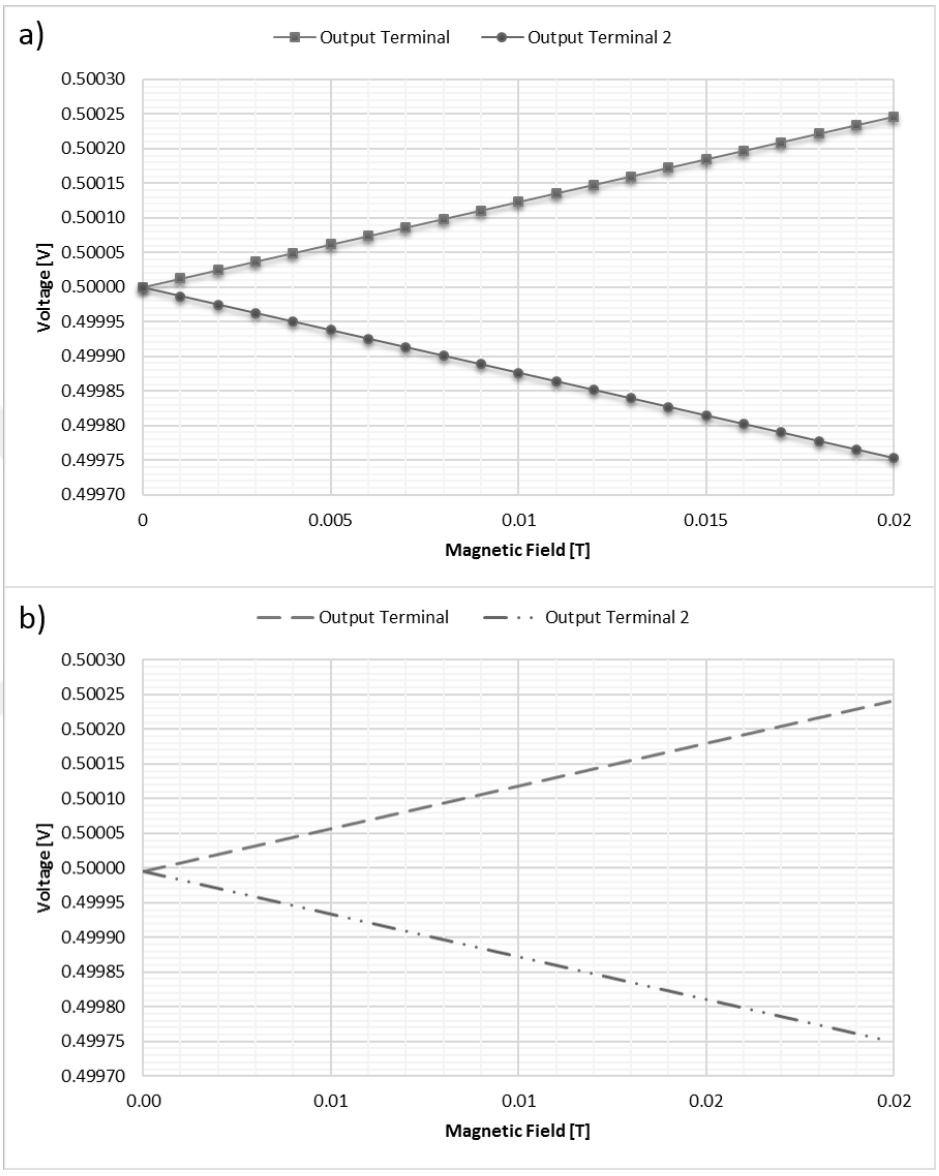

Figure 2.11. Results of a) a FEM-based simulation of the cross-shaped Hall sensor and b) compact SPICE model simulation as a voltage difference of 1 V is applied to two nonconsecutive terminals of the sensor.

3. LOW OFFSET AND LOW NOISE FRONT END CIRCUIT DESIGN

The function of the front end circuits in magnetic sensing microsystems is to maximize the precision of the magnetic field measurements.

3.1. State of Art

State of the art studies focus on removing or reducing the effect of factors which limit the performance of the sensor and the precision of the magnetic field measurements: offset, noise, temperature drift, and nonlinearity. Different methods for offset cancellation, noise reduction, minimization of temperature drift effect, and maximization of linearity are presented in the studies. The characteristics and performance metrics of the Hall sensor microsystems in the state of art are presented in the Table 3.1.

Heidari et al. proposed a current-mode Hall sensor microsystem which includes two Hall plates for providing differential current at the output and implements a 4-phase spinning current technique by using 32 switches in the biasing circuit for rejecting the sensor offset as it is one of the possible methods to reduce the offset voltage and the low frequency noise of the Hall sensor by periodic supply and output permutations [19]. The Hall sensors is biased by injecting a constant current to two consecutive contacts of the first Hall plate and draining the same current from two consecutive contacts of the second Hall plate whereas the other contacts of two plates are connected to each other to form the differential system output. An integrator with chopper stabilization, which is connected directly to the output of the sensor pair, to amplify the low-level output signal while eliminating the offset and low frequency noise of the amplifier, and a switched-capacitor filter to increase the stability of the system response were added in the further works [20, 21]. The stated low offset levels present the effectiveness of the spinning current method in cancelling the sensor offset.

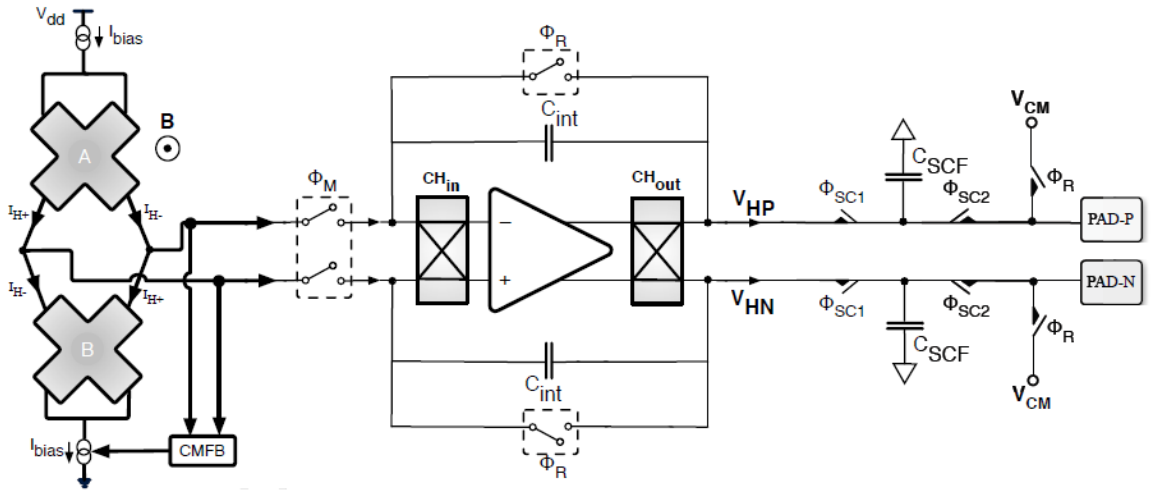

Figure 3.1. Magnetic sensing microsystem with spinning current method and chopper modulation, presented in [20] and [21].

The Hall sensor microsystem developed by Min et al. is composed of a Hall plate, a biasing circuit with spinning current method implementation, a switched biasing amplifier with chopping technique realization, an integrating filter to remove the Hall plate offset and reject the residual noise, and a switched capacitor delta-sigma ($\Delta\Sigma$) modulator to convert analog signal to digital bitstream [4]. Chopping technique, which is realized in the switched biasing amplifier, is a widely-used method in amplifiers for cancellation of offset and 1/f noise without folding the noise into the baseband as the input signal is modulated with a square wave before being processed, and the processed signal is demodulated at the output. In spite of the known success of the technique in rejecting the low frequency noise, the microsystem has degraded noise performance due to the charge injections by the switched biasing in the amplifier, which decreases power consumption of the microsystem significantly by periodically switching between active and inactive states.

Frounchi et al. presented a magnetic sensing microsystem which consists of four Hall sensors, a biasing circuit implementing the spinning current technique, a differential difference amplifier with five input pairs where the Hall sensors are connected, a standard two-stage CMOS amplifier which provides the gain of the microsystem, a

switched-capacitor synchronous demodulator, and an output low-pass filter [22]. As the input signal is modulated to a higher frequency by the application of spinning current technique, the switched-capacitor synchronous demodulator shifts the spectrum of the modulated input back to the baseband; and, the low-pass filter extracts the Hall voltage by rejecting the noise and offset shifted to the higher frequencies. To further decrease the offset and improve the signal-to-noise ratio as stated in [23], an array of Hall sensors is used. Nevertheless, the use of an array of Hall sensors results in rather high thermal noise density in the microsystem due to the high resistance of the miniature Hall plates, which cannot be cancelled by using spinning current method. The noise and offset of the amplifiers are also left as residuals as the proposed microsystem lacks any method to cancel the offset and noise of the amplifiers.

Kammerer et al. proposed a biasing circuit which is designed for multiple strip Hall sensor and can also be used for biasing an array of Hall sensors [24]. The biasing circuit contains a low-noise operational transconductance amplifier with multiple output stages where the new shape of Hall sensor is inserted to be biased by a constant current. The Hall voltage is measured from one of the measurement contacts of the Hall sensor as the other measurement contact, which is connected to the inverting input of the operational amplifier, is grounded due to the ground connection of the noninverting input. A chopping technique is applied to reject the flicker noise and mismatch-caused offset to higher frequencies by switching the output stages symmetrically. And, the output signal is low-pass filtered for removing the noise and offset. In addition, a network of Hall sensors is inserted to the output stages of the operational transconductance amplifier in the biasing circuit while the output voltage of the system is equal to the sum of individual contributions of the Hall sensors [25]. Also, orthogonal coupling is employed in the study by connecting even number of orthogonal (in terms of biasing directions) Hall sensors by their measurement contacts for removing the offset caused by mechanical stress. However, the effectiveness of the orthogonal coupling method depends on the matching of the mechanical stress on the Hall sensors in the network as well as the physical structure of the Hall sensors including the imperfections, but they do not generally match [26].

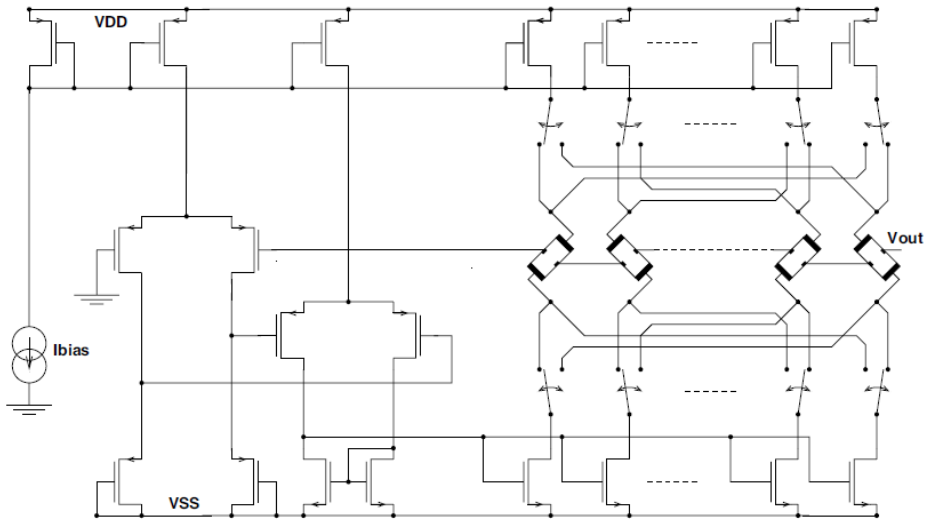

Figure 3.2. Sensor front end with chopper modulation and quadrature coupling method, presented in [25].

Operational transconductance amplifiers which have single output stages are used to bias the Hall sensors with constant current [27, 28]. A nested chopper modulation structure is added to the biasing circuit to remove 1/f noise and offset of the operational transconductance amplifier, and implements spinning current technique to reduce the sensor offset [29]. As shown in Figure 3.3, two chopping stages at the input and output of the amplifier are employed with the aim of generating a steadier virtual ground at the sensor measurement contact. The study reports a decrease in the noise level of the system due to the chopper modulation method; however, no success metric for the offset cancellation is presented.

Blagojevic et al. presented another Hall sensor microsystem composed of sensor biasing system which provides the biasing current and performs dynamic spinning of the bias current, analog front end which incorporates a high-linearity differential amplifier to amplify the sensor output signal, and digital back end which converts the analog signal to the digital domain with the $\Delta\Sigma$ modulation technique and low-pass filtering [30]. To improve the performance of the system in terms of offset and low-frequency noise, a synchronized chopper modulation and demodulation scheme is included in the sensor bias system and $\Delta\Sigma$ convertor, respectively. The inverting unity gain amplifier in

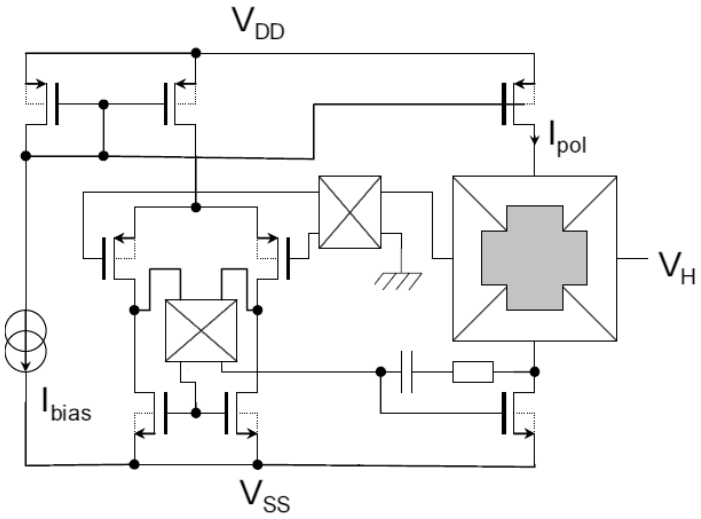

Figure 3.3. Sensor front end with spinning current method and chopper modulation, presented in [29].

the sensor bias system, which provides fully differential ground-centered voltage across the sensor, complicates the design of the microsystem as it requires the operational amplifier to have high open loop gain and small output resistance in order to prevent distortions of the bias current, and resistors in the feedback loop to have high resistances. Moreover, 2-stage dynamic offset cancellation scheme performed in the study fails in removing all types of offset which can occur in the Hall sensors. The earlier work in [31] presents an analog front end with a differential difference amplifier which consists of two differential transconductance stages, one connected to the sensor output and the other to the output feedback network formed with resistors. The limited system performance by the linearity of the differential difference amplifier makes the instrumentation amplifier a better alternative for the magnetic sensing microsystem even though it consumes larger area.

Bilotti et al. developed a magnetic sensing microsystem to include a Hall plate, a biasing circuit which implements dynamic offset cancellation method, a differential amplifier with differential output, four sample-and-hold circuits which serve the low-pass filtering function, and a summing feedback difference output amplifier [32]. The microsystem incorporates the operation of a quasi-chopped amplifier where the first

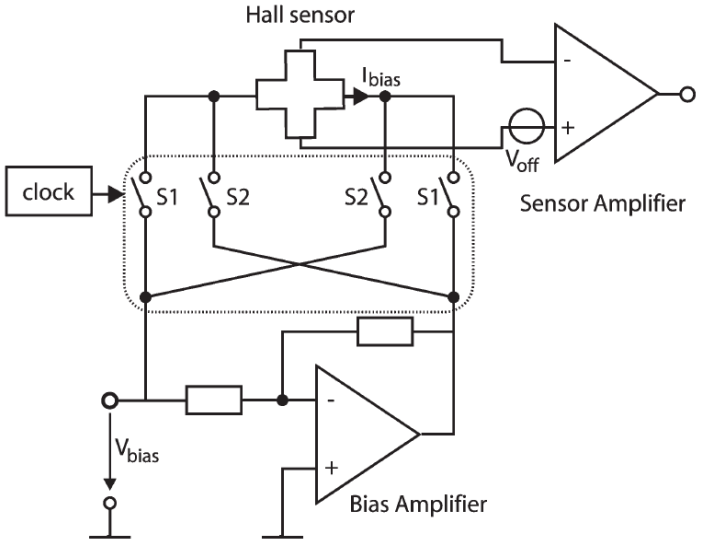

Figure 3.4. Sensor front end with spinning current method, presented in [30] and [31].

pair of switches is placed into the switched Hall plate configuration and the second pair is built in the sample-and-hold circuits. The sampling of the signal performs the low-pass filtering operation by removing the high offset ac ripples; and the output amplifier adds the sampled output signals of two phases and rejects the offset and low frequency noise of the sensor and amplifier. Although the proposed offset cancellation scheme is stated to remove the offset of the sensor and the first amplifier successfully, 2-phase dynamic offset cancellation is known to fail mainly in rejecting sensor offset caused by mechanical stress. Moreover, any possible offset in the output amplifier will be visible at the system output as the study does not propose any solutions for its cancellation. Portmann et al. presented a modified biasing circuit in [33] where a floating body transistor was added in between the nodes marked as Hi and Lo in Figure 3.5 to limit the capacitive coupling through the disconnected input switches whereas the remaining of the proposed microsystem includes an amplifier which converts Hall voltage to current before amplification, a demodulation stage which is implemented in voltage mode as the signal is converted to voltage before and converted back to current after, a low-pass filter, and an A/D converter.

Some of the studies, such as the ones presented in [34] and [35], employ integrated magnetic flux concentrators, which are placed between the Hall plates and the magnetic

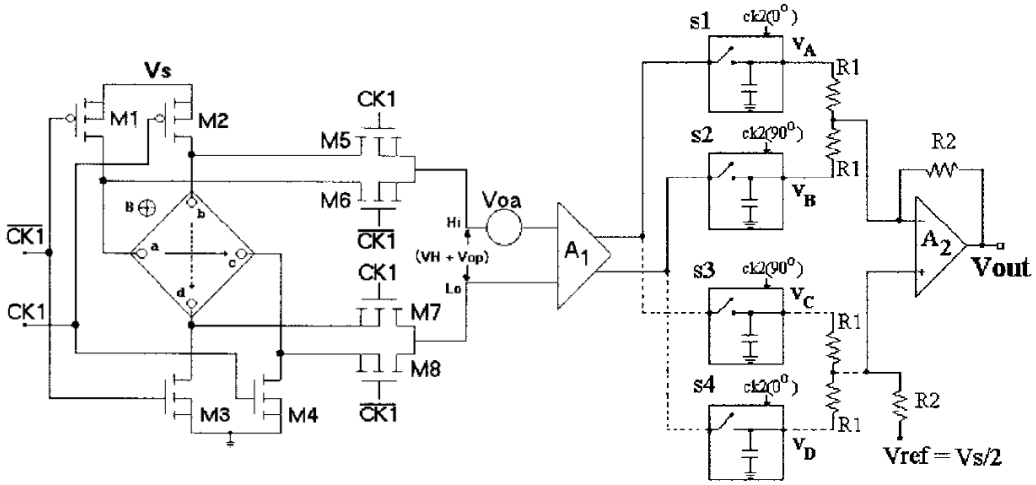

Figure 3.5. Magnetic sensing microsystem with dynamic offset cancellation method, as presented in [32].

field source as the chip surface is deposited with a high-permeability ferromagnetic layer, to intensify the magnetic field and to improve the sensitivity of the sensor. The use of magnetic flux concentrators increases the detectability of the magnetic field, resulting in eased design of low-offset circuits.

The Hall sensor analog front ends in references [36] and [37] incorporate integrated reference coils to be used in continuous gain calibration scheme for increasing the temperature stability of the system. The microsystem includes three switched capacitor demodulators, which are connected to the output of the amplifier, to extract the signal to be sensed, offset of the system, and modulated reference signal generated by the reference coil. The gain of the system is continuously calibrated by comparing the extracted reference signal with a nominal value and adjusting biasing current of the sensor accordingly. And, the offset is corrected by changing compensation current of the amplifier based on the comparison of the extracted offset value with zero. The studies in [38] and [39] presented a modified microsystem which includes voltage-to-current converter to provide current-mode output. The proposed solutions are stated to generate similar temperature stability figures to the state of the art but including integrated coils which increase the area of the system.

Table 3.1. Performance summary and comparison of the Hall sensor microsystems in the state of the art and proposed front end circuit.

	Technology	**Supply Volt.**	**Bias Mode**	**Out. Mode**	**Sensor Bias**	**Amp. Gain**	**Sensitivity**	**Resolution**	**Offset**	**Noise**	**Bandwidth**
[19]	0.18 um	1.8 V	Current	Current	12 uA	n/a	0.02 1/T				
[20, 21]	0.18 um	1.8 V	Current	Voltage	12 uA	1000	20 V/T		50 uT		
[4]	0.18 um	3.3 V	Current	Voltage			0.005 V/T	195 uT	150 uT	25 uT/$\sqrt{Hz}$	
[22]	0.8 um	5 V	Current	Voltage	2.3 mA	500	86 V/T	33 uT	160 uT	0.8 uT/$\sqrt{Hz}$	1.7 kHz
[24, 25]	0.6 um	5 V	Current	Voltage	2 mA		0.195 V/T	32 uT			1 kHz
[27, 28]	0.6 um	5 V	Current	Voltage	1.2 mA	100	0.134 V/T	5.2 uT			1 kHz
[29]	0.35 um		Current	Voltage	1 mA		0.092 V/T	15 uT	2.8 mT		1.6 kHz
[30]	0.5 um SOI	3 V	Current	Voltage	0.7 mA	13.5	0.490 V/T				
[31]	0.5 um	3 V	Current	Voltage		13.5					
[32]	2 um BiCMOS	5 V	Current	Voltage	2 mA	30	25 V/T		0.5 mT		30 kHz
[33]	1 um SOI	5 V	Current	Current	0.4 mA		0.082 V/T	1 mT	1.5 mT	17 uT/$\sqrt{Hz}$	3.5 kHz
[34]						n/a	125 V/T		0.15 mT		30 kHz
[35]	0.8 um	5 V	Current	Voltage		210	420 V/T	0.1 mT	20 uT		25 kHz
[38, 39]	0.35 um	3.3 V	Current	Current	1 mA		50 1/T		40 uT		500 kHz
[40]	0.18 um	5 V	Current	Voltage	0.35 mA	50		89 uT	25 uT	0.28 uT/$\sqrt{Hz}$	100 kHz
[41]	0.8 um	5 V	Current	Voltage	1 mA	10	0.2 V/T	0.1 uT			
This Work	0.13 um	1.2 V	Voltage	Voltage	1.2 V	103.5	5.25 V/T	31.75 uT	7.62 uT	167 uV (rms)	1 kHz

3.2. Circuit Architecture

The function of front end circuits in Hall sensor microsystems is to maximize the precision of the magnetic field measurements by minimizing the limitations on the sensor performance. The precision of the measurement is determined by the figures such as the measurement resolution, nonlinearity of the response, and stability of the system. As the resolution is defined by signal-to-noise ratio (SNR) of the sensing microsystem, the front end circuit should provide high amplification factor for the significant signal while decreasing the noise level of the system. Offset of the sensing microsystem is another limitation on the DC resolution as it causes distortions in the measurements; therefore, the microsystem should also cancel the offset.

The magnetic sensing microsystem contains the main building blocks of the sensor biasing circuit, Hall sensor, amplifier, and integrator with low-pass filter; whereas the sensor biasing circuit and amplifier are the components of the front end circuit. The front end circuit needs to be designed to increase the sensitivity of the sensor, remove the sensor offsets caused by imperfections and mechanical stress, reduce the system offsets caused by the electronics circuits, and reduce the noise of the whole system including the thermal and 1/f noise generated by the sensor and electronics circuits.

The biasing circuit applies a voltage difference across the sensor to supply the Hall Effect sensor with a current flow. The current flow across the sensor makes a Hall voltage appear between the unbiased sensor contacts when the sensor is exposed to a magnetic field perpendicular to the Hall plate.

The voltage difference across the unbiased sensor contact pair, which is the significant signal defined as Hall voltage, is on the order of hundred microvolts. A differential amplifier is connected to the output of the sensor to amplify the voltage difference at the sensor output. The required amplification factor for increasing the sensitivity of the sensor is provided by the differential amplifier. A single stage instrumentation amplifier with two operational amplifiers and a resistive feedback is designed to have differential input and differential output.

As imperfections in the fabrication process and mechanical stress causes offsets in the response of the Hall sensor to the applied magnetic fields, dynamic offset cancellation method is employed in the front end circuit for rejecting the distortions in the sensor response. Biasing contact pair of the sensor is periodically permuted to bias the sensor across 4 different directions. Together with the biasing contact pair, the measurement contact pair is also changed in each phase to generate Hall voltage across 4 different directions. The contacts of the Hall sensor are set as input and output contact pairs such that the polarity of the Hall voltage across the sensor changes through the phases of the dynamic offset cancellation scheme while the offsets due to the fabrication imperfections and mechanical stress has constant polarity at all phases.

For rejecting the offset of the amplifier and reducing the low frequency noise of the sensor and readout electronics including the amplifier, chopping technique is implemented in the instrumentation amplifier. A chopper modulation stage is placed to the input of the amplifier for changing the polarity of the signal to be amplified in each consecutive phase. Although the signal changes polarity, the input offset of the amplifier is constant at all phases. Therefore, with the application of chopping in the amplifier input, the signal gets modulated to the chopping frequency while the offset is left at DC. Chopper demodulation is applied to the output of the amplifier to bring the modulated signal back to DC and reject the combined amplifier and sensor offset to higher frequencies. Demodulation is achieved by interchanging the polarity of amplifier outputs at the same frequency as the one used in modulation. The noise components at low frequency are treated just the same as the offset of the system by the chopping technique. Therefore, the chopping technique reduces 1/f noise in the Hall sensor and front end circuit as the chopping frequency is chosen to be higher than the corner frequency where the 1/f noise becomes negligible. A low-pass filter in the back end circuit of the magnetic sensing microsystem can cancel the offset and noise of the sensor and front end circuit as they are pushed to higher frequencies. The cut-off frequency of the low-pass filter should be sufficiently smaller than the chopping frequency to achieve good attenuation of the offset and 1/f noise, increasing the performance of the cancellation.

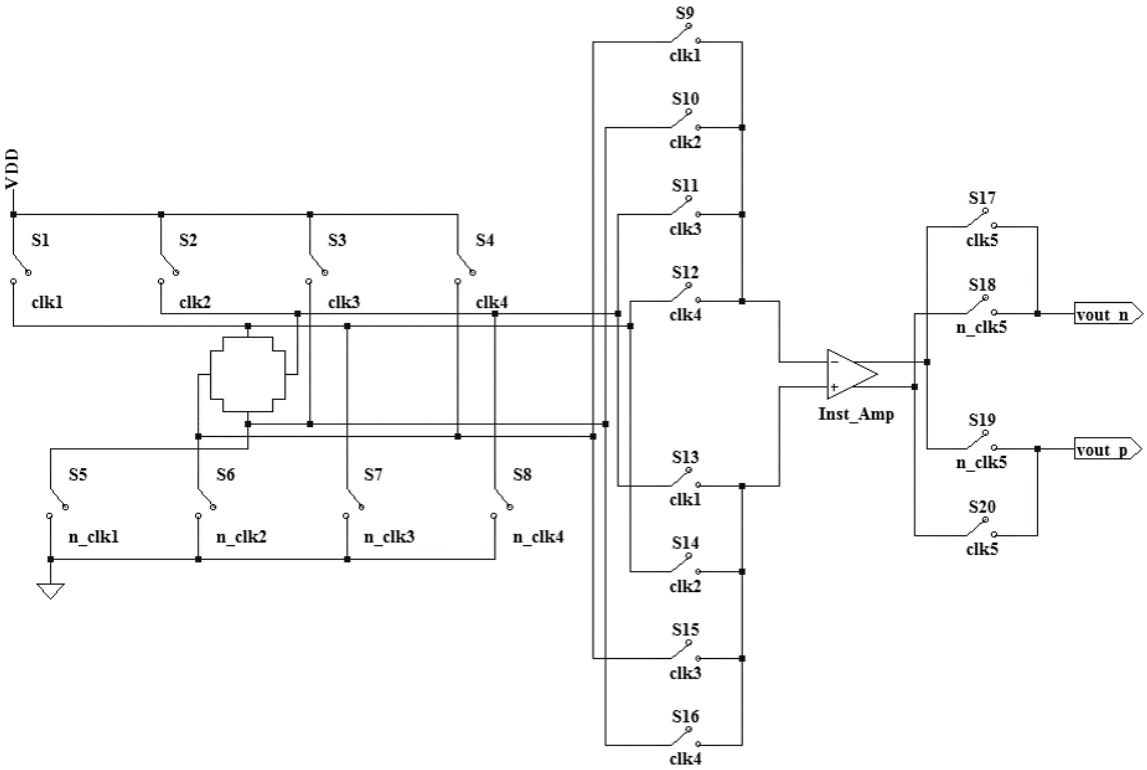

Figure 3.6. Low offset and low noise front end circuit architecture in the magnetic sensing microsystem.

The biasing circuit with an implementation of 4-phase dynamic offset cancellation method is designed using 8 switches to bias the Hall sensor between a voltage supply of 1.2 V and ground. Four of the switches are connected to voltage supply for directing current to a different contact of the Hall sensor in each phase, defining the positively biased sensor contact. The other switches are used to connect ground to the sensor contacts while only one of them is closed in each phase to define the other biased contact. The measurement contacts of the sensor are determined similarly by using 8 switches between the Hall sensor output and the input of the amplifier. Four of them define the positive measurement contact while the other four switches set the negative measurement contact. All of the switches are controlled by 4 clock signals which have nonoverlapping high states so that only one switch in the groups of four switches is closed during a phase and the others are open.

The switches between the Hall sensor output and the input of the amplifier also serves as the chopper modulation stage of the proposed chopping technique implementation. Moreover, 4 switches are placed to the output of the amplifier to apply the chopper demodulation. They are connected in groups of two to the positive and negative amplifier output contacts and controlled by another clock signal, whose frequency is twice the one of other clocks, to interchange the polarity of the amplifier output in each phase.

The architecture of the proposed low offset and low noise front end circuit in the magnetic sensing microsystem is presented in Figure 3.6.

3.3. Dynamic Offset Cancellation

Although the cross shaped Hall sensor is the optimum structure to fit lowest noise and offset, the need for methods of noise reduction and offset cancellation still exists. The offset cancellation method should be designed properly to cancel all types of offset caused by imperfections and mechanical stress. Since the responses of the Hall sensor to different offset sources differentiate from each other, the performance of the method in cancelling offset should be examined carefully.

Orthogonal coupling method is one of the methods used widely in offset cancellation, especially in the microsystems where an array of Hall plates is used. The method reduces the sensor offset as much as the offsets in the orthogonally biased Hall plates match; therefore, its success is determined by the matching of the imbalance sources such as physical structure of the sensors. Nevertheless, offsets of closely located Hall plates on a wafer generally do not present a significant correlation [33], degrading the effectiveness of the offset cancellation method.

A dynamic offset cancellation method based on spinning of the current flow is proposed to cancel the sensor offset. A 2-phase dynamic offset cancellation method would be the simplest implementation by interchanging the supply and output contact pairs periodically. However, it is noticed to be insufficient to cancel out the sensor

offset completely. Using a 2-phase cancellation scheme whose input and output contact configurations are given in Table 3.2, the shear stress, which produces the highest amount of offset in the sensor response, can be successfully removed. The offsets due to shear stress in two phases, $V_{offset1}$ and $V_{offset2}$, are given by,

$$V_{offset1} = V_{bias} \times \delta R1 \times \frac{2R_D}{R_H \times (2R_D + R_H)} \tag{3.1}$$

and,

$$V_{offset2} = -V_{bias} \times \delta R1 \times \frac{2R_D}{R_H \times (2R_D + R_H)} \tag{3.2}$$

where V_{bias} denotes the biasing voltage difference across the sensor and resistances in Figure 2.7 are used without taking into account the nonlinear resistance effect. In spite of the evaluated success of the method in cancelling offset caused by shear stress, it fails to cancel the offset caused by combined effects of shear and compression stress. The offsets in two phases are,

$$V_{offset1} = V_{bias} \times \delta R1 \times (R_D + 2\delta R4) \times \frac{1}{R_H \times (2R_D + R_H)} \tag{3.3}$$

and,

$$V_{offset2} = -V_{bias} \times \delta R1 \times (R_D - 2\delta R4) \times \frac{1}{R_H \times (2R_D + R_H)} \tag{3.4}$$

whose average clearly leads to a residual offset [42],

$$V_{offset} = V_{bias} \times \delta R1 \times 2\delta R4 \times \frac{1}{R_H \times (2R_D + R_H)} \tag{3.5}$$

Fabrication imperfections in the biasing direction do not produce offset at the sensor output as it is symmetric from the measurement contacts but the common-mode voltage of the sensor output changes based on the amount of imperfection. Nevertheless, fabrication mismatch perpendicular to the biasing direction creates a weak offset

Table 3.2. Input and output contact configurations of a 2-phase offset cancellation method where the sensor contact names refer to Figure 2.7.

	Vin1	Vin2	Vout1	Vout2
Phase #1	1	3	4	2
Phase #2	2	4	1	3

due to the modulation of the sensor resistance by voltage. The offset voltages due to fabrication imperfections along the vertical (1 – 3) and horizontal (2 – 4) directions are given by,

$$V_{offset1} = -V_{bias} \times \delta R3 \times (\Delta R_H + \delta R2) \times \frac{2R_D}{{R_H}^2 \times (2R_D + R_H)} \tag{3.6}$$

and,

$$V_{offset2} = V_{bias} \times \delta R2 \times (\Delta R_H + \delta R3) \times \frac{2R_D}{{R_H}^2 \times (2R_D + R_H)} \tag{3.7}$$

for two phases of the offset cancellation scheme, where ΔR_H denotes the difference between the nonlinear R_H resistances across the biasing direction [42]. The residual offset depends on the difference between $\delta R2$ and $\delta R3$,

$$V_{offset} = V_{bias} \times \Delta R_H \times (\delta R2 - \delta R3) \times \frac{R_D}{{R_H}^2 \times (2R_D + R_H)} \tag{3.8}$$

and becomes zero only when the amounts of fabrication imperfections along two directions are equal. If nonlinearity is not taken into account, 2-phase offset cancellation method would be sufficient to cancel the offset caused by imperfections [43].

The presented insufficiency of 2-phase offset cancellation method necessitates a 4-phase implementation. Using a 4-phase cancellation scheme whose input and output contact configurations for each phase are given in Table 3.3, the offset in the additional phases, caused by fabrication imperfections along the vertical (1 – 3) and horizontal (2

– 4) directions, would be,

$$V_{offset3} = -V_{bias} \times \delta R3 \times (-\Delta R_H - \delta R2) \times \frac{2R_D}{{R_H}^2 \times (2R_D + R_H)} \tag{3.9}$$

and,

$$V_{offset4} = V_{bias} \times \delta R2 \times (-\Delta R_H - \delta R3) \times \frac{2R_D}{{R_H}^2 \times (2R_D + R_H)}. \tag{3.10}$$

The residual offset, the average of offset voltages in four phases, becomes zero at the end of four phases, presenting the success of the 4-phase cancellation scheme.

Table 3.3. Input and output contact configurations of the offset cancellation method extended to 4-phase.

	Vin1	Vin2	Vout1	Vout2
Phase #1	1	3	4	2
Phase #2	2	4	1	3
Phase #3	3	1	2	4
Phase #4	4	2	3	1

As the failure of 2-phase offset cancellation method in removing all types of offset is noticed and the need for a 4-phase scheme for better offset cancellation is presented, it is decided to design a 4-phase dynamic offset cancellation method. The proposed dynamic offset cancellation method separates Hall voltage and sensor offset in frequency domain by modulating the Hall sensor output. The input and output contact pairs of the Hall sensor are changed periodically based the 4-phase scheme defined in Table 3.4, to make electrical current direction rotate by $\pi/2$ from one phase to another. The contacts are assigned as biasing and measurement contacts such that the polarity of the Hall voltage changes in each phase whereas the one of offset is constant in all phases as it is achieved by rotating biasing and measurement contacts in opposite directions in each consecutive phase. Nevertheless, the magnitudes of Hall voltage and offset voltage are not affected by current spinning since sensitivity of the Hall sensor does not change

throughout the phases. The proposed method effectively shifts Hall voltage to a higher frequency while the sensor offset caused by fabrication imperfections and mechanical stress is left as a DC component.

Table 3.4. Input and output contact configurations of the dynamic offset cancellation method where the sensor contact names refer to Figure 2.7.

	Vin1	Vin2	Vout1	Vout2
Phase #1	1	3	4	2
Phase #2	2	4	3	1
Phase #3	3	1	2	4
Phase #4	4	2	1	3

It should be noted that the input and output contact definitions in Table 3.4 makes the sensor offset indistinguishable from the offset of the amplifier, enabling the simultaneous processing and cancelling of sensor offset together with the amplifier offset.

The phases are determined by the non-overlapping clocks. Clk1, clk2, clk3, and clk4 are used to activate phase #1, phase #2, phase#3, and phase #4. In each phase, only one of the clock signals is at high state as they are shown in Figure 3.7. The frequency of the clocks is limited by the settling time after each transition; and, the settling time is determined by the parasitic elements in the Hall sensor and biasing circuit. During a transition from phase #1 to phase #2, the voltage at sensor contact named as 1 should decay to 0.6 V from 1.2 V and the one at the sensor contact 3 should increase to 0.6 V from ground. As large changes of the contact voltages are presented, a certain time is needed for voltages at the contacts to settle to their final values. A clock frequency of 100 kHz is determined to provide enough time for settling of the contact voltages. Furthermore, due to the switching of the input and output contacts, transient spikes appear in the sensor response occurring at the transitions between the stages. To minimize the spikes and their effects, nonoverlapping clocks are used in the biasing circuit.

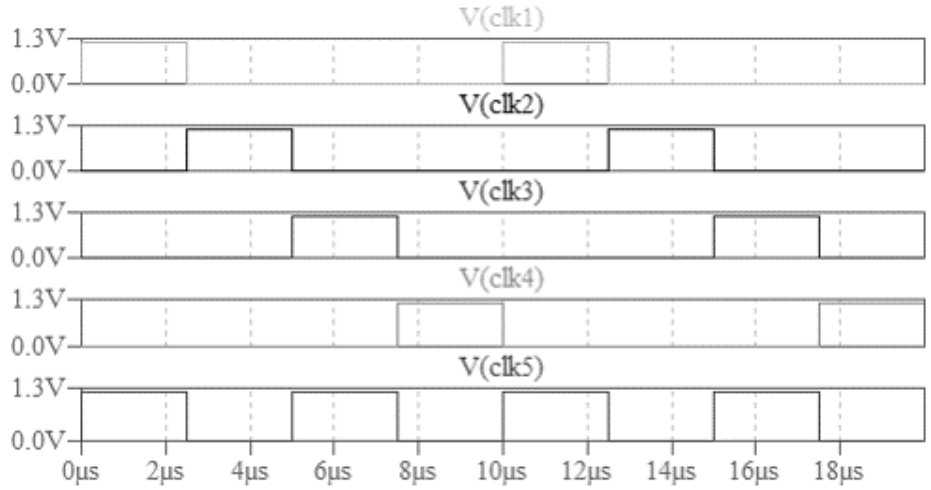

Figure 3.7. Clocks of the dynamic offset cancellation method and chopping technique implementations.

Periodic permutations of the sensor contacts to form the input and output contact pairs are made by using of switches. 8 switches are used in the biasing circuit to direct positive voltage and ground connection to the contacts of the Hall sensor based on four different configurations shown in Table 3.4. The switches which define the positively biased contact are implemented with PMOS transistors whose sources are at 1.2 V and gates are used as control nodes. Drains of four transistors are connected to sensor terminals to bias one of them with positive voltage as the transistor is enabled by the respective clock signal. Furthermore, NMOS transistors are used to direct ground connection to the sensor terminals as their sources are at ground and gates are clocked while their drains are connected to the sensor terminals. It should also be noted that transistors in the biasing circuit have their bodies connected to their sources.

The NMOS and PMOS transistors, which are connected to ground and voltage supply, respectively, are properly sized so that the voltage drop across the switches in the closed state is small enough not to decrease the voltage difference across the sensor so much as it degrades the sensitivity of the sensor. Moreover, they are sized accordingly to equalize their drain-to-source voltages, generating symmetric biasing across the sensor, which sets the common mode voltage at the sensor output to 0.6 V.

Another set of 8 switches are placed between the Hall sensor output and the input of the amplifier to define the measurement contacts based on the configuration scheme in Table 3.4. All of the switches are implemented with NMOS transistors whose gates form the control nodes of the switches. The transistors pass the voltage at the source of the transistor to the drain terminal if high voltage is applied to the gate terminal, to operate as a voltage controlled switch. Therefore, clock signals are applied to the gates of the transistors to control their operation. Four of the transistors are used to direct a different sensor contact to the positive input of the amplifier in each phase while the other four transistor define the sensor contact to be connected to the negative amplifier input.

The schematics of the biasing circuit which biases the Hall sensor between the voltage supply, 1.2 V, and ground and implements the dynamic offset cancelation method is presented in Figure 3.8. The terminal connections of the transistors, which set the sensor input and output contacts in each phase based on the configurations in Table 3.4, are also presented in the schematics.

Removal of the sensor offset which is discriminated from the Hall voltage at the sensor output is achieved by the processing circuits in the back-end circuit of the magnetic sensing microsystem. As the sensor offset and Hall voltage are separated in the frequency domain, a properly designed filter in the back end circuit can reject the sensor offset.

The dynamic offset cancellation method suppresses the disturbances that are slower than switching frequency as they can be considered constant during the phases of the switching scheme. By selecting a clock frequency which is higher than the 1/f noise corner frequency of the Hall sensor, the proposed method is also used to cancel the low frequency noise components. Nevertheless, thermal noise of the Hall sensor due to the resistive coupling is not affected by the application of dynamic offset cancellation method and cannot be reduced. The thermal noise depends on the resistance of the Hall sensor; and it can be neglected as it is small when compared to flicker noise.

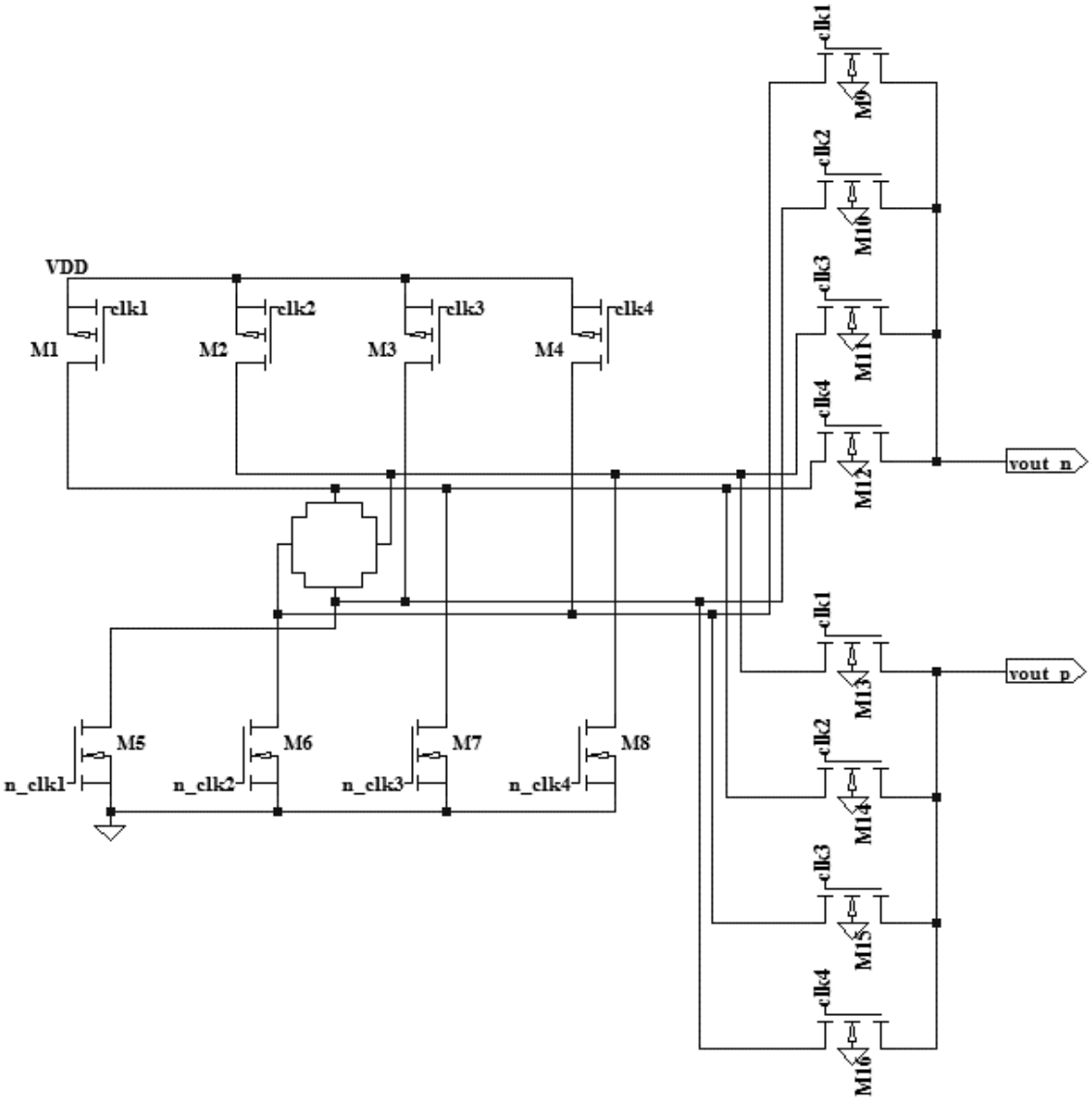

Figure 3.8. Schematics of the biasing circuit with dynamic offset cancellation method implementation.

3.4. Low Offset and Low Noise Amplifier

As the Hall voltage appears differentially between two sensor contacts, an amplifier with differential input is required to strengthen the significant signal, the voltage difference at the sensor output. The amplification of the signal should be low noise and have low offset for high resolution. To decrease the offset and noise of the system, a chopping technique implementation is incorporated to the amplifier. The chopping technique improves the noise and offset cancellation performance of the differential amplifiers, which already have higher immunity to common mode signals than the single ended amplifiers do. A fully differential amplifier with differential input and differential output is proposed to be able to apply chopper modulation and demodulation stages at the input and output of the amplifier, respectively.

Auto-zeroing and chopping techniques are two methods which are used widely in CMOS amplifiers to reduce the offset and noise of the amplifier. Auto-zero method incorporates passive components such as capacitors and switches to sample amplifier offset in one phase and generate an offset-free output voltage in the other phase by subtracting the offset voltage stored on the capacitor in the previous phase. While the offset and 1/f noise can be reduced by the auto-zeroing technique, the input-referred noise increases due to the sampling process. Moreover, a specific operational amplifier architecture can be required for better offset cancellation. However, chopping technique can eliminate input offset of the amplifier and low frequency noise without using passive components and requiring any operational amplifier architecture. The method does not increase the input-inferred noise either since it does not employ a sampling phase. Furthermore, amplifier operation is not interrupted when chopping technique is used as an offset cancellation method.

A differential amplifier with chopping technique implementation is proposed to achieve low offset and low noise amplification since it does not require interruption of the amplifier operation and increase the input-inferred noise. The applied chopping technique modulates the voltage at the input of the amplifier by inverting the roles of amplifier inputs such that the polarity of the signal at the amplifier input is inter-

changed periodically between positive and negative. The chopper modulation does not affect the offset of the amplifier or the low frequency components of the noise. Therefore, the chopping technique effectively modulates the input voltage of the amplifier to the chopping frequency while the sensor offset is left at DC frequency. Discriminating input voltage and amplifier offset in frequency domain before the amplification enables cancellation of the amplifier offset by processing circuits in the back end of the magnetic sensing microsystem.

The chopper modulation is implemented by the switches between the output of the Hall sensor and the amplifier input. They serve two purposes: defining the output terminals of the Hall sensor and modulating the input voltage of the amplifier. As the Hall voltage is made to change polarity in each phase by the eight switches which are controlled by four clock signals (clk1, clk2, clk3, and clk4), it is modulated to the chopping frequency, which is twice the frequency of the clocks in the dynamic offset cancellation method implementation.

A chopper demodulator is added to the output of the amplifier to complete the operation of the chopping technique. As the demodulator changes the roles of the amplifier outputs at the same chopping frequency, the voltage at the amplifier input, which is previously modulated to the same frequency, is brought back to the baseband being strengthened by the amplifier gain. Meanwhile, the chopper demodulator rejects the amplifier offset and noise components which are at smaller frequencies than the chopping frequency to higher frequencies.

Four switches are placed at the output of the amplifier to implement chopper demodulation. They are connected to positive and negative amplifier contacts in groups of two. A clock signal, which is shown in Figure 3.7 as clk5, is used to control the switches. The clock has twice frequency as the one of the other clocks; and, the frequency of the clock is defined as the chopping frequency. The roles of the amplifier outputs are interchanged in consecutive phases by the operation of the demodulation switches between closed and open states. During the high states of the clk5, the amplifier outputs are directly connected to the outputs of front end circuit without

changing the polarity of the output signal. However, the output signal polarity is inverted by interchanging the roles of the amplifier outputs during the low states of the clk5 signal.

The switches in the demodulation stage are implemented with NMOS transistors whose gates are connected to clk5 signal as they form control terminals of the switches. When the transistor is enabled by the high states of the clk5 signal, the voltage at the source of the transistor passes to the drain terminal without any loses. It should also be noted that bodies of the transistors are grounded.

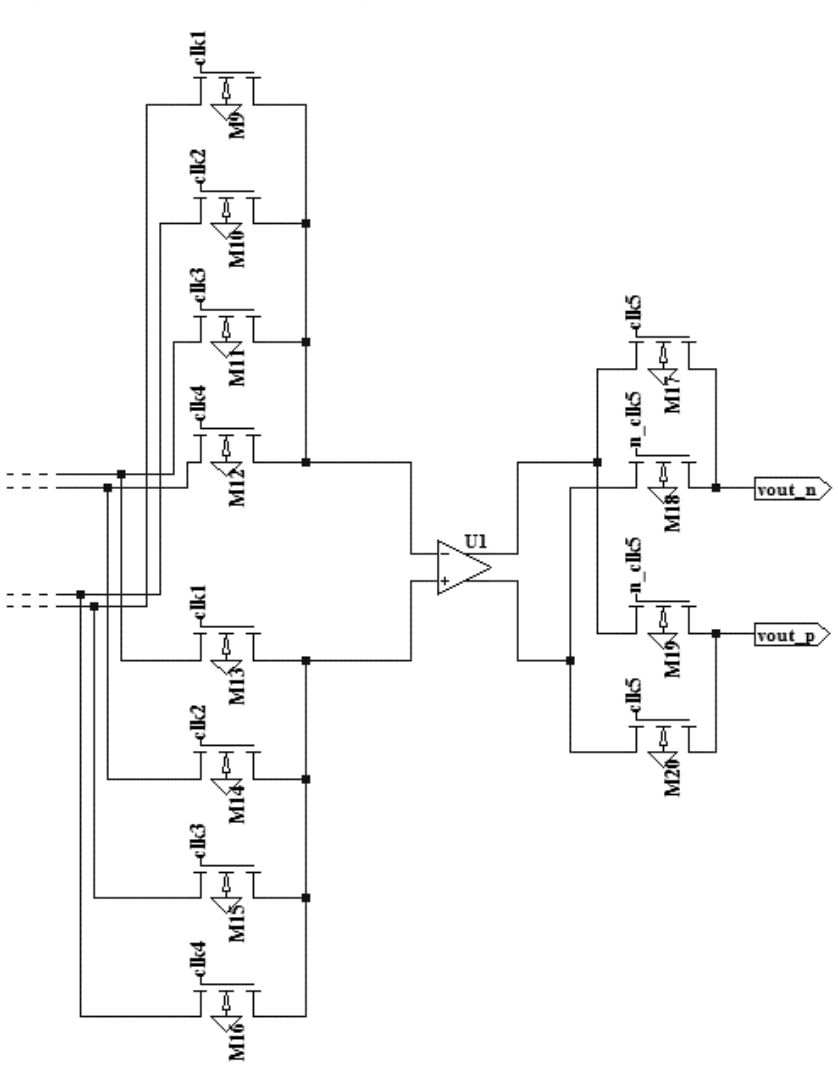

Figure 3.9. Circuit implementation of the chopping technique for achieving low offset and low noise amplifier.

The circuit implementation of the chopping technique in the amplifier is presented in Figure 3.9 as the circuit composes 8 NMOS transistors in the chopper modulation stage and 4 NMOS transistors in the chopper demodulation stage.

The chopping frequency should be sufficiently higher than the flicker noise corner frequency of the Hall sensor and readout electronics including the amplifier. And, it should also be twice the frequency of the clocks used in the dynamic offset cancellation method. Therefore, the frequency should be high enough to reduce 1/f noise of the system whereas its value is limited by the settling time of the Hall sensor contact voltages. Since 1/f noise in the system prevails up to 100 kHz and a clock signal with a frequency of 100 kHz provides enough time for settling of the contact voltages in the biasing circuit, the chopping frequency is set as 200 kHz.

The proposed amplifier with chopping technique implementation suppresses the offset and noise of the Hall sensor, together with the amplifier offset and flicker noise, by rejecting them to higher frequencies. Dynamic offset cancellation method modulates the Hall voltage whereas the polarity of the sensor offset and low frequency noise components are kept constant through all phases as they are shown in Table 3.6. Therefore, the offset and flicker noise of the sensor becomes indistinguishable from the offset and noise of the amplifier to be processed just like the amplifier offset and noise. The chopper demodulation stage at the amplifier output rejects the combined offset and low frequency noise components to higher frequencies whereas the significant Hall signal is brought back to DC frequency as it is presented in Table 3.7.

A low-pass filter can be used in the subsequent stage of the microsystem to remove the offsets and noise of the Hall sensor and front end circuit. The cut-off frequency of the filter should be sufficiently smaller than the chopping frequency to suppress all of the offset and noise components successfully.

The output of the Hall sensor is amplified by using a fully differential amplifier which has differential input and differential output for easing the implementation of chopping technique. The amplifier is designed as a single stage instrumentation am-

Table 3.5. Signal polarities of the Hall voltage and undesired voltage components such as offset and noise before the chopper modulation stage.

	Phase #1	Phase #2	Phase #3	Phase #4
Hall Voltage	+ S	+ S	+ S	+ S
Sensor Offset	-	+	-	+
Amplifier Offset	+	+	+	+
Sensor Noise	+	+	+	+
Amplifier Noise	+	+	+	+

Table 3.6. Signal polarities of the Hall voltage and undesired voltage components such as offset and noise after the chopper modulation stage.

	Phase #1	Phase #2	Phase #3	Phase #4
Hall Voltage	+ S	- S	+ S	- S
Sensor Offset	-	-	-	-
Amplifier Offset	+	+	+	+
Sensor Noise	+	+	+	+
Amplifier Noise	+	+	+	+

Table 3.7. Signal polarities of the Hall voltage and undesired voltage components such as offset and noise after the chopper demodulation stage.

	Phase #1	Phase #2	Phase #3	Phase #4
Hall Voltage	+ S	+ S	+ S	+ S
Sensor Offset	-	+	-	+
Amplifier Offset	+	-	+	-
Sensor Noise	+	-	+	-
Amplifier Noise	+	-	+	-

plifier with two operational amplifiers and a resistive feedback to provide the required amplification factor for increasing the sensor sensitivity. Both of the operational amplifiers are connected in noninverting configuration to amplify the input signal without inverting the signal polarity. Gain of the instrumentation amplifier, shown in Figure 3.10, is defined by the resistances in the resistive feedback as,

$$A_1 = \frac{2R_2 + R_1}{R_1} \tag{3.11}$$

where A_1 denotes the gain of the closed loop amplifier and the resistances of R21 and R22 are equal to R_2 while the one of R1 is R_1.

The gain of the amplifier is set considering the risk of output clamping of the operational amplifiers in the instrumentation amplifier. Although the Hall voltage at the sensor output is very small, the sensor offset, especially the one caused by shear stress, can be significantly high, restricting the amplifier gain. The gain of the instrumentation amplifier is defined such that the amplified Hall voltage with offset caused by shear stress does not cause clamping of any operational amplifier. Therefore, the gain of the instrumentation amplifier is set to 101 using feedback resistors whose resistances are 5 kΩ and 250 kΩ.

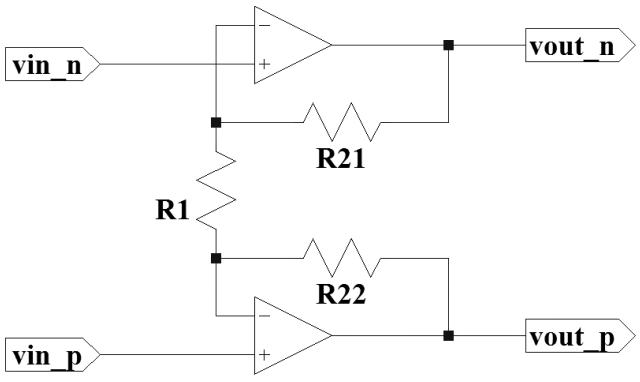

Figure 3.10. Single stage instrumentation amplifier with two operational amplifiers and a resistive feedback.

The specifications for the operational amplifiers in the instrumentation amplifier are determined by analyzing the performance of dynamic offset cancellation and chopping method realizations in the front end circuits which include ideal operational amplifiers. The open loop gains and gain bandwidth products of the ideal operational amplifiers are set to several values and the performance of the offset and noise cancellation methods are tested. Operational amplifiers with a gain of 60 dB and a gain bandwidth product of 100 MHz are noticed to cancel offsets caused by all types of sources and amplifier offset successfully when they are used in the instrumentation amplifier.

Operational amplifiers are implemented using folded cascode topology, which is shown in Figure 3.11, to achieve the determined specifications. M1 and M2 form the input differential pair which provides the transconductance gain of the amplifier whereas M3 and M4 are PMOS cascode transistors. Cascode current mirror formed by M5 – M8 provides high output resistance just like the cascode structure formed by M1 – M4 does.

The operational amplifier is designed to provide an extended input common-mode range since the common-mode voltage at the sensor output can change with mechanical stress as it causes the resistance of the sensor change significantly. The transistors in the input differential pair of the folded cascode operational amplifier are biased by a current of $I_1/2$ while the cascode transistors operate at I_2–$I_1/2$. I_2 is made to be greater than I_1 by 20% to minimize the distortions of the output in response to large differential input signals. Voltage at the node Vbias is set carefully to keep M1 – M4, M9, and M10 in saturation even if the offset of the sensor changes the voltage at the amplifier input and output significantly. The biases of the folded cascode operational amplifier are given in Table 3.8.

The sizes of the transistors are set to keep the overdrive voltages of the NMOS and PMOS transistors around 0.1 V as low overdrive voltages increase the common mode input and output ranges, and increases the amplifier gain. Moreover, small overdrive voltages of the cascode current mirror transistors also makes the common mode voltage

Table 3.8. Biases of the folded cascode operational amplifier design.

I1	48 uA
I2	40 uA
Vbias	0.56 V

of the differential amplifier output small. Although the use of low overdrive voltage degrades the frequency response of the amplifier, the gain bandwidth product of the designed amplifier is higher than the needed one.

The designed folded cascode amplifier has an open loop gain of 66.5 dB and unity gain frequency of the unloaded amplifier is 610 MHz while its 3-dB frequency is 662 kHz. The input common mode range of the amplifier is between 0.37 V and 1.34 V whereas the amplifier output has a narrower range between 0.45 V and 0.96 V.

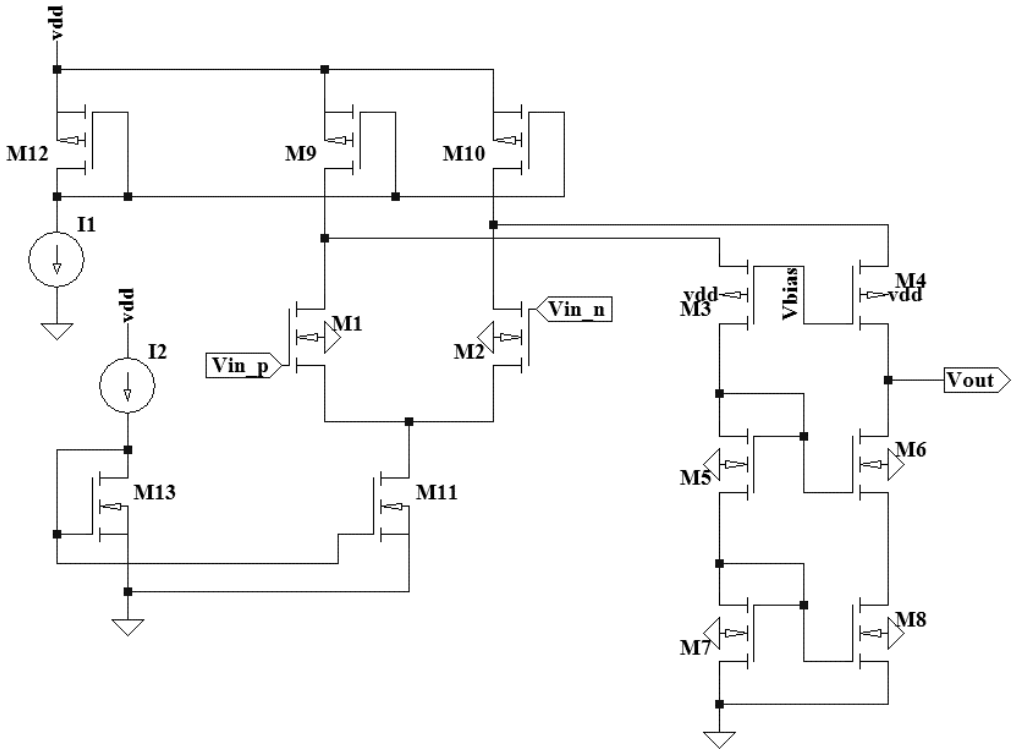

Figure 3.11. Operational amplifier with folded cascode topology.

3.5. Conclusion

The proposed front end circuit in the magnetic sensing microsystem is designed to increase the sensitivity of the sensor while simultaneously reducing the sensor offsets caused by imperfections and mechanical stress, the amplifier offset, and the 1/f noise generated by the sensor and electronics circuits including the switches and amplifier. The front end circuit proposal implements dynamic offset cancellation method by including 8 switches for biasing the Hall sensor across 4 different sensor contact pairs and 8 more switches for discriminating Hall voltage and sensor offset in frequency domain to enable the rejection of the sensor offset. The gain factor for increasing the small Hall sensor sensitivity is provided by the fully differential instrumentation amplifier with 2 operational amplifiers and a resistive feedback. The amplifier is equipped with chopping technique to achieve low offset and low noise figures. The chopper modulation stage is implemented by 8 switches which also discriminate Hall voltage and sensor offset; and, the chopper demodulation realization composes 4 additional switches in the output of the amplifier to reject the undesired voltage components such as offset and noise of the sensor and readout electronics. The full schematics of the front end circuit is presented in Figure 3.12.

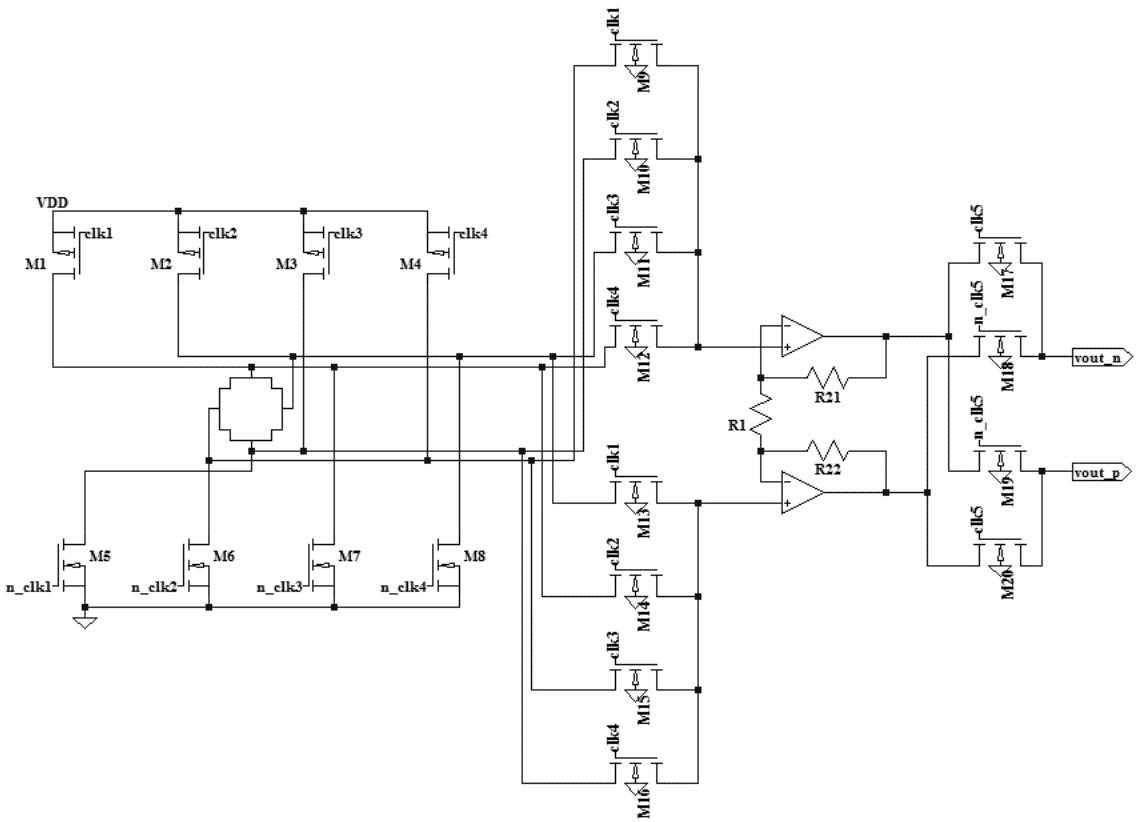

Figure 3.12. Proposed low offset and low noise front end circuit architecture in the magnetic sensing microsystem.

4. SIMULATION RESULTS

4.1. Compact Cross-Shaped Hall Sensor Model

Table 4.1 presents the voltages at the outputs of the Hall Effect sensor as a function of the applied perpendicular magnetic field. The equations are formed experimentally using the compact Hall sensor model, which incorporates nonlinearity, temperature drift effect, and geometrical effect, as the magnetic field ranges from 0 to 20 mT. The effects of offsets due to fabrication dispersion and mechanical stress are given separately by forming a different equation for each offset type. The effect of nonlinearity presents itself as different sensitivities of sensor output contacts which are seen in the equations at the forth row of the table. The difference between the sensitivities of two output contacts causes a weak offset as it is the case for the fabrication mismatch perpendicular to the biasing direction.

4.2. Low Offset and Low Noise Front End Circuit Design

4.2.1. Simulation of the Front End Circuit

The performance of the dynamic offset cancellation method and chopping technique in cancelling the sensor offsets due to fabrication dispersion and mechanical stress and offset of the amplifier is presented in Table 4.2. The table shows the differential signal at the output of the front end circuit for each of the four phases of dynamic offset cancellation method; and P1, P2, P3, and P4 denote phase #1, phase #2, phase #3, and phase #4, respectively. The performance of the cancellation methods for different offset sources are analyzed in different columns of the table. Amplified Hall voltage is seen to be almost constant in all of the phases of the cancellation scheme. However, the polarity of the offset voltage changes, as it is expected, in each consecutive phase: the offset is added with negative polarity to the Hall voltage in phase #1 and #3 whereas it is added as a signal with positive polarity in the remaining phases. The addition of the outputs of all phases cancels the offsets in the sensor response and extracts the

Table 4.1. Voltages at the Hall sensor output as a function of the applied magnetic field due to different offset sources.

Vbias(1, 3) = 1V	V(4)	V(2)
deltaR1	0.012235x + 0.4955	-0.012235x + 0.5045
deltaR2	0.012235x + 0.4953	-0.012235x + 0.4953
deltaR3	0.01224x + 0.5	-0.012235x + 0.5
deltaR4	0.01222x + 0.5	-0.01222x + 0.5
Vbias(2, 4) = 1V	V(1)	V(3)
deltaR1	0.012235x + 0.5045	-0.012235x + 0.4955
deltaR2	0.01224x + 0.5	-0.012235x + 0.5
deltaR3	0.012235x + 0.5047	-0.012235x + 0.5047
deltaR4	0.01225x + 0.5	-0.01225x + 0.5
Vbias(3, 1) = 1V	V(2)	V(4)
deltaR1	0.012235x + 0.4955	-0.012235x + 0.5045
deltaR2	0.012235x + 0.5047	-0.012235x + 0.5047
deltaR3	0.01224x + 0.5	-0.012235x + 0.5
deltaR4	0.01222x + 0.5	-0.01222x + 0.5
Vbias(4, 2) = 1V	V(3)	V(1)
deltaR1	0.012235x + 0.5045	-0.012235x + 0.4955
deltaR2	0.01224x + 0.5	-0.012235x + 0.5
deltaR3	0.012235x + 0.4953	-0.012235x + 0.4953
deltaR4	0.01225x + 0.5	-0.01225x + 0.5

significant signal, amplified Hall voltage.

Table 4.2. Differential signal at the output of the front end circuit for each phase of 4-phase dynamic offset cancellation method.

	Ideal	$\delta R1$	$\delta R2$	$\delta R3$	$\delta R4$	All $\delta's$	+Amp.	-Amp.
P1	0.0262	-0.0215	0.0262	0.0262	0.0262	-0.0215	0.1296	-0.0773
P2	0.0263	0.074	0.0263	0.0263	0.0263	0.0739	-0.0772	0.1297
P3	0.0262	-0.0215	0.0262	0.0262	0.0262	-0.0215	0.1296	-0.0773
P4	0.0263	0.074	0.0263	0.0263	0.0263	0.074	-0.0772	0.1297
TOTAL	0.105	0.1049	0.105	0.105	0.105	0.105	0.1048	0.1048

A perfect offset cancellation is not possible when nonidealities are involved in the circuits. Although they are tried to be minimized, there will always be a residual offset due to, mainly, Hall sensor and amplifier nonlinearity and combined effects of different offset sources. Table 4.3 presents the errors at the output of the front end circuit for different offset types. Output errors are defined with respect to the ideal value which is calculated as the multiplication of the sensitivity of the Hall plate, applied perpendicular magnetic field of 20 mT, and the gain of the instrumentation amplifier. The mean of the output errors for different offset types is 0.00104 while their variance is 0.00000023. The residual offset in the worst case is 0.168 mV, corresponding to an input inferred offset of 1.62 μV.

Table 4.3. Output errors in cancelling offset caused by different offset sources.

Ideal	$\delta R1$	$\delta R2$	$\delta R3$	$\delta R4$	All $\delta's$	+Amp.	-Amp.
-0.00087	0.00018	-0.00089	-0.00085	-0.00089	-0.00147	0.00154	0.0016

Figure 4.1 presents front end circuit transient simulation which includes eight phases. A Hall plate with offsets of all types is used in the front end to demonstrate the transient behavior of the dynamic offset cancellation and chopping technique realizations. V(1), V(2), V(3), and V(4) are the voltages at the contacts of the Hall

sensor. The voltages at the outputs of the front end circuit, V(vout_p) and V(vout_n), are presented together with the differential signal at the output, V(vout_p, vout_n). Although transient spikes are minimized by using nonoverlapping clocks, they are still visible at the transitions.

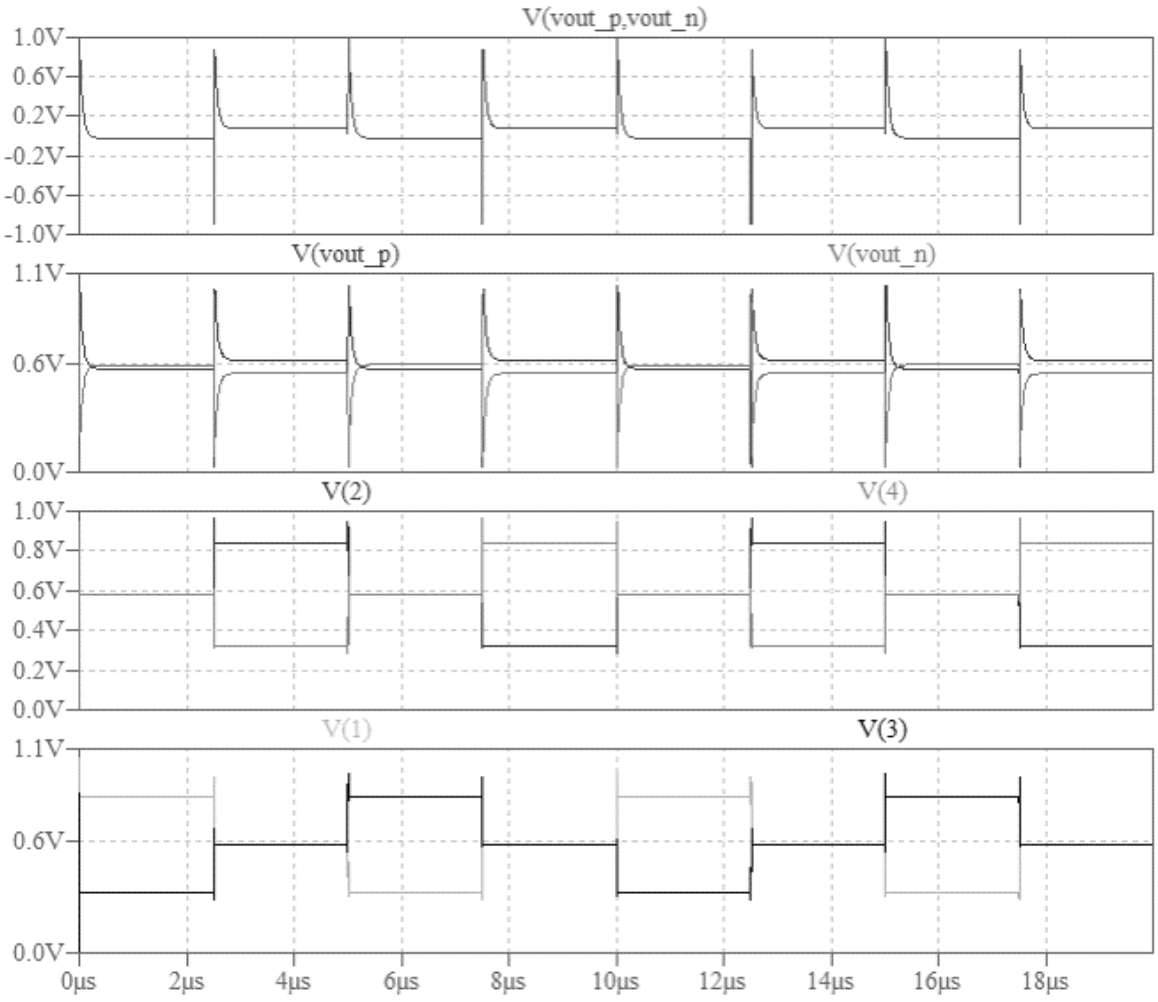

Figure 4.1. Transient simulation of the front end circuit and Hall sensor with offsets of all types.

4.2.2. Noise Analysis

Noise density of the proposed microsystem is shown in Figure 4.2. As it is seen in Figure 4.2, noise of the proposed microsystem at low frequencies is suppressed and pushed to higher frequencies. A low-pass filter with a corner frequency of 1 kHz can be used to reject the noise of the sensor and readout electronics which are pushed to

higher frequencies. Root-Mean-Square (RMS) value of noise voltage of the proposed microsystem in the bandwidth of 1 Hz – 1 kHz is given as 167 μV. The calculated RMS noise voltage corresponds to a resolution of 31.75 μT. Increasing the corner frequency of the low-pass filter improves the resolution of the microsystem as it is presented for different corner frequencies in Table 4.4.

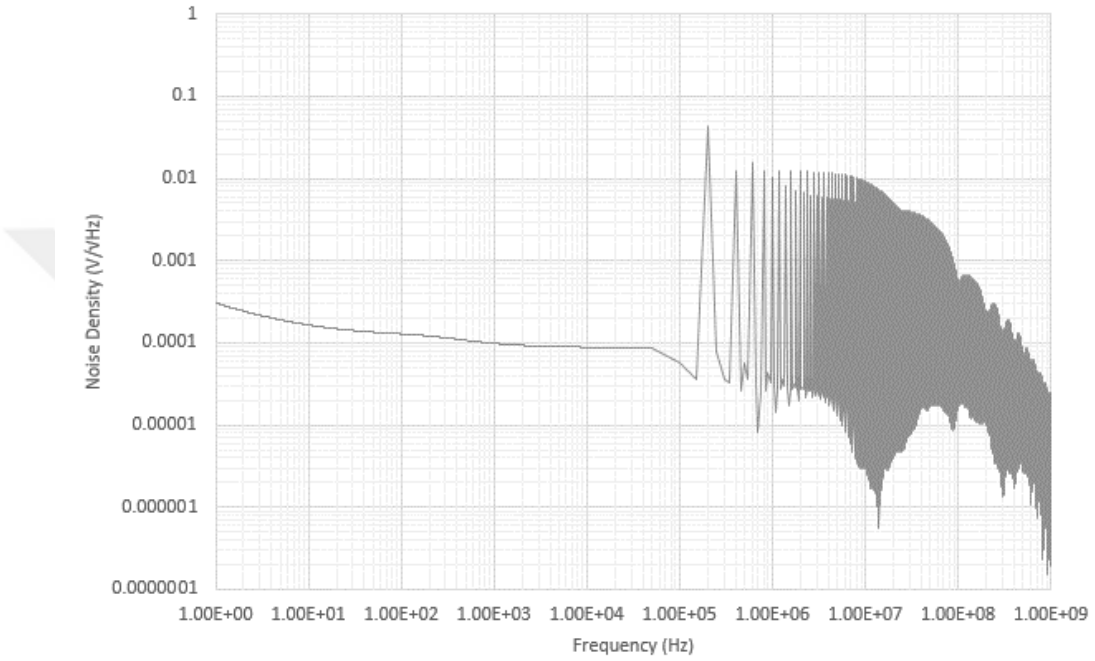

Figure 4.2. Noise density of the proposed microsystem.

Table 4.4. RMS noise voltages for low-pass filters with different corner frequencies.

Corner Frequency	Noise Voltage (RMS)	Resolution
100 Hz	188 μV	35.72 μT
1 kHz	167 μV	31.75 μT
10 kHz	151 μV	28.85 μT
100 kHz	144 μV	27.37 μT

4.2.3. Simulation of the Instrumentation Amplifier

The frequency response of the instrumentation amplifier is shown in Figure 4.3. As the resistances in the resistive feedback define the gain of the instrumentation amplifier, it is shown in the figure as 40.3 dB. The amplifier has a bandwidth of 13.90 MHz as it is defined by the cutoff frequency; and the unity gain frequency is 608.14 MHz.

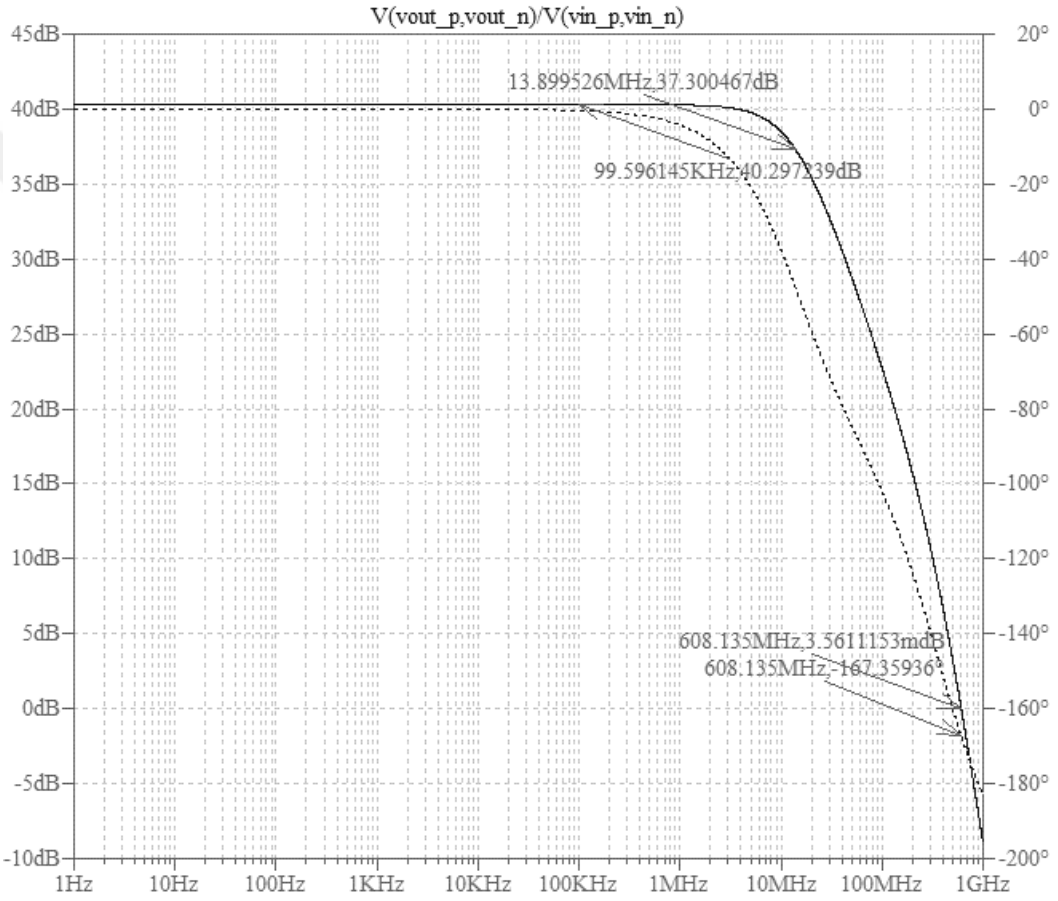

Figure 4.3. Frequency response of the instrumentation amplifier.

Figure 4.4 presents the frequency response of the designed folded cascode operational amplifier, which has a gain of 66.5 dB and a unity gain frequency of 232.81 MHz when the operational amplifier is loaded with a 0.2 pF capacitor. The phase margin of the unloaded folded cascode operational amplifier is 14.88 degrees; nevertheless, the low phase margin increases to 45.92 degree by loading output of the amplifier with a

capacitive load of 0.2 pF. It should also be noted that the high open loop gain of the amplifier increases the linearity of the instrumentation amplifier.

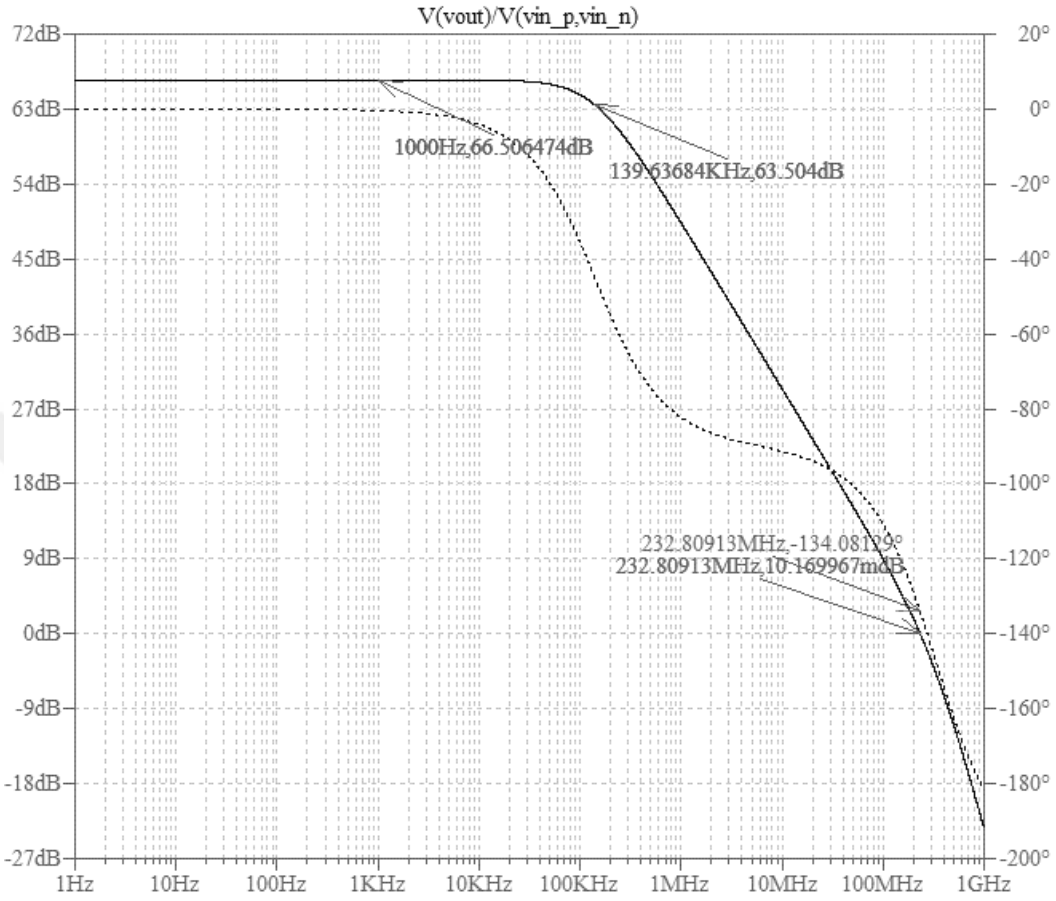

Figure 4.4. Frequency response of the folded cascode operational amplifier.

5. CONCLUSION

The presented compact cross-shaped Hall sensor model accurately models the behavior of the Hall Effect sensor in response to applied perpendicular magnetic field without producing long simulation durations. The model incorporates nonlinearity, temperature drift effect, offsets due to fabrication dispersion and mechanical stress, geometrical effect, and frequency response; however, magneto-resistance effect and carrier scattering effect are not included in the model since strong magnetic fields will not be used in the magnetic sensing microsystem. Lateral diffusion effect is also neglected considering the dimensions of the Hall plate in the microsystem.

The proposed front end circuit in the magnetic sensing microsystem, which is designed using UMC 130 nm CMOS technology, maximizes the precision of the magnetic field measurements by minimizing the limitations of the offset and noise of the sensor and readout circuit on the sensor performance. The front end circuit increases the sensitivity of the sensor with an amplification factor equal to the gain of the instrumentation amplifier. Dynamic offset cancellation method is implemented successfully in the biasing circuit for cancelling the sensor offset caused by fabrication imperfections and mechanical stress. The residual offset in the case where all of the sources to cause sensor offset exists is 40 μV with respect to the case with ideal Hall plate, corresponding to an input-inferred residual offset of 7.62 μT, which is quite low than the residual offsets in the state of the art.

The instrumentation amplifier is coupled with the chopping technique realization for reducing the offset of the amplifier and rejecting the undesired voltage components such as offset and 1/f noise of the sensor and readout electronics. With the use of chopping technique in the amplifier, an offset of 1 mV at the input of the instrumentation amplifier is successfully suppressed to an input-inferred offset of 1.62 μV. Moreover, the noise density of the microsystem in the bandwidth of 1 Hz – 1 kHz corresponds to an RMS noise voltage of 167 μV at the microsystem output. A low-pass filter which can be employed in the back end circuit of the magnetic sensing microsystem with a

corner frequency of 1 kHz makes the resolution of the microsystem as low as 31.75 μT. The proposed resolution is comparable to the one presented in the state of the art studies.

Table 5.1 presents the simulated characteristics of the proposed front end circuit with 4-phase dynamic offset cancellation implementation and chopping technique realization.

Table 5.1. Simulated characteristics of the proposed front end circuit.

Specification	**Value**	**Unit**
Supply Voltage	1.2	V
Absolute Sensitivity	5.25	V/T
Sensor Gain	0.05	V/T
Amplifier Gain	103.5	-
Equivalent Input Inferred Offset	7.62	μT
Noise (RMS Value)	167	μV
Bandwidth	1	kHz
Resolution	31.75	μT
Measurement Range	0 - 20	mT

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