# NEW ANALOG FILTER DESIGN POSSIBILITIES WITH MOSFET-C TECHNIQUE

by

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# ABSTRACT

## NEW ANALOG FILTER DESIGN POSSIBILITIES WITH MOSFET-C TECHNIQUE

There are many analog filter examples available in the literature to address various needs, such as certain bandwidth, transfer function, and low power consumption. To meet such requirements, operational amplifier based analog filters are widely used in the last several decades and they are still popular. However, today's applications expect analog design engineers to achieve low power consumption and small chip areas. Therefore, much research has been done on MOS based circuits because of their easy IC implementable features. There are some designs, called as MOS-only, primarily relying on utilizing transconductance $g_m$ and gate-to-source capacitance $C_{gs}$ of the MOSFET instead of external passive components. Even though MOS-only design approach has some attractive features, width and length of transistors must be set in accordance with strict rules. We have included some on-chip capacitors, such that the effect of non-ideal MOS factors on filter parameters are moderated to some extent.

In this thesis, we have designed novel current mode agile, transimpedance, transconductance, and voltage mode analog filters. Besides that, to demonstrate circuit operation we have chosen some of them and biased properly. Since we have provided transfer functions by taking non-ideal MOS parameters into account, we are able to predict circuit behaviour under electronic adjustments. By relying on this, we have tuned our designs under different bias possibilities without violating saturation conditions. Such methodology, of course, broadens the application range of designs. Additionally, how the biased designs behave under various environmental conditions is examined by introducing temperature effects and possible implementation errors.

# ÖZET

## MOSFET-C YÖNTEMİYLE YENİ ANALOG SÜZGEÇ TASARIM İMKANLARI

Mevcut literatürde, belli bant genişliği, aktarım fonksiyonu ve düşük güç tüketimi ihtiyaçlarını karşılayan birçok analog süzgeç örneği vardır. Bu ihtiyaçları gidermek amacıyla, hala popüler olan işlemsel kuvvetlendirici tabanlı analog süzgeçler geçtiğimiz birkaç on yılda geniş çapta kullanılmıştır. Fakat, günümüzün uygulamaları analog tasarım mühendislerinden düşük güç tüketimi ve az çip alanı kullanımını beklemektedir. Bu yüzden, MOS-tabanlı devrelerin kolay tümleşik devre üretimine uygun özellikleri olması sebebiyle, bu devreler üstünde birçok araştırma yapılmıştır. Salt-MOS olarak adlandırılan tasarımlar temel olarak geçiş iletkenliğini ($g_m$) ve kapı-kaynak kapasitesini ($C_{gs}$) harici pasif bileşenler yerine kullanmaya dayalıdır. Salt-MOS tasarım yaklaşımı ilgi çekici özelliklere sahip olsa da, transistörün genişlik ve boy parametrelerinin katı kurallara göre ayarlanması gerekir. MOSFET'in ideal olmayan faktörlerinin etkisinin bir dereceye kadar hafifletilmesi amacıyla bazı harici kapasiteler ekledik.

Bu tezde, akım modlu atik, geçiş dirençli, geçiş iletkenlikli ve voltaj modlu yeni süzgeçler tasarlandı. Bunun yanında, devre işleyişini ispat etmek amacıyla bu tasarımların bazılarını seçip uygun şekilde kutupladık. Transfer fonksiyonlarını MOSFET'lerin ideal olmayan faktörlerini göz önüne alarak sağladığımız için, elektronik uyumlandırma durumunda devre tutumlarını öngörebiliyoruz. Buna dayanarak, tüm devreleri farklı kutuplandırma koşulları uygulayarak, doyum durumunu bozmaksızın, uyumlandırabildik. Bu yöntem tasarımların uygulama sahasını elbette genişletir. Ek olarak, devrelerin değişken çevresel koşullar altında nasıl davrandığı sıcaklık etkileri ve olası üretim hataları uygulanarak incelenmiştir.

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# LIST OF SYMBOLS

| | |
|---|---|
| $C_{ox}$ | The gate oxide capacitance of a MOSFET transistor per unit area |
| $C_{db}$ | Drain-to-bulk capacitance |
| $C_{gs}$ | Gate-to-source capacitance |
| $C_{gd}$ | Gate-to-drain capacitance |
| $C_{ov}$ | Overlapping capacitance |
| $C_{sb}$ | Source-to-bulk capacitance |
| $f_0$ | Central frequency |
| $f_c$ | Cut-off frequency |
| $f_{L3dB}$ | Low cut-off frequency |
| $f_{H3dB}$ | High cut-off frequency |
| $g_{ds}$ | Output conductance of MOSFET |
| $g_m$ | Transconductance |
| $I_D$ | DC Drain current of a MOSFET transistor |
| $I_{IN}$ | DC input current |
| $i_{IN}$ | Combination of small signal and DC input current |
| $i_{in}$ | Small signal input current |
| L | Length of a MOSFET transistor |
| $L_{ov}$ | Overlapping length between gate and source |
| Q | Quality factor of a biquad filter |
| $r_o$ | Output resistance of transistor |
| $V_B$ | Bulk (substrate) potential |
| $v_{bs}$ | Small signal Bulk-source voltage |
| $V_{BS}$ | DC Bulk-source voltage of MOSFET |
| $V_D$ | DC Drain voltage of MOSFET |
| $V_{DS}$ | DC Drain-source voltage of MOSFET |
| $V_G$ | DC Gate voltage of MOSFET |
| $v_{gs}$ | Small signal Gate-source voltage |

| | |
|---|---|
| $V_{GS}$ | DC Gate-source voltage of MOSFET |
| $v_{in}$ | Small signal input voltage |
| $V_{OV}$ | Overdrive voltage |
| $V_S$ | Source voltage of MOSFET |
| $V_{Thi}$ | The threshold voltage of the MOSFET corresponding to a $V_B$ bulk potential, where $i$=N for NMOS and $i$=P for PMOS |
| $V_T$ | Thermal voltage |
| W | Width of a MOSFET transistor |
| $\lambda$ | Channel-length Modulation Parameter |
| $\omega_0$ | Central angular frequency |

# LIST OF ACRONYMS/ABBREVIATIONS

| | |
|---|---|
| BP(F) | Band-pass (Filter) |
| FAF | Frequency Agile Filter |
| GPS | Global Positioning System |
| HP(F) | High-pass (Filter) |
| IC | Integrated Circuit |
| LP(F) | Low-pass (Filter) |
| MOS | Metal-Oxide Semiconductor |
| MOSFET | Metal oxide semiconductor field effect transistor |
| MST | Multi Standard Transceivers |
| NMOS | N-type Metal-Oxide Semiconductor |
| OPAMP | Operational Amplifier |
| OTA | Operational Transconductance Amplifier |
| PMOS | P-type Metal-Oxide Semiconductor |
| THD | Total Harmonic Distortion |
| VCCS | Voltage Controlled Current Source |

# 1. INTRODUCTION

Analog filters consisting of active components play an important role in the development of electronics. Especially in the field of telecommunications, these filters have been an integral part in a lot of technological breakthroughs and have been the source of enormous benefit for signal processing studies. There are many analog filter designs based on active elements, such as OPAMPs, OTAs, by utilizing standard cell libraries. Even if this approach makes design procedure much easier for automatization, the resulting design contains more transistors than required to fulfill filter specifications. To issue this problem, MOS-based design method is pursued, so it is possible to obtain simpler and more efficient filters. However, such design methodology requires somewhat strict rules by setting W/L ratios for MOSFETs. In our designs, we have included on-chip capacitances to alleviate the effect of internal MOS capacitances of $C_{gs}$ and $C_{gd}$. Additionally, transistor transconductances of $g_m$ and $g_{ds}$ are used instead of passive elements to obtain resistive dimension in the saturation region. Hence electronic tunability is achieved, which is a very important feature of IC analog filters.

Since MOSFET operation is highly based on device geometry, NMOS structural perspective view is presented in Figure 1.1, which can be also validated for PMOS with appropriate doping. An NMOS transistor has a p-type substrate, or body (B), made by single-crystal silicon. N-type doped fields are located above the substrate. These fields bring out the source terminal (S) and drain terminal (D). Moreover, silicon dioxide is deployed as a very thin layer of insulator between gate (G) and body. As a result, four different main terminals are created. To electronically control the device, metal contacts are deposited on the surface of these four terminals.

By applying positive voltage on the gate, electrons from the n+ typed source and drain are attracted. When an adequate number of electrons are accumulated between substrate and gate regions, a channel is induced. The channel connects drain

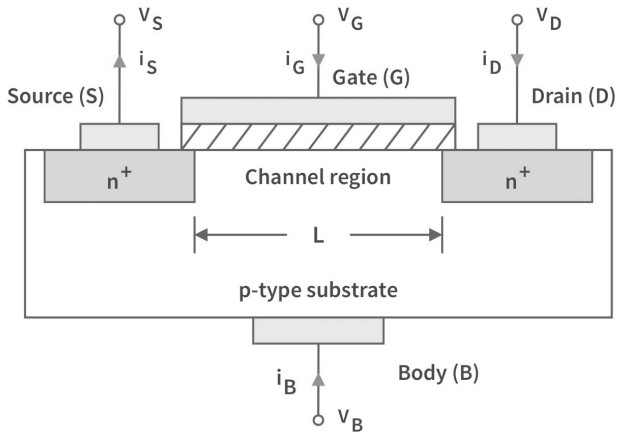


Figure 1.1. Physical structure of the NMOS transistor from cross view.

and source regions by allowing current flow in the longitudinal direction from drain to source. Thus n-channel MOSFET is obtained. Note that, the value of $V_{GS}$ at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted as $V_{ThN}$.

As a starting point for MOS-based design in our study, all of transistors must stay in the saturation region to fit into proposed small signal model, as it is depicted in Figure 1.2. For n-type MOSFET, following conditions must be kept:

(i) $V_{GS} > V_{ThN}$
(ii) $V_{DS} > V_{GS} - V_{ThN}$

Similar to NMOS, PMOS saturation condition must satisfy following ones:

(i) $V_{SG} > -V_{ThP}$
(ii) $V_{SD} > V_{SG} + V_{ThP}$

As Equation 1.1 suggests $I_D$ is independent of $V_{DS}$. However, near the drain, the gate and drain collectively set the electric field pattern. But, in practice, increasing $V_{DS}$ beyond $V_{OV}$ does affect the channel somewhat. Specifically, as $V_{DS}$ is increased,

the channel pinch-off point is moved slightly away from the drain, toward the source.

$$I_D = \mu_n C_{ox}(\frac{W}{2L})(V_{GS} - V_{ThN})^2 \tag{1.1}$$

Note that the voltage across the channel remains constant at $V_{OV}$, and the additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons by making easy to reach drain and clear them across the depletion region into the drain. Note, however, that (with depletion-layer widening) the channel length is in effect reduced, a phenomenon known as channel-length modulation [1]. Now, since $I_D$ is inversely proportional to the channel length, $I_D$ increases with $V_{DS}$. Equation 1.2 is a modified version of Equation 1.1

$$I_D = \mu_n C_{ox}(\frac{W}{2L})(V_{GS} - V_{ThN})^2(1 + \lambda V_{DS}) \tag{1.2}$$

In the saturation region, MOSFET behaves as a VCCS in terms of small signal $v_{gs}$. In Figure 1.2, small-signal equivalent of MOS transistors is provided. Note that such model is valid for both NMOS and PMOS, hence it is possible to redesign a MOS-only or MOSFET-C filter circuitry by setting proper bias conditions. Additionally, a designer may eliminate any bulk-source factor by applying direct connection between them. We have also followed this routine in our designs, throughout the thesis. To construct a small-signal model for MOSFET, we have to express the relationship between $I_D$, $V_{GS}$, and $V_{DS}$.

$$g_m = \mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_{Th})(1 + \lambda V_{DS}) \tag{1.3}$$

$$g_{ds} = \frac{1}{r_o} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GSconst.}} = \lambda \mu_n C_{ox}(\frac{W}{2L})(V_{GS} - V_{Th})^2 \tag{1.4}$$

By omitting $\lambda$ for quick design, it is possible to predict relationship between $I_D$, $V_{OV}$, and W, where $V_{OV}$ is defined as overdrive voltage and equals $|V_{GS} - V_T|$ .

$$g_m \approx \frac{2I_D}{V_{OV}} = \sqrt{2\mu_n C_{ox}}\sqrt{\frac{W}{L}}\sqrt{I_D} \tag{1.5}$$

In addition to transconductance parameters, internal MOS capacitances of $C_{gs}$ and $C_{gd}$, have an effect on the frequency response of filter. Actually, there are two additional internal capacitances as $C_{sb}$ and $C_{db}$, which are the depletion capacitances of the pn junctions formed by the source region and the substrate, and the drain region and the substrate, respectively. We have neglected depletion capacitances. In addition to gate and depletion capacitances, there is an overlapping capacitance between gate and drain, expressed as $C_{ov} = WL_{ov}C_{ox}$ leading to $C_{ov}$ capacitance.

For the gate-to-drain capacitance, we note that the channel pinch-off at the drain end causes $C_{gd}$ to consist entirely of the overlap component $C_{ov}$, hence it is possible to accept these two capacitances are equal. By relying on this fact, $C_{gs}$ can be calculated as Equation 1.6. $C_{ox}$ is oxide capacitance and dependent on optical and electrical property, taken as 8.784e-03 F/m$^2$ for 0.18 $\mu$m process [2]. Besides that $C_{gd}$ can be calculated as Equation 1.7, where $C_{gd0}$ is defined as gate-drain overlap capacitance and provided by technology as 7.9e-10 F/m, 6.34e-10 F/m for NMOS and PMOS respectively. Figure 1.2 visualizes all capacitances on saturated NMOS device.

$$C_{gs} = \frac{2}{3}WLC_{ox} + C_{ov} \tag{1.6}$$

$$C_{gd} = C_{ov} = C_{gd0}W \tag{1.7}$$

After giving insight on and providing some required MOSFET basics, it is helpful to depict all of them on a simple model as shown in Figure 1.2. This figure is an illustra-

tion of how MOSFET behaves as a VCCS. Note that all of equations accommodated in this part is valid for long-channel devices. Otherwise velocity saturation effects should be taken into account. To moderate such factors, we have set all transistor length as 0.9 $\mu$m. The rest of thesis is organized into four different chapters, discussing current mode, transimpedance, transadmittance, and voltage mode filters. Each chapter starts with a brief introduction on associated part.

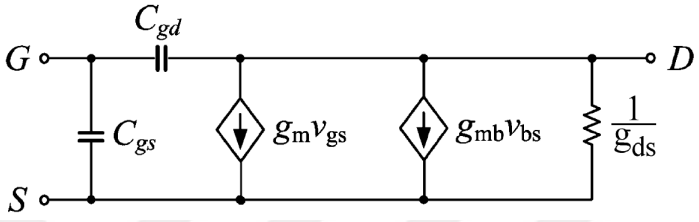


Figure 1.2. MOSFET small signal model.

# 2. MOSFET-C CURRENT MODE DUAL OUTPUT FILTER WITH AN AGILE FILTER APPLICATION

In this chapter, a dual output current mode biquad filter with band-pass and low-pass outputs and a design procedure to construct the filter is proposed. Starting from an initial core circuit the complete design process is given as a step by step procedure. The resistorless MOS-only type initial core consists of two transistors only. The presented final circuit enjoys having two grounded capacitors and the circuit's operation is also shown in an agile filter application.

## 2.1. Introduction

The standard design approach of analog filters employs active building blocks such as operational transconductance amplifiers (OTA), OP-AMPs, current conveyors and passive elements such as resistors and capacitors to implement the desired filter transfer function. However, these active elements, in general, include a large number of transistors, and this in turn increases power consumption and circuit complexity [3,4]. As an alternative method, numerous circuits are proposed recently in the literature [5–12] using only MOS transistors. Instead of passive resistors, $g_m$ of MOSFETs are used in these circuits. This provides circuit implementation with fewer transistors and eliminates the need for external passive resistors. In this chapter, we present a procedure starting from a two transistor MOS-only core circuit designed for low-pass (LP) and band-pass (BP) dual outputs implementing a biquad current mode filter function. This provides an alternative method to the classical active block-based design. In the proposed design, MOSFETs operate in saturation mode and transconductances of transistors are used with the capacitors to form the necessary coefficients in the standard transfer function. Theoretical analysis is verified with simulation results. In the simulations, TSMC 0.18 $\mu$m n-well process parameters are used in LT Spice simulator program. Furthermore, an agile filter application is presented to prove the advantage of the presented circuit.

## 2.2. The Design Procedure

The step-by-step design procedure is as follows: As the initial step, we start with the functional core that can give LP and BP outputs. Then we add additional circuitry to pick up the drain current to be used as the output. Our final aim is to design an agile filter based on the philosophy suggested by [13]. The proposed initial second-order LP-BP dual output filter core circuit is shown in Figure 2.1. Note the simplicity of

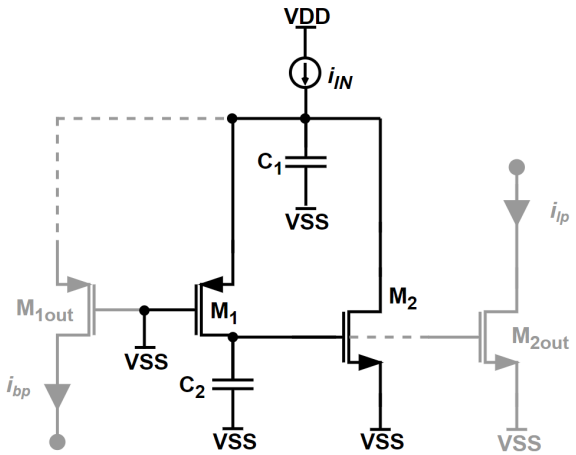


Figure 2.1. The proposed LP-BP dual output filter core circuit with output transistors.

the circuit that has only two in terms of ac non-grounded nodes which is a minimum number for a second order circuit. Both of these nodes are connected to the ground by filter capacitors therefore, any additional parasitic capacitances at these nodes to the ground can be accommodated in them. This circuit has another advantage of giving distortionless output at very low frequencies which will be explained as follows. A closer look to the circuit reveals that at these frequencies where the capacitors are practically open circuited the input current has only one path which is the drain of $M_2$ and this is the output signal of the filter at the same time. In other words the input signal is identical to the output signal. However, the core design is enriched by adding output transistors ($M_{1out}$ and $M_{2out}$) to pick the output current. Therefore, current mirroring will be the only source for distortion. Since all transistors must be

kept in the saturation region, the designer must provide required voltage conditions for the output current nodes, drains of both $M_{1out}$ and $M_{2out}$. The related transfer functions considering the simplified small signal AC model of the MOS transistor and the capacitors of the presented circuit are given in Equation 2.1 and 2.2. Note that these transfer functions are obtained for the design without output transistors. This configuration is denoted as the core filter throughout this thesis.

$$TF_{BP} = \frac{i_{d1}}{i_{in}} = \frac{C_2 g_{m1} g_{m1} s}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{2.1}$$

$$TF_{LP} = \frac{i_{d2}}{i_{in}} = \frac{g_{m1} g_{m2}}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{2.2}$$

For a biquad filter $\omega_0$ and $Q$ are important parameters for design and application. The general equations for transfer functions of $TF_{BP}$ (s), $TF_{LP}$ (s), and $TF_{HP}$ (s) are in the form of ones given in Equation 2.3, 2.4, and 2.5, where $a$, $a^{'}$, $b$, and $d^{'}$ are real positive constants. To compare equations with other studies, such as those in [13, 14], this notation is also preferred in this thesis.

$$TF_{BP}(s) = \frac{i_{d1}}{i_{in}} = \frac{a^{'} s}{1 + as + bs^2} \tag{2.3}$$

$$TF_{LP}(s) = \frac{i_{d2}}{i_{in}} = \frac{d^{'}}{1 + as + bs^2} \tag{2.4}$$

$$TF_{HP}(s) = \frac{d^{'} s^2}{1 + as + bs^2} \tag{2.5}$$

Moreover, $\omega_0$ and $Q$ are given in terms of these parameters as follows,

$$\omega_0 = \sqrt{\frac{1}{b}}\,,\, \frac{\omega_0}{Q} = \frac{a}{b} \tag{2.6}$$

As a result, central angular frequency and the quality factor for the Equation 2.1 and 2.2 given for ideal case in terms of transistor parameters and passive components as

$$\omega_0 = 2\pi f_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{2.7}$$

$$Q = \frac{f_0}{\Delta f} = \sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}} \tag{2.8}$$

The design process starts considering the MOS transistors in Figure 2.1 as voltage controlled current sources. As an example, for a design requirement of $f_0$ = 138.64 MHz and $Q$= 2.743 by utilizing Equation 2.7 and 2.8 we select the transconductance gains $g_{m1}$ and $g_{m2}$ as 127 $\mu$A/V and 236 $\mu$A/V respectively. In addition to that, we have set $C_1$ and $C_2$ as 0.4 pF and 0.1 pF. Having obtained $Q$ and $f_0$ values for BP filter type we can calculate $f_{L3dB}$ as 115.6 MHz and $f_{H3dB}$ as 166.19 MHz which gives $\Delta f = f_{H3dB} - f_{L3dB}$ = 50.59 MHz. It is also possible to get LP current response from another branch of the circuit. Hence, we may calculate the cut-off frequency by utilizing low-pass filter transfer function given in Equation 2.2. As a result, $f_{3dB}$ is 210.25 MHz and low frequency gain is 0 dB. On the other hand, if nonidealities such as $g_{dsn}$, $C_{gdn}$, $C_{gsn}$ are taken into account the transfer functions describing a more realistic behaviour of the design are obtained. To make reasonable intuitive predictions on the overall design, higher order non-idealistic terms are ignored which are related to components such as $C_{gsn}$ and $g_{dsn}$. They are given in Equation 2.9 and 2.10.

$$TF_{BP} = \frac{i_{d1}}{i_1} = \frac{g_{m1}g_{ds1} + C_2 g_{m1} s}{\Delta} \tag{2.9}$$

$$TF_{LP} = \frac{i_{d2}}{i_1} = \frac{g_{m2}(g_{m1} + C_{gd2}s)}{\Delta} \tag{2.10}$$

where

$$\begin{aligned}\Delta = \; & g_{m1}g_{m2} + (C_1g_{ds1} + C_2g_{ds1} + C_2g_{ds1out} + C_2g_{ds2} + \\ & C_2g_{m1} + C_{gd1}g_{m1} + C_{gd2out}g_{m1} + C_{gs2}g_{m1} + \\ & C_{gs2out}g_{m1} + C_2g_{m1out} + C_{gd1}g_{m1out} + \\ & C_{gd2}g_{m1out} + C_{gd2out}g_{m1out} + C_{gs2}g_{m1out} + \\ & C_{gs2out}g_{m1out} + C_{gd2}g_{m2})s + \\ & (C_1C_2 + C_1C_{gd1} + C_1C_{gd2} + C_2C_{gd2} + \\ & C_1C_{gd2out} + C_2C_{gs1} + C_2C_{gs1out} + \\ & C_1C_{gs2} + C_1C_{gs2out})s^2\end{aligned}$$

Moreover, the central angular frequency and quality factor are given in Equation 2.11 and 2.12.

$$\omega_0 = 2\pi f_0 = \sqrt{\frac{g_{m1}g_{m2}}{\begin{array}{c}(C_1C_2 + C_1C_{gd1} + C_1C_{gd2} + C_2C_{gd2} + C_1C_{gd2out} + \\ C_2C_{gs1} + C_2C_{gs1out} + C_1C_{gs2} + C_1C_{gs2out})\end{array}}} \tag{2.11}$$

In order to make MOS transistors operate in the saturation region, we chose the bias voltages and other node voltages affecting the bias conditions accordingly. Note that band-pass and low-pass current outputs are on $M_{1out}$ and $M_{2out}$ respectively. Therefore, core circuitry transistors ($M_1$, $M_2$) must have same $V_{GS}$ and W/L configurations as the output transistors ($M_{1out}$, $M_{2out}$). $M_5$ is utilized to pick up the current of $M_2$. $M_3$, $M_4$ are added to provide the required current bias for output transistors.

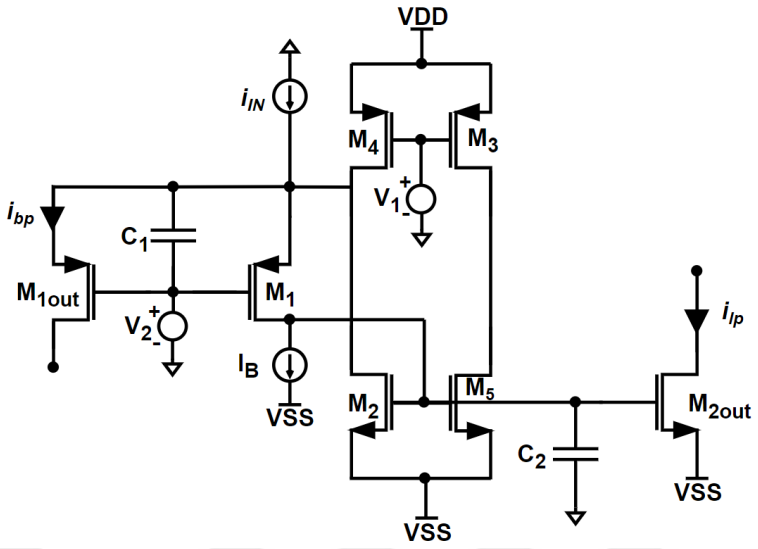


Figure 2.2. Proposed design with bias circuitry.

$$Q = \frac{f_0}{\Delta f} = \frac{\sqrt{\begin{array}{c}(C_1C_2 + C_1C_{gd1} + C_1C_{gd2} + C_2C_{gd2} + C_1C_{gd2out} + \\ C_2C_{gs1} + C_2C_{gs1out} + C_1C_{gs2} + C_1C_{gs2out})g_{m1}g_{m2}\end{array}}}{\begin{array}{c}(C_1g_{ds1} + C_2g_{ds1} + C_2g_{ds1out} + C_2g_{ds2} + C_2g_{m1} + \\ C_{gd1}g_{m1} + C_{gd2out}g_{m1} + C_{gs2}g_{m1} + C_{gs2out}g_{m1} + C_2g_{m1out} + \\ C_{gd1}g_{m1out} + C_{gd2}g_{m1out} + C_{gd2out}g_{m1out} + C_{gs2}g_{m1out} + \\ C_{gs2out}g_{m1out} + C_{gd2}g_{m2})\end{array}} \tag{2.12}$$

The biased circuit is obtained from the core design, as given in Figure 2.2. Applying both current and voltage bias to $M_1$, which leads $M_1$ to conduct bias current and this sets the corresponding source voltage of $M_1$ and $M_{1out}$. Besides that, $C_1$ blocks DC component of $I_{in}$, which results in a small swing of the source voltage of $M_1$. $M_5$ is added for supplying bias voltage, actually, it conducts a small amount of current provided by $M_{1out}$ . $M_3$ and $M_4$ are used to provide bias current required for $M_2$, $M_{2out}$. In addition to that, $M_4$ is also responsible for supplying current for $M_{1out}$ if $I_B$ is smaller than half of $I_{in}$. To supply the required current without violating saturation conditions, we have chosen the size of $M_3$ and $M_4$ much larger than other transistors. Effects of $C_{gs1}$ and $C_{gs2}$ are accommodated by adding extra capacitance to $C_1$ and $C_2$ .

For the biased circuitry shown in Figure 2.2, we need to calculate $C_{gs}$, $g_{ds}$, and $C_{gd}$. Since we have connected source and bulk of MOSFET's, we do not need to take $C_{sb}$ into account. The internal capacitance values are provided in Table 2.1, additionally $g_{ds}$ values are given in Table 2.3. $C_{gs}$ and $C_{gd}$ are calculated for a device, operating in the saturation region, by utilizing the Equation 1.6 and 1.7, respectively. By applying these values we can calculate $f_{3dB}$ as 150.11 Hz and gain as 0 dB for low-pass case. Biased circuitry filter, i.e. calculated, results show that $f_{L3dB}$ as 74.17 MHz and $f_{H3dB}$ as 158.94 MHz, which leads to 84.77 MHz bandwidth for band-pass case. Central frequency ($f_0$) can be calculated as 108.58 MHz and $Q$ as 1.28, utilizing Equation 2.11 and 2.12, respectively. According to calculations, the maximum obtainable gain from BP case is -6.56 dB. Moreover, due to the non-ideal effect primarily caused by $g_{ds1}$, the circuit has a flat band-pass response for low frequencies. By examining the transfer function provided in Equation 2.9, we can see that

$$\lim_{s\to 0} TF_{BP}(s) = \frac{g_{ds1}g_{m1}}{g_{m1}g_{m2}}$$

Hence low-frequency response can be characterized as $\frac{g_{ds1}}{g_{m2}}$. As a result, we expect to get about -45.84 dB flat response for low frequencies. This is due to the fact that the transfer function zero is moved from the origin.

Table 2.1. Internal Capacitances of MOSFET's.

| | $\mathbf{C_{gs1}}$, $\mathbf{C_{gs1out}}$ | $\mathbf{C_{gd1}}$, $\mathbf{C_{gd1out}}$ | $\mathbf{C_{gs2}}$, $\mathbf{C_{gs2out}}$ | $\mathbf{C_{gd2}}$, $\mathbf{C_{gd2out}}$ | $\mathbf{C_{sb1}}$, $\mathbf{C_{sb1out}}$ | $\mathbf{C_{sb2}}$, $\mathbf{C_{sb2out}}$ |
|---|---|---|---|---|---|---|
| **Value(fF)** | 53.14 | 5.71 | 10.91 | 1.42 | 0 | 0 |

It is important to note that all MOS transistors must be kept in the saturation region during operation with largest amplitude input signal. To achieve this goal, bias conditions, transistor parameters, and passive component values must be chosen properly. Since we have connected bulk of transistors with source of MOSFET's, some of non-idealistic effects caused by voltage difference between bulk and source are eliminated. After determining required parameters, transconductance values must

be calculated to get corresponding ideal VCCS model of the both LP and BP filter by applying Equation 2.9 and 2.10. One can be seen clearly in Table 2.3, transistor length is chosen as 0.9 $\mu$m to moderate velocity saturation effects, a dominant factor in sub-micron devices.

Detailed design parameters for active and passive components of biased circuitry are given in Figure 2.2 with proper bias conditions that are provided in Table 2.2 and 2.3. To simulate biased circuitry, we have applied $V_{SS}$ and $V_{DD}$ to the drains of $M_{1out}$ and $M_{2out}$ , respectively.

Table 2.2. Bias Conditions for the filter in Figure2.2

| $\mathbf{V_{DD}(V)}$ | $\mathbf{V_{SS}(V)}$ | $\mathbf{V_1(V)}$ | $\mathbf{V_2(V)}$ | $\mathbf{I_{IN}}(\mu\mathbf{A})$ | $\mathbf{I_B}(\mu\mathbf{A})$ |
|---|---|---|---|---|---|
| 1.8 | 0 | 1.2 | 0.9 | 30 | 15 |

Table 2.3. Transistor parameters for the circuit in Figure2.2.

| | **Type** | $\mathbf{W}(\mu\mathbf{m})$ | $\mathbf{L}(\mu\mathbf{m})$ | $\lvert\mathbf{V_{Th}}\rvert$ | $\mathbf{g_m}(\mu$A/V) | $\mathbf{g_{ds}}(\mu$A/V) |
|---|---|---|---|---|---|---|
| $\mathbf{M_1}$ | P | 9 | 0.9 | 0.396 | 127 | 1.2 |
| $\mathbf{M_{1out}}$ | P | 9 | 0.9 | 0.396 | 133 | 1.05 |
| $\mathbf{M_2}$ | N | 1.8 | 0.9 | 0.372 | 239 | 2.29 |
| $\mathbf{M_{2out}}$ | N | 1.8 | 0.9 | 0.372 | 239 | 2.23 |
| $\mathbf{M_3}$ | P | 72 | 0.9 | 0.396 | 796 | 29.3 |
| $\mathbf{M_4}$ | P | 72 | 0.9 | 0.396 | 815 | 14.9 |
| $\mathbf{M_5}$ | P | 1.8 | 0.9 | 0.396 | 239 | 2.27 |

## 2.3. Simulations for Core Circuitry

The frequency response of BP filter for both ideal and biased design is shown in Figure 2.3 using LT Spice with TSMC 0.18 $\mu$m CMOS process parameters. Transient response is also provided in Figure 2.4 to show a comparison between input and output.

In the frequency domain simulations examining BP response for biased design, we can see the center frequency value as 100.31 MHz. According to design calculations provided in the previous part, center frequencies are found as 138.64 MHz for the ideal design. At the center frequency we see 0 dB gain for ideal case and -6.56 dB in biased design. Besides, -3 dB drop points can be seen from the BP simulation response. These points are observed as $f_{L3dB}$ 115.6 MHz and $f_{H3dB}$ as 166.19 MHz for the ideal circuit. In addition to that, simulation results show that $f_{L3dB}$ as 67.97 MHz and $f_{H3dB}$ as 148.02 MHz for biased design. By combining these results, it is possible to find $Q$ and $f_0$ values for both ideal and biased designs. All of the mentioned results can be observed in Table 2.4, by comparing with values for ideal, biased design calculation, and biased design simulations. Note that, ideal transfer functions are simulated by ideal voltage controlled current sources by replacing transistor model provided in Figure 2.1 while keeping the bias conditions the same.

Table 2.4. Comparison of Ideal, Simulated (Figure2.2) and Calculated (Figure2.2) BPF Results.

| **Spec.** | **Ideal Calculated Results** | **Biased Design Sim. Results** | **Biased Design Calculated Results** |
|---|---|---|---|
| $\mathbf{f_{L3dB}}$ | 115.6 MHz | 67.97 MHz | 74.17 MHz |
| $\mathbf{f_{H3dB}}$ | 166.19 MHz | 148.02 MHz | 158.94 MHz |
| **BW** | 50.59 MHz | 80.04 MHz | 84.77 MHz |
| **BP Gain** | 0 dB | -5.65 dB | -6.56 dB |
| $\mathbf{f_0}$ | 138.64 MHz | 100.31 MHz | 108.58 MHz |
| **Q** | 2.743 | 1.253 | 1.28 |

In the frequency domain simulations examining LP response for both ideal and biased circuitries, we have calculated the cut-off frequency as 210.25 MHz for ideal case and 150.11 MHz for biased one. According to simulation results, current mode LP filter shows 138.92 MHz of bandwidth. Simulation results show that biased design

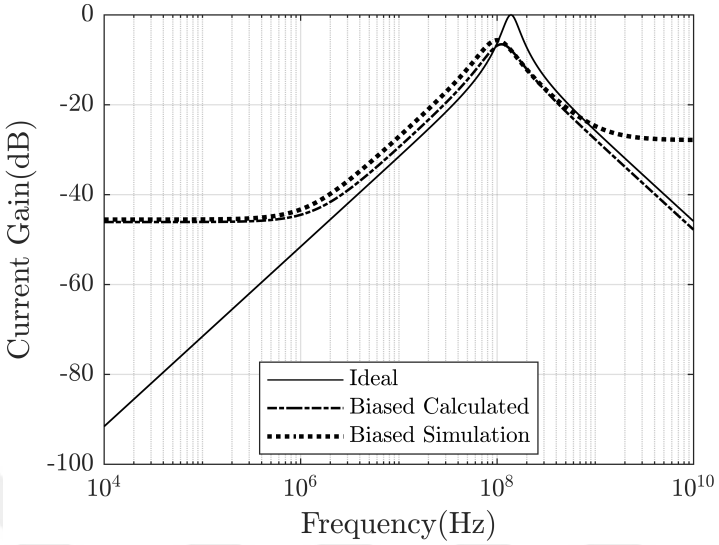


Figure 2.3. Band-pass filter AC response.

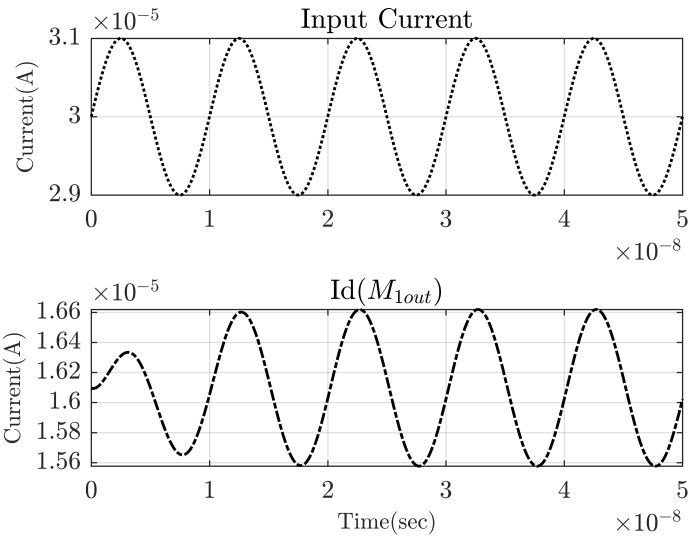


Figure 2.4. Band-pass filter transient response.

has 0 dB low-pass gain. Comparison between ideal, biased design simulation, and calculated biased design results are provided in Table 2.5. The frequency response is shown in Figure 2.5. Transient response is also provided in Figure 2.6 to show comparison between input and LP current output.

Table 2.5. Comparison of Ideal, Simulated (Figure 2.2) and Calculated (Figure 2.2) LPF Results.

| **Spec.** | **Ideal Calculated Results** | **Biased Design Sim. Results** | **Biased Design Calculated Results** |
|---|---|---|---|
| $\mathbf{f_{3dB}}$ | 210.25 MHz | 138.92 MHz | 150.11 MHz |
| **LP Gain** | 0 dB | 0 dB | 0 dB |

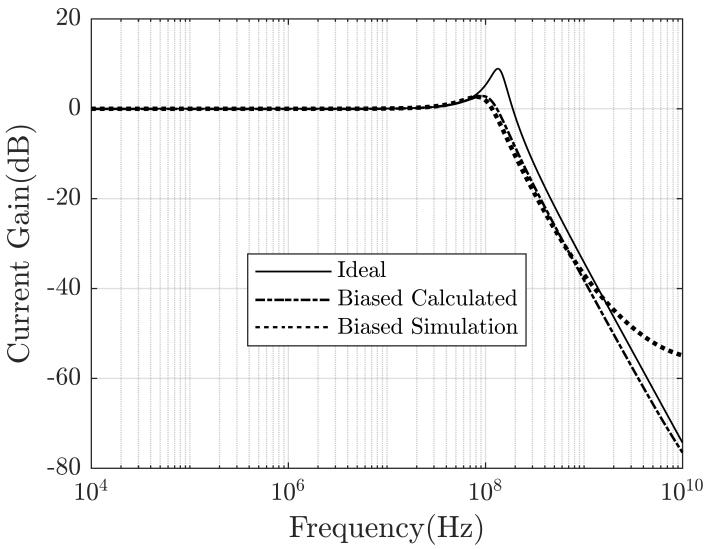


Figure 2.5. Low-pass filter AC response.

To evaluate the practical performance of the circuit we need to perform Monte Carlo analysis in LT Spice. Results will show us the frequency response in case where manufacturing errors are present. Tolerance values are selected as 5% in Monte Carlo analysis applied for both lengths and widths of all MOSFETs and external capacitance sizes. According to simulation results, there is an acceptable difference between perfect implementation and worst case deviated design. Figure 2.7 and 2.8 show both Monte Carlo results with respect to implementation variations.

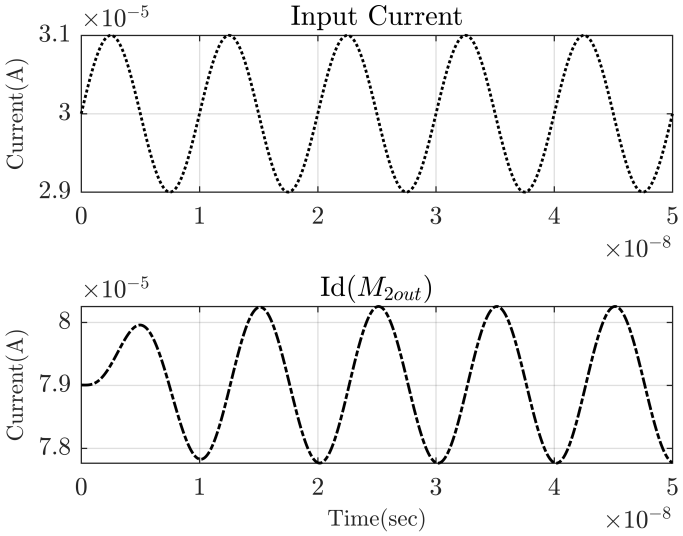


Figure 2.6. Low-pass filter transient response.

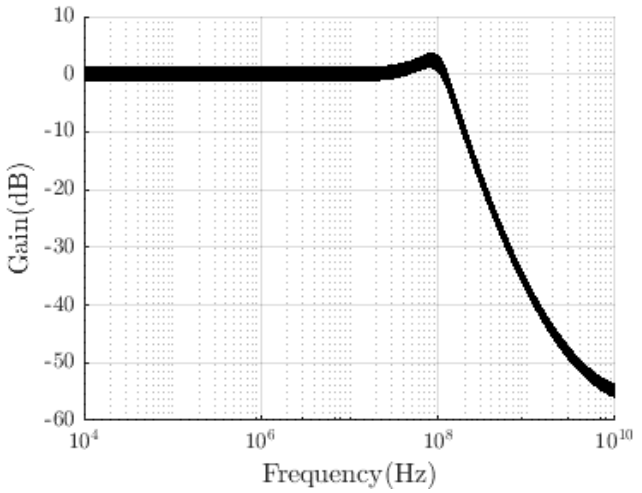


Figure 2.7. Monte Carlo Analysis performed on LP output.

Moreover, we tested the circuit behavior in the frequency domain with temperature ranging from 0° to 100° with the increment of 1° Celsius. Figure 2.9 shows the response variation of the circuit to temperature changes.

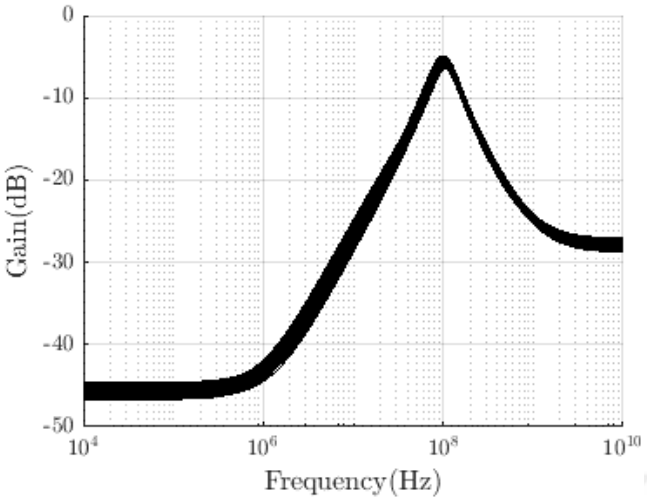


Figure 2.8. Monte Carlo Analysis performed on BP output.

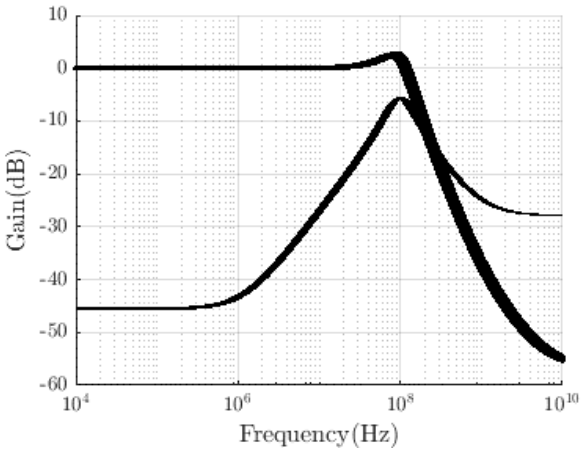


Figure 2.9. Temperature Analysis performed on both BP and LP output.

## 2.4. Proposed Agile Filter Application

Recently, due to their cost, accuracy and integrability of conventional current mode integrated filters working in radio frequency region, frequency-agile filters have taken great interest in radio applications & structures, encrypted communication and global positioning system applications.

The center frequency of tunable filters is corrected by additional hardware to compensate the drifts (thermal, technological, etc.). If the variation of center frequency is expected to be carried out over a very wide frequency range, reconfigurable filters are useful. Recently introduced frequency-agile filters are special type of reconfigurable filters with the property of agility, i.e. the hop between two consecutive frequencies can occur very quickly during the transmission of the signal without disturbing the signal [13]. The main application areas of frequency-agile filters (FAF) are multi-standard transceivers (MST), encrypted communication, cognitive radio, software-defined radio structures, and global positioning systems (GPSs).

By on-chip integration of FAF its size, price, complexity, and power consumption can be reduced while parameters can be still modified in order to be able to adapt to the specifications of different protocols and standards. A frequency-agile filter shown in Figure 2.10 is a reconfigurable filter that has the property of agility, i.e. the hop between two consecutive frequencies $f_1$ and $f_2$ must be able to be carried out very quickly during the transmission of the signal. This is necessary in order not to disturb the signal processing. Its implementation is based on a classical $2^{\text{nd}}$ order frequency filter structure, which provides at least band-pass and low-pass responses.

Class 1 FAF given in Figure 2.11 can be obtained from basic $2^{\text{nd}}$ order filter shown in Figure 2.2 by amplifying the low-pass output current $\text{Id}_{\text{M2out}}$ by adjustable gain A, which is added to the input current $I_{in}$ of the previous circuit. Now the new input current of the filter is $I_E$ , which is given by the formula $I_E = I_{IN} - A.I_{LP0}$ . The output $I_{BP1}$ remains band-pass response and its corresponding transfer function $TF_{BP1}(s)$ is primarily derived from Equation 2.3 and 2.4 by applying feedback factor of A. A is the change of $\text{g}_\text{m}$ of parallel transistors given in Figure 2.12.

Note that $\text{g}_\text{m}$ is proportional to the $\sqrt{W/L}$ ratio. In addition to that, $\text{C}_{\text{gs}}$ , one of the most dominant internal capacitances in affecting frequency response, has a relationship with $W.L$ as the Equation 1.6 suggests. Equations 2.13 and 2.14 demonstrate the relationship between transfer functions obtained for proposed core circuitry in the

first section and agile filter.

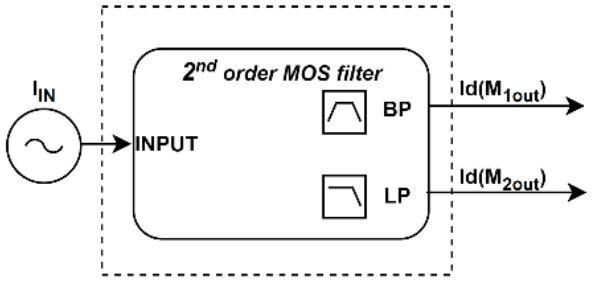


Figure 2.10. Class 0 Frequency Agile Filter.

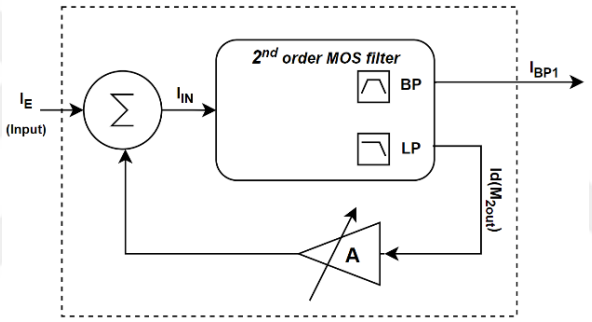


Figure 2.11. Class 1 Frequency Agile Filter made from the basic $2^{\text{nd}}$ – order filter.

$$TP_{BF1}(s) = \frac{I_{BP1}}{I_E} = \frac{TF_{BP}}{1 - A\,TF_{LP}} \tag{2.13}$$

$$TP_{BF1}(s) = \frac{I_{BP1}}{I_E} = \frac{\dfrac{a's}{1 - Ad'}}{1 + \dfrac{as}{1 - Ad'} + \dfrac{bs^2}{1 - Ad'}} \tag{2.14}$$

Moreover, characteristic parameters of both class 0, namely core circuit, and class 1 FAFs are listed in Table 2.6.

Table 2.6. Class 1 Frequency Agile Filter made from the basic 2nd – order filter.

| **Specification** | **Class 0 FAF** | **Class 1 FAF** |
|---|---|---|
| **Center Freq.** | $f_0 = 1/\left(2\pi\sqrt{b}\right)$ | $f_{0A} = f_0\sqrt{1 - Ad'}$ |
| **Q** | $Q = \sqrt{b}/a$ | $Q_A = \sqrt{1 - Ad'}$ |
| **BP gain** | $G_{BP0} = a'/a$ | $G_{BPA} = G_{BP0}$ |
| **BP Bandwidth** | $\Delta f = a/(2\pi b)$ | $\Delta f_A = \Delta f$ |
| **LP gain** | $G_{LP0} = d'$ | – |

The agile filter is constructed by using parallel MOSFETs, having different W/L ratios, as the output MOSFET. The LP output is used as a feedback signal to the input current node. By doing frequency domain analysis, we see that we can alter center frequency of the agile filter with these parallel MOSFETs, which are denoted as $M_6$, $M_7$, and $M_8$ in the circuit diagram. To achieve different $W/L$ ratios, we have switched between parallel MOSFETs [14]. To get applicable results by adding feedback factor of A, we need to keep the following restriction: $0 < A < 1/d'$ . We have applied a negative gain factor of A in order to have frequencies higher than the starting frequency of $f_0$ of the band-pass core filter. By setting transistor sizes as $M_5$ ($1.8\mu/0.9\mu$), $M_6$ ($3.6\mu/0.9\mu$), $M_7$ ($5.4\mu/0.9\mu$), and $M_8$ ($7.2\mu/0.9\mu$), we have obtained various frequency responses. Note that remaining transistor sizes have the same with ones provided in Table 2.3. There are a total of 16 different switch position combinations. As a result, we have obtained various central frequencies between 168.42 MHz and 99.05 MHz corresponding to total size of the parallel MOSFETs. As it is expected, BP gain and BP bandwidth remain unchanged. Note that there is a small decrease in the base (lowest) central frequency, because there is a small amount of current flowing into the gate of $M_5$, $M_6$, $M_7$, and $M_8$ even if their switches are open. Parallel transistors play an additive role in the $C_{gs}$ of $M_2$. As a result, $f_0$ gets lower by the relationship provided in Equation 2.11. Simulation results are also provided in Figure 2.13.

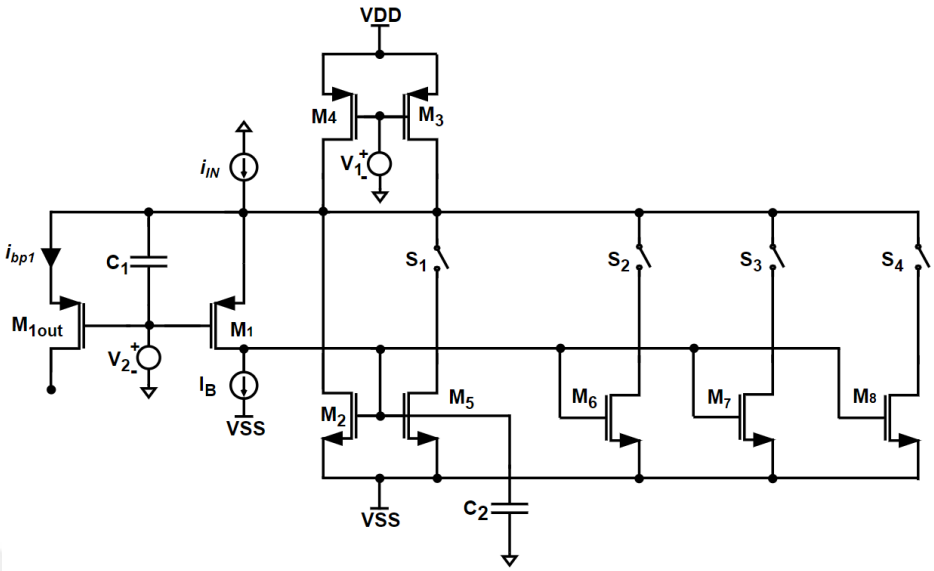


Figure 2.12. Agile Filter with feedback from LP Output.

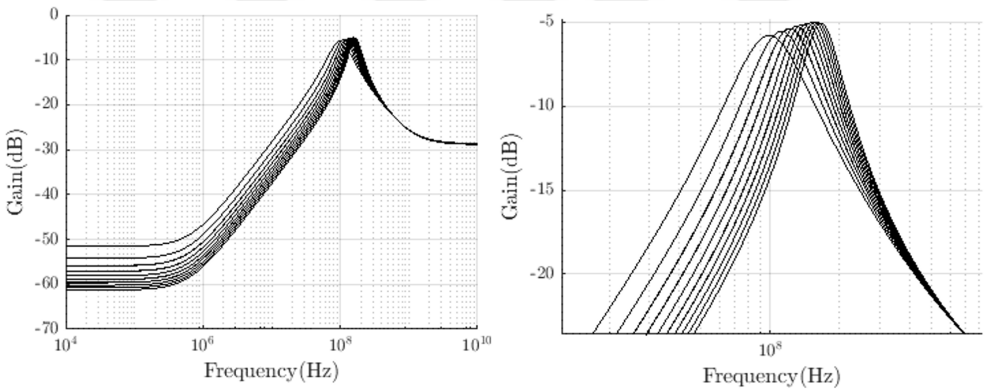


Figure 2.13. Band-pass response of the agile filter for various switch positions with zoomed view of it.

## 2.5. Conclusion for Agile Filter Application

In this part of the thesis, we have proposed a MOS transistor based analog filter core circuit and its extended version to pick up the output current at a high output impedance terminal. The design is capable of providing both low-pass and band-pass responses on different transistors. Moreover, we have obtained modified transfer

functions by taking non-ideal effects into account. Comparisons between ideal transfer functions, biased design calculation, and biased design simulations are illustrated. It is concluded that the circuit responses will stay in acceptable regions for most applications when % 5 deviation is applied on both length and width of transistors by changing filter capacitor values at the same time.

In the last part of the chapter, an agile filter is constructed by using biased initial core design to achieve various central frequencies by allowing a user to switch between them quickly. Finally, it is shown that one is able to tune the filter to different central frequencies which depend on switch positions without disturbing the bandwidth. It is expected that MOS-only designs provide simplicity and extended frequency range for analog filters in the future.

# 3. MOSFET-C TRANSIMPEDANCE FILTERS WITH CENTRAL FREQUENCY TUNABILITY FEATURE

In this section, we have provided eight different MOSFET-C transimpedance filters with their corresponding transfer functions and basic filter specifications. Presented designs show second order standard band-pass, low-pass, and high-pass characteristics. Moreover, some filters provide both low-pass and band-pass characteristics. Especially, having a tunability feature makes a design more useful and applicable for various communication and instrumentation systems. To that end, we have chosen a filter among other designs and biased it under various biasing conditions to tune central frequency by keeping bandwidth constant. To elaborate design with different aspects, we have checked its small signal performance by introducing both changing temperature and implementation errors.

## 3.1. Introduction

MOS-Only design approach mainly utilizes internal $g_m$ and $g_{ds}$ parameters for description of resistive effects and internal capacitances of $C_{gs}$ and $C_{gd}$ for description of capacitive effects. For each physical effect, the former parameter is usually the desired one and the latter describes parasitic effects. Such designs, generally, attract attention with less chip area, reduced energy consumption thanks to resistorless design, and easy fabrication methods. MOSFET-C filters, however, introduce on-chip capacitances, made by polysilicon, to minimize implementation errors [3, 6, 7, 11, 15–18]. Moreover, such on-chip capacitances help a designer to choose operating frequency much easier. In this part of the thesis, we have presented eight different MOSFET-C transimpedance filters and biased one of them with on-chip realizable current and voltage sources. Some related design examples are published before [19–21] to illustrate application range of such filters. Transfer functions are obtained both considering also $g_{ds}$, $C_{gd}$ denoted as non-ideal transfer functions and ignoring such disturbing effects. Comparisons between transfer functions and simulated results are presented in Bode plot and tabulated

form. In addition to mathematical design and analysis, the designs are elaborated in terms of electrically tunability feature, such as constant bandwidth under various bias conditions while altering other filter specifications. Such approach, definitely, paves the way of deploying the design in various frequency ranges easily. However, operating under various bias conditions requires more careful design methodology to keep MOS transistor component always in the saturation region without deviating from expected results. Moreover, circuit performance is evaluated with considering implementation errors and various temperature conditions.

### 3.2. The Design Procedure with Mathematical Explanations

We have presented eight different core transimpedance filters with their ideal transfer function. Note that in this context, ideal transfer function means the one obtained by ignoring internal transconductance and capacitive factors except $g_m$ . For non-ideal transfer function, $g_m$, $g_{ds}$, $C_{gs}$, and $C_{gd}$ factors are taken into account. In this section, ideal transfer functions, quality factors, and central frequencies are provided. By examining Equation [3.1-3.8], it is possible to detect the tunable ones. For example, we have determined focusing on designs giving an opportunity of altering $f_0$ without affecting bandwidth. Hence various $Q$ parameters are achieved which broadens application range of designs.

The core filters without bias are shown in Figure 3.1-Figure 3.8. Note that small-signal equivalent circuits of both PMOS and NMOS devices are identical. Therefore, the presented designs will give the same response for both doping type if proper bias conditions are satisfied. The following section gives design schematics then provides ideal transfer functions with filter specifications.

As can be seen clearly, core designs consist of two or three MOSFETs and two on-chip capacitances. Note that outputs are marked as ground-referenced positive voltages. Some designs are capable of providing multiple outputs with different characteristics. To get more predictive design approach, we provide ideal transfer functions

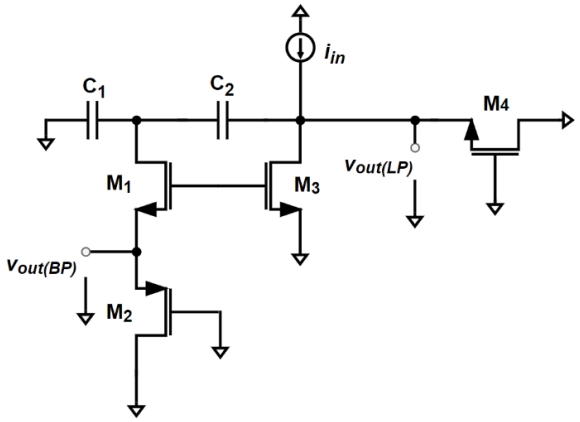


Figure 3.1. 1st proposed transimpedance filter design.

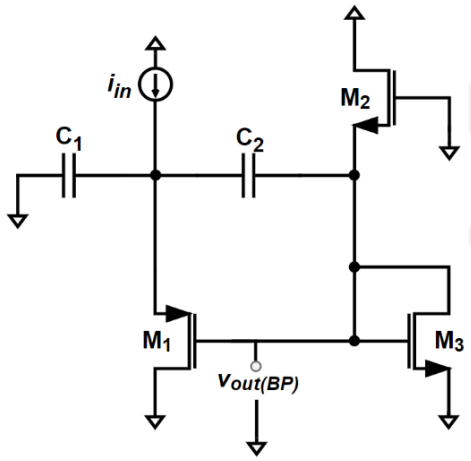


Figure 3.2. 2nd proposed transimpedance filter design.

corresponding to figures Figure 3.1 through Figure 3.8. Note that transfer functions are also in the same order with design schematics. Equation 3.2 gives input-output relation of Figure 3.2.

$$TF_{1.a(BP)} = \frac{C_2 s}{g_{m1}g_{m2}g_{m4} + g_{m1}\left(C_1 g_{m3} + C_1 g_{m4} + C_2 g_{m4}\right)s + C_1 C_2 g_{m4} s^2} \tag{3.1a}$$

$$TF_{1.b(LP)} = \frac{g_{m1}g_{m2}}{g_{m1}g_{m2}g_{m4} + g_{m1}\left(C_1 g_{m3} + C_1 g_{m4} + C_2 g_{m4}\right)s + C_1 C_2 g_{m4} s^2} \tag{3.1b}$$

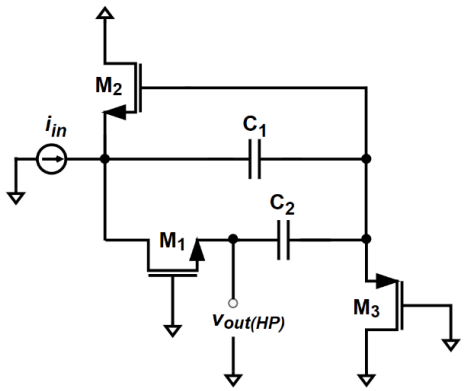


Figure 3.3. 3rd proposed transimpedance filter design.

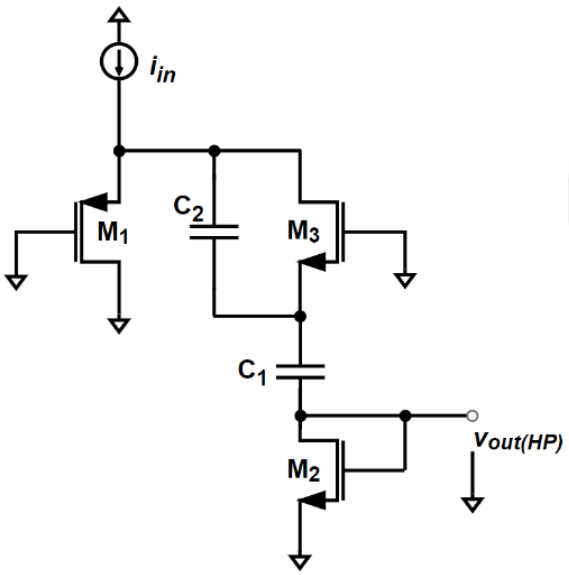


Figure 3.4. 4th proposed transimpedance filter design.

$$TF_2 = \frac{C_2 s}{g_{m1}\left(g_{m2}+g_{m3}\right)+\left(C_1+C_2\right)\left(g_{m2}+g_{m3}\right)s+C_1C_2s^2} \tag{3.2}$$

$$TF_3 = \frac{C_1C_2s^2}{g_{m1}g_{m2}g_{m3}+\left(C_1g_{m1}g_{m3}+C_2g_{m1}g_{m2}+C_2g_{m2}g_{m3}\right)s+C_1C_2g_{m3}s^2} \tag{3.3}$$

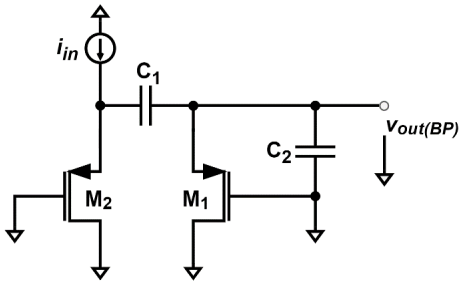


Figure 3.5. 5th proposed transimpedance filter design.

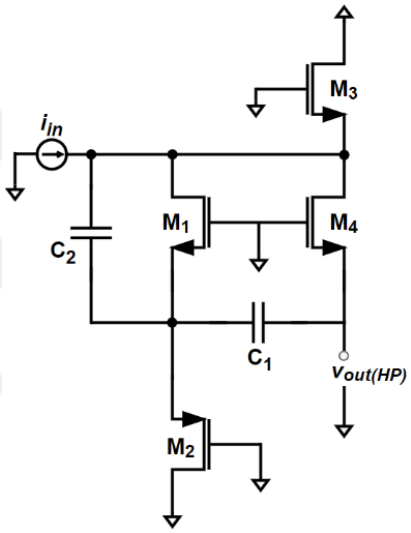


Figure 3.6. 6th proposed transimpedance filter design.

$$TF_4 = \frac{C_1 C_2 s^2}{g_{m1} g_{m2} g_{m3} + g_{m1} \left(C_1 (g_{m2} + g_{m3}) + C_2 g_{m2}\right) s + C_1 C_2 \left(g_{m1} + g_{m2}\right) s^2} \tag{3.4}$$

$$TF_5 = \frac{C_1 s}{g_{m1} g_{m2} + \left(C_1 g_{m1} + C_1 g_{m2} + C_2 g_{m2}\right) s \ + C_1 C_2 s^2} \tag{3.5}$$

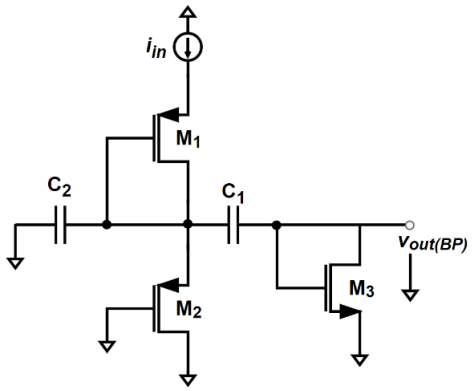


Figure 3.7. 7th proposed transimpedance filter design.

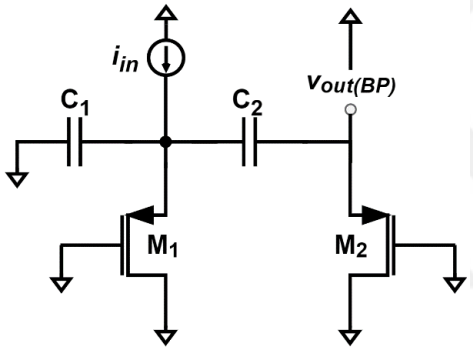


Figure 3.8. 8th proposed transimpedance filter design.

$$TF_6 = \frac{C_1 C_2 s^2}{\begin{array}{c} g_{m3}g_{m4}\left(g_{m1}+g_{m2}\right)+ \\ \left(C_1 g_{m1}g_{m3}+C_1 g_{m2}g_{m3}+C_2 g_{m2}g_{m4}+C_1 g_{m3}g_{m4}+C_2 g_{m3}g_{m4}\right)s+ \\ C_1 C_2\left(g_{m2}+g_{m3}\right)s^2 \end{array}} \tag{3.6}$$

$$TF_7 = \frac{C_1 s}{g_{m2}g_{m3}+\left(C_1 g_{m2}+C_1 g_{m3}+C_2 g_{m3}\right)s+C_1 C_2 s^2} \tag{3.7}$$

$$TF_8 = \frac{C_1 s}{g_{m1}g_{m2} + (C_1 g_{m1} + C_1 g_{m2} + C_2 g_{m2})\, s + C_1 C_2 s^2} \tag{3.8}$$

After calculating ideal transfer functions for eight different core designs, we can evaluate $\omega_0$ and $Q$. Proposed filters show high-pass, band-pass, and low-pass characteristics. The general equations for transfer functions $TF_{BP}(s)$, $TF_{HP}(s)$, and $TF_{LP}(s)$ are in the form of ones given in Equations [2.3-2.5], respectively. In this manner, filter specifications, given in 2.6, can be rearranged as

$$\omega_0 = 2\pi f_0 \quad , \quad \text{Bandwidth(BW)} = \frac{\omega_0}{Q} = \frac{a}{b} \tag{3.9}$$

Equations [3.10-3.17] provide formulas of $\omega_0$ and $Q$ for transfer functions given for Figure [3.1-3.8] respectively, i.e. Equation 3.10 for the design presented in Figure 3.1. The topologies shown in Figure 3.1 and 3.2 permit complex pole filters where the remaining circuits are real pole filters. However, they are included here for the sake of completeness.

$$\omega_{0_1} = \sqrt{\frac{g_{m1}g_{m2}g_{m4}}{C_1 C_2 g_{m3}}},\ Q_1 = \sqrt{\frac{C_1 g_{m1} g_{m2} g_{m3} g_{m4}}{C_2 \left(g_{m1}g_{m4} + g_{m3}\left(g_{m1} + g_{m4}\right)\right)^2}} \tag{3.10}$$

$$\omega_{0_2} = \sqrt{\frac{g_{m1}\left(g_{m2} + g_{m3}\right)}{C_1 C_2}},\ Q_2 = \sqrt{\frac{C_1 C_2 g_{m1}}{\left(C_1 + C_2\right)^2 \left(g_{m2} + g_{m3}\right)}} \tag{3.11}$$

$$\omega_{0_3} = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_2}},\ Q_3 = \sqrt{\frac{C_1 C_2 g_{m1} g_{m2} g_{m3}^2}{\left(C_1 g_{m1} g_{m3} + C_2 g_{m2}\left(g_{m1} + g_{m3}\right)\right)^2}} \tag{3.12}$$

$$\omega_{0_4} = \sqrt{\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2\left(g_{m1}+g_{m2}\right)}},\ Q_4 = \sqrt{\frac{C_1C_2g_{m2}\left(g_{m1}+g_{m2}\right)g_{m3}}{g_{m1}\left(C_2g_{m2}+C_1\left(g_{m2}+g_{m3}\right)\right)^2}} \tag{3.13}$$

$$\omega_{0_5} = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}},\ Q_5 = \sqrt{\frac{C_1C_2g_{m1}g_{m2}}{\left(C_2g_{m2}+C_1\left(g_{m1}+g_{m2}\right)\right)^2}} \tag{3.14}$$

$$\begin{aligned} \omega_{0_6} &= \sqrt{\frac{\left(g_{m1}+g_{m2}\right)g_{m3}g_{m4}}{C_1C_2\left(g_{m2}+g_{m3}\right)}}\ , \\ Q_6 &= \sqrt{\frac{C_1C_2\left(g_{m1}+g_{m2}\right)g_{m3}\left(g_{m2}+g_{m3}\right)g_{m4}}{\left(C_2\left(g_{m2}+g_{m3}\right)g_{m4}+C_1g_{m3}\left(g_{m1}+g_{m2}+g_{m4}\right)\right)^2}} \end{aligned} \tag{3.15}$$

$$\omega_{0_7} = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}},\ Q_7 = \sqrt{\frac{C_1C_2g_{m2}g_{m3}}{\left(C_2g_{m3}+C_1\left(g_{m2}+g_{m3}\right)\right)^2}} \tag{3.16}$$

$$\omega_{0_8} = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}},\ Q_8 = \sqrt{\frac{C_1C_2g_{m1}g_{m2}}{\left(C_2g_{m2}+C_1\left(g_{m1}+g_{m2}\right)\right)^2}} \tag{3.17}$$

To get more predictive design approach, we can search on designs in terms of bandwidth parameters. By adjusting bias current, it is possible to change $g_m$ values according to Equation 1.5 . As a result, $g_m$ is proportional with square root of drain bias current for each transistor, which appears as $I_D$ in the equation.

The design demonstrated in Figure 3.2 has the bandwidth expression of

$$\frac{(C_1+C_2)g_{m2}}{C_1C_2\sqrt{C_1C_2}}$$

by relying on the Equation 3.9. As the expression suggests, there is no $g_{m1}$ dependency

determining the bandwidth. Hence it is possible to electrically tune $f_0$ and $Q$ without disturbing the bandwidth. Since biasing is an integral part of the overall design, we, also, need to design current sources by using wide-swing cascode current mirrors. In addition to that, realization of current sources in this way may moderate the effect of channel length modulation of 180 nm TSMC CMOS process [22]. Considering Equation 3.11 and 1.5 together it is obvious that, $f_0$ is proportional to the $\sqrt[4]{I_D}$. By choosing relatively larger MOS transistors for this part of design, we can eliminate the need of large $V_{GS}$ changes while driving significant amount of current. Figure 3.9 and 3.10 give a deeper insight of how the core circuitry given in Figure 3.2 is biased. Figure 3.9 demonstrates the biasing method of core circuit and Figure 3.10 presents more practical design approach to utilize current sources as cascode current mirrors.

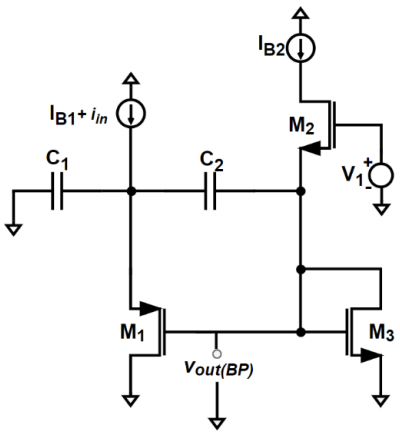


Figure 3.9. Biasing Band-pass core filter given in Figure 3.2 with ideal current sources.

To perform design steps in detail, we can start with the one biased by ideal current sources. In this design, $V_1$ and $I_{B2}$ provide bias condition, so source voltage of $M_2$ to keep saturation is achieved. Since $C_2$ blocks DC current, there should be a path for current flow. Hence $M_3$, also, is responsible for setting this way for drain current of $M_2$ . Besides that, thanks to the connection between its source and ground, reaching saturation condition is much easier for $M_3$ . Such methodology leads $M_3$ to behave as a resistor. The gate voltage of $M_1$ is already obtained by biasing $M_2$. Moreover,

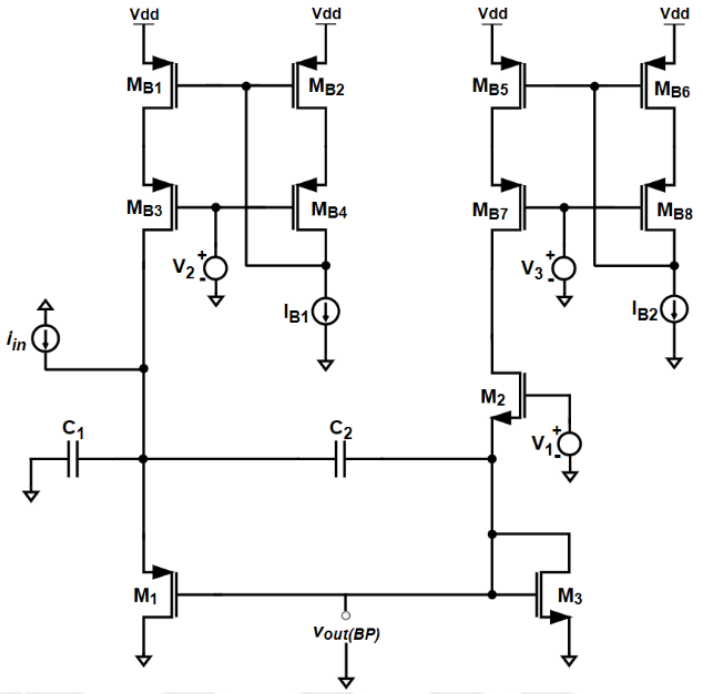


Figure 3.10. Biasing core filter given in Figure 3.2 with cascode current mirror.

source voltage of $M_1$ is set by applying biasing current of $I_{B1}$. Apart from such ideal bias design approach, we can realize current sources as demonstrated in Figure 3.10. To summarize cascode mirror operation, we can observe the effect of $I_{B1}$ on $V_{GS}$ of $M_{B1}$-$M_{B2}$ and $M_{B3}$-$M_{B4}$ . Any increase of $I_{B1}$ results in increase of $|V_{GS}|$ . $M_{B1}$ and $M_{B3}$ , also, are utilized for current picking.

To verify circuit design, we have set $g_{m1}$, $g_{m2}$, and $g_{m3}$ as 640 $\mu$A/V, 51.6 $\mu$A/V, and 69.8 $\mu$A/V respectively. To obtain high $Q$, $g_{m1}$ is selected larger than $g_{m2}$ and $g_{m3}$. It is well known that in integrated circuit implementations low component spread is desired. Therefore, we have selected $C_1 = C_2 = 5$ pF. After having inserting transistor parameters in Equation 3.2, we calculated $f_{L3dB}$ and $f_{H3dB}$ as 5.81 MHz and 13.54 MHz, respectively, corresponding to bandwidth of 7.73 MHz. Additionally, $f_0$ is obtained as 8.87 MHz, which corresponds to $Q$ equal to 1.148. The maximum transimpedance magnitude ratio is calculated as 72.295 dB$\Omega$ , which corresponds to 4.12 K$\Omega$ .

### 3.2.1. Non-Ideal Analysis of Biased Transimpedance Design

Non-ideal factors of a MOS device, namely internal resistances and capacitances, may affect overall circuit response. By getting numerical values of them from Table 3.1 and transfer function calculated in Equation 3.18 by including non-ideal effects, we can predict circuit response under different bias conditions. The corresponding $\omega_0$ and $Q$ equations are also calculated in both exact and simplified form. A designer should note that $g_\gamma \equiv \ g_{m2} + \ g_{m3} + \ g_{ds2} + \ g_{ds3}$ and $C_\delta \equiv C_{\text{gs2}} + C_{\text{gs3}}$. In this regard we denoted the Equations [3.18-3.22] as "exact" ones, because no simplification is applied on them.

$$TF_{BP\ exact} = \frac{(C_2 + C_{gs1})\, s}{\begin{array}{c}(\ g_{m1} + \ g_{ds1})\, g_\gamma + \\ ((C_2 + C_{gd1} + C_{gs1} + C_\delta)\ \ g_{ds1} + \\ (C_1 + C_2 + C_{gs1})\, g_\gamma + (C_{gd1} + C_\delta)\ \ g_{m1})s + \\ (C_1C_2 + (C_1 + C_2)\, C_{gd1} + (C_1 + C_{gd1})\, C_{gs1} + \\ (C_1 + C_2 + C_{gs1})\, C_\delta)s^2\end{array}} \tag{3.18}$$

By applying Equation 3.9, we can get corresponding exact $\omega_0$, $Q$, and bandwidth expressions as given in Equation 3.19, Equation 3.20, and 3.21, respectively.

$$\omega_{0_exact} = \sqrt{\frac{(\ g_{m1} + \ g_{ds1})\, g_\gamma}{(C_1C_2 + (C_1 + C_2)\, C_{gd1} + (C_1 + C_{gd1})\, C_{gs1} + (C_1 + C_2 + C_{gs1})\, C_\delta)}} \tag{3.19}$$

$$Q_{exact} = \frac{\sqrt{\begin{array}{c}(C_1C_2 + (C_1 + C_2)\, C_{gd1} + (C_1 + C_{gd1})\, C_{gs1} + \\ (C_1 + C_2 + C_{gs1})\, C_\delta)\,(\ g_{m1} + \ g_{ds1})\, g_\gamma\end{array}}}{\begin{array}{c}(C_2 + C_{gd1} + C_{gs1} + C_\delta)\ \ g_{ds1} + \\ (C_1 + C_2 + C_{gs1})\, g_\gamma + (C_{gd1} + C_\delta)\ \ g_{m1}\end{array}} \tag{3.20}$$

$$BW_{exact} = \frac{\begin{array}{c}(C_2 + C_{gd1} + C_{gs1} + C_\delta)\ g_{ds1} + \\ (C_1 + C_2 + C_{gs1})\, g_\gamma + (C_{gd1} + C_\delta)\ g_{m1}\end{array}}{C_1C_2 + (C_1 + C_2)\, C_{gd1} + (C_1 + C_{gd1})\, C_{gs1} + (C_1 + C_2 + C_{gs1})\, C_\delta} \quad (3.21)$$

$$Max.\ BP\ Gain_{exact} = \frac{(C_2 + C_{gs1})}{\begin{array}{c}(C_2 + C_{gd1} + C_{gs1} + C_\delta)\ g_{ds1} + \\ (C_1 + C_2 + C_{gs1})\, g_\gamma + \\ (C_{gd1} + C_\delta)\ g_{m1}\end{array}} \quad (3.22)$$

For the biased circuitry band-pass designs, we need to calculate $C_{gs}$, $g_{ds}$, and $C_{gd}$. Since we have connected source and bulk of MOSFET's, we do not need to take $C_{sb}$ into account. Internal capacitance values are provided in Table 3.1, additionally $g_{ds}$ values are given in Table 3.3. How to calculate internal capacitances are explained in detail in Chapter 1 by providing Equations 1.6 and 1.7. By applying these parameter values in Equation 3.18 biased circuitry filter theoretical results show that $f_{L3dB}$ as 5.47 MHz and $f_{H3dB}$ as 13.15 MHz , which leads to 7.68 MHz bandwidth for band-pass filter. Central frequency, $f_0$ is calculated as 8.48 MHz and $Q$ as 1.105, utilizing Equation 3.19 and 3.20, respectively. According to calculations, the maximum obtainable magnitude ratio from BP biased filter can be calculated as 72.148 dBΩ , which corresponds as 4.04 KΩ .

### 3.2.2. Tunability Feature Observation of the Biased Circuitry

Equations [3.18-3.22] are too complicated and does not give much insight about the effect of parameters. To make these equations useful in terms of engineering some simplifications are needed. Some parameters can be ignored against dominant ones. The following paragraph describes this simplification procedure. The simplification starts by ignoring relatively smaller terms such as $C_{gd}g_{ds}$. Note that since we have chosen large $M_1$, making $C_{gs1}$ comparable to $C_{1,2}$ , we cannot omit $C_{gs1}$ with respect to $C_{1,2}$. Moreover, we have set $M_1$ much larger than $M_{2,3}$ , so we can reduce $g_{m2,3}$ with

respect to $g_{m1}$. As a general rule, $g_m \gg g_{ds}$ and $C_{gs} \gg C_{gd}$ , so we can also apply these simplifications. On-chip capacitances of $C_{1,2}$ , also, are much larger than $C_{gd}$. Hence, we obtain reduced $g_\gamma$ as $g_\gamma^{'} \equiv g_{m2} + g_{m3}$. By relying on magnitude comparisons between these variables, we can simplify filter-governing equations of $TF_{BP\ exact}$, $\omega_{0_exact}$, $Q_{exact}$, and $BW_{exact}$ as stated in Equation [3.23-3.27].

$$TF_{BP}^{'} \approx \frac{(C_2 + C_{gs1})\, s}{g_{m1} g_\gamma^{'} + \left((C_1 + C_2 + C_{gs1})\, g_\gamma^{'}\right) s + (C_1 (C_2 + C_{gs1}))\, s^2} \tag{3.23}$$

$$\omega_0^{'} \approx \sqrt{\frac{g_{m1} g_\gamma^{'}}{(C_1 (C_2 + C_{gs1}))}} \tag{3.24}$$

$$Q^{'} \approx \frac{\sqrt{(C_1 (C_2 + C_{gs1}))\ \ g_{m1} g_\gamma^{'}}}{(C_1 + C_2 + C_{gs1})\, g_\gamma^{'}} \tag{3.25}$$

$$BW^{'} \approx \frac{(C_1 + C_2 + C_{gs1})\, g_\gamma^{'}}{(C_1 (C_2 + C_{gs1}))} \tag{3.26}$$

$$Max.\ BP\ Gain^{'} \approx \frac{(C_2 + C_{gs1})}{(C_1 + C_2 + C_{gs1})\, g_\gamma^{'}} \tag{3.27}$$

According to theoretical calculations, explicitly provided in Equations 3.26 and 3.27, bandwidth and maximum band-pass gain is not affected by $g_{m1}$ changes. Note that terms in these equations, including $g_{m1}$, are omitted by relying on magnitude difference between $(C_{gd1} + C_\delta)\, g_{m1}$ and $(C_1 + C_2 + C_{gs1})\, g_\gamma$ . To illustrate this fact, $(C_{gd1} + C_\delta)\, g_{m1}$ is about 40 times less than $(C_1 + C_2 + C_{gs1})\, g_\gamma$ according to design parameters chosen for this filter, so a designer would prefer to choose larger on-chip capacitances at the expense of smaller chip area and higher $f_0$ to get more robust design

with respect to electrical tunability of $g_{m1}$. To explore all of the design parameters, details of MOSFET parameters are explicitly shown in Table 3.1 and 3.3.

Table 3.1. Internal Capacitance of MOSFET's.

| **Comp.** | $\mathbf{C_{gs}(fF)}$ | $\mathbf{C_{gd}(fF)}$ | $\mathbf{C_{sb}(fF)}$ |
|---|---|---|---|
| $\mathbf{M_1}$ | 425.07 | 45.6 | 0 |
| $\mathbf{M_2}$ | 5.45 | 0.71 | 0 |
| $\mathbf{M_3}$ | 10.91 | 1.42 | 0 |
| $\mathbf{M_{B1,2,3,4}}$ | 566.85 | 60.9 | 0 |
| $\mathbf{M_{B5,6}}$ | 425.07 | 45.6 | 0 |
| $\mathbf{M_{B7,8}}$ | 58.85 | 5.71 | 0 |

To achieve saturation conditions for both NMOS and PMOS transistors, we have selected proper bias conditions shown in Table 3.2. Hence we obtained transistor parameters presented in Table 3.3.

Table 3.2. Bias Conditions for biased circuitry filter.

| $\mathbf{V_{DD}(V)}$ | $\mathbf{V_{1,3}(V)}$ | $\mathbf{V_2(V)}$ | $\mathbf{I_{B1}}(\mu\mathbf{A})$ | $\mathbf{I_{B2}}(\mu\mathbf{A})$ |
|---|---|---|---|---|
| 1.8 | 1.2 | 1 | 50 | 5.5 |

As a conclusion for theoretical design part, higher $Q$ requires higher $g_{m1}$ according to Equation 3.25, which can be accomplished either setting larger $M_1$ or higher bias current of $I_{B1}$.In addition to high $Q$ requirement for band-pass filter, to get more predictable electrical tunability feature of design, to get more predictable electrical tunability feature of design, bandwidth expression is also given where Equation 3.26 does not depend $g_{m1}$.

Table 3.3. Transistor parameters for the circuit in Figure 3.10 .

| | **Type** | **W**($\mu$**m**) | **L**($\mu$**m**) | $\mathbf{\lvert V_{Th}\rvert}$ | $\mathbf{g_m}$($\mu$A/V) | $\mathbf{g_{ds}}$($\mu$A/V) |
|---|---|---|---|---|---|---|
| $\mathbf{M_1}$ | P | 72 | 0.9 | 0.396 | 640 | 4.25 |
| $\mathbf{M_2}$ | N | 0.9 | 0.9 | 0.372 | 51.6 | 0.45 |
| $\mathbf{M_3}$ | N | 1.8 | 0.9 | 0.372 | 69.8 | 0.61 |
| $\mathbf{M_{B1}}$ | P | 96 | 0.9 | 0.396 | 699 | 7.29 |
| $\mathbf{M_{B2}}$ | P | 96 | 0.9 | 0.396 | 699 | 7.33 |
| $\mathbf{M_{B3}}$ | P | 96 | 0.9 | 0.396 | 703 | 5.26 |
| $\mathbf{M_{B4}}$ | P | 96 | 0.9 | 0.396 | 699 | 6.93 |
| $\mathbf{M_{B5,6}}$ | P | 72 | 0.9 | 0.396 | 105 | 41.8 |
| $\mathbf{M_{B7,8}}$ | P | 9 | 0.9 | 0.396 | 72.8 | 0.58 |

### 3.3. Simulations for Proposed Transimpedance Circuitry

After getting an insight on theoretical design, to have more practical design specifications and verify calculated results obtained so far, we have performed frequency domain AC analysis as well as time domain transient analysis by utilizing parameters of TSMC 0.18 $\mu$m. Such SPICE analysis demonstrates deviations from paper-based design. In addition to frequency and time domain analysis, a designer must test how implementation errors and environmental changes affect the circuit performance. To check whether the design can achieve acceptable performance under such conditions, we have applied Monte Carlo analysis in LT SPICE by introducing 5% error for both length and width of MOSFETs and on-chip capacitances of $C_1$ and $C_2$. Additionally, temperature change simulations are also done from $0^0$ Celsius until $100^0$ Celsius with the increment of $1^0$ Celsius. In real applications, solid-state systems behave strictly non-linear. However, a system can be assumed to be linear by applying a small-enough AC amplitude. This method allows us to calculate the impedance even though the system is strongly non-linear as a whole. To detect the linear operation limits, we have simulated THD analysis on LT SPICE by increasing input AC current starting from 0.1 $\mu$A with 0.1 $\mu$A increments up to 3 $\mu$A.

The upcoming section is dedicated for providing LT SPICE simulation results by comparing them with calculated ones. According to SPICE simulations, central frequency is found as 6.96 MHz. By utilizing Equation 3.11, provided in previous part, central frequency is calculated as 8.87 MHz with ignoring non-ideal factors. If internal capacitive effects of transistors are taken into account, central frequency is calculated as 8.48 MHz by deploying Equation 3.19. Moreover, SPICE simulation reveals that 3 dB drop points of $f_{L3dB}$ and $f_{H3dB}$ are obtained as 4.4 MHz and 11.02 MHz, which corresponds to bandwidth of 6.62 MHz. As it is explained in Equation 3.9, $Q$ is the ratio of $f_0$ and bandwidth, so $Q$ is achieved as 1.051 according to simulation results. By returning back to preceding section, $f_{L3dB}$ and $f_{H3dB}$ can be calculated for ideal case as 5.81 MHz and 13.54 MHz by utilizing transfer function provided in Equation 3.2, hence bandwidth is 7.73 MHz and $Q$ is 1.148. Moreover, if non-idealities are considered, we can get $f_{L3dB}$ and $f_{H3dB}$ as 5.47 MHz and 13.15 MHz, respectively, by utilizing Equation 3.18. Hence bandwidth is calculated as 7.68 MHz and $Q$ is 1.105. Since this design accepts current as input and voltage as output, it is more convenient to nominate such ratio as magnitude ratio instead of gain. The transimpedance magnitude ratio of design is calculated as 72.295 dBΩ for ideal case, 72.148 dBΩ for one taking non-ideal effects into account. Maximum band-pass simulation response is 72.961 dBΩ . As can be seen clearly, both transfer functions and simulation result give very close magnitude ratios. Table 3.4 summarizes and compares results.

Figure 3.11 demonstrates the frequency response of the circuit. According to the figure, theoretical calculations for considering ideal and non-ideal effects are close to each other.

To demonstrate the signal handling capability of the filter, transient analysis is run at the central frequency of AC simulation response. The result is shown in Figure 3.12.

To evaluate the harmonic distortion performance simulations are carried out. Figure 3.13 shows the THD performance of the circuit. In fact, THD simulations are

Table 3.4. Comparison of Ideal, Biased Design Calculated, and Biased Design Simulated BP Transimpedance Filter Results.

| **Spec.** | **Ideal Calculated Results** | **Biased Design Calculated Results** | **Biased Design Sim. Results** |
|---|---|---|---|
| $\mathbf{f_{L3dB}}$ | 5.81 MHz | 5.47 MHz | 4.4 MHz |
| $\mathbf{f_{H3dB}}$ | 13.54 MHz | 13.15 MHz | 11.02 MHz |
| **BW** | 7.73 MHz | 7.68 MHz | 6.62 MHz |
| **BP Gain** | 72.295 dBΩ | 72.148 dBΩ | 72.961 dBΩ |
| $\mathbf{f_0}$ | 8.87 MHz | 8.48 MHz | 6.96 MHz |
| **Q** | 1.148 | 1.105 | 1.051 |

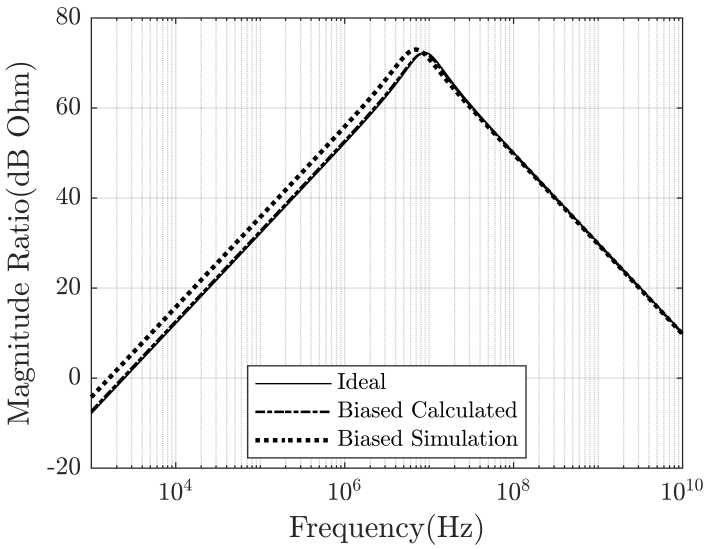


Figure 3.11. Frequency response analysis of circuit vs. calculated transfer functions.

more appropriate for low-pass filters where the input signal is kept well below the cut-off frequency. Therefore, the results of these simulations should be used carefully.

Differential signaling could be used as a remedial method for THD lowering. Since this approach eliminates even harmonics, especially the second fundamental component

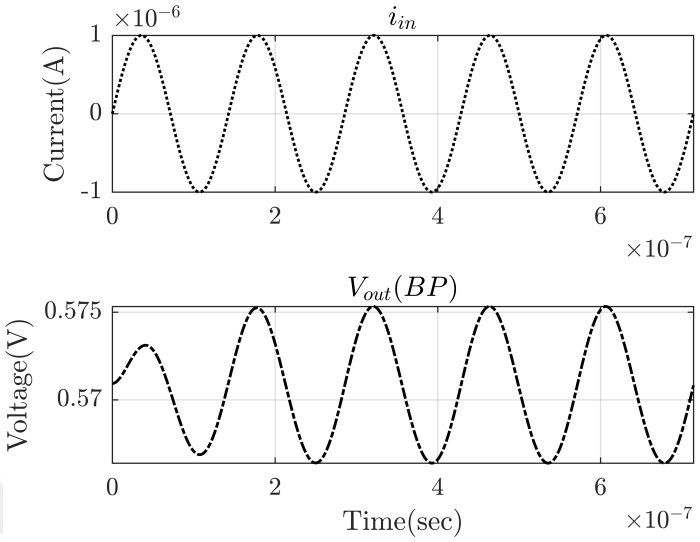


Figure 3.12. Time domain analysis of input current and output voltage.

which is the most dominant distorting factor. To apply differential input pair, we need to get the copy of the single-ended transimpedance circuit, then connect differential pair of small signal input current to first and latter circuitries. Furthermore, the output is obtained as a difference between responses of the pairs. By relying on this procedure, we have achieved to increase $i_{in}$ up to 30 $\mu$A by keeping THD less than 1.95% as shown in the Figure 3.14.

To evaluate the performance of the circuit against temperature and component variations additional simulations are performed. To that end, temperature analysis is executed between 0° C to 100° C with the increase of 1° C. Monte Carlo analysis provides response caused by implementation deviations. To that end, W and L parameters of transistors and on-chip capacitances' values are deviated 5% and executed 200 times. Temperature and Monte Carlo analysis results are shown in Figure 3.15 and 3.16, respectively.

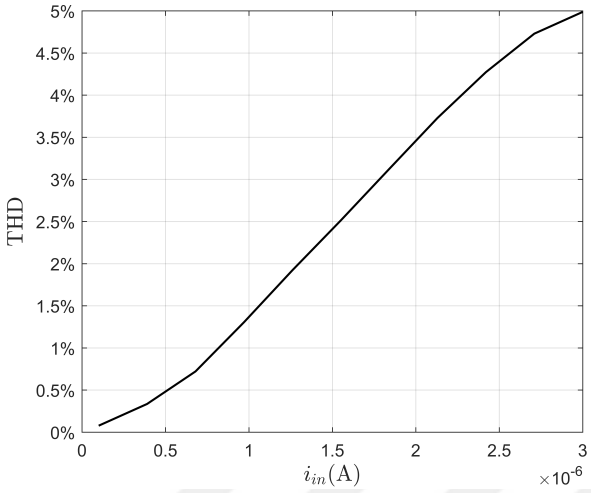


Figure 3.13. THD value versus input currents for single-ended configuration.

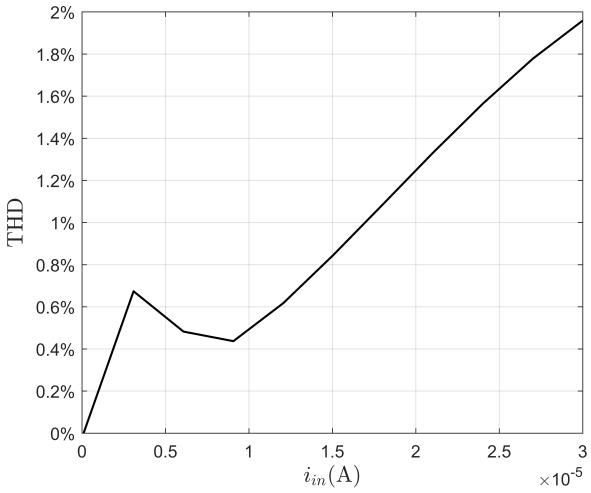


Figure 3.14. THD value versus input currents for differential configuration.

### 3.4. Tunability of Center Frequency

Having a tunability for a design provides an opportunity of altering some design parameters while keeping others constant [23]. According to Equation 3.24 and 3.26, it is possible to tune central frequency without affecting bandwidth significantly. Note that, such equations are all simplified by relying on overwhelming factors. Hence per-

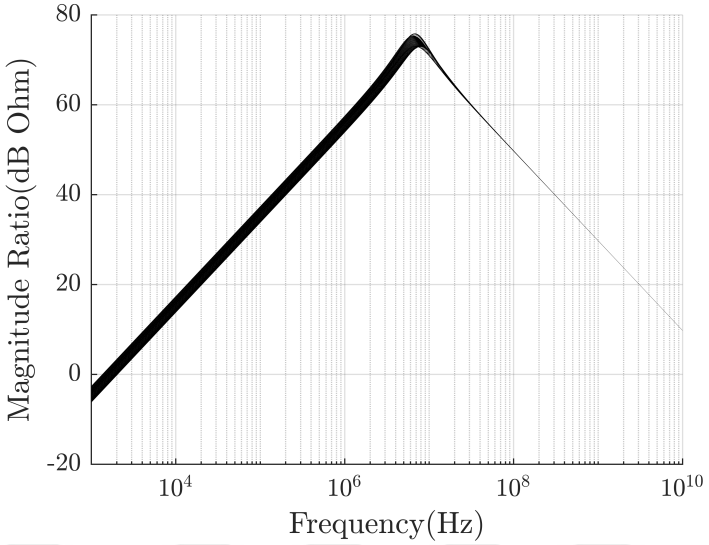


Figure 3.15. AC simulation response with respect to various temperatures.

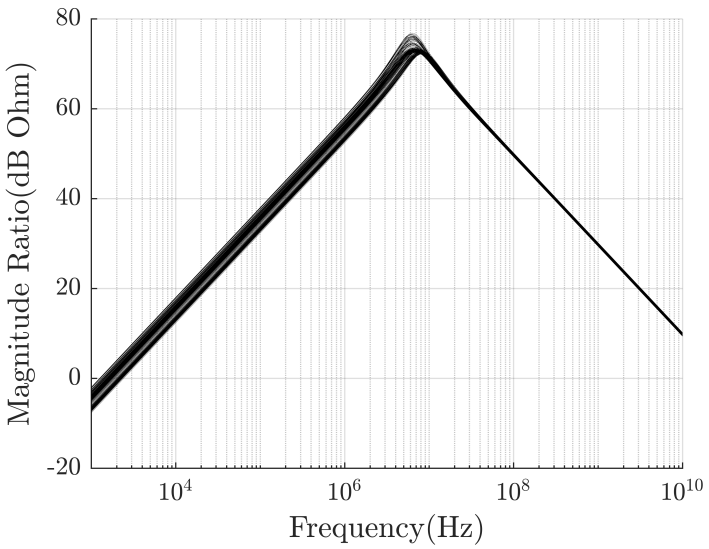


Figure 3.16. AC response of Monte Carlo Analysis.

fect bandwidth conservation is not achievable by utilizing simplified equations but a designer can predict how he or she should set component parameters to obtain results fitting theoretical ones. As it is stated in previous section, handling transfer function considering non-ideal effects, a designer may choose to set larger $C_{1,2}$ to suppress the

effects of $g_{m1}$ on bandwidth. To prove model and give a more practical design approach, we have applied 3 different bias conditions of $I_{B1}$ as 30, 60, and 120 $\mu$A by setting $C_{1,2}$ as 20 pF. Comparative studies for various bias conditions are shown in Figure 3.17. Note that, other circuit design parameters and bias conditions are exactly same with ones provided in previous part. A designer may be requested to get more precise central frequency shifting while preserving bandwidth. To that end, the effect of $(C_{gd1} + C_\delta)\ g_{m1}$ must be moderated with respect to $(C_1 + C_2 + C_{gs1})\, g_\gamma$, as Equation 3.21 suggests, while setting larger $C_{1,2}$ at the expense of high $f_0$. Hence deviations from hand calculations can be alleviated.

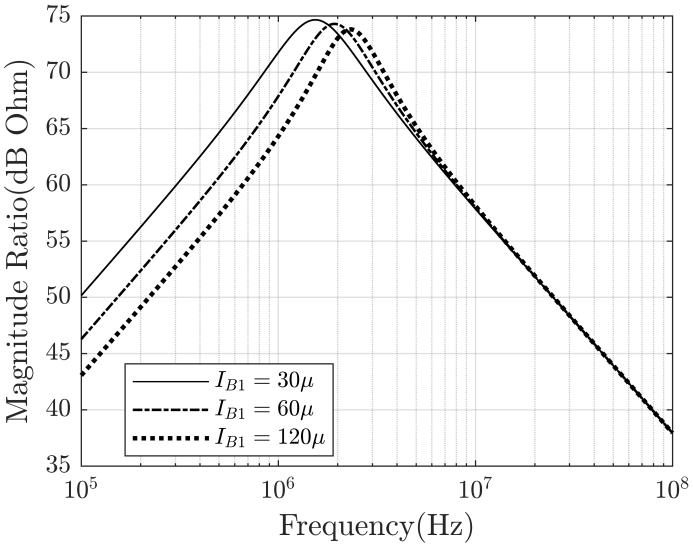


Figure 3.17. Comparison between various bias conditions for selecting on-chip capacitances as 20 pF.

According to SPICE simulation results, for $C_{1,2}$ =20 pF and the bias condition of 30 $\mu$A , we have obtained $f_0$ and bandwidth as 1.54 MHz and 1.41 MHz, respectively. By applying 120 $\mu$A bias current of $I_{B1}$, $f_0$ is switched to 2.32 MHz and bandwidth is demonstrated as 1.56 MHz. As it is suggested by Equation 3.21 and 3.26, there is a slight increase in bandwidth. Quality factor is changed from 1.09 to 1.49. There is just 0.86 dB maximum band-pass magnitude ratio decrease occurs. Remaining details

can be observed in Figure 3.17.

## 3.5. Conclusion

In this chapter our work is on MOSFET-C transimpedance filters, we presented eight different core circuitries with their corresponding transfer functions. To evaluate filter specifications in terms of MOS parameters and on-chip capacitances, we provided $\omega_0$ and $Q$ equations. From this point of view, we also analyzed our filter designs in terms of tunability feature. After completing theoretic analysis for all of designs, we chose one of designs and bias it properly to verify calculated filter specifications. As a result, hand calculations fit SPICE simulation results in quite acceptable manner. Since the circuit we biased is available for filter adjustment, we proposed a tuning method by relying on calculations and simulate it. Hence it is possible for a designer to achieve central frequency switching without affecting bandwidth significantly. Moreover, prerequisites for such tuning are stated explicitly to pave the way for future circuit adjustments.

# 4. MOSFET-C TRANSADMITTANCE FILTERS WITH HIGH-Q BAND-PASS OUTPUT RESPONSE

In some instrumentation and communication applications current output signal is desired where the available input signal is voltage. This chapter presents a group of band-pass biquad filters accepting voltage as input and providing an output current signal. In one section of this chapter, a high-$Q$ transadmittance type biquad band-pass filter is introduced with electronically tunable filter parameters for bandwidth and quality factor adjustments while keeping central frequency constant. The design specifications of the filter are validated by providing mathematical equations and SPICE-based circuit simulations. Transfer functions are presented with and without MOSFET non-ideal effects, primarily caused by internal capacitances. The design consists of four MOSFETs and two capacitances. Moreover, in this chapter four additional transadmittance filters are designed and their corresponding transfer functions are provided. Thanks to such transfer functions, a designer can easily predict the effects of tuning MOSFET parameters and on-chip capacitances.

There are some studies utilizing MOSFET-based design approach to for various filter types [3–7, 10, 11, 15–18]. These filters are called MOS-only because such designs aim at providing capacitive effects by deploying, primarily, $C_{gs}$ rather than introducing additional capacitances. Since MOS-only designs are shaped by internal parameters, W and L of transistors must be set in accordance with strict rules. In this part of the thesis, we have included on-chip capacitors in our designs, practically to be implemented for example poly-poly type such that the effect of internal capacitances on filter parameters are moderated to some extent. Furthermore, electronic tunability plays a crucial role in circuit development such as modifying $Q$ without disturbing $f_0$. There are some proposed designs achieving electronic tunability on MOSFET-C designs for current mode filters [10]. The circuit presented in this part of the thesis is capable of giving high-$Q$ transadmittance band-pass response meanwhile accomplishing electronic tunability. The core design is biased properly to validate circuit operation proposed by

transfer functions. In addition to that, low passive component ratio is achieved. The advantage of such design is to give an opportunity of utilizing energy-efficient chip by using resistorless design. For simulations TSMC 0.18 $\mu$m n-well process parameters are used in LT Spice simulator program.

### 4.1. The Design Procedure with Mathematical Explanations

Five different transadmittance core designs without biasing network are depicted in Figure [4.1-4.5]. Note that additional bias network is necessary for proper operation. Only one of the given filters, namely in Figure 4.5, is suitable for high $Q$ design permitting complex poles, where the others are real pole type. However, they are included for completeness. For all circuits ideal transfer functions are provided.

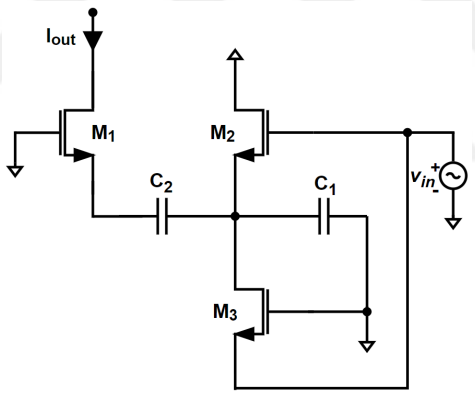


Figure 4.1. 1st proposed transadmittance filter design.

Equation [4.1-4.5] correspond to core designs given in Figure [4.1-4.5], i.e. Equation 4.1 for the circuit in Figure 4.1.

$$TF_1 = \frac{C_2 g_{m1} \left(g_{m2} + g_{m3}\right) s}{g_{m1} g_{m2} + \left(C_1 g_{m1} + C_2 \left(g_{m1} + g_{m2}\right)\right) s + C_1 C_2 s^2} \tag{4.1}$$

$$TF_2 = \frac{C_1 C_2 g_{m1} s^2}{g_{m1} g_{m3} + \left(C_2 g_{m1} + C_1 \left(g_{m1} + g_{m3}\right)\right) s + C_1 C_2 s^2} \tag{4.2}$$

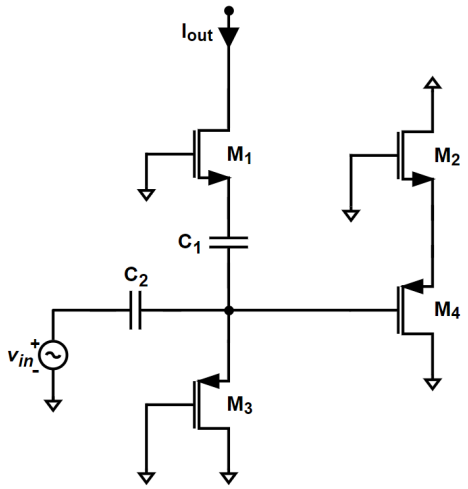


Figure 4.2. 2nd proposed transadmittance filter design.

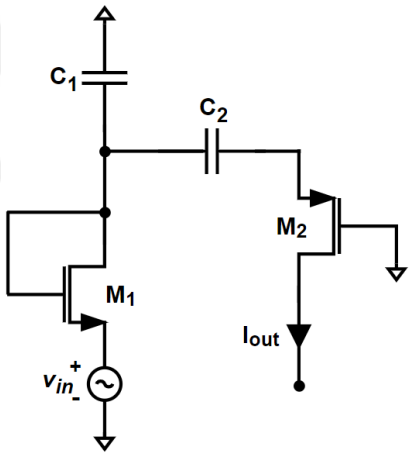


Figure 4.3. 3rd proposed transadmittance filter design.

$$TF_3 = \frac{C_2 g_{m1} g_{m2} s}{g_{m1} g_{m2} + \left(C_1 g_{m2} + C_2 \left(g_{m1} + g_{m2}\right)\right) s + C_1 C_2 s^2} \tag{4.3}$$

$$TF_4 = \frac{C_2 g_{m1} g_{m3} s}{g_{m3} \left(g_{m1} + g_{m2}\right) + \left(C_1 \left(g_{m1} + g_{m2}\right) + C_2 \left(g_{m1} + g_{m2} + g_{m3}\right)\right) s + C_1 C_2 s^2} \tag{4.4}$$

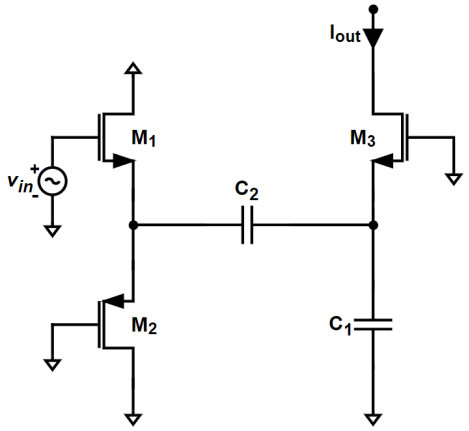


Figure 4.4. 4th proposed transadmittance filter design.

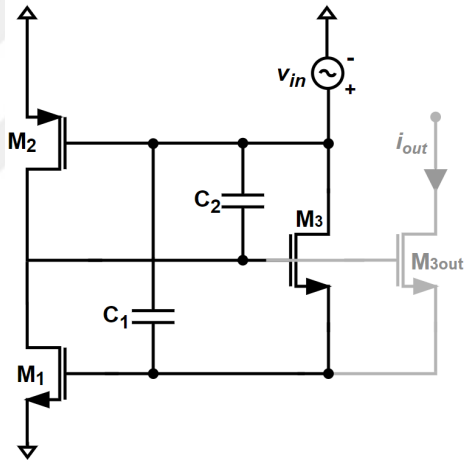


Figure 4.5. 5th proposed transadmittance filter design.

$$TF_5 = \frac{C_1 \left(g_{m1} + g_{m2}\right) g_{m3out}\ s}{g_{m1} \left(g_{m3} + g_{m3out}\right) + C_2 \left(g_{m3} + g_{m3out}\right) s + C_1 C_2 s^2} \tag{4.5}$$

The filter given in Figure 4.2 shows high-pass characteristics and others provide band-pass responses. Equations [4.6-4.10] provide formulas of $\omega_0$ and $Q$ for transfer functions given for Figure [4.1-4.5] respectively, i.e. Equation 4.6 for the design presented in Figure 4.1. Note that how to obtain $\omega_0$ and $Q$ from transfer functions can

be observed by relations between Equation [2.3-2.5] and Equation 2.6.

$$\omega_{0_1} = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}\ ,\ Q_1 = \sqrt{\frac{C_1C_2g_{m1}g_{m2}}{\left(C_1g_{m1} + C_2\left(g_{m1} + g_{m2}\right)\right)^2}} \tag{4.6}$$

$$\omega_{0_2} = \sqrt{\frac{g_{m1}g_{m3}}{C_1C_2}}\ ,\ Q_2 = \sqrt{\frac{C_1C_2\ g_{m1}g_{m3}}{\left(C_2g_{m1}\ + C_1\left(g_{m1} + g_{m3}\right)\right)^2}} \tag{4.7}$$

$$\omega_{0_3} = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}\ , Q_3 = \sqrt{\frac{C_1C_2g_{m1}g_{m2}}{\left(\ C_1g_{m2} + C_2\left(g_{m1} + g_{m2}\right)\right)^2}} \tag{4.8}$$

$$\omega_{0_4} = \sqrt{\frac{\left(g_{m1} + g_{m2}\right)g_{m3}}{C_1C_2}}\ , Q_4 = \sqrt{\frac{C_1C_2\left(g_{m1} + g_{m2}\right)g_{m3}}{\left(C_2\left(g_{m1} + g_{m2} + g_{m3}\right) + C_1\left(g_{m1} + g_{m2}\right)\right)^2}} \tag{4.9}$$

$$\omega_{0_5}\ = \sqrt{\frac{g_{m1}\left(g_{m3} + g_{m3out}\right)}{C_1C_2}}\ ,\ Q_5 = \sqrt{\frac{C_1g_{m1}}{C_2\left(g_{m3} + g_{m3out}\right)}} \tag{4.10}$$

To verify transadmittance filter circuitry operation, we have chosen circuit shown in Figure 4.5 to implement. The main reason of why we preferred this circuitry among others is to obtain high-$Q$ response. None of them can achieve $Q$ values higher than 0.5, which can be verified by setting $g_{m1,2,3}$ and on-chip capacitance ratios for various applicable values and applying formulas provided in Equations [4.6-4.9]. $Q$ values, smaller than 0.5, correspond to real-poled transfer functions and therefore they are also obtainable by passive components only. However, prospective deployment of such low-$Q$ designs may be helpful for some future circuits enjoying energy efficient and chip area efficient resistorless designs. As a brief explanation regarding the Figure 4.5, the proposed core transadmittance band-pass filter consists of three MOSFETs and one current-picking output transistor, shown in light grey. The circuit is suitable for

communication and instrumentation circuit applications.

### 4.2. Filter Tunability and High-$Q$ Design Considerations

In this section, the raw filter shown in Figure 4.5 is worked out and the design is completed considering real life filter specification requirements. Since having a tunability feature for a design gives an opportunity of adjusting circuit response characteristics such that manufacturer's implementation errors can be remedied. Besides that, if the design permits, tuning the filter's specific parameter extends application range. As the ideal design approach suggests, getting high $Q$ values are possible either by setting $C_1 \gg C_2$ or electronically tuning $g_{m1}$ by using bias current. By relying on this, the design will be called as "high-$Q$ transadmittance filter" in the rest of the chapter. Generally, it is preferred to select passive component values with reasonable spread. Additionally, we set some MOS transistors relatively larger than others. Our motivation behind following such methodology is to keep $M_{1,2}$ in the saturation region with respect to large variations in bias current of $I_{B1}$. The relationship between $g_m$ and $I_D$ is represented in Equation 1.5, hence we can set different transconductance values for $M_1$ by just changing bias current applied for it. Due to the fact that neither $\omega_0$ nor $Q$ are affected by the change on $g_{m2}$, we may ignore the change on $M_2$ parameters for ideal design approach.

To demonstrate design verification, we have replaced transistors with their voltage controlled voltage source equivalents, then we have set $g_{m1}$, $g_{m2}$, $g_{m3}$, and $g_{m3out}$ as 436 $\mu$A/V, 209 $\mu$A/V, 17.7 $\mu$A/V and 17.7 $\mu$A/V, respectively. Moreover, we have chosen $C_1$ and $C_2$ as 25 pF and 5 pF, respectively. To achieve high $Q$, the width of $M_1$ is applied larger than other ones and relatively larger bias current is set for $M_1$ than $M_3$. After having applied such transistor parameters, we can calculate $f_{L3dB}$ and $f_{H3dB}$ as 1.66 MHz and 1.88 MHz, respectively,corresponding to a bandwidth of 225.36 KHz. Moreover, $f_0$ is obtained as 1.77 MHz, which corresponds to $Q$ as 7.84. The maximum transadmittance magnitude ratio is calculated as -55.85 dBS, which can be also expressed as 0.0016 mho in transconductance units.

By biasing the circuitry depicted in Figure 4.5 properly to keep saturation conditions for all components, we are able to obtain the design in Figure 4.6. One of

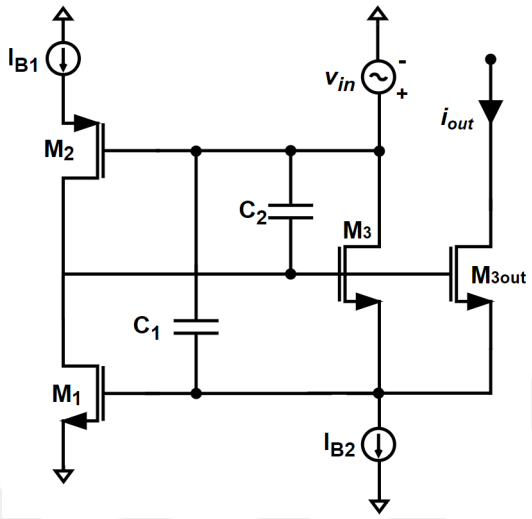


Figure 4.6. Biased high-$Q$ transadmittance filter.

the advantages of the proposed design is to use few components to achieve proposed band-pass filter specifications. $I_{B1}$ directly biases $M_2$ and $M_1$ , which makes a designer eligible to electronically tune $g_{m1}$ and $g_{m2}$. Moreover, $I_{B2}$ biases $M_3$, while giving an opportunity of tuning $g_{m3}$. $C_1$ blocks the DC component of $V_{in}$ and passes its small signal component. Since $I_{B2}$ has no AC component, the signal fluctuation in gate voltage of $M_3$ is achieved thanks to bypassed small signal component of input voltage. Moreover, $M_{3out}$ is responsible for current picking and as an output device for the next stage.

### 4.2.1. Non-Ideal Analysis for Biased High-$Q$ Transadmittance Filter Design

Considering parasitic resistance and capacitance elements, we can obtain the transfer function given in Equation 4.11. Note that $g_\varphi \equiv g_{m3} + g_{m3out}$, $g_\beta \equiv g_{ds3} + g_{ds3out}$ , $C_\gamma \equiv C_{gd3} + C_{gd3out}$ , and $C_\delta \equiv C_{gs3} + C_{gs3out}$. Considering these definitions, the transadmittance is given in Equation [4.11-4.13]. In this context this transadmittance is defined as exact transadmittance and related parameters with this subscript

since these expressions are given without any simplification.

$$\frac{i_{out}}{v_{in}} = \frac{\begin{array}{c} g_{m3out}\ ((g_{ds1}+g_{ds2}+g_{m1}+g_{m2})+ \\ (C_1\,(g_{ds1}+g_{ds2}+g_{m1}+g_{m2})+C_{gs1}g_{m2})\,s- \\ C_{gs1}(\ C_2+C_{gd2}+C_\gamma)\,s^2) \end{array}}{\begin{array}{c} (g_\beta+g_\varphi)\,(g_{ds1}+g_{ds2})+g_{m1}g_\varphi+ \\ ((\ C_1+C_{gd1}+C_{gs1}+C_\delta)\,(g_{ds1}+g_{ds2})+ \\ (\ C_2+C_{gd1}+C_{gd2}+C_\gamma\ +C_\delta)\,g_\beta+ \\ (C_{gd1}+C_\delta)\,g_{m1}+(\ C_2+C_{gd2}+C_\gamma)\,g_\varphi)\,s+ \\ (C_1C_2+C_{gd1}\,(C_1+C_2)+(C_{gd2}+C_\gamma)\,(\ C_1+C_{gd1})+ \\ C_{gs1}(\ C_2+C_{gd1}+C_{gd2}+C_\gamma)+ \\ C_\delta\,(\ C_1+\ C_2+C_{gd2}+C_\gamma+C_{gs1}))s^2 \end{array}} \tag{4.11}$$

Moreover, $\omega_0$ and $Q$ can be obtained as presented in Equation 4.12 and 4.13.

$$\omega_{0\ exact} = \sqrt{\frac{(g_\beta+g_\varphi)\,(g_{ds1}+g_{ds2})+g_{m1}g_\varphi}{\begin{array}{c} C_1C_2+C_{gd1}\,(C_1+C_2)+(C_{gd2}+C_\gamma)\,(\ C_1+C_{gd1})+ \\ C_{gs1}(\ C_2+C_{gd1}+C_{gd2}+C_\gamma)+ \\ C_\delta\,(\ C_1+\ C_2+C_{gd2}+C_\gamma+C_{gs1}) \end{array}}} \tag{4.12}$$

$$Q_{exact} = \frac{\sqrt{\dfrac{\begin{array}{c} C_1C_2+C_{gd1}\,(C_1+C_2)+(C_{gd2}+C_\gamma)\,(\ C_1+C_{gd1})+ \\ C_{gs1}(\ C_2+C_{gd1}+C_{gd2}+C_\gamma)+ \\ C_\delta\,(\ C_1+\ C_2+C_{gd2}+C_\gamma+C_{gs1}) \end{array}}{(g_\beta+g_\varphi)\,(g_{ds1}+g_{ds2})+g_{m1}g_\varphi}}}{\begin{array}{c} (C_1+C_{gd1}+C_{gs1}+C_\delta)\,(g_{ds1}+g_{ds2})+ \\ (\ C_2+C_{gd1}+C_{gd2}+C_\gamma+C_\delta)\,g_\beta+ \\ \dfrac{(C_{gd1}+C_\delta)\,g_{m1}+(\ C_2+C_{gd2}+C_\gamma)\,g_\varphi}{(g_\beta+g_\varphi)\,(g_{ds1}+g_{ds2})+g_{m1}g_\varphi} \end{array}} \tag{4.13}$$

For the biased circuitry band-pass designs, we need to calculate $C_{gs}$ , $g_{ds}$ , and $C_{gd}$. Since we have connected source and bulk of MOSFET's, we do not need to take $C_{sb}$ into account. How to calculate internal capacitances are explained in detail in the Chapter 1 by providing Equations 1.6 and 1.7. Internal capacitance values are provided in Table 4.1, additionally $g_{ds}$ values are given in Table 4.3. $C_{gs}$ and $C_{gd}$ calculation methods are presented in previous chapters. As a result, biased circuitry high-$Q$ transadmittance filter theoretical results show that $f_{\mathrm{L3dB}}$ as 1.55 MHz and $f_{\mathrm{H3dB}}$ as 1.97 MHz , which leads to 415.5 KHz bandwidth for band-pass filter. By utilizing Equation 4.12 and 4.13, respectively, $f_0$ is calculated as 1.75 MHz and $Q$ as 4.20. According to calculations, the maximum obtainable magnitude ratio from BP biased filter can be formulated as -61.36 dBS.

The long and complicated $\omega_0$ and $Q$ expressions do not give much intuition and design guidelines to the application engineer. Therefore, it is preferred to work on simplified versions of $\omega_0$ and $Q$, denoted as $\omega_0^{'}$ and $Q^{'}$ respectively. By considering these facts of $g_{ds} \ll g_m$ and $C_{gs,\,gd} \ll C_{1,2}$, we may simplify equations provided in 4.12 and 4.13. Equations [4.14-4.17] are obtained in this view.

$$\omega_0^{'} \approx \sqrt{\frac{g_{m1}g_{\varphi}}{(C_1 + C_{gs1})\,C_2}} \;\cong\; \frac{1}{C_2}\sqrt{\frac{g_{m1}g_{\varphi}}{\alpha}} \tag{4.14}$$

$$Q^{'} \approx \frac{\sqrt{\dfrac{(C_1 + C_{gs1})\,C_2}{g_{m1}g_{\varphi}}}}{\dfrac{(C_1\,(g_{ds1} + g_{ds2}) + C_2 g_{\varphi})}{g_{m1}g_{\varphi}}} \;\cong\; \frac{\sqrt{\alpha g_{m1}g_{\varphi}}}{((g_{ds1} + g_{ds2})\,\alpha + g_{\varphi})} \tag{4.15}$$

$$BW^{'} \approx \frac{(\;C_1\,(g_{ds1} + g_{ds2}) + \;C_2 g_{\varphi})}{C_1\,(C_2 + C_{gs1})} \;\cong\; \frac{(g_{ds1} + g_{ds2})\,\alpha + g_{\varphi}}{C_1} \tag{4.16}$$

$$Max.\ BP\ Gain \cong \;\frac{g_{m3out}\,((g_{m1} + g_{m2})\,\alpha + (C_{gs1}/C_2)g_{m2}))}{(g_{ds1} + g_{ds2})\,\alpha + g_{\varphi}} \tag{4.17}$$

As a design approach with low component spread we have chosen $C_1$ / $C_2$, symbolized by $\alpha$ , not much greater than one. According to filter parameters given in Table 4.1 and 4.3, there is not much difference between $(g_{ds1} + g_{ds2})\,\alpha$ and $g_{\varphi}$ . However, $C_1$ is overwhelming on $C_{gs1}$, so Equation 4.14 and 4.15 can be applicable. A designer may consider to connect larger $C_1$ by without disturbing $C_1$ / $C_2$ ratio to moderate the effect of $C_{gs1}$ factor in denominator of Equation 4.11 and 4.12. Hence simplified Equation 4.14 is made applicable.

Table 4.1. Internal Capacitance of High-$Q$ Transadmittance Filter MOSFET's.

| **Comp.** | $\mathbf{C_{gs}(fF)}$ | $\mathbf{C_{gd}(fF)}$ | $\mathbf{C_{sb}(fF)}$ |
|---|---|---|---|
| $\mathbf{M_1}$ | 436.37 | 56.9 | 0 |
| $\mathbf{M_2}$ | 106.27 | 11.4 | 0 |
| $\mathbf{M_3}$ | 5.45 | 0.71 | 0 |
| $\mathbf{M_{3out}}$ | 5.45 | 0.71 | 0 |

To achieve saturation conditions for both NMOS and PMOS transistors, we have applied proper bias conditions. Using these bias conditions we obtained the transistor parameters presented in Table 4.3.

Table 4.2. Bias Conditions for selected filter to be designed.

| $\mathbf{V_{DD}(V)}$ | $\mathbf{V_{IN}(V)}$ | $\mathbf{I_{B1}}(\mu\mathbf{A})$ | $\mathbf{I_{B2}}(\mu\mathbf{A})$ |
|---|---|---|---|
| 1.8 | 1.35 | 20 | 2 |

## 4.3. Simulations for Proposed High-$Q$ Transadmittance Filter Circuitry

To verify the functionality of the proposed design, we performed AC and transient simulations on LT SPICE by utilizing TSMC 0.18 $\mu$m parameters. The comparison between calculated results and SPICE results, also, are depicted clearly. Moreover, we will run Monte Carlo analysis more than 200 times to detect the circuit performance

Table 4.3. Transistor parameters for the circuit in Figure 4.6.

| | **Type** | **W**($\mu$**m**) | **L**($\mu$**m**) | $\mathbf{\lvert V_{Th}\rvert}$ | $\mathbf{g_m}$($\mu$A/V) | $\mathbf{g_{ds}}$($\mu$A/V) |
|---|---|---|---|---|---|---|
| $\mathbf{M_1}$ | N | 72 | 0.9 | 0.372 | 436 | 3.55 |
| $\mathbf{M_2}$ | P | 18 | 0.9 | 0.396 | 209 | 1.54 |
| $\mathbf{M_3}$ | N | 0.9 | 0.9 | 0.372 | 17.7 | 0.146 |
| $\mathbf{M_{3out}}$ | N | 0.9 | 0.9 | 0.372 | 17.7 | 0.146 |

while introducing 5% deviations transistor geometric parameters and capacitances. Temperature analysis, also, is provided by changing temperature from 0° C to 100° C to give insight for a designer to explore circuit limitations under various environmental factors. Furthermore, THD analysis is demonstrated with respect to changes observed in $v_{\text{in}}$ . Note that, all of analysis is carried out with the parameters given in Table 4.2 and 4.3.

Figure 4.7 and 4.8 demonstrate frequency domain and time domain responses of the circuit by examining transfer function outputs of Equation 4.5 and 4.11, respectively. As a reminder, Equation 4.5 corresponds to ideal result and Equation 4.11 gives calculated response of biased design result in Figure 4.7. Moreover, "biased simulation" results in the figure depicts LT SPICE simulation responses.

Following section is dedicated to compare simulation results and their corresponding theoretical transfer function results. SPICE simulations reveal that $f_0$ is obtained as 1.747 MHz. Ideal transfer function given in Equation 4.5 and the one taking internal capacitances give $f_0$ as 1.77 MHz and 1.75 MHz, respectively. Moreover, -3dB drop points $f_{3\text{dBL}}$ and $f_{3\text{dBH}}$ are gotten from SPICE simulation as 1.58 MHz, 1.93 MHz respectively. Such results correspond to bandwidth of 348.65 KHz and quality factor of 5.01. From previous section, we have calculated maximum magnitude ratio for ideal case -55.85 dBS and -61.43 dBS by including internal capacitive effects into design. SPICE simulation demonstrates that -63.56 dBS magnitude ratio is achievable. As a conclusion overall results obtained from both theoretical calculations and SPICE sim-

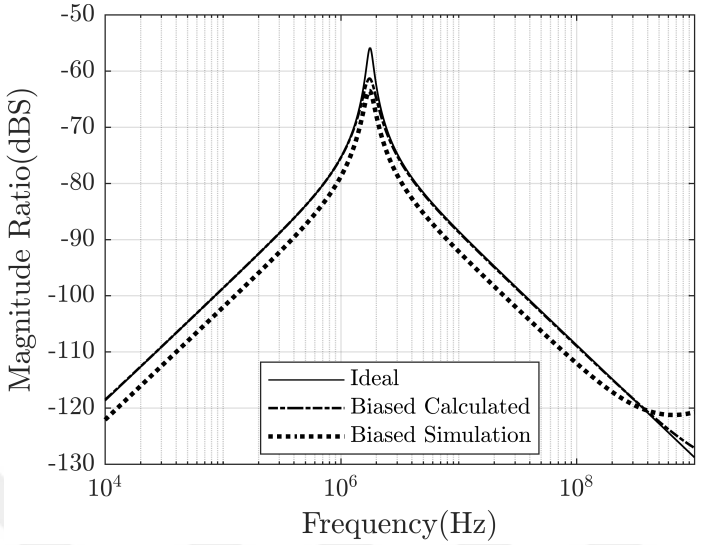


Figure 4.7. Frequency domain responses of band-pass transadmittance filter design.

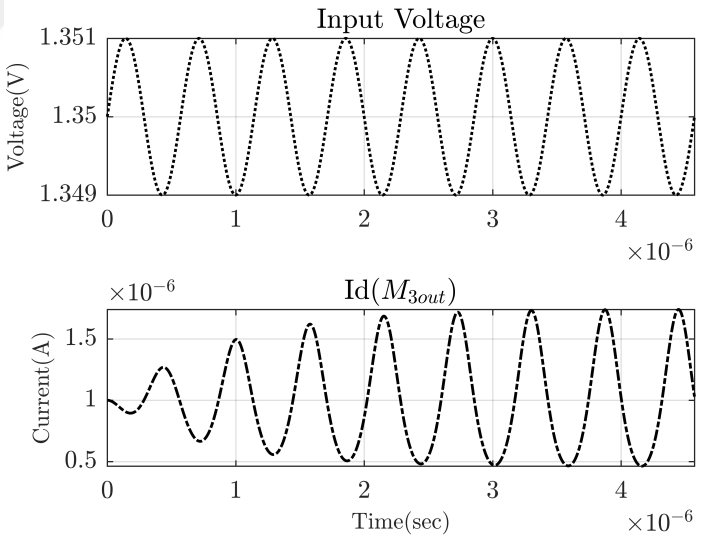


Figure 4.8. Time domain responses of band-pass transadmittance filter design.

ulations match each other in a quite acceptable manner. Summarized results are also demonstrated in Table 4.4.

Table 4.4. Comparison of Ideal, Biased Design Calculated, and Biased Design Simulated BP High-$Q$ Transadmittance Filter Results.

| **Spec.** | **Ideal Calculated Results** | **Biased Design Calculated Results** | **Biased Design Sim. Results** |
|---|---|---|---|
| $\mathbf{f_{L3dB}}$ | 1.66 MHz | 1.55 MHz | 1.58 MHz |
| $\mathbf{f_{H3dB}}$ | 1.88 MHz | 1.97 MHz | 1.93 MHz |
| **BW** | 225.36 KHz | 415.5 KHz | 348.65 KHz |
| **BP Gain** | -55.85 dBS | -61.36 dBS | -63.56 dBS |
| $\mathbf{f_0}$ | 1.77 MHz | 1.75 MHz | 1.75 MHz |
| **Q** | 7.84 | 4.20 | 5.01 |

To detect the input variation range we have performed THD analysis. As a design guide output current distortion is shown up to 5%. According to obtained analysis results, there is a linear relationship between input amplitude variation and output distortion. In contrast to a low-pass or high-pass filter where the test signal is selected such that the harmonics are not attenuated, for a band-pass filter however THD simulation is to be interpreted carefully.

Temperature analysis is also performed between 0° C to 100° C to evaluate the behavior of the circuit under various environmental conditions. These simulations demonstrate that the increase of temperature results in decrease of both $f_0$ and maximum magnitude ratio. Results are shown in Figure 4.10.

In addition to THD and temperature analysis, caused by variations in external factors, Monte Carlo analysis provides response caused by implementation deviations. To that end, W and L parameters of transistors and on-chip capacitances are deviated 5% by running 200 times. Monte Carlo analysis is provided in Figure 4.11 to depict how the circuit behaves due to such errors.

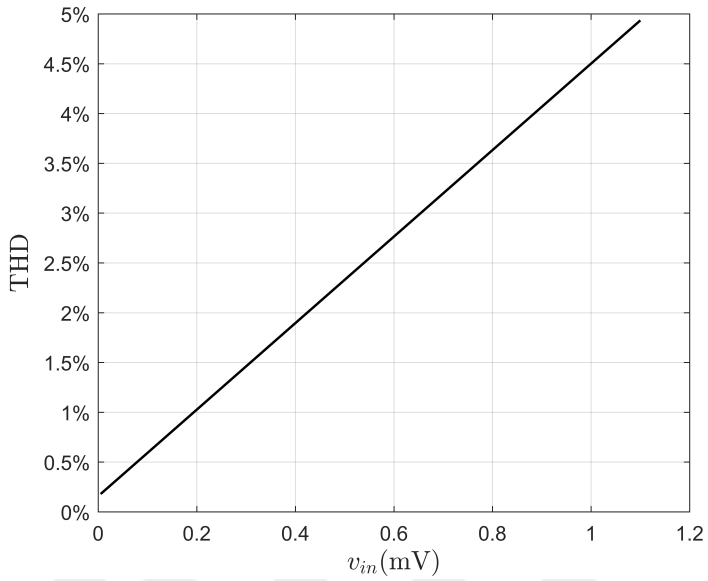


Figure 4.9. THD analysis of band-pass transadmittance response.

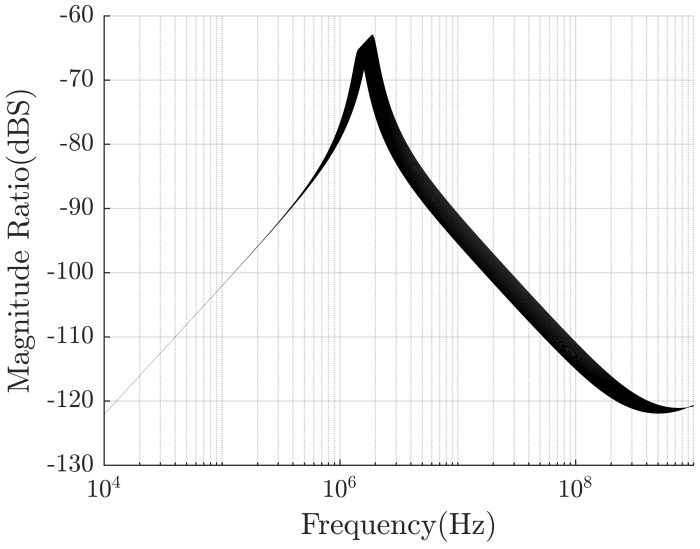


Figure 4.10. Temperature Analysis of High-$Q$ Transadmittance Filter.

## 4.4. Tunability of Bandwidth

It is one of the most unique and advantageous features of MOS-only or MOSFET-C designs, to make a designer able to tune bandwidth, quality factor, or central angu-

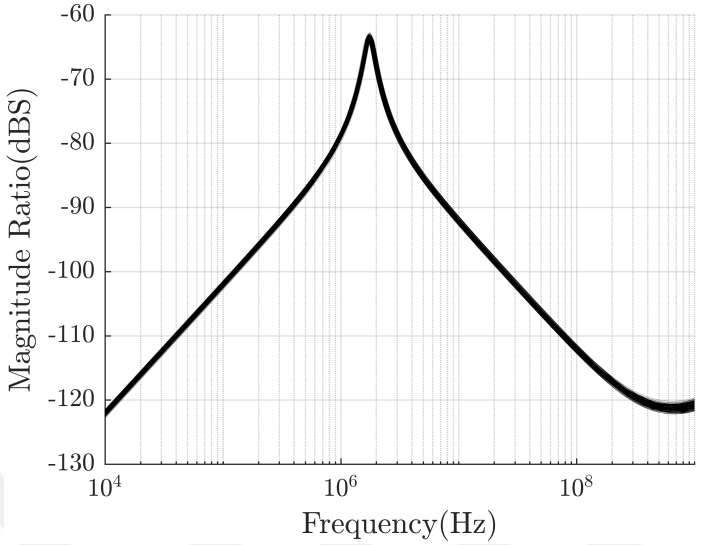


Figure 4.11. AC response of Monte Carlo Analysis.

lar frequency by just arranging some bias conditions. To that end, simplified transfer functions provided in Equation [4.14-4.17] give details on relationship between bias-dependent ($g_m$ , $g_{ds}$) MOS transistor specifications and band-pass filter features. Furthermore, to explore a methodology granting a designer a chance of setting $f_0$ , $Q$, or bandwidth independently, i.e. without affecting other filter parameters, is among most preferable design goals. For this purpose, it is a helpful starting point to utilize simplified circuit parameter equations. As it is stated in Equation 4.14, central angular frequency depends on none of $M_2$ parameters, such as $g_{m2}$, $C_{gs2.}$ However, according to design depicted in Figure 4.6, $M_1$ and $M_2$ share the same bias current, so single tuning is not possible. Hence to keep $f_0$ constant, we can choose to scale up $I_{B1}$ and scale down $I_{B2}$ in the same ratio. Meanwhile, as Equation 4.16 demonstrates that bandwidth can be increased without affecting $f_0$ by following this approach. We have applied 3 different bias currents ($I_{B1}$, $I_{B2}$) scenarios by keeping $g_{m1}g_{\varphi}$ constant to get nearly same $f_0$ . As it is mentioned previously, $I_{B1}$ is utilized to set $g_{m1,2}$ and $g_{ds1,2}$ , besides $I_{B2}$ is for $M_3$ and $M_{3out}$ parameters. According to SPICE simulations given in Figure 4.12 , we have $f_0$ values as 1.75 MHz, 1.75 MHz, and 1.68 MHz for 3 different bias current case. Corresponding bandwidths are obtained as 348.75 KHz, 503.73 KHz, and 768.92

KHz. Hence $Q$ values of 5.01, 3.47, and 2.18 are obtainable. Detailed bias conditions and simulation results and zoomed version are depicted in Figure 4.12. Note that, saturation conditions must be fulfilled while changing bias conditions.

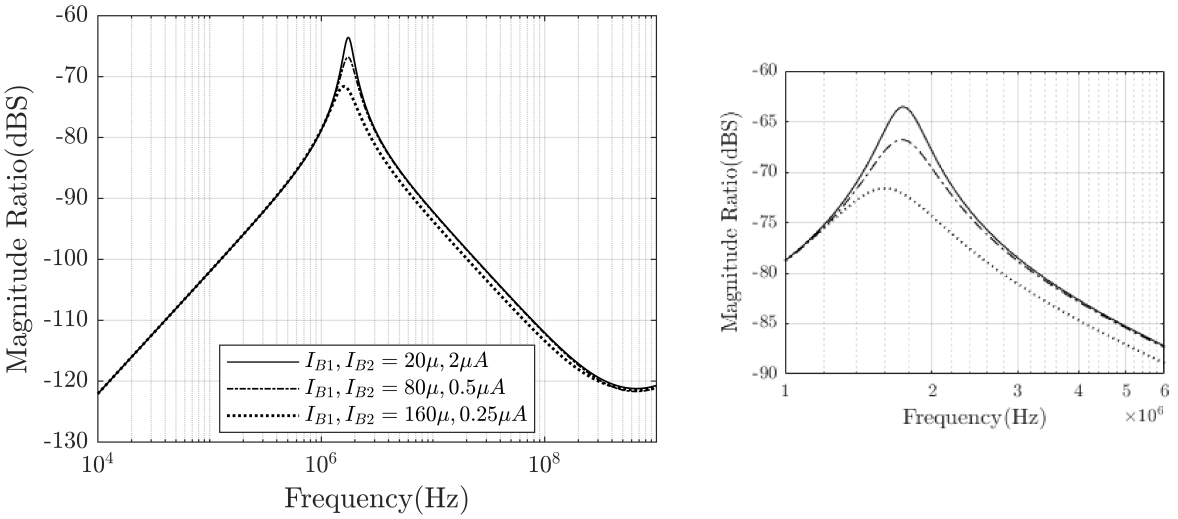


Figure 4.12. Band-pass filter results for various bias conditions and zoomed version of it.

As can be seen clearly there is a decrease in magnitude ratio due to increase of $I_{B1}$ and decrease of $I_{B2}$ . To moderate effect an external current amplifier may be connected on the output of the transadmittance filter.

## 4.5. Conclusion

This chapter aims at providing several MOSFET-C transadmittance type biquadratic filters. From the five presented core filters one is suitable for high $Q$ designs and the others are real pole filters. The complete design of high $Q$ filter was described by biasing it properly and detailed analysis providing ideal as well as non-ideal transfer functions with $\omega_0$ and $Q$ equations were given. Simplified versions of these equations were also provided to give guidelines to the design engineer since it gives a quick design insight. Therefore, the circuits can also be used as part of a communication or

instrumentation circuit.

To illustrate the possibility of tuning, a method was shown to keep central frequency unaffected while changing bandwidth under various bias conditions. To verify the functionality of the high $Q$ filter circuit operation, LT SPICE was executed with TSMC 180 nm parameters. SPICE simulation and theoretical results were illustrated in both graphic and tabulated form.

# 5. VIRTUALLY INFINITE BANDWIDTH MOSFET-C TUNABLE HIGH-PASS ANALOG FILTER

High-pass filters attenuate the signals below their cut-off frequency. The expectation from them is to pass all signals above their cut-off frequency without attenuation which in general is not possible since active filters based on OPAMPs, OTAs or other active devices have cut-off frequencies at the high frequency side. For these cases the frequency response is mainly limited by the active device itself. Voltage mode filter design is an attention-grabbing topic, so several voltage mode filters with different signal passing characteristic, [24–37] are demonstrated. In this chapter, we designed some voltage mode MOSFET-C filter cores and presented with corresponding ideal and non-ideal transfer functions. The first six core circuits are real pole filters and the seventh is a complex pole filter. The real pole filters are included for the sake of completeness. It is well-known that by applying feedback the poles can easily be moved to the complex plane. This technique is repeated briefly in the Appendix B for convenience. Each of the presented core design gives a starting point to a designer and with necessary bias and feedback circuits a new filter circuit can be obtained. This is left to the application engineer reading this work and not considered here to keep the length of the chapter reasonably short. However, we selected the raw filter which can have complex poles with appropriate selection of element values and transconductances and finished a complete design. The circuit exhibits virtually infinite bandwidth if driven by an ideal voltage source since both filter capacitors form a feedforward path from input to output. The bandwidth limitation will be due to output impedance of the signal source as well as due to loading of the filter which means the filter itself will not contribute to bandwidth limitation.

Since none of proposed raw designs contain resistors, a designer is expected to achieve energy- and area-efficient core circuits. The only passive components deployed in designs is on-chip capacitors which are generally on the order of 10 pF, so they could be obtained by poly-silicon layers. It is well known that $Q > 0.5$ is an exclusive

attribute of active filters. Otherwise the filter is equivalent to a passive filter. Having a tunability feature for an active filter, not only broadens the application range but also makes the circuit recoverable against production tolerances. To get an intuition from an engineering point of view for the tuning purpose, we applied some simplifications on non-idealistic cumbersome transfer functions by relying on comparative magnitude analysis between MOSFET-C design factors. Based on theoretical works mainly composed of transfer functions, we have chosen the design which enables high $Q$ without additional hardware except bias circuit, then biased it to meet these two design specifications. According to the results, it is proven that tuning $f_c$ without disturbing $Q$ significantly is feasible for the chosen filter. After SPICE simulations, the biased circuit layout is provided to get more realistic results. To ease circuit layout implementation, low on-chip passive component ratio is taken as a rule of thumb.The biased design is validated by simulations executed in LT SPICE program for TSMC 0.18 $\mu$m design technology.

The chapter is organized as follows: In Section 5.1, six real pole core filters which may be considered as raw circuits, as well as a complex pole filter are given. Moreover, non-ideal analysis is included. Section 5.2 gives the selected design with simulation results, layout and non-ideality analysis. In Section 5.3 tunability is discussed. Finally Section 5.4 is the conclusion section.

## 5.1. The Design Procedure for Voltage Mode Filters

Figure [5.1-5.7] demonstrate core filter designs. They consist of three MOSFETs and two capacitors. Transfer functions ignoring MOSFET internal capacitances are obtained to show the relationship between input signal $v_{in}$ and output signal $v_{out}$. Equation [5.1-5.7] correspond to core designs given in Figure [5.1-5.7], i.e. Equation 5.1 is for the circuit in Figure 5.7.

$$TF_1 = \frac{C_1 g_{m2} s}{g_{m2}\left(g_{m1}+g_{m3}\right)+\left(\left(C_1+C_2\right)\left(g_{m1}+g_{m3}\right)+C_1 g_{m2}\right)s+C_1 C_2 s^2} \tag{5.1}$$

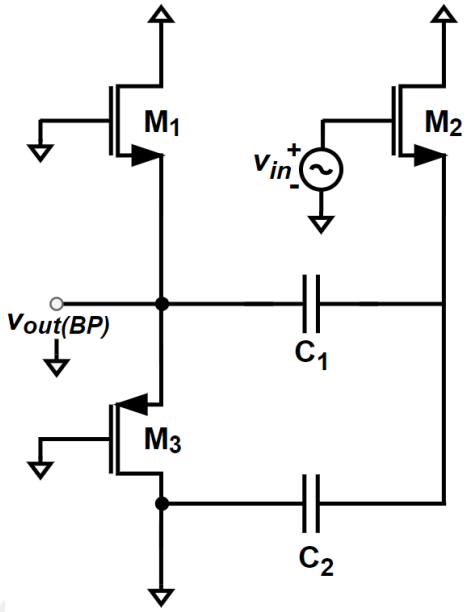


Figure 5.1. 1st proposed voltage mode filter design core.

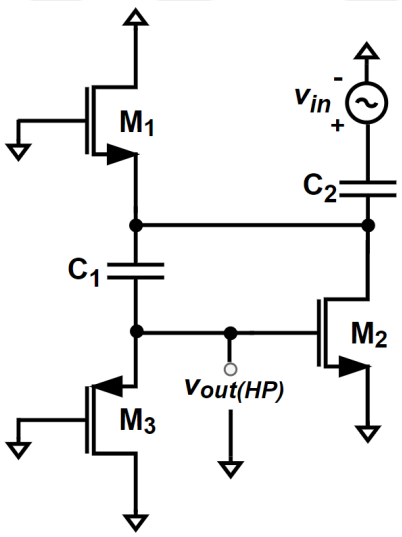


Figure 5.2. 2nd proposed voltage mode filter design core.

$$TF_2 = \frac{C_1 C_2 s^2}{g_{m1} g_{m3} + \left(C_1 \left(g_{m1} + g_{m2}\right) + \left(C_1 + C_2\right) g_{m3}\right) s + C_1 C_2 s^2} \tag{5.2}$$

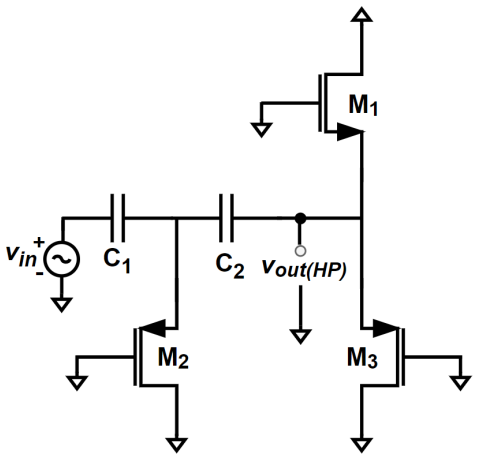


Figure 5.3. 3rd proposed voltage mode filter design core.

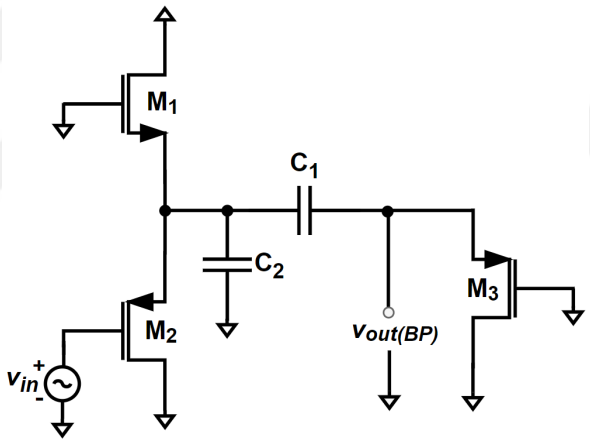


Figure 5.4. 4th proposed voltage mode filter design core.

$$TF_3 = \frac{C_1 C_2 s^2}{g_{m2}\left(g_{m1}+g_{m3}\right)+\left(\left(C_1+C_2\right)\left(g_{m1}+g_{m3}\right)+C_2 g_{m2}\right)s+C_1 C_2 s^2} \tag{5.3}$$

$$TF_4 = \frac{C_1 g_{m2} s}{g_{m3}\left(g_{m1}+g_{m2}\right)+\left(C_1\left(g_{m1}+g_{m2}+g_{m3}\right)+C_2 g_{m3}\right)s+C_1 C_2 s^2} \tag{5.4}$$

$$TF_5 = \frac{C_2 g_{m1} s}{g_{m1}\left(g_{m2}+g_{m3}\right)+\left(\left(C_1+C_2\right)\left(g_{m2}+g_{m3}\right)+C_2 g_{m1}\right)s+C_1 C_2 s^2} \tag{5.5}$$

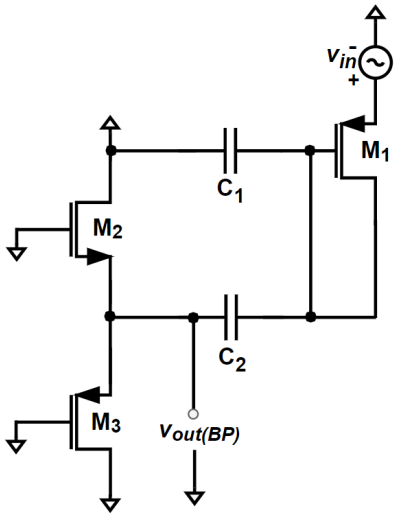


Figure 5.5. 5th proposed voltage mode filter design core.

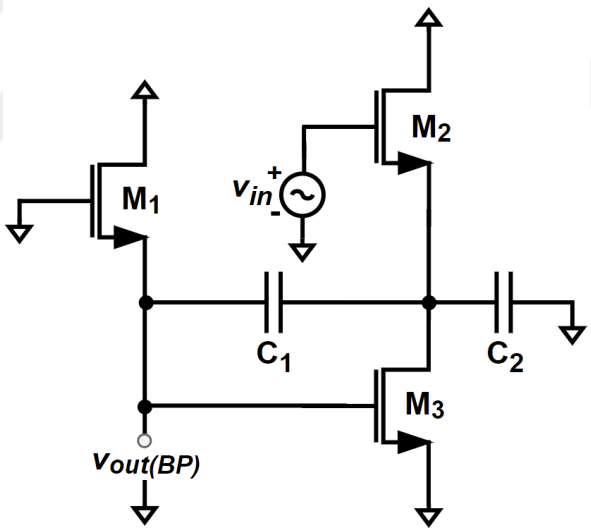


Figure 5.6. 6th proposed voltage mode filter design core.

$$TF_6 = \frac{C_1 g_{m2} s}{g_{m1} g_{m2} + \left(C_1 \left(g_{m1} + g_{m2} + g_{m3}\right) + C_2 g_{m1}\right) s + C_1 C_2 s^2} \tag{5.6}$$

$$TF_7 = \frac{C_1 C_2 s^2}{g_{m1} \left(g_{m2} + g_{m3}\right) + \left(\left(C_1 + C_2\right) g_{m1} + C_2 g_{m3}\right) s + C_1 C_2 s^2} \tag{5.7}$$

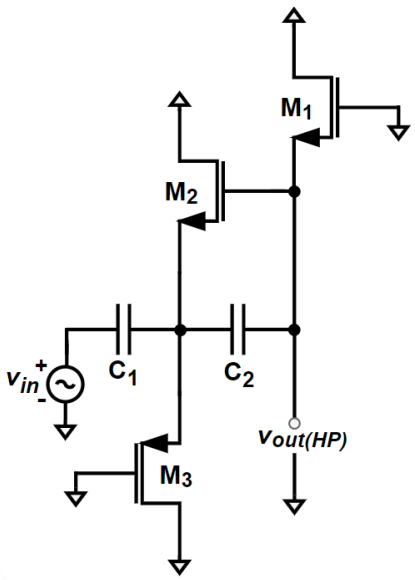


Figure 5.7. 7th proposed voltage mode filter design core.

After providing ideal transfer functions for seven different core designs, we can evaluate $\omega_0$ and $Q$ in terms of transconductance $g_m$ and on-chip capacitances. The general equations for transfer functions of $TF_{BP}(s)$, $TF_{LP}(s)$ , and $TF_{HP}(s)$ are in the form of Equation 2.3, 2.4, and 2.5, respectively. Equations [5.8-5.14] provide formulas of $\omega_0$ and $Q$ for transfer functions given for Figure [5.1-5.7] respectively, i.e. Equation 5.9 for the design presented in Figure 5.2. The well-known relation between transfer function coefficients and $\omega_0$, $Q$ values are shown in Equation [2.3-2.5] and Equation 2.6 for easy comparison. According to these equations, only the design demonstrated in Figure 5.7 allows complex pole responses, which is an exclusive feature of active filters. However, other topologies are also given to accomplish resistorless MOSFET-C based circuits to replace corresponding passive ones, or one can use them in a feedback loop to move their poles to complex plane. Circuits in Figure 5.2 and 5.3 are high-pass type and applying negative feedback can move the poles to the complex plane. The circuits in Figure 5.1, 5.4, 5.5, 5.6 are band-pass type and integrating type feedback would be necessary for them. Detailed information about this issue is given in Appendix B. The design procedure for them is kept out of the scope of this thesis. However they are included here for the sake of completeness. We will present the complete design for

circuit in Figure 5.7.

$$\omega_{0_1} = \sqrt{\frac{g_{m2}\left(g_{m1}+g_{m3}\right)}{C_1C_2}}\ , \quad Q_1 = \sqrt{\frac{C_1C_2g_{m2}\left(g_{m1}+g_{m3}\right)}{\left(\left(C_1+C_2\right)\left(g_{m1}+g_{m3}\right)+C_1g_{m2}\right)^2}} \tag{5.8}$$

$$\omega_{0_2} = \sqrt{\frac{g_{m1}g_{m3}}{C_1C_2}}\ , \quad Q_2 = \sqrt{\frac{C_1C_2g_{m1}g_{m3}}{\left(C_1\left(g_{m1}+g_{m2}\right)+\left(C_1+C_2\right)g_{m3}\right)^2}} \tag{5.9}$$

$$\omega_{0_3} = \sqrt{\frac{g_{m2}\left(g_{m1}+g_{m3}\right)}{C_1C_2}}\ , \quad Q_3 = \sqrt{\frac{C_1C_2g_{m2}\left(g_{m1}+g_{m3}\right)}{\left(\left(C_1+C_2\right)\left(g_{m1}+g_{m3}\right)+C_2g_{m2}\right)^2}} \tag{5.10}$$

$$\omega_{0_4} = \sqrt{\frac{g_{m3}\left(g_{m1}+g_{m2}\right)}{C_1C_2}}\ , \quad Q_4 = \sqrt{\frac{C_1C_2g_{m3}\left(g_{m1}+g_{m2}\right)}{\left(C_1\left(g_{m1}+g_{m2}+g_{m3}\right)+C_2g_{m3}\right)^2}} \tag{5.11}$$

$$\omega_{0_5} = \sqrt{\frac{g_{m1}\left(g_{m2}+g_{m3}\right)}{C_1C_2}}\ , \quad Q_5 = \sqrt{\frac{C_1C_2g_{m1}\left(g_{m2}+g_{m3}\right)}{\left(\left(C_1+C_2\right)\left(g_{m2}+g_{m3}\right)+C_2g_{m1}\right)^2}} \tag{5.12}$$

$$\omega_{0_6} = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}\ , \quad Q_6 = \sqrt{\frac{C_1C_2g_{m1}g_{m2}}{\left(C_1\left(g_{m1}+g_{m2}+g_{m3}\right)+C_2g_{m1}\right)^2}} \tag{5.13}$$

$$\omega_{0_7} = \sqrt{\frac{g_{m1}\left(g_{m2}+g_{m3}\right)}{C_1C_2}}\ , \quad Q_7 = \sqrt{\frac{C_1C_2g_{m1}\left(g_{m2}+g_{m3}\right)}{\left(\left(C_1+C_2\right)g_{m1}+C_2g_{m3}\right)^2}} \tag{5.14}$$

The circuit given in Figure 5.7 is biased properly to verify circuit operation and obtained transfer functions. Figure 5.8 provides details of how voltage and current sources are connected to the core design. $V_1$ is mainly deployed to set saturation

condition for $M_1$. Since neither gate of $M_2$ nor $C_2$ allow DC current flow originating from $M_1$, $I_{B1}$ create a way for current. Because both $I_{B1}$ and $V_1$ have a serious effect on the gate voltage of $M_2$, $V_1$ should be chosen a relatively larger value and $I_{B1}$ should be small. By applying this method, high gate voltage of $M_2$ can be obtainable, then saturation condition could be easily applicable for both $M_1$ and $M_2$. Since on-chip capacitances of $C_1$ and $C_2$ do block DC source current flow of $M_2$, $M_3$ sets a current passing way through itself by implying as a current source. $I_{B2}$ leads current flow over $M_4$, then required current source for $M_{2,3}$ is acquired.

Having set voltage and current sources as shown in Table 5.2, we get $g_{m1}$, $g_{m2}$, $g_{m3}$, and $g_{m4}$ as 46.4 $\mu$A/V, 355 $\mu$A/V, 54.7 $\mu$A/V, and 227 $\mu$A/V respectively. As Equation 5.14 suggests, setting relatively larger $g_{m2}$ than other $g_m$'s allows a designer to increase $Q$ of the filter. High-pass filters with underdamped response, i.e. $Q$ >0.5, exhibit quick transient response. Since on-chip capacitor value ratios are generally preferred not to be much larger than unity, denoted as component spread, we have set $C_1$ as 20 pF and $C_2$ as 10 pF. After having applied $g_m$ values presented in Table 5.3, we get $f_c$ and $f_0$ as 1.21 MHz and 1.55 MHz respectively. Furthermore, $Q$ is calculated as 1.005.

### 5.1.1. Non-Ideal Analysis of Selected and Biased Voltage Mode Filter Design

To elaborate circuit response by considering internal non-ideal factors of MOSFET, we take resistive and capacitive components into account. Such component values, presented in Table 5.1, should be inserted on the transfer function provided in Equation 5.15. This equation is denoted as "exact", because there is no simplification applied on it.

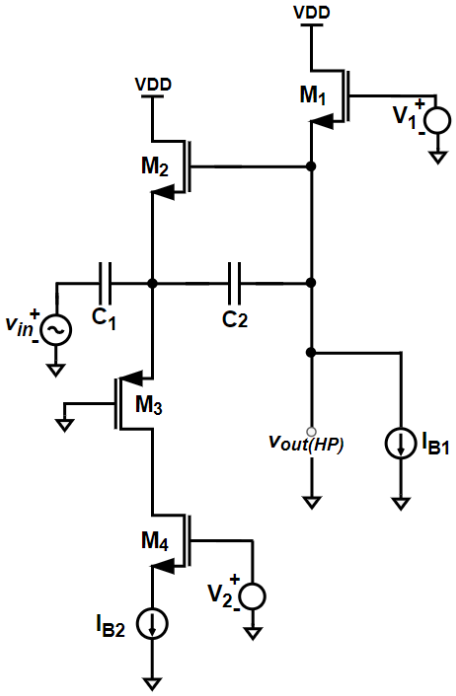


Figure 5.8. 7th proposed voltage mode filter design with biasing.

$$TF_{7\ exact} = \frac{C_1(C_2 + C_{gs2})s^2}{\begin{array}{c} g_{ds1}\left(g_{ds2} + g_{ds3} + g_{m2} + g_{m3}\right) + \\ g_{m1}\left(g_{ds2} + g_{ds3} + g_{m2} + g_{m3}\right) + \\ \left(\left(C_1 + C_2 + C_{gs2} + C_{gs3}\right)\left(g_{ds1} + g_{m1}\right)\right. \\ \left(C_2 + C_{gd2} + C_{gs1} + C_{gs2}\right)\left(g_{ds2} + g_{ds3} + g_{m3}\right) \\ \left.\left(C_{gd2} + C_{gs1}\right) g_{m2}\right)s + \\ \left(C_1\left(C_2 + C_{gs1} + C_{gs2} + C_{gd2}\right) + \right. \\ \left(C_2 + C_{gs2}\right)\left(C_{gd2} + C_{gs1} + C_{gs3}\right) + \\ \left.C_{gs3}\left(C_{gd2} + C_{gs1}\right)\right)s^2 \end{array}} \tag{5.15}$$

Similarly exact $\omega_0$ and $Q$ equations are given in Equation 5.16 and Equation 5.17 respectively.

$$\omega_{0_exact} = \sqrt{\frac{\begin{array}{c} g_{ds1}\left(g_{ds2}+g_{ds3}+g_{m2}+g_{m3}\right)+ \\ g_{m1}\left(g_{ds2}+g_{ds3}+g_{m2}+g_{m3}\right) \end{array}}{\begin{array}{c} C_1\left(C_2+C_{gs1}+C_{gs2}+C_{gd2}\right)+ \\ \left(C_2+C_{gs2}\right)\left(C_{gd2}+C_{gs1}+C_{gs3}\right)+ \\ C_{gs3}\left(C_{gd2}+C_{gs1}\right) \end{array}}} \tag{5.16}$$

$$Q_{exact} = \sqrt{\frac{\begin{array}{c} \left(g_{ds1}\left(g_{ds2}+g_{ds3}+g_{m2}+g_{m3}\right)+ \right. \\ g_{m1}\left(g_{ds2}+g_{ds3}+g_{m2}+g_{m3}\right) \\ \left(C_1\left(C_2+C_{gs1}+C_{gs2}+C_{gd2}\right)+ \right. \\ \left(C_2+C_{gs2}\right)\left(C_{gd2}+C_{gs1}+C_{gs3}\right)+ \\ \left. C_{gs3}\left(C_{gd2}+C_{gs1}\right)\right) \end{array}}{\begin{array}{c} \left(\left(C_1+C_2+C_{gs2}+C_{gs3}\right)\left(g_{ds1}+g_{m1}\right)\right. \\ \left(C_2+C_{gd2}+C_{gs1}+C_{gs2}\right)\left(g_{ds2}+g_{ds3}+g_{m3}\right) \\ \left.\left(C_{gd2}+C_{gs1}\right)g_{m2}\right)^2 \end{array}}} \tag{5.17}$$

To evaluate transfer function or $\omega_0$ and $Q$ values, presented in Equation [5.15-5.17] of biased design, one has to obtain $C_{gs}$, $C_{gd}$, and $g_{ds}$ values. The effect of $C_{sb}$ is eliminated, because source and bulk nodes of transistors are connected each to other. The calculation methods and required technology related parameters are presented in Chapter 1. As a result, internal capacitance and $g_{ds}$ parameter values can be observed in Table 5.1 and Table 5.3. By inserting this parameter values into Equation [5.15-5.17], we calculated $f_c$ and $f_0$ as 1.21 MHz and 1.52 MHz respectively. Besides that, $Q$ is calculated as 0.97.

### 5.1.2. Tunability Feature Observation of the Biased Voltage mode Filter Circuitry

By considering parameter values in the transfer function shown in Equation 5.15, it is possible to apply some approximations to simplify non-ideal analysis results. This will allow a more intuitive understanding of equations. Hence a more practical design approach can be followed by a designer. We have set $C_{1,2}$ relatively larger than internal MOS capacitance values to achieve larger $Q$. therefore, $C_{1,2} \gg C_{gs,gd}$. Moreover, as a general rule, $g_m \gg g_{ds}$ and due to a design choice $C_{gs2} \gg C_{gs3}$. Thus, one can obtain simplified, versions of $\omega_{0_exact}$ and $Q_{exact}$ as stated in Equation 5.18 and Equation 5.19, respectively. Since we have chosen relatively large $C_{1,2}$, simplified expressions of $\omega_0^{'}$ and $Q^{'}$ reduce to the ones stated in Equation 5.14 as expected.

$$\omega_0^{'} \approx \sqrt{\frac{g_{m1}\left(g_{m2}+g_{m3}\right)}{C_1 C_2}} \tag{5.18}$$

$$Q^{'} \approx \sqrt{\frac{C_1 C_2 g_{m1}\left(g_{m2}+g_{m3}\right)}{\left(\left(C_1+C_2\right)g_{m1}+C_2 g_{m3}\right)^2}} \tag{5.19}$$

Now assume $C_1 / C_2 = \alpha$ , and $g_{m1} / g_{m3} = \beta$ are constant ratios. Then Equation 5.18 and 5.19 turn into Equation 5.20 and 5.21, which give an insight for a designer on choosing parameter sizes for tuning the filter. As Equation 5.21 suggests, larger $M_2$ device leads higher $Q$ achievement. Moreover, it is possible to adjust $\omega_0$ without affecting $Q$ significantly by relying on Equation 5.20. To that end, tuning the biased design is feasible by changing $I_{B1}$ and $I_{B2}$ at the same ratio.

$$\omega_0^{'} \approx \frac{g_{m3}}{C_2}\sqrt{\frac{\beta\left(g_{m2}/g_{m3}+1\right)}{\alpha}} \tag{5.20}$$

$$Q' \approx \sqrt{\frac{\alpha\beta\left(g_{m2}/g_{m3}+1\right)}{\left(\left(\alpha+1\right)\beta+1\right)^2}} \tag{5.21}$$

The above-mentioned transistor parameters can be taken from Table 5.3 which are obtained under saturation conditions for both NMOS and PMOS transistors, with proper bias conditions we have applied.

Table 5.1. Internal Capacitance of Voltage Mode Filter MOSFET's.

| **Comp.** | $\mathbf{C_{gs}}$**(fF)** | $\mathbf{C_{gd}}$**(fF)** | $\mathbf{C_{sb}}$**(fF)** |
|---|---|---|---|
| $\mathbf{M_1}$ | 109.07 | 14.2 | 0 |
| $\mathbf{M_2}$ | 327.3 | 42.7 | 0 |
| $\mathbf{M_3}$ | 10.63 | 1.14 | 0 |
| $\mathbf{M_4}$ | 218.13 | 28.4 | 0 |

Table 5.2. Bias Conditions for the filter in Figure 5.8.

| $\mathbf{V_{DD}}$**(V)** | $\mathbf{V_1}$**(V)** | $\mathbf{V_2}$**(V)** | $\mathbf{I_{B1}}$**(**$\mu$**A)** | $\mathbf{I_{B2}}$**(**$\mu$**A)** |
|---|---|---|---|---|
| 1.8 | 1.8 | 0.2 | 2 | 16.4 |

Table 5.3. Transistor parameters for the circuit in Figure 5.8.

| | **Type** | **W(**$\mu$**m)** | **L(**$\mu$**m)** | $\mathbf{\lvert V_{Th}\rvert}$ | $\mathbf{g_m}$**(**$\mu$**A/V)** | $\mathbf{g_{ds}}$**(**$\mu$**A/V)** |
|---|---|---|---|---|---|---|
| $\mathbf{M_1}$ | N | 18 | 0.9 | 0.372 | 46.4 | 0.411 |
| $\mathbf{M_2}$ | N | 54 | 0.9 | 0.372 | 355 | 2.9 |
| $\mathbf{M_3}$ | P | 1.8 | 0.9 | 0.396 | 54.7 | 0.639 |
| $\mathbf{M_4}$ | N | 36 | 0.9 | 0.372 | 227 | 4.6 |

## 5.2. Simulations for Proposed Voltage Mode Circuitry

To verify theoretical analysis proposed in previous section, we need to perform small signal AC and time domain transient analysis on LT SPICE simulator via apply-

ing bias conditions expressed in Table 5.2. Hence, we can compare calculated results and simulations with the regard of making predictions on deviations from expected results. In real implementation, factors could deteriorate circuit performance by affecting passive component values and active component design sizes. Even under such harsh conditions, the circuit should perform satisfactorily and maintain its expected response as much as possible. To insert physical errors into design process, we have applied Monte Carlo analysis by introducing 5% error for both length and width of MOSFETs and on-chip capacitances of $C_1$ and $C_2$. Besides that, environmental conditions could cause that the design does not behave in expected manner. Since one of the most common environmental issue on MOS-based design is temperature effect, we observed the frequency response by altering temperature from $0^o$ Celsius until $100^o$ Celsius with the increment of $1^o$ Celsius. Since all of designs are modeled by assuming active elements to operate in saturation region, one must ensure that increasing the input signal level should not drive one of the transistors out of the saturation region. Moreover, significant distortion may occur at the edges of saturation region. Hence we have adopted 5% THD ratio as a maximum allowable limit to plot the THD graph. To detect the linear operation limits, we have simulated THD analysis on LT SPICE by increasing peak-to-peak input AC voltage starting from 2 mV with 3 mV increments up to 50 mV.

This section mainly expresses small signal AC simulation results and comparisons between calculated results for the proposed design in Figure 5.8. According to LT SPICE simulation results, $f_c$ and $f_0$ are obtained as 1.18 MHz and 1.44 MHz, respectively. Furthermore, $Q$ is obtained as 0.917 via simulations. By deploying Equation 5.7 and Equation 5.14, we have calculated $f_c$, $f_0$, and $Q$ as 1.21 MHz, 1.55 MHz, and 1.005, respectively. An additional approach is derived by including non-ideal MOS factors, hence after utilizing Equation 5.15, 5.17, and 5.16 we get $f_c$, $f_0$, and $Q$ as 1.21 MHz, 1.52 MHz, and 0.97, respectively. As a result, we can conclude that theoretical calculations match simulation results in a quite acceptable manner. Frequency domain response is demonstrated in Figure 5.11 explicitly. Since $f_0$ corresponds to where $90^o$ phase change occurs, with respect to low frequency phase, we have also included phase

Table 5.4. Comparison of Ideal, Biased Design Calculated, Biased Design Simulated, and Layout HP Voltage Mode Filter Results.

| **Spec.** | **Ideal Calculated Results** | **Biased Design Calculated Results** | **Biased Design Sim. Results** | **Post Layout Sim. Results** |
|---|---|---|---|---|
| $\mathbf{f_c}$ | 1.21 MHz | 1.21 MHz | 1.18 MHz | 1.19 MHz |
| **HP Gain** | 0 dB | -0.2 dB | -0.13 dB | -0.16 dB |
| $\mathbf{f_0}$ | 1.55 MHz | 1.52 MHz | 1.44 MHz | 1.45 MHz |
| **Q** | 1.005 | 0.97 | 0.917 | 0.922 |

response of the biased design.

Additional to SPICE simulations, circuit layout gives details of chip area and deviations caused by real implementation steps. We prefer to use Magic VLSI design tool to get circuit layout and corresponding small signal AC analysis. Since the design contains the capacitance of $C_2$ between floating nodes, we have to implement it. On the other hand, $C_1$ is connected between input node and $C_2$, shown in Figure 5.8, so it can be added as a passive element into the circuit. As a design choice, $C_2$ is obtained by deploying an NMOS device as a capacitive element ($M_{cap}$) by setting width and length of it 66.15 $\mu$m and 49.5 $\mu$m respectively, then the design turns into one demonstrated in Figure 5.9. Furthermore, whole chip, depicted in Figure 5.10, has the dimensions of 64.2 $\mu$m x 69 $\mu$m. According to the post layout simulation results, we have obtained $f_c$, $f_0$, and $Q$ as 1.19 MHz, 1.45 MHz, and 0.922, respectively. To sum up, post-layout simulation results have a promising agreement with pre-layout ones. Furthermore, according to simulation results demonstrated in Figure 5.11 the circuit is able to operate in a quite broad frequency range, which could be handled by the direct capacitive path, established by $C_1$ and $C_2$, between input and output nodes.

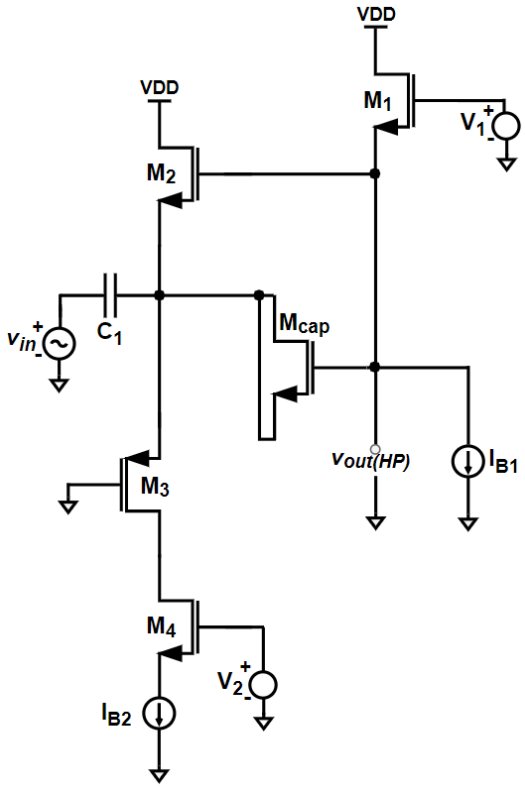


Figure 5.9. On-chip capacitance implemented version of the design in Figure 5.8

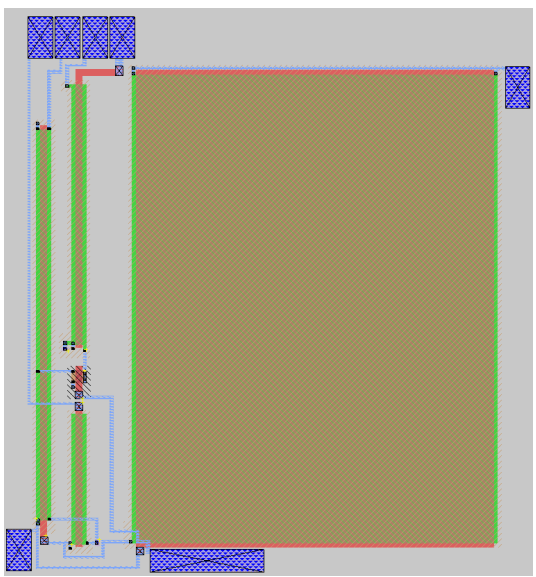

Figure 5.10. Layout of the design in Figure 5.9

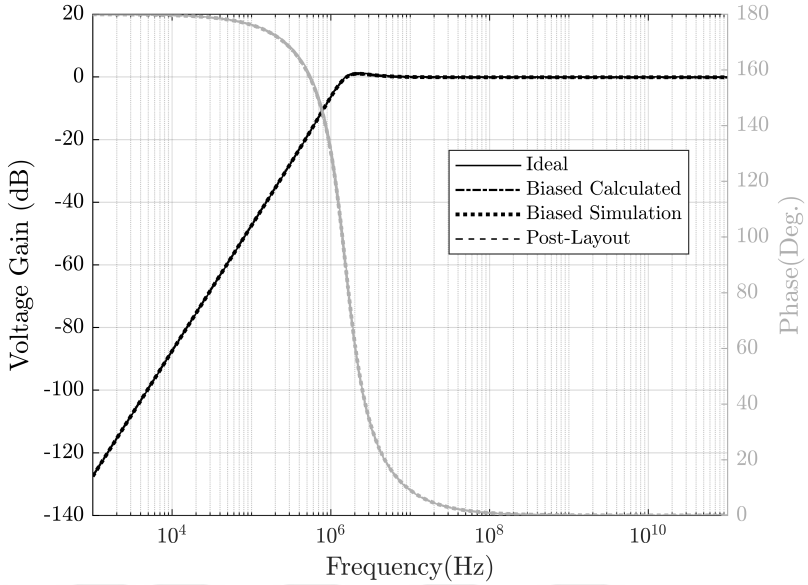


Figure 5.11. Frequency domain response of high-pass voltage mode design.

In addition to frequency response evaluation, we examine whether biased design gives acceptable time domain response under bias conditions in Table 5.2. After running transient analysis at the central frequency of the filter, we get time domain responses showing there is a 90° phase difference between input and output voltages. Moreover, since $Q$ is approximately unity, the system reaches steady state condition readily and exhibits oscillatory behaviour as represented in Figure 5.12.

According to simulation results provided in Figure 5.13, a designer is able to apply 50 mV small signal AC input without violating this design specification. Since even harmonics have serious effect on THD, we shall eliminate them. To that end, differential-ended configuration is applied for the design in the Figure 5.8. As a result, THD for 50 mV input is lowered to about 1%.

As it is stated previously, one of the most real-life challenging factor is temperature effect which could cause the circuit to exhibit unacceptable deviation from ideal response. To that end, we need to investigate frequency response at different temperatures. Accordingly, we apply simulation with temperature from 0° Celsius until 100°

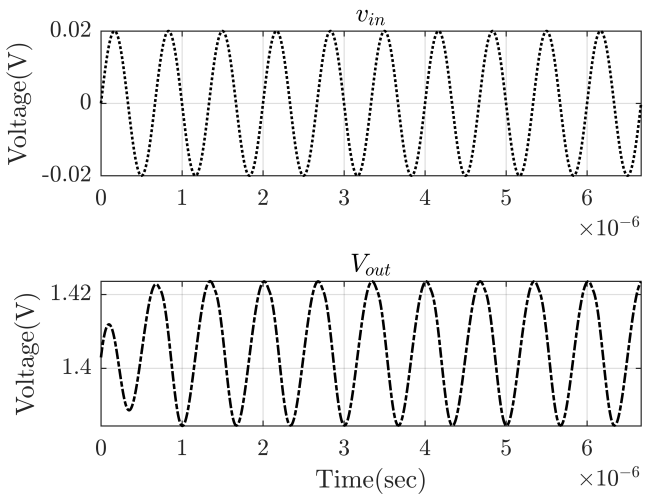


Figure 5.12. Time domain response of high-pass voltage mode design.

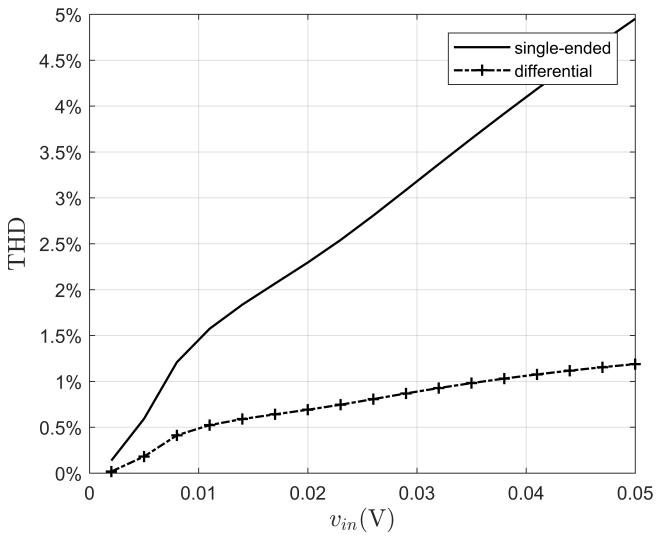


Figure 5.13. THD analysis of high-pass voltage mode design for single-ended and differential mode configurations.

Celsius with the increment of 1° Celsius.

Similar to external factors, non-deterministic steps in implementation processes should be taken into account to cover possible errors and their effects. Monte Carlo

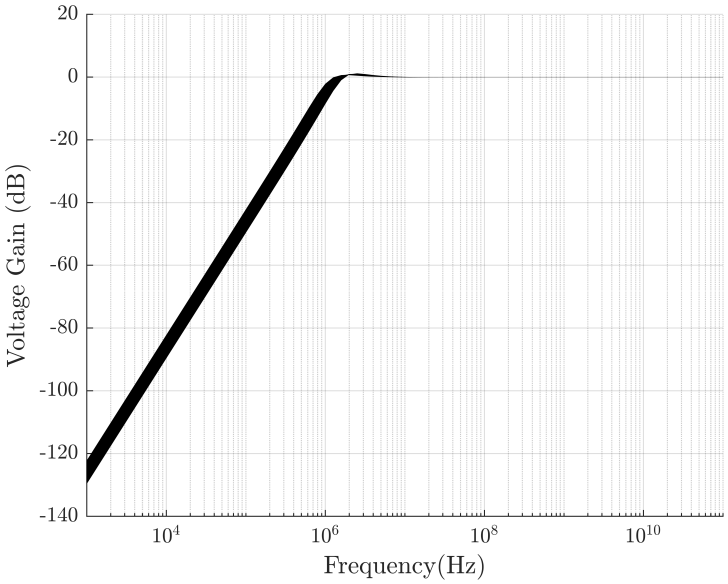


Figure 5.14. Temperature analysis of high-pass voltage mode design.

analysis gives an insight for a designer by allowing him to insert random deviations in circuit design parameters. For this purpose, W and L parameters of transistors and on-chip capacitances' values are diverted up to 5% and executed 200 times.

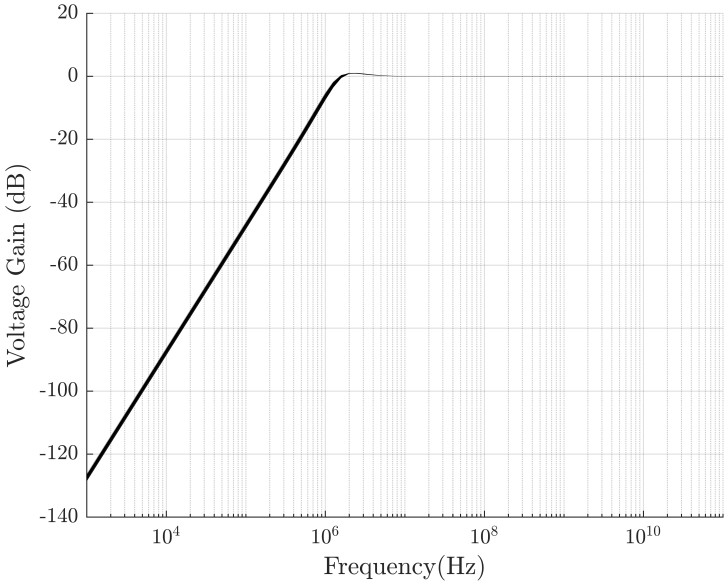


Figure 5.15. Monte Carlo analysis of high-pass voltage mode design.

### 5.3. Simulations for Tuning the Proposed High-Pass Filter

As the Equation 5.21 suggests, we can keep $Q$ unaffected by changing $I_{B1}$ and $I_{B2}$ at the same ratio while switching $f_0$. To that end, we apply 3 different bias conditions by setting $I_{B1}$-$I_{B2}$ pair as 2$\mu$-18$\mu$A, 3$\mu$-27$\mu$A, and 4$\mu$-36$\mu$A. According to simulation results shown in Figure 5.16, circuit response shifts in frequency domain while preserving $Q$. By deducing from simulation results, $f_0$ is altered as 1.598 MHz, 2.254 MHz, and 2.917 MHz by corresponding $Q$ values of 0.985, 0.984, and 0.984, respectively, for proposed current bias conditions. Furthermore, it is observed that $f_c$, also, could be tuned as 1.249 MHz, 1.794 MHz, and 2.323 MHz.

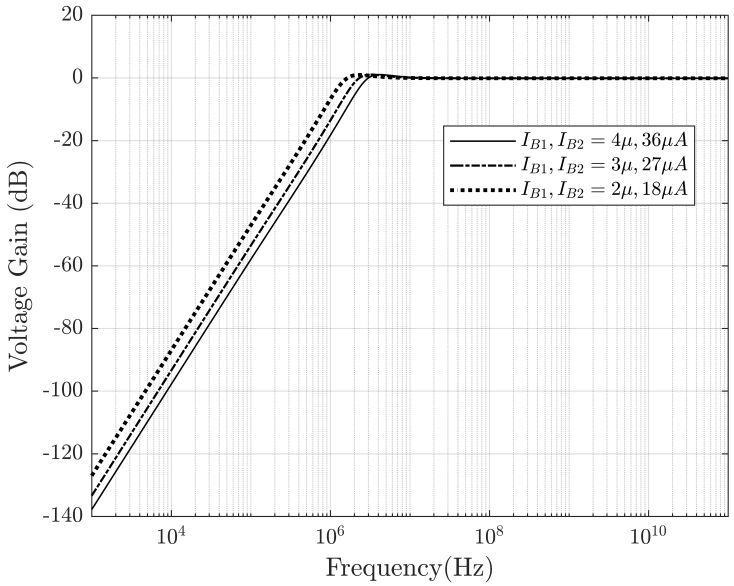


Figure 5.16. High-pass filter results for various bias conditions.

### 5.4. Conclusion for Voltage Mode Filter Design

In this part of the thesis, we presented seven raw core MOSFET-C voltage mode filters, gave their corresponding transfer functions with $\omega_0$ and $Q$ equations. One of the circuits permit complex poles and therefore is suitable to be used directly after biasing in active filter applications. The remaining core circuits are real pole filters,

they are included for the sake of completeness and it is suggested that their poles can be moved to complex plane with additional feedback circuits. Furthermore, non-ideal analysis, including MOSFET internal parasitics, was performed. One selected circuit with high-pass response is biased and the complete design process is presented. Both of its capacitors forming a feedforward path from input to output is the unique property of the filter which therefore shows virtually infinite bandwidth. Since tuning is achieved by simple bias current alterations, the circuit has a broad range of applications.

In order to verify mathematical analysis, LT SPICE was executed with TSMC 180 nm parameters. Moreover, post-layout simulations were carried out for the high-pass MOSFET-C filter by deploying MOSFET-based on-chip capacitance. According to results, paper-based analysis fits both pre and post-layout simulations.

# 6. CONCLUSION

Conventional analog active filters are mainly designed using standard active elements such as OPAMPs, OTAs, current conveyors and similar components. These types of designs, generally, deploy external resistances and capacitances, which results in both high energy consumption and a need for a large chip area although fully integrated versions are also available. On the other hand, all of the filters presented in this thesis mainly utilize active components and poly-silicon made capacitances. Furthermore, required resistive effects are obtained by transistor transconductances of $g_m$ . Such methodology, also, is called as MOSFET-C design approach. In this technique, on-chip capacitances are added to alleviate the effect of internal MOSFET capacitances of $C_{gs}$ and $C_{gd}$. All mentioned design steps in the thesis are not difficult to apply in fabrication of the chips. Since transistor bias point shifts can be used for electronic adjustments, it is possible to alter filter specifications without introducing new components. To explore such application range of presented filters, transfer functions were elaborated in terms of tunability feature and verified by running LT SPICE simulations. By relying on these analog design basics, four different mode filters defined in terms of their voltage and current input/output relations, namely current mode, transimpedance mode, transadmittance mode, and voltage mode circuits were designed and proposed.

In the Chapter 2, a dual-mode current mode MOSFET-C filter was introduced. Besides, since current mode addition requires no extra circuitry, the design is capable of feeding output current back. Thus, it is possible to achieve agility by setting a closed loop control path with various gain adjustments via switches. By pursuing this approach, we have proposed an agile filter application which is able to be tuned for $f_0$ quickly.

Transimpedance filter designs are demonstrated in Chapter 3. In this part, we, also, selected one of the filters to bias and tune. Having obtained equations for $\omega_0$

and $Q$, we checked whether the biased design simulation fits theoretical calculations. Additionally, we verified that it is possible to achieve $f_0$ switching without affecting bandwidth significantly. From this point of view, the conditions to be satisfied for tuning were expressed in detail.

Having higher $Q$, gives an opportunity making a band-pass filter more frequency selective. One of the presented transadmittance designs in Chapter 4 can meet such criteria by achieving $Q$ value of 5. By relying upon transfer functions, we examined whether the design permits electronic adjustments. To illustrate the possibility of tuning, a method was shown to keep $f_0$ unaffected while changing bandwidth under various bias conditions. All of the hand calculation and simulation results are presented explicitly in both tabulated and graphical form.

Voltage mode filters were provided in Chapter 5. In this part of the thesis, a filter showing high-pass response was selected for circuit tuning and biased properly. The filter parameter adjustment is applicable for $f_0$ tuning without changing $Q$ significantly. Since tuning is achieved by simple bias current alterations, the circuit has a broad range of application. Furthermore, since the presented design has a capacitive feedforward path between input and output, it exhibits virtually infinite bandwidth. The voltage mode filter was verified with both SPICE-based and post-layout simulations.

As a conclusion, this thesis comprises four different mode core filters with necessary design equations. Our main approach could be modeled as the following: design the core circuitry, perform theoretical analysis, explore tuning opportunities by relying on the analysis, bias the tuning-friendly core filter, and verify the functionality of the completed design. Thanks to the mathematical analysis presented for filters, any researcher could reevaluate core designs for future deployment possibilities.

# REFERENCES


1. Sedra, A. S. and K. C. Smith, *Microelectronic circuits*, Oxford University Press, New York, 2004.

2. Baker, R., *CMOS Circuit Design, Layout, and Simulation*, Wiley-IEEE Press, Hoboken, New Jersey, 2010.

3. Arslan, E., B. Metin and O. Cicekoglu, "MOSFET-only multi-function biquad filter", *AEU-International Journal of Electronics and Communications*, Vol. 69, No. 12, pp. 1737–1740, 2015.

4. Yildiz, H., S. Ozoguz, A. Toker and O. Cicekoglu, "On the realization of MOS-only allpass filter", *Circuits, Systems, and Signal Processing*, Vol. 32, No. 3, pp. 1455–1465, 2013.

5. Aydin, O., H. Yildiz and S. Ozoguz, "MOS-only complex filter design for dual-band GNSS receivers", *AEU-International Journal of Electronics and Communications*, Vol. 82, pp. 83–92, 2017.

6. Cicekoglu, O., N. Herencsar and B. Metin, "Supplementary MOS-only Butterworth LP BP filter circuits", *24th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 194–197, 2017.

7. Yesil, A., D. Ozenli, E. Arslan and H. Kuntman, "Current mode single-input multi-output MOSFET-only filter", *AEU-International Journal of Electronics and Communications*, Vol. 80, pp. 157–164, 2017.

8. Uygur, A., B. Metin, H. Kuntman and O. Cicekoglu, "Current mode MOSFET-only third order Butterworth low pass filter with DTMOS tuning technique", *Analog Integrated Circuits and Signal Processing*, Vol. 89, pp. 645–654, 2016.

9. H.A.Yildiz, "MOS-only polyphase filter with small chip area", *Analog Integrated Circuits and Signal Processing*, Vol. 97, pp. 59–68, 2018.

10. Metin, B., O. Cicekoglu and S. Ozoguz, "A class of MOSFET-C multifunction filters", *Analog Integrated Circuits and Signal Processing*, Vol. 97, pp. 5–13, 2018.

11. Atasoyu, M., B. Metin, H. Kuntman and O. Cicekoglu, "Simple realization of a third order Butterworth filter with MOS-only technique", *AEU International Journal of Electronics and Communications*, Vol. 81, pp. 205–208, 2017.

12. Ozenli, D., E. Alaybeyoglu, H. Kuntman and O. Cicekoglu, "MOSFET-Only filter design automation based on polynomial regression with exemplary circuits", *AEU-International Journal of Electronics and Communications*, Vol. 84, pp. 342–354, 2018.

13. Lakys, Y. and A. Fabre, "Shadow filters –new family of second order filters", *Electronics Letters*, Vol. 46, No. 4, pp. 276–277, 2010.

14. Alaybeyoglu, E., M. Atasoyu and H. Kuntman, "Frequency agile filter structure improved by MOS-only technique", *Telecommunications and Signal Processing (TSP), 38th International Conference on. IEEE*, pp. 55–61, 2015.

15. Safari, L., S. Minaei and B. Metin, "A low power current controllable single-input three-output current-mode filter using MOS transistors only", *AEU International Journal of Electronics and Communications*, Vol. 68, pp. 1205–1213, 2014.

16. Yildiz, H., A. Toker, A. Elwakil and S. Ozoguz, "MOS-only allpass filters with extended operating frequency range", *Analog Integrated Circuits and Signal Processing*, Vol. 81, No. 1, pp. 17–22, 2014.

17. Metin, B., H. Yildiz, O. Cicekoglu and S. Ozoguz, "A new class of MOSFET-C multifunction filters", *10th International Conference on Electrical and Electronics Engineering (ELECO)*, pp. 1235–1237, 2017.

18. Arslan, E., B. Metin, H. Kuntman and O. Cicekoglu, "MOS-only second order current-mode LP/BP filter", *Analog Integrated Circuits and Signal Processing*, Vol. 74, No. 1, pp. 105–109, 2013.

19. L. Tan, R. L. J. T., Q. Li, "Design of active transimpedance band-pass filters with different Q values", *International Journal of Electronics*, Vol. 100, No. 2, pp. 142–149, 2013.

20. B. Peg, M. S., S. Maheswari, "Digitally controlled fully differential voltage- and transadmittance-mode biquadratic filter", *IET Circuits Devices Syst.*, Vol. 7, No. 4, pp. 193–203, 2013.

21. N.A. Shah, S. I., M. Quadri, "CDTA based universal transadmittance filter", *Analog Integrated Circuits and Signal Processing*, Vol. 52, No. 1–2, pp. 65–69, 2007.

22. Babanezhad, J. and R. Gregorian, "A programmablegain/loss circuit", *IEEE Journal of Solid-State Circuits*, Vol. 22, No. 6, pp. 1082–1090, 1987.

23. Pul, J. and Y. Tsividis, "Transistor-only frequency selective circuits", *IEEEJ Solid-State Circuits*, Vol. 25, pp. 821–832, 1990.

24. Metin, B. and K. Pal, "Cascadable allpass filter with a single DO-CCII and a grounded capacitor", *Analog Integrated Circuits and Signal Processing*, Vol. 61, No. 3, pp. 259–263, 2009.

25. Horng, J. W., "Current conveyors based allpass filters and quadrature oscillators employing grounded capacitors and resistors", *Computers and Electrical Engineering*, Vol. 31, pp. 81–92, 2005.

26. Maheshwari, S., "High input impedance VM-APSs with grounded passive elements", *IET Circuits Devices Syst.*, Vol. 1, No. 1, pp. 72–78, 2007.

27. Maheshwari, S., "High input impedance voltage-mode first-order allpass sections",

*Int. J. Circuits Theory Appl.*, Vol. 36, No. 1, pp. 511–512, 2008.

28. Cam, U., O. Cicekoglu, M. Gülsoy and H. Kuntman, "New voltage and current mode first-order all-pass filters using single FTFN", *Frequenz*, Vol. 54, No. 7–8, pp. 177–179, 2000.

29. Metin, B. and O. Cicekoglu, "Component Reduced All-pass Filter with a Grounded Capacitor and High Impedance Input", *Int. Journal of Electronics*, Vol. 96, No. 5, pp. 445–455, 2009.

30. Khan, A. and S. Maheshwari, "Simple first order all-pass section using a single CCII", *Int. Journal of Electronics*, Vol. 87, No. 3, pp. 303–306, 2000.

31. Biolek, D. and V. Biolkova, "All- pass filters employing differential OpAmps", *Electronics World*, Vol. 116, No. 1891, pp. 44–45, 2010.

32. Toker, A., S.Ozcan, H. Kuntman and O. Cicekoglu, "Supplementary all-pass sections with reduced number of passive elements using a single current conveyor", *Int. Journal of Electronics*, Vol. 88, No. 9, pp. 969–976, 2001.

33. Higashimura, M. and Y. Fukui, "Realization of all-pass networks using a current Conveyor", *Int. Journal of Electronics*, Vol. 65, No. 2, pp. 249–250, 1988.

34. Biolek, D. and V. Biolkova, "First-order voltage-mode all- pass filter employing one active element and one grounded capacitor", *Analog Integrated Circuits and Signal Processing*, Vol. 65, No. 1, pp. 123–129, 2010.

35. Minaei, S. and E. Yuce, "Novel Voltage-Mode All-Pass Filter Based on Using DVCCs", *Journal of Circuits System Signal Process*, Vol. 29, pp. 391–402, 2010.

36. Pandey, N. and S. K. Paul, "All-pass filters based on CCII- and CCCII-", *Int. Journal of Electronics*, Vol. 91, No. 8, pp. 485–489, 2004.

37. Maheshwari, S., J. Mohan and D.S.Chauhan, "Voltage-mode cascadable all-pass sections with two grounded passive components and one active element", *IET Circuits, Devices  Systems*, Vol. 4, No. 2, pp. 113–122, 2010.

38. Torres, J. A. and J. C. Freire, "K Band SiGe HBT single ended active inductors", *Integration, the VLSI Journal*, Vol. 52, pp. 272–281, 2016.

39. Samiei, M. and O. Hashemipour, "Design of active inductor-based current-controlled oscillators using gm/Id methodology", *International Journal of Electronics and Communications (AEU)*, Vol. 87, pp. 1–9, 2018.

40. Pantoli, L., V. Stornelli and G. Leuzzi, "A low-voltage low-power 0.25 $\mu$m integrated single transistor active inductor-based filter", *Analog Integrated Circuits Signal Process*, Vol. 87, pp. 463–469, 2016.

41. Ou, J. and P. Ferreira, "Design considerations of CMOS active inductor for low power applications", *Analog Integrated Circuits Signal Process*, Vol. 89, pp. 1–10, 2017.

42. Saad, S., M. Mhiri, A. B. Hammadi and K. Besbes, "A new low-power, high-Q, wide tunable CMOS active inductor for RF applications", *IETE J. Res*, Vol. 62, pp. 265–273, 2016.

43. Tajalli, A., Y. Leblebici and E. Brauer, "Implementing ultra-high-value floating tunable CMOS resistors", *Electron. Lett.*, Vol. 44, No. 5, pp. 349–350, 2008.

44. Wang, Y., J. Chen and C. Chen, "Chebyshev Bandpass Filter Using Resonator of Tunable Active Capacitor and Inductor", *VLSI Design*, Vol. 2017, pp. 112–123, 2017.

45. Zito, D., D. Pepe and A. Fonte, "High-frequency CMOS active inductor: Design methodology and noise analysis", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, Vol. 23, No. 6, pp. 1123–1136, 2015.

46. Pantoli, L., V. Stornelli and G. Leuzzi, "Class AB tunable active inductor", *Electronics Letters*, Vol. 51, No. 1, pp. 65–67, 2015.

47. Prommee, P., A. Tiamsuphat and M. Abuelma'atti, "Electronically Tunable MOS-only Current-Mode High-Order Band-Pass Filters", *Turkish Journal Of Electrical Engineering And Computer Sciences*, Vol. 25, No. 2, pp. 1116–1136, 2017.

48. Göknar, C., M. Yıldız and S. Minaei, "Metamutator Applications: a Quadrature MOS-Only Oscillator and Transconductance / Transimpedance Amplifiers", *Analog Integrated Circuits and Signal Processing*, Vol. 89, No. 3, pp. 801–808, 2016.

49. Minaei, S. and E. Yuce, "High input impedance NMOS-based phase shifter with minimum number of passive elements", *Circuits, Systems and Signal Processing*, Vol. 31, pp. 51–60, 2012.

50. José, S. M., S. Michiel and W. Sansen, *High-Performance CMOS Continuous-Time Filters*, Springer, USA, 1993.

# APPENDIX A: 180 nm TSMC MOS PARAMETERS

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jul 29/05
* LOT: T55U WAF: 3003
* Temperature_parameters=Default

.MODEL nfet NMOS ( LEVEL = 8
+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9
+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3719233
+K1 = 0.5847845 K2 = 1.987508E-3 K3 = 1E-3
+K3B = 3.846051 W0 = 1.00001E-7 NLX = 1.66359E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.616073 DVT1 = 0.4422105 DVT2 = 0.0205098
+U0 = 276.4769418 UA = -1.287181E-9 UB = 2.249816E-18
+UC = 5.695845E-11 VSAT = 1.050018E5 A0 = 1.8727159
+AGS = 0.4223855 B0 = -8.460618E-9 B1 = -1E-7
+KETA = -6.583564E-3 A1 = 0 A2 = 0.8925017
+RDSW = 105 PRWG = 0.5 PRWB = -0.2
+WR = 1 WINT = 0 LINT = 1.509138E-8
+XL = 0 XW = -1E-8 DWG = -3.993667E-9
+DWB = 1.211844E-8 VOFF = -0.0926198 NFACTOR = 2.4037852
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 2.64529E-3 ETAB = -1.113687E-5
+DSUB = 0.0107822 PCLM = 0.7114924 PDIBLC1 = 0.1861265
+PDIBLC2 = 2.341517E-3 PDIBLCB = -0.1 DROUT = 0.708139
+PSCBE1 = 8E10 PSCBE2 = 9.186022E-10 PVAG = 5.128699E-3
+DELTA = 0.01 RSH = 6.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 7.9E-10 CGSO = 7.9E-10 CGBO = 1E-12

+CJ = 9.604799E-4 PB = 0.8 MJ = 0.3814692

+CJSW = 2.48995E-10 PBSW = 0.8157576 MJSW = 0.1055989

+CJSWG = 3.3E-10 PBSWG = 0.8157576 MJSWG = 0.1055989

+CF = 0 PVTH0 = -4.358982E-4 PRDSW = -5

+PK2 = 2.550846E-4 WKETA = 1.466293E-3 LKETA = -7.702306E-3

+PU0 = 23.8250665 PUA = 1.058432E-10 PUB = 0

+PVSAT = 1.294978E3 PETA0 = 1.003158E-4 PKETA = -3.857329E-3 )

*

.MODEL pfet PMOS ( LEVEL = 8

+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3955237

+K1 = 0.5694604 K2 = 0.0291529 K3 = 0.0997496

+K3B = 13.9442535 W0 = 1.003165E-6 NLX = 9.979192E-8

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.5457988 DVT1 = 0.2640392 DVT2 = 0.1

+U0 = 118.0169799 UA = 1.591918E-9 UB = 1.129514E-21

+UC = -1E-10 VSAT = 1.545232E5 A0 = 1.6956519

+AGS = 0.3816925 B0 = 4.590751E-7 B1 = 1.607941E-6

+KETA = 0.0142165 A1 = 0.4254052 A2 = 0.3391698

+RDSW = 168.2822665 PRWG = 0.5 PRWB = -0.5

+WR = 1 WINT = 0 LINT = 3.011839E-8

+XL = 0 XW = -1E-8 DWG = -4.05222E-8

+DWB = 4.813652E-9 VOFF = -0.099839 NFACTOR = 1.8347784

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.201776 ETAB = -0.1409866

+DSUB = 1.0474138 PCLM = 1.4195047 PDIBLC1 = 2.422412E-4

+PDIBLC2 = 0.022477 PDIBLCB = -1E-3 DROUT = 1.228009E-3

+PSCBE1 = 1.245755E10 PSCBE2 = 3.598031E-9 PVAG = 15.0414628

+DELTA = 0.01 RSH = 7.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 6.34E-10 CGSO = 6.34E-10 CGBO = 1E-12

+CJ = 1.177729E-3 PB = 0.8467926 MJ = 0.4063096

+CJSW = 2.417696E-10 PBSW = 0.851762 MJSW = 0.3387253

+CJSWG = 4.22E-10 PBSWG = 0.851762 MJSWG = 0.3387253

+CF = 0 PVTH0 = 1.406461E-3 PRDSW = 11.5261879

+PK2 = 1.718699E-3 WKETA = 0.0353107 LKETA = -1.277611E-3

+PU0 = -1.4642384 PUA = -6.79895E-11 PUB = 1E-21

+PVSAT = 50 PETA0 = 1.003152E-4 PKETA = -3.103298E-3 )

*

# APPENDIX B: MOVEMENT OF THE POLES TO THE COMPLEX REGION

It is well known that the real poles of a second order circuit can easily be moved to the complex plane by applying sufficient negative feedback [1]. Assume $A_{LP}(s)$ is a low-pass, real poled filter, where $\omega_{p1}$ and $\omega_{p2}$ are real poles and $A_0$ is the DC, i.e. frequency independent, where the transfer function is given as,

$$A_{LP}(s) = \frac{A_0\omega_{p1}\omega_{p2}}{(s+\omega_{p1})(s+\omega_{p2})} \tag{B.1}$$

By applying frequency independent feedback of H(s) =$\beta$, as demonstrated in Figure

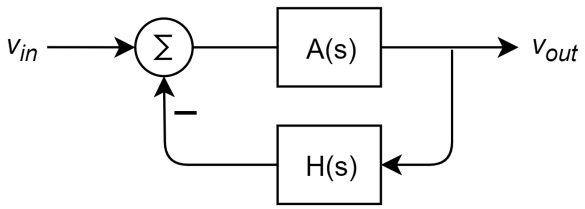


Figure B.1. The second order circuit with negative feedback.

B.1 , the poles can be obtained as given in Equation B.2. Obviously by increasing $\beta$ , poles can be moved to complex plane.

$$s_{1,2(LP)} = \frac{-(\omega_{p1}+\omega_{p2}) \pm \sqrt{(\omega_{p1}+\omega_{p2})^2 - 4(1+A_0\beta)\omega_{p1}\omega_{p2}}}{2} \tag{B.2}$$

A similar approach can be applied to filters with high-pass response. Assume $A_{HP}(s)$ is in the form of Equation B.3 given as,

$$A_{HP}(s) = \frac{A_0\omega_{p1}\omega_{p2}s^2}{(s+\omega_{p1})(s+\omega_{p2})} \tag{B.3}$$

Then by applying the same feedback factor of H(s) =$\beta$, poles are converted into the ones stated in Equation B.4. As a result, complex plane poles are also achievable for high-pass filters by increasing $\beta$ .

$$s_{1,2(HP)} = \frac{-(\omega_{p1} + \omega_{p2}) \pm \sqrt{(\omega_{p1} + \omega_{p2})^2 - 4\omega_{p1}\omega_{p2}(1 + A_0\beta\omega_{p1}\omega_{p2})}}{2(1 + A_0\beta\omega_{p1}\omega_{p2})} \tag{B.4}$$

The above feedback technique however cannot be applied to obtain complex poles for band-pass type real-pole filters. To verify this fact, assume the filter transfer function is in the form of Equation B.5.

$$A_{BP}(s) = \frac{A_0\omega_{p1}\omega_{p2}s}{(s + \omega_{p1})(s + \omega_{p2})} \tag{B.5}$$

By connecting the same feedback loop we get new poles as it is stated in Equation B.6. Since $A_{BP}(s)$ has real poles, it can be deduced that $(\omega_{p1} + \omega_{p2})^2 \geq 4\omega_{p1}\omega_{p2}$ . As a result, it is not possible to move poles into complex domain by changing $\beta$.

$$s_{1,2(BP)} = \frac{-(\omega_{p1} + \omega_{p2} + A_0\beta\omega_{p1}\omega_{p2}) \pm \sqrt{(\omega_{p1} + \omega_{p2} + A_0\beta\omega_{p1}\omega_{p2})^2 - 4\omega_{p1}\omega_{p2}}}{2} \tag{B.6}$$

Therefore, for a band-pass filter an integrating type feedback network is necessary which converts band-pass transfer function to a low-pass one to be used as a feedback signal.