DESIGN AND DEVELOPMENT OF CURRENT—MODE HALL SENSOR MICROARRAY WITH ANALOG FRONT-END AND ADC INTEGRATED CIRCUIT

by

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ABSTRACT

DESIGN AND DEVELOPMENT OF CURRENT—MODE HALL SENSOR MICROARRAY WITH ANALOG FRONT-END AND ADC INTEGRATED CIRCUIT

A study of current-mode cross-shaped Hall effect sensors with detailed analyses of each building block of Hall effect sensor microsystems including analog front-end components, and readout circuitry is presented. These include 4-phase current spinning, chopper amplifier, switched capcitor low-pass filter, and single-slope analog-to-digital converters. Significant effort is devoted to eliminate the offset and $1/f$ noise of current-mode Hall sensors. In addition, current-to-voltage conversion using chopper amplifiers is also investigated. The noise magnitude around 1 kHz is reduced from 65 nv to 8 nv using the chopping technique. The optimum W/L ratio of a cross-shaped Hall sensor is found to be 2.55 which provides a sensitivity of 239 nA/T by biasing at 10 μA. A switched capacitor 5th order elliptic low-pass filter is designed to remove the unwanted noise components that appear at odd harmonics of the chopping frequency. A 10-bit single-slope ADC is designed to digitally represent the magnetic field data. The designs presented are made using UMC 180 nm CMOS technology.

ÖZET

AKIM MODLU HALL SENSÖR MİKRODİZİNİ İÇİN ANALOG ÖN UÇ VE ADC ENTEGRE DEVRE TASARIMI VE GELİŞTİRİLMESİ

Analog ön uç parçaları ve okuma devresi de dahil olmak üzere çalışılan akım modlu ve çapraz şekilli Hall etkisi algılayıcısı mikrosisteminin her yapı bloğu detaylı bir şekilde sunulmuştur. Bunlar, 4 fazlı akım eğirme, kıyıcı amplifikatörü, anahtarlamalı kondansatör alçak geçiren filtre ve tek eğimli analogdan dijitale dönüştürücülerdir. Akım modlu Hall sensörlerin ofset ve 1/f gürültüsünü ortadan kaldırmak için önemli çaba sarfedilmiştir. Ek olarak kıyıcı yükselticileri kullanan akım-voltaj dönüşümü de araştırılmıştır. 1 kHz civarında gürültü büyüklüğü, doğrama tekniği kullanılarak 65 nV'dan 8 nV'a düşürülmüştür. Çapraz şekilli bir Hall sensörünün optimum W/L oranı 2.55 olarak bulunmuştur, bu 10 uA'lik Hall akımı ile 239 nA/T duyarlılık sağlar. Doğrama frekansının tekli harmoniklerindeki istenmeyen gürültü bileşenlerini ortadan kaldırmak için 5. derece eliptik anahtarlamalı kondansatör alçak geçiren filtre tasarlanmıştır. Manyetik alan verilerini dijital olarak temsil etmek için 10 bitlik tek eğimli ADC tasarlanmıştır. Sunulan tasarımlar UMC 180 nm CMOS teknolojisi kullanılarak yapılmıştır.

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LIST OF SYMBOLS

B	Magnetic field
C	Capacitance
f	frequency
G	Geometric correction factor
I	Current
k	Boltzmann constant
L	Hall sensor length
n	Carrier concentration
$N_{A,sub}$	P-substrate doping concentration
$N_{A,nw}$	N-well doping concentration
n_i	Intrinsic carrier concentration
q	Electron charge
R	Resistance
R_H	Hall coefficient
r_H	Hall scattering factor
R_s	Sheet resistance
s	Hall sensor contact size
S_{Vn}	Voltage noise spectral density
$S_{Vn\alpha}$	Voltage noise spectral density
S_{VnT}	Thermal voltage noise spectral density
S_I	Supply-current related sensitivity
S_V	Supply-voltage related sensitivity
t	Hall sensor thickness
T	Temperature
t_{nw}	N-well thickness
U_{pn}	Voltage across the pn junction
V	Voltage
V_D	Diffusion voltage of pn junction

V_H	Hall voltage
W	Hall sensor width
$w_{nw,sub}$	Depletion region thickness of pn junction
δ_R	Offset resistance
ϵ_{si}	Silicon absolute permittivity
μ_n	Electron mobility
μ_p	Hole mobility
σ_n	Semiconductor conductivity
θ_H	Hall angle

LIST OF ACRONYMS/ABBREVIATIONS

A/D	Analog-to-digital
AC	Alternating Current
ADC	Analog-to-digital Converter
CG	Common Gate
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
CTAT	Complementary to Absolute Temperature
DAC	Digital-to-Analog Converter
dB	Decibels
DC	Direct Current
DFF	D Flip Flop
GMR	Giant Magneto Resistance
IC	Integrated Circuit
ICMR	Input Common Mode Range
LPF	Low Pass Filter
MDAC	Multiplying Digital-to-Analog Converter
NMOS	N-channel Metal Oxide Semiconductor
Op-Amp	Operational Amplifier
OTA	Operational Transconductance Amplifier
OVSR	Output Voltage Swing Range
PM	Phase Margin
PMOS	P-channel Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
SAR	Successive Approximation Register
SNR	Signal-to-Noise Ratio
UMC	United Microelectronics Corporation

1. INTRODUCTION

1.1. Motivation and Objectives

Magnetic sensors have gained significant attention and have found widespread use in diverse fields over the last few decades. A magnetic sensor can detect the surrounding magnetic field strength based on the Lorentz force that the field exerts. The Hall-Effect sensor is the most common type of magnetic sensor and is widely used among various magnetic field detection technologies. Besides magnetic field measurement, Hall-Effect sensors are used to indirectly measure other parameters including position, velocity, and rotational angle. The Hall-Effect sensor is used in a wide range of fields including automotive, mechanical, electronic, medical, spatial, and environmental sciences [3, 4, 12]. For instance, they can be used for controlling brushless DC motors, measuring the speed of a vehicle, replacing mechanical switches and so on. The typical range of magnetic signals is shown in Figure 1.1 for various sources and applications [1]. It is expected that the Hall-Effect current sensor market is going to grow at a Compound Annual Growth Rate (CAGR) of 8.4% between the years 2017 and 2023, and would be valued at USD 1,473.7 million by 2023 [13]. Magnetic sensors used in various fields have different characteristics depending on sensitivity, size, resolution, noise and similar parameters. The approximate sensitivity ranges of commonly used magnetic sensors are given in Figure 1.2. Also, different characteristics of these sensors are given in Figure 1.3 [1].

A further reason behind Hall sensors being widely used in various fields is their compatibility with contemporary technologies. Hall sensors have the unique advantage of being fabricated in low-cost standard CMOS processes which means that they can be placed on a single integrated circuit with the entire electronic interface. This results in considerable advantages in terms of cost, reliability, size, and accuracy. Nevertheless, there are several negative factors, which result in a lower sensitivity in CMOS integrated Hall sensors. For instance, package-induced mechanical stress, temperature-drift, and process variations cause offsets and noise even if there is no magnetic field

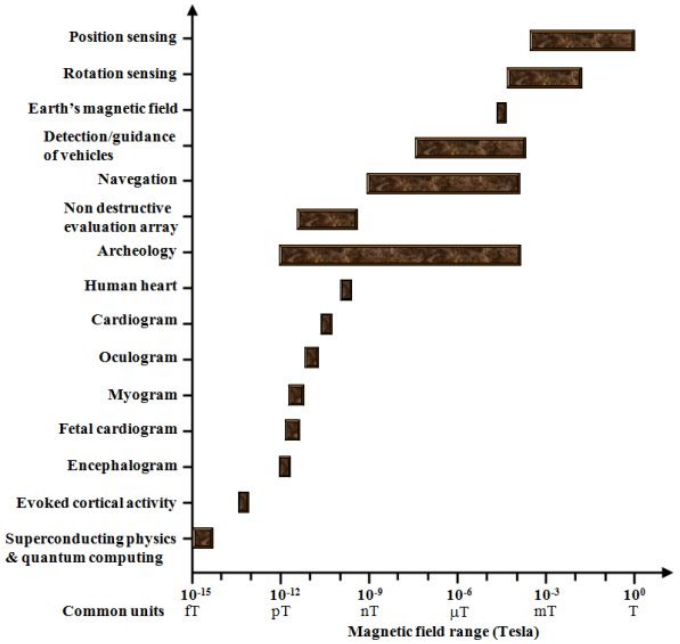

Figure 1.1. Range of magnetic signals for several sources and applications [1].

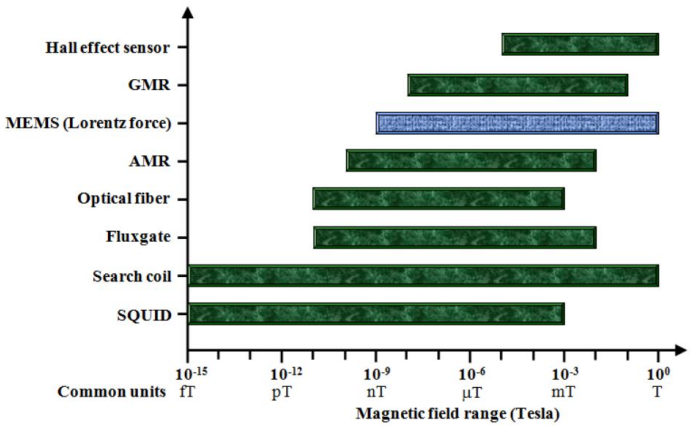

Figure 1.2. Ranges of sensitivity of different magnetic sensors [4].

Technology	Resolution (nT)	Noise ($nTHz^{-1/2}$)	Power consumption (mW)	Minimum size (mm × mm)
Hall effect [6,54]	~10^5	~4,000	~150	<1 [a]
GMR AAL002-02 [55]	5V 10 @ 1 Hz	10 @ 1Hz	~5	0.44 × 0.34 [a]
MEMS (Lorentz force) [49,50,52]	~1	~0.5 [b]	<10	<1 [a]
AMR HMC1022 [56]	5 V 8.5 @ 10 Hz	5 V 48 @ 1 Hz	~25	~ 1 [a]
Optical fiber [6,26,57]	<1	<10	<1,000	~100 × 25[c]
Fluxgate [58]	60	~10^{-1}	~100	5 × 2.5
Search coil [6,13]	20 × 10^{-6}	30 × 10^{-3}	<10	50 × 25
SQUID [59-62]	~10 × 10^{-6}	~30 × 10^{-3}	~1.8 W	<10× 10 [d]

[a] Die size of the sensor.

[b] Noise of sensor developed by Tucker, Wesoleck and Wickenden [52].

[c] Typical size of the sensor.

[d] Approximation of the chip size of SQUID without considering the cooling system.

Figure 1.3. Characteristics of most common magnetic sensors [4].

present [5]. Consequently, novel techniques are needed to eliminate offsets and the low frequency noise in integrated CMOS Hall-Effect sensors. In order to enable evaluation of these new circuit techniques, an accurate and easily understandable simulation model that includes all necessary characteristics of the sensor should be established. For implementing such a simulation model, an additional essential feature required for the model is its compatibility with modern simulation software programs such as Cadence Virtuoso, Mentor Graphics, etc.

In order to obtain improvements on speed, depth, and resolution for different applications, magnetic sensor arrays have been utilized. Magnetic sensor arrays are used in magnetic flux leakage testing and eddy-current testing. Arrays of multiple sensors enable quick scanning of an area for defects in a single-pass instead of scanning point by point. Improvements on single-chip arrays can be enhanced further by means of deposition on active silicon substrates. As a result, multiplexing and signal processing can be implemented within the chip, simplifying the signal processing interface with the sensor and minimizing the effect of noise. Therefore, very small magnetic fields can be detected with the aid of small single-chip magnetic sensor arrays [14].

Demand for biosensors that can accurately read signals from biochemical processes by interfacing with biological entities has been rising steadily. Such sensors will

put forward fundamental solutions for prospective medical applications. These sensors should have high sensitivity, large dynamic range and ideally should also achieve portability. After multiple phases of testing and improvements, they can be used as convenient and portable medical diagnostic platforms for applications including environmental monitoring, epidemic disease control, low-cost home health care, and biohazard detection [15, 16].

A number of available molecular biosensors use electrochemical and optical transduction rather than a magnetic sensing mechanism. In these sensors, on-chip electrodes are employed by electrochemical sensors in order to perceive dielectric property variations and extra charges caused by target molecules. Although electrochemical sensors can be integrated in CMOS, they are sensitive to offset and signal drifting [17]. Photoluminescence detection is frequently used as the typical optical approach in many microarray sensors. Molecular tags emit light and are able to achieve nanomolar level detections when they are subjected to optical stimulations. Due to the requirement of optical setups and filters, these sensors are highly expensive and complex [18, 19]. In contrast, magnetic sensors provide significant advantages over electrochemical or optical sensors. First of all, magnetic sensors do not require bulky optical devices or setups. Second, magnetic sensors entail lower system costs and provide highly stable signals in contrast to optical approaches. Furthermore, since most biological samples are not magnetic, a more robust detection scheme with lower noise can be achieved using magnetic sensors in comparison to electrochemical detection. In addition, magnetic particles in samples can be exposed to external magnetic fields enabling manipulation at the molecular level. Finally, a higher signal-to-noise ratio (SNR) can be achieved using magnetic sensors compared to optical or electrochemical approaches [20].

A molecular test contributes to the detection of biomarkers. Determining their precise quantity assists in medical diagnoses and optimal treatment for patients. Certain diseases are related to specific biomolecular signatures that can be found by examining gene or protein expression of patients. Therefore, with the help of molecular tests, it is possible to provide personalized medical care, which involves treatment based on a patient's proteomic or genetic information [21]. The latest improvements

in nanotechnology make molecular tests possible using electronic detection rather than optical methods.

In order to perform a number of molecular tests in parallel, microarrays are useful platforms for analyzing comprehensive gene and protein expression change in biological samples [22]. Deoxyribonucleic acid (DNA) microarrays demonstrated success in genomic research by means of amplification techniques which enable large-scale replication of DNA. Protein microarrays require more sensitivity and higher dynamic range due to the lack of equivalent amplification techniques [23]. Hence, a highly sensitive electronic platform is required for molecular tests with possible new applications in areas such as the study of protein-protein interactions, clinical diagnostics, monitoring of disease states and drug discovery [22].

Recent years have seen a rise in the demand for technological improvements that facilitate medical diagnostic testing in small clinics, physician offices, and even at patients' homes. Expensive optical detectors and long incubation durations make laboratory immunoassays based on colorimetric or fluorescent detection methods difficult to be used in small clinics. Using superparamagnetic microbeads as labels enables implementing assays in a small and inexpensive form factor and thereby magnetic labels can be detected electromagnetically instead of optically. To have stable signals in biological systems and buffer solutions, magnetic beads are appropriate for labels. This feature enables longer shelf life and robust detection [24].

Various types of magnetic sensors such as spin-valve sensors, inductors, magnetoresistance (GMR) and Hall-effect sensors have been used to detect magnetic beads. GMR sensors provide outstanding sensitivity but require additional magnets and are not suitable for standard CMOS technology. On-chip inductive sensors also offer good sensitivity but require calibration and lead to interference from non-magnetic conductors. Hall-Effect sensors integrated in the standard CMOS process provide less sensitivity compared to other types of magnetic sensors, but are not reactive to conductors and can be used even with integrated electromagnets [24].

The primary motivation for this thesis is to design a current-mode Hall-Effect sensor array with its readout circuitry. To this end, the following have been taken into consideration:

(i) Modelling of the sensor using the Verilog-A language
(ii) Analog front-end building blocks
(iii) The system design and proper operation of the entire system

First, an accurate and simplified model of the cross-shaped CMOS integrated Hall-Effect sensor has been constructed in order to be able to analyze the sensor along with its electrical circuits. Simulations considering temperature drift, geometrical effects, nonlinear conductivity, and junction field effects have been performed on the model. Second, analog front-end building blocks for the sensor have been carefully designed. These consist of a current spinning circuit, a biasing circuit for twin Hall plates, a fully-differential chopper amplifier with its common mode feedback (CMFB), a low-pass filter to eliminate the chopper frequencies, and an A/D converter block. Finally, operation of the entire system including compatibility with each of the building blocks has been tested for and ensured. Overall system simulations including sensitivity, offset, and overall noise analysis have been completed.

1.2. Thesis Organization

This thesis consists of six chapters. Chapter 1 provides a brief introduction to Hall-effect sensors and their areas of usage. This chapter also outlines the motivation behind studying and using Hall-effect sensors the need for converting the readout circuitry data into more meaningful forms. The purpose behind using array-based sensors has also been stated.

In Chapter 2, the fundamental physical theory behind the Hall-Effect sensor is introduced. Performance differences between current-mode and voltage-mode of operation is specified. Effects of factors such as temperature, sensor shape and material on the functioning of the sensor are investigated. Hall-effect sensor characteristics includ-

ing offset, noise, sensitivity, nonlinearity, and parasitic effects are explored. Finally, state-of-the-art of sensitivity improvements and offset reduction are presented.

In Chapter 3, different choices of readout circuits and their advantages and disadvantages over each other have been discussed. Chapter 3 also presents detailed analyses of different alternatives for essential building blocks of a sensor interface such as offset reduction, current-to-voltage conversion, low-pass filtering, and analog-to-digital conversion.

In Chapter 4, the preferred building blocks are presented. In order to reduce the offset, a current-spinning technique is chosen, and the implementation of associated switches is explained. Furthermore, the biasing circuit of the sensor, the integrator-capacitive detection circuit and a fully-differential chopper-amplifier are analyzed. In addition, an elliptical fifth-order switched-capacitor low-pass filter is designed to filter out the frequency components springing from the chopper amplifier. This is followed by the details of a column level single slope A/D converter compatible with image sensors. All relevant simulations of these building blocks are provided in this chapter. The entire system design and its simulation results are presented in Chapter 5, followed by conclusions and possible future work in Chapter 6.

2. HALL MAGNETIC SENSORS

2.1. The Hall Effect

The Hall effect, discovered in 1879 by Edwin Hall, is the phenomenon of an emf, called the Hall emf, arising in a current-carrying conductor placed in a magnetic field. The Hall emf is distinct from the emf arising from electromagnetic induction in that it is perpendicular to both the direction of current flow and the magnetic field vector. The Hall effect can be explained using the basic theory of electromagnetism as follows: when a current flows through a conductor that is exposed to a magnetic field, the charge carriers in the conductor experience a force, called the Lorentz force, leading to deflection in a direction perpendicular to both the current flow and the magnetic field. This gives rise to charge accumulation and charge separation, and hence an electric field (the Hall electric field) is generated along this perpendicular direction. The Hall electric field $\boldsymbol{E}_H$ is equal to the cross product of the drift velocity $\boldsymbol{v}_d$ of charge carriers and the magnetic field vector $\boldsymbol{B}$:

$$\boldsymbol{E}_H = \boldsymbol{v}_d \times \boldsymbol{B} \tag{2.1}$$

and the drift velocity $\boldsymbol{v}_d$ is proportional to the external electric field $\boldsymbol{E}_e$:

$$\boldsymbol{v}_d = \mu \boldsymbol{E_e} \tag{2.2}$$

where μ denotes the carrier mobility of charge carriers.

Combining (2.1) and (2.2), the Hall electric field can be expressed as:

$$\boldsymbol{E}_H = \mu[\boldsymbol{E_e} \times \boldsymbol{B}] \tag{2.3}$$

The Hall effect has found numerous applications including in magnetic sensors known as Hall effect sensors that act as transducers performing electromechanical energy con-

version using magnetic fields. The Hall emf or the Hall voltage induced in a conductor is proportional to the Hall electric field. Since the Hall voltage is dependent on various factors including current density, magnetic field intensity, charge density, and carrier mobility of the conducting material, a measurement of this voltage provides information about these crucial parameters. However, since the Hall voltage is relatively small (on the order of a few microvolts to a few millivolts), additional electronics need to be employed along with the conducting material to obtain meaningful and precise measurements [4]. Another application is in the field of semiconductors that use galvanomagnetic effects due to the Lorentz forces on charge carriers. This is particularly useful for semiconductors thanks to their high mobility and low carrier concentration which amplify galvanomagnetic effects [3].

2.2. Hall Effect Devices and applications

2.2.1. Hall Plates

A conceptual diagram of a rectangular Hall plate is shown in Figure 2.1. Four electrical contacts are placed at the outer edges of a thin plate of conducting material. Two of these contacts are utilized for biasing the device by supplying a bias current I. The other two contacts are called sense contacts which would be at the same potential in the absence of a perpendicular magnetic field. However, when a perpendicular magnetic field is applied, the Lorentz force deflects moving charged carriers along the S1-S2 axis, leading to a charge separation between the sense contacts. This creates a potential difference between S1 and S2 and this potential difference is called the Hall voltage V_H [4]. The Hall voltage V_H is the integral of the Hall electric field $\boldsymbol{E}_H$ over the width W between the sense contacts:

$$V_H = \int_{S1}^{S2} \boldsymbol{E}_H d\boldsymbol{W} \tag{2.4}$$

For the configuration shown in Figure 2.1, the external field is given by $\boldsymbol{E}_e = (V/L)\hat{\boldsymbol{i}}$, where L is the length of the device, and $\hat{\boldsymbol{i}}$ is the unity vector collinear with the longitude

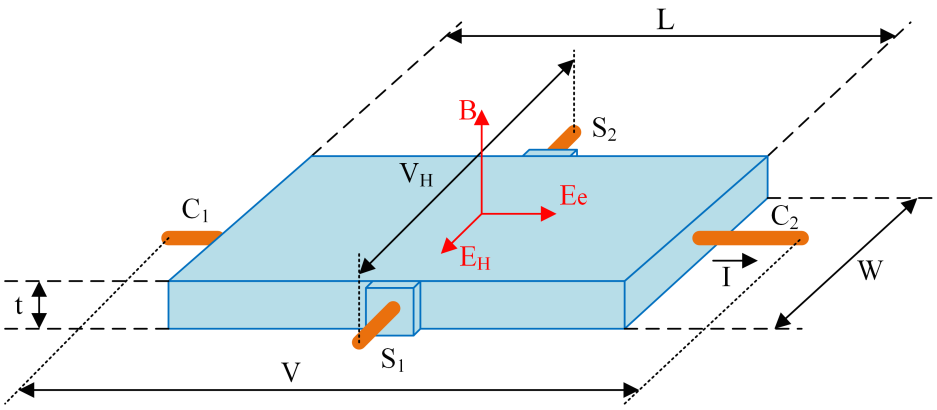

Figure 2.1. A conceptual diagram of a rectangular Hall plate. An applied bias voltage V between the contacts C1 and C2 generates an electric field $\boldsymbol{E}_e$ resulting in current I. Under the perpendicular magnetic field $\boldsymbol{B}$, the Hall effect gives rise to the Hall electric field $\boldsymbol{E}_H$ and the Hall voltage V_H is induced across sense contacts S1 and S2.

of the device. Therefore, the Hall voltage can be expressed in the following form:

$$V_H = \mu \frac{W}{L} V B \tag{2.5}$$

The Hall voltage can also be expressed in terms of the bias current I as:

$$V_H = \frac{1}{qnt} I B \tag{2.6}$$

where q is the magnitude of the electron charge, n is the carrier concentration and t is the thickness of the plate.

2.2.2. Geometry

In order to simplify the theoretical analysis, Hall plates are assumed to be rectangular. However, the shape does have an influence on Hall devices. The Hall voltage varies according to the geometry of device; thus a geometrical correction factor is needed to take the effects of geometrical differences into account. The geometrical correction factor represents the dependence of the Hall voltage on the current which in turn is limited by the geometry. It can be thought of as an efficiency factor for the

sensor. The correction factor is taken to be 1 for very long Hall devices and 0 for very short devices, so that it is bounded between 0 and 1 [4]. The width W and length L of the Hall plate, size and position of the contacts, and the Hall angle are among the parameters that determine the geometrical correction factor.

For the rectangular case, a uniform current sheet is formed by biasing electrodes that extend along the width of the device. The total current passing through the sense contacts specifies the sensitivity. Making the sensor wider results in greater bias current for a particular bias voltage. However, wider bias electrodes create a lower resistance path, which creates a short circuit across the Hall voltage. In order to prevent short circuiting, cross-shaped Hall plates can be used. Due to the quick growth in the input resistance by increasing the length of the Hall plates, this shape is not very suitable for high-sensitivity applications. An alternative method to avoid short circuiting the Hall voltage is using a diamond shaped sensor. This geometry too is not desirable for sensitivity improvements, but it provides the advantage of reducing the Ohmic offset caused by contact misalignments [3]. These common Hall plate shapes are shown in Figure 2.2.

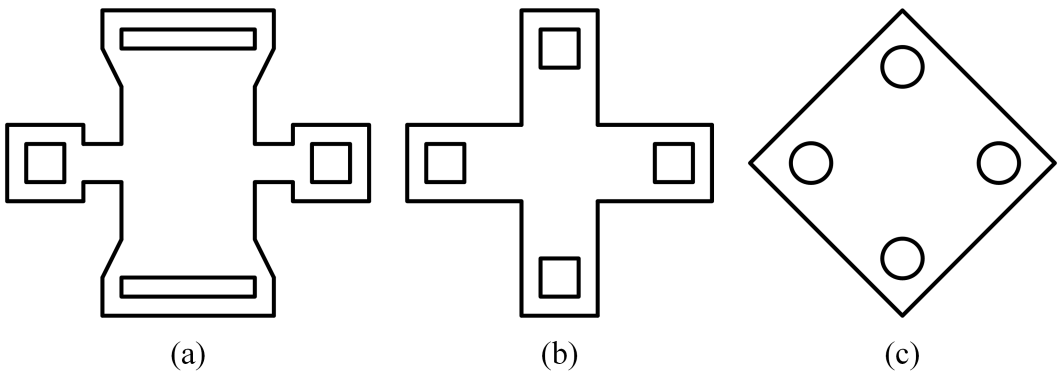

Figure 2.2. Common Hall plate shapes: (a) rectangle, (b) cross, and (c) diamond.

2.2.3. Material

Choice of material has a significant impact on Hall sensor performance. Lower carrier concentration and smaller plate thickness leads to greater sensitivity. Therefore, materials with lower carrier concentration are better choices for making Hall sensors.

Other criteria for selecting the proper material include high mobility and low conductivity. Metals exhibit the favorable properties of high conductivity and low mobility, but it is difficult to decrease their thickness substantially. Thus, metals are not suited for Hall-effect sensors.

Since electron mobility is greater than hole mobility in n-type semiconductors, they are preferred for use in the manufacture of Hall devices. For instance, the ratio of electron mobility to hole mobility μ_n/μ_p is approximately 2.5 for Si, 20 for GaAs, and 70 for InAs. Although Si has lower electron mobility compared to the other two, it is a better candidate for use in Hall sensor devices due to its compatibility with IC technology [3, 4]. Table 2.1 shows the basic material properties of semiconductors suitable for use in the fabrication of Hall devices.

Table 2.1. Material properties of semiconductors for Hall sensors at 300 K [2].

Material	$\mathbf{E}_g$ **[eV]**	**n [cm^{-3}]**	μ_n **[cm^{2}V^{-1}s^{-1}]**	**-R$_H$ [cm^{3}C^{-1}]**
Ge	0.67	2.4×10^{13}	3.9×10^{3}	9×10^{4}
Si	1.12	2.5×10^{15}	1.3×10^{3}	2.5×10^{3}
InSb	0.17	9×10^{16}	7.0×10^{4}	70
InAs	0.36	5×10^{16}	2.2×10^{4}	125
GaAs	1.42	3×10^{15}	6.4×10^{3}	2.1×10^{3}

2.2.4. Applications of Hall Magnetic Sensors

Hall sensors are used for measuring current, power, pressure, position, speed etc. They are used as a contactless switch for brushless DC motor control and used in applications in the automotive industry. The following presents a few applications of Hall-effect sensors.

2.2.4.1. Current Transducers. Electrical current can be sensed by measuring the magnetic field associated with the current flow without inserting an ammeter into the circuit. Magnetic current sensing has the advantage of not needing to interfere with the circuit being sensed, and is particularly very useful for measuring large DC currents [2, 3]. Figure 2.3 demonstrates the basic positioning of a contactless current

Hall-effect sensor. The Hall-effect sensor is mounted in the spacing between the ends of the ring of magnetic core around the current conductor. The magnetic flux is then measured and a calibration to the current in the conductor is made using Ampere's Law. Applying Ampere's law $\oint \boldsymbol{B} \cdot d\boldsymbol{l} = \mu_0 I$, we obtain $I = 2\pi r V_H/(\mu_0 S_A)$, where I is the measured current, S_A is the sensitivity, r is the distance between the center of the conductor and the Hall sensor, and μ_0 is the permeability of free space [2].

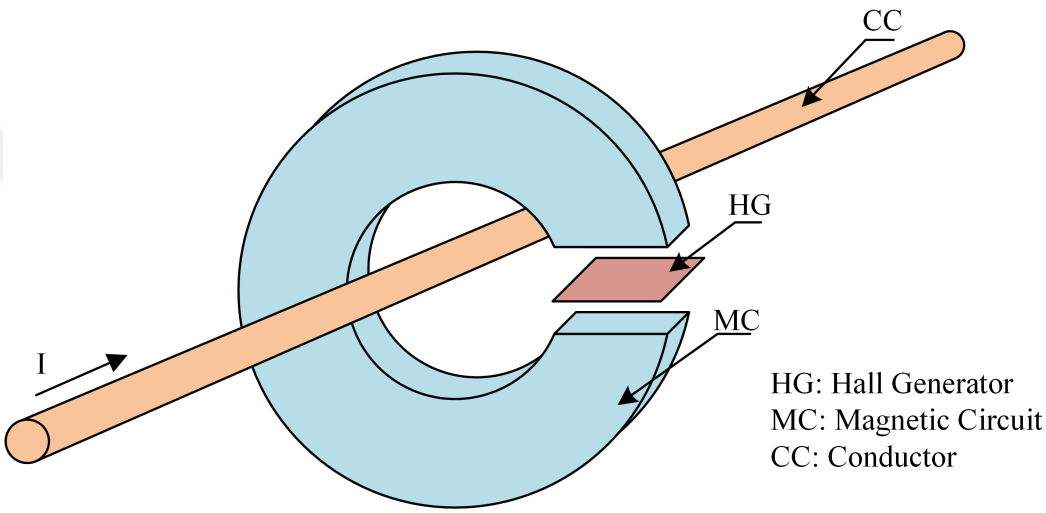

Figure 2.3. Configuration of contactless current Hall-effect sensor [2].

2.2.4.2. Contactless Signal Generation. For detecting the relative position of two objects at short distances, the Hall-effect sensor is used as a receiver for magnetic fields, and a small magnet is used as a transmitter. Measurements made using the Hall-effect sensor then provide information about the presence or absence of the magnetic field and helps to determine the sign of the field. One advantage of using permanent magnets is that they do not require power thus eliminating the need for connecting cables. Moreover, the relative velocity between transmitter and receiver does not affect the magnitude of the signal. The output signal is generally handled in digital form [2].

One typical operation is head-on actuation as shown in Figure 2.4. Bringing one of the poles of the magnet near the device activates it. The magnetic field strength increases as the distance between the device and the magnet decreases. When the field becomes greater than the operating point of the sensor, it is activated. On the

other hand, the sensor is deactivated if the field reduces to a specified *release threshold* point [3].

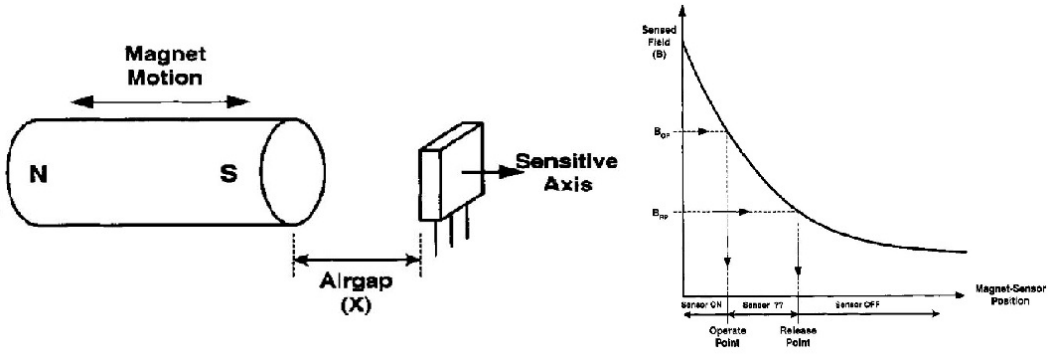

Figure 2.4. Head-on actuation operation and operating range on flux map [3].

2.2.4.3. Contactless Linear and Angular Position Sensors. In addition, Hall sensors are utilized in sensing linear and angular displacement. As shown in Figure 2.5, the biaxial Hall sensor is placed below a small, cylindrical permanent magnet which is magnetized perpendicular to the sensor plane. The magnet moves parallel to the sensor plane at a certain height above it and at a certain distance from the sides of the sensor. The position of the magnet is a function of the direction of the magnetic field vector (or the magnetic field lines) passing through the sensor. The angle that the magnetic field makes with the sensor plane can be read and thus the position of the magnet can be determined [25]. For measuring the angular displacement, the sensor is positioned under a rotating shaft, and the magnet is placed below the shaft as shown in Figure 2.6. The magnet is magnetized diametrically, thus the magnetic field on the sensor rotates with the rotation of the shaft. The angle can be calculated by taking the arctangent of the output voltages in the X and Y directions [4]. Hall sensors are also used to measure the speed of wheels and shafts. For instance, they are used in anti-lock braking systems, tachometers, internal combustion engine ignition timing and DC brushless motor control [3]. Recently they have also started to be used in labeling bioassays magnetically and are soon expected to meet the requirements of a point-of-care diagnosis system [26].

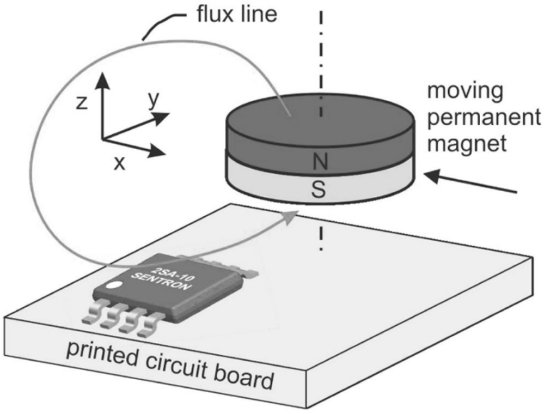

Figure 2.5. Linear positioning sensor by using biaxial Hall sensor and a permanent small magnet [4].

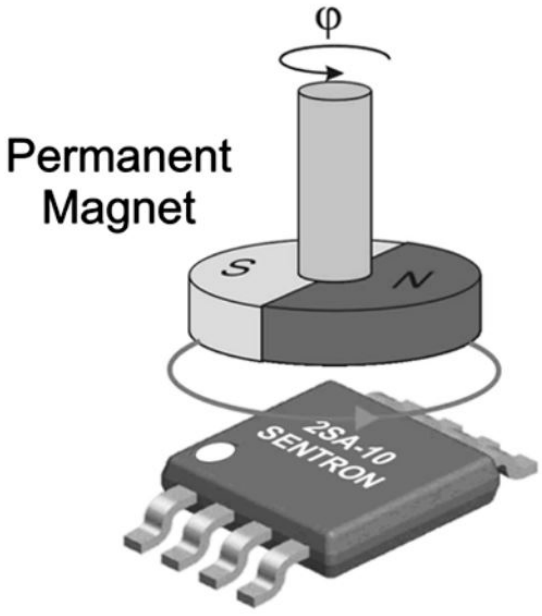

Figure 2.6. Angular positioning sensor by using biaxial Hall sensor [4].

2.3. Operation in Voltage Mode and Current Mode

A Hall plate exposed to a perpendicular magnetic field is biased through a pair of contacts at opposite ends and the output signal is obtained as a voltage between a second pair of contacts oriented orthogonally to the first pair. This is the typical use of Hall plates in the voltage-mode of operation. The mode of operation is defined by the type of the output signal: either voltage or current. The Hall-effect arises from current deflection, which prevails in short devices. *Large contact Hall device* is the appropriate term to be used instead of *short device* [4]. There is no difference in the physical structure of the device; the distinction is only in the type of signal used as the output. Furthermore, offset cancellation techniques such as *current spinning* are still applicable in the current mode of operation since the physical structure of the device is still symmetrical which means input and output terminals of the plate may be used interchangeably.

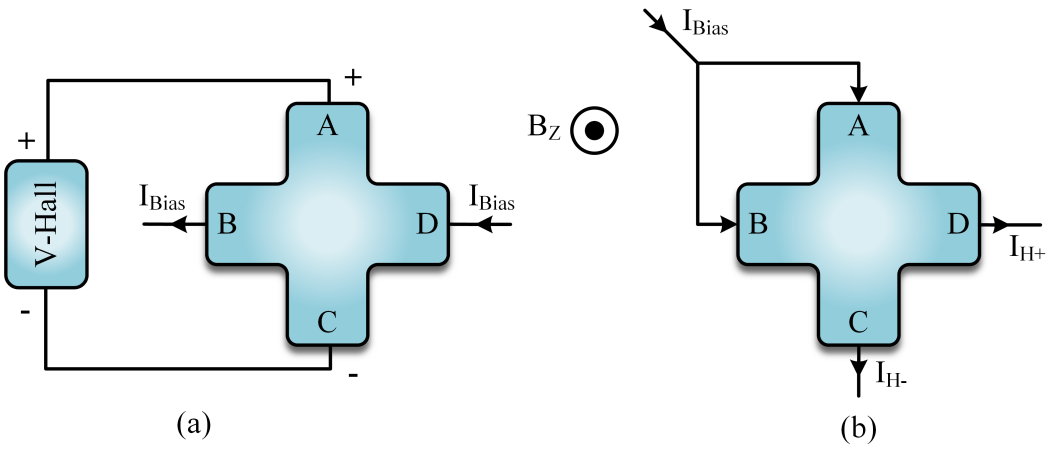

Figure 2.7. Hall plates working in (a) voltage mode, and (b) current mode.

For the device shown in Figure 2.7(a), the Hall voltage can be calculated as $V_H = R_H GIB/t$ where R_H is the Hall coefficient, G denotes the geometrical correction factor, B is the normal magnetic field, and t is the plate thickness. R_H can be found using $R_H = -\mu_n/\sigma_n = -r_H/(qn)$ where n denotes the carrier concentration and r_H is the Hall scattering factor. As can be seen from these equations, high mobility and low carrier concentration are desired for achieving a high Hall voltage.

For operation in current mode, the plate is biased by applying a current from two consecutive leads laterally, and the other two output currents show a deviation under the influence of magnetic field. The Hall current I_{Hall} is the difference between the output currents and can be calculated as $I_{\text{Hall}} = \mu_H \frac{W}{L} B I_{\text{Bias}}$ where μ_H denotes the Hall mobility of majority carriers, B is the normal magnetic field, and $\frac{W}{L}$ is the ratio of width to length of the plate. The output currents I_{H+} and I_{H-} can be calculated as:

$$I_{H+} = \frac{I_{\text{Bias}}}{2} + \frac{I_{\text{Hall}}}{2} \tag{2.7}$$

$$I_{H-} = \frac{I_{\text{Bias}}}{2} - \frac{I_{\text{Hall}}}{2} \tag{2.8}$$

There are several benefits of operating in current-mode. One of them is that the size of the devices can be scaled down further, since sharing the current allows reduction of the number of terminals. A further advantage is that current-mode Hall sensors provide higher resolution in low magnetic fields by using high mobility plates [27]. Moreover, the voltages at the terminals will be theoretically fixed and thus will not be the affected by parasitic capacitances.

2.4. Compact Cross-Shaped CMOS Hall-Effect Sensor Model

The realization of low power, high precision, and miniaturized integrated Hall devices has been feasible through down scaling in CMOS processes. The current-related sensitivity of the miniaturized integrated Hall devices gets better with lower doping levels caused by N-well lateral diffusion [5]. However, the junction field effect causes higher offsets in miniaturized Hall sensors.

Figure 2.8 shows a cross-shaped horizontal Hall-plate that is fabricated using an N-type layer on top of a P-type substrate. An N-type layer is preferred due to its higher mobility which provides greater sensitivity. The plate is delimited by a lateral p-diffusion boundary which is used as an insulating layer by forming a reverse-biased p-n junction. The contacts are produced by using N^+ diffusion which provides

Ohmic contacts as an intermediate layer between the metal layer and the substrate. Eventually, the surface of the Hall-plate is covered by a shallow p-layer which reduces the flicker noise and prevents carrier scattering [5, 28].

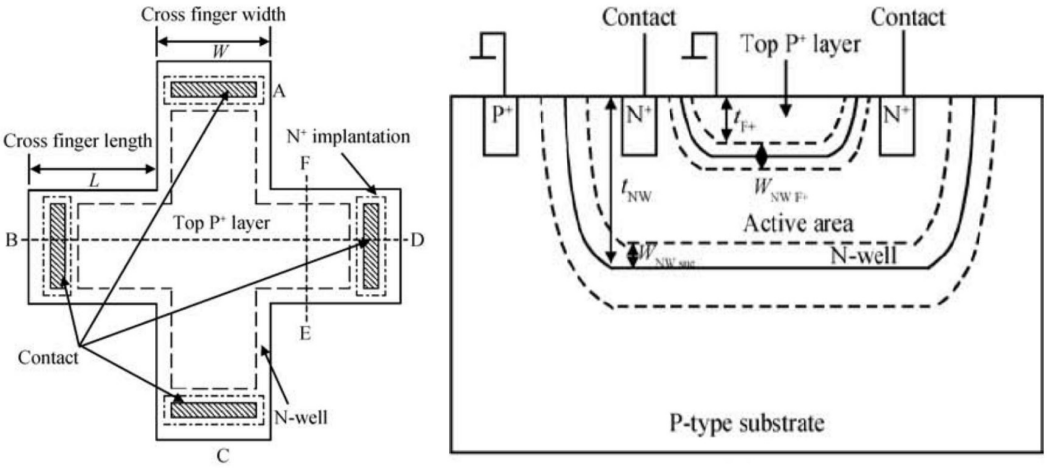

Figure 2.8. Top view and cross-section of cross-shaped Hall sensor fabricated in standard CMOS technology [5].

The simplified compact model of an integrated cross-shaped horizontal Hall sensor is presented in Figure 2.9. The model includes eight resistors and four current-controlled current sources.

The Wheatstone bridge with four resistors have been utilized to model the characteristics and the behavior of the Hall plates previously. In the four-resistor model, because the current flowing through two adjacent contacts does not cross the center of the plate, the equivalent resistance calculated between two adjacent contacts is not entirely correct. In addition, the offset induced by the piezo-resistive effect in silicon is not modeled accurately.

R_H and R_D are the resistances between two adjacent contacts and between two diagonal contacts respectively. They are calculated based on the N-well sheet resistance R_S using the Van der Pauw method. R_S is also a function of potential difference

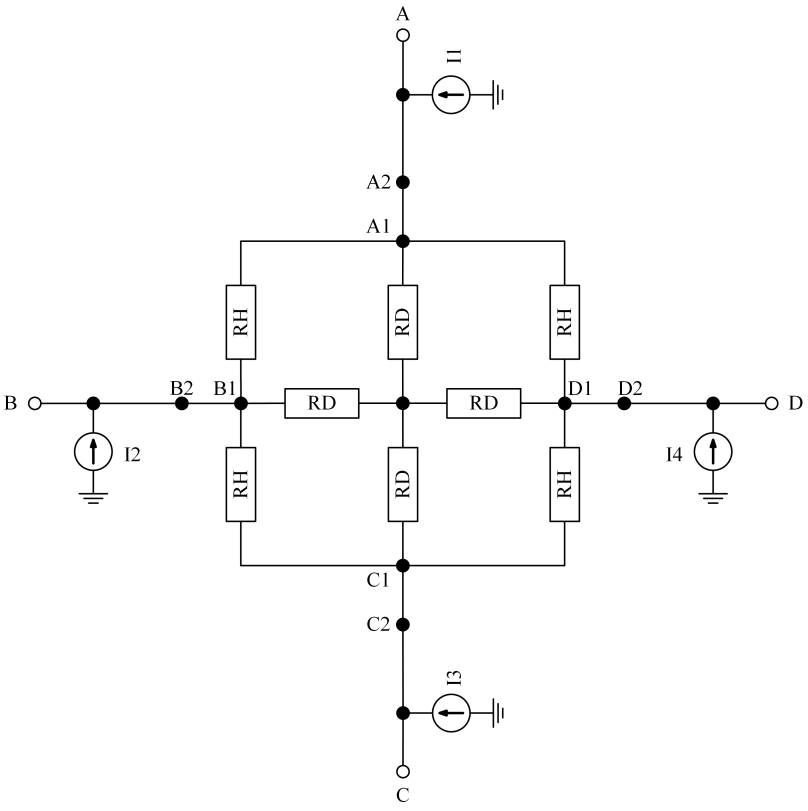

Figure 2.9. Cross-shaped horizontal CMOS integrated Hall plate model adopted from [6].

between contacts C and D divided by the current flowing between A and B [29].

$$R_{AB,CD} = \frac{V_{CD}}{I_{AB}} = \frac{\ln 2}{\pi} R_S \tag{2.9}$$

Furthermore, $R_{AB,CD}$ can be calculated based on the model structure using the values of R_H and R_D.

$$R_{AB,CD} = \frac{R_H}{4}\left(\frac{2R_D - R_H}{2R_D + R_H}\right) \tag{2.10}$$

R_H and R_D are calculated as:

$$R_H = R_S \times \frac{2}{\pi}\left(\left(2\frac{L}{w} + \frac{2}{3}\right)\pi - 2\ln(2)\right) \tag{2.11}$$

$$R_D = R_s \times \frac{(\frac{2L}{w} + \frac{2}{3}) \times ((\frac{2L}{W} + \frac{2}{3})\pi - 2\ln(2))}{(\frac{2L}{W} + \frac{2}{3})\pi - 4\ln(2)} \tag{2.12}$$

$$\frac{R_H}{R_D} = 2 - \frac{8}{\pi}\left(\frac{\ln 2}{2L/W + 2/3}\right) \tag{2.13}$$

where R_S denotes the sheet resistance of the N-well, W and L denote the width and length of the cross-shaped Hall plate respectively.

The equivalent resistance between the two diagonal contacts A and C can be calculated by using both the model structure and geometry of the Hall plate:

$$R_{AC} = \frac{2R_D R_H}{2R_D + R_H} = \left(2\frac{L}{W} + \frac{2}{3}\right) R_S \tag{2.14}$$

$2L/W + 2/3$ is the effective number of squares of the N-well diffusion resistance and is an approximation to the center square number, since sensor fingers are placed parallel to each other [30]. In these equations, N^+ contact resistances are not taken into

consideration since they are negligible compared to the sheet resistance of the N-well.

For the model shown in Figure 2.9, each Hall current can be found by using the following equations:

$$I_{H/2_1} = \frac{1}{2R_{AC}} S_I I(D_1, D_2) B \tag{2.15}$$

$$I_{H/2_2} = \frac{1}{2R_{AC}} S_I I(A_1, A_2) B \tag{2.16}$$

$$I_{H/2_3} = \frac{1}{2R_{AC}} S_I I(B_1, B_2) B \tag{2.17}$$

$$I_{H/2_4} = \frac{1}{2R_{AC}} S_I I(C_1, C_2) B \tag{2.18}$$

where S_I, the current related sensitivity of the plate is given by:

$$S_I = \frac{G r_H}{q N_{D,nw} t_{eff}} \tag{2.19}$$

where G is the geometrical correction factor, t_{eff} is the effective thickness, r_H is the Hall scattering factor of majority carriers and $N_{D,nw}$ is the N-well doping concentration. r_H can be calculated as the ratio of μ_H to μ_n, which are the Hall and electron mobilities respectively.

The geometrical correction factor can be calculated by using the following formula for cross-shaped Hall plate if the geometrical ratio of $W/2L \leq 0.39$ is satisfied:

$$G = 1 - 5.0267 \frac{\theta_H}{\tan \theta_H} \exp\left[-\frac{\pi}{2}\left(\frac{W + 2L}{W}\right)\right] \tag{2.20}$$

where $\theta_H = \tan^{-1}(\mu_H B)$ is the Hall angle [31]. Equation (2.20) can be further simplified if a low magnetic field is induced:

$$G = 1 - \exp\left(-\frac{\pi L}{W}\right) \tag{2.21}$$

The effective thickness t_{eff} of the conduction channel in 2.19 is given by:

$$t_{eff} = t_{nw} - w_{nw,sub} \tag{2.22}$$

where t_{nw} is the depth of the N-well and $w_{nw,sub}$ is the thickness of the depletion region between the N-well and the P-substrate which are given by (2.23) and (2.24) respectively.

$$t_{nw} = \frac{1}{q\mu_n N_{D,nw} R_S} \tag{2.23}$$

$$w_{nw,sub} = \sqrt{\frac{2\epsilon_{si}}{q} \times \frac{N_{A,sub}}{(N_{A,sub} + N_{D,nw})N_{D,nw}}} \times \sqrt{V_D} \tag{2.24}$$

Technology files provide the value of the N-well sheet resistance, the doping concentrations of the N-well and the P-substrate, and the diffusion voltage of the pn junction.

The following subsections present a study of the most important characteristics of Hall magnetic sensors: sensitivity, linearity, offset, noise and the effect of temperature drift.

2.4.1. Sensitivity

The biasing effects the sensitivity. The magnetic sensitivity of a voltage-biased Hall sensor is related to the result obtained by multiplying the Hall mobility and the bias voltage. On the other hand, the sensitivity of current-biased Hall sensors is correlated with the product: (Hall coefficient / effective thickness) × (bias current) [Heidari, Thesis]. Therefore, sensitivity of current-biased Hall sensors are less temperature dependent compared to voltage-biased ones [32].

Leaving aside the effects of biasing conditions, the absolute sensitivity of both voltage and current mode Hall sensors can be found from equations (2.25) and (2.26)

respectively.

$$S_V = \frac{V_{\text{Hall}}}{B} \qquad [V/T] \tag{2.25}$$

$$S_I = \frac{I_{\text{Hall}}}{B} \qquad [A/T] \tag{2.26}$$

The sensitivity in current mode is the amount of output current change per unit change in applied magnetic field difference:

$$S_I = \frac{\Delta I}{\Delta B} = \frac{I_{H+} - I_{H-}}{\Delta B} \tag{2.27}$$

Several methods have been studied in order to increase the sensitivity. One such method uses a pair of Hall plates as shown in Figure 2.10. Here, I_{HP} and I_{HN} denote the positive and negative output currents of a twin current-mode Hall sensor. In this configuration, the difference of the output currents is twice the Hall current ($2 \times I_{\text{Hall}}$). Hence the sensitivity of the sensor can be doubled with respect to the regular implementation [33]].

$$I_{HP} = I_{H+} - I_{H-} \tag{2.28}$$

$$I_{HN} = I_{H-} - I_{H+} \tag{2.29}$$

$$\text{Sensitivity} = \frac{\Delta I}{\Delta B} = \frac{I_{HP} - I_{HN}}{\Delta B} \tag{2.30}$$

2.4.2. Offset

The offset of the Hall device is the value of the output when no magnetic field is applied. The main reasons for a non-zero offset are geometrical errors, contact resistance, non-uniform doping density, piezoresistive effects, and alignment errors of

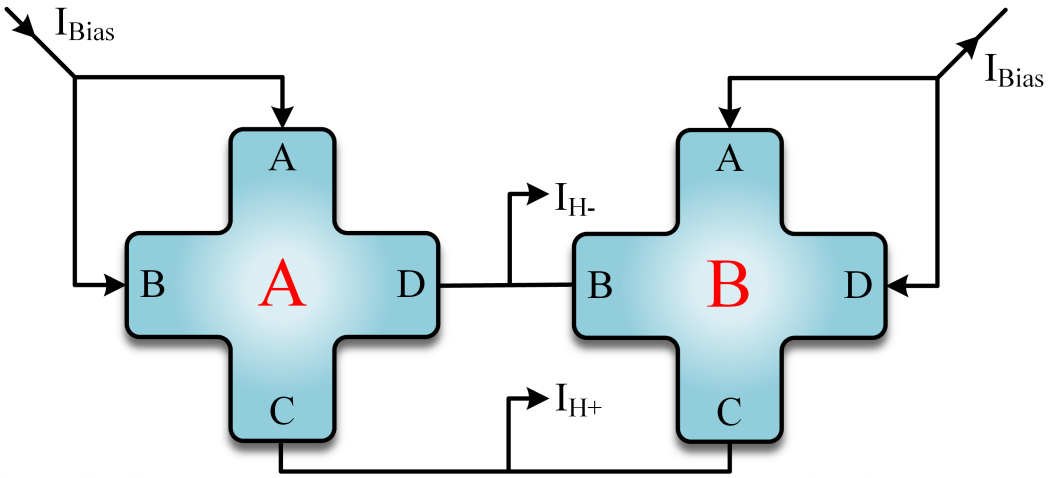

Figure 2.10. Twin current-mode Hall sensor structure.

the sense leads. Possible approaches for reducing the offset are discussed in Chapter 3. Four different types of small resistors have been added to the model in order to simulate the effects of offset as shown in Figure 2.11.

For the model presented in Figure 2.11:

- δR_1 is used to model the effect of shear stress on the Hall device. Small positive changes in resistance are included along 1-4 and 2-3 and small negative changes are also added between 1-2 and 3-4.
- δR_2 and δR_3 are used to model fabrication defects such as non-uniform doping density, material thickness, and the difference between the cross finger lengths along the directions 1-3 and 2-4 respectively. These imperfections cause a change in resistance between terminals and the center of the plate. δR_2 is used to model the resistance change between terminal 1 and the center and that between the center and terminal 3. δR_3 is used to model the resistance change between terminal 2 and the center and that between the center and terminal 4.
- δR_4 is used to model the compression or expansion of the plate along the directions 1-3 and 2-4. The variations between directions 1-3 and 2-4 are inversely proportional to each other [34].

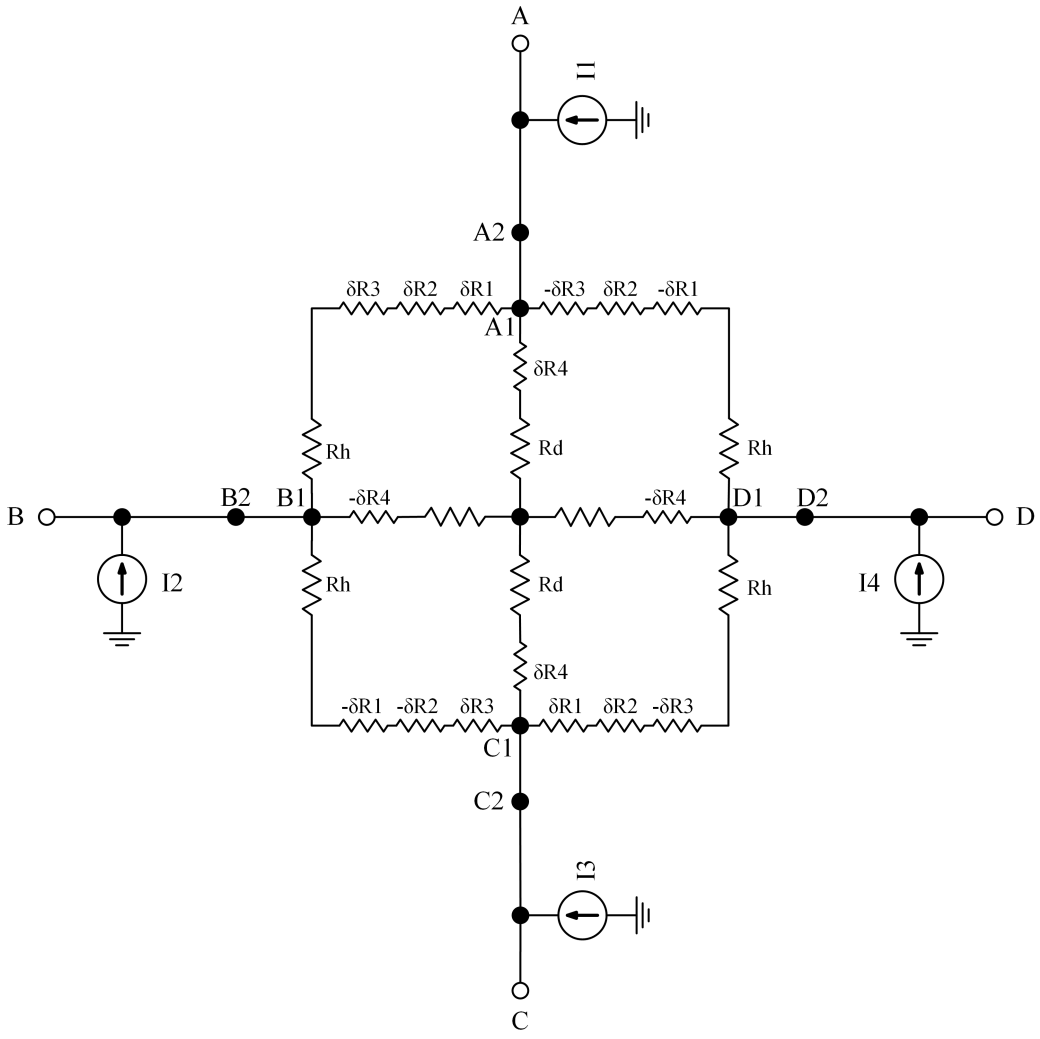

Figure 2.11. The cross-shaped Hall sensor with eight resistances to model the offset.

2.4.3. Temperature Drift Effect

Temperature dependent parameters that have an influence on sheet resistance and sensitivity are electron mobility, doping concentration, Hall scattering factor and the diffusion potential.

With temperature rise, phonon concentration increases and causes increased scattering. As the temperature increases, atomic vibrations in the crystal structure increase and hence mobility of carriers decreases. The temperature dependence of mobility is as follows:

$$\mu_n(T) = \mu_n(T = 300K) \left(\frac{T}{300K} \right)^{-1.5} \tag{2.31}$$

The difference in diffusion potential caused by temperature change results in variation in the thickness of the depletion region. The temperature dependence of diffusion potential V_D is given by:

$$V_D(T) = \frac{kT}{q} \ln \left(\frac{N_{D,nw} N_{A,sub}}{n_i^2} \right) \tag{2.32}$$

where k denotes the Boltzmann constant. Intrinsic carrier concentration n_i also has an exponential dependence on temperature as follows:

$$n_i = 7.3 \times 10^{21} \times T^{1.5} \exp \left(\frac{-1.12}{2 \times 8.62 \times 10^{-5} T} \right) \tag{2.33}$$

Temperature dependence of Hall scattering factor is found empirically by modifying the value of r_{H0} in (2.34) [35].

$$r_H = r_{H0} \left(\frac{T}{300K} \right)^{0.13} \tag{2.34}$$

These are the temperature dependent parameters included in the model presented in this study.

2.4.4. Nonlinearity

The thickness of the depletion region changes due to reverse biased PN junction voltage U_{pn}, thus it causes variations in the thickness of the conduction channel. The thickness of depletion region around the junction is calculated using the following formula:

$$w_{nw,sub} = \sqrt{\frac{2\epsilon_{si}}{q} \times \frac{N_{A,sub}}{(N_{A,sub} + N_{D,nw})N_{D,nw}}} \times \sqrt{V_D - U_{pn}} \tag{2.35}$$

Nonlinear voltage dependence of conduction channel results in nonlinearity in sheet resistance and current related sensitivity. The effect of nonlinearity is included in the current related sensitivity by substituting for $w_{nw,sub}$ from (2.35) into (2.22) and subsequently into (2.19), and the new equation for S_I is expanded using the Taylor series up to the second order as a function of voltage difference. Defining the constant k_1 as:

$$k_1 = \frac{2\epsilon_{si}}{q} \times \frac{N_{A,sub}}{(N_{A,sub} + N_{D,nw})N_{D,nw}} \ , \tag{2.36}$$

the sensitivity can be expressed as:

$$S_I(U_{pn}) = S_{I0} + S_{I1} \times U_{pn} + S_{I2} \times U_{pn}^2 \ , \tag{2.37}$$

where,

$$S_{I0} = \frac{G \times r_H}{q \times N_{D,nw} \times (t_{nw} - \sqrt{k_1 \times V_D})} \ , \tag{2.38}$$

$$S_{I1} = \frac{1}{2} \times \frac{G \times r_H \times \sqrt{k_1}}{q \times N_{D,nw} \times \sqrt{V_D} \times (t_{nw} - \sqrt{k_1 \times V_D})^2} \ , \tag{2.39}$$

and,

$$S_{I2} = \frac{1}{8} \times \frac{G \times r_H \times \sqrt{k_1} \times (3\sqrt{k_1 \times V_D} - t_{nw})}{q \times N_{D,nw} \times V_D\sqrt{V_D} \times (t_{nw} - \sqrt{k_1 \times V_D})^3} \ . \tag{2.40}$$

Thus, the sheet resistance definition is also updated accordingly:

$$R_S(U_{pn}) = R_{S0} + R_{S1} \times U_{pn} + R_{S2} \times U_{pn}^2 \tag{2.41}$$

where,

$$R_{S0} = \frac{1}{q \times \mu_n \times N_{D,nw} \times (t_{nw} - \sqrt{k_1 \times V_D})} \ , \tag{2.42}$$

$$R_{S1} = \frac{1}{2} \times \frac{\sqrt{k_1}}{q \times \mu_n \times N_{D,nw} \times \sqrt{V_D} \times (t_{nw} - \sqrt{k_1 \times V_D})^2} \ , \tag{2.43}$$

and,

$$R_{S2} = \frac{1}{8} \times \frac{\sqrt{k_1} \times (3\sqrt{k_1 \times V_D} - t_{nw})}{q \times \mu_n \times N_{D,nw} \times V_D\sqrt{V_D} \times (t_{nw} - \sqrt{k_1 \times V_D})^3} \ . \tag{2.44}$$

In this new model, R_{AC} in (2.14) is modified according to R_S in (2.41), and the output of the current controlled current sources is also modified according to the new current related sensitivity [30].

2.4.5. Noise

The noise voltage at the output terminals of a Hall device places the deterministic part of Hall output above the precise limit to which we can measure. The noise in Hall sensors stems from thermal noise, generation-recombination noise and $1/f$ noise. The generation-recombination noise can be neglected, since its value is very less compared to flicker and thermal noise. Hence, the voltage spectral density of noise across the

sense leads is specified by

$$S_{NV}(f) = S_{V\alpha} + S_{VT} \tag{2.45}$$

where $S_{V\alpha}$ and S_{VT} are the voltage noise spectral densities resulting from thermal noise and flicker noise respectively. Figure 2.12 demonstrates a typical voltage noise spectral density function of a Hall sensor. In the graph, f_c stands for corner frequency; it is the corner point where the spectral density of thermal noise is equal to the spectral density of flicker noise. Thermal noise is also called white noise because of its flat spectral

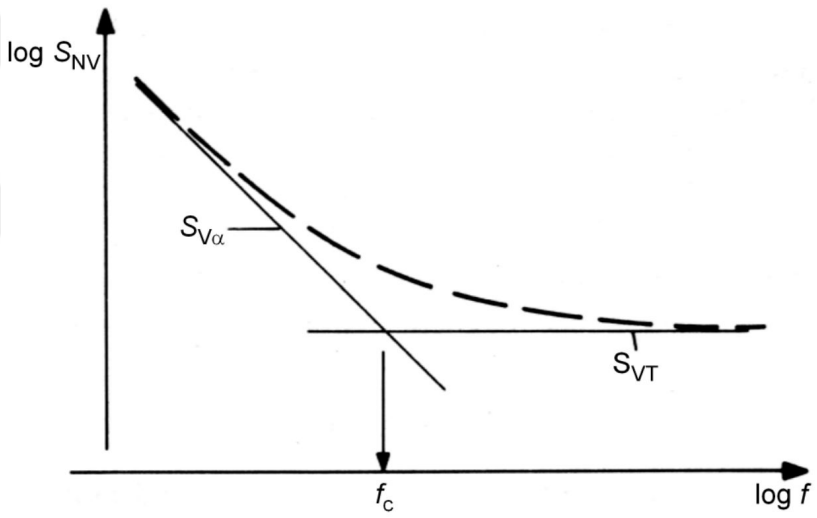

Figure 2.12. Typical spectral noise density as a function of frequency.

density over a given frequency. Thermal noise is caused by thermal agitation of charge carriers. The voltage spectral density of thermal noise is calculated using:

$$S_{VT} = 4kTR \tag{2.46}$$

where R is the resistance of noise source, k denotes the Boltzmann constant and T is the absolute temperature. In order to calculate the voltage spectral density of thermal noise for a cross-shaped horizontal Hall sensor, resistance of noise source is found by taking the potential difference between the sense terminals per unit current flowing between the input terminals. If the resistance value of noise is substituted into the

equation, spectral thermal noise density turns out to be:

$$S_{VT} = 4kT \left(\frac{\ln 2}{\pi} \right) R_S \tag{2.47}$$

The spectral density of flicker noise for a cross shaped Hall sensor is calculated by using the Hooge's empirical relation [36]. The following equation is used to calculate the noise spectral density between the sense terminals of Hall cross:

$$S_{V\alpha,\text{out}} = \frac{\alpha I^2 R_S^2}{N F_Q f^\beta} \tag{2.48}$$

where α is the Hooge's constant related to the fabrication process, $\beta \approx 1$, N is the total number of carriers in the active region of the Hall cross. F_Q is the geometrical reduction factor between the sense terminals [37]. Likewise, noise spectral density between the input terminals of a Hall cross is given by:

$$S_{V\alpha,\text{in}} = \frac{\alpha I^2}{N_S A F_D f^\beta} \left(\frac{1}{q\mu N_S} \right)^2 \tag{2.49}$$

where F_D is geometrical reduction factor between the input terminals. N_S denotes the carrier density in the active region and is calculated by taking the integral of doping concentration within the depth of the active layer.

$$N_S = \int_{x_t}^{x_b} n(x) dx \tag{2.50}$$

Geometrical reduction factors F_Q and F_D rely on the two dimensional current distribution as:

$$F_Q = I^4 \Big/ \sum_A \left(i_x \tilde{i}_x + i_y \tilde{i}_y \right)^2 \tag{2.51}$$

$$F_D = I^4 \Big/ \sum_A \left(i_x^2 + i_y^2 \right)^2 \tag{2.52}$$

where i_x and i_y are x and y components of the current and $\tilde{i}_x$ and $\tilde{i}_y$ are the current components after the input and output leads are exchanged. The geometrical reduction factor is only affected by the L/W ratio and is taken as 1 based on the length and width of the Hall plate used in this study. The low noise voltage V_N between the output

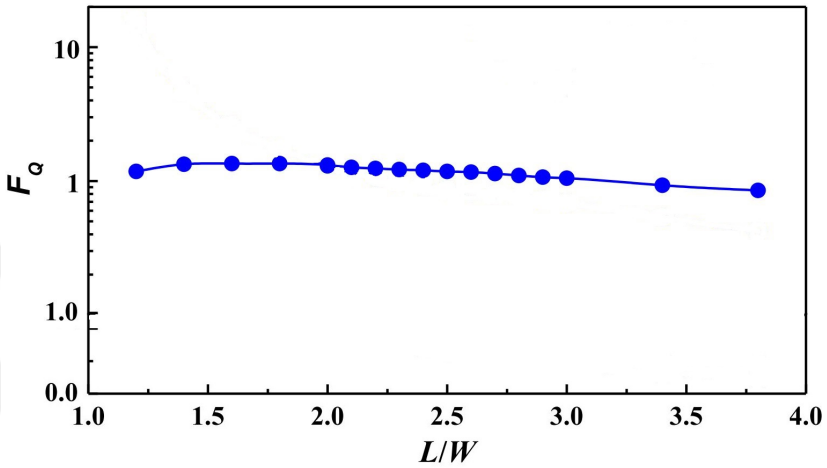

Figure 2.13. F_Q vs L/W for Hall cross [7].

leads of the Hall plate is calculated by taking the square root of the integrated noise spectral density within a specific frequency range:

$$V_N = \sqrt{\int_{f_1}^{f_2} S_Q(f)df} \tag{2.53}$$

Therefore, after substitution of noise spectral density, the noise voltage can be found using the following equation:

$$V_N = \frac{IN_S^{-1.5}}{q\mu}\sqrt{\ln(f_2/f_1)\alpha AF_Q} \tag{2.54}$$

The SNR can be calculated as given in (2.55) [7].

$$\text{SNR} = G_H B\mu\sqrt{\frac{N_S AF_Q}{\alpha \ln(f_2/f_1)}} \tag{2.55}$$

The parameters for cross shaped Hall sensors and their values are given in Table 2.2.

Table 2.2. Parameters for a cross-shaped Hall plate.

Parameter	**Symbol**	**Value**	**Unit**
Electron charge	q	1.6×10^{-19}	C
Electron mobility	μ_n	4.16×10^{-2}	$m^2/V{\cdot}s$
Silicon absolute permittivity	ϵ_{si}	1.04×10^{-10}	F/m
Boltzmann constant	k	1.38×10^{-23}	m^2kg/s^2K
Intrinsic carrier concentration	n_i	1.49×10^{16}	m^{-3}
N-well doping concentration	$N_{D,nw}$	1.7×10^{23}	m^{-3}
N-well thickness	t_{nw}	2.33×10^{-6}	m
N-well—P-substrate depletion region thickness	$w_{nw,sub}$	9.74×10^{-10}	m
P-substrate doping concentration	$N_{A,sub}$	3.41×10^{19}	m^{-3}
PN junction diffusion voltage	V_D	6.2×10^{-1}	V
Hall scattering factor	r_H	1.2	-
Geometrical correction factor	G	0.6952	-
Geometrical reduction factor	F_Q	1	-
Hooge's constant	α	2.5×10^{-5}	-
Carrier density in active region	N_S	9.7×10^{12}	cm^{-2}
Sensor width	W	2.55×10^{-6}	m
Sensor length	L	1.00×10^{-6}	m

3. CURRENT-MODE HALL-EFFECT SENSOR READOUT CIRCUIT

The Hall effect sensor provides a very small output owing to the factors that limit its performance. The function of a readout circuitry is to amplify the output of the sensor by eliminating or decreasing the effects of these factors which include nonlinearity, temperature drift, offset and low-frequency noise. A variety of techniques have been proposed for minimizing the effect of these factors.

3.1. Dynamic Offset Cancellation

There are different types of offset in the Hall voltage that stem from packaging stress and other imperfections. The output offset restricts the DC resolution of the sensor excessively. Therefore, an offset cancellation technique has to be selected based on its compatibility with the Hall plate structure and its effectiveness in eliminating all offset sources.

One method of offset cancellation known as *orthogonal coupling* typically involves using an array of plates. This method works based on the assumption that the imbalance source that gives rise to the offset is invariant and fixed from plate to plate and hence the offsets of any pair of plates will be equal but of opposite polarity [Bilotti et al]. Thus in a multiplate configuration, the offsets ideally cancel out provided there is no offset mismatch between plates. In practice, however, two physically different plates reliably have significantly different offsets owing to their differing temperature-dependent built-in stresses, among other factors. This leads to undesirable residual offsets in multiplate sensors.

To overcome this drawback, a different approach known as *dynamic offset cancellation* has been proposed and employed [8, 38–40]. This procedure does not require multiple plates but rather relies on a single switched Hall plate setting. In this tech-

nique, the current supplied through a single plate is alternated between two orthogonally oriented directions. Since the offset Hall voltage is always perpendicular to the current direction, if the orientation of the supplied current is alternated between two states: 0° and 90° (with respect to a reference axis along the plate), the offset voltage will alternate between 90° and 0° respectively. If this orientation switching is conducted at a sufficiently high frequency, the result is a virtually zero offset across either of the two orientations [39]. This improvement can be attributed to all sources of imbalance and irregularity on a single plate being reliably constant, in comparison to separate plates which inevitably have independent sources of imperfections that cannot perfectly cancel out in a multiplate configuration.

The biggest factor contributing to offset is shear stress, and the 2-phase current spinning technique successfully eliminates this. However, other sources of offset such as fabrication imperfections and compression stress cannot be removed by 2-phase cancellation. The lack of success in a 2-phase configuration makes it necessary to implement 4-phase current spinning. In this technique, the output and supply terminals of the Hall plate are interchanged periodically, resulting in the biasing current direction being rotated by $\pi/2$ in each phase. The average offset is expected to be 0 after the fourth phase [41]. The 4-phase current spinning technique is demonstrated in Figure 3.1. Figure 3.2 shows the output offset of a single cross-shaped Hall plate for each of the 4 phases.

There is also an 8-phase current spinning technique that is implemented with eight different biasing modes. An offset on the order of a few hundred μT is achieved by using the 2-phase current spinning technique for CMOS integrated Hall plates. Offset values of 25 μT and 5 μT are obtained using 4 phases and 8 phases of current spinning respectively [8, 9]. Figures 3.3 and 3.4 show the implementation of current spinning techniques in 4-contact, 4-phase and 8-contact, 8-phase configurations respectively.
The flicker noise of the sensor is also reduced by selecting a spinning frequency that is greater than the noise corner. Despite this, thermal noise of the Hall sensor is not effected since it is determined by the resistance of the Hall sensor.

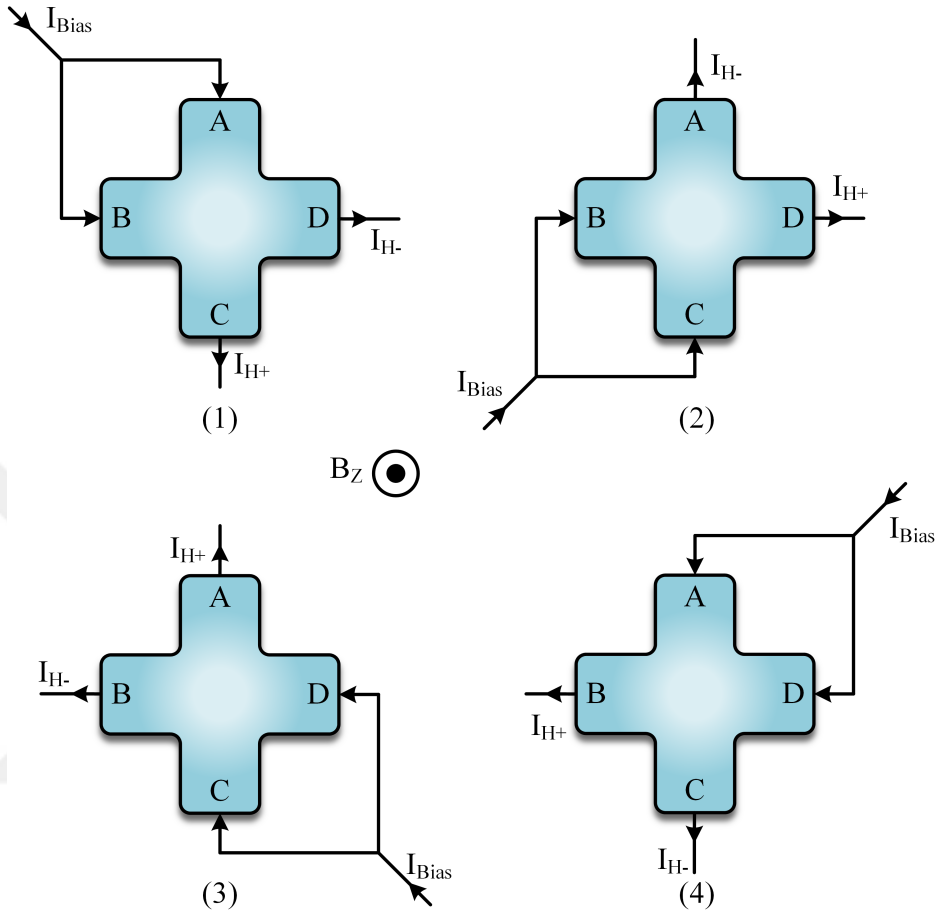

Figure 3.1. Current Spinning Technique in 4 phases.

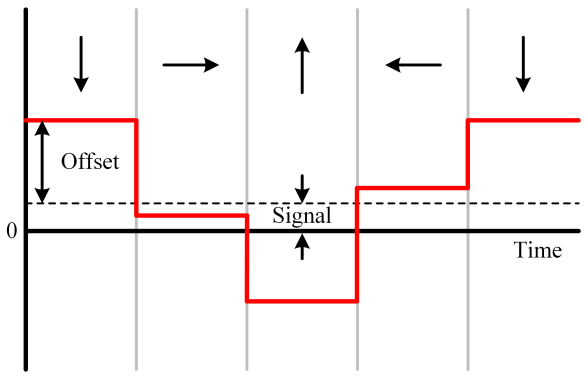

Figure 3.2. Output offset of a cross-shaped Hall sensor after 4-phase current spinning.

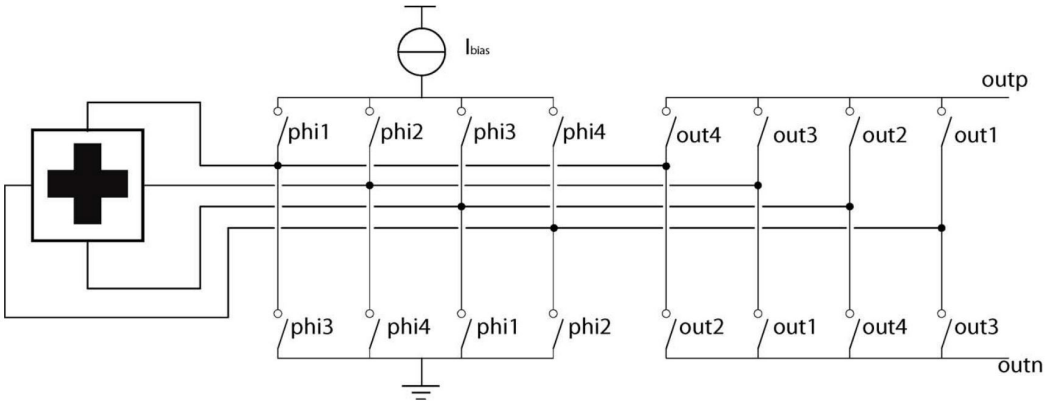

Figure 3.3. Current Spinning Technique in 4-phases [8].

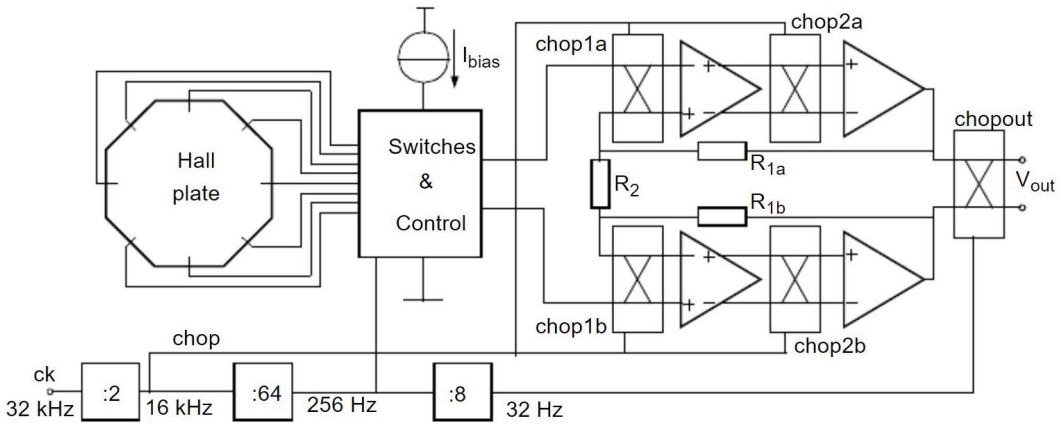

Figure 3.4. Output offset of a cross-shaped Hall sensor after 8-phase current spinning [9].

3.2. Analog Front End

The magnetic Hall sensor microsystem consists of a current-to-voltage converter and a low-pass filter in order to generate useful information from the applied magnetic field. The magnetic field is detected by Hall plates and produces a differential electrical current based on the bias current.

3.2.1. Current-to-Voltage Conversion

Various configurations may be used to convert a differential current into a differential voltage such as *common-gate detection*, *resistive detection*, *integrated capacitive detection*.

3.2.1.1. Common-Gate detection. I/V conversion using a common-gate amplifier configuration is performed by flowing the Hall current into sources of common-gate transistors as shown in Figure 3.5. The current gain of a common-gate amplifier is unity, thus in theory, the input Hall current at the source exactly appears at the drain, and the output voltage at the drain can be measured across R_{out}. However, the thermal noise of the resistance and the current noise introduced by MOS adversely affects the output voltage. Hence, it is difficult to achieve good SNR without using a large bias current [33].

3.2.1.2. Resistive Detection. Another current-to-voltage conversion technique is resistive detection as shown in Figure 3.6. In this case, the output current of the sensor is detected by the feedback resistance, R_f, connected between the input and output terminals of an operational amplifier. This configuration provides better results compared to common-gate detection but the feedback resistor has a significant impact on output noise which limits the gain of the sensor interface [33].

3.2.1.3. Integrated Capacitive Detection. In order to achieve a better noise performance, the Hall current can be integrated over a capacitor for a specific period of time

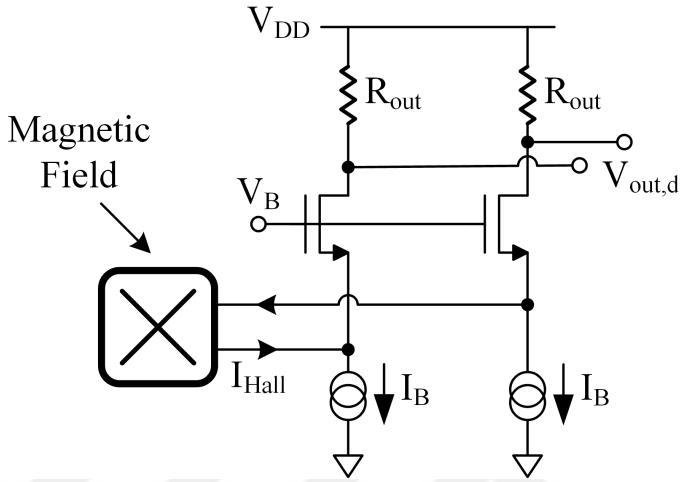

Figure 3.5. Common-gate detection scheme.

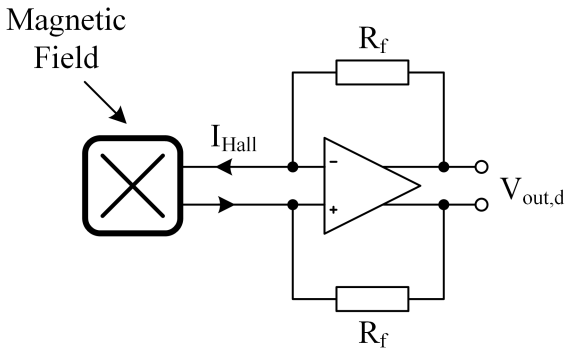

Figure 3.6. Resistive current detection scheme.

as demonstrated in Figure 3.7. In this configuration, the noise performance is more or less dependent on the value of the capacitance, and the voltage-to-current gain is proportional to the integration time. Another advantage of capacitive detection is the better matching performance of capacitors over resistors. Besides these benefits, a lower residual offset can be obtained by using a low-noise operational amplifier [42,43].

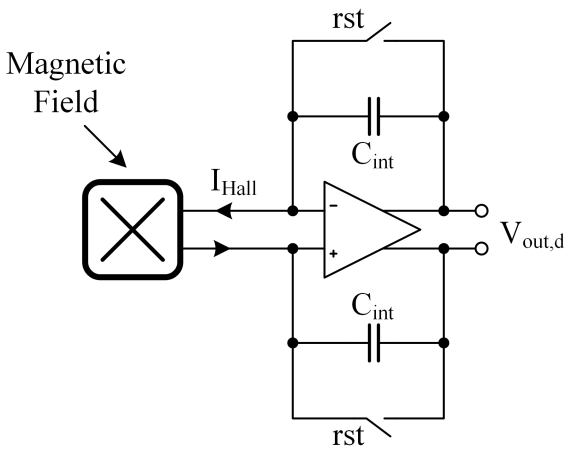

Figure 3.7. Integrated capacitive detection scheme.

3.2.2. Amplifier Design

Designing high-gain, low-offset and low-noise operational amplifiers is required for dedicated sensor readout electronics. To this end, techniques such as *auto-zeroing*, *correlated double sampling* and *chopping* are employed. Various combinations of these techniques are also used depending on system requirements [33].

3.2.2.1. Auto-zeroed Amplifiers. The auto-zeroing technique consists of two-phases. The offset and low-frequency noise are sampled and stored in one phase, then the signal is amplified and the offset and noise are subtracted from the signal in the other phase. This technique can be analyzed in two different ways: in terms of the output or the input offset storage.

(a) *Output offset storage*: The capacitor is placed at the output of the amplification stage as shown in Figure 3.8. The offset is amplified by the voltage gain of the

amplifier and stored on the auto-zero capacitor during the sampling phase, F_2. The voltage across the capacitor during the sampling phase can be expressed as:

$$V_{out1} = V_c = AV_{os} \tag{3.1}$$

where A is the voltage gain of the amplifier. Both the voltage and the offset are amplified during the signal phase, F_1, and the output voltage can be found using the difference between the voltages in the two phases.

$$V_{out1} = (V_{in} + V_{os})A \tag{3.2}$$

$$V_{out2} = V_{out1} - V_c = AV_{in} \tag{3.3}$$

All offset is compensated in theory. However, repeated switching on and off of the CMOS transistor switches by results in charge-injection, which in turn gives rise to residual offset at the end. The primary disadvantage of the auto-zeroing technique with output offset storage is a reduction of output range due to residual offset, thus this technique is not suitable for high-gain amplifiers.

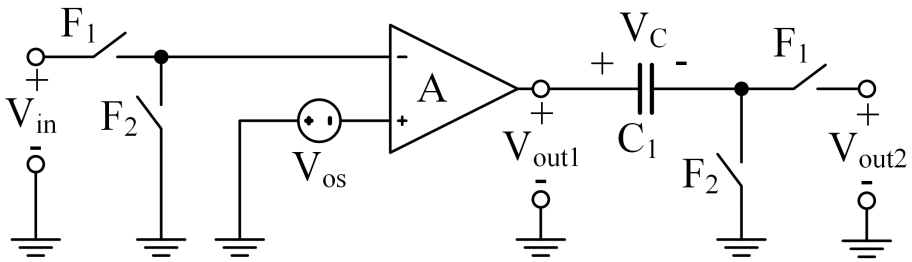

Figure 3.8. Auto-zeroed amplifier with output offset storage.

(b) *Input offset storage*: This is an alternative auto-zeroing technique established in the literature [44, 45]. In this approach, an auto-zeroing capacitance is positioned on the input side of the amplifier as shown in Figure 3.9. The capacitor is charged by the offset voltage during the sampling phase:

$$V_c = \frac{A}{A+1}V_{os} \tag{3.4}$$

And the output voltage during the signal phase, F_1, is given by:

$$V_{out} = (V_{in} + V_{os} - V_c)A = \left(V_{in} + \frac{1}{1+A}V_{os}\right)A \tag{3.5}$$

As seen in (3.4), finite gain causes a residual offset in the amplifier. The charge

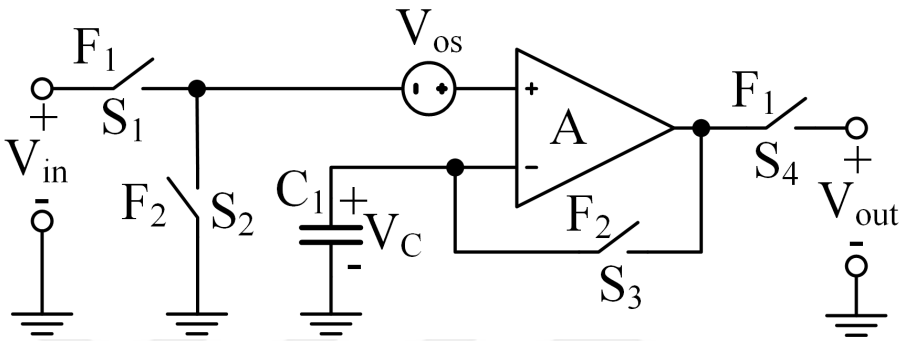

Figure 3.9. Auto-zeroed amplifier with input offset storage.

injection error is also included in the residual offset in addition to the finite gain of the amplifier. Since the auto-zeroing capacitor is already on the input side, the residual offset due to charge injection in switch S_3 on the feedback branch (see Figure 3.9) and the leakage of the capacitor cannot be divided by the gain of the amplifier and hence, the error stays on the input side. Therefore, this technique is more suitable for use with high-gain amplifiers.

There are a few disadvantages of the auto-zeroing technique. One of them is that auto-zeroing can only be used in discrete-time applications. There are continuous-time implementations of auto-zeroing by using *ping-pong arrangements* in the literature [44, 45], however these bring in other drawbacks such as greater circuit complexity and increased power dissipation. A second disadvantage of auto-zeroing is noise folding. The thermal noise of the amplifier is folded back into the signal band due to sampling, hence thermal noise floor of the amplifier increases.

3.2.2.2. Correlated Double Sampling. This technique is used by many different types of switched-capacitor circuits. The working principle is similar the auto-zeroing tech-

nique. During the calibration phase, the input voltage is sampled and stored in the capacitors, and the output of the amplifier is sampled. Then the low-frequency noise and the offset voltage are separated from the input signal [44, 45]. The basic circuit schematic is shown in Figure 3.10. The total charge in each phase can be expressed as:

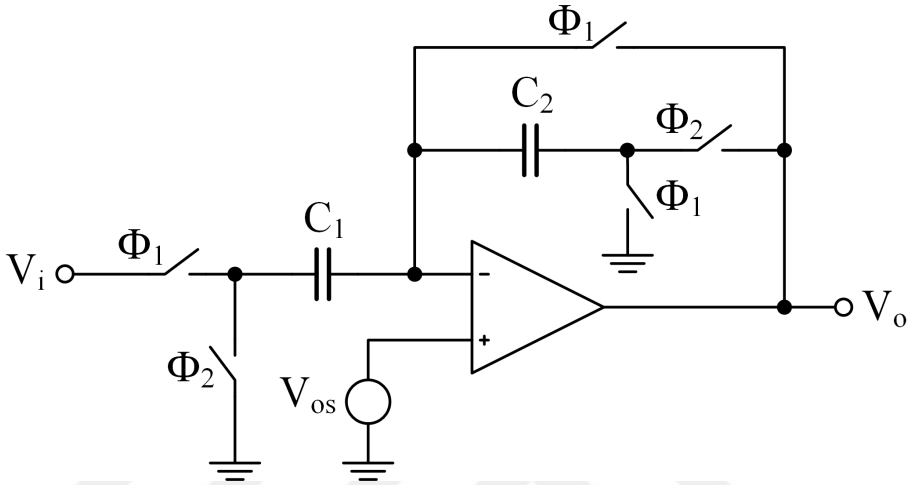

Figure 3.10. Correlated Double Sampling Technique.

$$\Sigma Q(\Phi_1) = [V_i(n) - V_{os}]C_1 - V_{os}C_2 \tag{3.6}$$

$$\Sigma Q(\Phi_2) = -V_{os}C_1 + [V_o(n) - V_{os}]C_2 \tag{3.7}$$

The total charge in each phase should be equal: $\Sigma Q(\Phi_1) = \Sigma Q(\Phi_2)$. Therefore, the transfer function is given by:

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \tag{3.8}$$

This technique can be used in switched-capacitor amplifiers, integrators, high-order filters and oversampling A/D converters.

3.2.2.3. Chopping. The chopping technique is a frequency-modulated technique in contrast with auto-zeroing and correlated double sampling, which are time-modulated. The offset and the signal are separated from each other by moving the offset and low-frequency noise to outside the band of interest. Sampling of thermal noise at low

frequencies for auto-zeroing and correlated double sampling causes noise folding. Likewise, noise folding also occurs in chopping, but it is small at high frequencies since the signal harmonics decay with the square of the frequency. An additional advantage of chopping is a lower on-chip capacitance requirement, due to the lack of sample and hold circuitry. The chopper amplifier is formed by a modulator, an operational amplifier, a demodulator and a low-pass filter as shown in Figure 3.11.

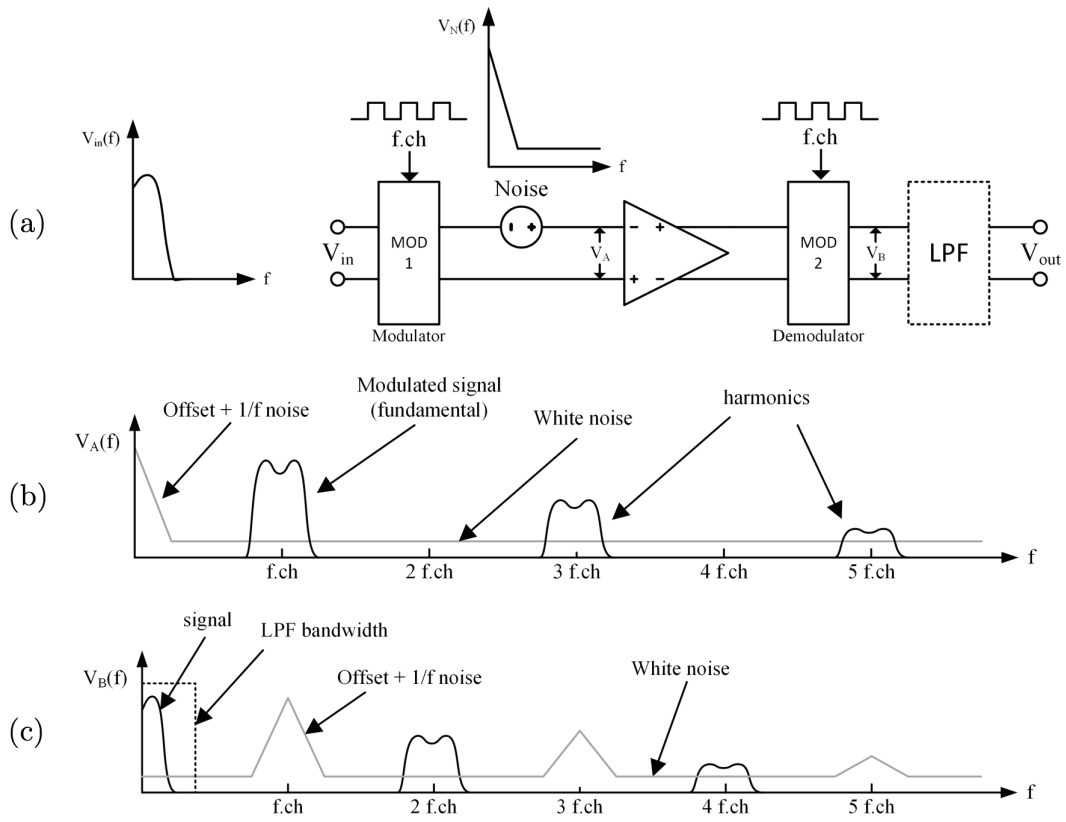

Figure 3.11. Chopper Amplifier Design. (a) Block diagram of chopping amplification. (b) First modulator output. (c) Second modulator output.

The input signal shown in Figure 3.11(a) is modulated to higher frequencies by multiplying the input signal with a carrier wave at chopping frequency. Then, the odd harmonics of the signal are generated with decaying amplitude toward higher frequencies, as shown in Figure 3.11(b). After modulating the input signal, noise and offset are also added to the modulated input signal and the superposition of these is amplified. This is followed by modulation of the amplified signal using the same carrier wave, so that the input signal is demodulated and the noise and offset are modulated,

for the first time, to the odd harmonics of the chopping frequency, as shown in Figure 3.11(c). The harmonics are filtered out and the output signal is eventually cleaned up [46–49].

3.3. Analog-to-Digital Converter

After isolating the output of the sensor from offset and low-frequency noise, the current output of the sensor is converted to voltage with the required amplification. The output of the sensor has to be converted into a digital format so that a microcontroller can process the data, hence an analog-to-digital converter (ADC) is required. While filtering the output after the current integration, it is also amplified by a switched capacitor low-pass filter to be fit into the full-scale range of the ADC. Since the system is planned to be an array of Hall sensors as imager, the placement topology of the ADC has to be considered initially before assessing other requirements of the ADC.

3.3.1. ADC Placement Topologies

There are primarily three different ADC placement topologies which are: chip-level ADC, pixel-level ADC and column-level ADC [50].

3.3.1.1. Chip-Level ADC. A chip-level ADC is dependent on placing the ADC in the final stage of the readout circuitry. Since the ADC is located after an array, chip-level ADC placement allows the ADC to span a larger area. The ADC area is confined to the pixel pitch for other architectures. Therefore, this method is the simplest to implement when considering the layout. Chip-level ADC placement is demonstrated in Figure 3.12.

Sampling frequency of the ADC is found by multiplying the frequency of processing a single pixel by the number of rows and columns. Since the sampling frequency increases as the pixel array grows, this topology needs a very high-speed ADC. One of the biggest advantages of this topology is its uniformity, i.e., a single ADC is used to

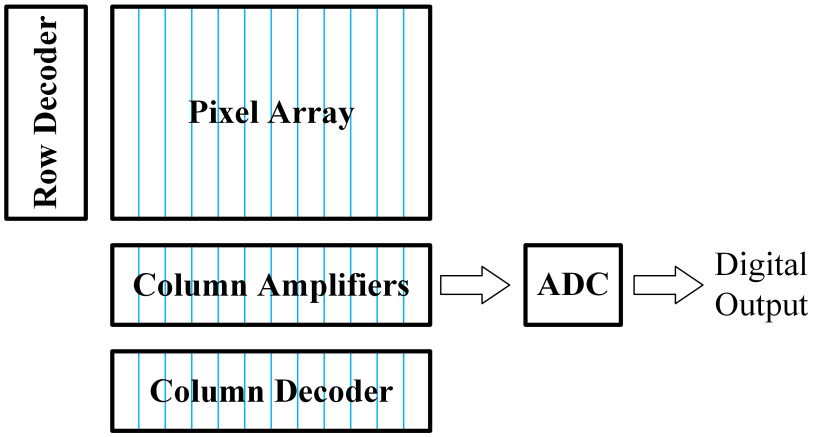

Figure 3.12. Chip-level ADC Placement Topology.

convert all the pixels as opposed to in other topologies where components with different offset voltages do not share the same ADC. On the other hand, designing a very high-speed ADC for larger arrays is difficult. Furthermore, the high speed requirement degrades the power efficiency of the ADC.

3.3.1.2. Pixel-Level ADC. The number of ADCs used in this topology is equal to the pixel count; each pixel is converted with a different ADC. Hence, the speed of each ADC does not need to increase with array size. Since the analog circuits are placed inside each pixel, it provides lower noise level and highest SNR with respect to other topologies. A pixel-level ADC topology is presented in Figure 3.13. The main disadvantage of this topology is that the ADC has to fit within a pixel pitch which places a limit on the layout.

3.3.1.3. Column-Level ADC. Also called column parallel ADC, this placement topology is the most suitable of the three because it optimizes both the layout area and sampling frequency. Each column has a particular ADC introduced into the column readout channels. It has a moderate sampling frequency that is lower than that of a chip-level ADC and higher than that of a pixel-level ADC. Sampling frequency of the column-level ADC is the product of the frequency of processing a single pixel by the number of rows. A column-level ADC placement topology is shown in Figure 3.14.

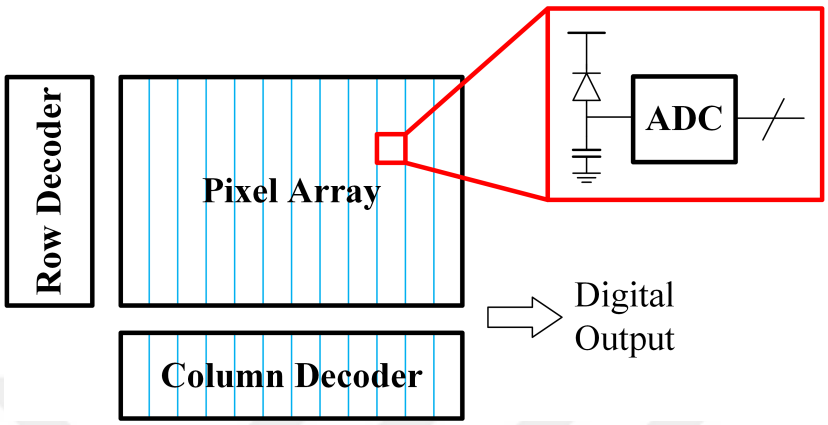

Figure 3.13. Pixel-level ADC Placement Topology.

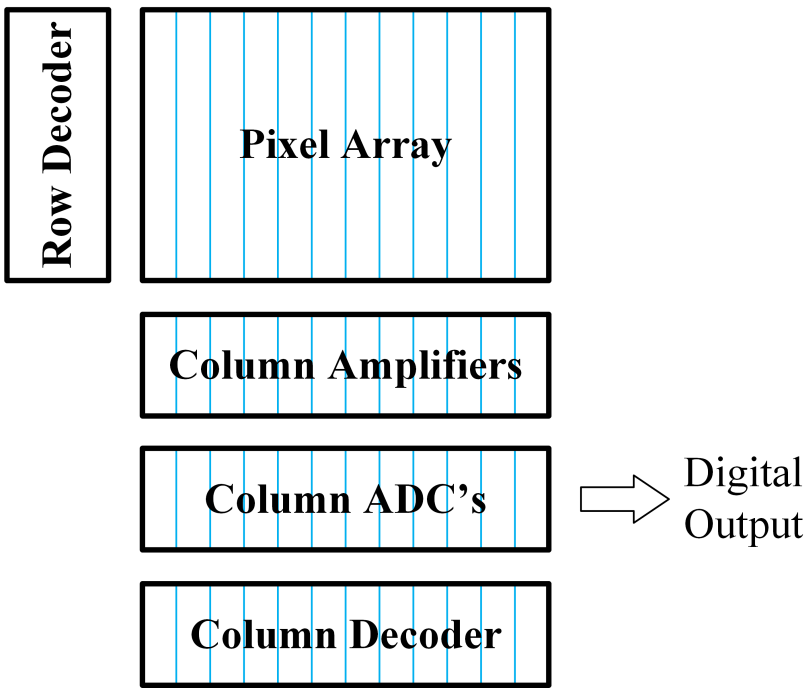

Figure 3.14. Column-level ADC Placement Topology.

The main drawback of the column parallel ADC is the layout area limitation. The width of the ADC layout cannot go beyond the pixel pitch. However, there is no restriction on the length of the ADC. Another disadvantage of this topology is that each column ADC may have a different amount of offset and this results in *fixed pattern noise*.

Considering all types of placement topologies, column-level ADC placement is usually the ideal choice but requires a realizable sampling frequency and sufficient layout area [50].

3.3.2. ADC Architectures Suitable for Column-Level ADC Placement

Since the column parallel ADC placement is the optimal choice in terms of layout and sampling speed, various ADC architectures can be used for implementing this topology. Among the most widely used architectures are: Integrating ADC, SAR ADC, Cyclic ADC and Sigma Delta ADC [10, 51]. Due to its larger layout area requirement and higher power consumption in comparison with other architectures, Pipeline and Flash ADC are not preferred ADC architectures for column parallel placement.

3.3.2.1. Integrating ADC. Integrating analog-to-digital converters are used in implementing highly accurate data conversion on slow signals at a widespread scale. They are frequently used in imaging devices due to the easier implementation and simpler circuitry. They are also conventionally used in measurement instruments like multimeters. The most basic implementation of integrating converters is the single-slope ADC.

The building blocks of a single-slope ADC are a comparator, a counter, a ramp generator and memory. The counter is incremented for each clock cycle simultaneously with the ramp generator. The comparator compares the ramped signal with the analog sampled input, and is triggered when the ramped signal passes over the sampled signal. Then, the value of the counter is saved onto the memory. The comparator and memory

elements are applied to each column while a single ramp generator and digital counter are shared throughout the circuit. The single-slope ADC architecture is shown in Figure 3.15.

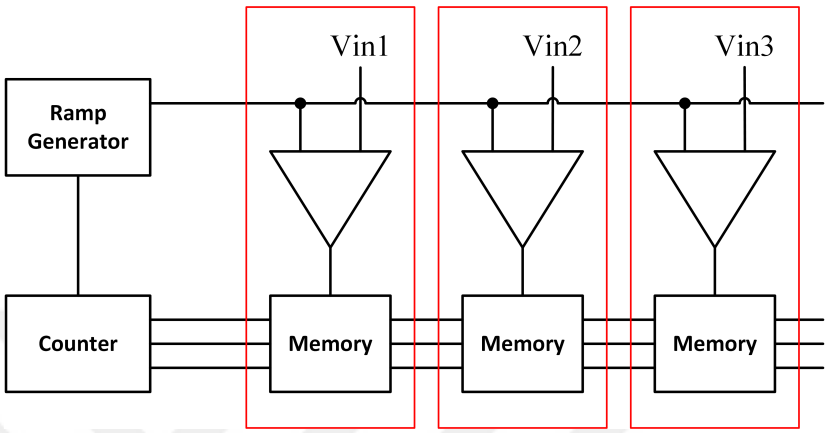

Figure 3.15. Single-Slope ADC Architecure.

The conversion rate is the fundamental constraint for this architecture. The resolution of the ADC limits the speed of the application, hence it is not preferred when both high speed and high resolution are required. The clock frequency can be found as:

$$f_{\text{clock}} = 2^n \times f_{\text{sampling}} \tag{3.9}$$

where n is the resolution of the ADC. The single-slope ADC is suited to applications that require up to 12 bits of resolution and a conversion rate of less than 100k samples per second. Various modifications have been attempted in order to increase the conversion rate. The dual-slope ADC [52], the two-step ramp [53] and multi-ramp ADC [54] are among the examples introduced in the literature.

3.3.2.2. Successive-Approximation Register (SAR) ADC. Successive-approximation ADCs are one of the most widely used architectures in implementing analog-to-digital conversion for its quick conversion time, less power consumption and high accuracy. The main building blocks of a SAR ADC are a comparator, a digital-to-analog converter (DAC) and a register. The basic operation of SAR converters is similar to the

binary search algorithm used to determine the closest digital representation of an analog signal. The input signal is sampled and then compared with the DAC's output at each clock cycle. After the comparison, the previous reference voltage is halved and then added to or subtracted from the DAC's output based on the comparator decision. A block diagram of the SAR ADC is presented in Figure 3.16.

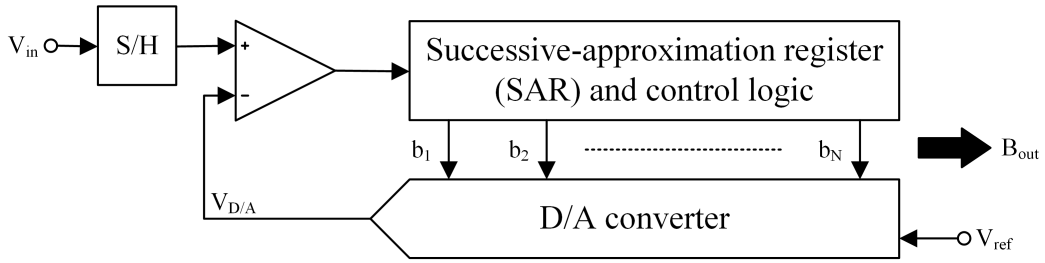

Figure 3.16. Block Diagram of the SAR ADC [10].

In order to minimize errors caused by mismatch and to increase the resolution, the DAC is designed using adequately large capacitors which make the area of a SAR ADC relatively big. N clock cycles are required to complete an N-bit conversion, leading to less power consumption. However, it is used less often compared to single-slope ADCs for column parallel placement.

3.3.2.3. Cyclic ADC. The cyclic ADC and the SAR ADC have similarities in their operations. While a SAR ADC halves the reference voltage, a cyclic ADC doubles the error voltage in each cycle. The reference remains the same in a cyclic ADC. Although cyclic ADCs allow operation at high frequencies, they are not suited for low power requirement applications [55]. A cyclic ADC spans less area compared to a SAR ADC, but more power is required due to the use of a low-noise amplifier. The reason for the preference of cyclic ADCs over single-slope ADCs is that the former provides a higher conversion rate. Cyclic ADCs are also preferable to SAR ADCs because they need smaller layout area. Similar to a SAR ADC, one bit of conversion is achieved in each clock cycle of a cyclic ADC. The architecture of a cyclic ADC is illustrated in Figure 3.17.

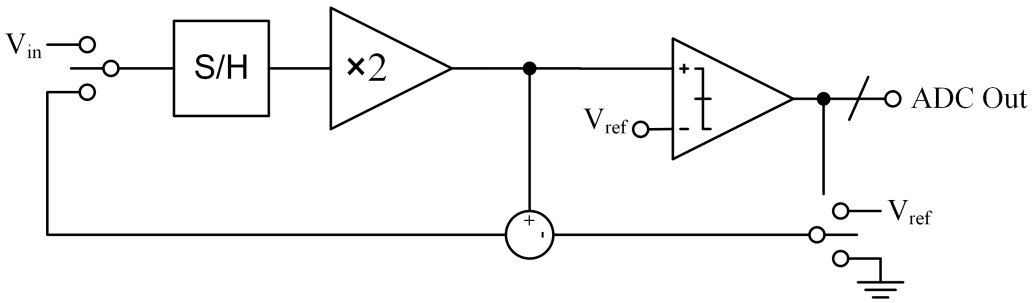

Figure 3.17. The Cyclic ADC Architecture.

3.3.2.4. Sigma Delta ADC. Sigma Delta A/D converters have gained popularity for their high resolution conversion thanks to their oversampling and noise shaping properties. The input signal is sampled at a rate higher than the Nyquist rate, and this sampled input is modulated and compared with the reference voltage. The comparator output is fed back through a DAC to the summing node. Thus, the average DAC output voltage is made to equal the input voltage by sampling many times. Then the comparator output is filtered out using a digital decimation filter. The noise is suppressed by making use of modulation and demodulation processes. Noise suppression can be increased by increasing the order of modulation. The block diagram of a first order Sigma Delta ADC is shown in Figure 3.18.

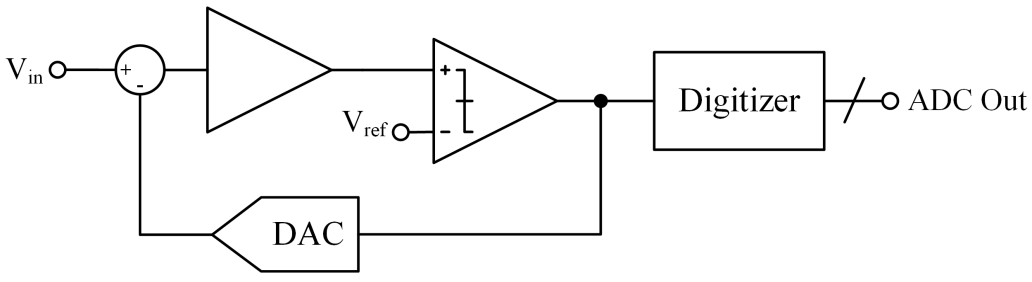

Figure 3.18. Block diagram of a first order Sigma Delta ADC.

3.3.3. Comparison of ADC Architectures

While choosing the most suitable ADC for a given application, ADC architectures must be evaluated based on various parameters such as power consumption, area, resolution and conversion rate. Table 3.1 presents a comparison of ADC architectures appropriate for column parallel ADC placement [56].

Table 3.1. Comparison of ADC architectures for column parallel ADC placement.

ADC Architecture	**Conversion Speed**	**Layout Area**	**Resolution**	**Power**
Single-Slope	Medium	Low	Medium	Low
Cyclic	High	Medium	Medium	Medium
SAR	High	High	Medium	Low
Sigma Delta	Medium	Medium	High	Medium

10 bits of resolution with a medium conversion speed would be sufficient for a Hall-effect sensor array readout circuit. The single-slope ADC meets these criteria besides its simple implementation.

4. BUILDING BLOCKS

In this chapter, comprehensive design methods for each integrated building block used in the sensor microsystem are presented. Each section of this chapter outlines the relevant simulation results, aspect ratios (W/L) of the transistors and necessary analyses for a building block.

4.1. Current Mode Hall Effect Sensor Microsystem Top Level Architecture

The integrated current-mode Hall-effect sensor array microsystem includes various analog integrated circuit blocks such as amplifiers, filters and ADCs. First, a sensor biasing circuit is used to equalize the currents flowing into and out of the twin Hall-effect sensor structure. Following this, a 4-phase current spinning technique including the digital control unit for generating clock signals is implemented to reduce offset and low-frequency noise of the sensor. In addition to that, integration detection topology is utilized to convert Hall current into voltage, which provides better noise performance. The Hall current is integrated over the integration capacitor during a specified time interval that determines the transresistance gain. The operational amplifier used in the integrator is designed as a chopper amplifier to achieve better offset and flicker noise performance by means of chopper switches. This is because the noise generated by the amplifier should be sufficiently below the noise of the sensor to prevent distortion of the data to be measured. The signal is modulated to the chopping frequency before amplification followed by demodulation by the same chopping frequency. This brings the signal back to the base band while the offset and low-frequency noise remain at the chopping frequency since they are only amplified and modulated. Therefore, low-pass filtering is required to remove the offset and low-frequency noise components. An elliptic fifth order switched capacitor low-pass filter is designed to filter out the offset and noise. Finally, a single-slope analog-to-digital converter is implemented in order for the sensor data to be processed by the microprocessor.

4.2. Twin Current Mode Hall Sensor Structure with Current Spinning Technique

The cross-shaped Hall plate has the appropriate geometry to take the advantage of the 4-phase current-spinning technique. As explained in Section 3.1, 4-phase current-spinning allows us to cancel all different sources of offset by interchanging the input and output terminals periodically. As shown in Figure 4.1, the switches are controlled by four clock signals, CLK_1, CLK_2, CLK_3 and CLK_4. The biasing current is supplied between two terminals while the output is obtained across the remaining two terminals during each phase so that the Hall plate completes a 360° rotation. An implementation of the technique using 32 switches is shown in Figure 4.2. Each switch is designed as a complementary CMOS pair.

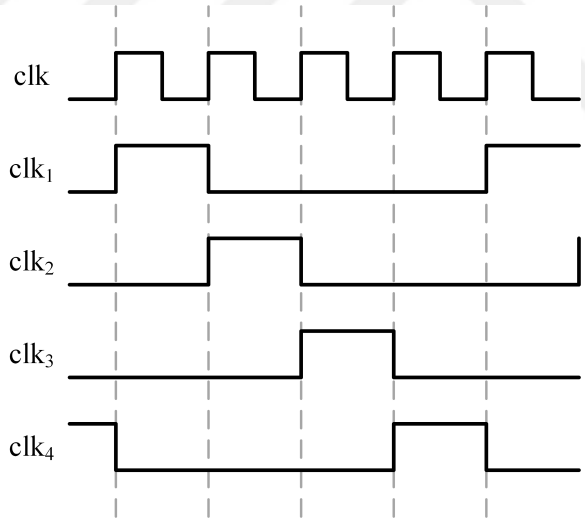

Figure 4.1. Non-overlapping clock distribution for current spinning operation

The detailed structure of twin cross-shaped Hall plate for each clock cycle is demonstrated in Figure 4.3.

4.2.1. Switch Design

Many switches are used in both current spinning and chopping blocks. When an ideal switch is on or off, the impedance is zero or infinite respectively. However, CMOS switches cannot achieve this criterion in practice. Therefore, non-idealities of

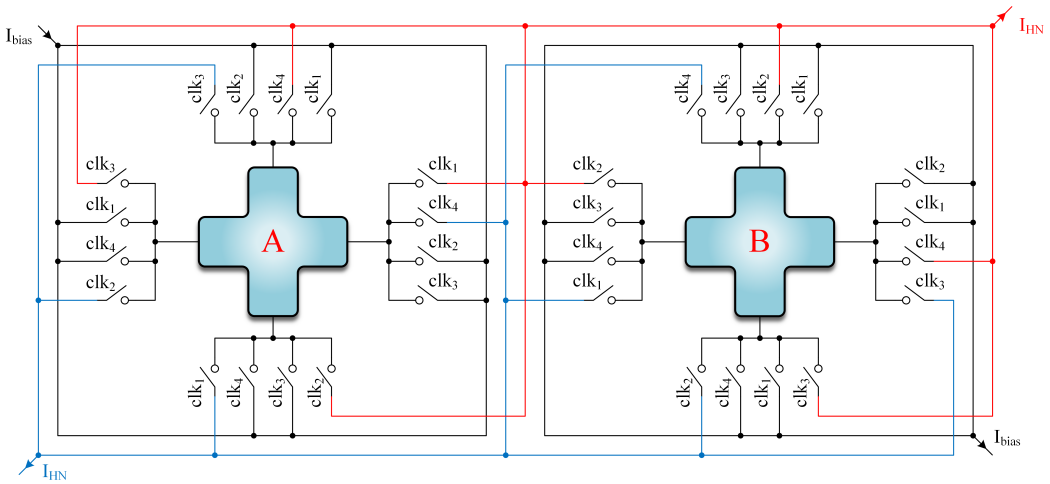

Figure 4.2. Twin Current Mode Hall Sensor Structure with Current Spinning

switches such as resistance, charge injection and clock-feedthrough have to be considered carefully, and design modifications must be made to suppress the effects of these imperfections [57].

4.2.1.1. Switching non-idealities. A single NMOS or PMOS device can be used as a switch. An NMOS switch configuration is shown in Figure 4.4.

The switches should be designed such that the on-resistance should be as low as possible to prevent voltage drop. Also, on-resistance becomes a critical specification when lower noise is desired. The on-resistance R_{on} exhibited when using a single NMOS device is given by:

$$R_{on} = \left[\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{in} - V_{TH})\right]^{-1} \tag{4.1}$$

Equation (4.1) shows that on-resistance of a switch depends on the input voltage V_{in}, and approaches large values as the input voltage tends to $V_{DD} - V_{TH}$. The total charge in the inversion layer when the switch is on can be expressed as:

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}). \tag{4.2}$$

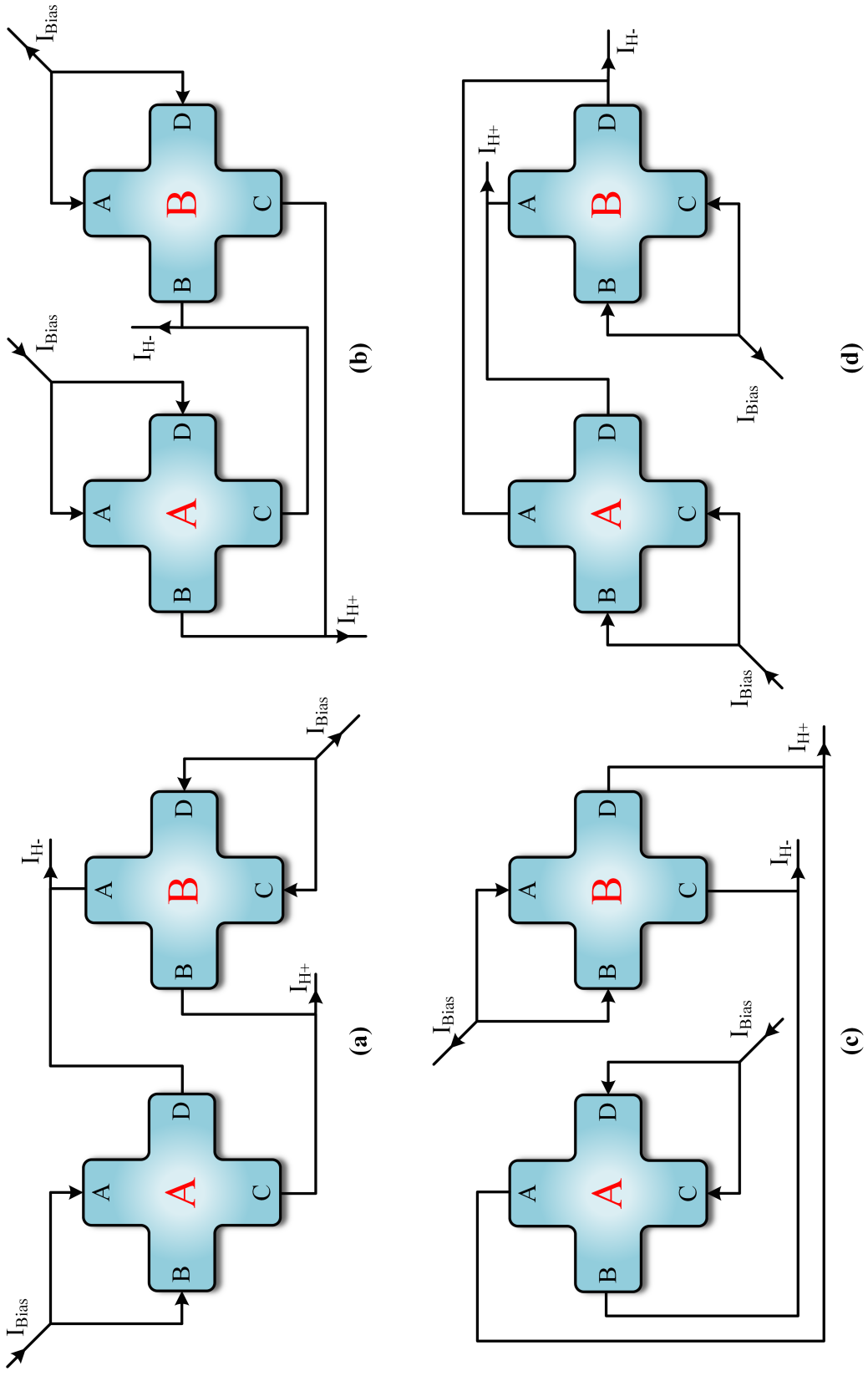

Figure 4.3. Detailed structure of twin cross-shaped Hall plate for each clock cycle.

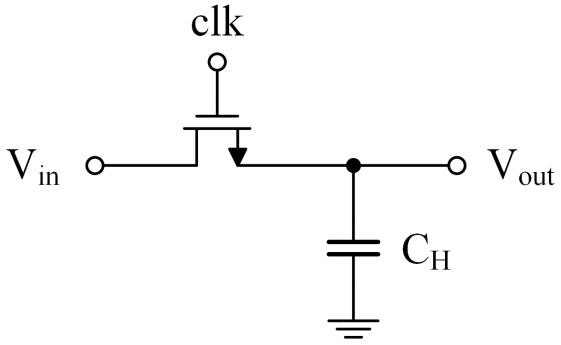

Figure 4.4. Switch implementation using an NMOS device.

After the switch is turned off, minority carriers exit through source and drain terminals as shown in Figure 4.5. This is called charge injection.

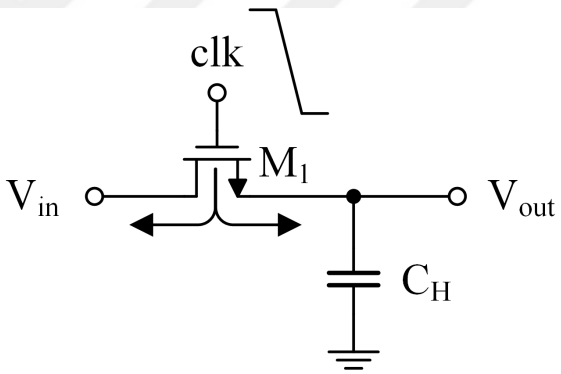

Figure 4.5. Charge injection when the switch turns off.

The charge injection through the input side does not cause an error, since it is absorbed there. However, the charge injected into the other side is accumulated on the capacitor and results in an error in the output voltage. The error is given by

$$\Delta V = \frac{1}{2C_H} W L C_{ox} (V_{DD} - V_{in} - V_{TH}) \tag{4.3}$$

assuming that the charge injection is distributed equally to both sides.

Another error source is called the clock feedthrough. The coupling through overlap capacitance causes an error at the output when the clock swings from high to low as shown in Figure 4.6

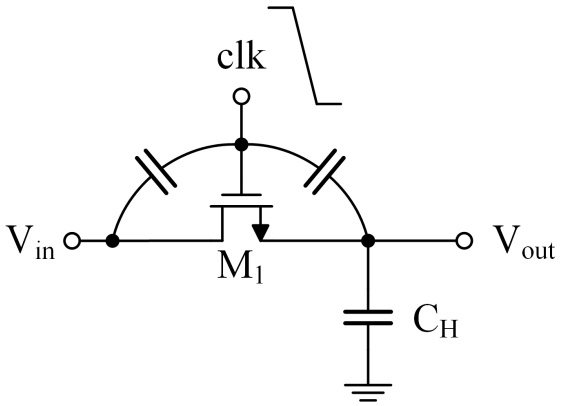

Figure 4.6. Clock feedthrough.

The error due to clock feedthrough can be expressed as

$$\Delta V = V_{CLK} \frac{WC_{ov}}{WC_{ov} + C_H} \tag{4.4}$$

where C_{ov} is the overlap capacitance per unit width. Since the error does not depend on the input voltage, it behaves as a constant offset. There is a significant trade-off between speed and precision due to these errors and so these should be configured accordingly. Various techniques that have been developed to reduce the on-resistance and the charge injection error are discussed next.

4.2.1.2. Methods to reduce effects of non-idealities. The use of larger sampling capacitors and transistors with a minumum size equal to the switch size slows the switching speed or leads to higher resistanc despite charge injection reduction. Making use of dummy switches, complementary CMOS pairs and differential circuits are practical techniques to combat errors due to non-idealities.

(a) *Complementary CMOS pairs:* In response to the input voltage growth, when the on-resistance of the PMOS switch decreases, the on-resistance of NMOS switch increases as shown in Figure 4.7.

Therefore, combinations of NMOS and PMOS switches as parallel decreases the on-resistance of the switch at the expense of requiring complementary clocks. The

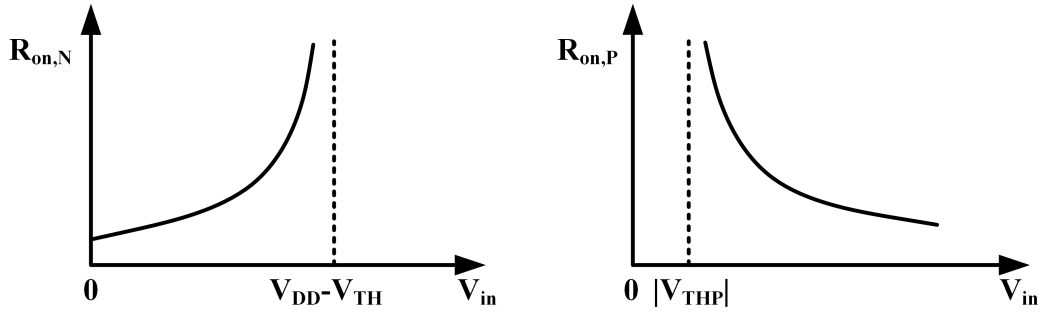

Figure 4.7. On-resistance of NMOS and PMOS switches in response to input voltage.

equivalent resistance of a complementary CMOS pair is shown in Figure 4.8 and can be expressed as:

$$R_{on,eq} = R_{on,N}||R_{on,P} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N (V_{DD} - V_{in} - V_{THN})}\Bigg|\Bigg|\frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_P (V_{in} - |V_{THP}|)}$$

$$= \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N (V_{DD} - V_{THN}) - \left[\mu_n C_{ox}\left(\frac{W}{L}\right)_N - \mu_p C_{ox}\left(\frac{W}{L}\right)_P\right] V_{in} - \mu_p C_{ox}\left(\frac{W}{L}\right)_P |V_{THP}|}$$

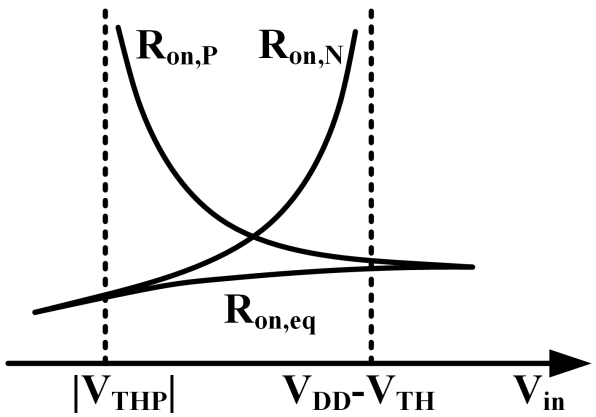

Figure 4.8. Equivalent on-resistance of complementary switch.

$R_{on,eq}$ does not depend on the input voltage when $\mu_n C_{ox}(W/L)_N$ and $\mu_p C_{ox}(W/L)_P$ are equalized. As shown in Figure 4.9, $R_{on,eq}$ exhibits far less deviation compared to on-resistance of each switch by itself. The source of error that needs particular attention in this configuration is the production of complementary clocks. If the complementary switches do not turn off simultaneously, it results in distortion in the output.

A further advantage of complementary CMOS switches is the elimination of charge injection by introducing opposite charge packets that cancel each other as shown in Figure 4.9. The charge of electrons should be equal to the charge of holes for the cancellation, hence the following equality holds:

$$W_1 L_1 C_{ox}(V_{CLK} - V_{in} - V_{THN}) = W_2 L_2 C_{ox}(V_{in} - V_{THP}) \tag{4.5}$$

Therefore, charge injection cancellation is achieved only for one input value. Also, cancellation is not achieved for clock feedthrough since the overlap capacitances of PMOS and NMOS are not equal.

(b) *Dummy Switches:* The charge injection of the main transistor can be eliminated with the help of a dummy transistor. The half of the charge injection going towards the sampling capacitance can be removed by the dummy transistor that is half the size of the main transistor and is driven by the opposite clock. It is assumed that the charges are distributed equally towards both input and output sides, thus the dummy transistor is sized to be half the size of the main transistor. However, the assumption of equal charge distribution does not hold due to different load impedances and the inability to achieve symmetry in the layout. Addition of a dummy switch is shown in Figure 4.9. In addition to charge injection, clock feedthrough is also suppressed when the width of the dummy switch is adjusted to half that of the main switch.

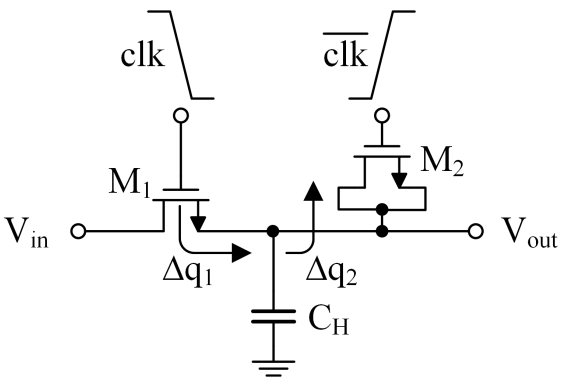

Figure 4.9. Addition of dummy switch to reduce the effects of charge injection and clock feedthrough.

(c) *Differential Circuits:* The charge injection problem can be overcome by means of a differential circuit as shown in Figure 4.10.

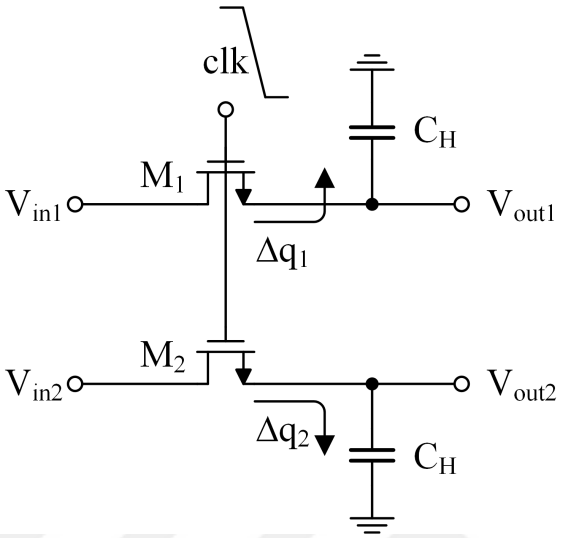

Figure 4.10. Differential sampling circuit with charge injection.

The charge injected into each capacitor can be expressed as

$$\Delta q_1 = WLC_{ox}(V_{CLK} - V_{in1} - V_{TH1}), \text{ and, } \Delta q_2 = WLC_{ox}(V_{CLK} - V_{in2} - V_{TH2}).$$

Therefore, charge injection is cancelled only when input voltages are equal. Nonetheless, offset is removed through differential operation. In addition, the second order harmonics are eliminated which reduces the nonlinear component.

4.2.2. Hall Sensor Model Simulations

The cross-shaped current-mode Hall sensor is modeled in VerilogA as given in Apendix A. Various simulations have been performed to examine the main features of the sensor. The change of Hall current with respect to magnetic field for a single Hall plate is shown in Figure 4.11. A 10 μA current is used for biasing the sensor and the Hall current is measured up to a magnetic field of 20 mT.

As shown in Figure 4.11, the Hall current deviates by 2.39 nA with a change of 20 mT in the magnetic field. Therefore the sensitivity is found as 119.5 nA/T. The

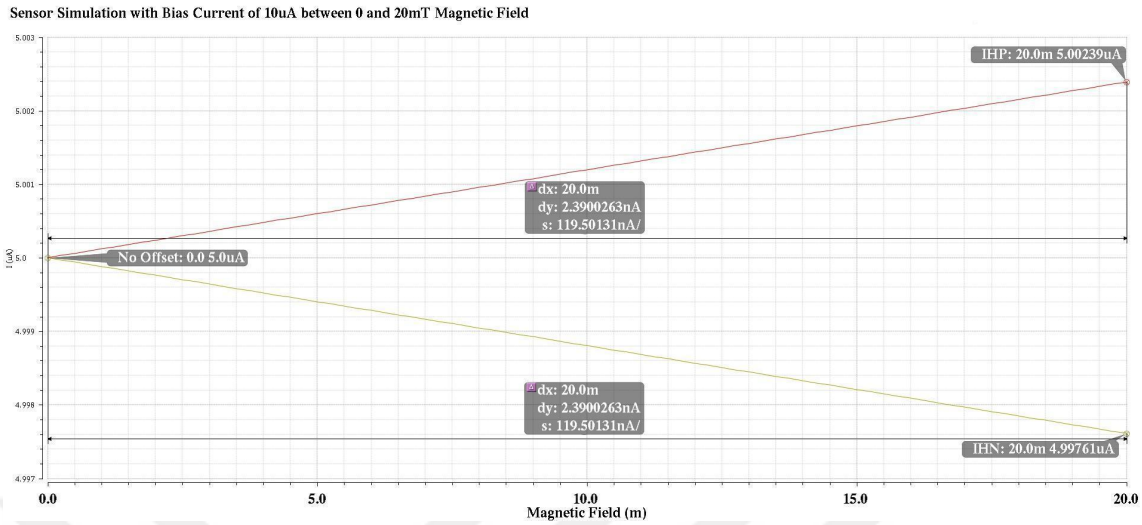

Figure 4.11. Single Hall sensor simulation with 10 μA bias current and magnetic field between 0 and 20 mT.

width over length ratio of the Hall plate is taken as 2.55 since it is the optimum ratio to achieve the best sensitivity as shown in Figure 4.12.

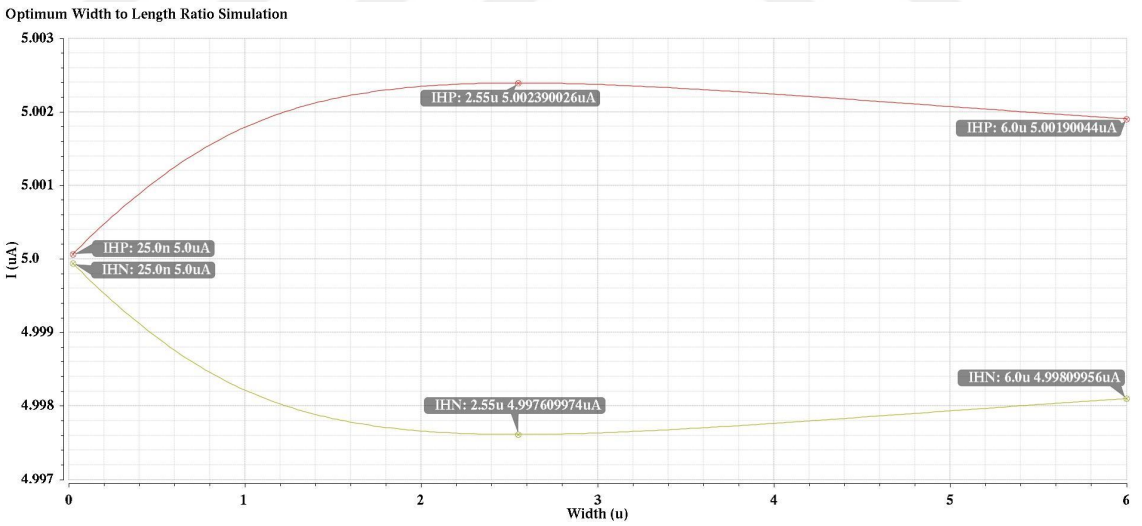

Figure 4.12. Optimum Sizing for a Hall plate.

The geometrical correction factor has a significant influence on sensor sensitivity. The length of the plate is taken as 1 μm and the width is increased up to 6 μm at intervals of 25 nm. The maximum Hall current is obtained when the width equals 2.55 μm. A pair of Hall sensors is utilized to measure the magnetic field since it doubles the sensitivity and is suitable for 4-phase current spinning to eliminate the

offset. Simulation results of a twin Hall plate structure without offset are presented in Figure 4.13.

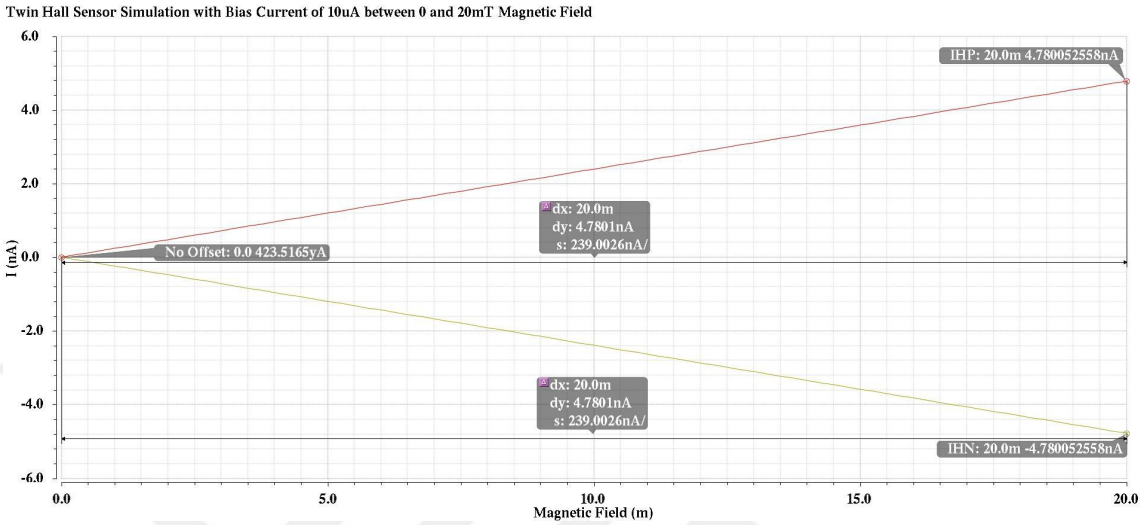

Figure 4.13. Simulation results of twin Hall plate structure without offset.

It can be seen from Figure 4.13 that the sensitivity is doubled in comparison with a single Hall plate structure. Another crucial point to note is the effect of bias current on the sensitivity. It is obvious from Equation (2.19) that the current sensitivity does not depend on biasing current and the simulation results shown in Figure 4.14 also support this view.

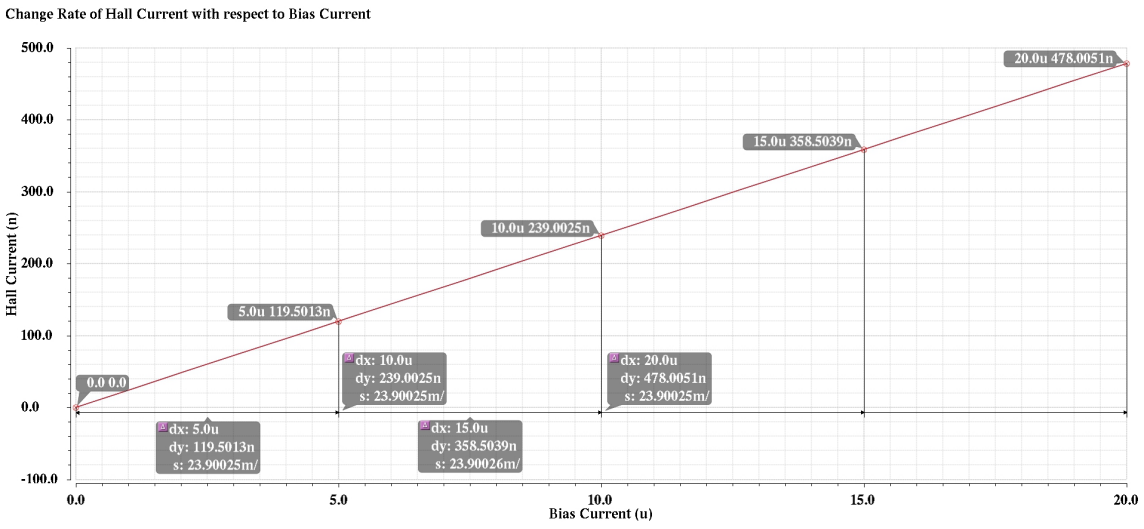

Figure 4.14. The rate of change for Hall current with respect to biasing current

The absolute sensitivity over biasing current is always constant for each biasing current as shown in Figure 4.14. Therefore, biasing current plays no role in determining sensitivity and only affects the power consumption.

In order to introduce an offset into a Hall sensor, the resistance values of δR_1, δR_2, δR_3, and δR_4 in Figure 2.11 are taken as 1 Ω. Simulation results of twin hall sensor structure including the effect of offset is shown in Figure 4.15.

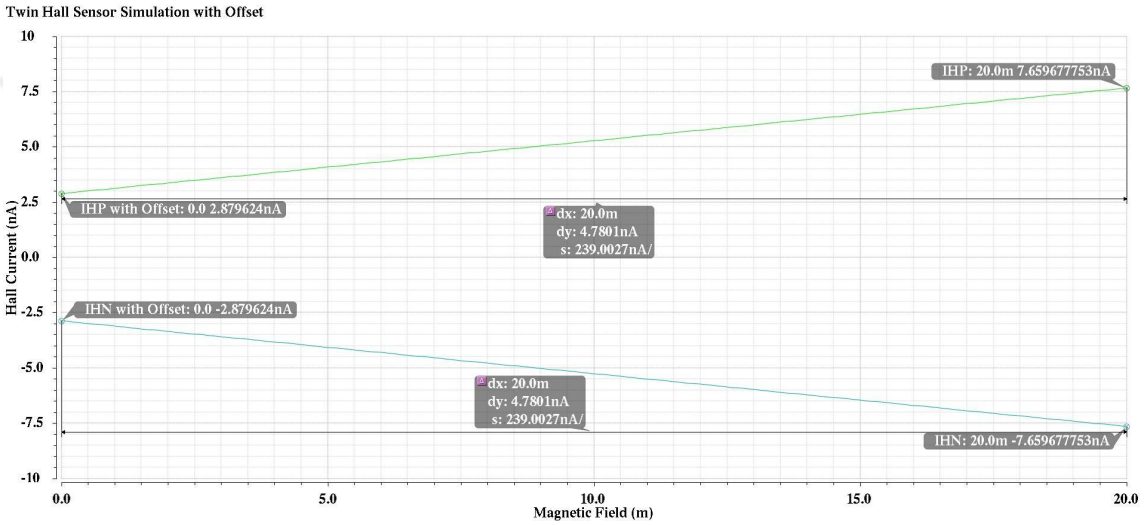

Figure 4.15. Twin Hall sensor simulation including the effect of offset.

Typically, the 1 Ω resistance that defines the effects of offset is much larger than normal, thus it creates an offset greater than what would result under ordinary conditions. However, it can still be eliminated using current spinning.

Design of a current spinning architecture requires a clock divider circuit. The digital circuit shown in Figure 4.16 is designed to generate four non-overlapping clock signals by dividing the main clock cycle into four intervals.

The clock generation circuit requires three D flip-flops with asynchronous reset and a D flip-flop with asynchronous set and reset to trigger the circuit as shown in Figures 4.17 and 4.18, respectively.

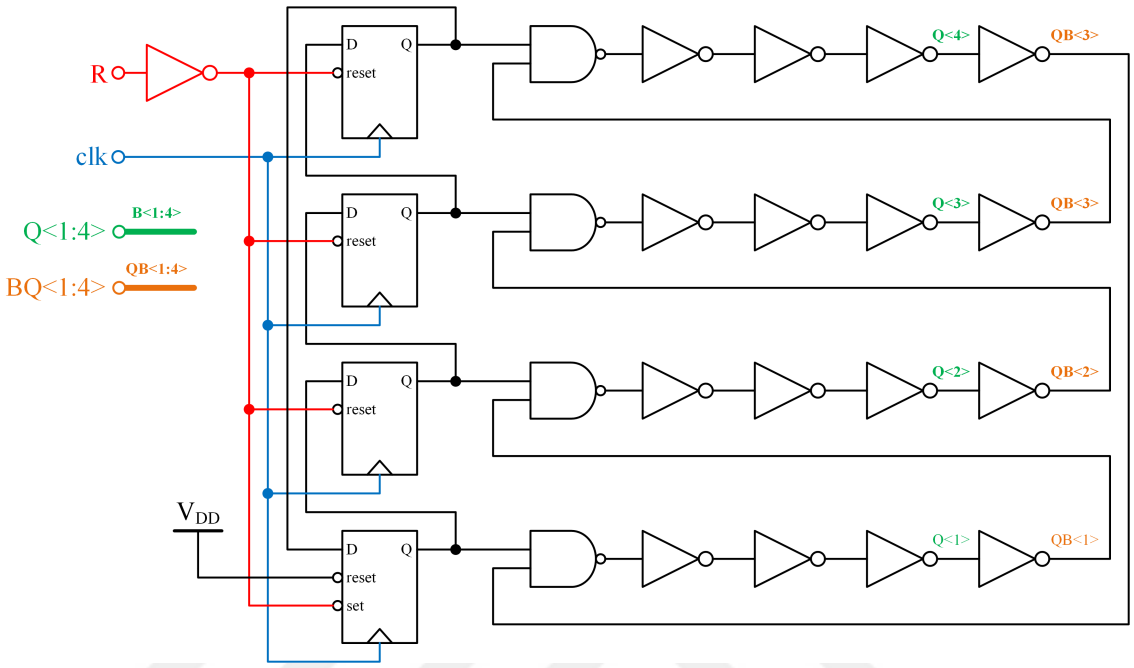

Figure 4.16. Clock generation circuit.

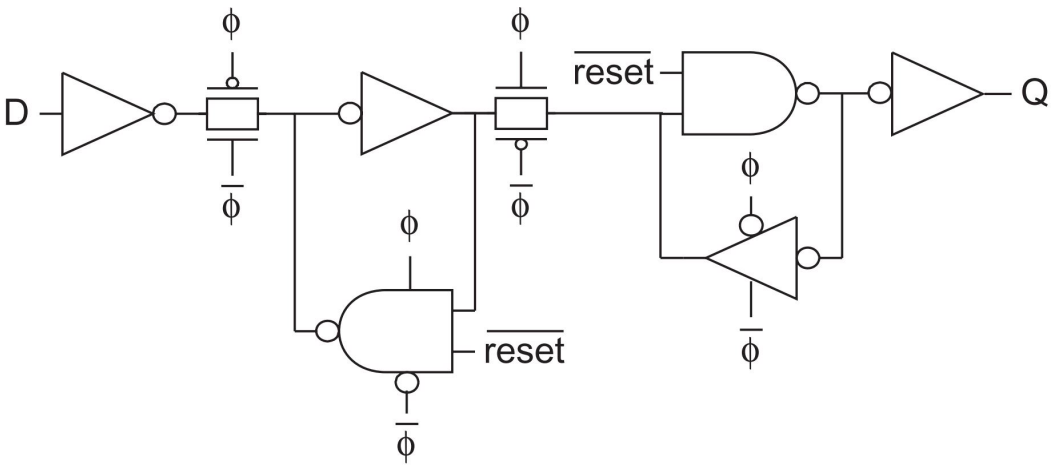

Figure 4.17. D flip-flop with asynchronous reset.

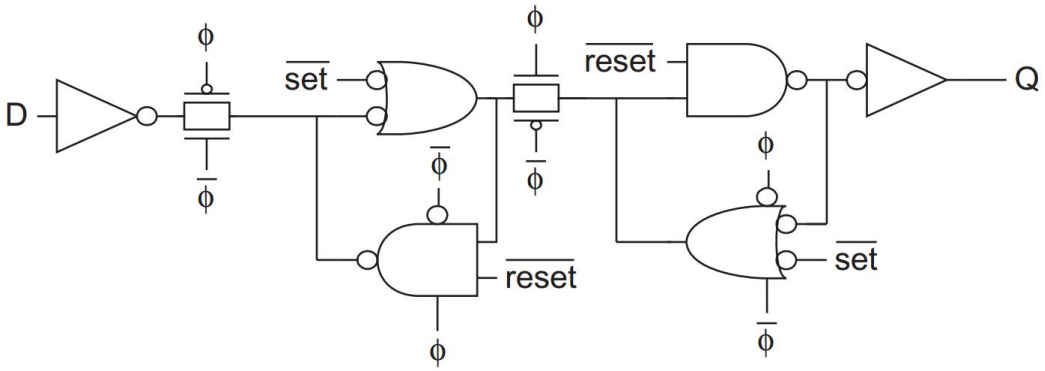

Figure 4.18. D flip-flop with asynchronous set and reset.

The main clock with 1 MHz frequency generates four non-overlapping clocks as shown in Figure 4.19.

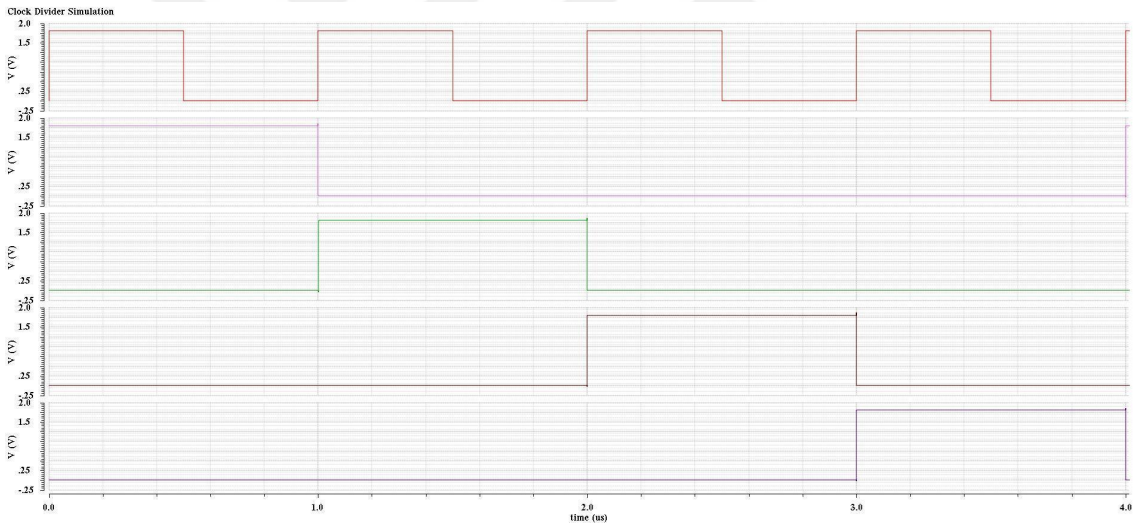

Figure 4.19. Simulation results of the clock generation circuit.

The simulation results of current spinning are demonstrated in Figure 4.20. The Hall current values are labeled for each phase of current spinning at different magnetic fields.

The Hall current is measured for magnetic fields of 0 T, 4 mT, 8 mT, 12 mT, 16 mT and 20 mT. As shown in Figure 4.15, an offset of approximately 5.76 nA is observed at a magnetic field of 0 T before spinning. The Hall current under a 0 T magnetic field is 5.076 nA, -5.001 nA, 5.1602 nA, and -5.085 nA for different phases. The sum of these currents is very close to 0, hence offset becomes zero after completing

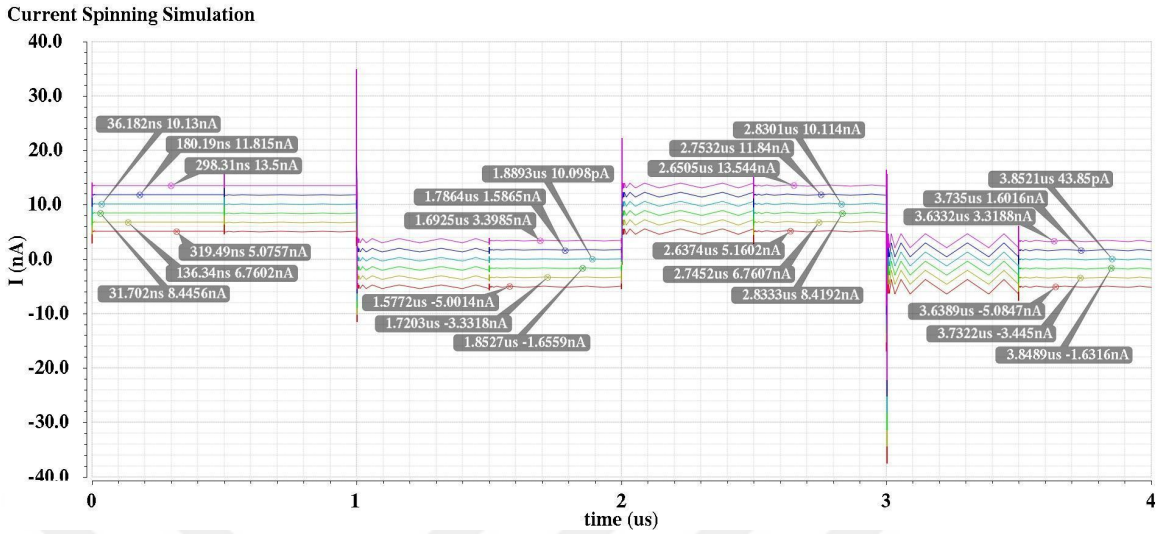

Figure 4.20. Simulation results of current spinning.

the current spinning operation. Current spinning also reduces the low-frequency noise of the sensor in addition to the offset. Figures 4.21 and 4.22 show the noise response of the sensor before and after current spinning.

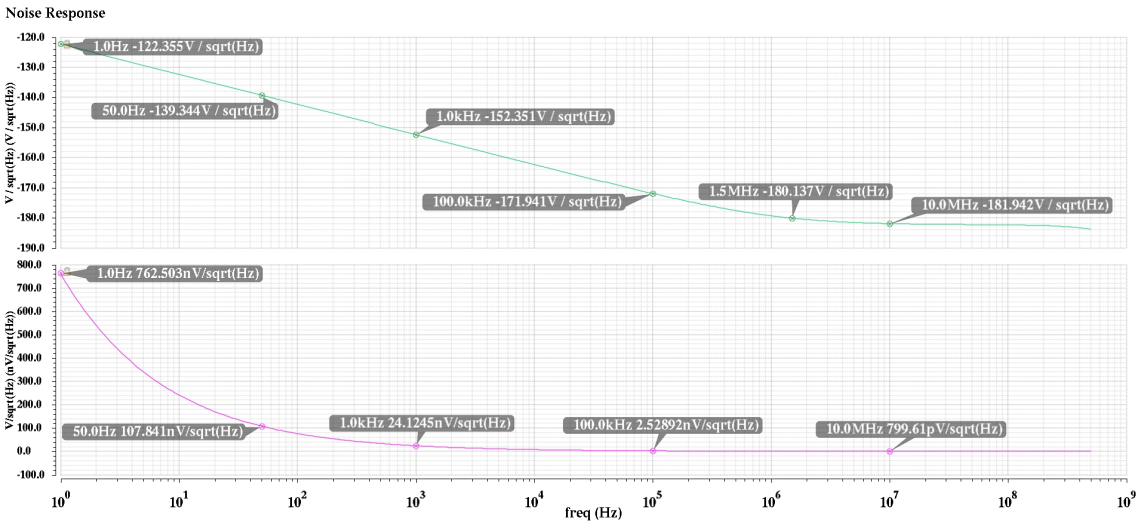

Figure 4.21. Noise response of Single Hall plate structure without current spinning.

4.3. Sensor Biasing Circuit

A pair of cross-shaped current-mode Hall sensor structures with current spinning requires two identical input currents to source and sink the equivalent currents. The mismatch between the transistors results in bringing the transistors to linear region,

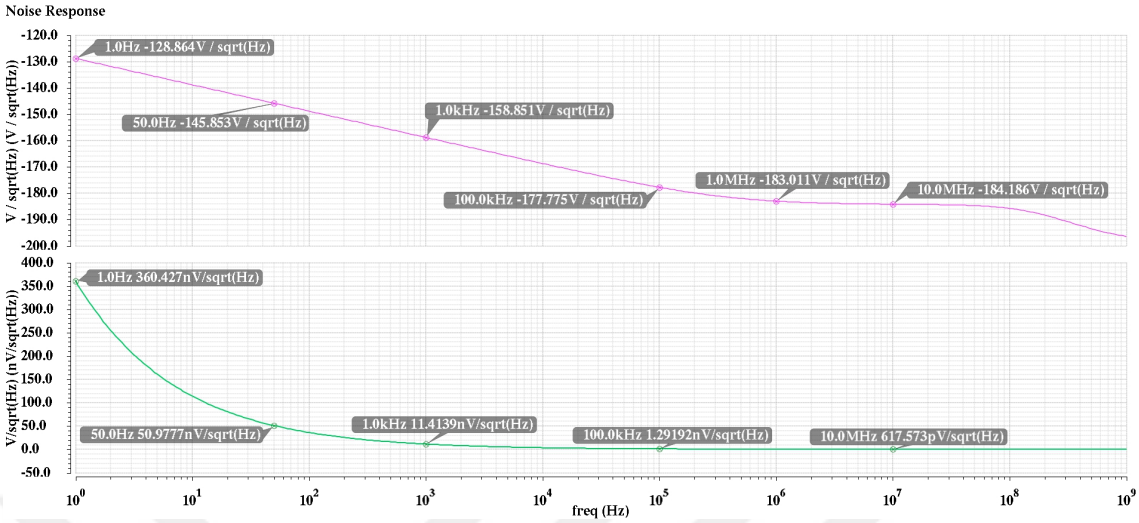

Figure 4.22. Noise response of twin Hall plate structure with current spinning.

thus generating different currents. Implementing a common mode feedback (CMFB) circuit overcomes the problem of mismatch and helps to keep source and sink currents identical. The common-mode voltage is detected by the CMFB circuit and compared with a reference voltage. Minimizing the resulting error eliminates the mismatch in bias currents and provides an output voltage that is close to the desired value. The schematic of the biasing current circuit is shown in Figure 4.23.

The P-type cascode current mirror makes a replica of bias current to produce a source current for the Hall plates, and the N-type cascode current mirror generates a sink current. The differential pair of M_{13} and M_{14} is used to implement the CMFB circuit. The voltage at the sensor output is matched to the common-mode voltage V_{CM} with current flowing through M_{12} which is replicated by transistors M_{15}-M_{18}. The current flowing through M_{11} is equal to sum of the currents in M_{12}, M_{13} and M_{14}. The gate voltages of M_{13} and M_{14} change such that as one increases, the other decreases, but the sum of the gate voltages of these transistors is constant and equal to $2V_{CM}$. Therefore, the sum of the currents flowing through M_{13} and M_{14} is fixed. These current

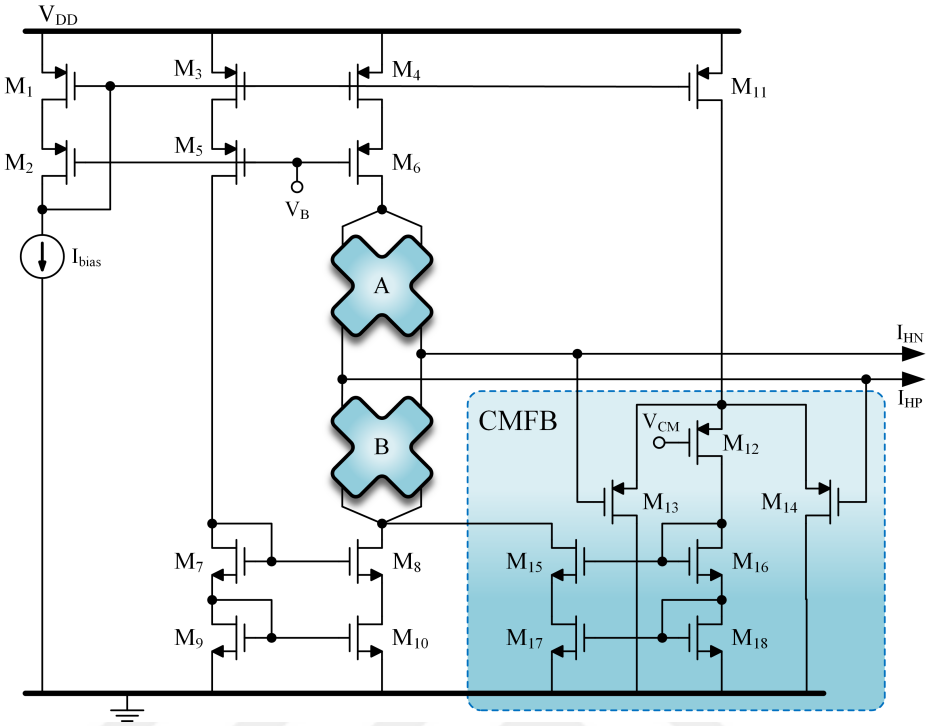

Figure 4.23. Schematic of twin Hall sensor structure biasing and CMFB circuit.

and voltage relationships are expressed in Equations (4.6)—(4.9).

$$I_{D_{M11}} = I_{D_{M12}} + I_{D_{M13}} + I_{D_{M14}} \tag{4.6}$$

$$V_{CM} = \frac{1}{2}(V_{G_{M13}} + V_{G_{M14}}) \tag{4.7}$$

$$I_{D_{M13}} + I_{D_{M14}} = I_{\text{constant}} \tag{4.8}$$

$$I_{D_{M11}} = I_{D_{M12}} + \left(\frac{1}{2}I_{\text{constant}} + \Delta I\right) + \left(\frac{1}{2}I_{\text{constant}} - \Delta I\right) \tag{4.9}$$

Equation (4.9) indicates that the current $I_{D_{M11}}$ flowing through M_11, does not change even under the influence of large differential voltages, thus identical currents are generated and the output voltages are brought to the desired level eventually. Table 4.1 lists the design parameters for the biasing and the CMFB circuit.

The biasing current, I_{bias}, in Figure 4.23 is configured to be 10 μA. It is generated by a current reference circuit across a wide range of temperatures.

Table 4.1. Design parameters for biasing and CMFB circuit.

Parameter	**Value**	**Finger**	**Multiplier**
M_1 — M_6, M_{11}	4.26 μm / 4 μm	1	2
M_7, M_{16}	14.12 μm / 5 μm	1	4
M_9, M_{18}	8 μm / 5 μm	1	2
M_8, M_{15}	14.12 μm / 5 μm	1	2
M_{10}, M_{17}	8 μm / 5 μm	1	1
M_{13}, M_{14}	0.5 μm / 0.92 μm	1	2
M_{12}	2.4 μm/ 0.5 μm	6	1

4.3.1. Current Reference Circuit

Current reference circuits are the essential building blocks for data converters, phase-locked loops, operational amplifiers etc. There are critical performance criteria for analog building blocks such as a wide range of temperature coverage, and robustness with respect to process and supply variations. Two current sources can be combined together such that one of them is proportional to temperature and the other is inversely proportional to temperature, and that enables the generation of stable currents across a wide range of temperatures with the minimization of the temperature coefficient [58,59].

The implementation of current reference circuit consists of 5 parts which are bias voltage generation, a start-up circuit, PTAT and CTAT current generators and a summing circuit. The difference between the base-emitter voltage of two BJTs is proportional to temperature and the PTAT current is generated using this principle. The CTAT current generation is accomplished by exploiting the threshold voltage difference of two NMOS transistors with different oxide thicknesses. The schematic diagram of the current reference circuit is shown in Figure 4.24 [11].

4.3.1.1. CTAT Current Generation. The threshold voltage of MN1 is higher than that of MN2 in Figure 4.24. The overdrive voltages of these two transistors are given by

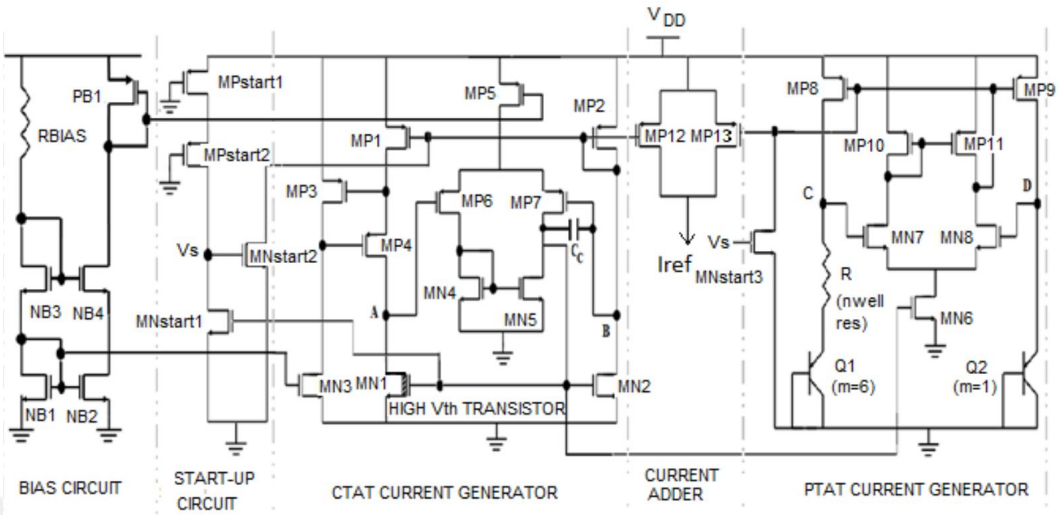

Figure 4.24. Schematic diagram of the current reference circuit [11].

Equations (4.10) and (4.11).

$$V_{GS} - V_{th1} = \sqrt{\frac{2I_{D1}}{k_{nT}S_1}} \tag{4.10}$$

$$V_{GS} - V_{th2} = \sqrt{\frac{2I_{D2}}{k_n S_2}} \tag{4.11}$$

V_{th1} and V_{th2} are the threshold voltages of MN1 and MN2 respectively. S_1 and S_2 are W/L ratios of these NMOS devices. k_{nT} and k_n are the conductivity parameters. By combining (4.10) and (4.11), V_{GS} can be obtained as:

$$V_{GS} = \frac{V_{th2}\sqrt{k_n} - V_{th1}\sqrt{Ak_{nT}}}{\sqrt{k_n} - \sqrt{Ak_{nT}}} \tag{4.12}$$

where $A = S_1/S_2$. Using (4.12), the drain current of MN2 can be expressed as:

$$I_{D2} = \frac{1}{2}k_n S_2 A k_{nT}\frac{(V_{th2} - V_{th1})^2}{(\sqrt{k_n} - \sqrt{Ak_{nT}})^2} \tag{4.13}$$

Equations (4.14)—(4.18) give the temperature dependence of V_{th}, Φ_F, V_T, n_i, and μ_n.

$$V_{th} = \Phi_{MS} + 2\Phi_F + \frac{\sqrt{4q\epsilon_{si}\Phi_F N_a}}{C_{ox}} \tag{4.14}$$

$$\Phi_F = V_T \ln\left(\frac{N_a}{n_i}\right) \tag{4.15}$$

$$V_T = \frac{kT}{q} \tag{4.16}$$

$$n_i = k_{si} T^{3/2} e^{-\frac{E_g}{2kT}} \tag{4.17}$$

$$\mu_n = \mu_0 T^{-3/2} \tag{4.18}$$

Here, Φ_F is the fermi potential, n_i is intrinsic carrier concentration, ϵ_{si} is permittivity of silicon, N_a is the doping concentration of p-substrate, Φ_{MS} is the difference in work functions between poly-silicon gate and silicon substrate, C_{ox} is the oxide capacitance, k is the Boltzmann constant, V_T is the thermal voltage, E_g is the silicon band-gap energy and K_{si} is the temperature coefficient of the intrinsic carrier concentration of silicon [11]. On substituting (4.14)—(4.18) into (4.13), one obtains:

$$I_{D2} = Z\mu_0 T^{-3/2}\left[\frac{kT}{q}\left(\ln N_a - \ln k_{si} - \ln T^{3/2} + \frac{E_g}{2kT}\right)\right] \tag{4.19}$$

where all the constants have been lumped into z as:

$$z = \frac{2AS_2 q\epsilon_{si} N_a (C_{ox1} - C_{ox2})^2}{C_{ox1}C_{ox2}(\sqrt{C_{ox2}} - \sqrt{AC_{ox1}})^2} \tag{4.20}$$

The derivative of I_{D2} with respect to temperature reveals the temperature dependence of current as:

$$\frac{\partial I_{D2}}{\partial T} = -\frac{Z\mu_n}{2}\left(\frac{k}{q}\ln\frac{N_a}{n_i} + 3\frac{k}{q} + \frac{E_g}{qT}\right) \tag{4.21}$$

The minus sign in (4.21) shows that the current is inversely proportional to temperature because it has a negative temperature coefficient.

4.3.1.2. PTAT Current Generation. The size of Q1 is taken as larger than Q2 which provides greater current carrying capacity to Q1. Applying KVL in the loop constructed by resistors and BJTs in Figure 4.24, one obtains:

$$V_{BE2} = V_{BE1} - IR. \tag{4.22}$$

If Q1 is considered to be m times higher than Q2, then (4.22) can be written as:

$$I_{\text{PTAT}} = \frac{V_T \ln m}{R} \tag{4.23}$$

The derivative of I_{PTAT} with respect to temperature indicates that the current has a positive temperature coefficient, and hence it is proportional to temperature.

$$\frac{\partial I_{\text{PTAT}}}{\partial T} = \frac{k}{qR} \ln m \tag{4.24}$$

As a result, summing I_{PTAT} and I_{CTAT} with an appropriate temperature coefficient enables the generation of a temperature independent current reference [11].

Results of the current reference circuit simulation across temperatures between -25°C and 120°C are shown in Figure 4.25.

4.4. Readout Circuit

The differential output currents of a Hall sensor are delivered to a readout circuit which is responsible for conversion of the current into voltage by providing low offset and noise. The differential output currents of a Hall sensor, I_{HN} and I_{HP}, are converted into voltages by integrating over an integration capacitor, C_{int}, for a specified time-slot. A block diagram of the readout circuit is illustrated in Figure 4.26.

Inititially, the integration capacitors are reset by turning on the switch around the feedback. The Hall currents are disconnected from the readout circuitry and flow to the

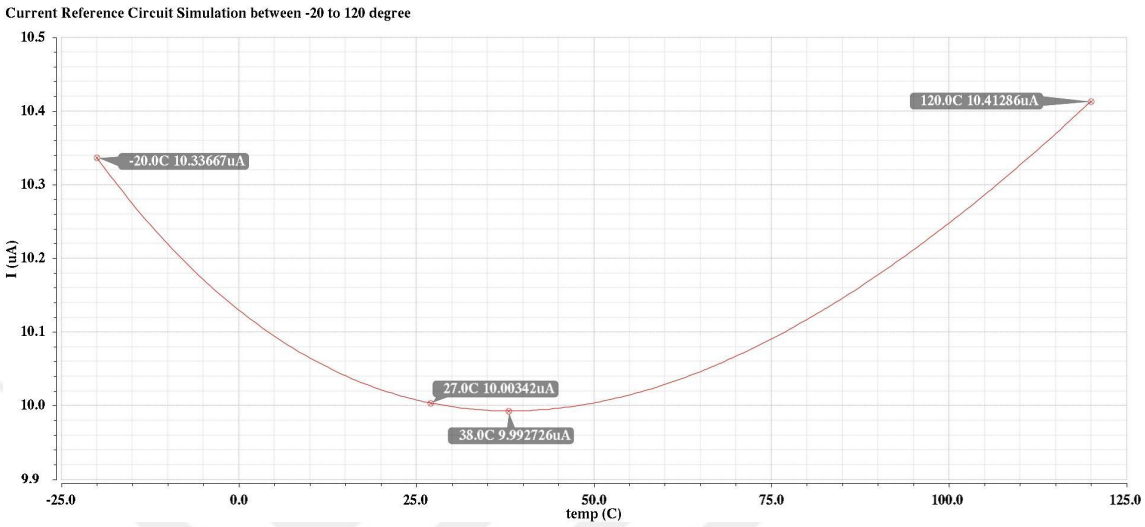

Figure 4.25. Current reference circuit simulation across temperatures between -25°C and 120°C.

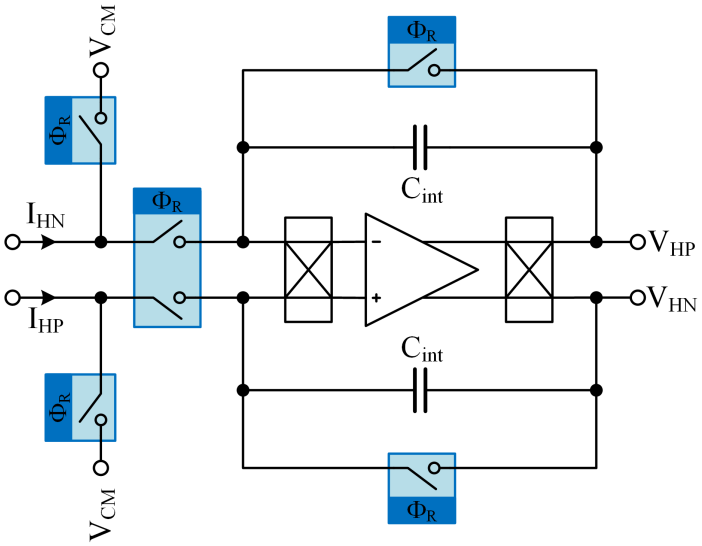

Figure 4.26. Block diagram of the current-to-voltage converter.

common-mode voltage during the reset phase. On the other hand, the integration of Hall currents starts with closing the measure switch and proceeds with integer numbers of current spinning cycles. Finally, the currents I_{HN} and I_{HP} are separated from the circuit after the integration duration. After this period, the output voltages V_{HN} and V_{HP} are ready for further amplification and filtering.

The crucial block in the readout is the fully differential amplifier. The amplifier should be designed as having low offset and noise, hence chopping switches are utilized to eliminate input offset and low-frequency noise. The accuracy of the measurement is also influenced by finite gain A_0 of the amplifier due to the voltage at the input terminals $(-V_{out}/A_0)$ which slightly disrupts the biasing of the Hall sensor. The chopping block is a passive mixer which consists of 4 identical switches as a complementary CMOS pair. It has two input and two output leads. It may also be designed with only one output to be used in single ended amplifiers. The polarity of the input signal is alternated each half cycle of the chopper clock. The input signals pass straight through the outputs in the first phase, and switch the outputs in the other. Non-overlapping clocks with short periods are utilized to prevent noise leakage during switching. The schematic of the chopper block used in the amplifier is shown in Figure 4.27.

4.4.1. Chopper Amplifier Design

Fully differential amplifiers have various advantages compared to single-ended amplifiers. For instance, in fully differential amplifiers, even order harmonic distortion components are canceled, leading to less distortion and better linearity. Differential amplifiers also have less output noise since they reflect the common-mode signal and the coupled noise is identical for both input terminals and is cancelled at the output. Moreover, the output amplitude of single-ended amplifier's output can be doubled when it is taken as differential, thus a 6-dB greater gain is achieved. Also, differential amplifiers have higher output voltage swing and this results in better SNR. There are three types of well known operational transconductance amplifier (OTA) topologies: two-stage OTAs, telescopic OTAs, folded-cascode OTAs. Each has its own advantages and disadvantages. These topologies are compared in terms of gain, speed, power and

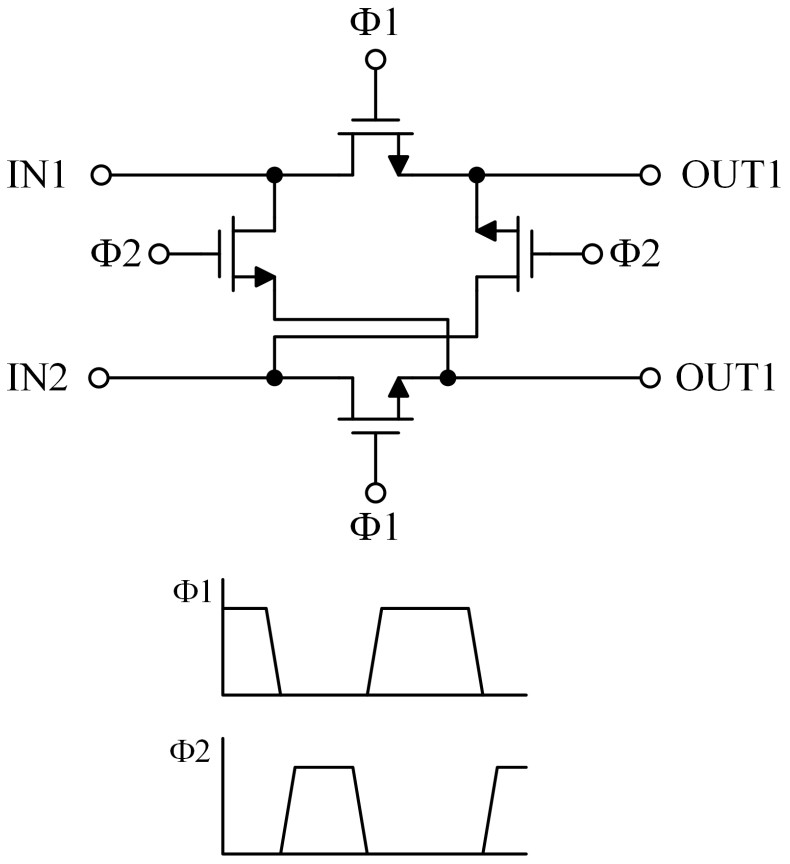

Figure 4.27. Schematic of the chopping block.

output swing in Table 4.2.

Table 4.2. Comparison of different OTA topologies.

Topology	**Gain**	**Power Dissipation**	**Speed**	**Output Swing**	**Noise**
Two-Stage	High	Medium	Low	Highest	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Telescopic	Medium	Low	Highest	Medium	Low

The gain parameter is one of the key factors in selecting the appropriate OTA for the readout circuitry, as opposed to power and speed which are not as significant. Although a two-stage OTA provides higher gain and better noise response, it requires a compensation capacitor between the first and second stages which increases its area usage — an important factor in the design of micro-arrays. Input and ouput terminals of the OTA in the readout circuit are shorted during the reset phase to discharge the capacitor. Therefore, telescopic OTAs are not suitable for this since it is more difficult to short their input and output terminals due to their limited output swing. As a result, a folded-cascode topology is more advantageous than others for this application because it provides higher bandwidth and greater output swing. Thus, it is possible to short its input and output terminals. Although folded cascode amplifiers provide a medium range gain, it can be increased further by utilizing gain boosting techniques.

4.4.1.1. Gain Boosting Techniques. There are two ideal methods to increase the gain of an amplifier which are known as normal cascode and regulated cascode circuits [57].

(a) *Normal cascode circuit:* A CG stage which is capable of current buffering is connected at the output of a CS amplifier as shown in Figure 4.28. The gain of an amplifier is calculated as the product of the transconductance and the output impedance. A normal cascode circuit increases the gain of an amplifier by providing higher output impedance. Additionally, normal cascode circuits improve the frequency response of an amplifier since the effective gate-drain capacitance of a CS transistor is reduced by the gain of the CG transistor. The output impedance R_o of a cascode circuit can be

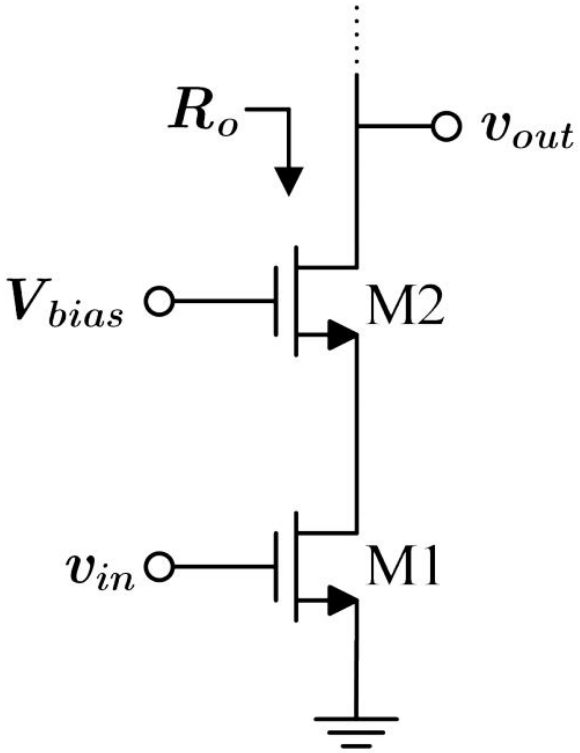

Figure 4.28. Simple cascode circuit.

calculated as:

$$R_o = r_{o1} + (1 + g_{m2}r_{o1})r_{o2} \approx g_{m2}r_{o1}r_{o2} \tag{4.25}$$

which is the same as the output impedance of a normal CS amplifier multiplied by $g_{m2}r_{o2}$ [57]. In spite of these advantages, the output voltage swing is reduced by the over-drive voltage of the CG transistor.

(b) *Regulated Cascode Circuit:* The regulated (gain-boosted) cascode circuit enables raising the output impedance without sacrificing output voltage swing. The gain-boosted cascode circuit is shown in Figure 4.29.

The output impedance of a gain-boosted cascode circuit is given by:

$$R_o = r_{o1} + (1 + g_{m2}Ar_{o1})r_{o2} \approx g_{m2}Ar_{o1}r_{o2} \tag{4.26}$$

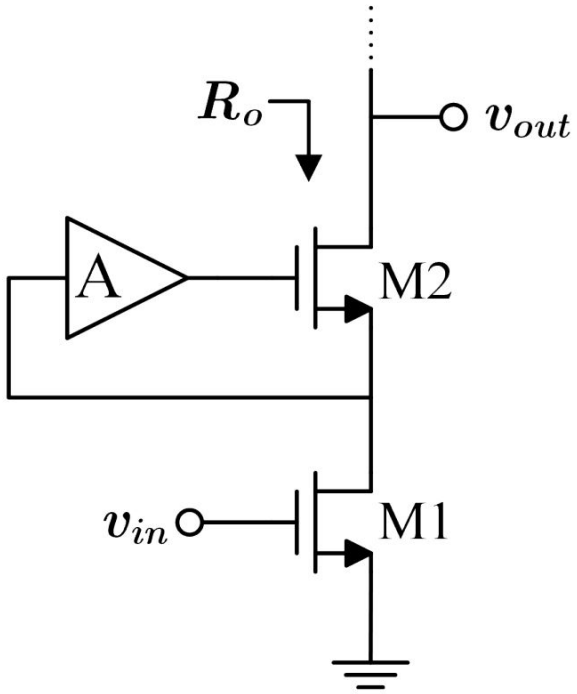

Figure 4.29. Regulated (gain-boosted) cascode circuit.

The output impedance of a gain-boosted circuit is increased by the gain of the feedback amplifier, A, which makes possible to increase the gain of the amplifier further by adjusting the value of A without cascoding another transistor. The feedback amplifier controls the drain voltage of the CS transistor by changing the gate voltage of M2, hence variations on the drain voltage of M1 are reduced [57].

4.4.1.2. Fully Differential Folded Cascode Amplifier. The issue of shorting input and output terminals of telescopic amplifiers is overcome by using folded cascode amplifiers. The structure of regular NMOS differential input folded cascode amplifier is shown in Figure 4.30. Although a folded cascode amplifier is primarily a single stage amplifier, it provides a reasonable amount of gain since the output impedance is quite high due to cascode transistors M5 – M8. Moreover, folded cascode amplifiers are naturally stable because they only have a single pole, hence compensation is not required and the value of the load capacitance does not depend on compensation capacitance. Furthermore, having non-dominant poles closer to the unity gain frequency makes folded cascode amplifiers faster. In addition, folded cascode amplifiers have better PSRR [57].

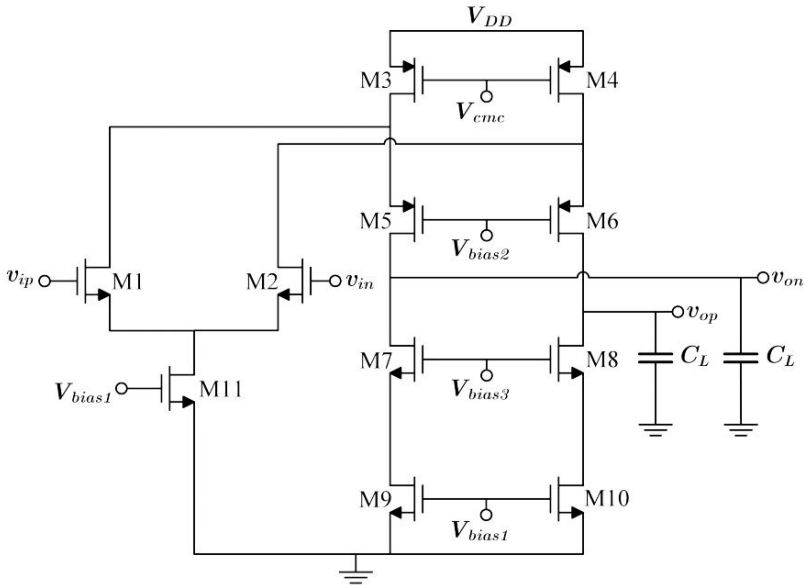

Figure 4.30. Fully differential folded-cascode amplifier.

Relationships between gain, dominant pole f_{p1}, output impedance R_o, input common-mode range (ICMR) and output voltage swing range (OSVR) are given in (4.27)—(4.31).

$$\text{Gain} = g_{m1}\{[g_{m5}r_{o5}(r_{o1}||r_{o3})]||(g_{m7}r_{o7}r_{o9})\} \tag{4.27}$$

$$V_{OV11} + V_{TH1} + V_{OV1} < ICMR < V_{DD} - V_{OV3} + V_{TH1} \tag{4.28}$$

$$V_{OV9} + V_{OV7} < OVSR < V_{DD} - V_{OV3} + V_{OV5} \tag{4.29}$$

$$f_{p1} = \frac{1}{2\pi C_L R_o} \tag{4.30}$$

$$R_o = [g_{m5}r_{o5}(r_{o1}||r_{o3})]||(g_{m7}r_{o7}r_{o9}) \tag{4.31}$$

Cascode devices contribute very little to the noise of the amplifier at low frequencies, therefore the noise of cascode devices is neglected and M1-M4 and M9-M10 in Figure 4.30 are the important noise sources. Output thermal noise of these transistors

can be found by using (4.32)—(4.34).

$$\overline{V_{n,out}^2}\Big|_{M3,4} = 2\left(4kT\frac{2}{3g_{m3,4}}g_{m3,4}^2R_{out}^2\right) \tag{4.32}$$

$$\overline{V_{n,out}^2}\Big|_{M9,10} = 2\left(4kT\frac{2}{3g_{m9,10}}g_{m9,10}^2R_{out}^2\right) \tag{4.33}$$

$$\overline{V_{n,out}^2}\Big|_{M1,2} = 2\left(4kT\frac{2}{3g_{m1,2}}g_{m1,2}^2R_{out}^2\right) \tag{4.34}$$

The input-referred noise is given by:

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out,tot}^2}}{A_v^2} = 8kT\left(\frac{2}{3g_{m1,2}} + \frac{2}{3}\frac{g_{m3,4}}{g_{m1,2}^2} + \frac{2}{3}\frac{g_{m9,10}}{g_{m1,2}^2}\right) \tag{4.35}$$

Also, the flicker noise can be calculated as:

$$\overline{V_{n,out}^2}\Big|_{M3,4} = 2\left(\frac{K_P}{C_{ox}(WL)_{3,4}}\frac{1}{f}g_{m3,4}^2R_{out}^2\right) \tag{4.36}$$

$$\overline{V_{n,out}^2}\Big|_{M9,10} = 2\left(\frac{K_N}{C_{ox}(WL)_{9,10}}\frac{1}{f}g_{m9,10}^2R_{out}^2\right) \tag{4.37}$$

$$\overline{V_{n,out}^2}\Big|_{M1,2} = 2\left(\frac{K_N}{C_{ox}(WL)_{1,2}}\frac{1}{f}g_{m1,2}^2R_{out}^2\right) \tag{4.38}$$

$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out,tot}^2}}{A_v^2} = \frac{2K_N}{C_{ox}f}\left(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{9,10}}\frac{g_{m9,10}^2}{g_{m1,2}^2}\right) + \frac{2K_P}{C_{ox}f}\frac{1}{(WL)_{3,4}}\frac{g_{m3,4}^2}{g_{m1,2}^2} \tag{4.39}$$

In order to decrease the flicker noise, W_1, L_1, and L_9 can be increased. Choosing a PMOS input pair might provide lower flicker noise, but PMOS input pair provides lower gain compared to an NMOS input pair folded cascode amplifier. Also, using NMOS input pair provides lower thermal noise. Moreover, increasing g_{m1} by increasing current consumption or lowering the overdrive voltage is also an effective method for achieving lower thermal noise. In addition, g_{m3} and g_{m9} can also be reduced for a lower thermal noise.

(a) *Common Mode Feedback Circuit:* Fully differential OTAs are usually used with feedback and the differential signal voltages are determined by feedback without affecting the common mode voltage. Therefore, an extra circuit is needed to indicate the output common-mode voltage and it should also be controlled to keep it at a certain value which is generally taken as half of the supply voltage. A schematic diagram of the common-mode feedback is demonstrated in Figure 4.31.

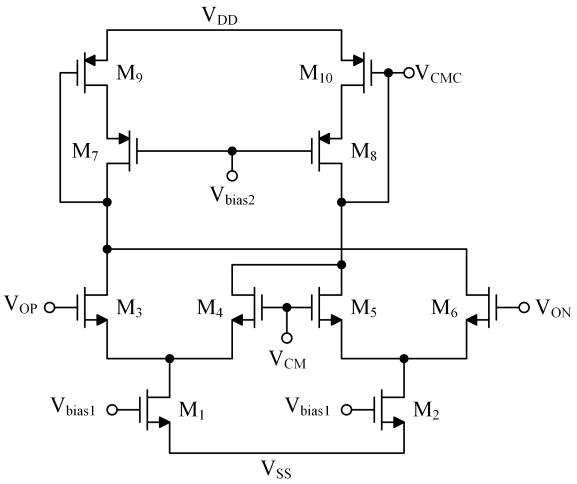

Figure 4.31. Common-mode feedback circuit for fully differential gain-boosted chopper amplifier.

The schematic of the gain-boosted folded cascode chopper amplifier is shown in Figure 4.32 and the design parameters are listed in Table 4.3. The open-loop AC response of the chopper amplifier is given in Figure 4.33. A gain of 102 dB, a 3-dB cut-off frequency of 15.8 kHz, a unity gain frequency of 703 MHz and a phase margin (PM) of 65° is achieved. Also, the transient response in unity-gain configuration is presented in Figure 4.34.

The input-referred noise response of the chopper amplifier without chopping and with chopping are given in Figures 4.35 and 4.36, respectively. Periodic noise simulation has been used to get more accurate results. Around 1 kHz, a noise of approximately 33 nV/$\sqrt{Hz}$ is obtained without using chopping, and this value decreases to 8.3 nV/$\sqrt{Hz}$ with chopping.

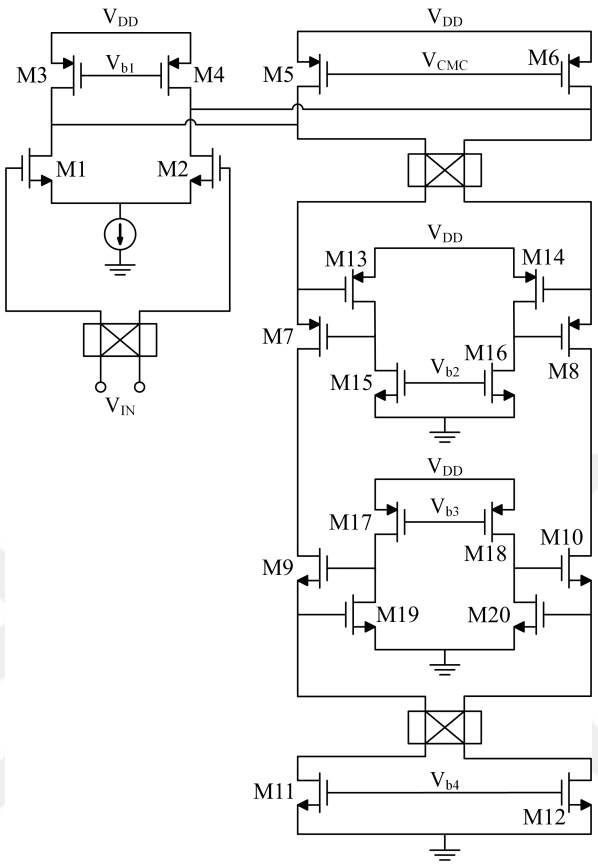

Figure 4.32. Fully differential gain-boosted chopper amplifier.

Table 4.3. Design parameters for gain-boosted folded cascode amplifier.

Parameter	**Value**	**Finger**	**Multiplier**
M1-M2	2.16 μm / 0.54 μm	4	84
M3-M4	1.76 μm / 0.85 μm	2	64
M5-M6	1.96 μm / 0.96 μm	2	8
M7-M8	0.96 μm / 0.24 μm	4	198
M9-M10	0.64 μm / 0.32 μm	2	244
M11-M12	3.06 μm / 3.06 μm	1	20
M13-M14	2.2 μm / 1.2 μm	2	24
M15-M16	1.08 μm / 0.72 μm	1	6
M17-M18	2.88 μm / 1.44 μm	2	32
M19-M20	0.6 μm / 0.64 μm	1	12

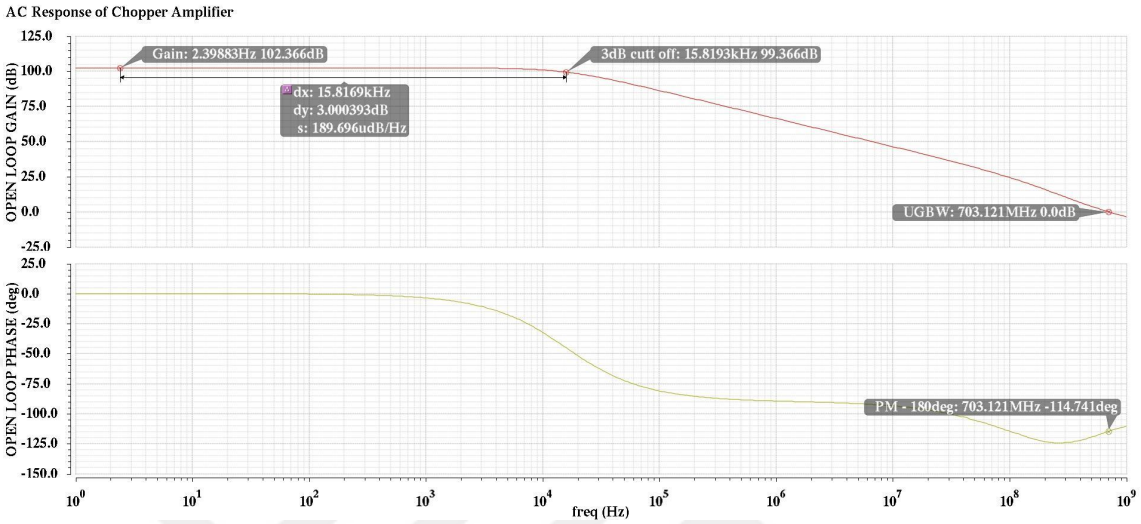

Figure 4.33. Open-loop AC response of chopper amplifier.

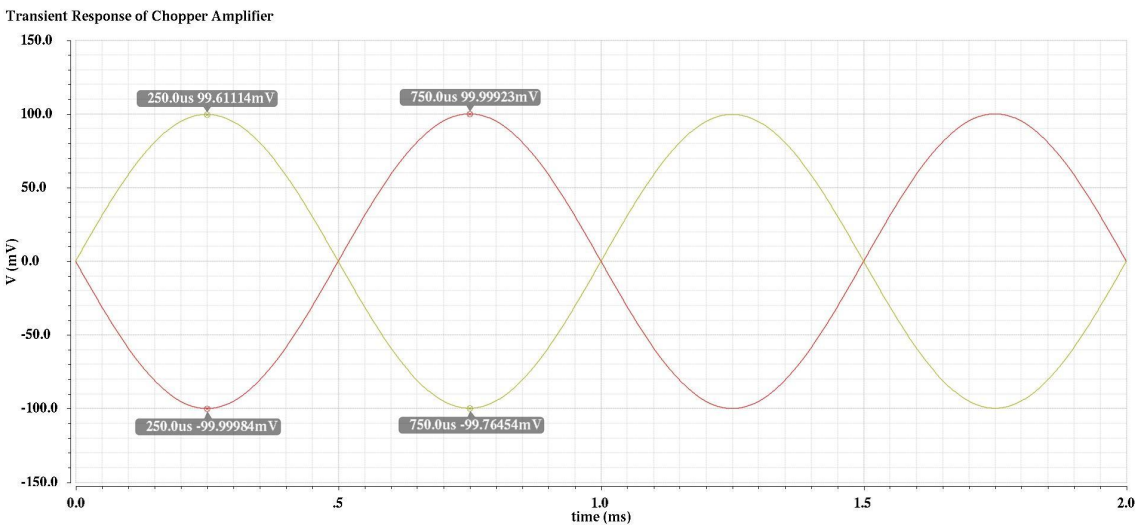

Figure 4.34. Transient response of chopper amplifier in unity-gain configuration.

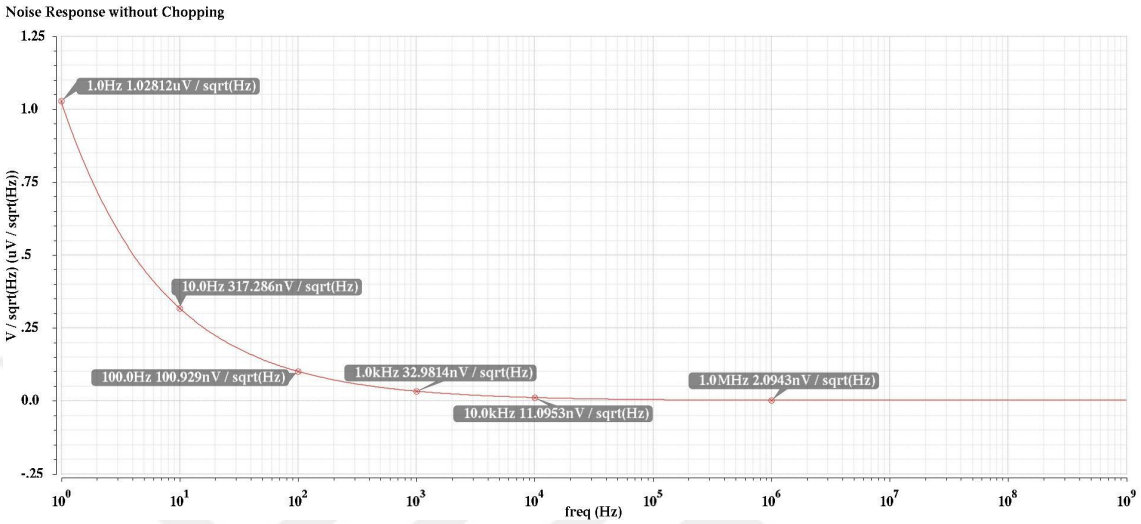

Figure 4.35. Input-referred noise response of chopper amplifier without chopping.

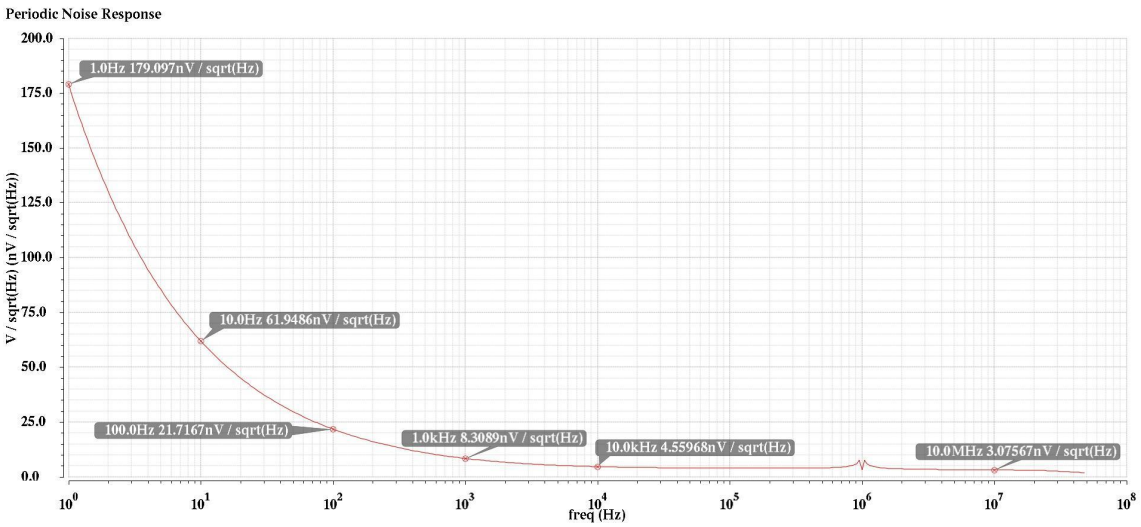

Figure 4.36. Input-referred noise response of chopper amplifier with chopping.

4.5. Switched-Capacitor Low-Pass Filter Design

The chopping technique modulates the flicker noise of the amplifier to odd multiples of the chopping frequency. These high-frequency unwanted noise components have to be removed from the desired signal by means of a low-pass filter. The output of the readout circuit is also required to be amplified further to fit the full-scale voltage of the ADC. Higher predictability, lower costs, and easier design makes switched capacitor circuits more popular for designing filters. Hence the required low-pass filter is designed by using switched capacitors in order to achieve a more precise gain to fit the full-scale voltage range of the ADC [60].

Table 4.4. Filter design specifications.

Parameter	**Specified Value**
Sampling Frequency	25 MHz
DC Gain	26.021 dB
Passband Frequency	1 MHz
Ripple in Passband	<1 dB
Stopband Frequency	2 MHz
Gain in Stopband	<- 70 dB

The filter orders for different filter types are derived using a Matlab filter design tool according to the specifications in Table 4.4. Filter order requirements are presented in Table 4.5 for different filter types.

Table 4.5. Filter order requirements.

Filter Type	**Minumum Order**
Butterworth	13
Chebyshev Type I	8
Chebyshev Type II	8
Elliptic	5

An elliptic filter is designed in order to minimize the area usage. A cascade of biquads and a linear filter would simplify the design and make it easier to find and correct errors. The transfer functions of linear, High-Q and Low-Q sections are given

in (4.40)—(4.42).

$$H(Z_L) = \frac{z+1}{z-0.9234} \tag{4.40}$$

$$H(Z_{LQ}) = \frac{z^2+1.4052z+1}{z^2-1.8604z+0.8886};\ (Q=1.47) \tag{4.41}$$

$$H(Z_{HQ}) = \frac{z^2-1.7315z+1}{z^2-1.9003z+0.9615};\ (Q=6.38) \tag{4.42}$$

The order of cascading for filter stages is shown in Figure 4.37. The High-Q stage is placed in the middle of the cascade for stability purposes. Since the linear stages exhibit better low-pass behaviour in comparison to the low-Q stage, linear section is kept at the beginning of the cascade. The schematic diagram of each stage is shown in Figures 4.38, 4.39 and 4.40 in line with the cascading order. In addition, values of capacitors used in the filter design are listed in Table 4.6.



Figure 4.37. Order of filter stages.

Table 4.6. Filter capacitor values after scaling.

Linear	**Value (pF)**	**Low-Q**	**Value (pF)**	**High-Q**	**Value (pF)**
C_A	3.01191	C_1	3.01191	C_1	3.01191
C_1	0.788509	C_2	2.732057	C_2	0.789898
C_2	1.577018	C_3	0.53721	C_3	0
C_3	0.25	C_4	3.01191	C_4	0.745305
		C_5	0	C_5	0.468589
		C_6	0.819314	C_6	3.01191
		C_7	0.53721	C_7	0.728076
		C_8	0.377434	C_8	0.745305

The OTAs in Figures 4.39—4.40 are designed to have identical specifications and their AC response is shown in Figure 4.41. As seen in Figure 4.41, the open-loop DC

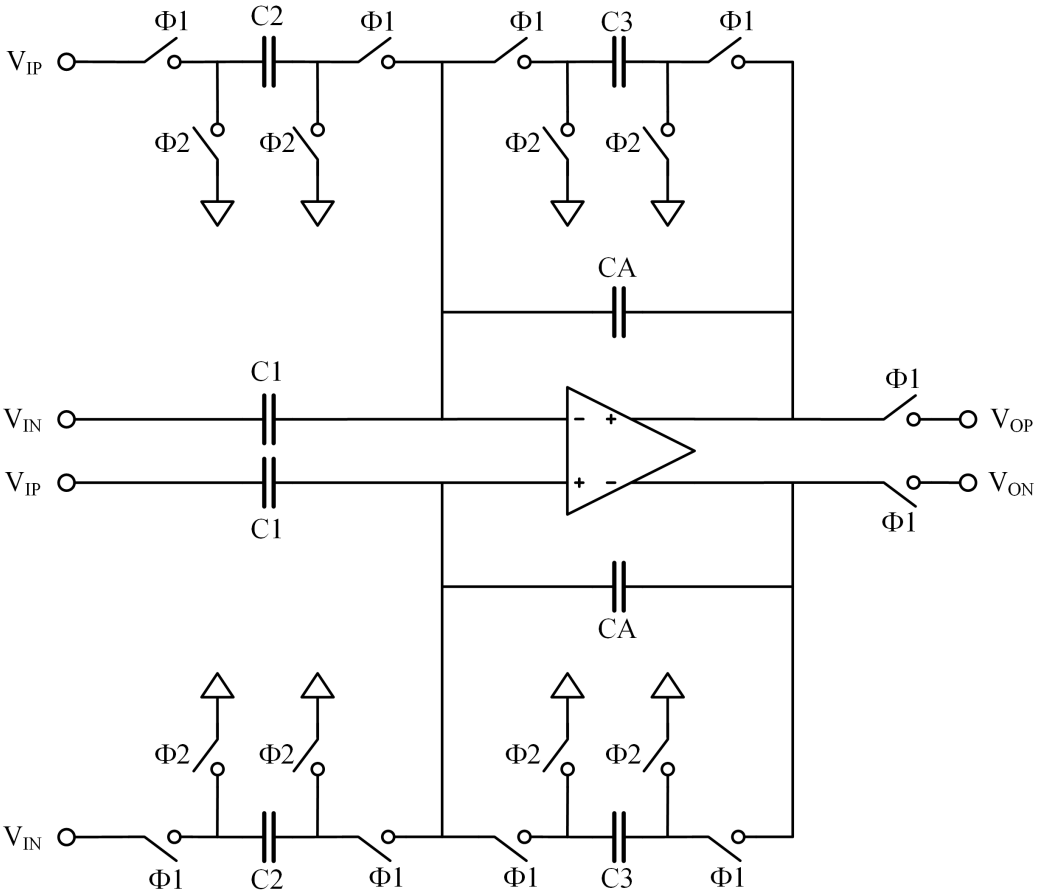

Figure 4.38. Linear section.

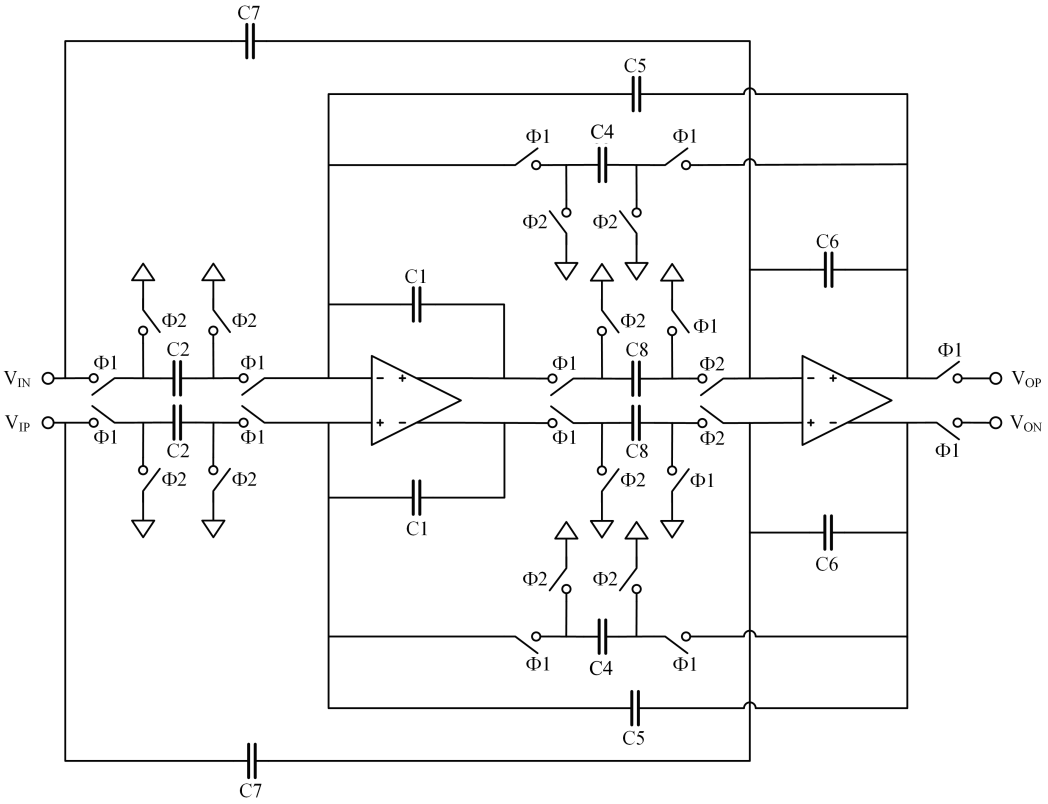

Figure 4.39. High-Q biquad section.

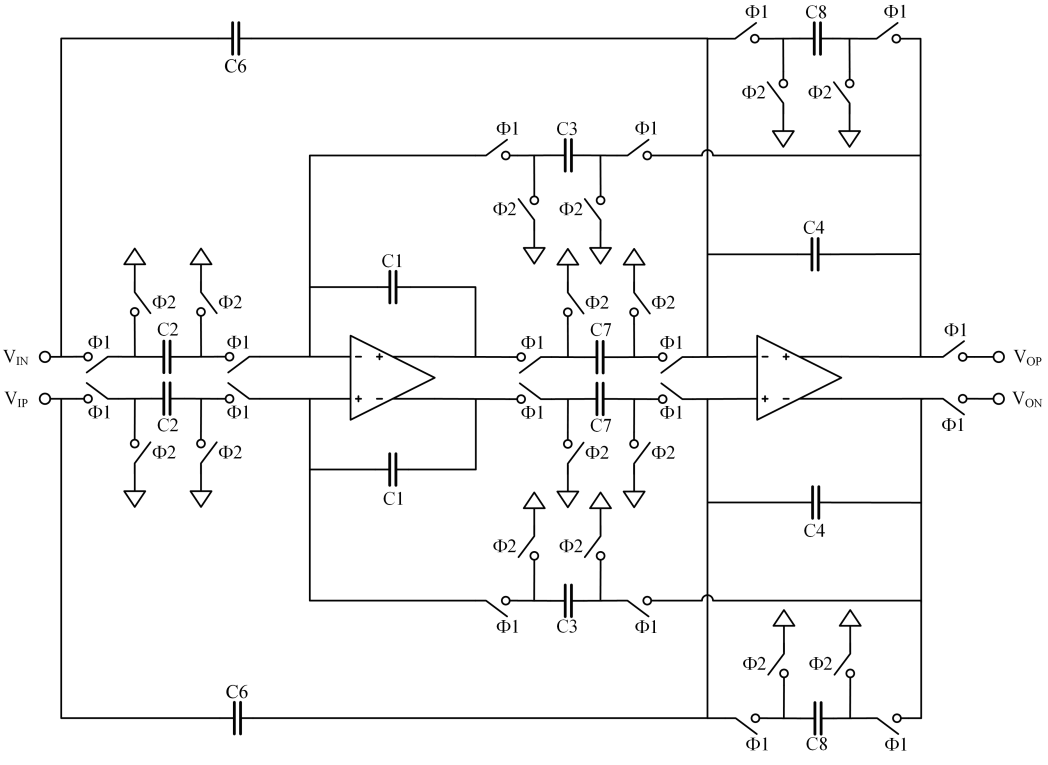

Figure 4.40. Low-Q biquad section.

gain is 99 dB, the 3-dB cut-off frequency is about 56 kHz and a unity-gain frequency of almost 1.5 GHz is achieved. The particularly high gain of 99 dB was achieved using gain-boosting, and a portion of the schematic that helped boost the gain is given in Figure 4.42.

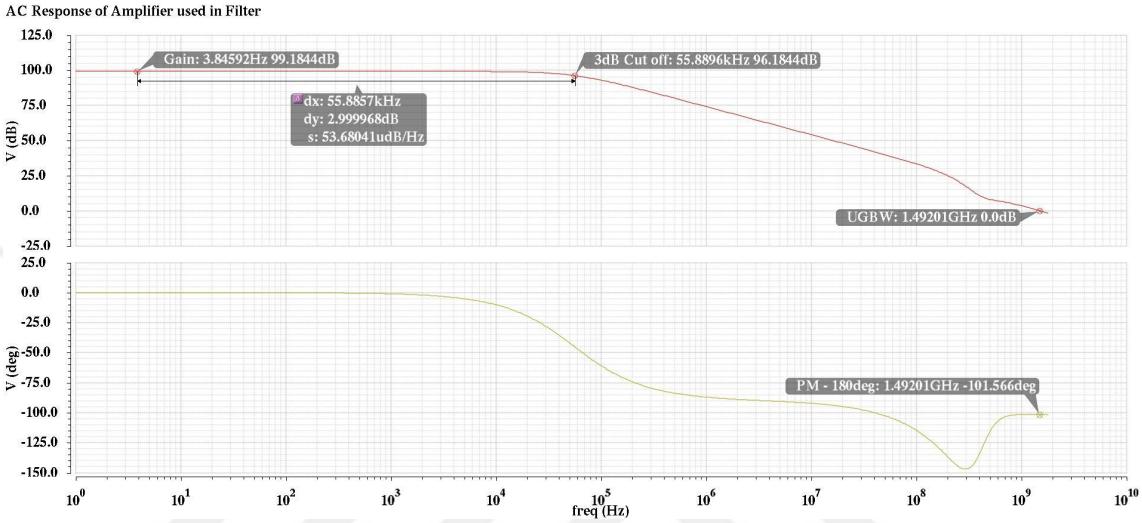

Figure 4.41. Open-loop AC response of OTA used in 5th order switched capacitor elliptic filter.

The magnitude response of the designed filter is presented in Figure 4.43. Although the actual specifications of the filter do not exactly match the desired values given in Table 4.4, they are sufficient for the intended function of the filter.

4.6. Single Slope A/D Converter for Column Parallel Placement

The single-slope ADC includes a ramp generator, a counter, a comparator, and memory. While each column uses an individual copy of the comparator and memory block, a single ramp generator and counter are utilized for the entire sensor microarray. Subsequent sections explain each of these blocks.

4.6.1. Ramp Generator

The design of a ramp generator is crucial since it directly influences the quality of an ADC. The ramp generator output should be monotonous and linear in order to

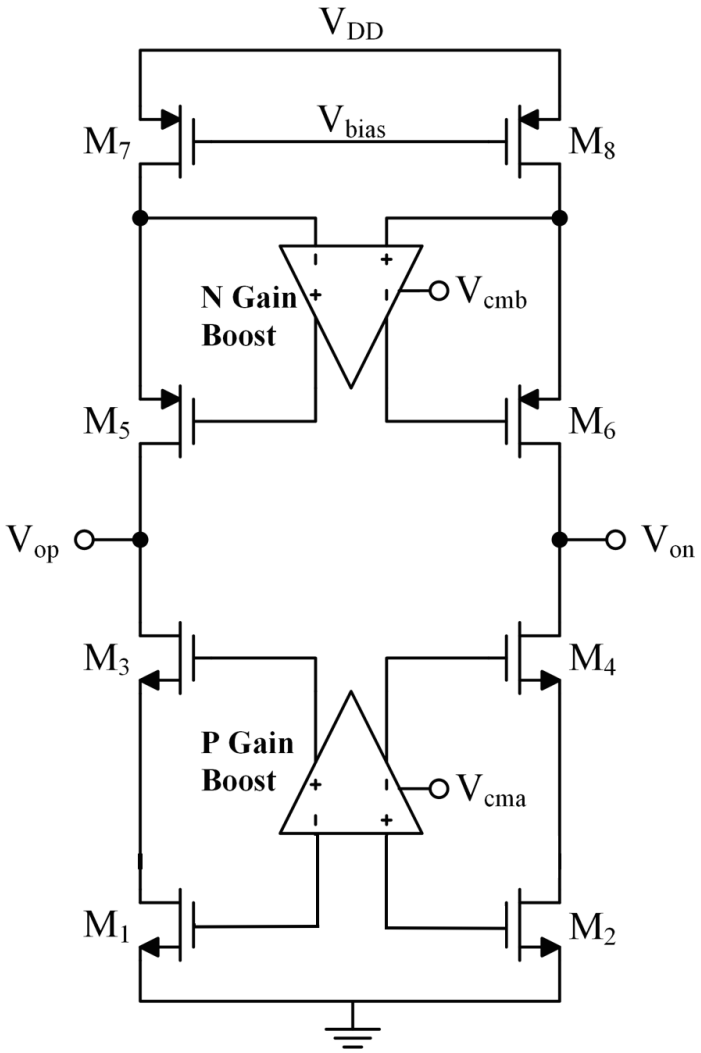

Figure 4.42. Gain-boosting circuit used in OTAs in filters.

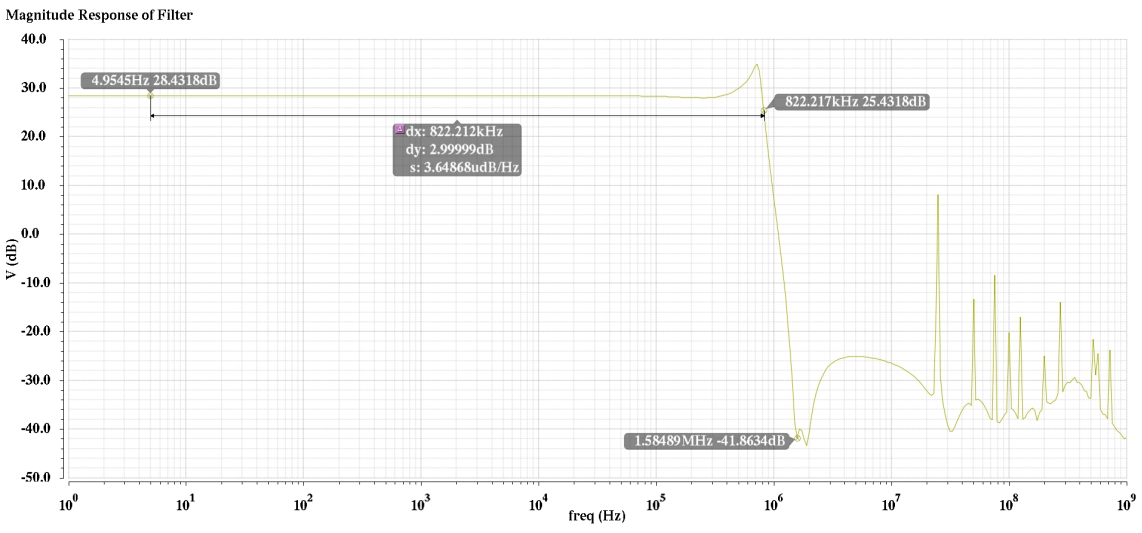

Figure 4.43. Magnitude response of 5th order switched capacitor elliptic filter.

encompass the entire ADC range. There are two ways to design a ramp generator: integrator based design and DAC based design.

4.6.1.1. Integrator Based Ramp Generator. Integrators have found widespread usage in generating triangular and sawtooth waves. Since the current supplied into the circuit is constant, the integrator output rises linearly with constant slope. Capacitance and current values affect the slope of the ramp as given in (4.43). Supplying more current and using large capacitances improves the noise performance of the integrator. An integrator based ramp generator is shown in Figure 4.44.

$$\frac{dV}{dt} = \frac{i}{c} \tag{4.43}$$

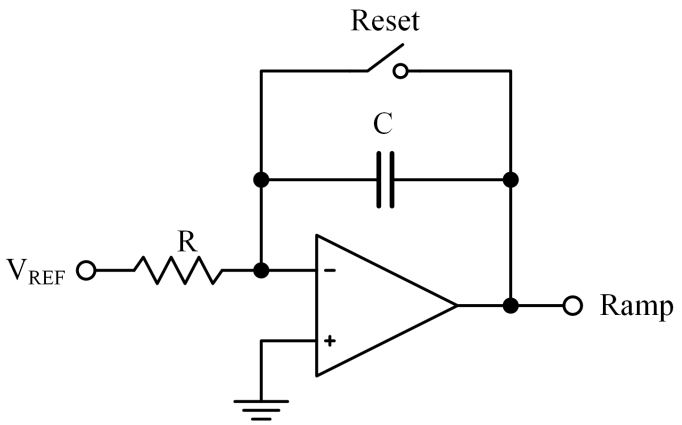

Figure 4.44. Integrator based ramp generator.

Mismatch variations between the resistor and the capacitor and the absence of any correlation between ramp generator and counter are the main drawbacks of an integrator based ramp generator. Also, an Op-amp with higher specifications than usual is required for an integrated based structure.

4.6.1.2. DAC Based Ramp Generator. In this structure, a correlation is established between ramp generator and counter. The counter is incremented at each clock pulse, and the generated digital value is converted to its analog counterpart by means of a DAC as shown in Figure 4.45.

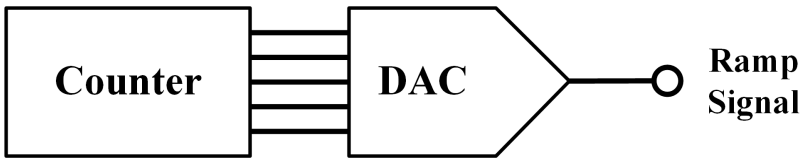

Figure 4.45. DAC based ramp generator.

There are capacitive, resistive and current-steering types of DACs. The desired resolution of the ADC designed in this project is 10 bits. Current-steering DACs are utilized in high-speed applications but their resolution is lower than 10 bits. Capacitive multiplying DACs (MDACs) can achieve 10 bits of resolution even though they require a relatively large layout area. The layout area can be reduced using an attenuation capacitance. The schematic of the designed capacitive MDAC with attenuation capacitance is shown in Figure 4.46.

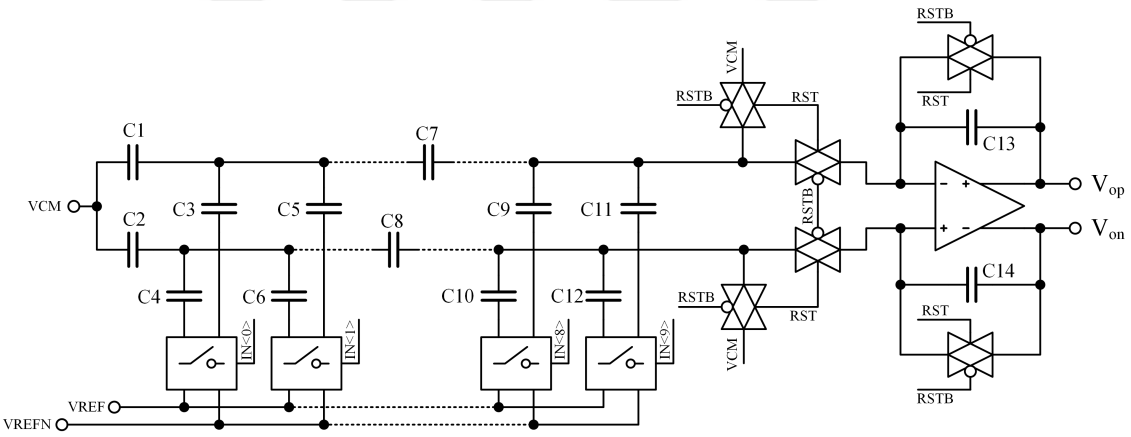

Figure 4.46. Capacitive MDAC with attenuation capacitance.

A unity capacitance of 155 fF is used in the MDAC design, and the attenuation capacitance C_A is calculated as 160 fF using (4.44) where C_U is the unity capacitance and n is the number of bits.

$$C_A = \frac{2^{n/2}}{2^{n/2}-1} C_U \tag{4.44}$$

The counter output is fed into the DAC in order to generate the ramp signal. Also, the digital output of the counter is stored in the memory circuit according to the

output of the comparator. A single counter circuit is allocated for all columns of ADC, thus the count data requires a strong buffer to drive a high load. Synchronous counter circuits with enable and reset inputs are designed. An implementation of the design for a 4-bit synchronous counter is shown in Figure 4.47.

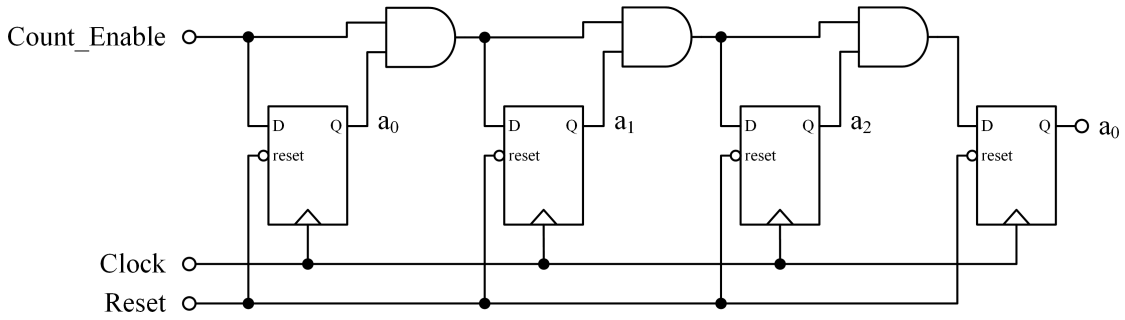

Figure 4.47. 4-bit synchronous counter implementation using DFFs.

The simulation results of the designed DAC based ramp generator are presented in Figure 4.48.

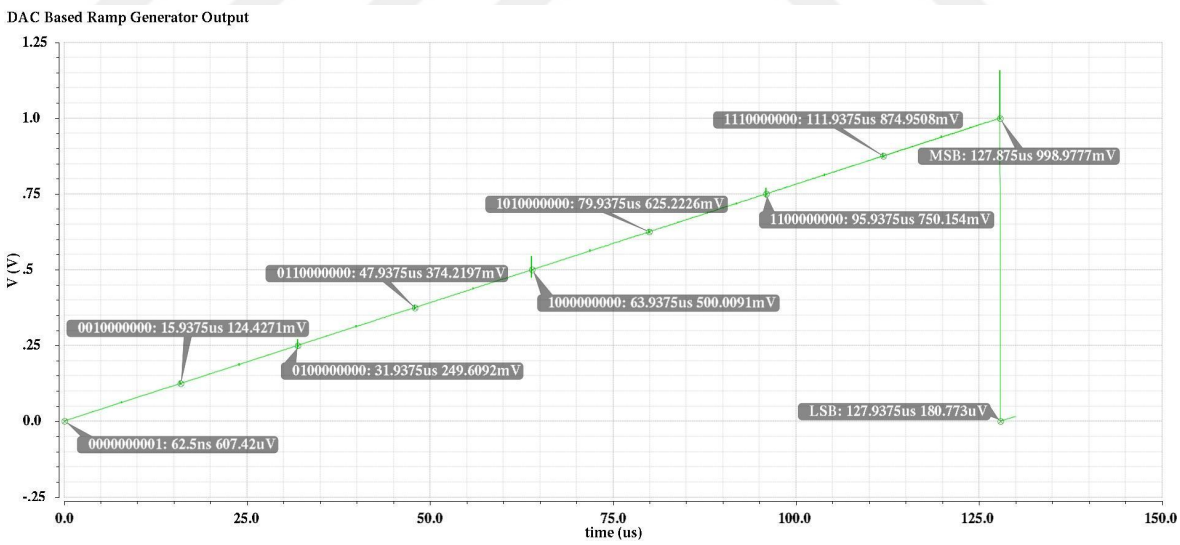

Figure 4.48. DAC based ramp generator output.

4.6.2. Comparator

The hall sensor output is fed through a switched capacitor low-pass filter and then compared with the output of the ramp generator using a comparator. The conversion in Single Slope ADC is done primarily by the comparator. Therefore, the performance of

ADC is mostly got affected by variations in comparator. Higher resolution requirement necessitates low noise and low offset of operation.

Dynamic latched comparators are widely used for modern high-speed and power-efficient applications. Dynamic latched comparators do not consume power when idle; power consumption only occurs during the rising and falling edges of the clock. They are implemented by utilizing a cross-coupled pair of inverters as shown in Figure 4.49.

Figure 4.50 shows the result of cascading a counter, a DAC, and a comparator. This arrangement allows us to quantize the range of magnetic fields and detect values between 0 mT and the maximum 20 mT. The example shown in Figure 4.50 is for detecting a field of 12 mT which corresponds to 600 mV. As seen in Figure 4.50, the counter counts up until it reaches 600 mV and then this digital count value is stored in memory.

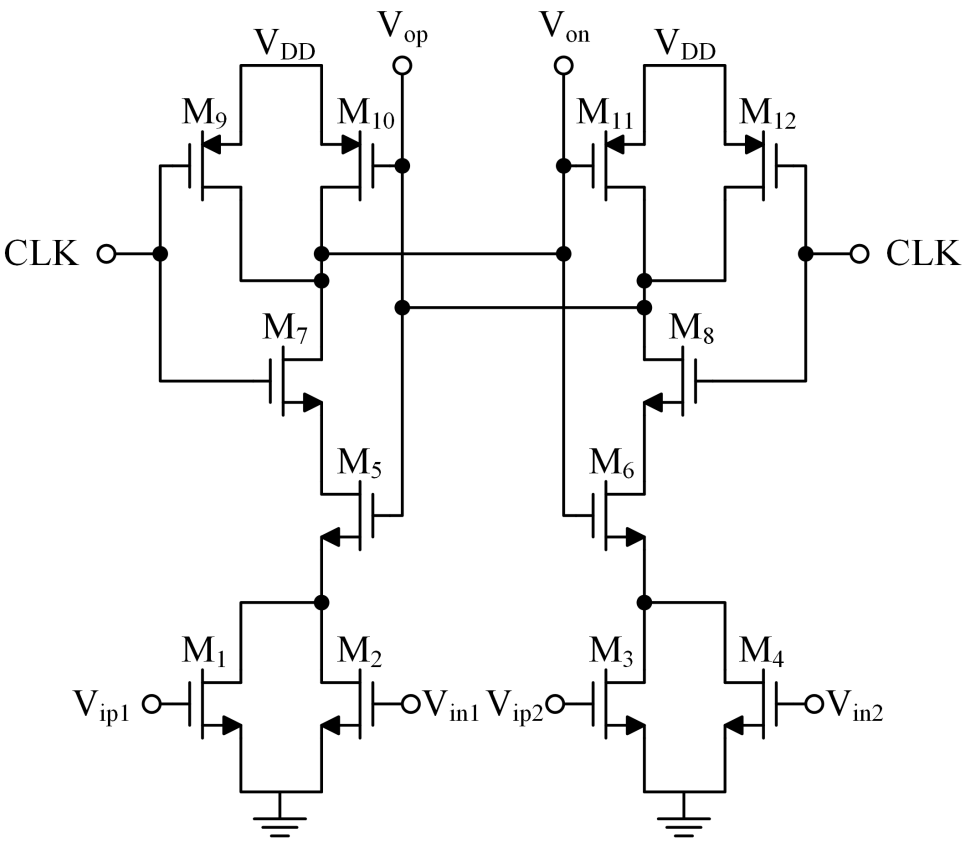

Figure 4.49. Dynamic latched comparator.

In Figure 4.49, the PMOS and NMOS transistors in the middle are controlled by the CLK signal. The PMOS transistors are on during the falling edge of the CLK so that both inverters produce an output of logical '1'. The PMOS transistors turn off while the NMOS transistors in the middle turn on during the rising edge of the CLK and this makes the NMOS transistors in the inverters begin to conduct current which were previously in the linear region due to their drain terminals being grounded. In accordance with the difference between input voltages, an imbalance occurs between the cross-coupled inverters. This imbalance enters into a positive feedback loop and keeps growing. Eventually, the output of one of the inverters becomes high while the other becomes low. These values is stored in the SR latch.

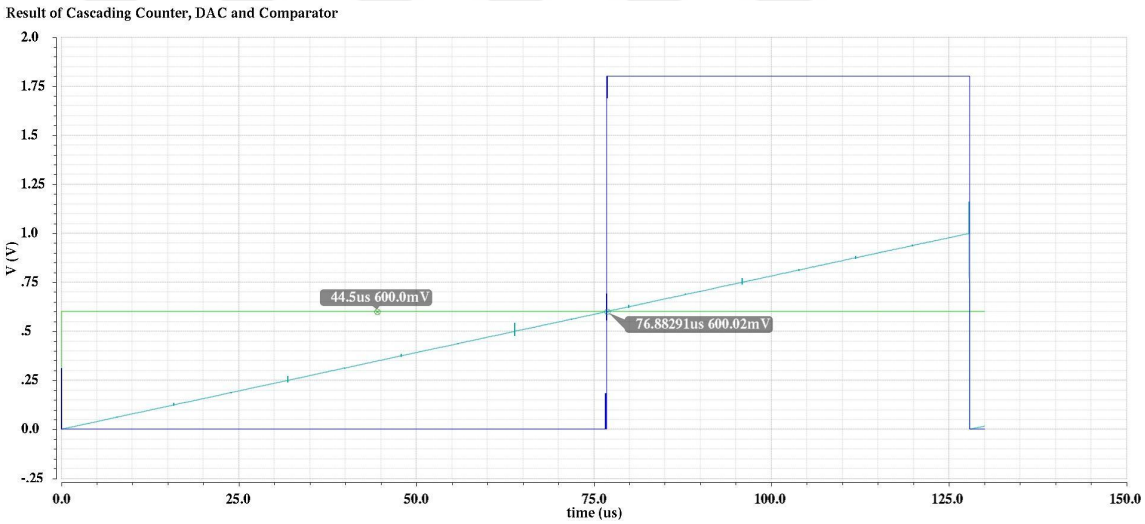

Figure 4.50. Result of cascading counter, DAC, and comparator.

4.6.3. Memory Circuit

Memory stores the digital count value right after the comparator transition, and the memory circuit is placed after the comparator in column. The memory circuit is implemented as a parallel load register comprising 10 DFFs. When the comparator is activated, all 10 bits of the output of the counter are loaded into the memory circuit at the same time. To avoid instability in the output of the comparator, only one of the counter and the comparator output is allowed to change at a time. This makes sure that a comparator output transition occurs only when the counter value is constant. A 3-bit memory circuit is shown in Figure 4.51.

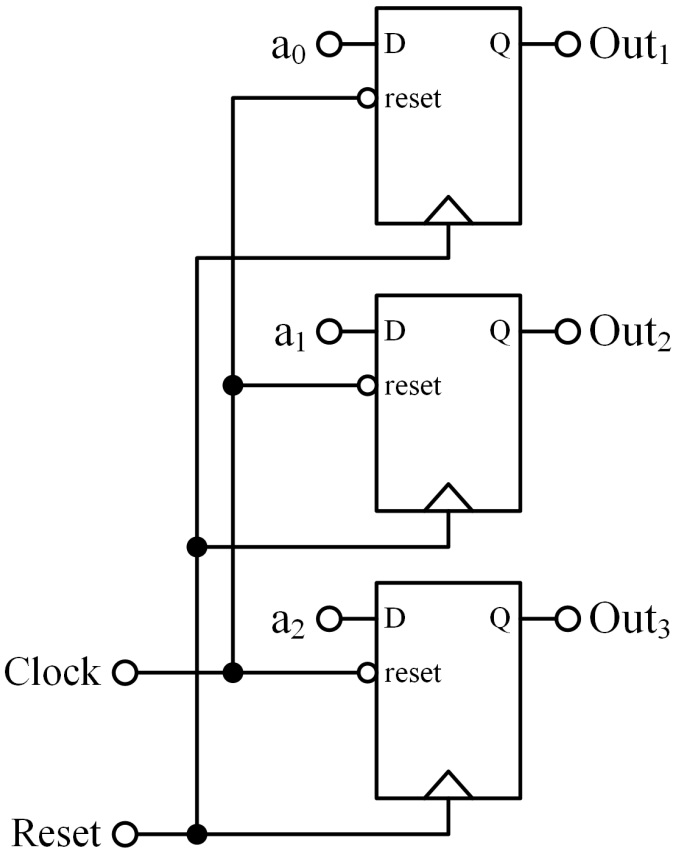

Figure 4.51. 3-bit register circuit.

5. SYSTEM DESIGN

This chapter presents simulation results for the overall system consisting of the building blocks described in Chapter 4. As outlined in Chapter 4, the integrated current-mode Hall-effect sensor array microsystem is constructed using several analog integrated circuit blocks such as amplifiers, filters and ADCs. First, the currents flowing into and out of the twin Hall-effect sensor structure are equalized using a sensor biasing circuit. Then, offset and low-frequency noise of the sensor are reduced using a 4-phase current spinning technique. A digital control unit is implemented for generating clock signals. The Hall current is then converted into voltage using an integration detection topology which provides better noise performance. In the next stage, an elliptic fifth order switched capacitor low-pass filter is used to filter out the offset and noise. Finally, a single-slope analog-to-digital converter is used so the sensor data can be processed by the microprocessor. The top level architecture for the current-mode Hall effect sensor microsystem is demonstrated in Figure 5.1.

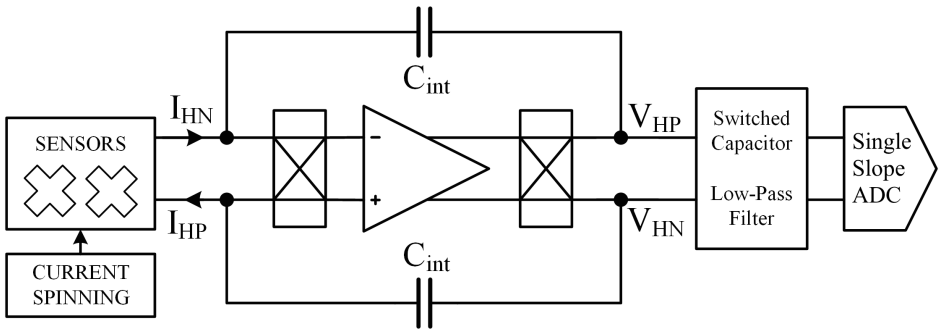

Figure 5.1. Top level architecture of the current-model Hall-effect sensor microsystem.

First, the Hall current is integrated over an integration capacitance and converted to voltage. Figure 5.2 demonstrates the Hall output voltage after the integration for magnetic fields ranging from 0 mT to 20 mT in increments of 4 mT. The periods of measurement and reset phases are set as 512 μs, and the first result is produced between 512 and 768 μs. A maximum output voltage of about 58.5 mV is achieved for an upper limit of 20 mT on the magnetic field in the specified range.

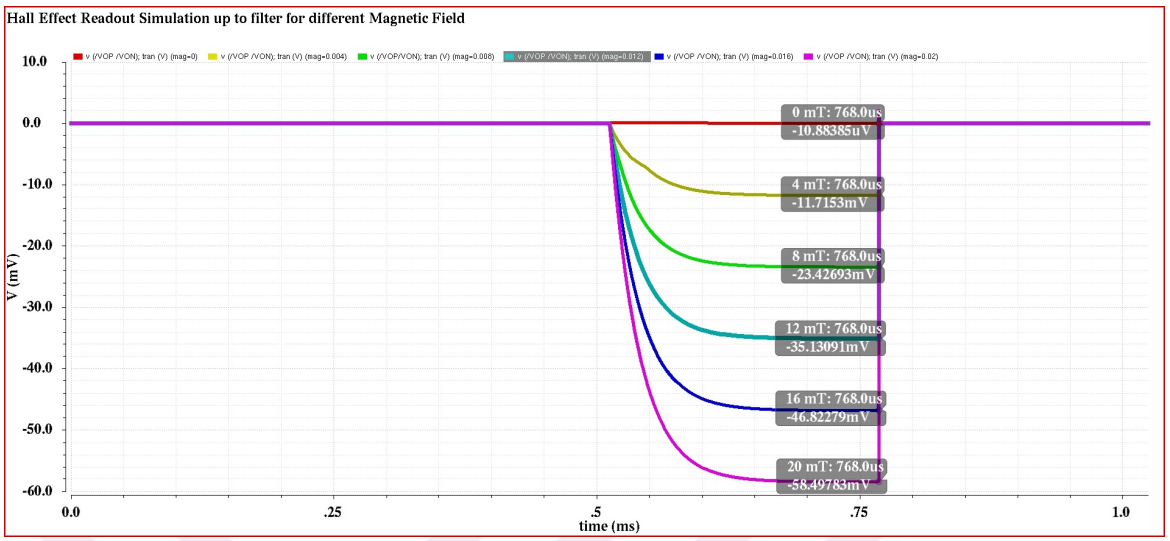

Figure 5.2. Hall output voltage for magnetic fields ranging from 0 to 20 mT in steps of 4 mT.

After the Hall current is converted to voltage, regions in the neighborhood of the maximum voltages are of particular interest. These are subsequently sampled as shown in Figure 5.3.

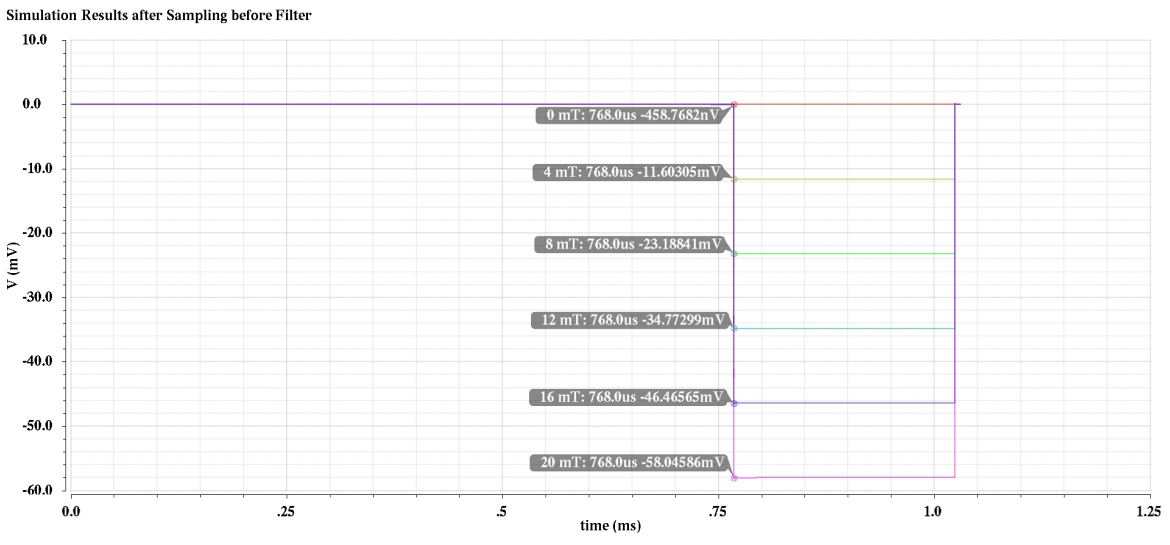

Figure 5.3. Sampled output voltages for magnetic fields ranging from 0 to 20 mT in steps of 4 mT.

The sampled values are then fed through a low pass filter to eliminate the low-frequency noise and offset which are modulated to high frequencies beyond the chopping frequency. Also, these values are amplified by the gain of the filter. The gain of the filter is arranged such that the output voltage of 58 mV at 20 mT is amplified to 1 V to be consistent with the full range of the analog-to-digital converter. The results after filtering and before the ADC for different magnetic field values are shown in Figure 5.4.

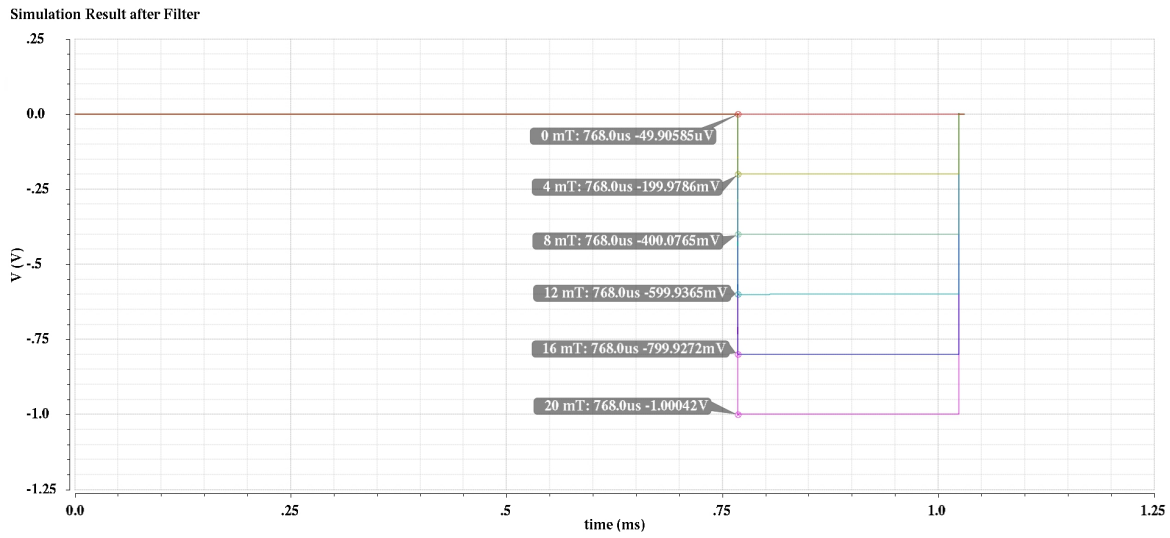

Figure 5.4. The simulation results after the filter for magnetic fields ranging from 0 to 20 mT in steps of 4 mT.

The results of a cascading counter, DAC, and comparator shown in Figure 4.50 are obtained by comparing the output of the DAC with a constant voltage of 600 mV. The digital output of the same structure is shown in Figure 5.5. As shown in Figure 5.5, the result “1001100111” is obtained, which is the binary representation of 615. Considering a 10-bit ADC, 615 is to be divided by 1024 giving 600.58 mV, which closely matches the intended value of 600 mV. Thus, Figure 5.5 shows that the ADC functions as intended.

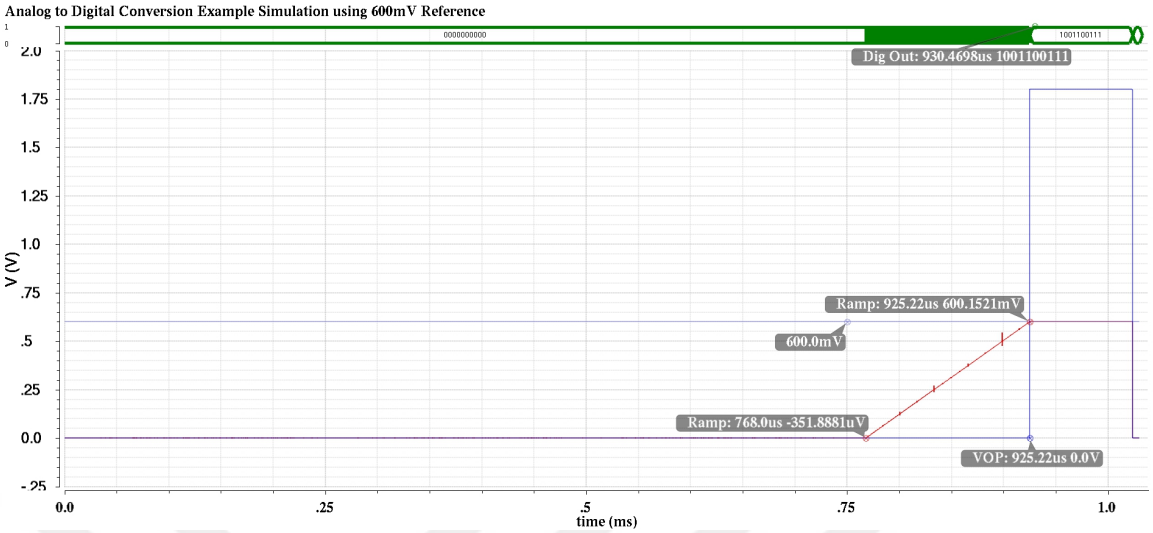

Figure 5.5. Analog-to-digital conversion for a constant voltage of 600 mV.

The filter output shown in Figure 5.4 is fed through a 10-bit single-slope analog-to-digital converter. The digital output of the ADC is shown in Figure 5.6.

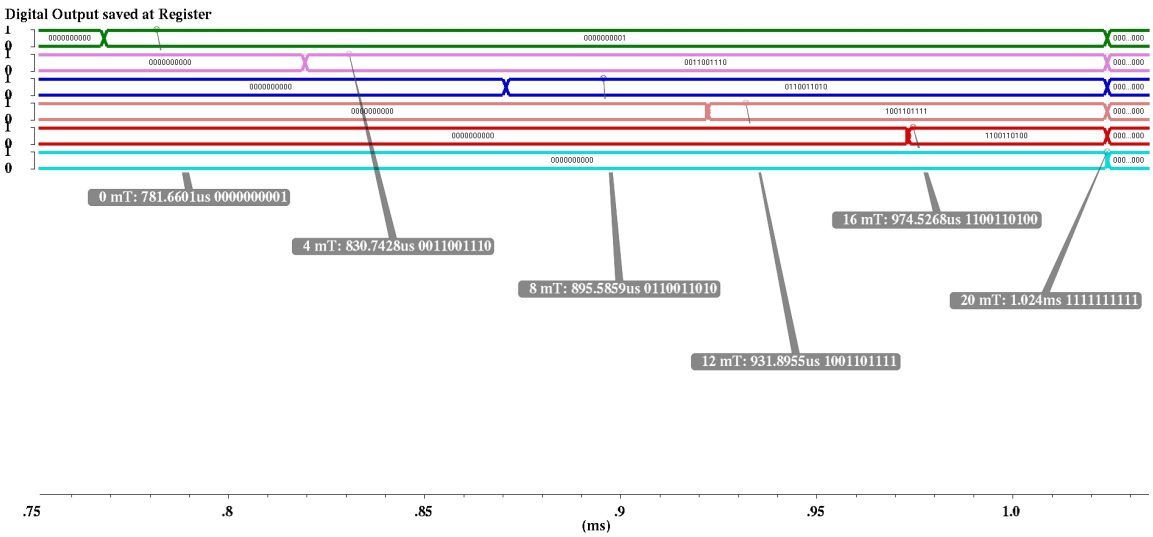

Figure 5.6. The digital output of the ADC stored in the register for magnetic fields ranging from 0 to 20 mT in steps of 4 mT.

6. CONCLUSIONS AND FUTURE WORK

The current-mode twin Hall effect sensor structure studied in this work incorporates various theoretical and practical considerations. Several useful techniques and devices such as dynamic offset cancellation, chopping, switched capacitor, filtering, etc. have been employed to demonstrate as a proof of concept, the functioning of an array based Hall effect sensor. In addition, a comparator, a counter, and a DAC have been designed to build a single-slope ADC for digitizing the detected magnetic field data.

A biasing current of 10 μA is used to bias the cross-shaped Hall effect sensor with the optimum W/L ratio of 2.55, and a sensitivity of 239 nA/T is obtained. When it comes to the chopping technique, the noise magnitude around 1 kHz is decreased from 65 nv to 8 nv. Following this, noise components that appear at odd harmonics of the chopping frequency are eliminated by a 5th order elliptic switched-capacitor low-pass filter. The Hall current is integrated over an integration capacitor, which increases the differential output voltage. The maximum output voltage varies according to the range of magnetic field and the maximum value of the output is sampled and utilized for analog-to-digital conversion. A 10-bit single-slope ADC is designed to represent the magnetic field data digitally.

Future work will involve production of the presented circuit layouts and implementation of the simulated building blocks for successful operation of an array-based Hall effect sensor. The conversion speed of the comparator should be increased further for the implementation of Hall effect sensor array readout. Row and column decoders need to be designed to provide access to each pixel in the array. In order to obtain practical and more useful measurements of magnetic fields with the proposed sensor, a further aim is to achieve greater detection resolution than suggested in this study.

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APPENDIX A: HALL EFFECT SENSOR VERILOG-A MODULE

VerilogA code for the Hall effect sensor is given in Figures A.1-A.3.

```
// VerilogA for Thesis, HallEff_Sens, veriloga

`include "constants.vams"
`include "disciplines.vams"

module HallEff_Sens(A, B, C, D);

    inout A, B, C, D;

    electrical A, B, C, D, A1, A2, B1, B2, C1, C2, D1, D2, M;

    branch (A1, B1) res1;
    branch (A1, M) res2;
    branch (A1, D1) res3;
    branch (B1, M) res4;
    branch (C1, B1) res5;
    branch (C1, M) res6;
    branch (C1, D1) res7;
    branch (D1, M) res8;

    parameter real q = 1.602e-19;
    parameter real Esi = 1.04e-10;
    parameter real k =  1.38e-23;
    parameter real ni0 = 1.49e16;
    parameter real NDnw = 1.7e23;
    parameter real NAsub = 3.41e19;
    parameter real el mob0 = 4.16e-02;
```

Figure A.1. VerilogA code for Hall effect sensor - Part 1

```
28      parameter real VD0 = 6.20e-01;
29      parameter real tnw = 2.33e-06;
30  //    parameter real wnwsub = 9.74e-10;
31      parameter real rHall0 = 1.2;
32      parameter real W = 6e-06;
33      parameter real L = 1e-06;
34      parameter real B_mag = 10e-06;
35      parameter real Upn = 0.0;
36      parameter real delR1 = 1.0;
37      parameter real delR2 = 1.0;
38      parameter real delR3 = 1.0;
39      parameter real delR4 = 1.0;
40      parameter real hooge_par = 2.5e-05;
41      parameter real Fq = 1.0;
42      parameter real Ns = 9.7e12;
43
44      real VD, ni, area, rHall, el_mob, devTemp, k1, wnwsub, teff, par, hall_mob, Rab_cd,
45          RS0, RS1, RS2, Rs, RH, RD, G, phi_H, SI0, SI1, SI2, SI, SVI, Req, cons, n,t;
46
47      analog begin
48
49          devTemp = $temperature;
50          ni = 7.3e21 * pow(devTemp, 1.5) * exp(-1.12 / (2 * 8.62e-05 * devTemp));
51          el_mob = el_mob0 * pow((devTemp / 300), -1.5);
52          rHall = rHall0 * pow((devTemp / 300), 0.13);
53          VD = ((k * devTemp) / q) * ln((NDnw * NAsub) / pow(ni, 2));
54          wnwsub = sqrt(((2*Esi)/q) * (NAsub / ((NAsub + NDnw) * NDnw))) * sqrt(VD - Upn);
55          k1 = ((2 * Esi) / q) * (NAsub / ((NAsub + NDnw) * NDnw));
56
57          teff = tnw - wnwsub;
58          par = 2.0 * (L / W) + 2.0 / 3.0;
59
60          hall_mob = rHall * el_mob;
61
62          phi_H = atan(hall_mob * B_mag);
63
64          G = 1.0 - 1.045 * exp(-1.0 * `M_PI * (L / W));
65
66          SI0 = (G * rHall) / (q * NDnw * (tnw - sqrt(k1 * VD)));
67          SI1 = (G * rHall * sqrt(k1)) / (2 * q * NDnw * sqrt(VD) * pow((tnw - sqrt(k1 * VD)),
            2));
68          SI2 = (G * rHall * sqrt(k1) * (3 * sqrt(k1 * VD) - tnw)) / (8 * q * NDnw * VD * sqrt(
            VD) * pow((tnw - sqrt(k1 * VD)), 3));
69
70          RS0 = 1 / (q * el_mob * NDnw * (tnw - sqrt(k1 * VD)));
71          RS1 = 1 / (2 * q * el_mob * NDnw * sqrt(VD) * pow((tnw - sqrt(k1 * VD)), 2));
72          RS2 = (sqrt(k1) * (3 * sqrt(k1 * VD) - tnw)) / (8 * q * el_mob * NDnw * VD * sqrt(VD)
             * pow((tnw - sqrt(k1 * VD)), 3));
73
74          Rs = RS0 + RS1 * Upn + RS1 * pow(Upn, 2);
75          RH = ((2.0 * Rs) / `M_PI) * (par * `M_PI - 2.0 * `M_LN2);
76          RD = (Rs * par * ((par * `M_PI) - 2.0 * `M_LN2)) / (par * `M_PI - 4.0 * `M_LN2);
77
78          SVI = 1.0 / (NDnw * q * teff);
```

Figure A.2. VerilogA code for Hall effect sensor - Part 2

```
55          k1 = ((2 * Esi) / q) * (NAsub / ((NAsub + NDnw) * NDnw));
56
57          teff = tnw - wnwsub;
58          par = 2.0 * (L / W) + 2.0 / 3.0;
59
60          hall_mob = rHall * el_mob;
61
62          phi_H = atan(hall_mob * B_mag);
63
64          G = 1.0 - 1.045 * exp(-1.0 * `M_PI * (L / W));
65
66          SI0 = (G * rHall) / (q * NDnw * (tnw - sqrt(k1 * VD)));
67          SI1 = (G * rHall * sqrt(k1)) / (2 * q * NDnw * sqrt(VD) * pow((tnw - sqrt(k1 * VD)),
            2));
68          SI2 = (G * rHall * sqrt(k1) * (3 * sqrt(k1 * VD) - tnw)) / (8 * q * NDnw * VD * sqrt(
            VD) * pow((tnw - sqrt(k1 * VD)), 3));
69
70          RS0 = 1 / (q * el_mob * NDnw * (tnw - sqrt(k1 * VD)));
71          RS1 = 1 / (2 * q * el_mob * NDnw * sqrt(VD) * pow((tnw - sqrt(k1 * VD)), 2));
72          RS2 = (sqrt(k1) * (3 * sqrt(k1 * VD) - tnw)) / (8 * q * el_mob * NDnw * VD * sqrt(VD)
             * pow((tnw - sqrt(k1 * VD)), 3));
73
74          Rs = RS0 + RS1 * Upn + RS1 * pow(Upn, 2);
75          RH = ((2.0 * Rs) / `M_PI) * (par * `M_PI - 2.0 * `M_LN2);
76          RD = (Rs * par * ((par * `M_PI) - 2.0 * `M_LN2)) / (par * `M_PI - 4.0 * `M_LN2);
77
78          SVI = 1.0 / (NDnw * q * teff);
```

Figure A.3. VerilogA code for Hall effect sensor - Part 3