DESIGN OF HIGH EFFICIENCY SWITCHING CONVERTERS FOR MOBILE APPLICATIONS

by

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Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfilment of
the requirements for the degree of
Doctor of Philosophy

Graduate Program in Electrical and Electronics Engineering

Boğaziçi University

2020

ACKNOWLEDGEMENTS

I consider myself lucky as I was able to appreciate the value of being a Ph.D. student while I was still a student. The insight and experience I gained during this period supported my career in the industry as well as provided the background for my new position in the academia. All this would not have been possible without the guidance, supervision and patience of my Ph.D. supervisor Prof. Dr. Günhan Dündar. I would also like to thank my thesis advisors Prof. Dr. Şenol Mutlu and Assoc. Prof. Dr. Hakan Doğan for their valuable insights and contributions to this work.

I would like to thank Assoc. Prof. Dr. Mustafa Berke Yelten and Asst. Prof. Dr. İsmail Faik Başkaya for their collaboration in many topics, help in correcting the mistakes in this work and accepting to join the Ph.D. dissertation defense.

I would like to thank Merve Toka Koç and Faik Durmaz for their contributions to this work during their MSc studies, their collaboration and feedback has considerably enriched this work.

I would like to thank Dr. Okan Zafer Batur, Dr. Engin Afacan, Naci Pekçokgüler, Dr. Berk Çamlı, Merve Albayrak, Dr. İsmail Kara, Mustafa Becermiş, Dr. Baykal Sarıoğlu, Dr. İskender Haydaroğlu, Dr. Bedri Gürkan Sönmez and other Beta Lab. members for their support and friendship during my Ph.D. studentship.

I would like to thank Dr. Erşed Akçasu for providing me the time flexibility to complete my coursework during the time I was working at OEA Microelectronics. I would also like to thank Dialog Semiconductor for supporting the patent applications mentioned in this work.

I would assume that I had inherited my academic curiosity from my mother Dr. Fahire Ozanoğlu. I would like to thank her, Selime Aksu and Principal Ferit Aksu for their limitless support. I would like thank my wife Burçak Aksu Ozanoğlu for her endless

unconditional love, and I would like to thank Eskut Ozanoğlu for providing me with an experience equivalent to a second Ph.D.

Finally, I dedicate this work to the memory of my father Dr. Enver Ozanoğlu, thanking him for the perspective and guidance he provided with me throughout the years.

ABSTRACT

DESIGN OF HIGH EFFICIENCY SWITCHING CONVERTERS FOR MOBILE APPLICATIONS

High power efficiency is a key design specification in mobile applications, mainly to increase battery life. To answer this need, switching converters are preferred in such applications to convert the battery voltage to voltage domains of various blocks. In this thesis, design improvements and novel solutions aiming to increase power efficiency and to enhance system performance for mobile platform switching converters are proposed for buck, boost, and buck-boost topologies. After a brief description of switching converter operation, a novel technique to improve power efficiency in buck converters is given, through optimized resistive and capacitive power losses of the output stage. Then, a charge recycling technique for single inductor dual output buck converters is described. Next, two improved control techniques for buck-boost converters based on hysteretic control and current mode control have been proposed. Finally, two novel techniques addressing the lock-out phenomenon occurring in boost and buck-boost converters are described. Simulation results show that the targeted performance improvements are achieved, thus demonstrating promising solutions for various future mobile platforms.

ÖZET

MOBİL UYGULAMALAR İÇİN YÜKSEK VERİMLİ ANAHTARLAMALI GÜÇ KAYNAĞI TASARIMI

Yüksek güç verimli çalışma, pil kullanım süresini uzattığı için mobil uygulamalarda en önemli tasarım ölçütlerinden biridir. Bu tasarım ölçütünü karşılamak amacıyla mobil uygulamalarda pil voltajını diğer farklı uygulamaların gerilim seviyelerine dönüştürmek için anahtarlamalı güç kaynakları tercih edilir. Bu tez çalışmasında, çıkış alçaltıcı, çıkış yükseltici ve alçaltıcı/yükseltici dönüştürücü örnekleri üzerinden, güç verimini ve sistem performansını geliştirmeyi hedefleyen tasarım iyileştirmeleri ve özgün mimari çözümler sunulmuştur. Anahtarlamalı güç kaynaklarının kısa bir özetini takiben, çıkış alçaltıcı dönüştürücüler için güç verimini iyileştirmeyi hedefleyen özgün bir tasarım tekniği verilmiştir. Bahsedilen teknik, çıkış katının direnil ve sığasal kayıplarının toplamını en aza indirgemeye dayanmaktadır. Sonraki bölümde tek endüktör çoklu çıkış dönüştürücüler için yeni bir yük geri dönüştürme tekniği anlatılmıştır. Bu bölümü takiben, alçaltıcı/yükseltici dönüştürücü uygulamaları için, histeretik ve akım modlu kontrol üzerine geliştirilmiş iki özgün kontrol tekniği verilmiştir. Son olarak, çıkış yükseltici ve alçaltıcı/yükseltici dönüştürücülerde gözlemlenen kilitlenme olayını çözmeyi hedefleyen iki yeni yaklaşım önerilmiştir. Benzetim sonuçları hedeflenen performans iyileştirmelerine ulaşıldığını, böylece çeşitli mobil uygulamalar için gelecekte kullanılabilir çözümler üretildiğini göstermektedir.

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LIST OF SYMBOLS

f_{CLK}	Clock frequency
f_{SW}	Switching frequency
g_m	Transconductance of a MOSFET
I_d	Drain current of a MOSFET
kHz	Kilo-hertz, frequency unit
MHz	Mega-hertz, frequency unit
r_{on}	On resistance of a MOSFET switch
T	Temperature
V_d	Drain voltage of a MOSFET
V_{ds}	Drain to source voltage of a MOSFET
V_g	Gate voltage of a MOSFET
V_{gs}	Gate to source voltage of a MOSFET
V_{in}	Input supply voltage
V_{out}	Output voltage

LIST OF ACRONYMS / ABBREVATIONS

CMC	Current Mode Control
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital Analog Converter
DCR	Direct Current Resistance
DVC	Dynamic Voltage Control
EMI	Electromagnetic Interference
HSS	High Side Switch
IC	Integrated Circuit
LDO	Low Drop-out Regulator
LSS	Low Side Switch
MIM	Metal Insulator Metal
NFC	Near Field Communication
OLED	Organic Light-Emitting Diode
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PMIC	Power Management Integrated Circuit
PSM	Pulse Skip Modulation
PWM	Pulse Width Modulation
SIDO	Single Inductor Double Output
SIMO	Single Inductor Multiple Output
VMC	Voltage Mode Control
ZXC	Zero Cross Comparator

1. INTRODUCTION

The growing popularity of portable devices has been the driving force of the electronics industry during the last decade. The rise in the demand for mobile phones was followed by tablets, smart watches, e-book readers, handheld game consoles to many other personal, biomedical, and industrial applications. Mostly powered by a single Li-ion rechargeable battery cell, a portable device system may include a wide range of integrated circuit (IC) components including microprocessors, sensors, data converters, memory, transceivers, audio modules, etc.

As an example of a portable device system, Figure 1.1 gives a teardown of iPhone 7 Plus, listing the applications on the printed circuit board (PCB) [1]. Figure 1.1(a) shows the components on the front side: Apple A10 Fusion (red), Qualcomm LTE Modem (orange), Skyworks and Avago power amplifier modules (yellow, green, blue). Figure 1.1(b) shows the components on the flip side: Murata Wi-Fi/Bluetooth module (orange), NXP near field communications (NFC) controller (yellow) and Qualcomm transceivers (blue, magenta).

All these applications come with different input supply voltage requirements with different input current specifications, e.g. most digital applications require ~1V supply voltage with up to >10A, whereas a display driver requires ~36V input supply voltage. In addition to that, the Li-ion battery source voltage changes over time: from ~4.8V (fully charged) to ~2.8V (almost discharged). This necessitates the use of different voltage converters for different applications.

Small form factor and long battery life are two of the critical requirements of portable devices. Merging different voltage converter modules in a single IC for smaller form factor has been possible by improvements in IC process fabrication such as twin well process and trench isolation. Called power management integrated circuits (PMIC), these ICs include various modules for voltage conversion, together with side applications such as temperature sensors, data converters and controllers in a single chip [2]. Referring back to Figure 1.1(b), Dialog PMIC (green) is an example of such an IC.



(a) (b)

Figure 1.1. Teardown of iPhone 7 Plus logic board: (a) front side (b) flip side [1].

To extend battery life, high power efficiency becomes an essential design target. Answering this need, most PMICs utilize high efficiency switching converters with a single inductor, such as buck, boost, or buck-boost converters [3]. Design specifications of such switching converters include supplying a wide current output range with high efficiency, low output voltage ripple, and sufficient line/load transient response. High power efficiency has another advantage in portable devices: the device is protected from over-heating due to loss power being converted to heat dissipation.

However, switching converter design inherently comes with many design challenges, particularly emerging from using an inductor and switching large (>1A) amount of currents which make reliable control techniques difficult to achieve while meeting the design specifications. In the meantime, design topologies aiming to improve power efficiency are

constantly evolving. Consequently, the mentioned challenges and demands present an ongoing research platform for new design topologies and control techniques.

1.1. Motivation and Key Contributions

The motivation of this work is to provide novel design solutions for mobile platform switching converters aiming to increase power efficiency and to enhance system performance, through the examples of buck, boost, and buck-boost converters. Within the framework of this thesis, the following contributions protected by patent applications have been achieved:

- A novel technique to improve power efficiency in buck converters has been proposed, targeting to optimize resistive and capacitive power losses of the output stage. Power losses are calculated in analog domain using a novel arithmetic cell called "adaptive g_m" [4-6].
- A charge recycling technique for single inductor dual output (SIDO) buck converters has been proposed, enabling double polarity operation [7].
- A control technique for buck-boost converters based on hysteretic control has been proposed targeting a low power solution owing to its simplicity in topology [8,9].
- An improved current mode control technique for buck-boost converters has been proposed utilizing separated buck and boost pulses aiming to improve power efficiency, to reduce inductor current ripple and to improve stability [10].
- Two novel techniques addressing the lock-out phenomenon occurring in boost and buck-boost converters have been proposed. Both techniques aim to sense the peak of voltage conversion vs. duty cycle curve and limit the duty cycle accordingly, thus achieving expanded operational range and reliability of the switching converter [11,12].

1.2. Thesis Organisation

This work is organized as follows:

Chapter 2 gives an introduction to switching converter operation, providing details on buck, boost, buck-boost and SIDO buck design architectures and control modes, followed by a survey of power efficiency improvement solutions in switching converters.

Chapter 3, which is the core work of this thesis, describes the adaptive pass device control technique through the example of a buck converter. An analytic background on capacitive and resistive power losses in buck converters is followed by system level to transistor level design implementation and simulation results focusing on efficiency improvement in different supply, temperature, process and load current corners. Appendix A gives details regarding layout design.

Chapter 4 provides a novel switching architecture topology for SIDO buck converters, enabling double polarity operation with charge recycling. Two switching sequences targeting low load current operation and high load current operation are proposed.

Chapter 5 describes two novel control techniques for buck-boost converters. The first technique addresses a low power design solution targeting wearable applications. The second technique proposes an improved switching technique for current mode operation.

Chapter 6 introduces two circuit level solutions to eliminate the lock-out phenomenon observed in boost and buck-boost converters, which are “duty cycle limitation by replica voltage drop” and “duty cycle limitation by sawtooth signal prediction”.

Chapter 7 concludes the thesis.

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2. SWITCHING CONVERTER OPERATION

Various circuit topologies and techniques for power management exist, each having different trade-offs and providing solutions for different problems. The basic topology incorporating a feedback loop is the linear regulator where a driver transistor sets the output voltage together with an operational amplifier. The loop is formed such that the output voltage matches a reference voltage and the driver transistor is biased accordingly. This transistor (initially a bipolar transistor, later typically replaced with a PMOS transistor) is historically called the “pass device”. Linear regulators preferably can operate with a small voltage drop on the pass device, allowing a higher range for output voltage, hence the term “Low Drop-out Regulator” (LDO) is commonly used. LDOs can achieve low output noise, high power supply rejection, very high loop gain [13] and preserve their place as one of the basic blocks of a power management system.

Capacitive charge pumps, also called switched capacitor voltage converters, can be used to generate voltages lower/higher than the input voltage supply. This is done by employing a floating or “bucket” capacitor where the floating capacitor is charged to a portion of the input supply voltage and together with various switch topologies, different output voltages can be generated [14,15]. Due to their relatively high output resistance but relatively simple topology, capacitive charge pumps are typically preferred in applications with sub-mA load current requirements.

Inductive switching converters step in when battery life is a concern and high power efficiency is needed. Though many topologies utilizing transformers and multiple inductors do exist, vendors of portable systems prefer switching converters with a single inductor to save PCB area and to reduce costs. This chapter focuses on the three possible switching converter architectures using a single inductor. Section 2.1 describes buck converters which step-down the input voltage to generate a lower output voltage, followed by boost converters stepping-up the input voltage to voltages higher than the input voltage, and Section 2.3 describes buck-boost converters which can generate output voltages lower and higher than the input voltage. The chapter proceeds with a brief description of SIDO buck converter

topologies and design challenges. Finally, a survey on design and implementation techniques for increasing power efficiency in switching converters is given.

2.1. Buck Converters

For many PMIC applications, buck converters are the most critical building blocks, as the battery lifetime is set by the efficiency performance of the buck converter. The buck converter output is always lower than its input, hence the name “buck” is given. In general, buck converters step in where power efficiency is a system requirement and step-down conversion is requested.

Figure 2.1 illustrates the difference between an ideal LDO and an ideal buck converter through the example of a 4V input voltage source and a 16A load current of a microprocessor operating at 1V. For the case of the LDO, the same 16A load current flows from the battery and pass device to the load. The 3V voltage drop on the pass device with 16A current generates a huge 48W power loss which is converted to heat. In contrast, buck converters ideally can achieve 100% power efficiency, as in the case example, only 4A load current will be drained from the input supply at 4V (16W), to supply the 16A load current at 1V output (16W). Thus, no power loss will be observed on the buck converter.

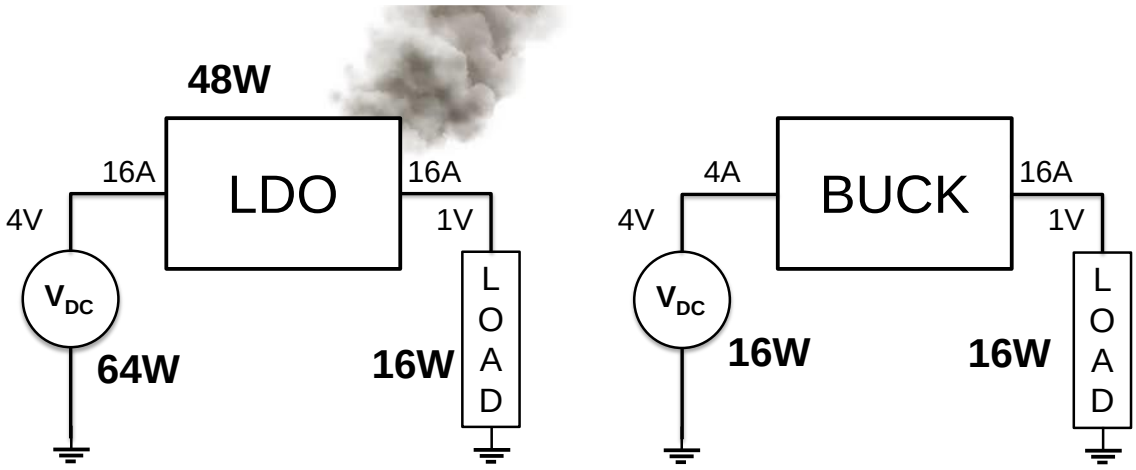


Figure 2.1. An LDO vs. a buck converter.

This high efficiency voltage conversion is made possible by the use of an inductor element and its capability to store current through its magnetic field. Figure 2.2 depicts the basic buck converter topology which consists of two switches, an inductor connected to the output node, and an output capacitor [16].

In the conventional switching sequence, there are two switching states: in state I, S_1 is ON, S_2 is OFF, current flows from the input supply to the output load through the inductor, while storing current on the inductor. In state II, S_1 is OFF, S_2 is ON, the inductor is connected to ground, still the stored current continues to supply the output load – while the input supply is left floating, hence the average current drawn from the input supply is reduced.

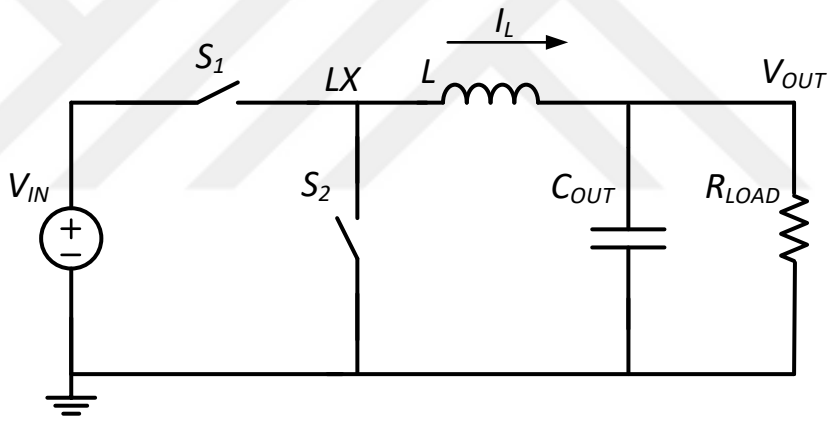


Figure 2.2. Basic buck converter topology.

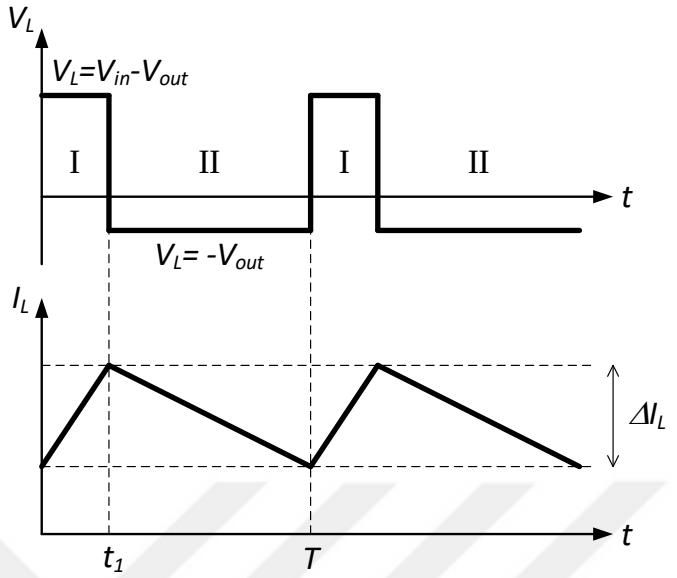


Figure 2.3. Inductor voltage and current waveforms.

The inductor voltage and current waveforms through this switching sequence is given in Figure 2.3. In state I, a $\Delta V_L=V_{in}-V_{out}$ voltage drop is observed on the inductor. With this voltage drop, the change in the inductor current during this time interval will be:

$$\Delta I_{L,I} = \frac{V_{in} - V_{out}}{L}\ t_1 \tag{2.1}$$

Similarly, when in state II, a $\Delta V_L= -V_{out}$ voltage drop will be observed on the inductor. Thus, the change in the inductor current during this time interval will be:

$$\Delta I_{L,II} = \frac{-V_{out}}{L}(T - t_1) \tag{2.2}$$

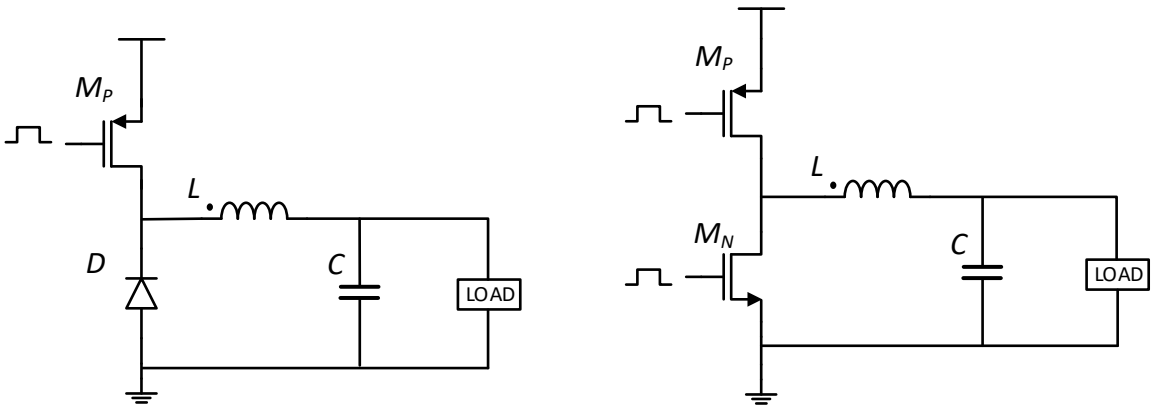
In steady state, ΔI_L in both switch states will be equal, hence equalizing both equations, the voltage conversion ratio of the switching converter can be achieved:

$$\frac{V_{out}}{V_{in}} = \frac{t_1}{T} = D \tag{2.3}$$

where *D* is the duty cycle of the switching converter. Equation (2.3) denotes two important outcomes: first the voltage conversion ratio increases linearly with the duty cycle, second the output voltage will always be less than the input voltage.

Early buck converters with active switches utilized a single “pass device” together with a diode to implement the switching sequence. Depicted in Figure 2.4(a), the diode element naturally conducted current flowing from the inductor in state II and prevented reverse current from the inductor to discharge the output capacitance, replacing S_2. Only one control signal is needed for this topology, hence called the “asynchronous buck converter”.

Together with technology scaling, recent IC applications continuously required less supply voltage. This necessitated a topology update in buck converters: the diode was replaced with a second pass device as the efficiency loss introduced by the diode element became more significant. This new topology required a separate control signal for each switch, hence called the “synchronous buck converter”, given in Figure 2.4(b). Synchronous switching requires security precautions to prevent overlapping of both switches which may result in short-circuit of the input supply and also allows to introduce more flexibility in the system, such as negative current operation to discharge the output capacitor. The upper switch is called high side switch (HSS) and the lower switch is called low side switch (LSS).



(a) (b)

Figure 2.4. Introducing the switch element: (a) asynchronous buck converter (b) synchronous buck converter.

A feedback loop modulates the duty cycle such that the output voltage matches the target voltage of the application. The target voltage can be a fixed voltage coming from a bandgap reference, or as in recent applications, the target voltage can be modulated with time. Many digital applications today, including microprocessors, utilize dynamic voltage control (DVC) to enhance system performance e.g. by reducing supply voltage when the microprocessor is not used in order to reduce leakage current, and by increasing supply voltage when high performance and higher clock frequency operation are requested. Buck converters with dynamically changing output voltages are also utilized as a part of RF power amplifier applications, where the envelope of the transmitted signal is set by the buck converter to increase power efficiency [17].

Various loop techniques are available modulating the duty cycle to set the output voltage, as defined in the following sections.

2.1.1. Voltage Mode Control

Voltage mode control (VMC) topology is given in Figure 2.5. The topology is based on the pulse width modulation (PWM) method. The output voltage V_{OUT} is fed back to an operational amplifier called the "error amplifier" comparing with a reference voltage V_{REF}. The error amplifier output V_{ERR} and a saw tooth signal V_{RAMP} are applied to inputs of the PWM comparator. The output of PWM comparator together with the system clock form inputs of a control logic block, which drives the control signals for the pass devices.

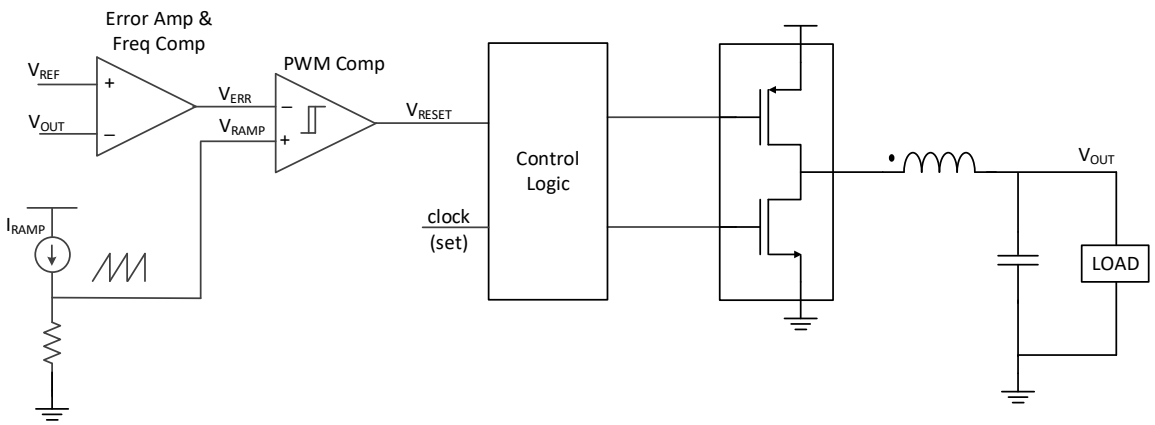


Figure 2.5. Voltage mode control feedback loop.

Figure 2.6 demonstrates the PWM operation waveforms, the HSS turns ON with the clock starting to charge the inductor. HSS stays ON until the sawtooth signal V_{RAMP} crosses the error amplifier output voltage V_{ERR}; following this crossing HSS is OFF and LSS is turned on, discharging the inductor through the ground path, until the clock signal. By using this technique, the duty cycle will increase when error voltage V_{ERR} increases and will decrease in the same manner.

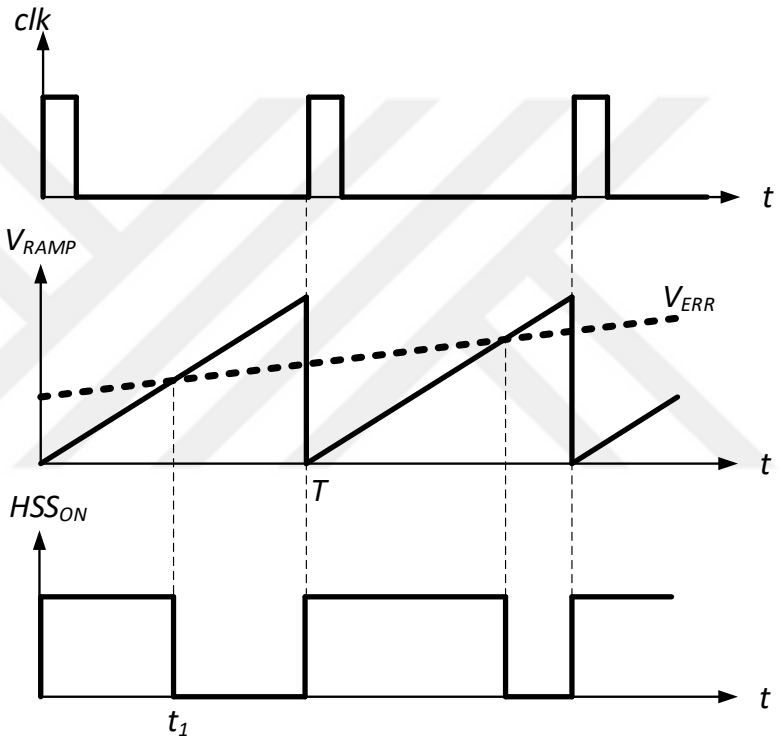


Figure 2.6. PWM modulation technique.

Though a robust control mode technique, the voltage mode control needs complicated frequency compensation techniques like Type-III, to compensate the complex conjugate pole formed by the inductor and output capacitor. Another design challenge in VMC designs is poor line regulation, as given with Equation (2.3) any change in input supply voltage directly translates to change in output voltage, which necessitates feed-forward techniques to improve line regulation performance.

2.1.2. Current Mode Control

Current mode control (CMC) topology is formed by introducing the inductor current to the feedback loop. Figure 2.7 gives the basic current mode control topology, where the ramp signal is replaced by a sensed replica of the inductor current – which coincidentally has the shape of a sawtooth signal. With this formation, the inductor current is set such that the output voltage meets the reference voltage.

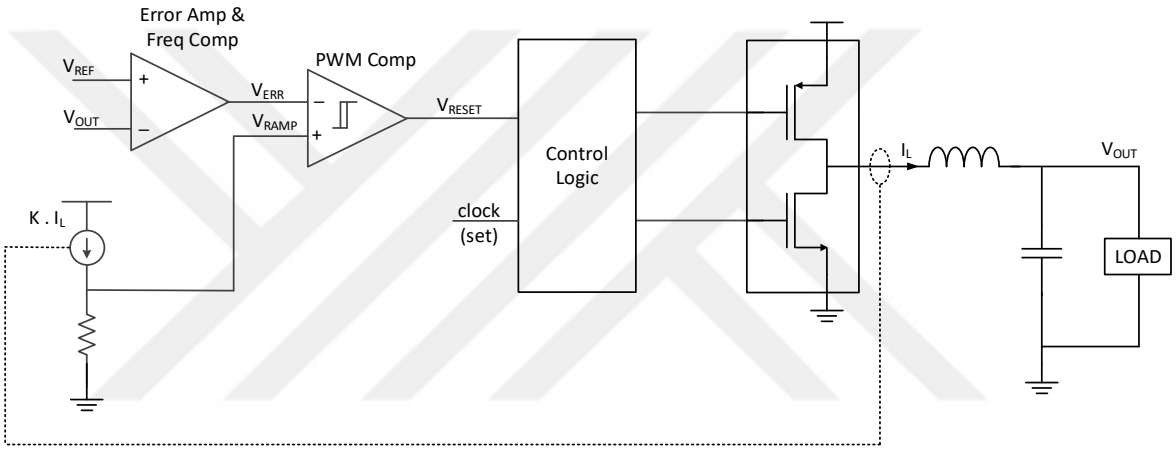


Figure 2.7. Current mode control feedback loop – basic topology.

The signaling of CMC is similar to PWM modulation, the HSS will be ON together with the clock, the sensed replica of the inductor current will rise until it crosses the error voltage, then LSS switch will take over. As the peak current of the inductor is controlled, it can be assumed that the buck converter behaves like a current source. This fact brings forth the following advantages:

- As the buck converter behaves like a current source, the complex conjugate pole at the output is cancelled out from the system. Thus, CMC loop is easier to stabilize.
- For higher power applications, CMC allows parallel connection of power stages – similar to parallel connection of current sources.
- CMC introduces a control on the peak inductor current, making implementation of protection mechanisms that protect the inductor from magnetic saturation easier.

In implementation, the added noise to the sensed replica of the inductor current introduces a jitter to the peak inductor current, which might be disadvantageous in some applications. Another disadvantage of CMC occurring at high duty cycles is a possible second operation mode with half of the clock frequency, thus called “sub-harmonic oscillation”. This phenomenon can be avoided by introducing a sawtooth signal in parallel to the sensed inductor current, called “slope compensation”. The complete CMC topology including slope compensation is given in Figure 2.8.

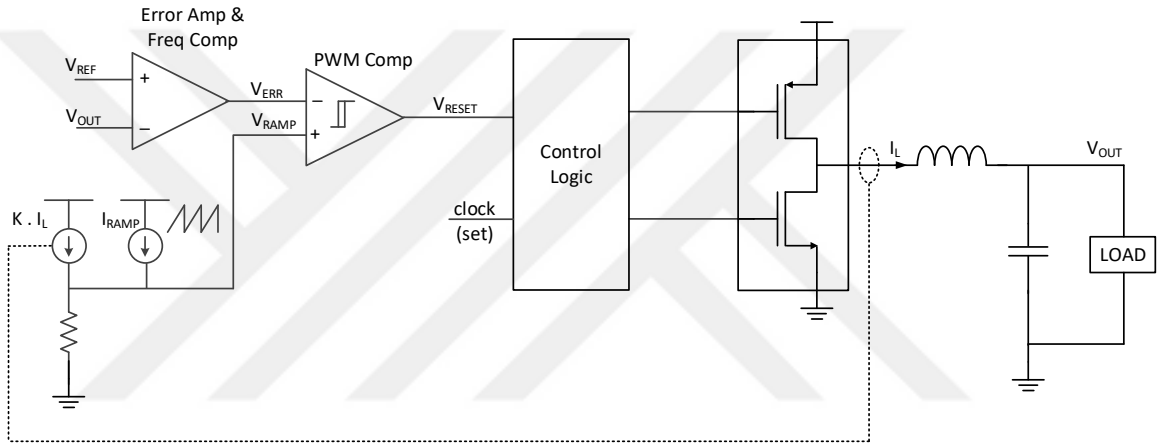


Figure 2.8. Current mode control feedback loop including slope compensation.

2.1.3. Hysteretic Control

Hysteretic control steps out as a simpler to implement control method, generally preferred at low load currents. Figure 2.9 gives an example of hysteretic control, where a hysteretic window is defined at the output voltage of the buck converter and HSS becomes active when the output voltage hits the lower limit of the window V_{REF}. A single pulse or a set of pulses are applied with the buck switch charging the output capacitor through the inductor until the output voltage hits the upper limit V_{REF1} [18].

An outstanding advantage of hysteretic control is its simplicity allowing very low quiescent current operation. As in Figure 2.9 when HSS is not active, the buck converter can stay in “idle mode” or “sleep mode” where the circuit blocks can be put to sleep, with only the output voltage comparator needing to be active, until the comparator toggles. Another

advantage of hysteretic control is line regulation: as in the loop formula, there are no terms associated with input voltage, the converter is strongly insensitive to variations in the supply voltage.

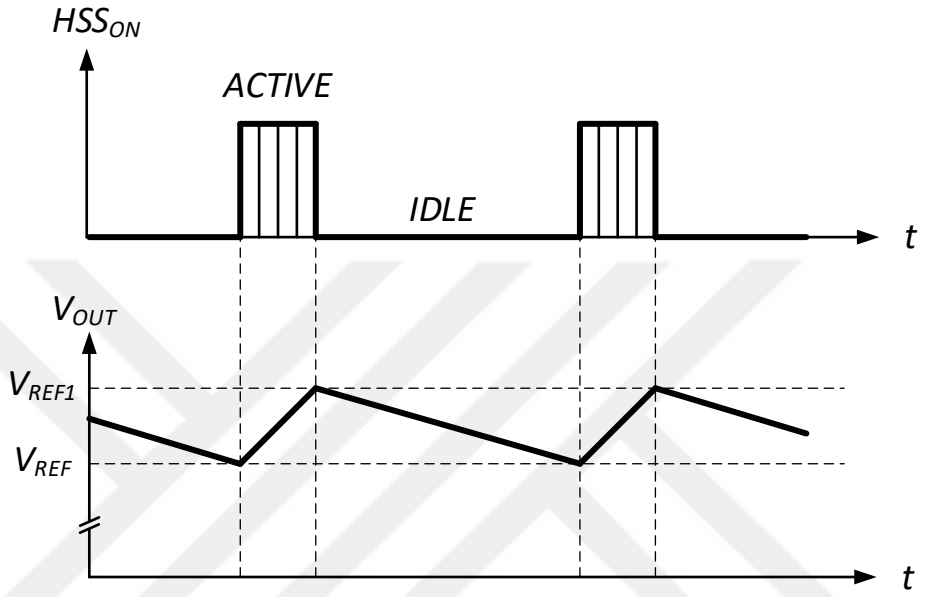


Figure 2.9. Hysteretic control through output voltage.

Alternative implementations of hysteretic control do exist, utilizing constant on-time for HSS switch signaling [19], or defining a hysteretic control window with peak and valley points of the inductor current as the upper and lower hysteretic limits [20].

2.2. Boost Converters

Considering mobile platforms using a single Li-ion battery cell of 3.8V, generation of voltages higher than the battery voltage is needed in many applications: display drivers, audio drivers, power amplifier modules, vibration motor drives, etc. The boost converter answering this need, is the second switching converter topology using a single inductor, formed by connecting the inductor to the input supply.

Shown in Figure 2.10, in state I, the boost switch is ON and the inductor is shorted to ground, hence the current flowing from the input supply is stored on the inductor. In state-

II, upon releasing the switch, the stored inductor current starts flowing from the input supply through the diode to the output node, charging the output capacitor to voltages higher than the input supply.

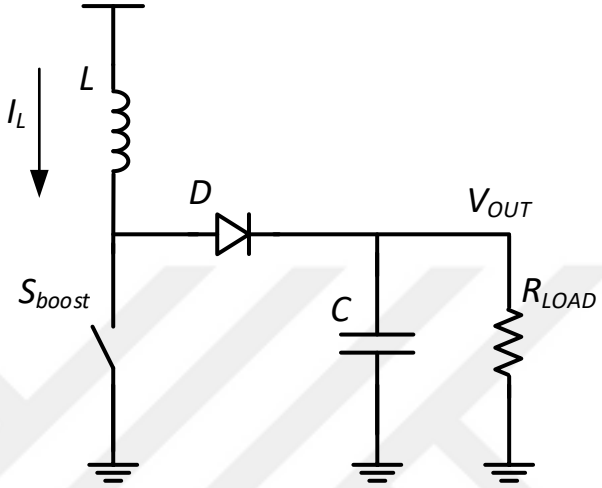


Figure 2.10. Boost converter topology.

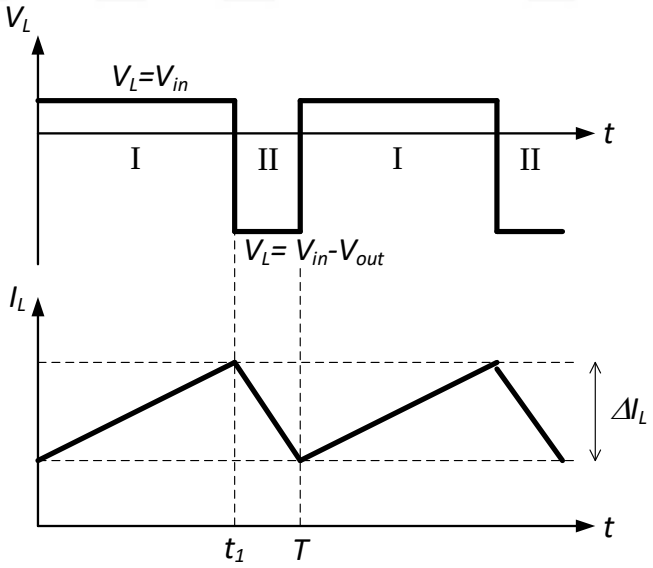


Figure 2.11. Boost converter inductor voltage and currents.

The inductor voltage and current waveforms of the boost converter are given in Figure 2.11. Similar to buck converters, using the inductor slope formula, the voltage conversion ratio of the boost converter can be calculated as:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.4}$$

Equation (2.4) shows that the voltage conversion ratio will always be higher than 1. Thus, the topology is also called a "step-up" converter. A deeper analysis on the voltage conversion ratio vs. duty cycle is given in Chapter 6, providing novel solutions to a lock-out phenomenon induced by the parasitic resistors on the inductor current path.

2.3. Buck-Boost Converters

The third switching converter topology employing a single inductor is the buck-boost converter. Figure 2.12(a) gives a traditional buck-boost converter, where the inductor is connected to ground. In state I the buck-boost switch is on, the inductor stores current flowing to ground, in state II the switch is off and current flows from V_{OUT} to ground through the diode thus producing a negative voltage at the output, hence the topology is also called "the inverting buck-boost converter". This topology is used in applications where a negative voltage domain is needed, like organic light-emitting diode (OLED) display drivers.

It is possible to re-configure the inverting buck-boost topology to generate positive output voltages, by introducing additional switches. Figure 2.12(b) gives the non-inverting buck-boost converter where the introduced switches help generate positive inductor current, hence positive output voltages. Figure 2.12(b) resembles a buck converter cascaded with a boost converter, hence the name "buck-boost" is given.

The switching sequence of the non-inverting buck-boost topology is given in Figure 2.13. In state I, buck switch and boost switch are ON, and current is stored on the inductor flowing from the input supply to ground. In state II, buck switch and the boost switch are OFF, the inductor current flows from ground to the output through the buck and boost diodes.

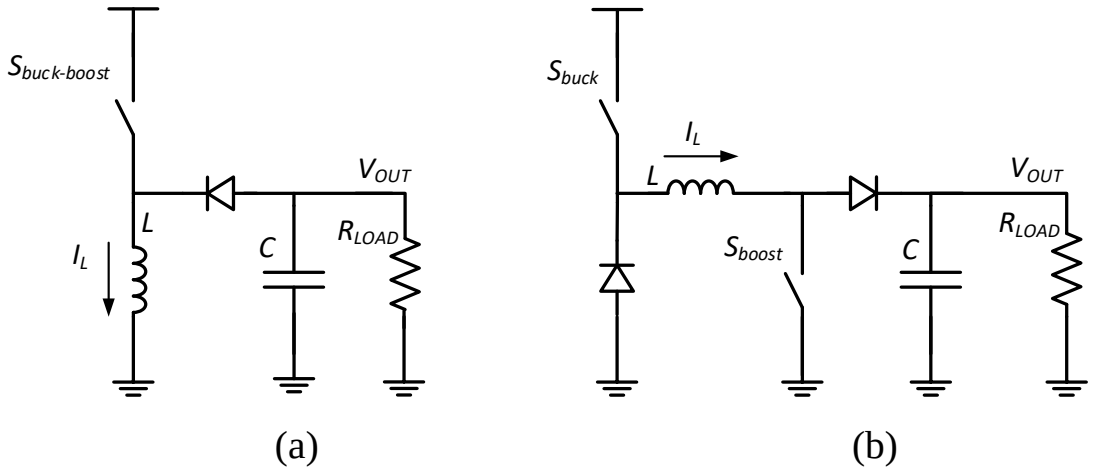


Figure 2.12. Buck boost topologies: (a) the inverting buck boost converter (b) the non-inverting buck-boost converter

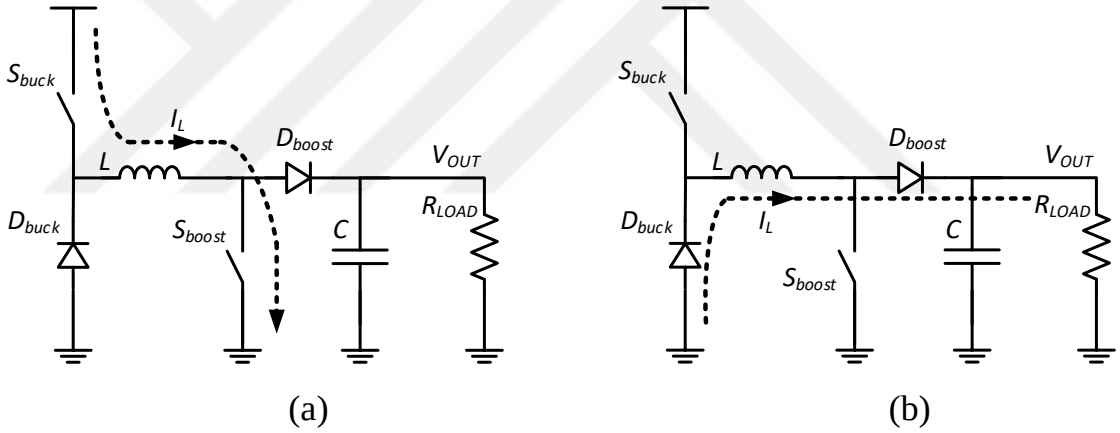


Figure 2.13. Non-inverting buck-boost switch states: (a) state I (b) state II

Similar to buck and boost converters, using the inductor slope formula, the voltage conversion ratio of the boost converter can be calculated as:

$$\frac{V_{out}}{V_{in}} = \frac{D}{1-D} \tag{2.5}$$

which is actually the buck conversion ratio multiplied by the boost conversion ratio. Equation (2.5) shows that the conversion ratio can be both less than one or higher than one depending on the duty cycle, meaning output voltages less than or higher than the input voltage can be generated, introducing flexibility to system level design. Also called “step-

up/step-down" converter, buck-boost converters have a unique place in power management circuit topologies.

Comparing the basic buck-boost operation with a typical buck or boost converter, we can list the following disadvantages [21]:

- Four switches (including diode-switches) change state at each cycle, thus switching loss is two times that of a typical buck or boost converter.
- The average inductance current is significantly higher than the load current, given as: $I_L=I_{LOAD}/(1-D)$ e.g. when D=0.5, $V_{IN}=V_{OUT}$, $I_L=2I_{LOAD}$, which leads to increase in inductor current.
- Resistive losses will be higher together with inductor current e.g. for D=0.5, losses due to the parasitic resistances will be four times of a buck converter.
- Higher inductor current ripple occurs with respect to buck or boost converters.

The mentioned disadvantages can be reduced if we separate the buck and boost pulses: meaning that in a given cycle, either the buck switches *or* the boost switch will be switching. Two improved control techniques using separated buck and boost pulses for CMC and hysteretic control are proposed in Chapter 5.

2.4. SIDO Buck Converters

In portable applications, form factor and cost are two of the most important system design criteria. Therefore, design topologies with smaller size and minimum number of extra components are preferred. Single inductor dual output (SIDO) and single inductor multiple output (SIMO) buck converters have been proposed which can supply more than one output voltage by using a single inductor, and which can achieve high power efficiency numbers at the same time [22]. SIDO and SIMO buck topologies are preferred when the total load current can be supplied by a single inductor and it is requested to save printed circuit board (PCB) area and cost by removing additional external components. Figure 2.14 shows a conventional SIDO buck converter. The buck switch S_{buck} charges the inductor and the load switches S_0 and S_1 distribute the inductor current to the outputs.

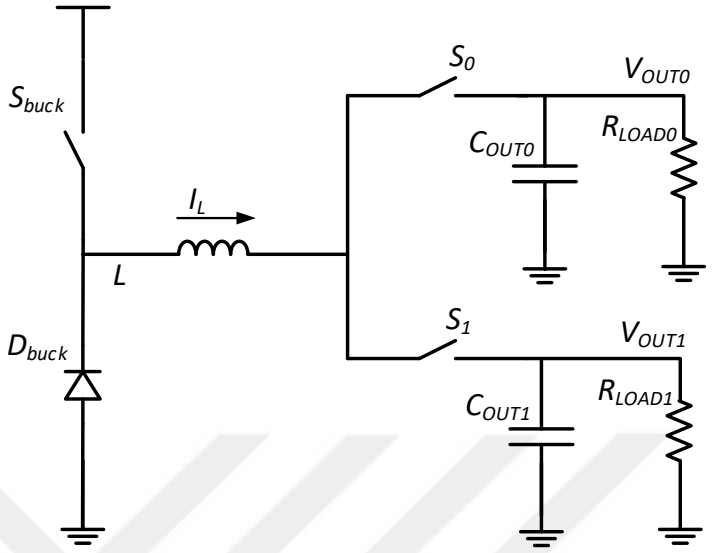


Figure 2.14. Conventional SIDO buck converter.

Saving from external components come back with the following drawbacks: limited output current capability, need for complex control modes supporting multiple outputs, increased voltage ripple at the output, and single polarity operation. Chapter 4 describes the single polarity operation limitations in more detail and provides a novel control technique achieving double polarity operation with charge recycling.

2.5. Techniques for Increasing Power Efficiency

The main design challenge in switching converters is to develop a system which is flexible and efficient at the same time. To address this challenge, numerous works have been presented in the literature aiming to reduce the switching and resistive losses associated by the output stage switch transistors together with quiescent current and other losses.

A popular control mode for increasing the efficiency in low load currents is the *sleep mode* where the buck converter stops switching until required [23], as described in Section 2.1.3. Sleep mode reduces capacitive losses due to reduced switching activity. However, as the switching frequency deviates as a function of load current in this mode, electromagnetic interference (EMI) at particular switching frequencies can emerge, such as interference with

audio band or interference with display drivers, which can become a critical issue for portable applications.

Pulse frequency modulation (PFM) technique has been proposed for light load currents to improve power efficiency [24,25]. In this technique a variable switching frequency is utilized, where the switching frequency is regulated as a function of output load current to reduce capacitive losses at low load currents. Similarly, pulse skip modulation (PSM) is proposed [26] where the clock operates with fixed frequency but some clock pulses are skipped at low load currents. However, similar to sleep and PFM modes, the switching frequency is a function of output load current, thus these mentioned techniques show susceptibility to EMI induced issues.

A technique for partially charging the pass devices is described in [27], targeting to reduce the capacitive losses, but this technique is not preferred in industrial applications as the gates of the pass devices are left floating. The practical application for driving pass devices is with as low impedance as possible, explained in Section 3.3.7 in detail.

Resonant gate drivers utilizing an inductor for gate charge recycling of pass devices have been proposed to reduce capacitive losses [28,29]. The trade-offs of this technique are the need for external inductors for both pass devices and added design complexity to safely support gate switching voltage levels.

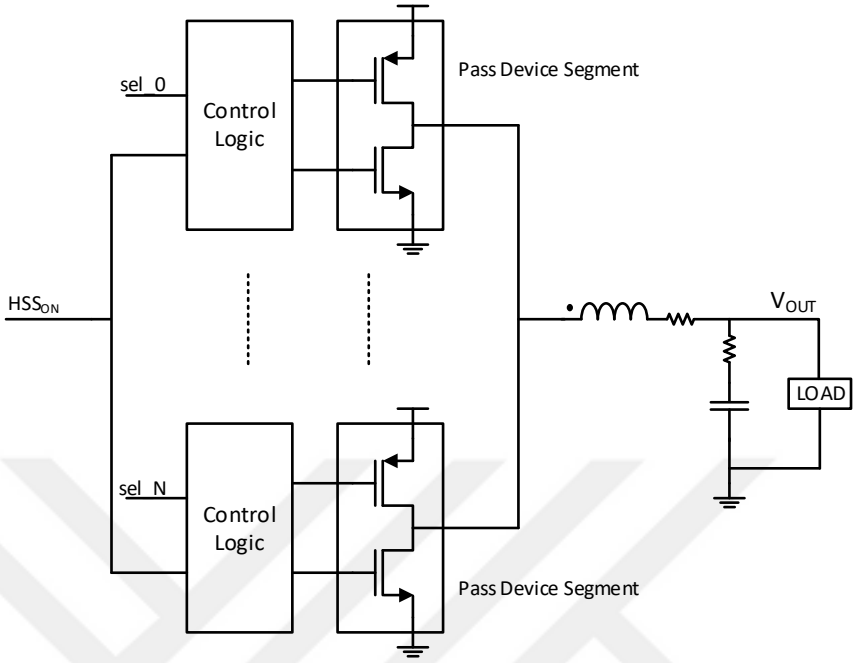


Figure 2.15. Switching converter with segmented pass devices.

Segmentation of pass devices are presented in [30-33] where portions of the pass device can be switched instead of the whole pass device, addressing the trade-off between gate capacitance losses and switch resistance. For instance, when a smaller portion of the pass device is switched, the resistive losses will be higher due to increased switch resistance, but the capacitive losses will be lower. Figure 2.15 gives a topology example for implementation of segmented pass devices: The output of PWM modulator (shown as HSS_{ON}) is distributed to control logic blocks together with a dedicated segment selection signal (shown as *sel_X*), hence each segment is driven by a separate control logic. Then, the outputs of pass device segments are joined to drive the inductor.

Conventional examples of segment selection methods determine the number of switching segments by monitoring the load current; in light-load conditions a smaller portion of the pass device is switched, and the full pass device is switched at high-load conditions [31,32].

One of the contributions of this work is an application of the segmented pass device technique, aiming to achieve optimum efficiency in any given and varying supply, load,

temperature, process, and aging conditions by adjusting the segmented pass device, such that the sum of capacitive and resistive power terms is minimized. Chapter 3 describes the principles of this novel technique together with an analytical approach, design implementation, and simulation results.

3. BUCK CONVERTER WITH ADAPTIVE PASS DEVICE

Adaptive pass device topologies can be utilized to increase the power efficiency of a switching converter. The core work of this thesis comprises a novel control technique to efficiently supply a wide range of output load current in a buck converter using an adaptive pass device at the output stage. The motivation of using this technique is to improve the power efficiency of a buck converter, as the proposed technique leads to optimum efficiency performance in any given load current, input supply voltage, temperature, process, and aging conditions, without the trade-offs of the mentioned efficiency improvement techniques.

The technique is based on power comparison of capacitive and resistive terms [4,5], carried out in analog domain, calculated by using a novel analog arithmetic function cell called the *adaptive* g_m stage [6]. The motivation of using analog arithmetic function cells is to reduce the power consumption of the converter. The additional current consumption introduced by the power calculation blocks is less than 1.4μA, which enables high efficiency system operation even at low load currents. The circuit and layout are implemented with a standard 130nm complementary metal–oxide–semiconductor (CMOS) technology and simulation results show 5% to 35% efficiency increase for mid/low load currents compared to a fixed output stage buck converter. Comparison with other reported adaptive pass device buck converters denote 4% increase in peak power efficiency with three times broader load current range.

This chapter is organized as follows: after an analytical investigation of efficiency loss mechanisms in a buck converter, Section 3.2 describes the adaptive pass device sizing technique, followed by design and system level implementation given in Section 3.3. Simulation results are presented in Section 3.4, showing power efficiency vs. load current plots for different input supply, process and temperature corners, transient and AC response, followed by conclusion.

Though the presented technique is described through the example of a buck converter, it can be applied to other switching converters where the trade-off between capacitive and resistive power losses exists.

3.1. Losses in a Buck Converter

Various power loss mechanisms exist in a buck converter as shown in Figure 3.1, usually classified as resistive losses, capacitive losses and other losses. Resistive power losses dominate at the high load current range, given by [16]:

$$P_R = I_L^2\, r + \frac{\Delta I_L^2}{12} r \tag{3.1}$$

where r is the equivalent lumped resistance in the load current path, the first term of the equation is due to the DC component of coil current, and the second term is due to the coil current ripple. Resistive losses occur due to switch resistance of pass devices, direct current resistance term (DCR) of the coil, and parasitics from the printed circuit board (PCB) traces and other external components in the inductor and load current path.

Capacitive losses dominate at low load current range and occur due to switching of pass devices and pass device drivers, given by [34]:

$$P_C = C\, f\, V_{DD}^2 \tag{3.2}$$

where f is the switching frequency of the buck converter, C is the equivalent switching capacitance including gate capacitance of the pass device, gate capacitance of the pass device drivers, parasitic capacitors due to chip layout and PCB traces, and V_{DD} is the input supply voltage of the power converter.

Other loss mechanisms include magnetic core losses in the coil [35], losses due to non-overlapping time duration of pass devices, pass device driver losses, and the quiescent current consumption of the buck converter. Even though these mechanisms cannot be

neglected in some particular applications, the efficiency loss is dominated by the resistive and switching losses introduced by the huge pass devices, for a typical buck converter driving amperes of output load current.

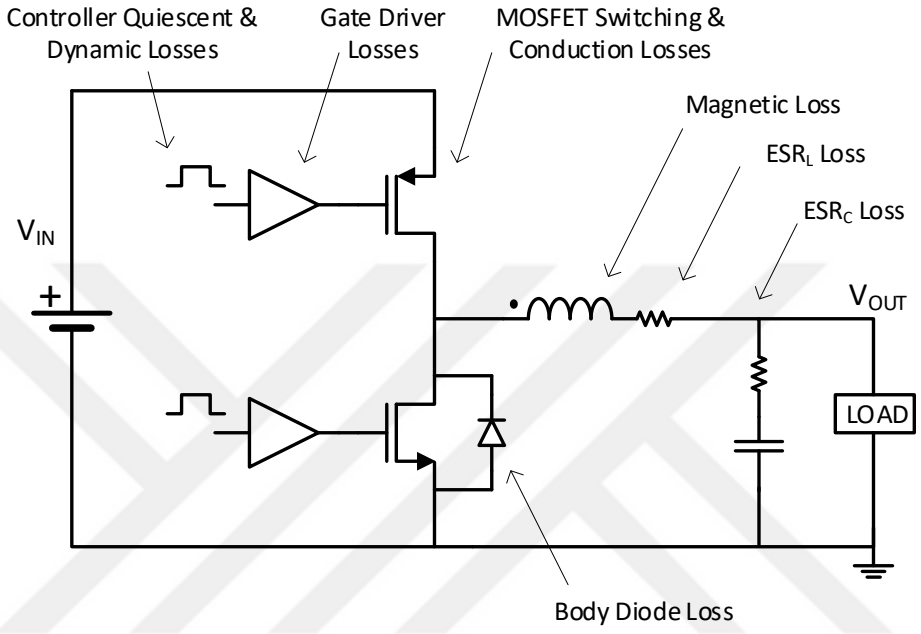


Figure 3.1. Mechanisms of power loss in a synchronous buck converter.

There is a trade-off between resistive and capacitive losses of a pass device. To minimize the resistive losses the width of the pass device has to be increased as much as possible – limited by the allowable layout area; conversely, to minimize the capacitive losses the width of the pass device should be minimized. The conventional solution in industrial applications is to optimize the width of the pass device such that the peak efficiency is achieved at 1/2 or 1/3 of the specified maximum load current. The mentioned trade-off can be overcome by introducing the segmented pass device technique, thus enabling to switch a smaller portion of the pass device, as described in the next section.

3.2. Adaptive Pass Device Technique

Referring back to Figure 2.15, Equations (3.1) and (3.2) related to the resistive and capacitive losses of a pass device can be adapted for a segmented pass device as follows:

Capacitive power loss of a segmented pass device, switching with frequency *f*, having a unit segment gate capacitance C_{gg}, and n_s being the number of selected segments can be expressed as:

$$P_C = n_s C_{gg} f V_{DD}^2 \tag{3.3}$$

Resistive power loss of a pass device, having a unit segment channel resistance r_{on}, with number of selected segments n_s, draining a total load current I_L and assuming first order approximation can be expressed as:

$$P_R = \frac{I_L^2 r_{on}}{n_s} \tag{3.4}$$

The proposed adaptive pass device technique will target minimum power loss by comparing capacitive and resistive losses and solving for the required number of switching segments (n_s) to achieve minimum power loss. As capacitive power loss is directly proportional to n_s (Equation (3.3)) and resistive power loss is inversely proportional to n_s (Equation (3.4)), it can be shown that the minimum power loss can be achieved at the point where capacitive loss is equal to resistive loss.

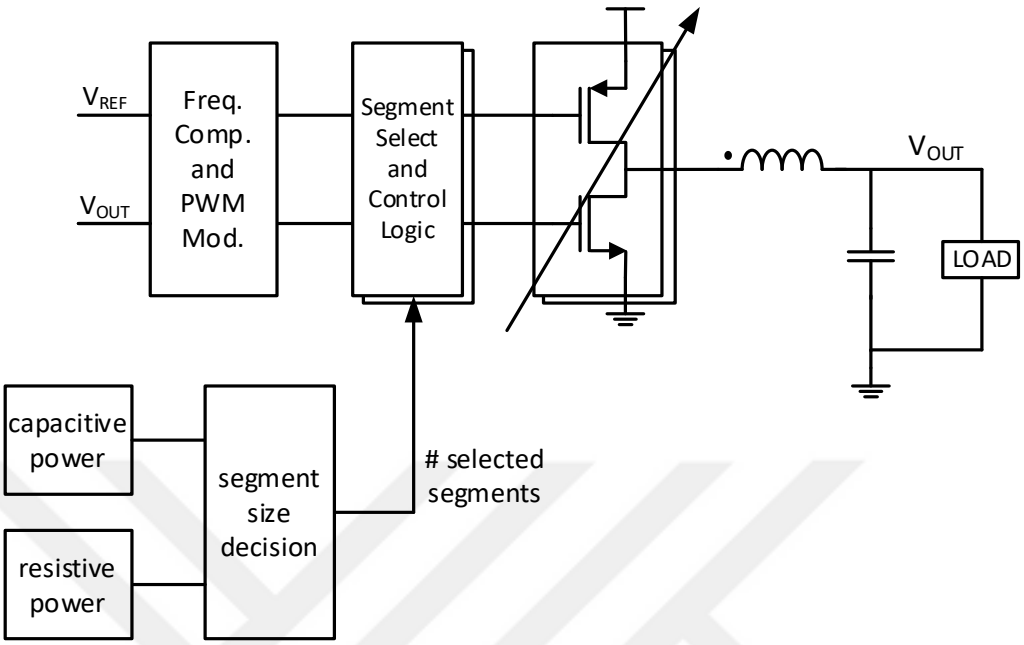


Figure 3.2. Block diagram of the proposed method.

Thus, the proposed system will increase the number of selected segments when the resistive loss is higher than the capacitive loss and decrease the number of selected segments when the capacitive loss is higher, to adaptively and continuously track the minimum power loss point as illustrated by Figure 3.2. This can analytically be expressed as Equations (3.5) and (3.6), where n_s is the number of selected switching segments:

$$P_C <> P_R \tag{3.5}$$

$$n_s C_{gg} f V_{DD}^2 <> \frac{I_L^2 r_{on}}{n_s} \tag{3.6}$$

One of the targets of the proposed technique is to solve the mentioned power loss comparison with analog circuit design techniques, to minimize additional power loss introduced by the segment size decision blocks. In order to solve Equation (3.6) with components and terms pertaining to analog circuit design (e.g. voltages and currents), first C_{gg} in Equation (3.6) will be replaced by a voltage V_c, utilizing a reference current I_R,

charging an identical pass device gate capacitor for a given time Δt, where $\Delta t=1/f$, and f is the PWM switching frequency.

$$V_c = \frac{I_R \Delta t}{C_{gg}} \tag{3.7}$$

Similarly, right side term of Equation (3.6) can be simplified by using a voltage term V_{sense}, which is actually the voltage drop on the unit pass device segment:

$$V_{sense} = \frac{I_L r_{on}}{n_s} \tag{3.8}$$

Thus, Equation (3.6) can be re-phrased without using resistor or capacitor terms as:

$$n_S \frac{I_R}{V_c} V_{DD}^2 <> I_L V_{sense} \tag{3.9}$$

Also noting that the total output current will equally be distributed between identical segments: $I_L = I_{seg} n_s$, the term n_s will cancel out in the equation:

$$\frac{I_R}{V_c} V_{DD}^2 <> I_{seg} V_{sense} \tag{3.10}$$

This equation can be interpreted as follows: if a unit pass device segment is operating with balanced capacitive/resistive power loss, then also the switching converter will be working with optimal efficiency.

As a final step, to simplify the quadratic term, both sides of the Equation (3.10) are divided with V_{DD}:

$$\frac{I_R V_{DD}}{V_c} <> \frac{I_{seg} V_{sense}}{V_{DD}} \tag{3.11}$$

Here both terms of the equation have the same form $I \times V/V$ to be directly processed by the proposed adaptive g_m block defined in Section 3.3.1.

3.3. Design of the proposed buck converter

This section describes the design implementation of a buck converter with proposed adaptive output stage technique. First the key design block for power comparison, the adaptive g_m block is described. The section proceeds with design details of other building blocks followed by system level implementation, performance specifications and the layout of the buck converter.

3.3.1. Adaptive g_m Stages

Various circuit topologies utilizing a feedback loop and self-bias to generate reference voltages and arithmetic functions have been proposed in the literature [36-38]. This section describes a novel arithmetic function cell with an inherent self-bias loop designed to compare the capacitive and resistive power terms expressed in Equation (3.11). Called the adaptive g_m cell, this block is designed to enable the comparison of capacitive and resistive terms by performing a simultaneous multiplication and division of three inputs: $I_1 \times V_1/V_2$ similar to the terms introduced in Equation (3.11). The outputs of the adaptive g_m blocks provide inputs to the segment size decision block shown in Figure 3.2 to find the optimum number of selected segments, e.g. by decreasing the number of selected segments if the capacitive power term is higher than the resistive term or by increasing the number of selected segments if the capacitive power term is lower than the resistive term. This block generates the core of power comparison, enabling optimal power efficiency for different input supply voltage, load current, temperature, process, and aging conditions. Without this block, e.g. by only providing load current information, the buck converter would not be tracking the supply voltage, temperature and process variations.

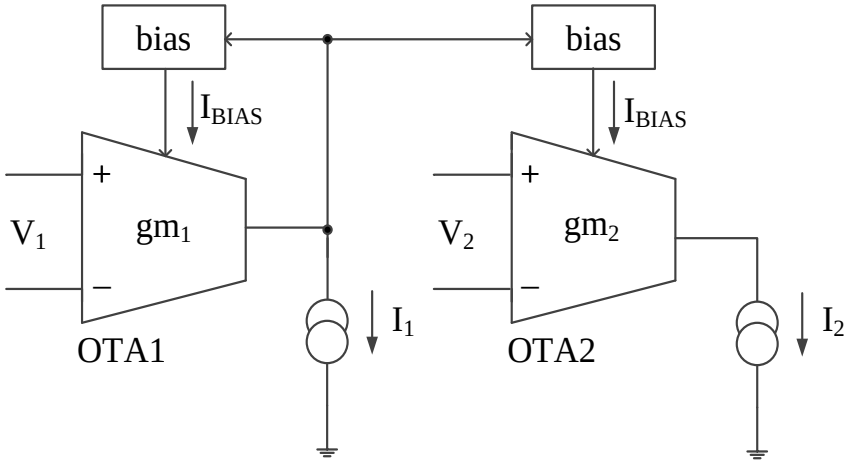


Figure 3.3. Adaptive g_m stage.

Figure 3.3 gives the operational block diagram of the adaptive g_m cell [6]. The topology is formed by using two Operational Transconductance Amplifiers (OTA) placed in a self-bias DC feedback loop.

The cell has three inputs V_1, V_2, and I_1; I_2 is the output current. *OTA1* and *OTA2* are two identical transconductance cells using same bias currents. *OTA1* has an input voltage of V_1 and sources the output current I_1. As *OTA1* input stage is formed by a differential pair stage, the transconductance of *OTA1* increases with its bias current. The self-bias feedback loop sets the bias current control voltage such that the output current of *OTA1* is equal to I_1. Thus, the conductance of *OTA1* is equal to:

$$g_{m1} = \frac{I_1}{V_1} \tag{3.12}$$

As *OTA2* uses the same topology with *OTA1* and using the same bias current, it will have an identical transconductance g_{m2}, where:

$$g_{m2} = g_{m1} = \frac{I_1}{V_1} \tag{3.13}$$

Thus, the output current of *OTA2* can be found as:

$$I_2 = V_2 \frac{I_1}{V_1} \tag{3.14}$$

which is equal to the multiplication of input current I_1 and input voltage V_2 and division by input voltage V_1.

The transistor level implementation of the block is given in Figure 3.4 [39]. *OTA1* and *OTA2* are implemented using symmetrical OTA topology biased by current mirrors M_{B1} and M_{B2}. The feedback loop is formed by sourcing the input current I_1 from the output of *OTA1* and connecting the output of *OTA1* to the gates of current mirrors M_{B1} & M_{B2}. By connecting this way, if the output current of *OTA1* is less than I_1, then the gate voltages of PMOS transistors M_{B1} & M_{B2} will decrease, leading an increase in bias currents and an increase in transconductance g_{m1} such that *OTA1* output is equal to I_1. The transconductance values will be set by sizing of input differential pairs M_{11}, M_{12}, M_{21}, M_{22} and their corresponding bias currents. Equations (3.12)-(3.14) will be valid as long as differential pairs and their bias are identical and the transistors are operating in saturation. To achieve the required input linearity range, long channel devices are used at input differential pairs M_{11}, M_{12}, M_{21} and M_{22}.

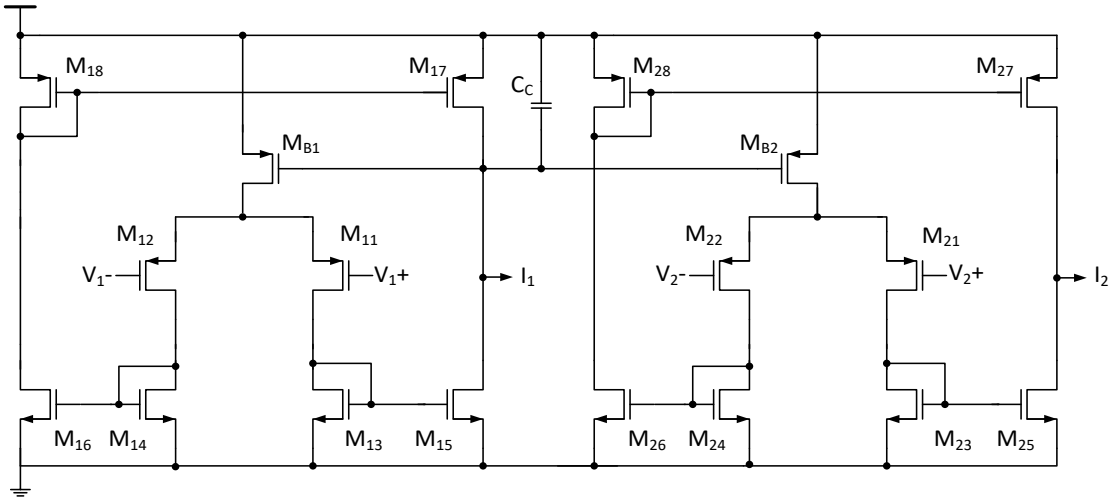


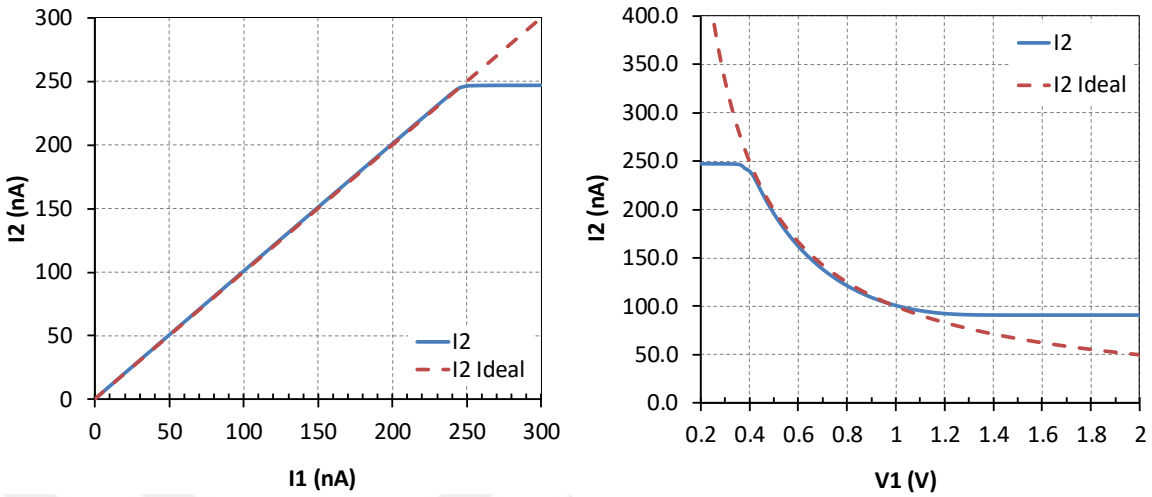
Figure 3.4. Schematic implementation of adaptive g_m cell [39].

There has been ongoing research on the stability of feedback loops with recently proposed novel compensation techniques [40,41]. As the output of *OTA1* is fed back to its bias, the adaptive g_m cell has an inherent feedback loop (shown in Figure 3.3). The frequency compensation technique used to stabilize the loop is to add a dominant pole by connecting a compensation capacitor C_C to the output of *OTA1* (shown in Figure 3.4), as this node is the high impedance node of the feedback loop.

The DC simulation results of adaptive g_m block is given in Figure 3.5: (a) I_2 vs. I_1 comparing with ideal calculation and (b) I_2 vs. V_1 and ideal calculation. For the input range of interest, output current I_2 is directly proportional to I_1 and inversely proportional to V_1 as given by Equations (3.12)-(3.14). At low values of V_1, the output current is limited by circuit output current sourcing capability. At high values of V_1 the output current saturates limited with the linearity range of input differential pair.

In typical operating conditions quiescent current consumption of a single adaptive-g_m stage from the supply is 0.66μA. This low power consumption will enable the system to perform power calculations without introducing noticeable efficiency loss even in low load conditions.

System level calculations determine 20% accuracy specification for the output current calculation of this block to achieve 0.1% efficiency error of the segment size decision block. Simulation results in Section 3.4 show that this condition is met in the overall PVT range of operation, together with the linearity range of the adaptive g_m stage. Owing to the symmetric OTA based topology, the circuit benefits from insensitivity to process, supply voltage, and temperature variations.



(a) (b)

Figure 3.5. Simulation results of adaptive transconductance cell
(a) I_2 vs. I_1, for V_1=V_2=1V (b) I_2 vs. V_1, for V_2=1V and I_1=100nA.

A replica of the circuit given in Figure 3.4 is used for generating the resistive power calculation term – the right side of Equation (3.11). As the input voltages V_{sense} and V_{DD} are referenced to input supply voltage, an NMOS input differential pair is preferred for the resistive power adaptive g_m, similarly using symmetrical OTA topology. The schematic of the replica circuit is given in Figure 3.6. The layout of both blocks with implementation details is given in Appendix A.1 [42].

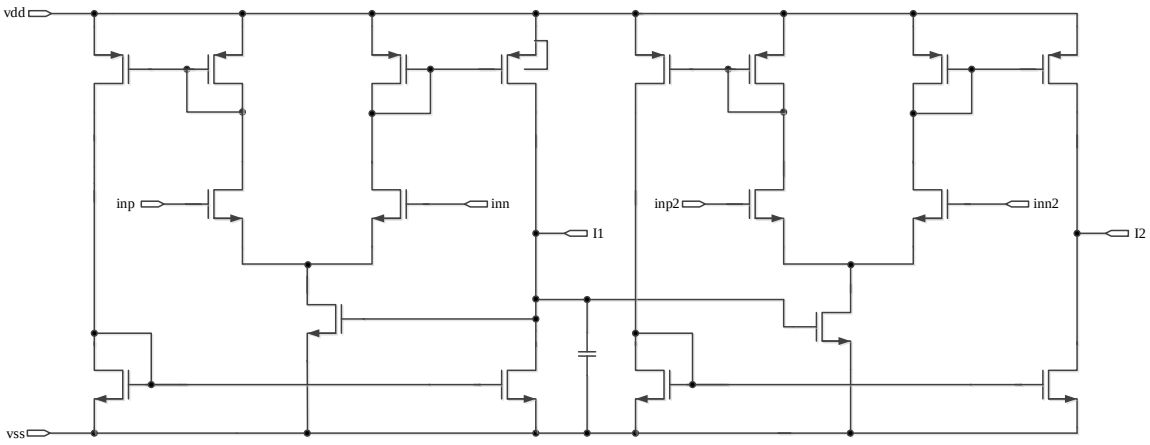
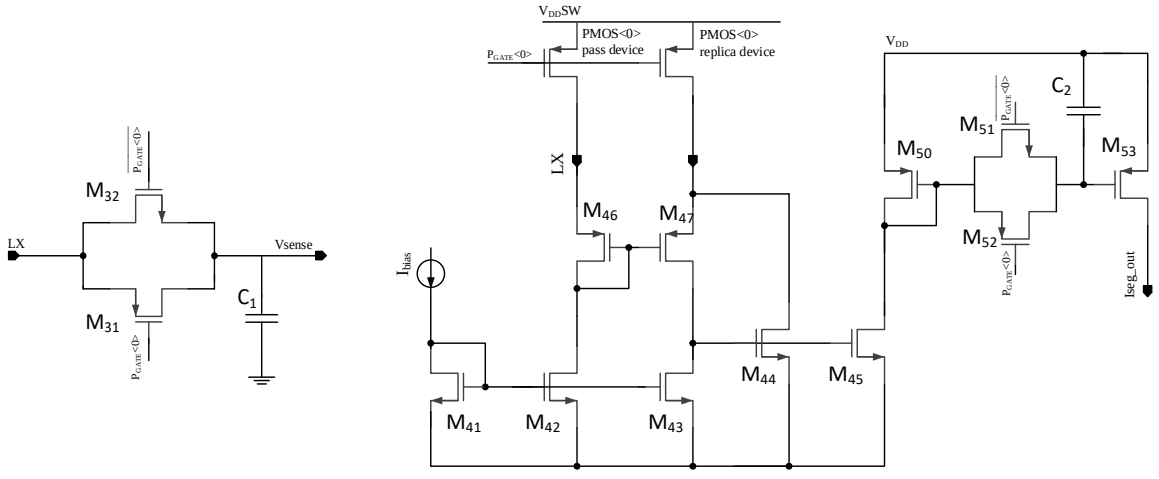


Figure 3.6. Schematic implementation of resistive term adaptive g_m cell [39].

3.3.2. Voltage and Current Sense

To evaluate the resistive power term (the right-hand side term of Equation (3.11)) V_{sense} and I_{seg} information is needed to provide an input to the adaptive g_m cell. V_{sense} is the voltage drop on the pass device during when the PMOS pass device is ON. Given in Figure 3.7(a), this voltage is simply generated by sampling the *LX* node voltage with a transmission gate, where the *LX* node is the drain node of the pass devices. The transmission gate will be ON during when the PMOS pass device is ON, shown in the figure with *PGATE<0>* signal. The capacitor C_1 stores the sampled voltage when the transmission gate is OFF.

I_{seg} is the drain current flowing through the unit pass device segment as defined in Equation (3.11). The current sense circuit topology is based on [43], replicating a ratio of PMOS pass device drain current, given in Figure 3.7(b). A feedback loop matches the drain voltages of the PMOS unit pass device and the replica device, as a consequence the drain current of the replica device is mirrored to provide a ratio of unit pass device drain current. The sensed current is mirrored and sampled with a transmission gate and a capacitor, to provide a continuous input to the adaptive g_m stage. The layout of the voltage sense block is given in Figure A.4. The current sense block is laid out together with the pass devices as the replica device needs to be physically located close to the pass device for good matching.



(a) (b)

Figure 3.7. Voltage sense (a) and current sense (b) blocks.

3.3.3. Error Amplifier

Targeting a voltage mode control application, the basic requirements of the error amplifier are high open loop gain with low quiescent current. System level specifications of the error amplifier are as follows: common mode input voltage V_{in} < 1.5V, open loop gain at DC > 60dB, 1σ input referred offset < 10mV, and I_{DDQ} < 10μA. The schematic design of the error amplifier is shown in Figure 3.8 [39]. It consists of a differential PMOS input stage together with a second gain stage. The compensation of the error amplifier and loop is done using Type-III compensation given with Section 3.3.7. The layout of the error amplifier is given in Figure A.5.

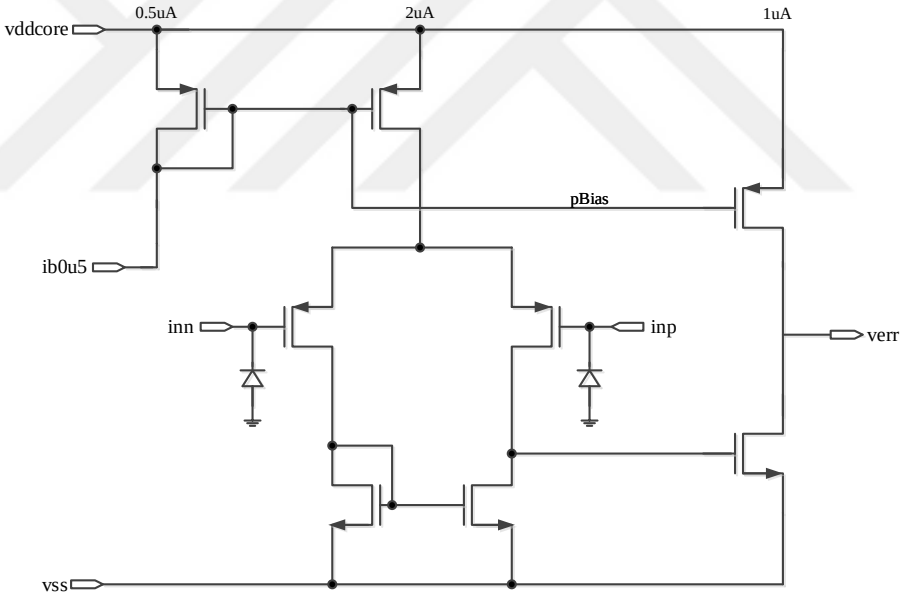


Figure 3.8. Schematic of error amplifier [39].

3.3.4. PWM Comparator

The PWM comparator is a latching comparator with less than 20ns propagation delay, less than 10mV 3σ input referred DC offset and less than 10μA quiescent current specifications. The comparator topology consists of two gain stages together with digital latching functionality. The latching function is required to prevent false triggering caused by

couplings induced by switching events. The latch is reset with each clock cycle. The schematic of the PWM comparator is given in Figure 3.9 [39] and the layout is given in Figure A.6 and Figure A.7 [42].

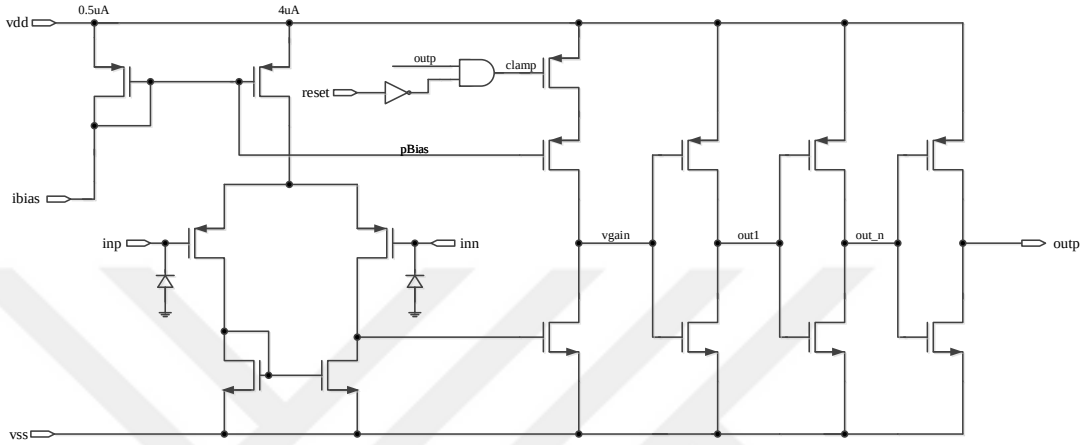


Figure 3.9. Schematic of the PWM comparator [39].

3.3.5. Ramp Generator

The ramp generator block generates the sawtooth signal necessary for PWM modulation in voltage control mode. The block level specifications include output voltage range between 100mV and 1.8V and trimmable ramp peak voltage. Switching frequency is 3MHz. The schematic design of the ramp generator is demonstrated in Figure 3.10 [39]. The working principle of the circuit is as follows: a reset input discharges the capacitor at the start of clock cycle; after reset is released, a bias current flowing to the capacitor ramps the capacitor voltage linearly, depending on the capacitance and the current. The capacitor voltage is replicated on a resistor through a current mirror; hence a linearly ramping output current is achieved. The ramp generator output is connected to a resistor at a higher schematic level, generating the *vRamp* voltage.

Trimmable ramp peak is generated by altering the bias current with a 3-bit current digital-analog-converter (DAC). The layout of the ramp generator is given in Figure A.8 [42].

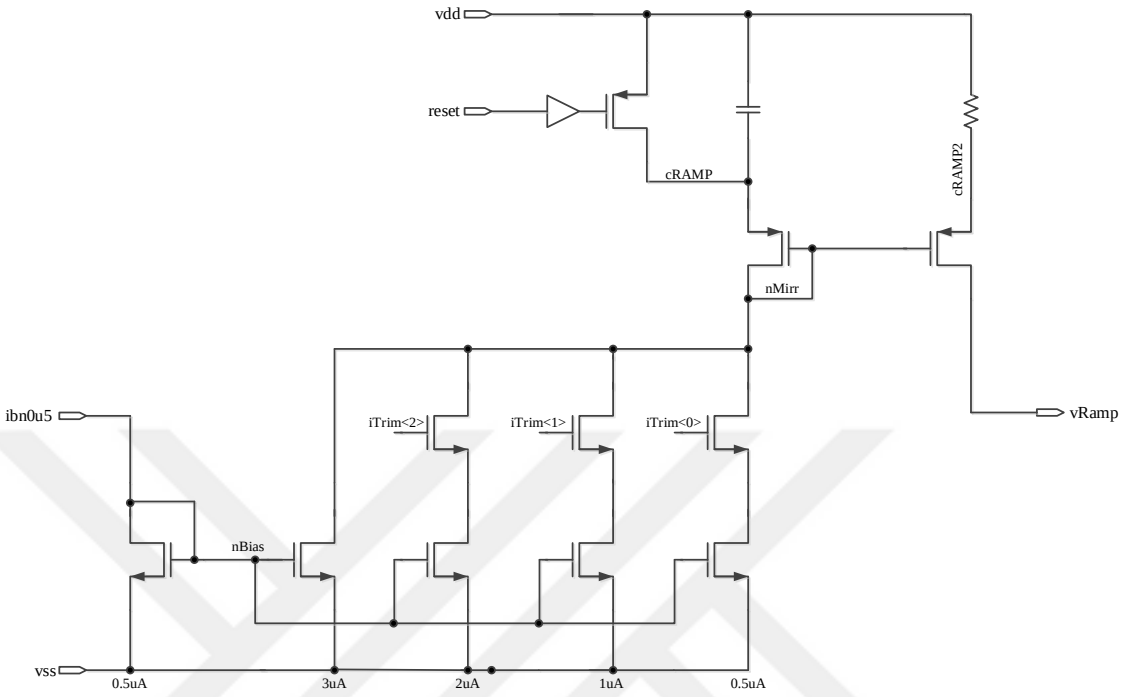


Figure 3.10. Schematic of the ramp generator [39].

3.3.6. Active Diode Comparator

After the HSS is OFF, LSS turns ON and the inductor current starts falling linearly with a negative slope. The active diode comparator (also called zero cross comparator – (ZXC)) detects the event that the inductor current crosses zero amperes and immediately turns OFF the LSS to prevent discharge of output capacitor of the buck converter – similar to the behavior of a diode element. This is done by monitoring the *LX* node voltage (the drain node of the pass devices) and comparing with zero volts. Block level specifications of the active diode comparator include ~0V input common mode voltage, typical propagation delay of 20ns, 3σ input referred offset voltage < 8mV trimmable input offset voltage, and I_{DDQ} < 10μA.

The trimmable input offset voltage is specified for correcting the input referred offset and to compensate for the comparator delay. Any delay in the comparator output will cause charge leakage from the output capacitor of the buck converter, resulting in efficiency loss.

A practical solution in reducing the comparator delay is introducing an intentional negative offset voltage at the input.

The schematic implementation is shown in Figure 3.11 [39]. A resistor string is used as a load for the first gain stage and at the same time allowing trimmable input offset voltage. NMOS switches serve to select different values of resistors with the option of creating positive and negative input offset. Replica NMOS switches are included in series with the resistor string to compensate for the switch resistance(s). The first stage output is followed by two gain stages, providing input to logic buffer cells.

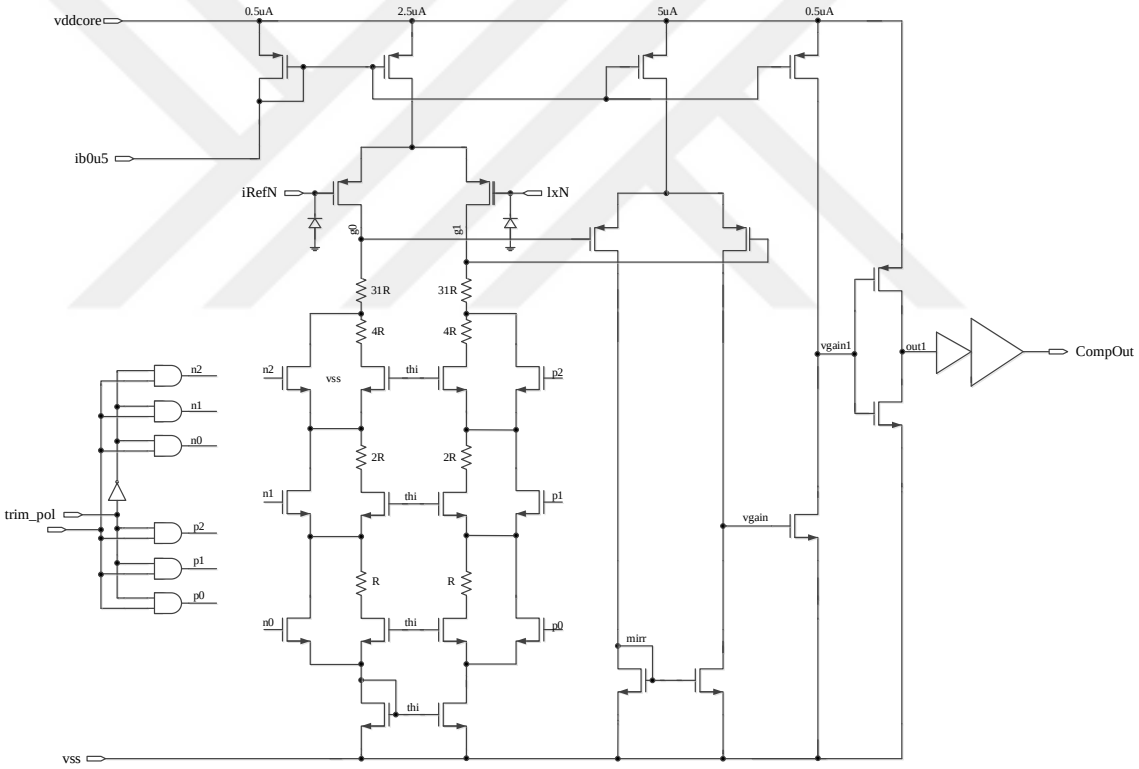


Figure 3.11. Schematic of active diode comparator [39].

3.3.7. Pre-Driver and Pass Devices

As pass devices are huge transistors switching amperes of current, special precautions need to be taken while driving the gates of the pass devices. One of the commonly implemented precautions in synchronous switching converters is “non-overlapping logic”, used to ensure a pass device is completely OFF before turning on the

other pass device. This precaution is necessary as if both pass devices are even partially ON (overlapped), amperes of short circuit current will flow from the input supply to ground. To prevent this short circuit current, a time duration when both switches are OFF (non-overlapped) is added to the switching sequence. During the non-overlapping time, the inductor current flows through the body diode of the LSS.

A trade-off of this technique exists as a long non-overlapping duration of both switches means loss in power efficiency due to body diode conduction losses – whereas a too short non-overlapping duration could lead to short circuit currents in different operating conditions. The technique implemented in this work is given in Figure 3.12, the logic gates between *nP* and *nN* nets provide a logic feedback loop ensuring a pass device is not turned ON until the gate of the other pass device is completely OFF. Various works for improved non-overlapping logic timing has been proposed, including loops for adaptively tracking input supply and process delay variations [44].

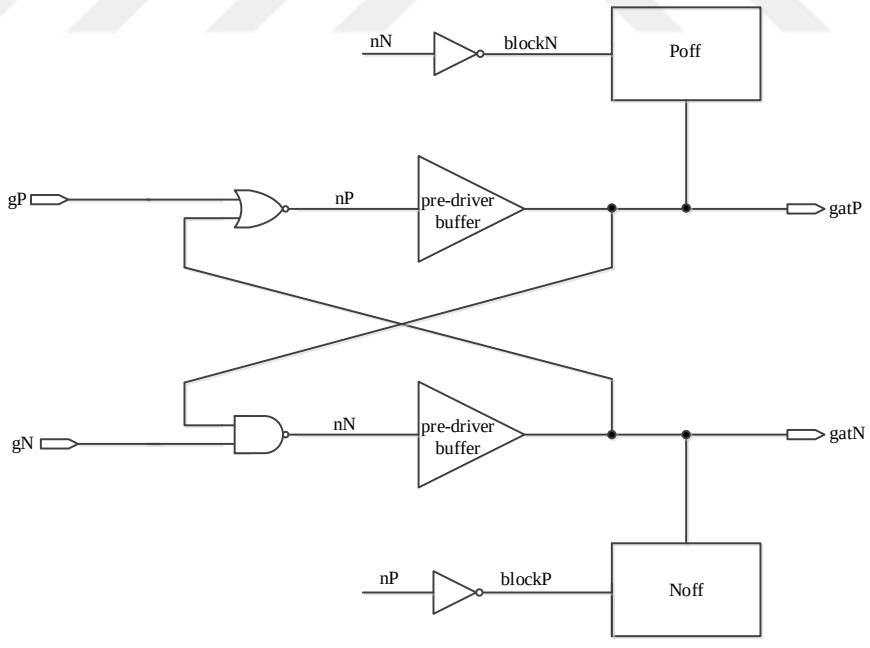


Figure 3.12. Schematic of unit pre-driver cell [39].

Another safety consideration in the pre-drivers is the *dv/dt induced turn-on phenomenon* [45]. As pass device gates are turned ON and OFF with high slew rates, and pass devices are connected with shared drains, charge injection from the C_{gd} of one pass

device to the gate of the other pass device might turn ON the other pass device, leading to a short circuit condition. *Poff* and *Noff* blocks shown in Figure 3.12 are connected in parallel with the pre-driver buffers to provide a short impedance path to the mentioned charge injection.

In top level implementation a pre-driver cell exists for each unit pass device cell. The layout of the pre-driver cell is given in Figure A.11 [42].

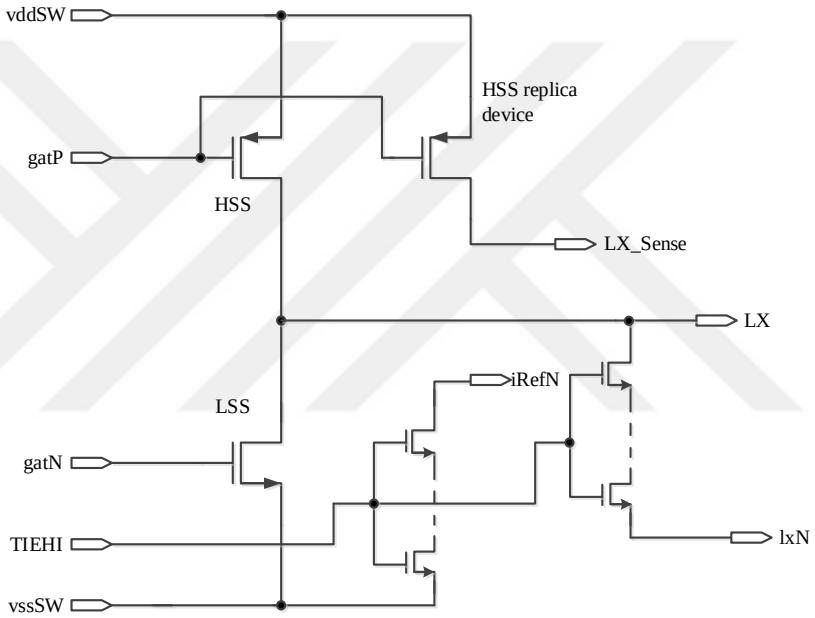


Figure 3.13. Schematic of unit pass device cell [39].

The schematic of a unit pass device cell is given in Figure 3.13 [39]. The PMOS driver (HSS) is sized by using efficiency curves of generic buck converters for the given process technology. The NMOS driver (LSS) transistor size is then calculated in compliance with the PMOS driver transistor's size. The unit pass device schematic also includes a small replica of the PMOS driver for current sense and a filtered replica of the *LX* node (*lxN*) providing an input to the active diode comparator.

3.3.8. System Level Implementation

System level implementation of the proposed switching converter topology is given in Figure 3.14. The topology is based on a voltage mode control buck converter [16], formed by a ramp generator, an error amplifier with Type-III compensation, a PWM comparator, and with a pass device segmented to 32 identical unit drivers, thus enabling logic control with 5 bits. The adaptive diode comparator providing the zero-cross signal for control logic is not shown for simplicity.

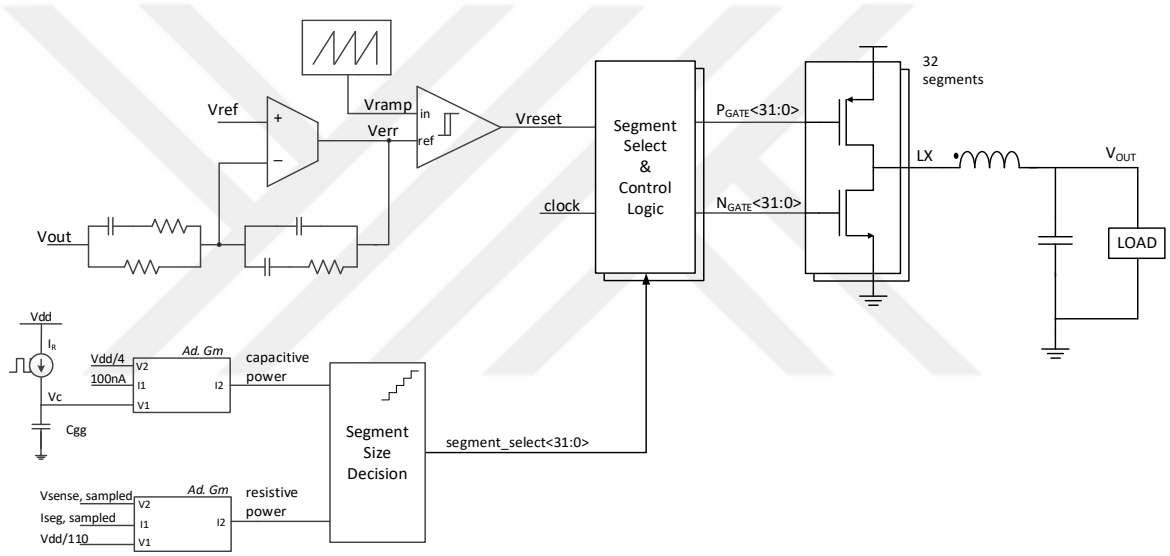


Figure 3.14. Block Diagram of the proposed method.

Two adaptive g_m blocks generate the capacitive power term and the resistive power term, where the inputs of the adaptive g_m blocks are as defined by Equation (3.11). The capacitive power term is generated by using three inputs: a V_c voltage formed on a PMOS capacitor - replicating the gate capacitance C_{gg} of the pass device as in Equation (3.7), a pulse current I_R and a portion of input supply voltage.

The resistive power term is generated by using the sampled V_{sense} voltage, the unit segment drain current I_{seg} as defined in Section 3.2 and a portion of input supply voltage set by the input linearity of the adaptive g_m block.

The segment size decision block includes a current comparator which compares the output currents of two adaptive g_m cells and increases or decreases the number of selected segments accordingly. Segment selection logic is updated with D-type flip flop cells clocked with the system clock to cast out any conflicts with the asynchronous control logic. This is to prevent a possible shoot-through between the unit driver stages.

Type-III frequency compensation is preferred in voltage mode buck converters to cancel the phase shift of the complex conjugate poles resulting from the output capacitor and inductor of the buck converter [46]. The frequency compensation of the buck converter in this work is implemented with a Type-III network formed by two pole/zero pairs generated by resistors R_1, R_2, R_3 and capacitors C_1, C_2, C_3 connected to the feedback node V_{OUT} at the left side of Figure 3.14 together with the error amplifier. Bode plots of the open loop system are given in Section 3.4.3.

Target specifications of the buck converter are given in Table 3.1. An SMD inductor TFM201610ALM is chosen for this switching converter, having 1μH inductance and 50mΩ DC resistance, with suitable size for portable applications (2.0×1.6×1.0 mm) [47].

Table 3.1. Buck converter specifications.

Technology	130nm
Input Voltage	2.8 – 4.8V
Output Voltage	1.0 V
Inductor / DCR	1μH / 50mΩ
Output Capacitor / ESR	22μF / 5mΩ
Switching Frequency	3MHz
Phase Margin	> 60°
Load Current	10mA - 1.5A
Efficiency	> 85%

The layout of the schematic has been implemented in a 130nm CMOS process, including block level details given in Appendix A [42]. Special precaution has been taken

for metal layers and a resistive 3-D extraction and analysis has been performed to ensure any unexpected resistive loss or electromigration will not occur [48]. Complete layout of the converter is given in Figure 3.15. The area of the adaptive output buck converter is 870μm×800μm, where the pass devices consume approximately 2/3rd of total layout area.

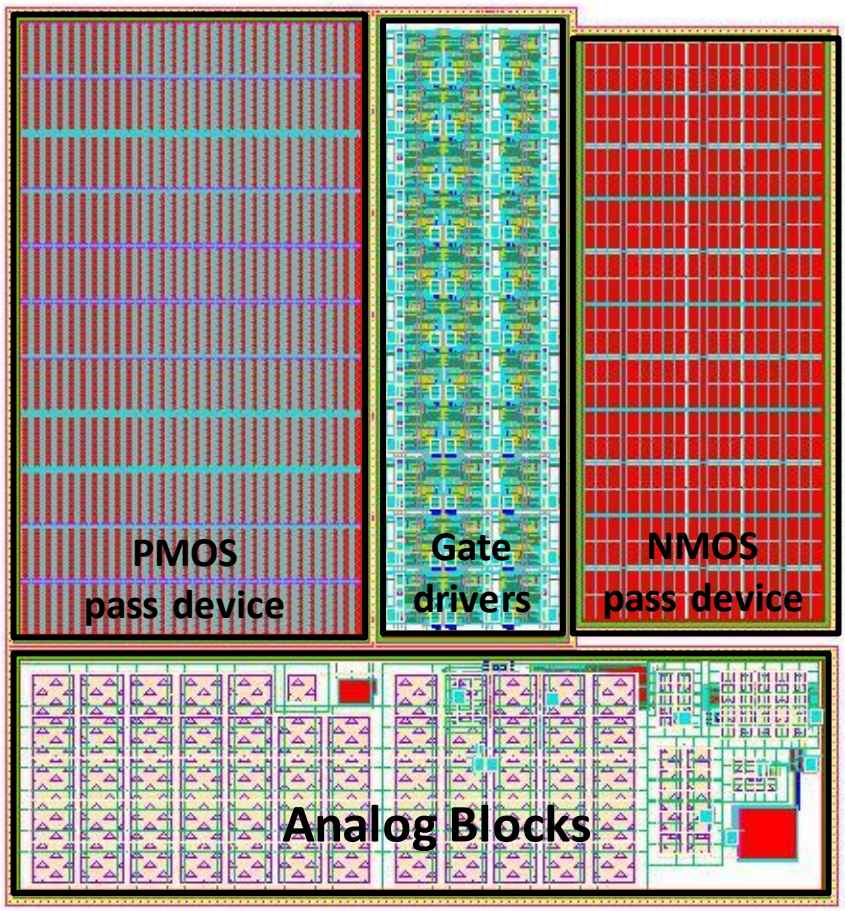


Figure 3.15. Layout of the buck converter with adaptive pass device [42].

3.4. Simulation Results

This section presents the simulation results of the buck converter with adaptive pass device. As power efficiency is the most important target specification of this work, Section 3.4.1 gives efficiency results vs. load current for different input supply voltage, process and operating temperature corners. This is followed by transient performance simulations given for line and load transient cases. Section 3.4.3 gives AC response and the associated setup

for performing AC simulations as switching converters need a linearized setup for small signal analysis. This section is concluded by comparison with similar works reported in the literature.

3.4.1. Efficiency Results

Figure 3.16 gives efficiency plots as a function of load current for different input supply voltage, process and operating temperature corners. Figure 3.16 (a) compares the efficiency of a fixed output stage buck converter and the buck converter with adaptive pass device vs load current. This plot shows the improvement achieved by the proposed adaptive output stage technique. More than 5% efficiency improvement is observed at typical 100mA output load and more than 35% efficiency improvement is observed at 10mA output load owing to reduced number of switching segments. It is observed that for low load currents the adaptive buck converter minimizes the number of selected switching segments, while the selected number of segments are increased with increasing load current, e.g. a larger pass device is used at higher load currents as decided by the segment size decision block, to reduce resistive losses, which is in line with Equation (3.4).

Capacitive power loss increases and resistive power loss decreases with input supply voltage. Figure 3.16(b) gives the efficiency plots for input supply voltage corners vs. load current. To achieve optimum efficiency response, it is observed that the segment decision block optimizes the number of selected segments for different input supply corners. At 100mA load and 2.8V input supply voltage, the segment decision block output indicates 13 pass device segments, however at 4.8V supply voltage the optimum number of selected pass device segments decreases to 5. This outcome is expected and is in line with Equation (3.3) as capacitive losses increase with increasing input supply voltage; fewer pass device segments are utilized to reduce capacitive losses at higher input supply voltages. The corner simulation results show more than two times change in optimum pass device size, marking the benefits of using an adaptive pass device.

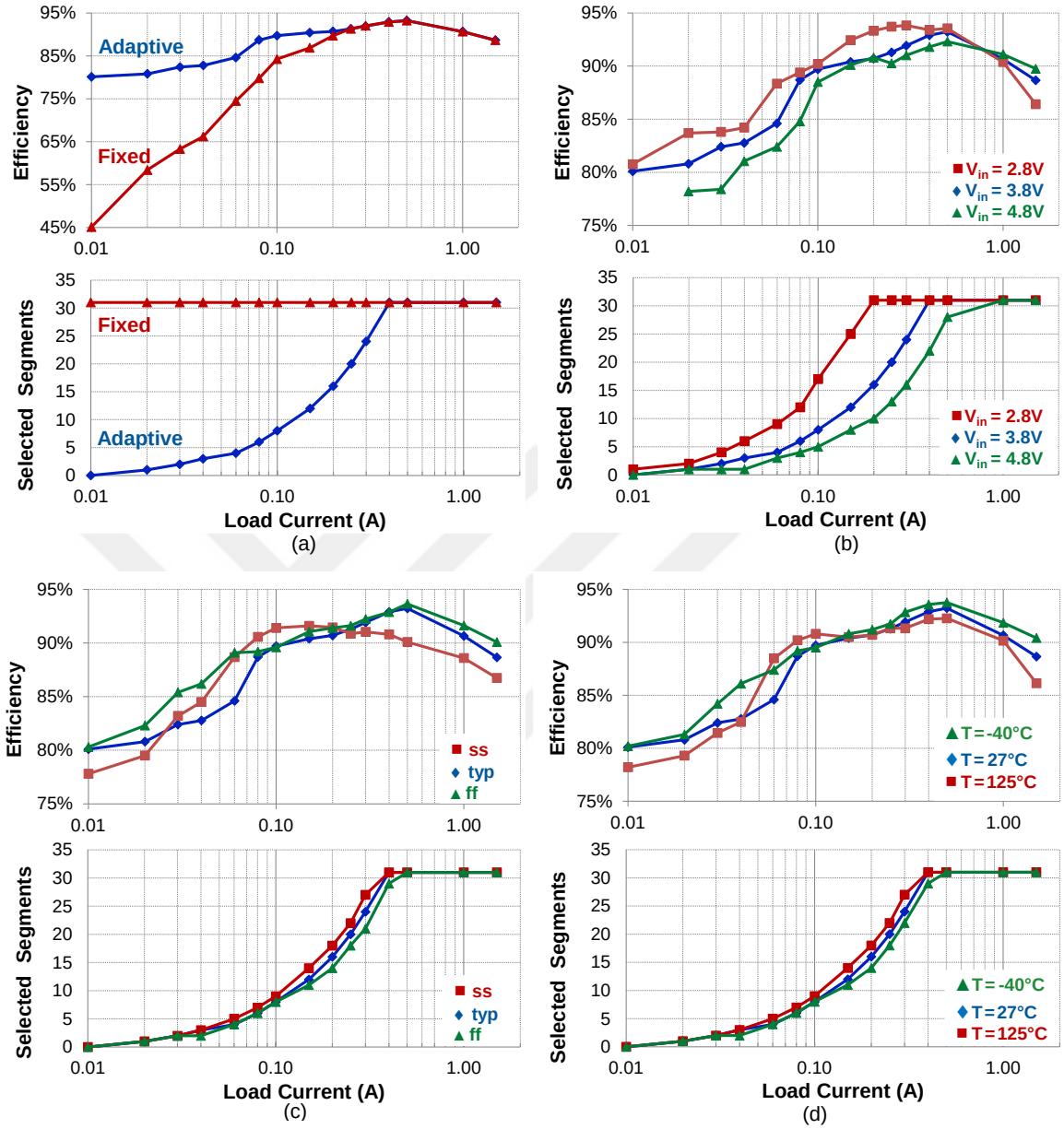


Figure 3.16. Efficiency plots for load sweep (a) comparison with fixed output stage (b) comparison for different input supply voltages (c) comparison for different process corners (d) comparison for different temperatures.

Figure 3.16(c) gives efficiency comparison for different process technology corners, showing the system response to different process conditions. For active device ss (slow NMOS - slow PMOS) process corner, the r_{on} of the pass device will be higher than nominal, leading to an increase in resistive losses. This will be compensated by the segment size decision block by increasing the selected number of switching segments. At 300mA load

and typical process technology parameters, the observed switching pass device segments is 24; however, for the same load current and ss process corner, the selected pass device segments increase to 27. Expected behavior is observed for ff (fast NMOS-fast PMOS) corner, where the switching pass device segments reduce to 21.

Efficiency comparison for different operating temperature corners is given in Figure 3.16(d). Increasing operating temperature leads to decrease in carrier mobility thus increase in resistive losses. Similar to previously given results, this increase is compensated by the segment size decision block by increasing the selected number of segments. At 300mA load and 27°C, the optimum number of selected pass device segments is 24, however for the same load current and high temperature corner 125°C, the optimum number of selected pass device segments increases to 27.

3.4.2. Transient Response

Transient response of this work is characterized by line sweep and load transient simulations. Line sweep simulation results are given in Figure 3.17, sweeping input supply voltage from 2.8 to 4.8V in 500μs with 300mA fixed output load. It is observed that with increasing input supply voltage (top brown trace), the capacitive power term increases linearly (bottom dotted red trace). The resistive power term decreases (bottom blue trace) with increasing input supply, with the segment size decision block decreasing the number of switching segments (green trace) to match resistive losses with capacitive losses, the current flowing per segment increases and a step increase in resistive losses is observed. Overall, the equalized capacitive power loss and resistive power loss terms per unit segment with no unexpected ringing or transients are observed in line with Equation (3.4) and Figure 3.16(b).

Load transient simulation results for a 1A load step at typical conditions is given in Figure 3.18. The capacitive power term stays constant as the input supply voltage, process conditions and clock frequency are constant (Equation (3.3)). The resistive power term increases with higher load current, limited by the output slew of the adaptive g_m stage. Here, in order to improve load transient results, to speed up segment size decision circuit, an output voltage comparator – V_{UNDER} *comparator* is utilized. This comparator senses dropping output

voltage and forces two times increase in selected number of segments per each segment decision clock, to help quickly increase the selected number of segments and improve the output voltage transient. Simulation results show 35mV drop at output for 1A load transient with 1A/μs slew at 1V output which is acceptable for portable applications.

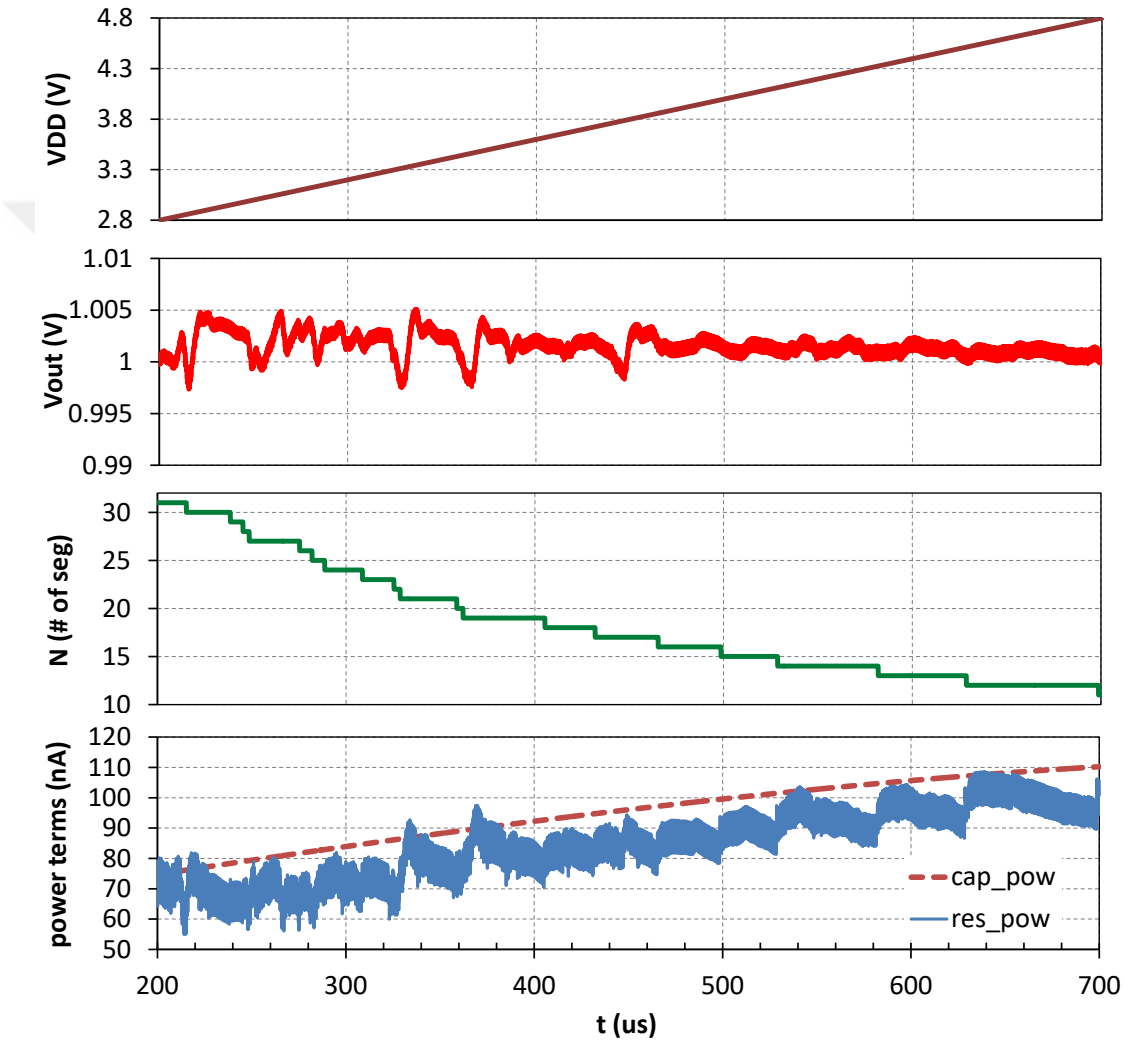


Figure 3.17. Line Sweep Simulation Results.

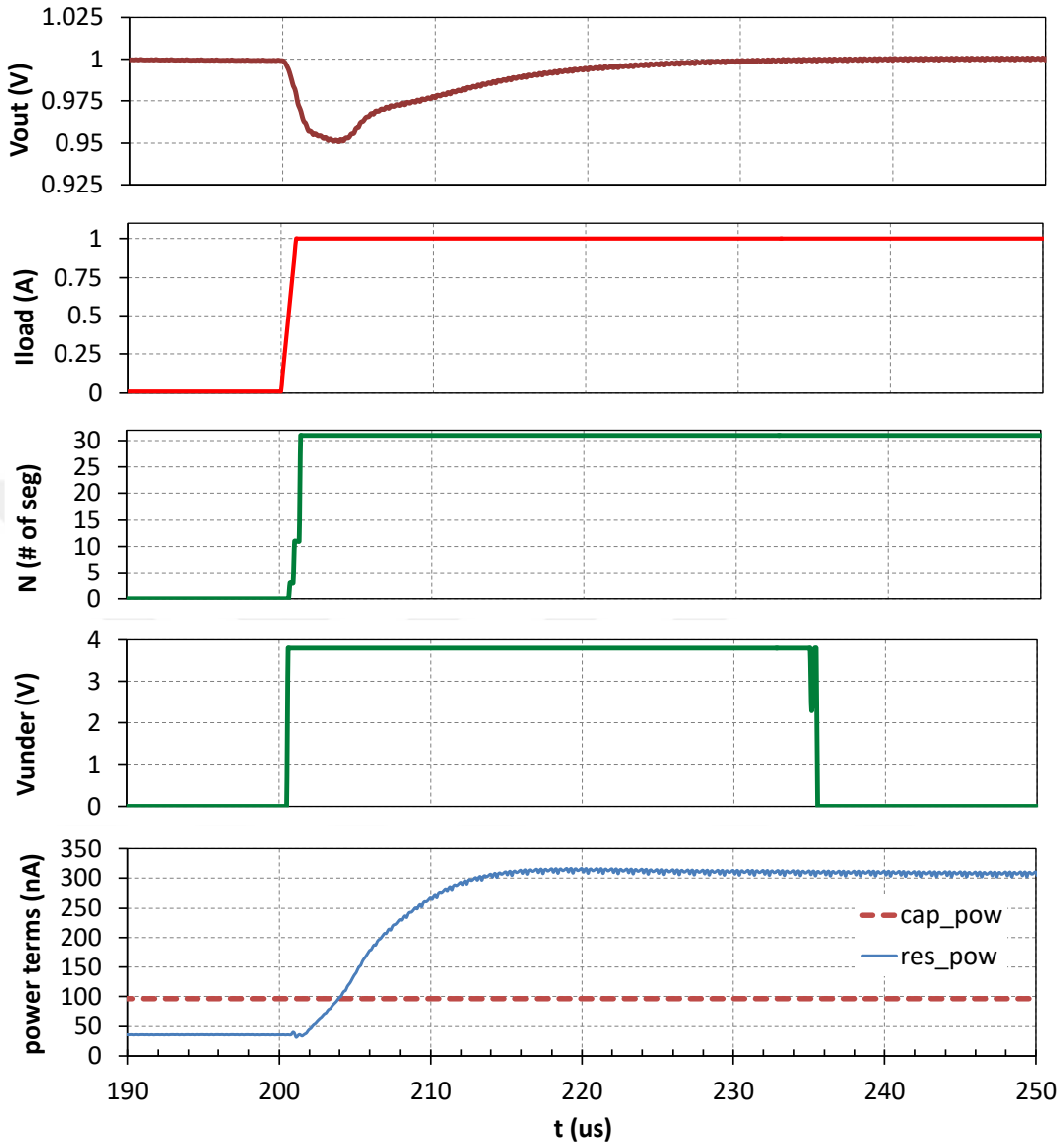


Figure 3.18. Load Transient Simulation Results.

3.4.3. AC Response

As the adaptive buck converter inherently employs a feedback loop for setting the output voltage to the target voltage, ensuring the stability of the converter is a design concern, especially considering the complex conjugate poles formed at the output due to the inductor and the load capacitor. However, small signal analysis of switching converters need additional pre-processing which utilize linearized models of switching blocks.

Therefore, a simulation setup with linearized switching components was generated also including a linearized model for the adaptive pass device. The model originates from [49] and was modified to take into account the change of output resistance as a function of the selected number of segments. The small signal simulation setup including the error amplifier, frequency compensation network, the linearized model of the adaptive pass device, and the load is given in Figure 3.19.

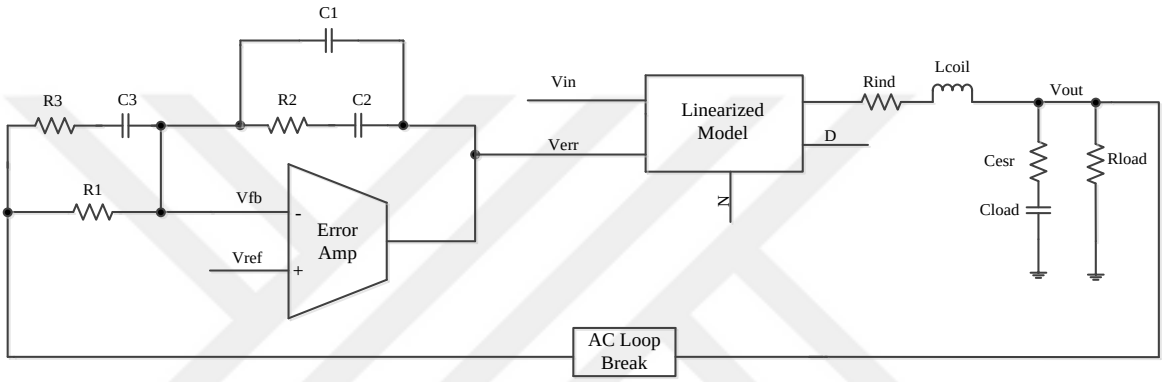


Figure 3.19. Linearized model for the adaptive pass device buck converter.

AC simulations using the linearized model are given in Figure 3.20. Under typical operating conditions, it is observed that the loop gain crosses 0dB at 125kHz, phase margin is 66.3°, and gain margin is 23.8dB which meet the stability specifications with a decent margin.

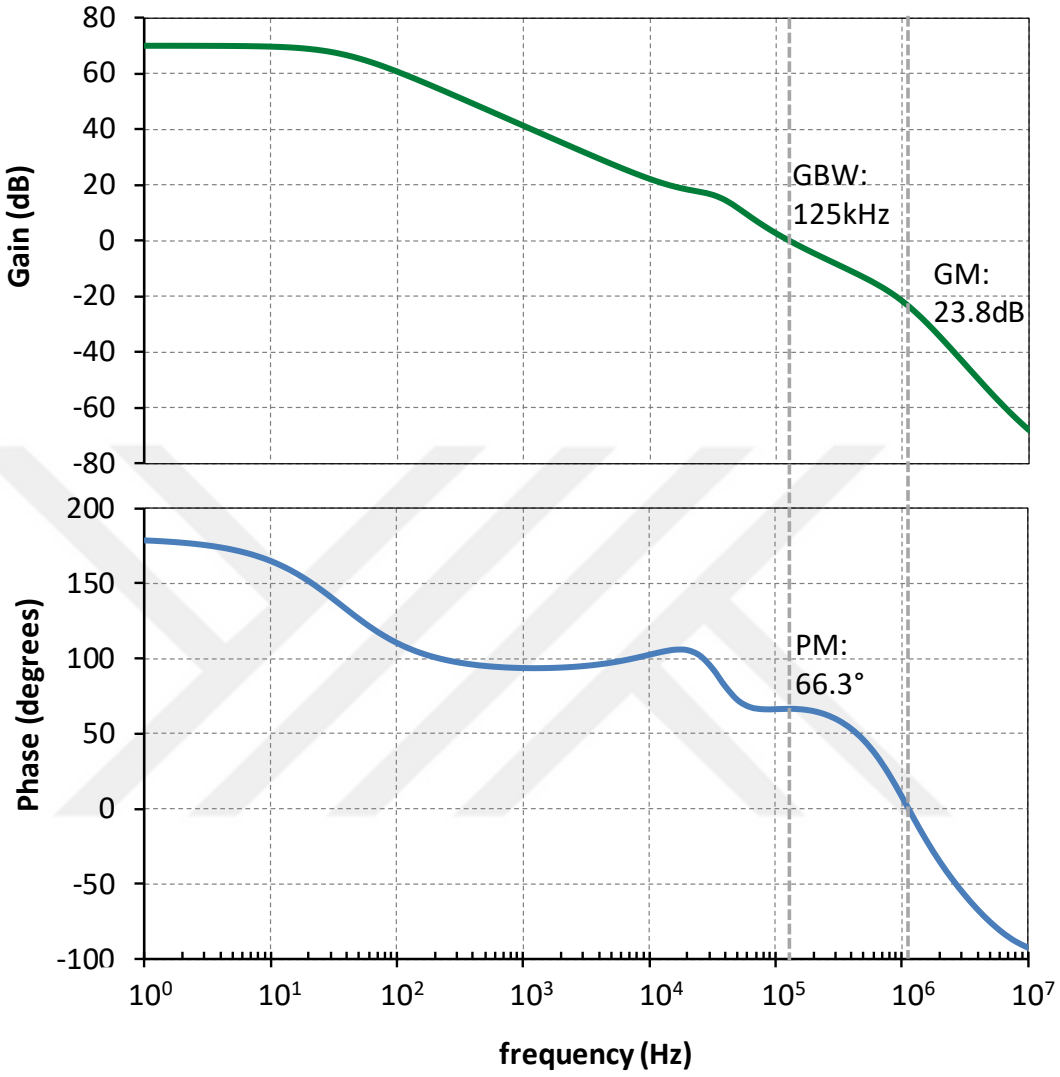


Figure 3.20. AC simulation results

3.4.4. Performance Comparison

In order to validate the performance improvements of the proposed technique, a comparison table with other buck converters using segmented output stage is given in Table 3.2. In PWM mode, the presented output load current range 10mA – 1.5A is wider than all mentioned articles, thus alleviating the use of sleep mode. Overall, this work achieves higher power efficiency values for PWM mode switching, considering both peak efficiency and minimum efficiency for different values of the load current. The external inductor and

capacitor values and switching frequency are in a similar range with other works thus allowing fair comparison.

Table 3.2. Performance comparison.

	This work	[31]	[50]	[51]	[52]	[53]	[54]	[55]
Inductor	1µH	0.1µH	1µH	2µH	N/A	400nH	N/A	N/A
Capacitor	22µF	30nF	4uF	4uF	N/A	0.9uF	N/A	N/A
Input Voltage	3.8V	5V	2.7V	3.6V	3.3V	2.5V	3.3V	3.3V
Output Voltage	1.0V	2.5V	1.8V	1.8V	1.8V	1V	1.2V	1.2V
Switching Freq.	3MHz	10MHz	4MHz	4MHz	1.2MHz	10MHz	2MHz	2MHz
I_{LOAD} (in PWM)	10mA – 1.5A	20mA – 80mA	15mA – 500mA	20mA – 200mA	10mA – 200mA	15mA – 500mA	10mA – 1A	15mA – 800mA
Min PWM Efficiency	80%	40%	74%	75%	35%	72%	60%	79%
Peak Efficiency	93%	60%	89%	89%	88%	83%	88%	87%
Process Technology	0.13µm	1.5µm	0.6µm	0.6µm	0.5µm	0.13µm	0.13µm	0.13µm

3.5. Conclusion

In this chapter, a novel technique to improve the efficiency of a buck converter using an adaptive pass device is presented. The proposed technique achieves optimum efficiency in any given and varying input supply voltage, load current, operating temperature, process technology, and aging conditions by adjusting the number of selected switching segments such that the total loss introduced by capacitive and resistive power terms are minimized, where the power terms are calculated employing a novel analog arithmetic function cell called the adaptive g_m stage.

The simplicity of the analog power loss equalization technique and the low quiescent current consumption of the adaptive g_m stage lead to high power efficiency even with low load currents. Maintaining PWM mode, the adaptive buck converter can supply load current range from 10mA to 1.5A, achieves 93% peak efficiency in typical operating conditions and 80% minimum power efficiency at low load currents. Compared to a buck converter with fixed output stage, a 5% efficiency increase in mid load current values and 35% efficiency increase in low load current values are observed. Comparison with other reported segmented pass device buck converters show higher power efficiency values for PWM mode switching considering both peak and minimum efficiencies, with 3 times broader load current range. Thus, the proposed technique steps out as an alternative solution to sleep mode and as an improvement to conventionally used segmented stage topologies in the low/mid load region.

4. SIDO BUCK CONVERTER WITH CHARGE RECYCLING

A topology limitation in conventional SIDO/SIMO bucks is that, it can only supply output currents with the same polarity to all outputs. As described in Section 2.4, assuming a positive inductor current is flowing to the outputs, the switching converter will not be able to reduce the output voltages if an overshoot happens in one of the outputs or a negative DVC is requested.

Similar to single output buck converters, negative current and DVC function capabilities are also requested in SIDO/SIMO buck converters thus having the functionality to supply opposite polarity current to its outputs. The straightforward solution to this problem (supplying positive output current to one output while discharging the other output) is to use a pulldown switch for discharging. When an overshoot event occurs or a negative DVC event is requested, the pulldown switch discharges the output capacitor to the requested voltage level, however, the major drawback of this solution is efficiency loss. In inductive switching converters, it is preferred to preserve charge by continued usage of the inductor, thus achieving high power efficiency.

This section describes a novel technique aiming to solve this limitation by using additional switches, making it possible to supply a negative current to one of the outputs while supplying a positive current to the other output(s). Even though the technique describes a new topology through the example of a SIDO buck converter, the concepts can be applicable to other switching converters.

4.1. SIDO Buck with Negative Current

Figure 4.1 describes the proposed SIDO converter switch topology [7]. Switch S_B is the buck high side switch. The diode (located below S_B) is usually implemented as a switch, allowing current in a single direction. S_{Y0} and S_{Y1} are the SIDO buck switches supplying current to outputs V_{OUT0} and V_{OUT1}. S_{X0}, S_{X1} and S_Z are the additional switches (novel)

allowing to supply complementary current to outputs - having both positive and negative polarity. During physical implementation, the switches S_{X0}, S_{X1} and S_Z can be designed smaller in size (relative to the other pass device switches), the design trade-off here is silicon area vs. efficiency in negative operation.

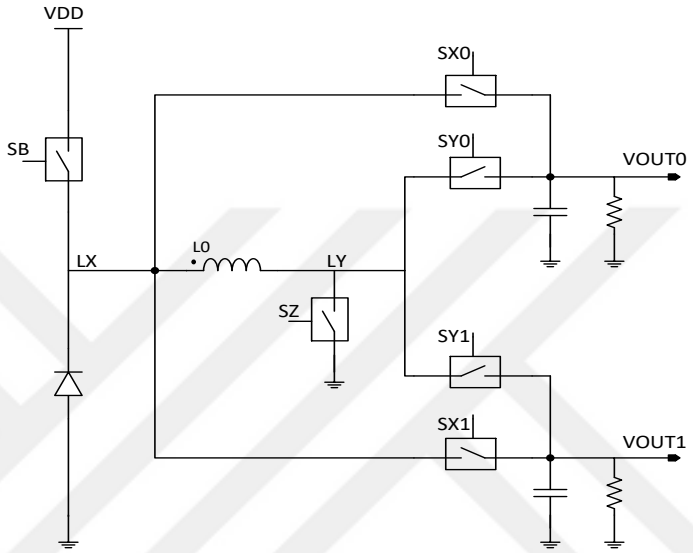


Figure 4.1. Proposed SIDO converter switch topology.

During typical SIDO operation, switches S_{X0}, S_{X1} and S_Z will be off. For the case where V_{OUT0} is supplying a positive load current (normal operation) and V_{OUT1} is requested to perform negative current operation, the switches will enable two different operation solutions as described in the following sections.

4.1.1. Negative SIDO Operation – Option 1

Figure 4.2 gives a bipolar operation example. In phase (a), which is typical SIDO operation, positive current is being sourced to V_{OUT0}. S_{Y0} is ON, S_{Y1} is OFF, S_B is performing buck switching, S_{X0}, S_{X1} and S_Z are OFF. Figure 4.2 phase (b) describes negative operation, where current flows from V_{OUT1} to ground. S_{Y0} and S_{Y1} are OFF, S_B is OFF, S_{X0} is OFF, S_{X1} and S_Z are ON. S_{X1} and S_Z enable current sink operation from V_{OUT1}, while maintaining positive current flow at the inductor L_0.

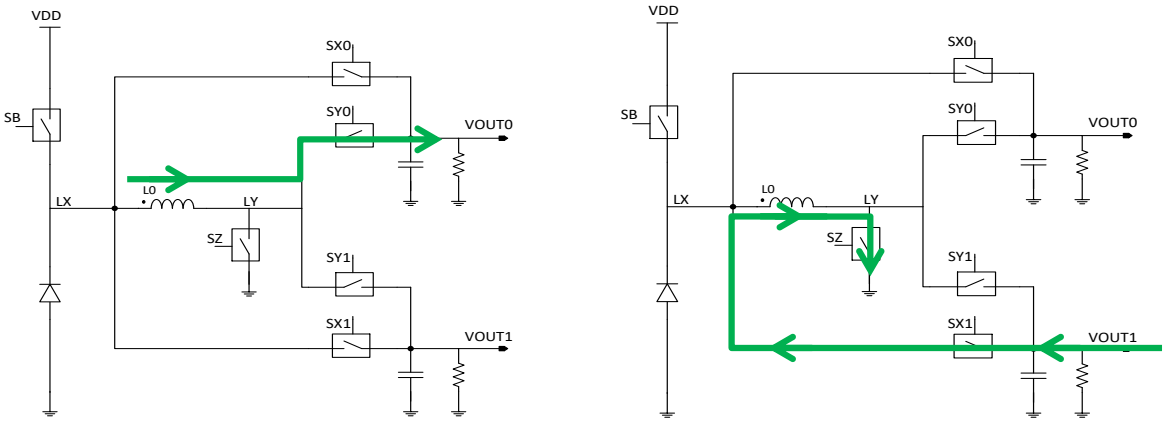


Figure 4.2. (a) Positive operation to V_{OUT0} (b) Negative operation to V_{OUT1}.

4.1.2. Negative Operation – Option 2

Figure 4.3 gives an alternative solution, with more power efficiency at high load currents. In phase (a) –similar to Figure 4.2-, positive current is being supplied to V_{OUT0} (normal operation). S_{Y0} is ON, S_{Y1} is OFF, S_B is performing buck switching, S_{X0}, S_{X1} and S_Z are OFF. In phase (b), negative current is being supplied to V_{OUT1} while at the same time providing a positive output current to V_{OUT0}. S_{X1} and S_{Y0} are on, S_{X0}, S_{Y1}, S_B and S_Z are off. In this switch configuration S_{X1} and S_{Y0} enable current flow from V_{OUT1} to V_{OUT0} through $L_{0,}$ maintaining a positive current flow at the inductor.

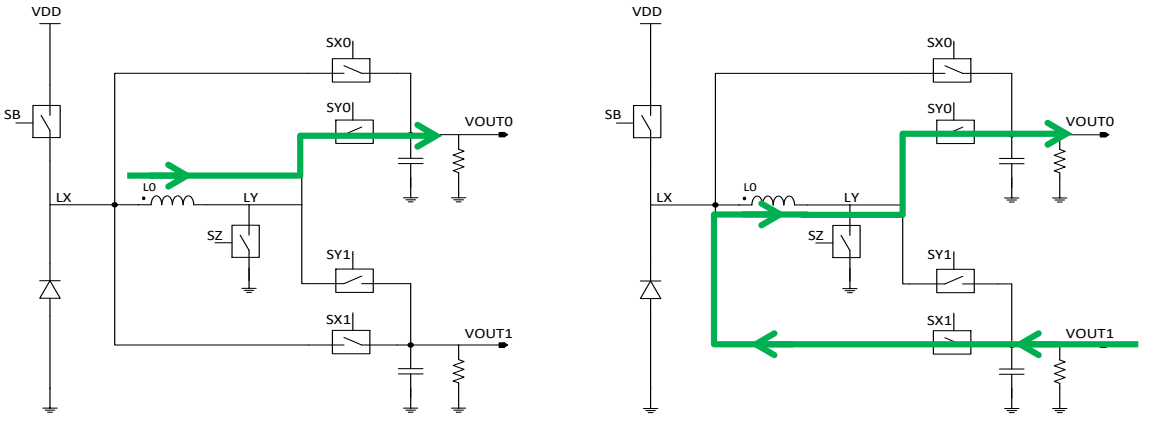


Figure 4.3. (a) Positive operation to V_{OUT0} (b) Negative operation to V_{OUT1}.

The advantage of this operation is that, the excess voltage in V_{OUT1} is used to supply load current to V_{OUT0} – not using any supply current, recycling stored energy in load capacitors. This advantage is expected to increase power efficiency in this operation mode and improve output voltage ripple (both outputs are being supplied at the same time – in normal SIDO operation only one output is supplied at a given phase). This mode might not be preferred when V_{OUT0} is in sleep mode (e.g. there is no load current at V_{OUT0}) since increasing V_{OUT0} could result in an over voltage (VOVER) condition. This mode also might not be preferred when V_{OUT0} is higher than V_{OUT1} and coil current is not high; in this condition, coil current will decay to zero and this mode will not be advantageous. In such conditions Option 1 described in Section 4.1.1 can be preferred over this solution.

4.2. Block Level Implementation

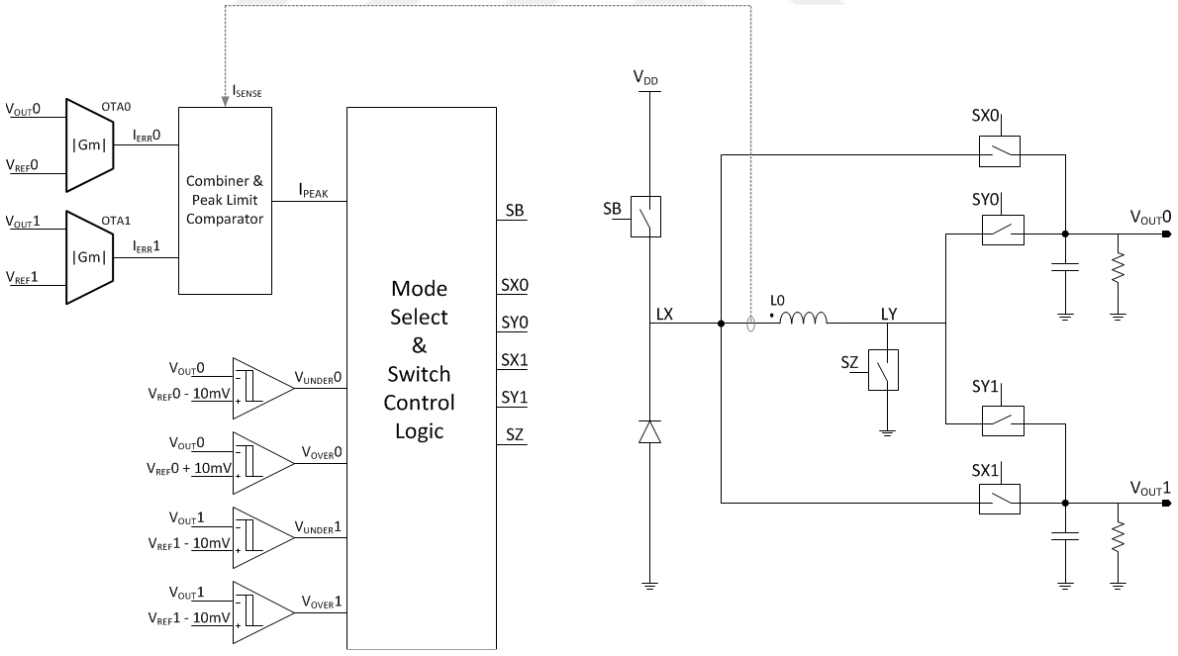


Figure 4.4. Block level implementation.

Figure 4.4 gives the block level implementation of the described topology. OTA_0 and OTA_1 generate error currents I_{ERR0} and I_{ERR1} which provide inputs to combiner and peak limit comparator. Using current mode control, peak limit will be a function of I_{ERR0} and I_{ERR1} added together with other compensation factors.

OTA_0 and OTA_1 provide the absolute value of error current as output, e.g. the error current will always be positive even if there is an undershoot or an overshoot. (without using absolute value, an overshoot in one output could be cancelled with an undershoot in the other output, resulting in no response of the system). Negative operation decision will be given by V_{UNDER} and V_{OVER} comparators. System operation will further be explained through the simulation results provided in the next section.

4.3. Simulation Results

In the following simulation results, switches S_{X0}, S_{X1}, S_{Y0} and S_{Y1} change logic positions synchronous with the clock. Though this is not a requirement of the proposed topology; this assumption helps building the macromodel in a more systematic way and enables to follow control signal transitions discretely.

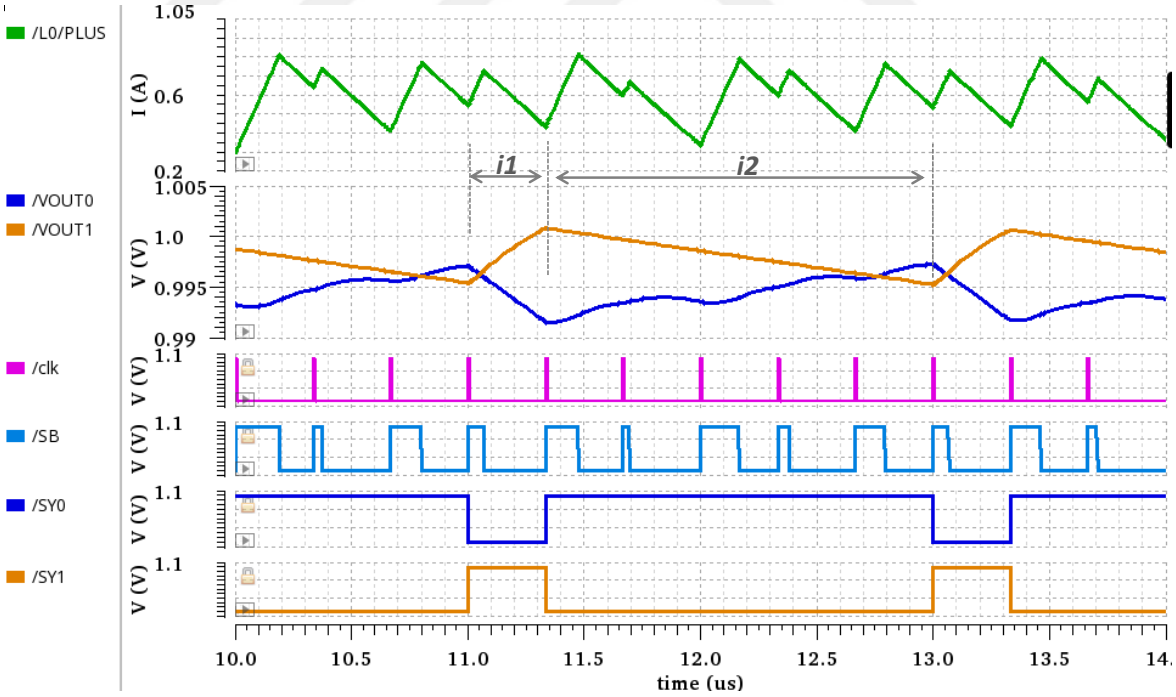


Figure 4.5. Typical SIDO operation- both outputs having positive load

Figure 4.5 gives typical SIDO operation where both outputs are loaded with positive current. Simulation conditions are as follows: V_{DD}=3.8V, V_{OUT0}=1V, V_{OUT1}=1V, L=1μH, C_{OUT0}=30μF, C_{OUT1}=30μF, f_{SW}=3MHz, I_{LOAD0}=500mA, and I_{LOAD1}=100mA.

As both output loads are positive, normal operation will be performed. At simulation time 11μs V_{OUT1} is lower, thus with the next clock S_{Y1} turns ON and coil current supplies V_{OUT1} (interval *i1* in the Figure). During interval *i2*, S_{Y0} is ON and coil current supplies V_{OUT0} until 13μs.

Figure 4.6 gives negative SIDO operation with option 1 type switching (as in Figure 4.2). In this simulation I_{LOAD0}=50mA (low load current, inductor current is expected to decay to zero), I_{LOAD1}= –100mA.

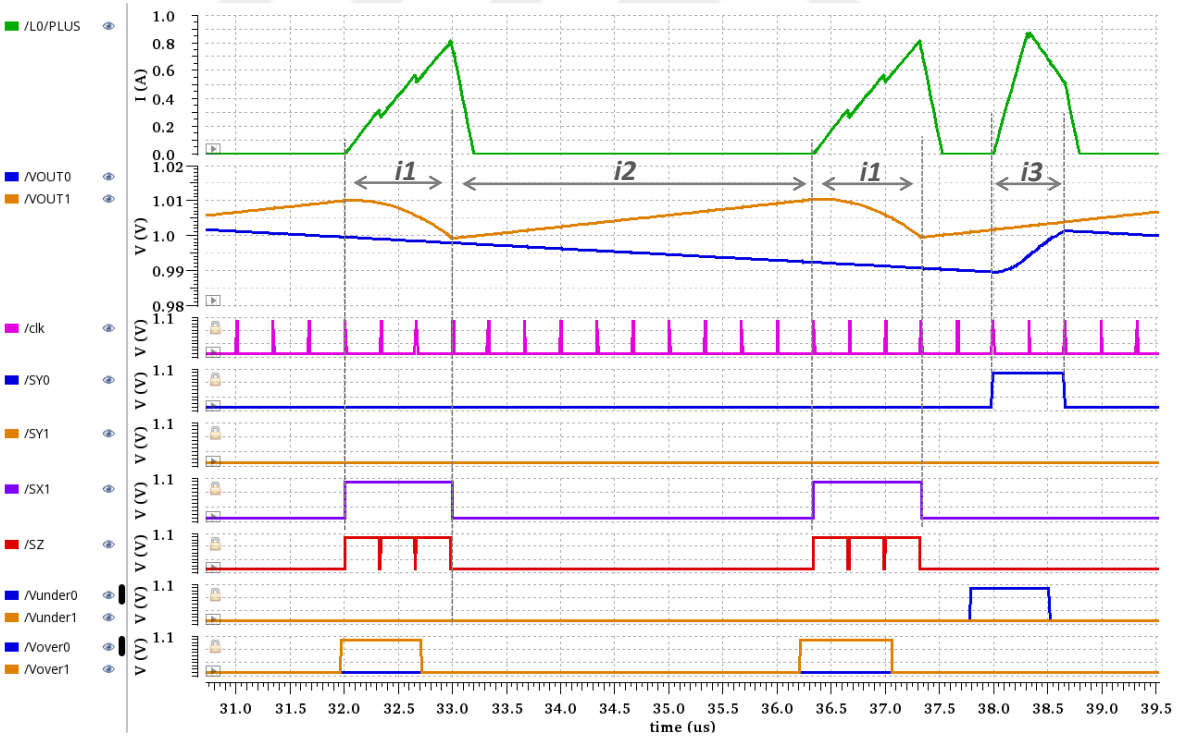


Figure 4.6. Negative SIDO operation- option 1.

At simulation time 32μs V_{OVER1} becomes high, requesting negative operation for V_{OUT1}. During interval *i1*, S_{X1} and S_Z are ON, discharging V_{OUT1} as defined in Figure 4.2 (b).

During interval *i2*, there are no V_{OVER}/V_{UNDER} signals, thus the system is not switching, staying in sleep mode. The build-up inductor current can optionally be discharged to V_{DD} by a recycling diode which can be connected between node L_Y and the input supply V_{DD}.

At simulation time 38μs, V_{UNDER0} is high, S_{Y0} turns on and positive load current is supplied to V_{OUT0} during interval *i3*.

Figure 4.7 gives negative SIDO operation with option 2 type switching (as in Figure 4.3). In this simulation I_{LOAD0}=1A (higher load current, inductor current will continuously stay above zero), I_{LOAD1}= -250mA.

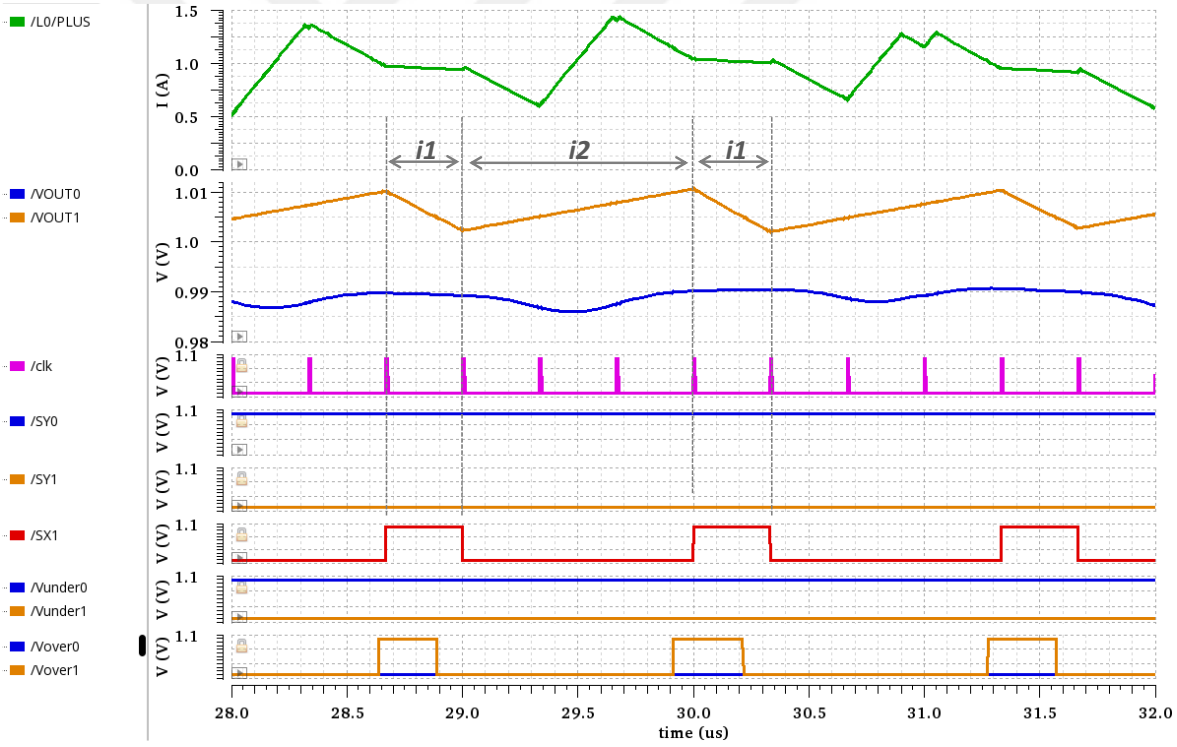


Figure 4.7. Negative SIDO operation- option 2.

Throughout the simulation V_{UNDER0} is on as V_{OUT0} is loaded with 1A. During interval *i1*, V_{OVER1} is high, requesting negative operation for V_{OUT1}. S_{X1} turns on, S_{Y0} continues to stay on. Thus, V_{OUT1} is discharged with the coil current at the same time supplying load current to V_{OUT0} as defined in Figure 4.3 (b). During *i2*, V_{UNDER0} is high, load current is supplied to V_{OUT0}, S_{Y0} stays on; buck switching (S_B switching) continues.

5. BUCK-BOOST CONVERTERS WITH IMPROVED MODE SWITCHING

Buck-boost converters are commonly used in wearable applications where input supply voltage is close to output voltage and high efficiency power conversion is required to extend battery life. A typical example of a Buck-boost converter is the battery-operated USB drive where the USB output is 3.3V and input supply (battery) voltage can be anywhere between 4.8V to 2.8V. As discussed in Section 2.3, due to their relatively complex switching sequence and complicated circuit topology, there are numerous design challenges associated with buck-boost converters.

This chapter brings forth two novel solutions for buck-boost circuit design. Section 5.1 introduces a hysteretic switching technique for low power applications with excellent line transient response, Section 5.2 introduces a current mode switching technique for high power efficiency and improved mode transitions.

5.1. Hysteretic Buck Boost Technique

Due to battery performance limitations buck-boost converters for wearable applications need to achieve very low quiescent current, high power efficiency, and excellent line transient performance. Among different control methods, hysteretic control steps ahead as a preferred control method for wearable buck-boost converters as the line transient performance will be excellent, topology will be simple and thus quiescent current at low load condition will be very low. On top of the mentioned features, two additional advantages of hysteretic control is dispensing with the error amplifier and the clock, thus further simplifying the converter design and achieving lower quiescent current.

Various examples of hysteretic buck converters have been mentioned with Section 2.1.3. Examples of hysteretic boost converters reported in the literature similarly utilize monitoring the output voltage and turning on the boost switch with constant on-time [56] or turning on the boost switch with adaptive on-time [57].

This section presents a novel hysteretic buck-boost converter control technique as defined in [8] and [9] using separate buck and boost pulses, and constant on-time (fixed duty cycle) operation. This section is organized as follows: an operational description of the proposed hysteretic buck-boost topology is followed by details on model implementation given with the next sub-section. Simulation results are given in Section 5.1.2.

The proposed control method is based on defining operation regions monitoring the condition of the output voltage. The operating modes will use separated buck mode and boost mode switching with using constant on and constant off times. Table 5.1 gives a simplified description of the proposed topology. For the defined region 1, where $V_{OUT} > V_{REF}$ there will be no switching. Here V_{REF} is the target output voltage. For region 2, where $V_{OUT} < V_{REF}$ and $V_{OUT} > V_{REF} - \Delta V_1$ there will be buck mode switching with a fixed duty cycle. Here ΔV_1 defines the hysteretic window where practical values of ΔV_1 can be around 10mV. For operational cases where the input voltage is greater than output voltage and output load current is low, this will be the default operating mode. Similarly, for region 3, where $V_{OUT} < V_{REF} - \Delta V_1$ there will be boost mode switching with a fixed duty cycle. When the input voltage is lower than the output voltage, buck mode switching (region 2) will not be able to increase the output voltage and V_{OUT} will start to decrease. Consequently, region 3 operation will take over and boost pulses will result in increased output voltage.

Table 5.1. A Simple operating diagram

Region	V_{OUT} Condition	Operating Mode
1	$V_{OUT} > V_{REF}$	Switches Off
2	$V_{REF} > V_{OUT} > V_{REF} - \Delta V_1$	Buck Mode
3	$V_{REF} - \Delta V_1 > V_{OUT}$	Boost Mode

The proposed system will be enhanced with two additional improvements. First, for faster response, the direction (or derivate) of the output voltage will be sensed, providing the output voltage rising or falling information, which will be an additional input to the region decision algorithm. Second, in addition to buck and boost switching modes, an additional

functional operating mode will be defined, which is 100% duty cycle *buck mode* or equivalently a 0% duty cycle *boost mode* also called as *bypass mode*. In this mode the switches S1 and S3 will be continuously ON. The advantage of this mode is reduced switching (reduced capacitive and non-overlapping) losses, as in this mode switches are continuously ON. As buck-boost converters spend most of their operating lifetime where the output voltage is close to the input voltage, this mode will be frequently used during the operation of the converter, thus enhancing power efficiency and resulting in increased battery life. A complete description of the proposed control system is given with Table 5.2. The introduced technique consists of 5 different operating regions based on the position of V_{OUT} with respect to V_{REF} and the derivative of V_{OUT}.

Table 5.2. Improved Operating Diagram

V_{OUT} Condition	**Reg.**	**$\partial V_{OUT}/\partial t$**	**Buck-Boost Mode**
$V_{OUT} > V_{REF}$	1	(don't care)	Switches Off
$V_{REF} > V_{OUT} > V_{REF} - \Delta V_1$	2	$\partial>0$, V_{OUT} rising	Buck Mode, $D=D_{buck}$
	3	$\partial<0$, V_{OUT} falling	Buck Mode, D=100% = Boost Mode, D=0%
$V_{REF} - \Delta V_1 > V_{OUT} > V_{REF} - \Delta V_2$	3	$\partial>0$, V_{OUT} rising	
	4	$\partial<0$, V_{OUT} falling	Boost Mode, $D=D_{boost}$
$V_{REF} - \Delta V_2 > V_{OUT}$	5	(don't care)	Boost Mode, $D=D_{boost}$

A graphical description of the proposed operating regions for a case example of 3.3V target output voltage and ΔV steps of 10mV is given in Figure 5.1.

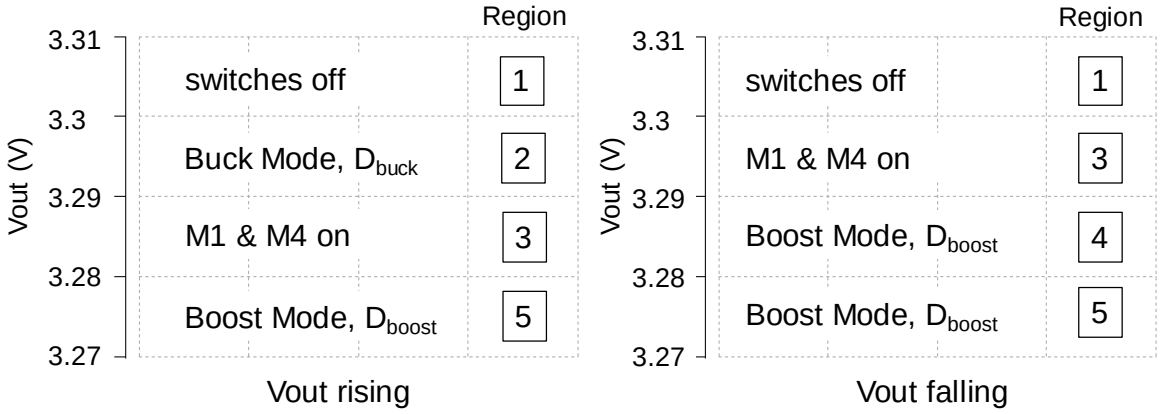


Figure 5.1. Graphical description of operating regions.

5.1.1. Model Implementation

In order to validate the proposed region-based control technique, a switching converter model using hysteretic control, and operating as defined in Table 5.2 has been built. Target specifications of the switching converter based on a typical wearable application platform is given with Table 5.3.

Table 5.3. Specifications

Input Voltage	2.5 – 4.8V
Output Voltage	3.3 V
Inductor / DCR	1μH / 50mΩ
Output Capacitor	30uF
Switching Frequency	3MHz
Load Current	< 500mA
Load Transient I_{LOAD} *from 0 to* I_{MAX}	< 5mV
Line Transient V_{IN} *from 2.5V to 3.8V*	< 5mV

A simplified block diagram of the proposed system is given in Figure 5.2. Three comparators are connected to the output voltage and the reference voltages (V_{REF}, V_{REF}-ΔV_1, V_{REF}-ΔV_2) to define the region of the output voltage. A derivative block connected to the

supply voltage monitors the direction of the output voltage. The derivative block has a binary output (rising / falling) and together with the other comparators they provide inputs to the control block called: “Logic and Timers”. This control block defines the operating modes as described in Table 5.2 and it generates the control signals for the buck-boost power switches. Timer blocks will be used to generate fixed duty cycle (constant on time) pulses for the power switches.

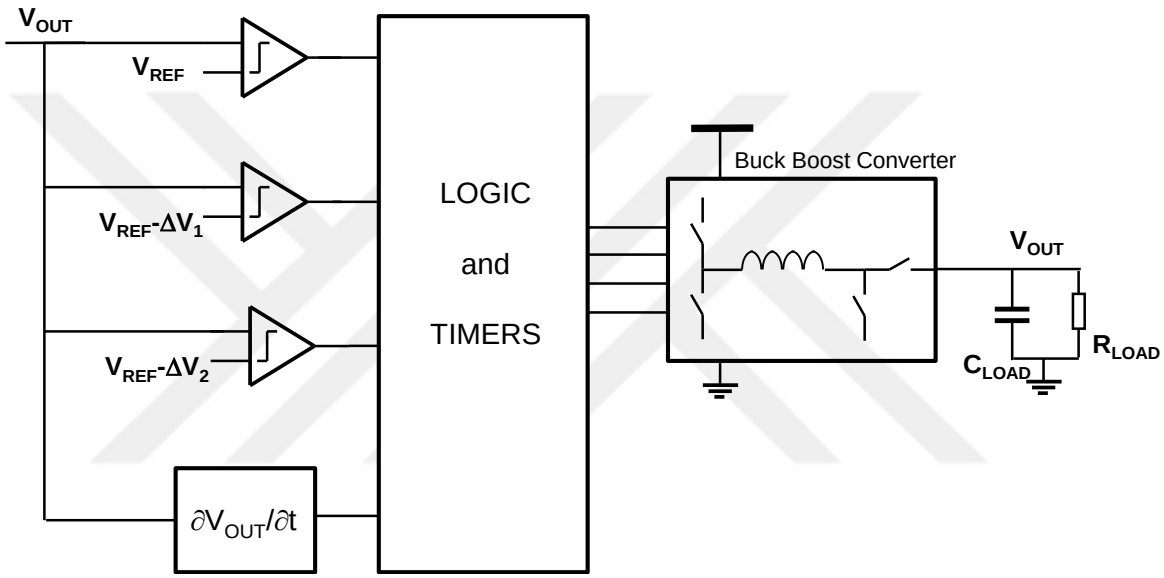


Figure 5.2. Simplified block diagram of the proposed system

The detailed block diagram of the proposed system is given by Figure 5.3. The operating regions *buck_mode*, *boost_mode* and *deep_boost_mode* are defined by the three comparators shown on the top part of the figure.

A sample and hold circuit samples the output voltage when the boost switch S_1 is ON, proving a control input to the derivative block. In step-up converters when the boost switch is ON, V_{OUT} falls due to the output load. The sample and hold circuit helps to eliminate a possible false triggering of the derivative block when the boost switch is ON. As the output of the derivative block is binary, it can simply be implemented as a comparator together with an RC pair. This will enable to use a low power comparator for the generation of the derivative signal thus it will help to achieve low dissipation current, improving efficiency at low load currents.

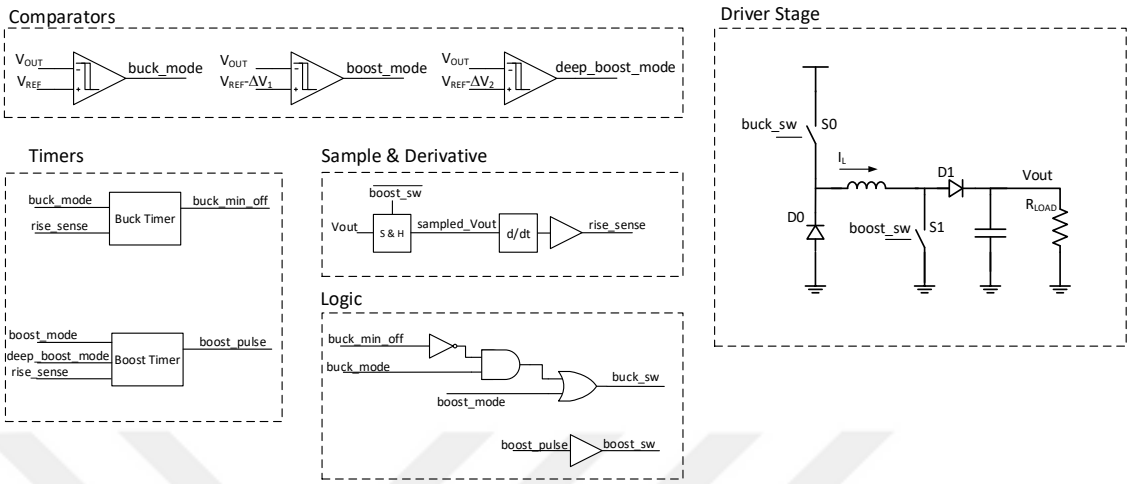


Figure 5.3. Detailed block diagram of the proposed system

The buck-boost converter logic is configured to use separated buck and boost pulses. In *buck mode* S_0 and the active diode D_0 will be switching, S_1 will be OFF and the D_1 will be continuously ON. In *boost mode* S_1 and the active diode D_1 will be switching, S_0 will be continuously ON and D_0 will be OFF.

Referring to Table 5.2, when $V_{OUT} > V_{REF}$, *buck_mode* will be logic 0 and no switching activity will occur, corresponding to Region 1 operation.

Following the value of V_{OUT}, when $V_{OUT} < V_{REF}$ and $V_{OUT} > V_{REF} - \Delta V_1$, *buck_mode* will be logic 1 and other comparator outputs will be at logic 0. From this zone, Region 2 or Region 3 operation will be selected depending on the condition of the derivative of V_{OUT}. If the derivative of V_{OUT} is positive, then the system will operate in Region 2: *Buck Timer* block will generate the switch ON and OFF timings for the fixed duty cycle pulses (D_{buck}), defined for *buck mode* operation. For the same value range of V_{OUT}, if the derivative of V_{OUT} is negative, then Region 3 operation will occur: power switches will be conditioned for bypass mode which is identical to 100% duty cycl*e buck mode* or 0% duty cycle boost mode. In this bypass mode S_0 and D_1 will be continuously ON, and S_1 and D_0 will be OFF.

For the next value range of V_{OUT}, where $V_{OUT} > V_{REF} - \Delta V_1$ and $V_{OUT} < V_{REF} - \Delta V_2$, *boost_mode* will be logic 1. Here, if the derivative of V_{OUT} is positive, then the system will

similarly operate in Region 3 as described in the previous paragraph. Conversely, if the derivative of V_{OUT} is negative, then the system will operate in Region 4, as defined by Table 5.2. In this switching mode boost timer block will generate the fixed duty cycle pulses for the power switches S_1 and D_1, resulting in *boost mode* operation with a duty cycle of D_{boost}.

Region 5 operation occurs regardless of the derivative of V_{OUT} when $V_{OUT} < V_{REF}$-ΔV_2; *deep_boost_mode* comparator output will be logic 1 and system will operate with *boost mode* switching with a duty cycle of D_{boost}, until the condition of V_{OUT} changes.

5.1.2. Simulation Results

A functional model of the switching converter as defined in Figure 5.3 has been built in Cadence design environment with ideal components and using 100mΩ switches in the driver stage. Simulation results of the converter for different input supply voltage / output load conditions are given in Figure 5.4 - Figure 5.7.

Typical operating conditions for the switching converter are V_{IN}=3.8V and I_{LOAD}=100mA. Figure 5.4 gives the simulation results for these input conditions. The system operates in Region 2 and Region 3 corresponding to buck switching and bypass mode, occurring interchangeably. During this simulation, it is observed that the derivative of V_{OUT} is not low enough to trigger a logic 0 in *rise_sense* signal. This is due to the internal hysteresis of the derivative voltage comparator.

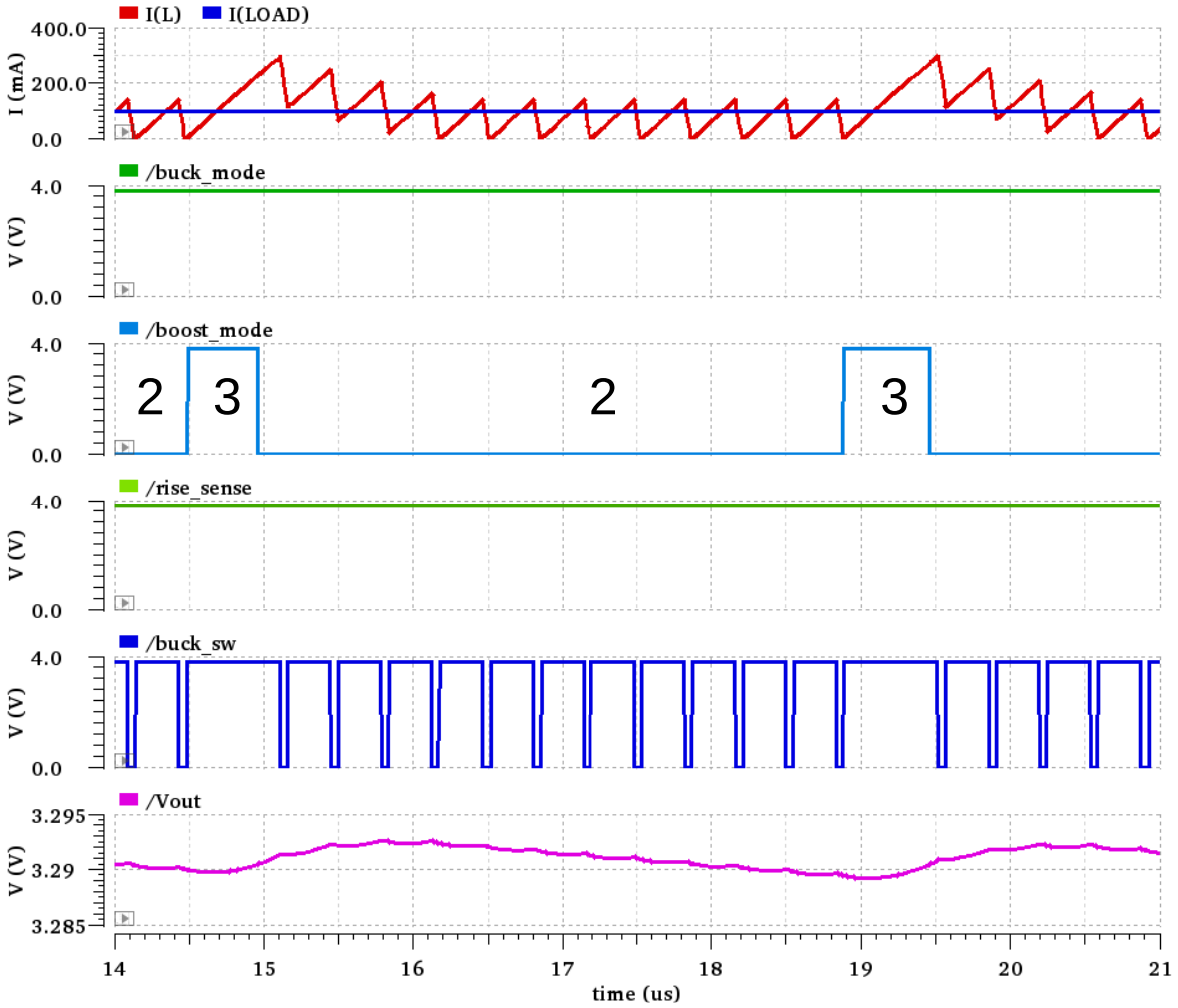


Figure 5.4. Simulation results for V_{IN}=3.8V, V_{OUT}=3.3V I_{LOAD}=100mA.

The highest input supply voltage for the switching converter is 4.8V as defined in Table 5.3. Simulation results for this input supply voltage condition and typical output load are given in Figure 5.5. As the input supply voltage is higher from the specified target output voltage, *buck mode* operation is expected. It is observed that the simulation starts with Region 1, "no switching" condition, as V_{OUT}>V_{REF} at the start of the simulation. As load current discharges the output capacitor and V_{OUT} starts to fall, the derivative of the output voltage will become negative and *rise_sense* will become logic 0, also given the input condition V_{OUT} > V_{REF} -ΔV_1, the system operates in Region 3: 100% *buck mode,* this is followed by V_{OUT} rising, *rise_sense* will become logic 1, and the system operates in Region 2 (*buck mode*) and consequently loops back to Region 1.



Figure 5.5. Simulation results for V_{IN}=4.8V, V_{OUT}=3.3V I_{LOAD}=100mA.

The lowest input supply voltage for the switching converter is 2.5V as defined in Table 5.3. Simulation results for this input supply voltage condition and typical output load are given in Figure 5.6. As the input supply voltage is lower than output voltage, boost mode operation is expected. It is observed that the simulation starts with Region 4, as $V_{OUT}<V_{REF}-\Delta V_1$, $V_{OUT}>V_{REF}-\Delta V_2$ and V_{OUT} is falling, thus boost pulses are observed. Region 3 operation follows (bypass mode operation) when V_{OUT} starts to rise.

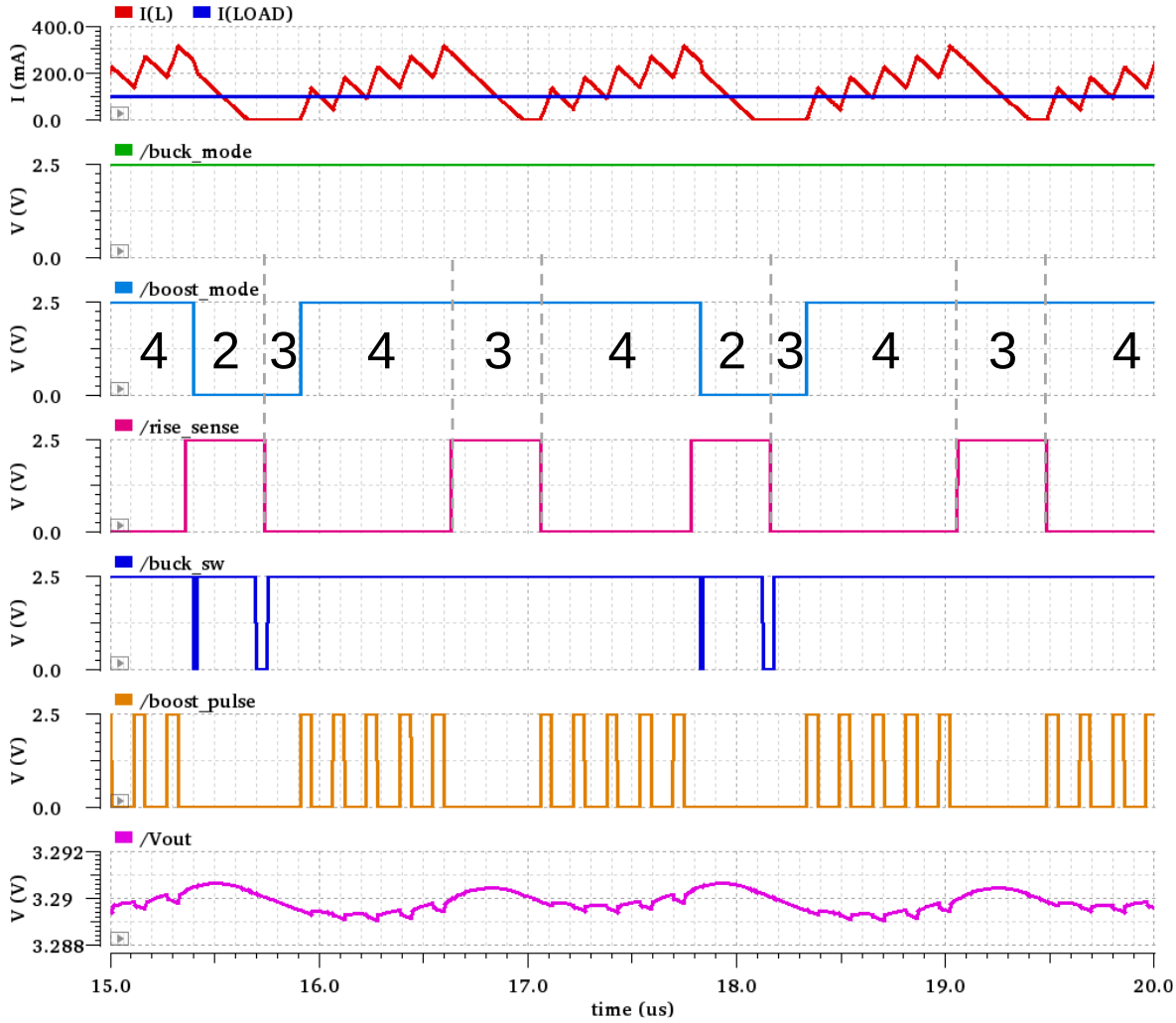


Figure 5.6. Simulation results for V_{IN}=2.5V, V_{OUT}=3.3V I_{LOAD}=100mA.

Line transient is an important performance criterion for battery operated systems, especially for systems with relatively small batteries as in wearable applications. Figure 5.7 gives line transient simulation results where the input supply voltage falls from 3.8V to 2.5V and rises back, with a rise/fall slew of 1V/μs and with I_{LOAD}=100mA. As a benefit of using hysteretic control mode, it can be observed that the output voltage regulation is less than 5mV, which defines a good performance metric for many possible switching converter applications.

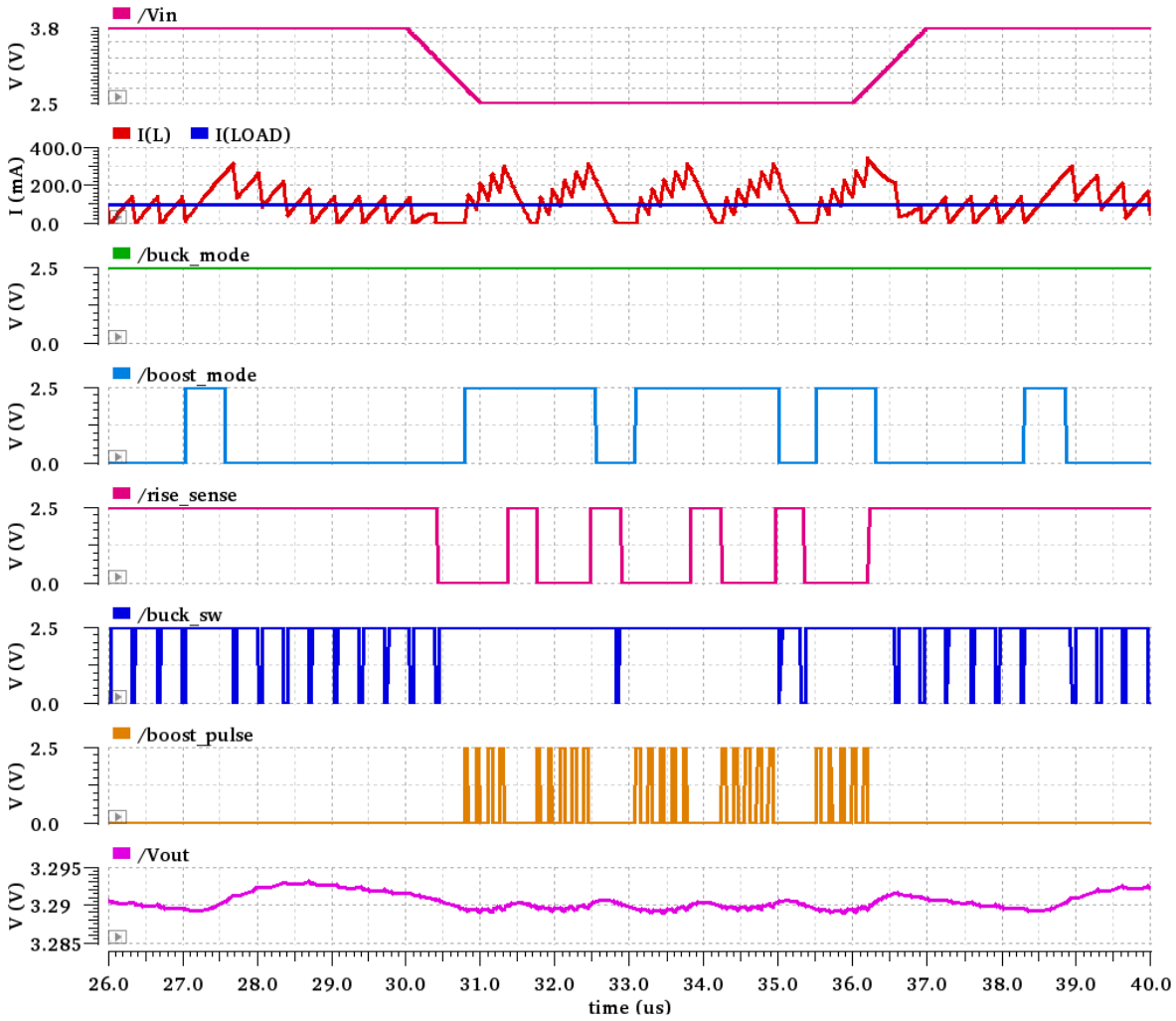


Figure 5.7. Line transient simulation results.

In summary, simulation results using the macromodel show that the proposed control topology is able to achieve very low line transient regulation performance with low quiescent current, owing to the simplicity of the architecture and meet the target specifications as defined in Table 5.3.

5.2. Current Mode Buck-Boost Converter with Continuous Mode Switching

To improve power efficiency and reduce inductor current ripple of a buck-boost converter, separated buck and boost pulses as defined in Section 2.3 can be preferred as an alternative switching sequence to conventional continuous switching operation.

An example of a buck-boost converter utilizing “separated buck and boost pulses” and using voltage mode control is implemented in [58] where the error voltage is compared against two adjacent sawtooth signals (buck ramp and boost ramp in Figure 5.8) by two comparators.

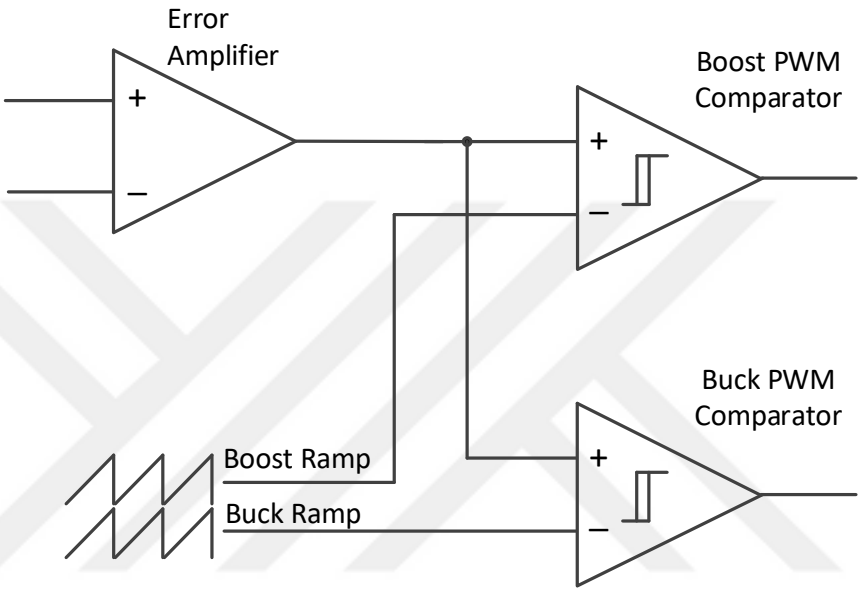


Figure 5.8. Voltage mode control buck-boost converter.

If the error voltage is low, it will only be crossing the buck ramp signal and only buck switching will occur. Similarly, if the error voltage is high, it will only be crossing the boost ramp signal and only boost switching will occur. An example of switching versus changing control voltage is given by Figure 5.9 (a).

A similar technique is using two-shifted error voltages and a single ramp signal, given by Figure 5.9 (b). When the buck error voltage (error voltage shifted up) crosses the ramp signal, buck switching will occur, similarly when the boost error voltage (error voltage shifted down) crosses the ramp signal, boost switching takes place. In Figure 5.9 (b) the difference of buck and boost error voltages is equal to the amplitude of the ramp signal. Thus, in a given clock cycle buck and boost switching will not overlap.

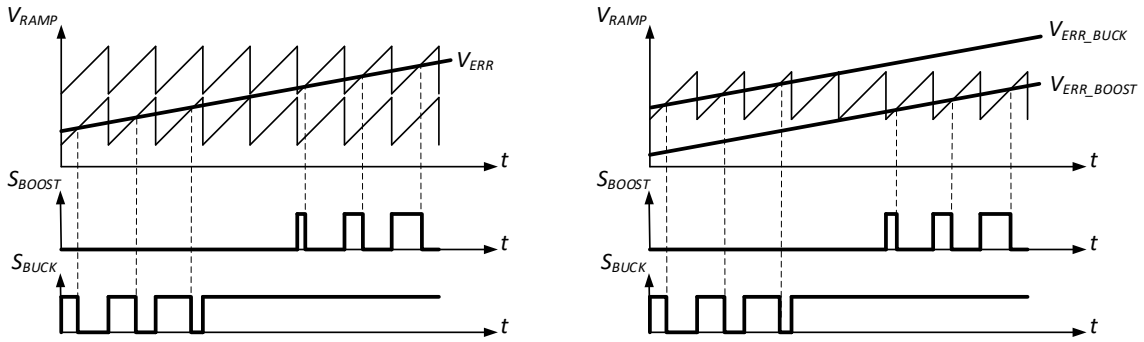


Figure 5.9. PWM pulse generation for buck and boost operations (a) using one error voltage and two ramp signals (b) using two error voltages and one ramp signal [58].

As in buck or boost converters, current mode control (CMC) can also be used in buck-boost converters. Though CMC is more desirable for most applications, it has serious challenges if separated buck and boost pulses are required.

There have been examples of current mode control buck-boost converters utilizing separated buck and boost pulses [59,60]. In both examples, the decision on staying in the buck region or in the boost region is given by checking the duty cycle. In [60], changing from buck to boost mode is decided when D_{buck}> 90% (in the next switching cycle, boost switching will take place), and changing from boost to buck mode is decided when D_{boost}<10%.

There is a serious disadvantage of changing modes with this technique, since it will take significant time for the loop filter to settle to normal operation when changing from buck mode to boost mode, unacceptable transients at the output voltage can be observed.

The following section describes a novel buck-boost mode control topology using current mode control, utilizing separated buck and boost pulses (reducing switching losses and inductor current ripple) and utilizing a buck/boost mode decision method with continuous error voltage for buck and boost mode therefore eliminating transients in the control loop between modes [10].

5.2.1. Proposed Control Mode Topology

A buck boost system which utilizes the mentioned features has been constructed with ideal elements and is given by Figure 5.10.

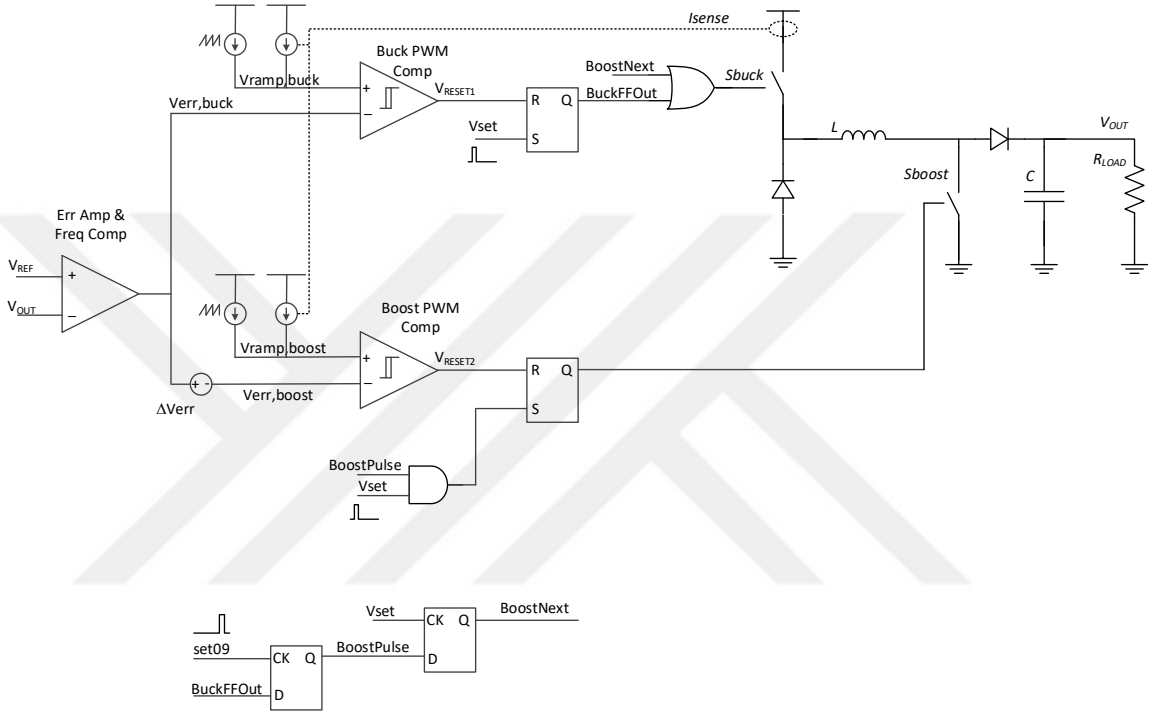


Figure 5.10. Current mode buck-boost topology.

In Figure 5.10, the upper section constitutes of buck part together with current sense, buck ramp, buck error voltage, PWM comparator, buck RS flip-flop and the buck switch. An OR gate forces buck switch to be continuously ON during *boost mode*. The inductor current sense is taken from buck switch side. The mid-section of the Figure gives the boost part together with current sense, boost ramp, boost error voltage, PWM comparator, logic cells and the boost switch. An AND gate at the input of boost RS flip-flop is for not setting the boost switch during *buck mode*. A voltage source relates the boost error voltage to buck error voltage with $V_{err,boost} = V_{err,buck} - \Delta V_{err}$.

Two D-type flip flops at the bottom part of the figure sample the buck RS flip flop output at $t=D_{set}T$ (e.g. comparing buck duty cycle with 0.9) and decide whether the next pulse will be a buck pulse or a boost pulse.

As described, the mentioned system is capable of generating separate buck and boost pulses, operating with current mode control and having a continuous error voltage. The following paragraph explains a simple technique to define ΔV_{err} such that mode transitions will be continuous.

For a continuous mode transition the error voltage value at 90% duty cycle for buck operation and the error voltage value at 10% duty cycle for boost operation need to be equalized (other maximum duty cycle for buck and minimum duty cycle for boost values can also be defined alternatively). For current mode operation, also considering the ramp voltage, at D=0.9 (the time the buck comparator changes output),

$$V_{err,buck} = I_{sense,max,buck} R_{sense} + D_{buck} V_{ramp,buck} \tag{5.1}$$

$$I_{sense,max,buck} = I_{LOAD} + \frac{V_{in} - V_{out}}{L} D_{buck} T \tag{5.2}$$

and at the time the boost comparator changes output or when $D=0.1$;

$$V_{err,boost} = I_{sense,max,boost} R_{sense} + D_{boost} V_{ramp,boost} \tag{5.3}$$

$$I_{sense,max,boost} = \frac{I_{LOAD}}{(1 - D_{boost})} + \frac{V_{in}}{L} D_{boost} T \tag{5.4}$$

where T is the cycle period. For the mentioned conditions, and for the sake of simplicity, it has been assumed that D_{boost} is close to 0 and V_{IN} is close to V_{OUT}, $I_{sense,max}$ in buck and boost modes will be similar, and:

$$V_{err,buck} - V_{err,boost} = 0.9 V_{ramp,buck} - 0.1 V_{rampboost} = \Delta V_{err} \tag{5.5}$$

Thus, we can relate the buck and boost error voltages. ΔV_{err} is implemented as an ideal dc source in the simulation setup of Figure 5.10. Figure 5.11 gives a graphical description of the mentioned mode switching technique.

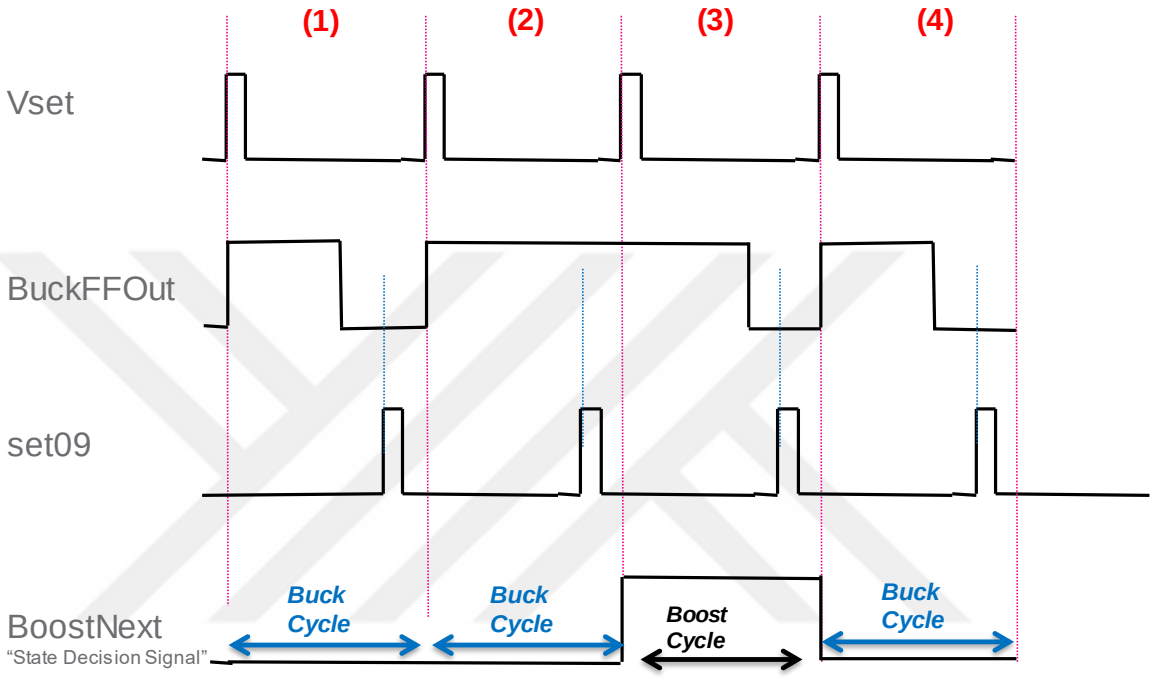


Figure 5.11. Current mode buck-boost topology operational diagram.

5.2.2. Simulation Results

Figure 5.12 gives the simulation results for V_{IN}=4.5V, V_{OUT}=3V and I_{LOAD}=1A, f_{SW} =1MHz. V_{IN}>V_{OUT} and the system works only in buck mode, with D_{buck}=0.76. As D_{buck}<0.9 the BoostNext signal (bottom in Figure 5.10) is logic zero, hence no boost cycle is observed.

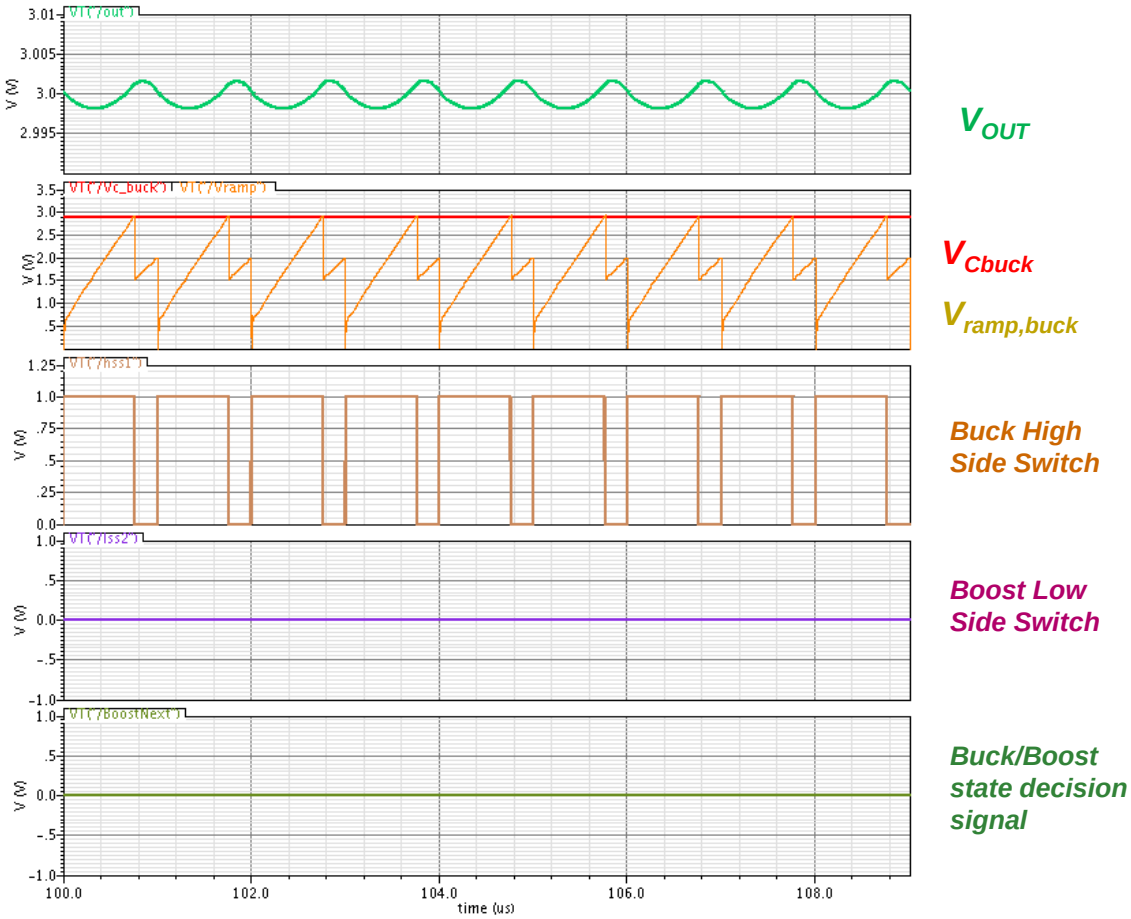


Figure 5.12. Simulation results for V_{IN}=4.5V, V_{OUT}=3V and I_{LOAD}=1A.

Figure 5.13 gives the simulation results for V_{IN}=2.5V, V_{OUT}=3V and I_{LOAD}=1A. V_{IN}< V_{OUT} and the system works only in boost mode, with D_{buck}=1. As D_{buck}>0.9 the *BoostNext* signal (bottom in Figure 5.10) is always logic 1, hence only boost cycles are observed. During boost mode, buck high side switch is continuously ON.

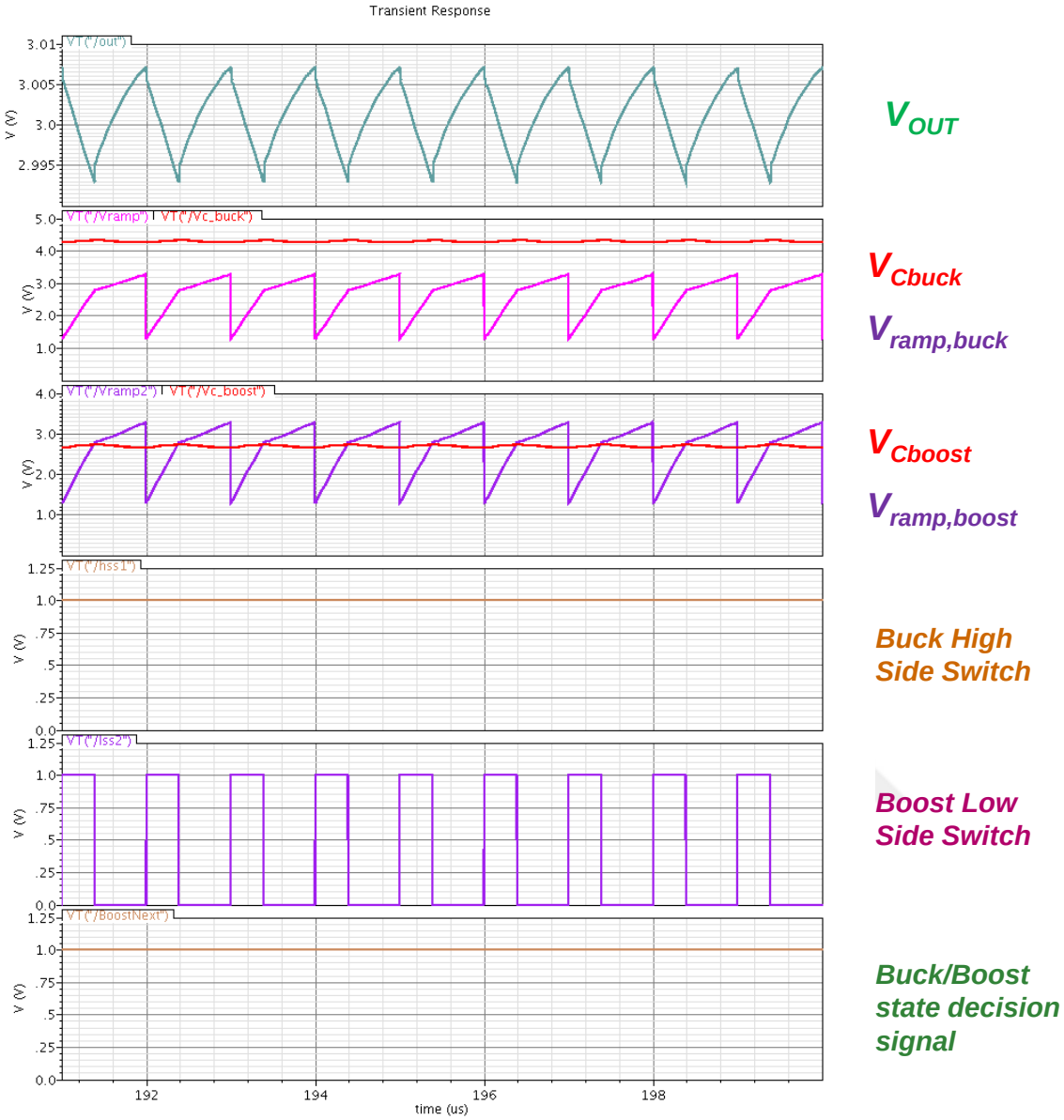


Figure 5.13. Simulation results for V_{IN}=2.5V, V_{OUT}=3V and I_{LOAD}=1A.

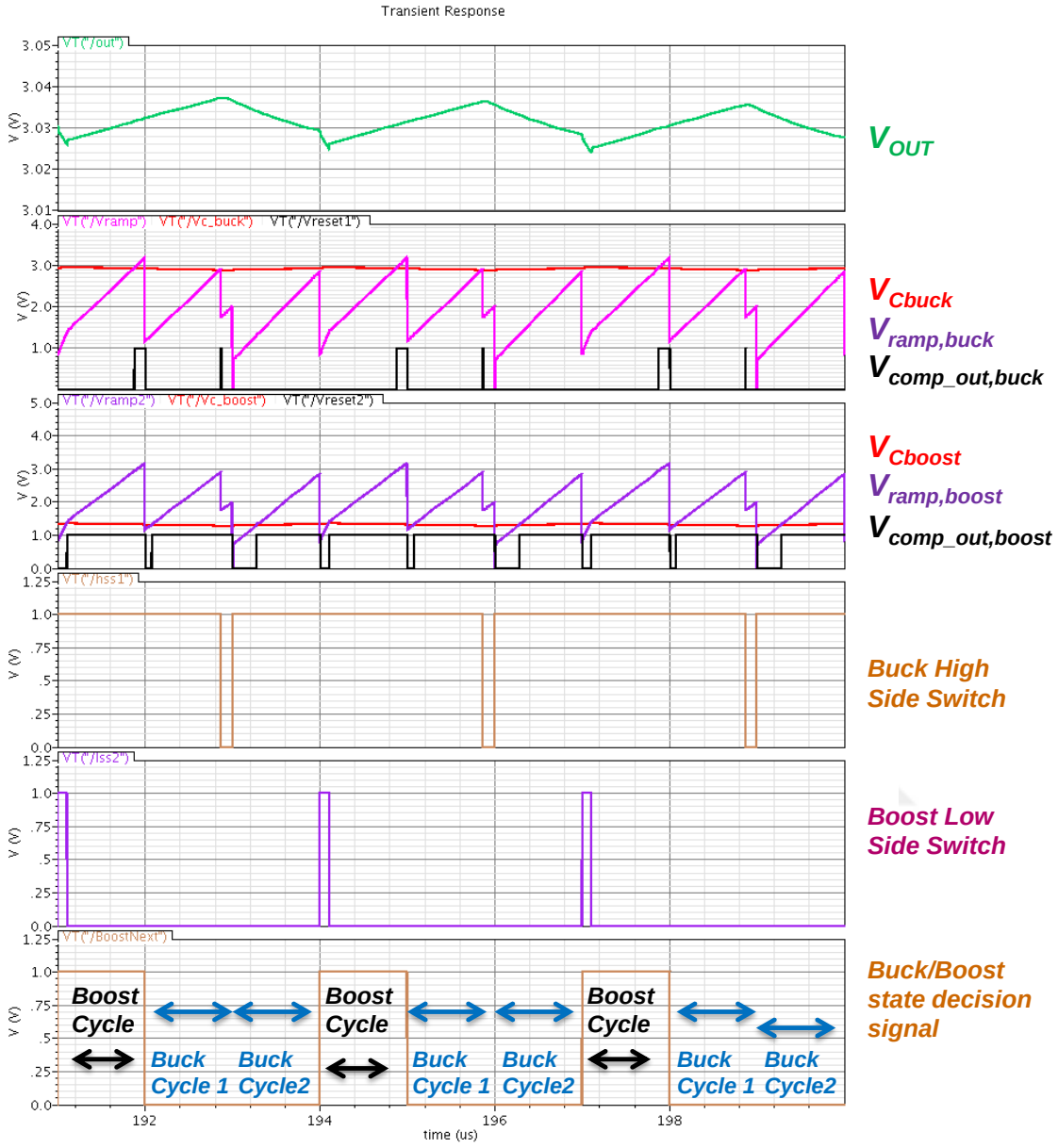


Figure 5.14. Simulation results for V_{IN}=3.5V, V_{OUT}=3V and I_{LOAD}=1A.

Figure 5.14 gives the simulation results for V_{IN}=3.5V, V_{OUT}=3V and I_{LOAD}=1A. This is the case where the proposed topology shows the improvement to system operation. V_{IN} is close to V_{OUT} and separate buck and boost pulses are observed: in this case, one boost cycle is followed by two buck cycles. The buck/boost cycle combinations vary with different operating conditions.

At simulation time 191μs (start of frame), a boost cycle takes place. After ~0.8μs (0.8xT, f_{SW}=*1MHz*) $V_{c,buck}$ crosses $V_{ramp,buck}$. As D_{buck}<0.9 the next cycle is a buck cycle. During this cycle D_{buck}=0.86 and the next cycle is also a buck cycle. During the second buck cycle D is 1 and the next cycle will be a boost cycle. A stable and continuous error voltage is observed throughout operation.

5.3. Conclusion

Two performance improvement techniques for buck-boost converters are presented in this section. The buck-boost converter with hysteretic control consists of a simple system: three comparators, a derivative circuit, logic, timers, and power switches. Simulation results show that this topology is able to achieve very low line transient regulation performance with low quiescent current, owing to the simplicity of the architecture, thus promising to be a convenient solution for wearable platform applications. Future work on the hysteretic control buck boost will be incorporating digital assistance for performance improvement.

The current mode buck-boost converter with continuous mode switching technique introduces a control technique to achieve continuous error voltage between buck mode and boost mode transitions. An unexpected advantage of this system is its ability to suppress sub-harmonic oscillation. Buck-boost converters encounter high duty cycle operation in buck mode, which requires extreme values for slope compensation for CMC (V_{in} is typically close to V_{out}). However, with this topology a high duty cycle buck will be followed by a low duty cycle boost cycle, which will force the system back to non-subharmonic operation.

6. LOCK-OUT PROTECTION CIRCUITS FOR BOOST AND BUCK-BOOST CONVERTERS

In both boost and buck-boost converters, V_{OUT}/V_{IN} is inversely proportional to *(1-D)* which states that V_{OUT} will reach infinity when $D=1$ (where D is the duty cycle, V_{OUT} is output voltage of the switching converter and V_{IN} is the input/supply voltage of the switching converter). However, due to the parasitic resistance in series with the inductor and the parasitic resistance of the inductor itself, V_{OUT}/V_{IN} starts to decrease with D after making a peak. This results in a positive feedback mechanism if the duty cycle exceeds the peak, followed by the collapsing of the output voltage; as at the right side of the peak the control loop will be increasing D further once V_{OUT}/V_{IN} starts to decrease and V_{OUT}/V_{IN} will decrease further as D is increased by the control loop. Hence, this phenomenon is called "Duty Cycle Induced Lock-Out Issue" [61-64]. The mentioned problem becomes more significant in buck-boost converters where two switching pass devices are in series with the inductor thus further increasing the value of the parasitic resistance in series with the inductor.

A practical solution to this issue is using a limit for the duty cycle (e.g. limiting D at 60%, such that it will not increase further). This limit (D_{limit}) is estimated considering the worst case scenario: minimum input supply voltage, worst case temperature, maximum r_{on} of pass devices, maximum load current, etc. However, setting a limit for the duty cycle based on worst case conditions also limits the operation of the switching converter in optimal conditions, as D cannot exceed D_{limit} in cases where it could be beneficial to the system performance to utilize higher values of D. As an example, the system should be able to utilize higher values of duty cycle at low load conditions to achieve higher output voltages. Other drawbacks of using D_{limit} with this method is that it is based on simulation results and models, and this technique requires special clock generation where considering the associated timing spread, usable value range of D will reduce further. It is preferable to sense *actual* peak of V_{OUT}/V_{IN} and limit D at the peak of V_{OUT}/V_{IN} with an adaptive system.

After an analytical description of the mechanisms causing the lock-out, this section describes two novel techniques for presenting a solution to the "Duty Cycle Induced Lock-

Out Issue". The mentioned techniques provide adaptive solutions aiming to eliminate the lock-out mechanism by limiting the duty cycle of the switching converter when the converter is operating in the positive feedback region.

6.1. Duty Cycle Induced Lock-Out Issue

Voltage gain *(V_{OUT}/V_{IN})* vs. duty cycle *(D)* plot for boost converters is given in Figure 6.1, plotted for different values of R_w/R, where R_w is the equivalent total parasitic resistance in series with the inductor and R is the load resistance [61]. The red curve (the leftmost trace) is for R_w=0 and the blue curve (the bottom trace) is for R_w/R=0.1. When the value of D for some reason reaches the right side of the peak (negative slope region in Figure 6.1), V_{OUT} will start falling, which will cause the control loop to increase D further resulting in a positive feedback and eventually D will be stuck at 1 and V_{OUT} will be a low voltage.

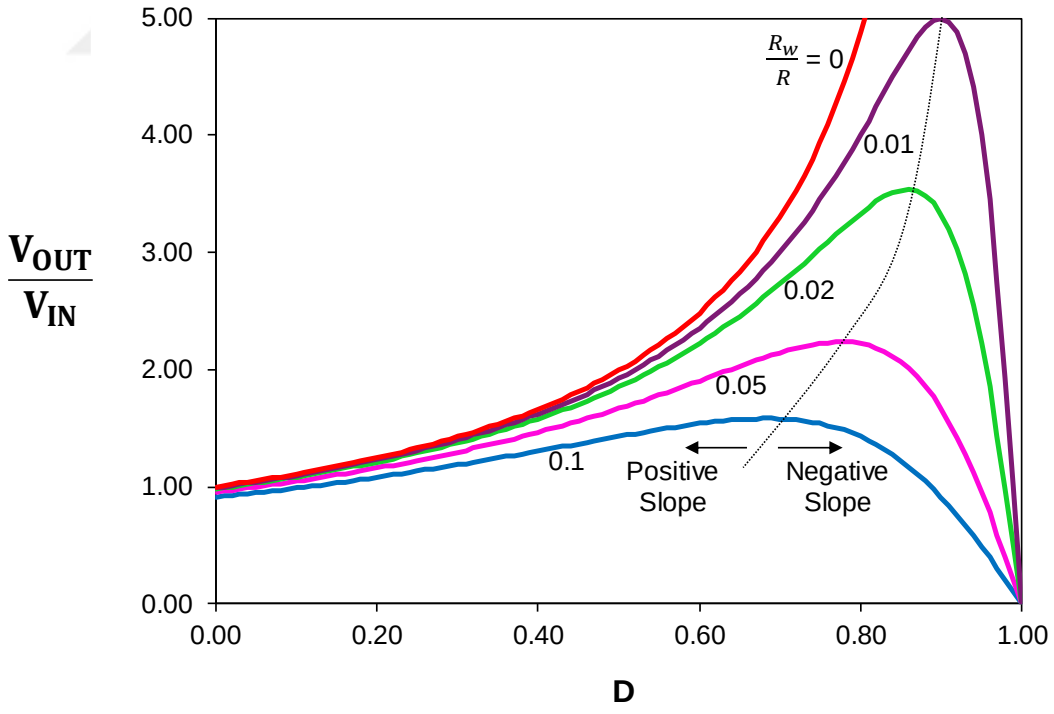


Figure 6.1. Effect of the parasitic resistance : voltage gain vs. duty cycle.

As shown in Figure 6.1, the peak value of V_{OUT}/V_{IN} is a function of R_w/R; it is observed that with increasing values of R_w/R the negative slope starts at earlier values of D.

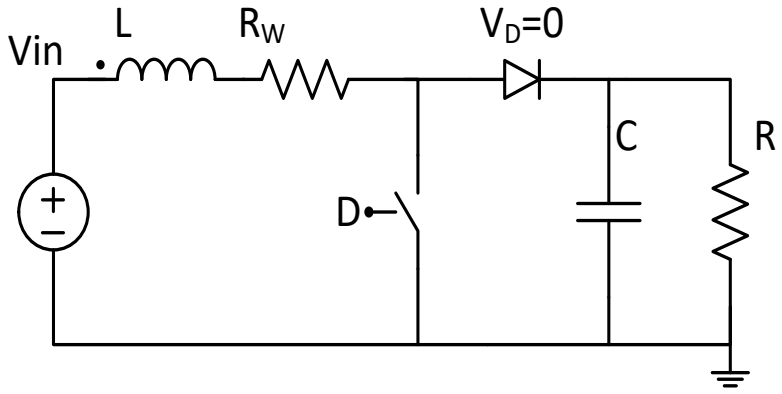


Figure 6.2. Simple boost converter model

To analytically locate the peak, assuming a simple boost converter with associated parasitic resistances in series with the inductor *L* being modelled as R_w, as shown in Figure 6.2, the following equations can be written [61]:

$$V_{in}I_L = R_w I_L^2 + \frac{V_{out}^2}{R} \tag{6.1}$$

as the input power is equal to the sum of the resistive loss and the output power, and from charge balance equations,

$$(1-D)I_L = \frac{V_{out}}{R} \tag{6.2}$$

as the average diode current is equal to the load current. Using these formulas, we can achieve the function of the curves given by Figure 6.1.

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D}\frac{1}{1+\frac{R_w}{(1-D)^2 R}} \tag{6.3}$$

The two proposed control techniques described in the next sections aim to locate the peak of the curve using analog circuit components and limit the duty cycle accordingly.

6.2. Duty Cycle Limitation by Replica Voltage Drop

Taking the derivative of Equation (6.3) with respect to *D* and solving to find the value of *D* where V_{OUT}/V_{IN} has a peak, we can achieve D_{max}:

$$D_{max} = 1 - \sqrt{\frac{R_w}{R}} \tag{6.4}$$

The D_{max} value should be the actual limit for duty cycle (D_{limit}). But it needs to be expressed in terms of parameters more compatible with analog design components for circuit level processing. Replacing *D* in Equation (6.3), with D_{max} given by Equation (6.4), at $D=D_{max}$, the equations simplify to:

$$\frac{V_{out}}{V_{in}} = \frac{1}{2}\sqrt{\frac{R}{R_w}} \tag{6.5}$$

and

$$\frac{V_{out}}{V_{in}} = \frac{1}{2(1 - D_{max})} \tag{6.6}$$

Solving for R_w from Equation (6.5), one gets:

$$R_w = \frac{R\, V_{in}^2}{4\, V_{out}^2} \tag{6.7}$$

and replacing *R* in Equation (6.7) with the expression from Equation (6.2) leads to:

$$R_w\, I_L = \frac{V_{in}^2}{4\,(1 - D_{max})\, V_{out}} \tag{6.8}$$

Replacing V_{OUT} with the expression obtained from Equation (6.6) to simplify Equation (6.8), we achieve:

$$R_w\, I_L = \frac{V_{in}}{2} \tag{6.9}$$

thus, a condition for stability is achieved which ensures the system operates in positive slope for V_{OUT}/V_{IN} (referring to Figure 6.1), when

$$R_w\, I_L < \frac{V_{in}}{2} \tag{6.10}$$

In Equation (6.10) R_w is the total resistance in series with L, which comprises: ESR of L, parasitic resistances due to on-chip and off-chip connections, the resistance due to the diode or the active-diode-pass-transistor multiplied by *(1-D)*, and the resistance of the switch (usually implemented as an NMOS switch) multiplied by D; in buck-boost converters the resistance of the buck switch in series with L will add to this lumped resistance.

An interpretation of Equation (6.10) from circuit behavior approach is: if the voltage drop on the lumped parasitic resistance exceeds half of the input supply voltage, then the boost converter cannot function as a step up converter anymore.

In circuit implementation, a comparator will check the ΔV on a replica R_w having a current of a replica I_L and will compare it with $V_{in}/2$, preferably with some margin and will generate a logic signal which limits the duty cycle [11] , thus saving the loop from entering the positive feedback region. As the mentioned problem becomes more significant in buck-boost converters where two pass devices are in series with the inductor (for any given cycle), the following technique and associated simulations will be carried out from the example of a buck-boost converter operating in boost switching mode.

6.2.1. Circuit Implementation

A circuit implementation which utilizes the mentioned features has been constructed with ideal circuit components for simulation purposes as given by Figure 6.3.

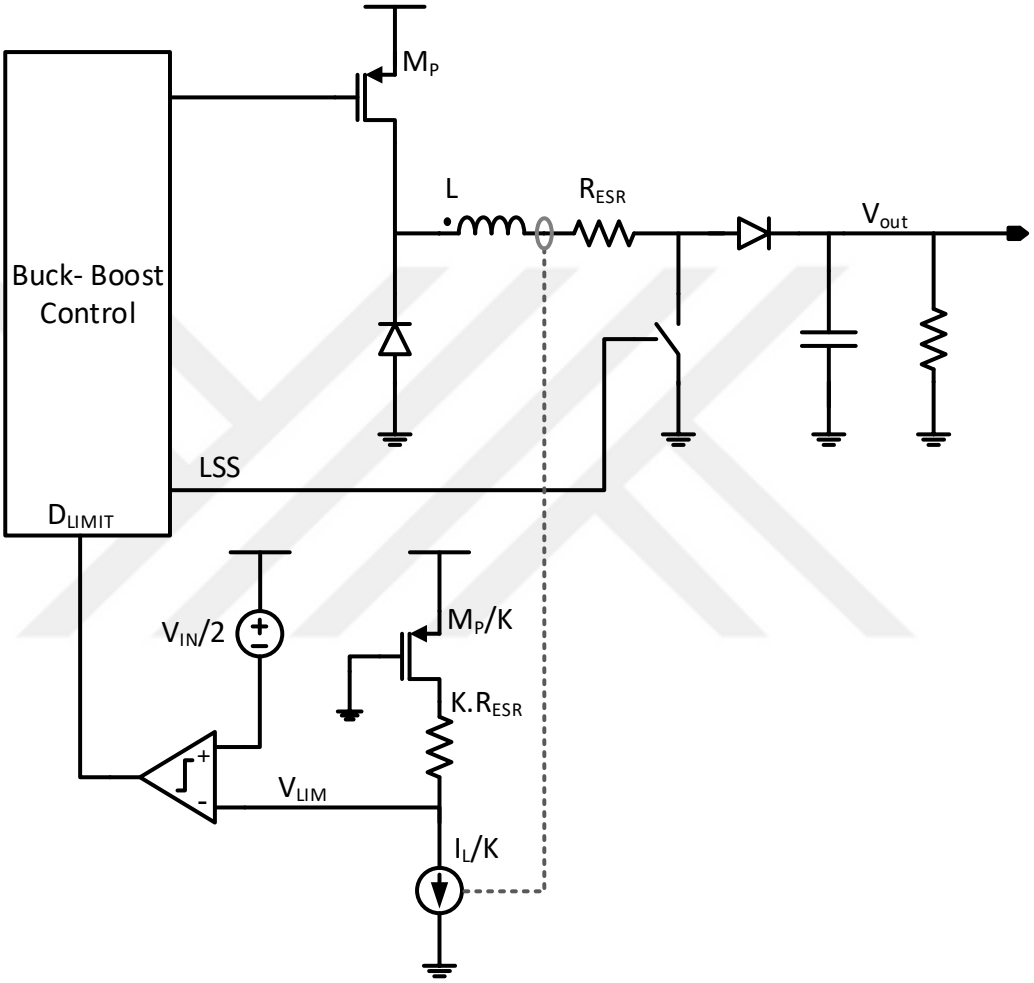


Figure 6.3. Block diagram of the circuit implementation.

The upper part of the block diagram describes a buck-boost converter together with the basic building blocks comprising the inductor *L*, load resistance, and the switches. In the bottom part of the block diagram a comparator checks the total ΔV on a replica parasitic resistor for R_w and a replica pass device for M_P with a drain current of I_L/K, compares the voltage drop with V_{LIM}, where V_{LIM} is equal to half of the input supply, referring to Equation (6.10). The comparator then generates a logic signal which limits the duty cycle of the switching converter through the buck-boost control logic. Thus, the lock-out issue is eliminated.

In many buck-boost converters for battery operated systems, at minimum input supply voltage and worst case conditions, the buck high side switch (usually implemented as a PMOS device - M_P in Figure 6.3) r_{ON} contributes to more than 50% of the series parasitic resistance with the inductor. Similarly, ESR of L and conduction losses will contribute to about 25% of total lumped series resistance to the inductor. Considering these facts, it will be possible to practically replicate R_w simply with the mentioned two contributors, which are a replica pass device M_P/K and a replica series resistance.

The value of the replica series resistance should be selected such that it replicates ESR of L and other associated parasitics (e.g. PCB parasitics) preferably with the correct temperature coefficient. Programmability option of this resistance can be utilized to cover different types of coils. On top of the calculated replica resistor value, some design margin can be added to cover non-idealities, such as process variation. For different applications other than buck-boost converters, other resistive factors can be taken into account replicating the pass device with correct replica devices. Simulation results of the proposed technique are given in the next section.

6.2.2. Simulation Results

Figure 6.4 gives simulation results for a buck-boost converter with V_{IN}=2.5V, f_{clk}=3MHz, with a load current profile starting to increase at 100μs and the output voltage starts to fall. There is no duty cycle limit protection (D_{limit}); thus, as the control voltage V_{ERROR} starts increasing, output voltage decreases more and collapses.



Figure 6.4. Simulation results for a buck-boost converter with V_{IN}=2.5V and no D_{limit}.

Figure 6.5 gives simulation results for a buck-boost converter with protection circuit enabled. The D_{limit} comparator reference voltage (V_{LIM}, pink color trace) is set to 1.25V ($1/2V_{IN}$). At simulation time 100μs, the load current starts to increase and output voltage starts to fall. When load current increases, the inductor current also increases and creates more drop on the replica PMOS M_P/K and KxR_w (Figure 6.3). With increasing load current, V_{LIM} starts to cross 1.25V and the comparator generates a logic high output (magenta trace). At the time the comparator output becomes high, switching converter control logic turns off the pass device. Thus, the inductor current starts to decrease, V_{LIM} returns back to higher values. This is the region where the protection circuitry is operational, limiting the duty cycle and protecting the output voltage from collapsing.

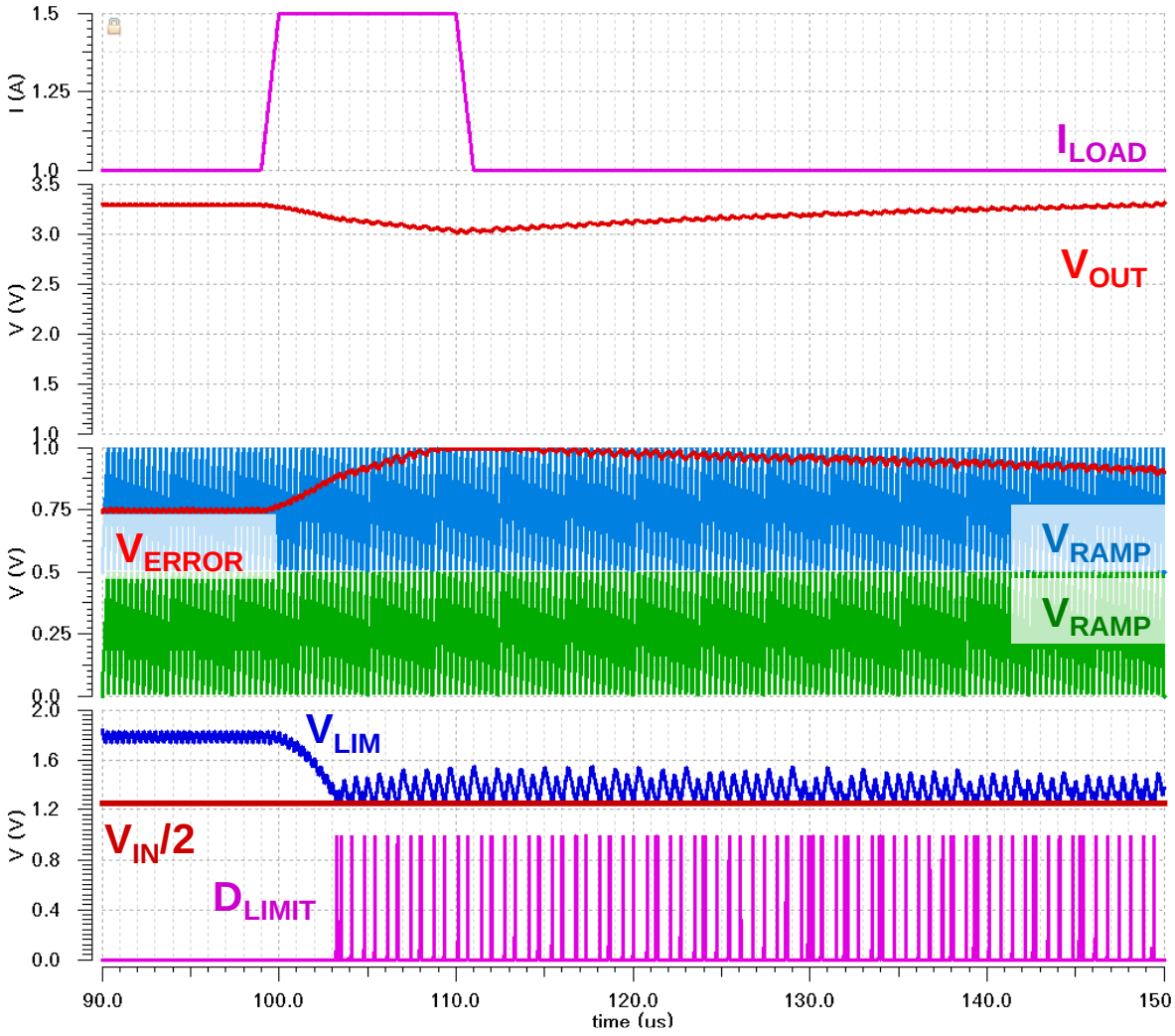


Figure 6.5. Simulation results for a buck-boost converter with proposed protection.

6.3. Duty Cycle Limitation by Sawtooth Signal Prediction

The solution presented in the previous subsection solves the lock-out issue by using a replica parasitic resistor (estimating sum of L_{DCR}, pass device resistances, etc.). This technique is quite practical for buck-boost converters where the pass device resistances dominate and which are easy to replicate on-chip, but specifically for boost converter applications where the pass device resistance is considerably less and L_{DCR} varies, a technique which is not affected by parasitic resistors is desirable. Such a technique is presented by [12]. This technique is based on the solution of (6.6) with analog components. Equation (6.6) can be re-written having V_{in} on the right side of the equation as follows:

$$V_{out}(1-D) > \frac{V_{in}}{2} \tag{6.11}$$

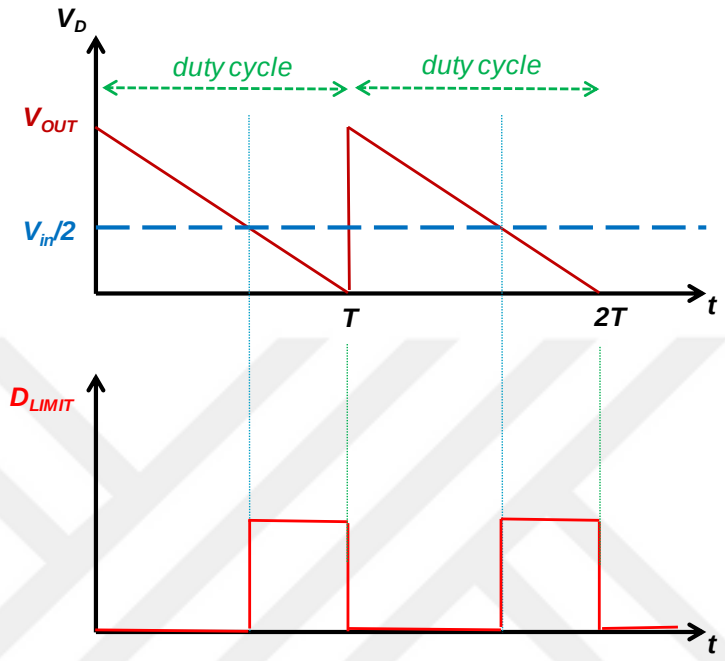


Figure 6.6. Graphical representation of Equation (6.11).

Figure 6.6 gives a graphical representation of Equation (6.11). In the upper plot, V_D voltage represents $V_{out}(1-D)$, which can be implemented with a sawtooth signal generator. In circuit implementation, a comparator will compare $Vin/2$ with V_D, preferably with some margin and will generate a logic signal which limits the duty cycle.

The circuit implementation and associated simulations are carried out from the example of a boost converter; however, this technique is also applicable to buck-boost converters. Figure 6.7 gives the circuit implementation utilizing the mentioned features.

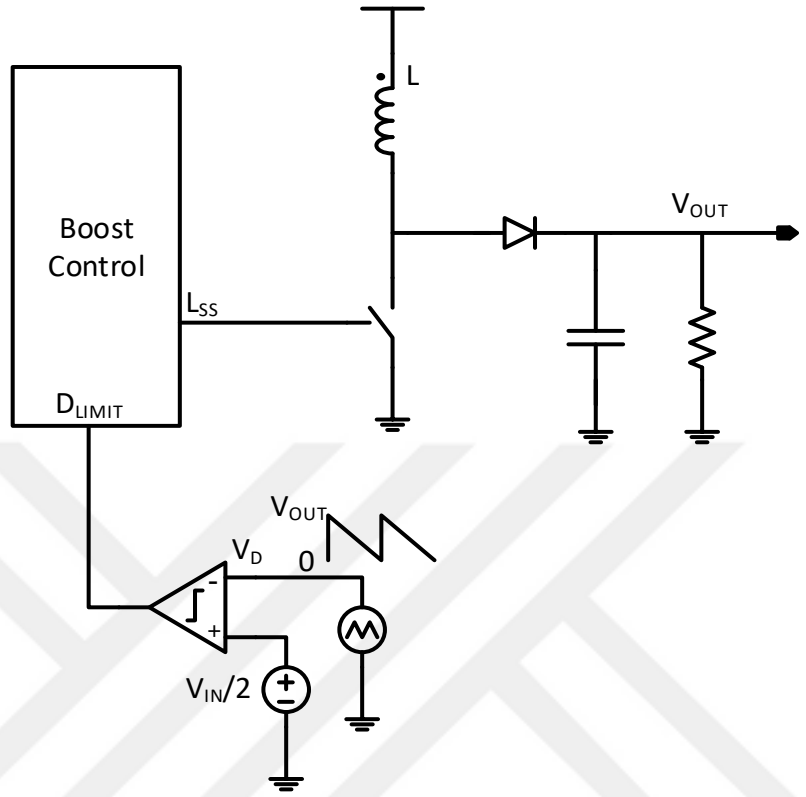


Figure 6.7. Block diagram of the circuit implementation.

The upper part of the block diagram describes a boost converter together with inductor *L*, load *R*, and switches. In the bottom part of block diagram, a comparator compares *Vin/2* with V_D. The comparator generates a logic signal D_{limit} which limits the duty cycle through the switching converter control logic.

It can be observed that only two inputs are needed to generate D_{limit}: The actual output voltage V_{OUT} and the switching period information. The result inherently compensates for temperature and process variations and any other parasitic resistances in series with *L*. This will result in a wide operation range of the switching converter with a variety of internal and external component selections.

Various methods can be utilized to generate the V_D voltage. A possible implementation can be converting V_{OUT} to a current V_{OUT}/R_D and extracting a sawtooth

shaped current from V_{OUT}/R_D called I_{SAW}. I_{SAW} will be 0 at start of duty cycle and will equate to V_{OUT}/R_D at the end of duty cycle. The resulting current can be multiplied by R_D to generate V_D as defined in Equation (6.12):

$$V_D = R_D\left(\frac{V_{out}}{R_D} - I_{SAW}\right) = \frac{V_{in}}{2} \tag{6.12}$$

6.3.1. Simulation Results

Figure 6.8 gives simulation results for a boost converter with V_{IN}=2.5V, f_{clk}=3MHz. At simulation time 100μs, the load current starts to increase and the output voltage starts to fall. When the load current increases, the control voltage V_{ERROR} will increase and the duty cycle will increase but will be limited with D_{limit}. This is the region where the protection circuitry starts to work, limits the duty cycle, and the output voltage does not collapse.

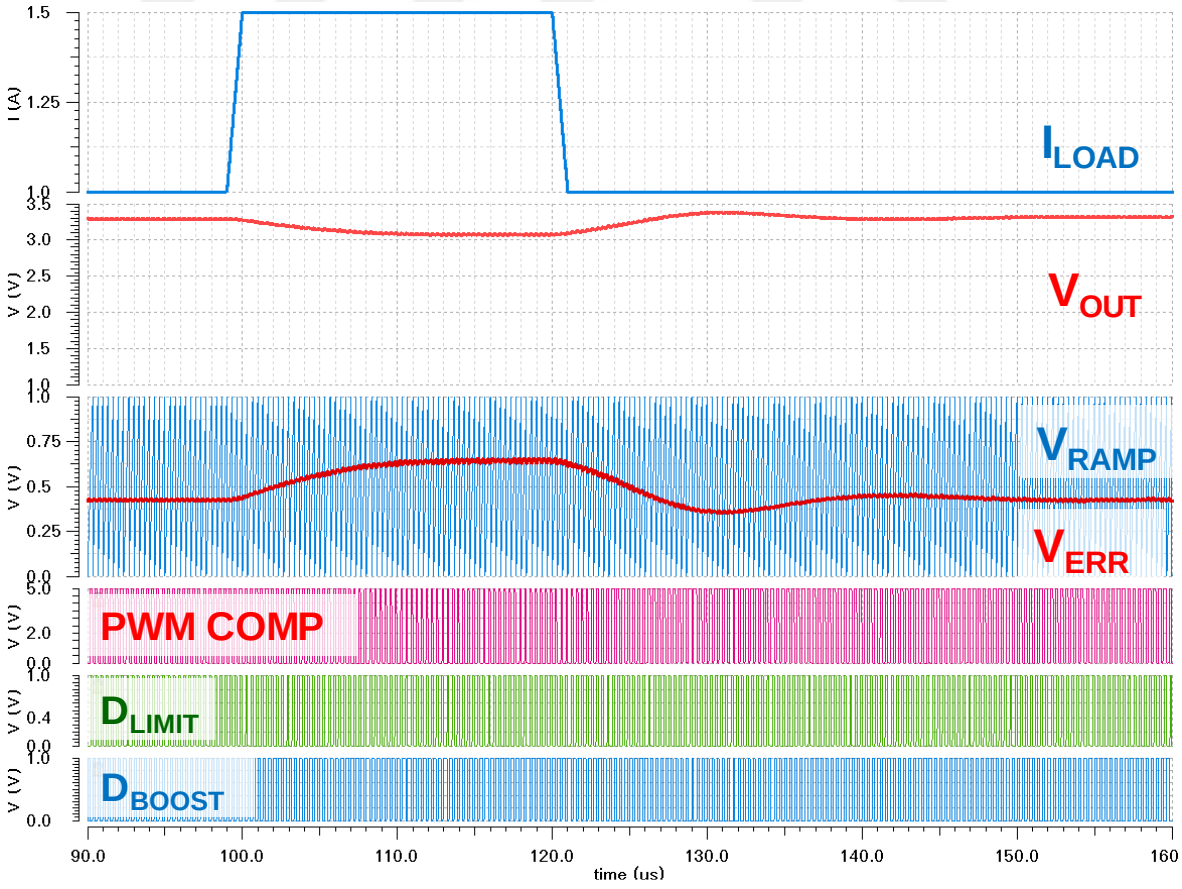


Figure 6.8. Simulation results with the proposed protection.

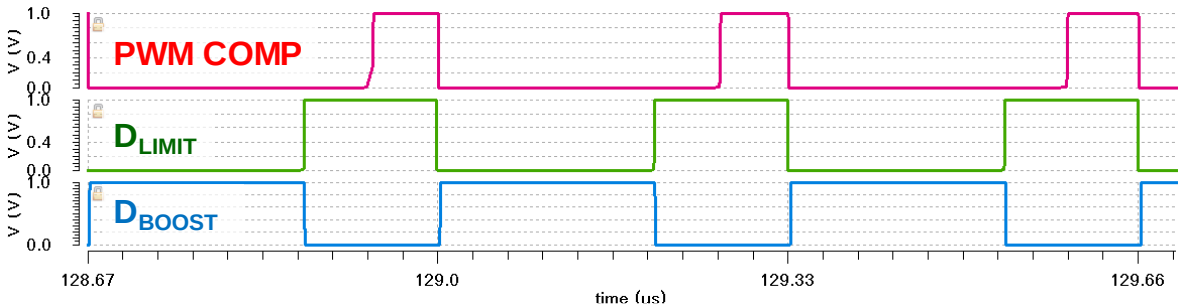


Figure 6.9. Simulation results with proposed protection – zooming on logic signals.

Figure 6.9 gives the results from the same simulation, zooming on logic signals. The duty cycle starts with the rising edge of D_{BOOST} , which also shows the time when the pass device switch is on. Under typical operation conditions D_{BOOST} will be ON until the rising edge of the PWM comparator. However, in the figure it is seen that even though PWM comparator output stays low (asking for a longer duty cycle), D_{BOOST} returns to zero with D_{LIMIT} signal. Here D_{LIMIT} signal is generated by comparing V_D (magenta) and $V_{IN}/2$. At the time D_{LIMIT} becomes high, the switching converter control logic turns off the pass device. Thus, the inductor current starts to decrease until the next clock signal.

6.4.Conclusion

Two novel techniques providing adaptive solutions to eliminate the lock-out mechanism by limiting the duty cycle of the switching converter are presented in this chapter. Owing to adaptive implementation, the resulting system is more flexible with limited circuit spread. The mentioned technique can also be regarded as a protection circuit, making sure the control loop to always be in the positive slope range. This protection mode can turn on during load/line transients, this is expected and desirable as a part of system operation.

7. CONCLUSION AND FUTURE WORK

In this thesis, first, a technique to improve efficiency of a buck converter using an adaptive pass device is presented. The proposed technique achieves optimum efficiency in any given and varying supply, load, temperature, process, and aging conditions by adjusting the selected number of switching segments, such that the cumulative capacitive and resistive power terms are minimized. A novel analog arithmetic function cell called the adaptive g_m stage is employed for calculating the power terms with low quiescent current. Owing to the simplicity and adaptivity of the introduced analog power loss equalization technique and low quiescent current consumption of the system, high power efficiency operation even in low load currents is achieved.

In PWM mode, the proposed converter can supply a load current ranging from 10mA to 1.5A with 80% minimum power efficiency at low load currents and 93% peak efficiency in typical operating conditions. Compared to the conventional buck converter with fixed output stage, simulation results show a 5% efficiency increase in mid load regime and 35% efficiency increase in low load regime in typical operating conditions. Compared to other reported adaptive pass device buck converters, this work achieves higher power efficiency values for PWM mode switching considering both peak and minimum efficiencies, with three times broader load current range in PWM mode. The proposed technique steps out as an alternative solution to sleep mode in the low/mid load region with no EMI issues.

Future work on this technique will be applying the demonstrated procedures to other applications where a trade-off between resistive and capacitive power loss exists. An example application is the capacitive charge pump where large width switches are employed to transfer charge from and to the flying capacitor.

A next achievement of the thesis is a charge recycling technique for single inductor dual output (SIDO) buck converters. Simulation results show that the proposed architecture achieves double polarity operation by re-using the charge stored in the output capacitors.

Following that, two control techniques for buck-boost converters have been proposed. The hysteretic control buck-boost steps out as a low power solution owing to its simplicity in topology. The improved current mode control technique utilizing separated buck and boost pulses demonstrates continuous mode transitions and immunity to sub-harmonic oscillation.

Finally, two techniques addressing the lock-out phenomenon occurring in boost and buck-boost converters have been proposed. The techniques aim at sensing the peak of the voltage conversion vs. duty cycle curve and limiting the duty cycle accordingly, thus preventing a lock-out event. Simulation results demonstrate that the techniques provide adaptive and flexible solutions increasing operational range and reliability of the switching converter.

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APPENDIX A: LAYOUT OF THE ADAPTIVE BUCK CONVERTER

The layout of a switching converter is the design stage that needs the most careful attention, as without proper security implementations, the switching converter IC will most likely fail due to process related mechanisms such as snapback or latch-up, or alternatively the chip will suffer from electromigration due to poor metal layer width sizing.

This section gives the layout of the building blocks of the buck converter with adaptive pass device, together with a brief description on layout implementation.

A.1. Adaptive g_m Cells

There are two implementations of adaptive g_m cells. The capacitive adaptive g_m block – solving the left side of Equation (3.11) has input voltages referenced to ground, and uses a PMOS input differential pair, as given in Figure 3.4. The compete layout of the capacitive adaptive g_m cell is given in Figure A.1 [42].

Figure A.2 gives transistor placement detail of the capacitive adaptive g_m block, with metal-insulator-metal (MIM) cap layers turned off for better visibility. Dummy transistors are placed at both ends of the differential pairs and current mirrors. Antenna diodes are placed at gate pins. The input differential pairs are surrounded with NWELL guard rings and PTAP guard rings to reduce bulk resistance and to reduce substrate noise coupling.

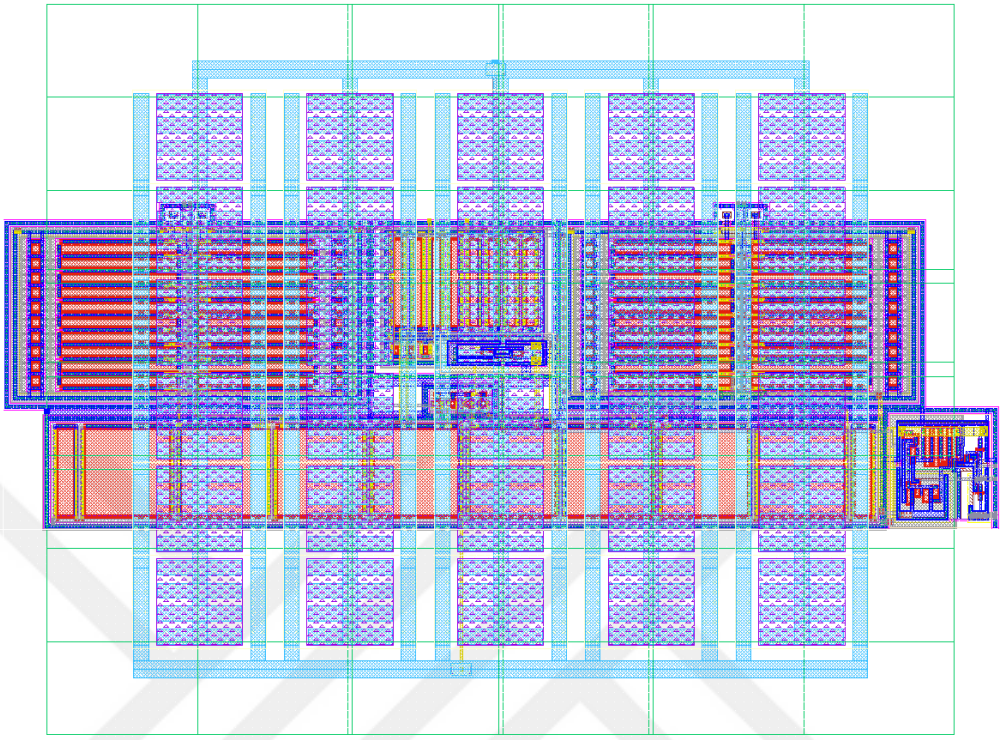

Figure A.1. Complete layout of capacitive adaptive g_m block [42].

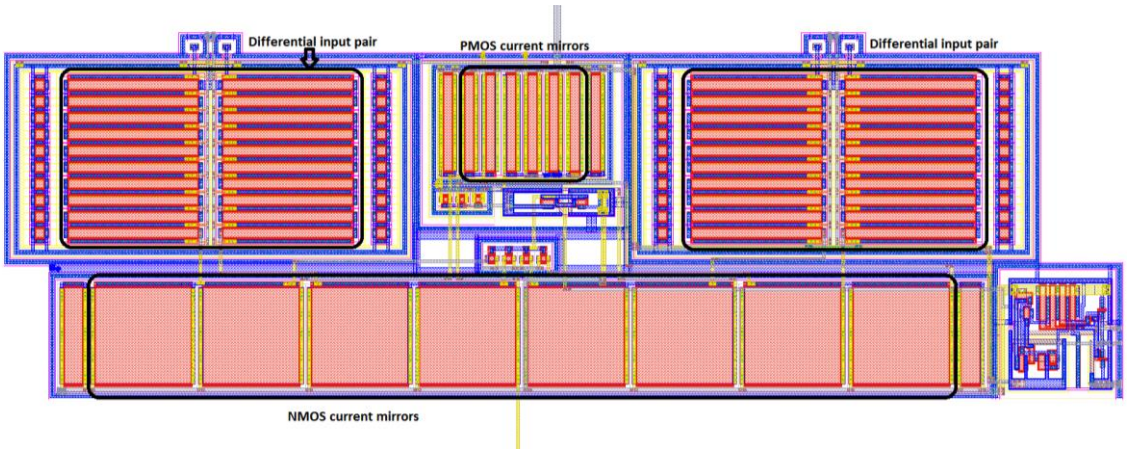

Figure A.2. Transistor placement detail of capacitive adaptive g_m block [42].

The resistive adaptive g_m block – solving the right side of Equation (3.11) has input voltages referenced to input supply, and uses a NMOS input differential pair, as given by Figure 3.6. The compete layout of the resistive adaptive g_m cell -excluding MIM caps- is given in Figure A.3 [42].

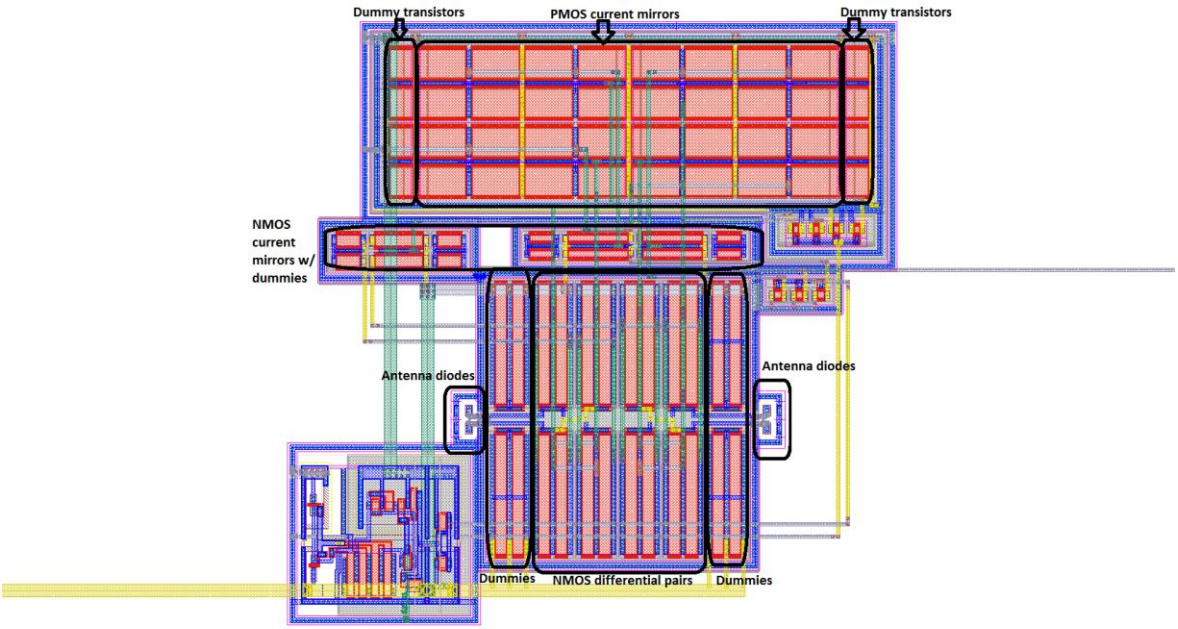

Figure A.3. Resistive adaptive g_m cell [42].

A.2. Voltage Sense

The layout of the voltage sense block is given in Figure A.4 [42]. A transmission gate, a buffer, and an inverter for driving the gates of the sampling transmission gate, and the hold capacitor is observed.

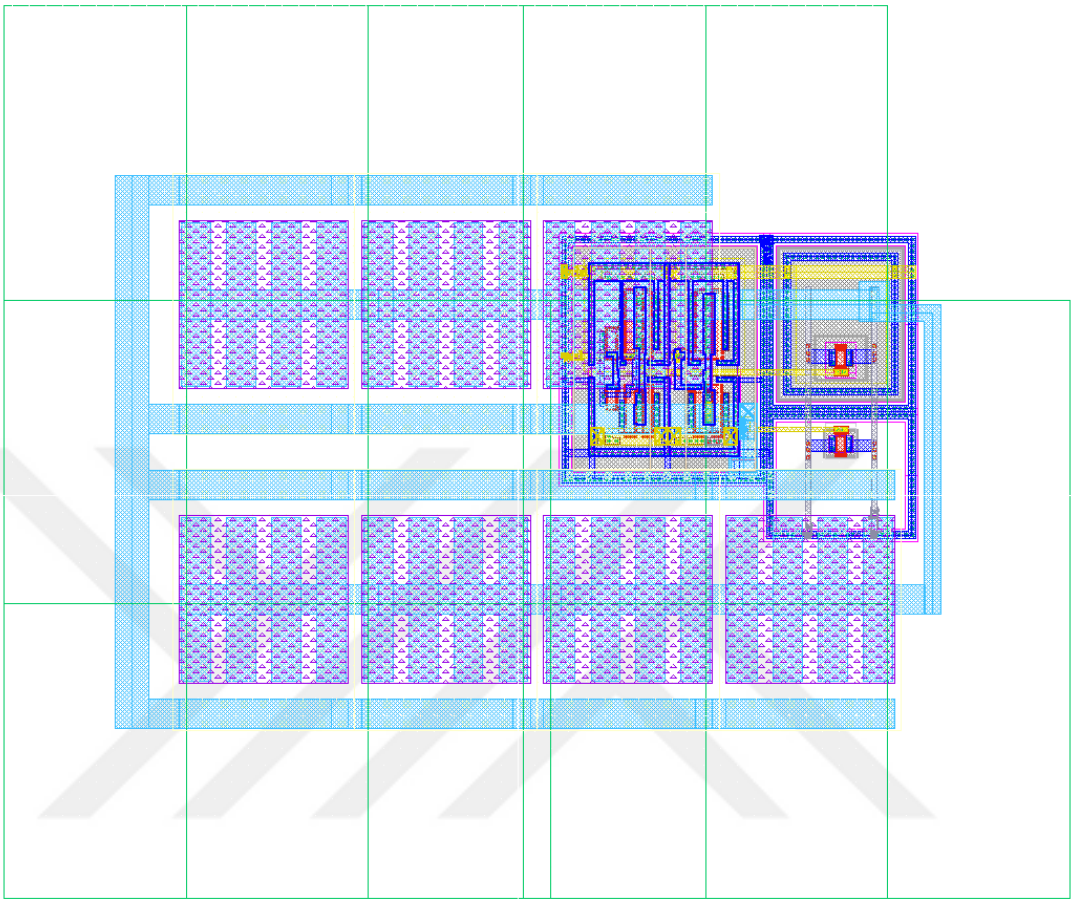

Figure A.4. Voltage sense block [42].

A.3. Error Amplifier

Layout of the error amplifier is given in Figure A.5 [42]. PMOS current mirrors are placed on the upper half of the layout while NMOS current mirrors are placed on the lower end of the layout. PMOS differential input pair is placed in the middle. ABABABABAB placement is used for the input differential pair, together with two dummies on each side, for improved matching. Logic gates are placed at empty spaces around the differential pair.

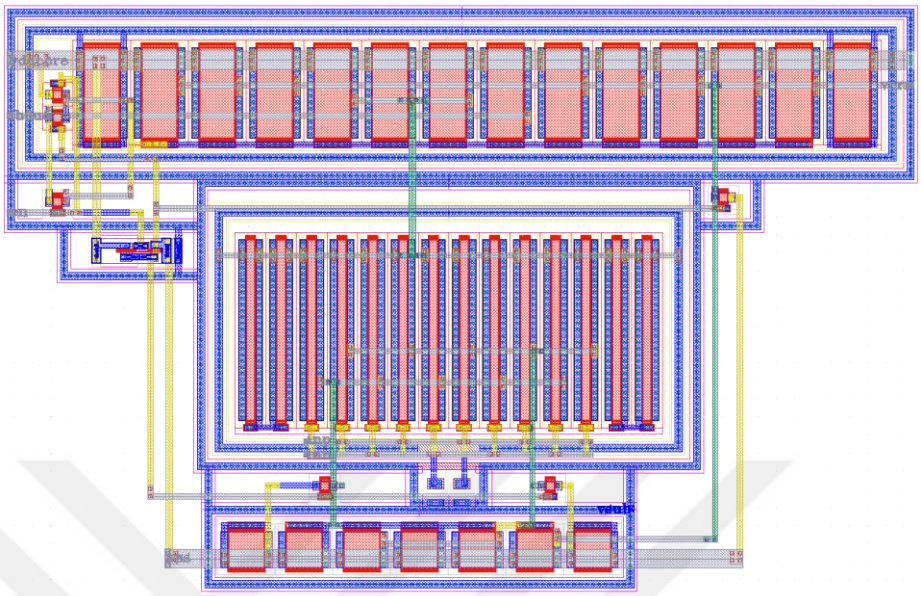

Figure A.5. Layout of the error amplifier [42].

A.4. PWM Comparator

Layout of the PWM comparator is given in Figure A.6 [42]. PMOS input differential pair is placed at lower left, PMOS current mirrors are placed on the upper half and NMOS transistors are placed at lower half of the layout. Logic blocks are placed at the available space in between. The input differential pair is laid out as common-centroid structure. Dummy transistors are located at both edges with same distance as the active transistors. Around the block NWELL guard ring and PTAP guard rings are placed.

A zoom-in to input stage is given in Figure A.7 [42]. Input differential pair is laid out by using common centroid and cross quad structure using dummy transistors on each side, hence leading to more complex connections.

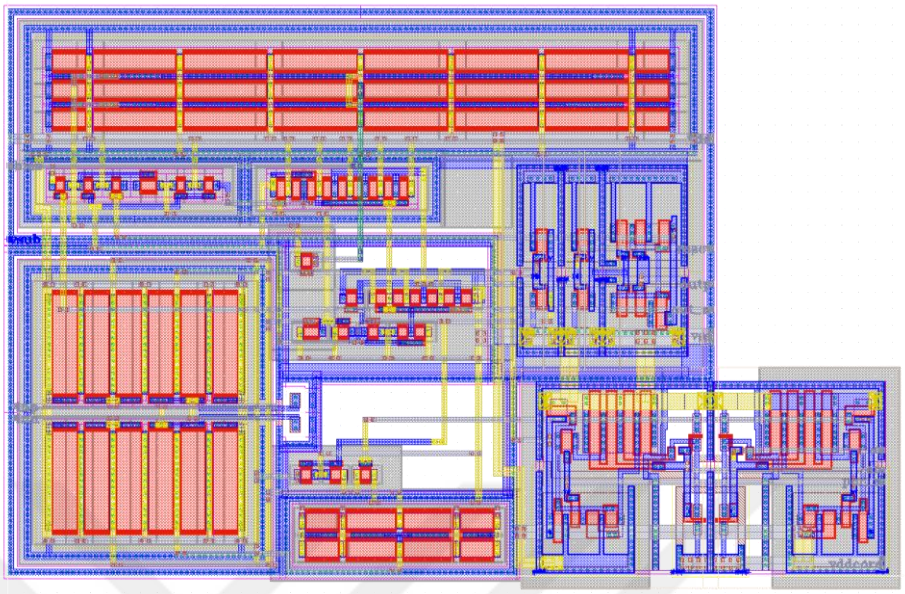

Figure A.6. Layout of the PWM comparator [42].

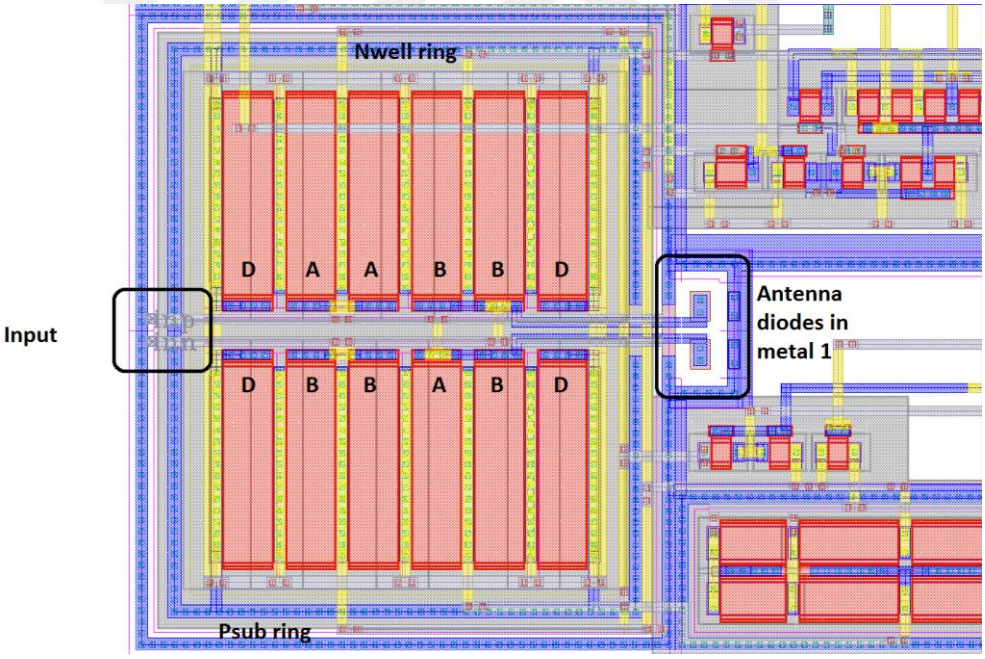

Figure A.7. Zoom-in to PWM comparator [42].

A.5. Ramp Generator

The layout of the ramp generator is given in Figure A.8 [42]. Dummy transistors are connected on each sides of the current mirrors. The MIM capacitor storing the ramp voltage is located on the upper half of the layout (not shown for improved visibility of base layers).

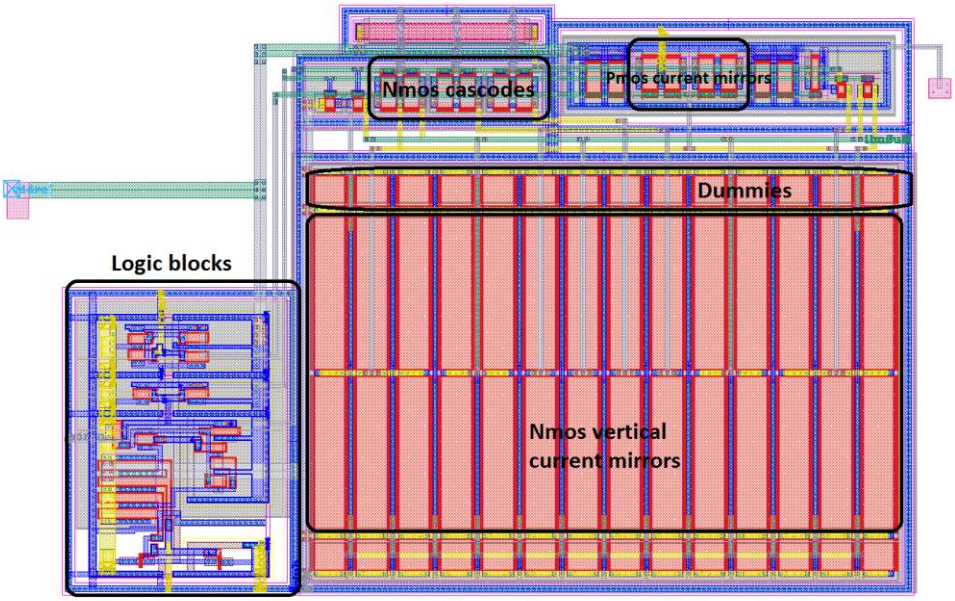

Figure A.8. Layout of the ramp generator [42].

A.6. Active Diode

The layout of the active diode comparator is given in Figure A.9 and Figure A.10 [42]. Placement of current mirrors, differential pairs, serial resistors, NMOS switches, first and second gain stages, and logic circuitry can be seen in Figure A.9.The input differential pair blocks are laid out such that diffusions and dummies are shared at both ends – using ABAB matching structure.

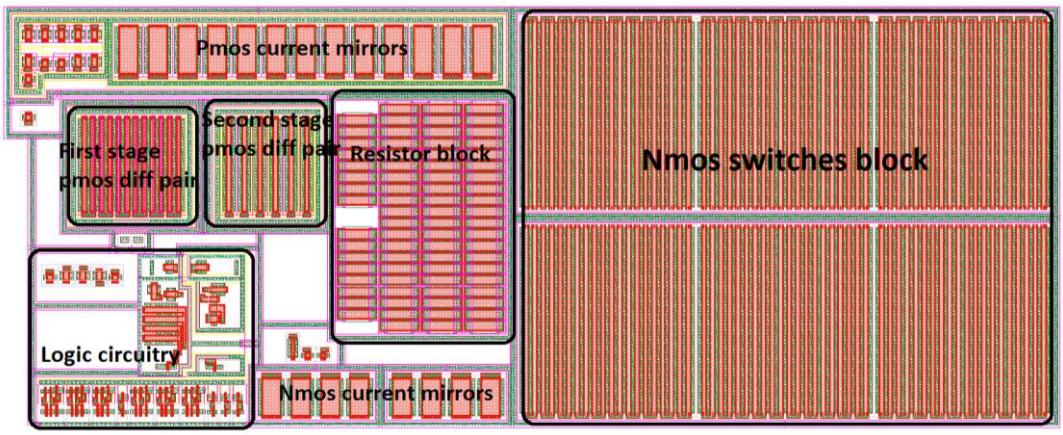

Figure A.9. Layout of the active diode comparator – base layers only [42].

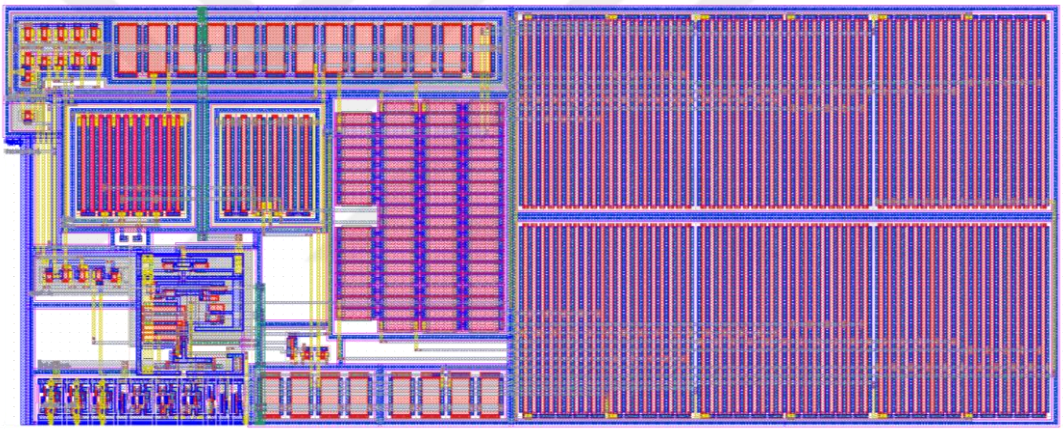

Figure A.10. Complete layout of the active diode comparator [42].

A.7. Pre-Driver

The layout of the pre-driver including *Noff* and *Poff* blocks and non-overlapping logic cells are shown in Figure A.11 [42]. At the top level, this block is instantiated for each unit pass device so that 32 replica pre-drivers will be observed.

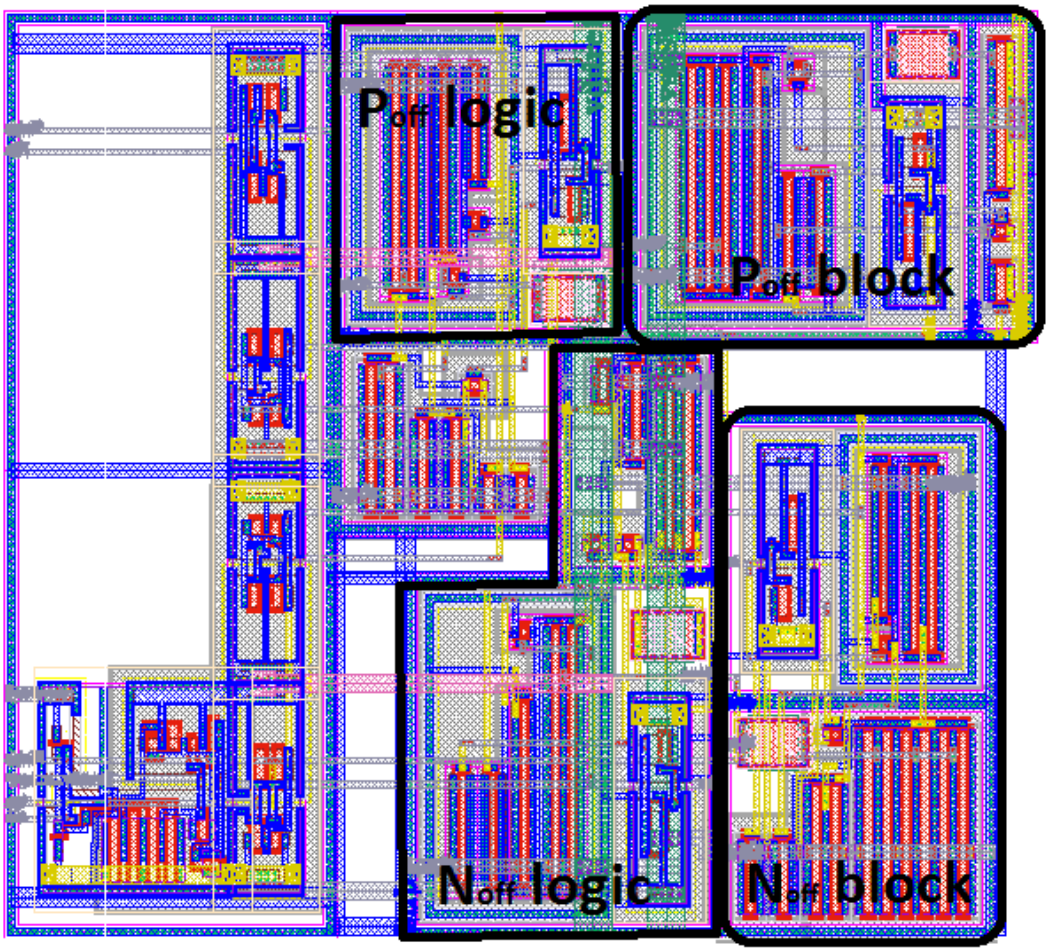

Figure A.11. Layout of the pre-driver cell [42].