SUPER REGENERATIVE RECEIVER DESIGN FOR MEDICAL IMPLANT DEVICES

by

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SUPER REGENERATIVE RECEIVER DESIGN
FOR MEDICAL IMPLANT DEVICES

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ABSTRACT

SUPER REGENERATIVE RECEIVER DESIGN FOR MEDICAL IMPLANT DEVICES

Implant devices are one kind of the state-of-art medical equipment, which have been started to be used widely in diagnosis and treatment. Implanted devices require wireless data transfer for the comfort of patients and ease of the operation. Since these devices are powered remotely or by a battery, low power operation is crucial to eliminate the need for any surgical intervention to maintain the functionality. The most power-hungry block in these devices is mostly the RF front-end. Super-regenerative receiver architecture overcomes high power consumption requirement by means of quenching the local oscillator that consumes most of the front-end power. Quenching the oscillator makes it possible to use almost-infinity gain at the start-up to regenerate the received weak signal. The super-regenerative reception theory is explained in detail and two super-regenerative receivers are proposed in this thesis work. The first receiver employs passive inductors; hence, an on-chip inductor was designed to be used in MedRadio band. On the other hand, the second receiver uses only inductorless architectures. For the second receiver, an active inductor was designed to emulate the inductance needed for the frequency selective circuitry. All designs were laid out, fabricated, and characterized. Comparison of the schematic and the post-layout simulation results are provided along with the performance comparison of silicon measurements with the previous work. Finally, a brief conclusion is drawn and perspective for future work is presented.

ÖZET

TIBBİ İMPLANT CİHAZLARI İÇİN SÜPER REJENERATİF ALICI TASARIMI

İmplant cihazları, teşhis ve tedavide yaygın olarak kullanılmaya başlanan son teknoloji tıbbi ekipmanlardan biridir. İmplante edilmiş cihazlar, hastaların rahatı ve kullanım kolaylığı için kablosuz veri aktarımı gerektirir. Bu cihazlar uzaktan veya bir batarya aracılığıyla çalıştırıldığından, çok düşük güç tüketimi, işlevselliği korumak için herhangi bir cerrahi müdahaleye olan ihtiyacı ortadan kaldırmak için çok önemlidir. Bu cihazlarda en çok güç tüketen blok çoğunlukla RF ön-uçtur. Süper rejeneratif alıcı mimarisi, ön-uç gücün çoğunu tüketen yerel osilatörü kapatıp açmak yoluyla yüksek güç tüketiminin üstesinden gelir. Osilatörün kapatılıp açılması, alınan zayıf sinyali yeniden oluşturmak için osilasyon başlangıcındaki neredeyse sonsuz olan kazancın kullanılmasını mümkün kılar. Süper rejeneratif alım teorisi ayrıntılı olarak açıklanmış ve bu tez çalışmasında iki süper rejeneratif alıcı önerilmiştir. İlk alıcı pasif indüktörler kullanır; bu nedenle, MedRadio bandında kullanılmak üzere çip üzerinde bir indüktör tasarlanmıştır. Öte yandan, ikinci alıcı sadece indüktörsüz mimariler kullanır. İkinci alıcı için, frekans seçici devre için gereken indüktansı taklit etmek üzere bir aktif indüktör tasarlanmıştır. Tüm tasarımların serimi yapılmış, tüm tasarım üretilmiş ve karakterize edilmiştir. Şematik ve serim-sonrası simülasyon sonuçlarının karşılaştırılması, silikon ölçümlerinin önceki çalışmalarla performans karşılaştırmasıyla birlikte sunulmuştur. Son olarak, kısa bir sonuç çıkarılmış ve gelecekteki çalışmalar için bakış açısı sunulmuştur.

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LIST OF SYMBOLS

A_v	Voltage gain of an amplifier
C	Capacitance
d	Diameter
e^i	e to the power i
f	Frequency in Hertz
F	Noise factor
g_m	Transconductance
G	Transconductance
G_v	Overall voltage gain of an amplifier
$G(t)$	Time-varying conductance
$i(t)$	Time-varying current
$\dot{i}(t)$	First derivative of current
$\ddot{i}(t)$	Second derivative of current
j	Imaginary number
k	Boltzmann Constant
L	Inductance
n	Slope correction factor of a MOSFET
$p(t)$	Oscillation envelope
Q	Quality factor of an inductor
R	Resistance
r_{oi}	Output resistance of MOSFET i
$s(t)$	Sensitivity
t	Time variable
T	Temperature in Kelvin
$v(t)$	Time-varying voltage
V_i^*	Complex conjugate of voltage i
$\dot{v}(t)$	First derivative of voltage
$\ddot{v}(t)$	Second derivative of voltage

w	Width
Z	Impedance
β	Transconductance coefficient
∂	Partial derivative
γ	Gamma factor of thermal noise in a MOSFET
λ	Integration variable
ω	Angular frequency in radians per second
τ	Integration variable
$\zeta(t)$	Time-varying damping factor

LIST OF ACRONYMS/ABBREVIATIONS

3D	3 Dimensional
AC	Alternating Current
ADE	Analog Design Environment
AI	Active Inductor
ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for Integrated Circuits
CCC	Capacitive Cross-Coupled
CGLNA	Common-Gate Low-Noise Amplifier
CMOS	Complementary Metal-Oxide-Semiconductor
CSF	Cerebrospinal Fluid
CSLNA	Common-Source Low-Noise Amplifier
DC	Direct Current
DFF	D Flip-Flop
EEG	Electroencephalography
EM	Electromagnetic
ESD	Electrostatic Discharge
FCC	the U.S. Federal Communications Commission
FOM	Figure-of-Merit
IC	Integrated Circuit
iEEG	Intracranial Electroencephalography
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low Noise Amplifier
MedRadio	Medical Device Radiocommunications Service
MIM	Metal-Insulator-Metal
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NA	Not Available
NF	Noise Figure
NMOS	N-Channel Metal-Oxide Semiconductor

ODE	Ordinary Differential Equation
OOK	On-Off Keying
PCB	Printed Circuit Board
PDK	Process Design Kit
PGS	Patterned Ground Shield
Ph. D.	Doctor of Philosophy
PMOS	P-Channel Metal-Oxide Semiconductor
PRIME	Conference on Ph. D. Research in Microelectronics and Electronics
RF	Radio Frequency
SGS	Solid Ground Shield
SNR	Signal-to-Noise Ratio
SRO	Super Regenerative Oscillator
SRR	Super Regenerative Receiver
UMC	United Microelectronics Corporation
U.S.	United States
VLSI	Very Large Scale Integration

1. INTRODUCTION

1.1. Motivation

Recent advances in technology has introduced new diagnosis and treatment methods in the field of medicine. Implant devices are one type of the state-of-art medical equipment, which has started to be used widely. These devices include implanted cardiac pacemakers and defibrillators as well as neuromuscular stimulators that help restore sensation, mobility, and other functions to limbs and organs (see Figure 1.1).

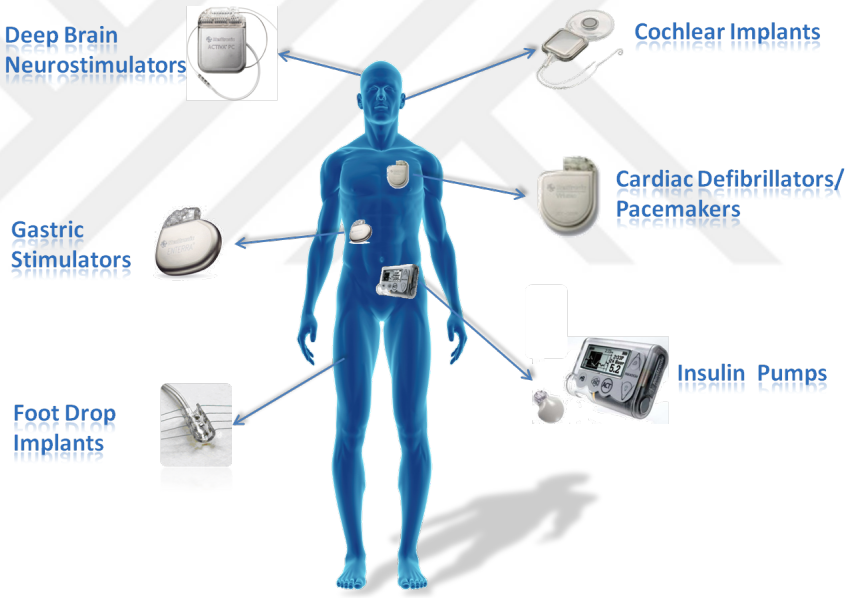


Figure 1.1. Usage areas of medical implant devices [1].

Wearable sensors and implanted devices require wireless data transfer for the comfort of patients and ease of operation. Since these devices are operated from a battery or powered remotely, the main bottleneck in their design is power consumption. The most power-hungry block in these devices is mostly the RF front-end. Commonly used receiver types, such as direct-conversion [7] and superheterodyne [8] architectures, employ continuously running local oscillators which themselves dissipate most of the power. Super-regenerative receiver (SRR) architecture, which was first proposed in

1913 by E. H. Armstrong [9, 10], offers a solution to this very problem. A generic block diagram of an SRR is depicted in Figure 1.2. In the SRR architecture, the local oscillator is periodically turned on and off, in other words, quenched. This operation enables the system to use the high non-linear gain of the oscillator at start-up to regenerate the received weak signal and obtain a strong enough signal to be processed by the following blocks. Thanks to quenching, the power consumption of the SRR architecture achieves much lower levels than that of other types of receivers. Unlike other receiver architectures [7, 8] in which the LNA output is fed to a mixer along with the local oscillator output, the LNA output is directly injected into the oscillator output in the SRR architecture. We obtain oscillation only if there exists a tuned excitation injected by the LNA, which is called super-regeneration.

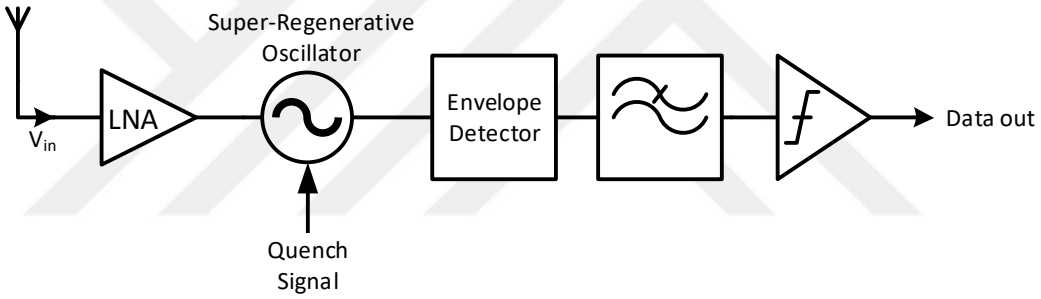


Figure 1.2. Generic block diagram of a super-regenerative receiver.

The SRR architecture was abandoned after the 1950s for a long time because of its lack of sensitivity. Other aforementioned architectures became more popular along with the advances in CMOS technology since they achieve much better sensitivity levels then the SRR. However, better sensitivity comes with the cost of higher power consumption. Strict power consumption requirements of the battery-powered systems and the first regulation on medical implants made by the U.S. Federal Communications Commission (FCC) in 1999 [11] drew the attention back on the SRR [12–14]. Regulations were finalized under the name of Medical Device Radiocommunications Service (MedRadio) in 2014 [15].

Super-regenerative receiver solves the battery lifetime problems and makes remote powering possible. Additionally, low sensitivity drawback of the SRR can be tolerated

since medical applications require close-range communication to establish a wireless link with the main station. The main motivation behind this thesis is, as an addition to the new regulations made for MedRadio, these suitable characteristics of super-regenerative receivers for implanted or wearable medical devices. Hence, the comfort of patients would be improved, the need for surgical operations to maintain the functionality of the implant would be decreased or may even be eliminated, and better life quality would be maintained.

1.2. Objective of the Thesis

This thesis work was performed as a part of the continuation of the project presented in [5, 16]. The problem described in [5] can be briefly stated as establishing a wireless link between the brain implant and the main station for epilepsy monitoring in order to get rid of wires in present wired systems. A study width the present wired system can be found in [2]. The clinical procedure they used to record electrical activities in the brain is called intracranial electroencephalography (iEEG). The system consists of the electrode array, wires, and the main station (see Figure 1.3). The biggest problem this system exhibits is the wired data transfer. From the electronics point of view, the closer the read-out circuitry to sensors, the better the signal acquisition. This is not the case in iEEG. From the medical point of view, wired connection creates the risk of cerebrospinal fluid (CSF) leakage or even worse, infection of the CSF.

Even though clinical scalp electroencephalography (EEG) is non-invasive, iEEG has started being used widely in epilepsy monitoring since it enables recording of higher frequency oscillations which give an insight into the electrical mechanisms underlying epilepsy [3].

A solution to the aforementioned disadvantages of iEEG while maintaining all the functionality is to have better sensors and wireless data transfer. Utah electrode array which is making use of the power of integration is shown in Figure 1.4. This sensor integrates a large number of sensors and enables simultaneous monitoring of many neurons, which solves the problem with sensor quality and density. Further studies

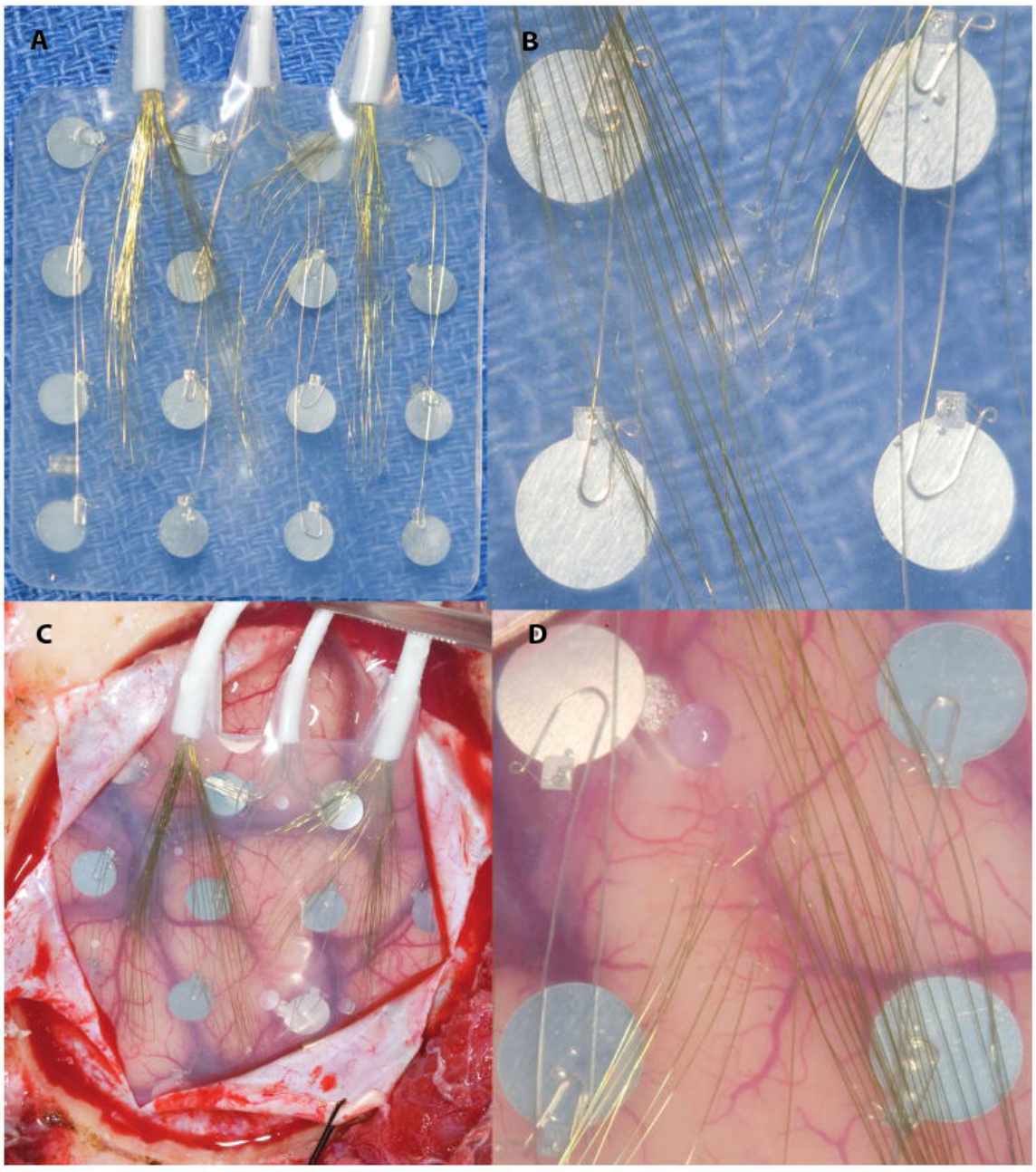


Figure 1.3. Schematics of a 1x4 contact strip with 32 micro-wires (A), a hybrid 4 x 6 grid with 104 micro-wires (B), and a hybrid 4 x 4 grid with 112 micro-wires (C). Clinical macro-contacts are 4-mm diameter and spaced 10-mm center-to-center [2].

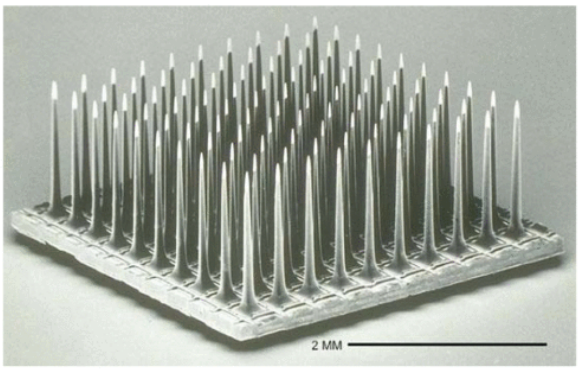


Figure 1.4. Scanning electron micrograph of silicon-based Utah electrode array [3, 4].

have been done on integrating the sensor interface, and there are successful examples in the literature [17], which solves the problem with the wired connection between the sensor array and the read-out circuitry and makes it possible to locate the read-out circuits physically very close to the sensor. The final issue, which is the data transfer between the base and the implanted system, can be solved by means of wireless data transfer solutions. This thesis work aims to solve the last problem stated. The general structure of the final system is shown in Figure 1.5.

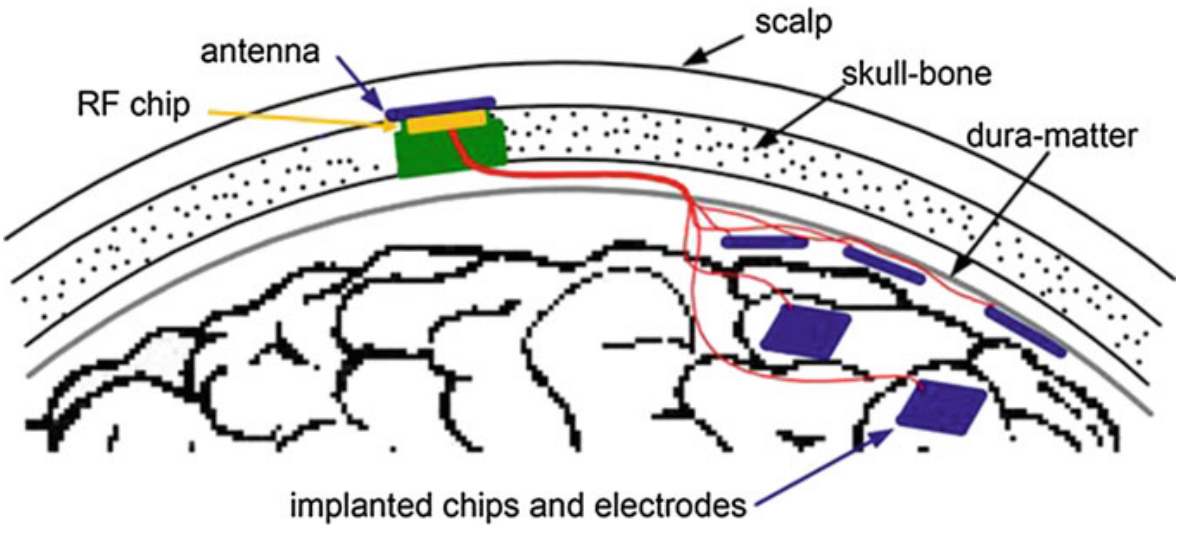


Figure 1.5. Schematics of the implanted system; here, five recording-integrated circuits are depicted on the surface of the cortex, in dark blue; these units are connected through a wire (red) to the RF chip (orange) [5].

As mentioned above, medical diagnosis and treatment technology follows a path to improve the comfort of the patient and avoid surgical incision as much as possible. Wireless powering of implants and wireless data link between implants and the main station is the best solution to prevent surgical interventions to maintain normal operation of implants. Moreover, this method of operation is also easier to perform for the operator that generally has a medical background rather than a technical background such as electronics. The thesis work proposes two low power wireless receivers for brain implants to monitor and intervene epileptic seizures as shown in Figure 1.5.

Both of the receivers proposed in the thesis are super-regenerative receivers. The first receiver consists of commonly used sub-blocks, some of which employ inductors. The second receiver consists only of inductorless sub-blocks. It employs an active inductor circuit which emulates the behavior of a passive inductor.

Passive inductors are well-understood and well-modeled components and are straightforward to use in designs. They maintain linear behavior even in high power conditions. Yet, they are not suitable for scaling. The smaller the inductor, the worse the performance and the lower the operating frequency, the bigger the required inductance value. Therefore, they occupy large areas on the die when integrated especially at MedRadio frequencies [15]. When integrated, because of the lossy silicon substrate, inductors exhibit very high losses, and therefore very low quality factors. Furthermore, inductors create magnetic fields which couple with other circuitry on the same die and degrade the performance of the system and sometimes drive the circuit to instability because of the unwanted feedback path stems from this coupling effect.

To sum up, the objective of the thesis can be stated as the design of super-regenerative receivers to be used in medical implant devices. Because of the aforementioned advantages of passive inductors, an SRR employing passive inductors and because of the aforementioned disadvantages, an inductorless SRR are presented in the thesis.

1.3. Contributions and Organization of the Thesis

The idea of using the SRR architecture for medical implants is not new, yet one that has not been investigated deeply, to the best of author's knowledge. There are only a few examples in the literature using this architecture for this purpose. Since the application only requires close-range wireless communication, the low sensitivity of the SRR architecture, which was the main reason why this architecture lost the attention in history, is not presenting a bottleneck here.

Design of two super-regenerative receivers is the main accomplishment in this thesis. The highest novelty is presented in the idea of an inductorless SRR. To the best of author's knowledge, there is no another example of such an SRR presented in the literature.

In the thesis work, *UMC 180nm CMOS* fabrication process was used. System-level modeling of the SRR architecture was performed and published in *2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)* [18] and in *Integration, the VSLI Journal* [19]. Since there was no appropriate inductor provided in the fabrication technology's process design kit (PDK), an on-chip inductor was designed to be used in the MedRadio band. Using this model and the inductor, an SRR was designed, laid out, fabricated, and tested. An active inductor was designed and an inductorless SRR was designed using this active inductor, laid out, fabricated, and tested.

This thesis is organized as follows. In Chapter 1, a summary of needs in medical implant devices is provided as well as the objective of the thesis and contributions made to literature. In Chapter 2, background knowledge on the theory of super-regenerative reception is provided. Chapter 3 presents system-level modeling of a generic SRR architecture. The mathematical procedure of the modeling and performance comparison of the model with real circuit simulations are provided in this chapter. Chapter 4 presents the analysis, design, and layout of each sub-block in the receiver that employs inductors. Test results of the SRR with inductors are presented and a conclusion is

drawn at the end of the chapter. Chapter 5 provides analysis, design, and layout of each sub-block in the inductorless receiver. This chapter is also concluded with test results and comments. Last but not least, Chapter 6 draws a general conclusion of the thesis and explains the future work to take the research performed in this work a step further.

2. BACKGROUND

In the reception of an RF signal, the goal is to amplify received ultra-weak signal in a limited bandwidth by adding as low noise as possible. For this purpose, low-noise amplifiers are employed at the beginning of the receiver chain since the first block is the most critical block in terms of the noise performance of the overall system. Afterwards, the amplified signal is down-converted and some signal processing is performed to obtain the received data. In classical receiver architectures, amplification is performed via amplifiers and down-conversion is performed through a mixer and a local oscillator.

In super-regenerative reception, the oscillator is periodically turned on and off, in other words, quenched. Since the oscillator is used for super-regeneration, it is called super-regenerative oscillator (SRO). There are two modes of operation in the super-regenerative reception, namely linear and logarithmic modes. Unlike the most common receiver architectures [7, 8] which employ free-running oscillators, the SRO is not allowed to reach the saturation amplitude in the linear mode of operation. There is an oscillation only if there exists an RF excitation. This mode is named as the linear mode since the maximum oscillation amplitude has a linear relationship with the RF excitation amplitude. In the logarithmic mode on the other hand, the SRO is allowed to reach the saturation amplitude. Even if there is no RF excitation, oscillation reaches saturation. When an RF excitation is present, oscillation builds up faster, which yields longer oscillation time in one quench period. The duration of the oscillation is logarithmically related to the initial RF excitation, which gives this mode its name. The response of the SRO in the logarithmic mode is governed by a nonlinear variable coefficient ordinary differential equation whose analytic solution does not necessarily exist [20]. Thus, the linear mode of operation hereafter is explained mathematically.

2.1. Super-Regenerative Reception

In the SRO, thanks to the positive feedback, ultra-high gain of the oscillator at the start-up is used to regenerate received weak signal. The gain of the oscillator

loop is ultra-high, almost infinity, at the beginning of oscillation start-up, whereas as oscillation amplitude grows, large voltage swing causes non-linearities to start showing their effects and decreases the loop gain down to one which is the criterion of the sustained oscillation [21].

Operation of the SRR in the linear mode under square-wave and sinusoidal quench signals is illustrated in Figure 2.1a and Figure 2.1b, respectively. $i(t)$ is the RF excitation inserted into the SRO, $\zeta(t)$ is the damping factor in the SRO, $s(t)$ is the sensitivity curve of the reception, $p(t)$ is the normalized output envelope, and $v_{out}(t)$ is the SRO output voltage, all of which will be explained in detail later in this chapter. Time points illustrated as t_1 and t_2 are also important and will be used in the analysis below.

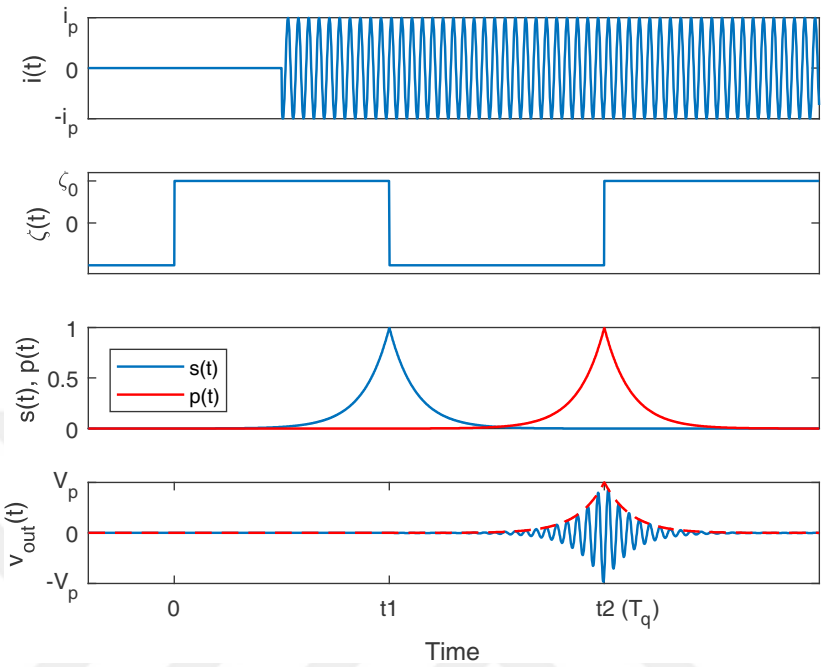
In order to understand the mechanism in the linear mode, the governing equation of the SRO must be found. Figure 2.2 shows a generic model of an SRO. L and C together form the resonant behavior which selects the oscillation frequency and G_0 is a positive conductance which models the loss in the LC tank. $-G_1(t)$ is a negative conductance which represents the active circuitry in the SRO. This negative conductance is varied by quench signal so that the SRO is turned on and off. $i(t)$ models RF excitation and $v(t)$ is the output voltage of the SRO.

The governing differential equation is obtained from the model as [20, 22]

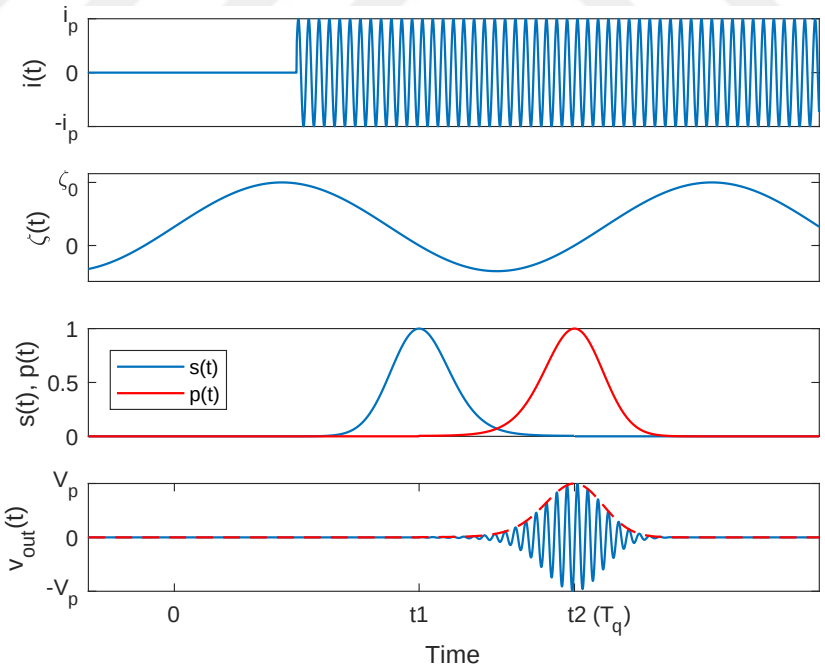
$$C\dot{v}(t) + G(t)v(t) + \frac{1}{L}\int v(t)dt = i(t) \tag{2.1}$$

where

$$G(t) = G_0 - G_1(t) \tag{2.2}$$



(a)



(b)

Figure 2.1. RF input signal $i(t)$, damping factor $\zeta(t)$, sensitivity curve $s(t)$, output envelope $p(t)$, and the SRO output voltage for (a) square and (b) sinusoidal quench.

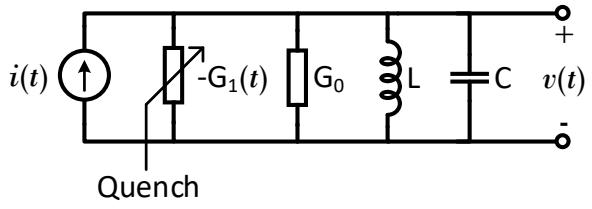


Figure 2.2. A generic model of a super-regenerative oscillator.

is the time-varying conductance of the LC tank. By differentiating both sides in Equation 2.1 and rearranging, the governing equation takes the following form

$$\ddot{v}(t) + \frac{G(t)}{C}\dot{v}(t) + \left(\frac{1}{LC} + \frac{\dot{G}(t)}{C}\right) v(t) = \frac{\dot{i}(t)}{C} \tag{2.3}$$

To gain more insight into the operation of the SRO, the above equation is converted to

$$\ddot{v}(t) + 2\zeta(t)\omega_0\dot{v}(t) + \left(\omega_0^2 + 2\omega_0\dot{\zeta}(t)\right) v(t) = \frac{\dot{i}(t)}{C} \tag{2.4}$$

where

$$\zeta(t) = \frac{G(t)}{2C\omega_0} \tag{2.5}$$

is the time-varying damping factor, and

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.6}$$

is the resonant frequency. Equation 2.4 is a second-order time-varying coefficient ordinary differential equation (ODE) and the solution is in the form of

$$v(t) = v_h(t) + v_p(t) \tag{2.7}$$

where $v_h(t)$ is the homogeneous solution and $v_p(t)$ is the particular solution of the governing equation.

Homogeneous equation of Equation 2.4 is obtained by assuming zero input as

$$\ddot{v_h}(t) + 2\zeta(t)\omega_0\dot{v_h}(t) + \left(\omega_0^2 + 2\omega_0\dot{\zeta}(t)\right) v_h(t) = 0 \tag{2.8}$$

To solve the above equation, it needs to be converted into the Hill equation. Conversion is performed by the method of change of variables with the relationship

$$v_h(t) = u(t)e^{-\omega_0\int_0^t \zeta(\tau)d\tau} \tag{2.9}$$

By differentiating the above equation once we obtain

$$\dot{v_h}(t) = \left[\dot{u}(t) - \omega_0\zeta(t)u(t)\right] e^{-\omega_0\int_0^t \zeta(\tau)d\tau} \tag{2.10}$$

and by differentiating twice we obtain

$$\ddot{v_h}(t) = \left[\ddot{u}(t) - 2\omega_0\zeta(t)\dot{u}(t) + u(t)\left(\omega_0^2\zeta^2(t) - \omega_0\dot{\zeta}(t)\right)\right] \times e^{-\omega_0\int_0^t \zeta(\tau)d\tau} \tag{2.11}$$

Substituting Equation 2.9, Equation 2.10, and Equation 2.11 into Equation 2.8 yields

$$\ddot{u}(t) + \left[\omega_0^2 - \omega_0^2\zeta^2(t) + \omega_0\dot{\zeta}(t)\right] u(t) = 0 \tag{2.12}$$

which is in the Hill equation form. This equation can be simplified to the free oscillation equation

$$\ddot{u}(t) + \omega_0^2 u(t) \approx 0 \tag{2.13}$$

by assuming

$$\zeta^2(t) \ll 1 \tag{2.14}$$

and

$$\left|\dot{\zeta}(t)\right| \ll \omega_0 \tag{2.15}$$

The first assumption requires an under-damped response. This is mostly the case in oscillator circuits. The second assumption requires the variation in the damping factor to be smaller than the oscillation frequency. This assumption is also valid since we always use quench periods which are longer than the oscillation period to let the oscillation have enough time to build up. The solution of Equation 2.13 is in the well-known form

$$u(t) = V_1 e^{j\omega_0 t} + V_1^* e^{-j\omega_0 t} \tag{2.16}$$

$$= 2Re\left[V_1 e^{j\omega_0 t}\right] \tag{2.17}$$

where V_1 is a constant to be determined from the boundary conditions. By substituting Equation 2.17 into Equation 2.9 we obtain the homogeneous solution as

$$v_h(t) = 2Re\left[V_1 e^{j\omega_0 t}\right] \cdot e^{-\omega_0 \int_0^t \zeta(\tau) d\tau} \tag{2.18}$$

The homogeneous solution is a damped cosine whose damping is determined by the integral of the overall damping factor. If the integral of the damping factor is negative, oscillation grows up and when the integral of the damping factor is positive, oscillation dies out.

The particular solution of Equation 2.4 can be obtained by the method of variation of parameters. The particular solution should be in the following form

$$v_p(t) = V_2(t)b(t) + V_2^*(t)b^*(t) \tag{2.19}$$

$$= 2Re\left[V_2(t)b(t)\right] \tag{2.20}$$

where

$$b(t) = e^{-\omega_0 \int_0^t \zeta(\tau)d\tau} e^{j\omega_0 t} \tag{2.21}$$

is the basis of the homogeneous equation.The method of variation of parameters states that the particular solution satisfies the complete equation if it satisfies

$$\dot{V}_2 b + \dot{V}_2^* b^* = 0 \tag{2.22}$$

$$\dot{V}_2 \dot{b} + \dot{V}_2^* \dot{b}^* = \frac{\dot{i}(t)}{C} \tag{2.23}$$

From Equation 2.22 and Equation 2.23, the derivative of V_2 can be found as

$$\dot{V}_2 = -j\frac{\dot{i}(t)}{2\omega_0 C b(t)} \tag{2.24}$$

Integrating both sides and rearranging yields

$$V_2 = \frac{-j}{2\omega_0 C}\int_0^t \dot{i}(\tau) e^{\omega_0 \int_0^\tau \zeta(\lambda)d\lambda} e^{-j\omega_0 \tau} d\tau \tag{2.25}$$

Inserting the above equation in Equation 2.19 yields

$$v_p(t) = e^{-\omega_0 \int_0^t \zeta(\tau)d\tau} \cdot 2Re\left[\frac{-j}{2\omega_0 C}\int_0^t \dot{i}(\tau) e^{\omega_0 \int_0^\tau \zeta(\lambda)d\lambda} e^{-j\omega_0 \tau} d\tau\right] \tag{2.26}$$

After further simplification, the particular solution takes the form

$$v_p(t) = \frac{-1}{\omega_0 C} \cdot e^{-\omega_0 \int_0^t \zeta(\tau)d\tau} \cdot \int_0^t \dot{i}(\tau) e^{\omega_0 \int_0^\tau \zeta(\lambda)d\lambda} \sin\omega_0(\tau - t)d\tau \tag{2.27}$$

The final form of the particular solution is too complicated to gain any insight into how the circuit works. In order to establish the intuitive connection between the circuit behavior and the mathematical expression, we redefine some expressions which have been used in the literature [22–24] as

$$s(t) = e^{\omega_0 \int_{t_1}^{t} \zeta(\tau) d\tau} \tag{2.28}$$

$$p(t) = e^{-\omega_0 \int_{t_2}^{t} \zeta(\tau) d\tau} \tag{2.29}$$

$$K_s = e^{-\omega_0 \int_{t_1}^{t_2} \zeta(\tau) d\tau} \tag{2.30}$$

where $s(t)$ is the sensitivity curve, $p(t)$ is the normalized output envelope and K_s is the super-regenerative gain. These expressions will be explained after the overall response of the system is described under an RF excitation signal. With the defined expressions, the final version of the particular response is obtained as

$$v_p(t) = \frac{-1}{\omega_0 C} K_s p(t) \int_0^t \dot{i}(\lambda) s(\lambda) \sin \omega_0(\lambda - t) d\lambda \tag{2.31}$$

For an excitation signal

$$i(t) = A \cos(\omega_0 t + \phi) \tag{2.32}$$

we can calculate its derivative as

$$\dot{i}(t) = -A\omega_0 \sin(\omega_0 t + \phi) \tag{2.33}$$

We obtain the forced response of the SRO by inserting Equation 2.33 into Equation 2.31 as

$$v_p(t) = \frac{-1}{\omega_0 C} K_s p(t) \int_0^t s(\lambda) \left[-A\omega_0 \sin(\omega_0 \lambda + \phi)\right] \sin \omega_0(\lambda - t) d\lambda \tag{2.34}$$

By applying product-to-sum trigonometric identities [25] and rearranging we obtain

$$v_p(t) \approx \frac{A\omega}{2\omega_0 C} K_s p(t) \int_0^t s(\lambda) \cos\left[(\omega - \omega_0)\lambda + \omega_0 t + \Phi\right] d\lambda \tag{2.35}$$

For the tuned input $\omega = \omega_0$, the solution becomes

$$v_p(t) \approx \frac{A}{2C} K_s p(t) cos(\omega_0 t + \phi) \int_0^t s(\lambda) d\lambda \tag{2.36}$$

In a properly designed SRO, the homogeneous solution should be too small compared to the forced response, which actually means there exists no free oscillation at the output. Therefore, only the regenerated signal is obtained at the output of the SRO.

The envelope of the SRO output is determined by $p(t)$ which directly modulates the output amplitude and an output is generated only if there exists an RF signal during the sensitivity period $s(t)$ since it determines how much of the injected signal is allowed to emerge from the integral. K_s determines the gain of the super-regeneration as its name suggests. Gain, output envelope and sensitivity are exponentially related to the amplitude and the shape of the damping factor.

The overall sensitivity of the SRR, which is a drawback of this architecture, is determined by NF of the LNA as well as the damping factor of the SRO (see Equation 2.28). Damping factor is determined by the loss in LC tank and negative conductance of the active circuitry in the SRO, where the former is determined by the physical properties of the components and the latter depends on power consumption. Quench current shape and amplitude determines overall damping shape and amplitude (see Figure 2.1a and Figure 2.1b). Consequently, the performance of the whole system must be optimized by taking all the aforementioned effects into account, which is a very complicated task. Furthermore, the complicated relationship between the analytic model and the circuit parameters makes it even harder. To resolve this complexity, a system-level model is presented in the subsequent chapter.

3. SYSTEM LEVEL MODELING OF A GENERIC ARCHITECTURE

In a well-designed system, system-level optimization must be performed to achieve the best performance with the given resources. To achieve this, system-level models should be available to evaluate the behavior of the system. Analytic models of the SRR are available in the literature. However, these models are too complex to gain enough inside into the connection between circuit-level parameters and the system response. In this chapter, a lumped-element model is provided, which can be used in the same environment where designs will be performed. Thus, the proposed model provides ease of use and a better understanding of the behavior. Moreover, oscillators are always hard-to-solve blocks for circuit simulator. They cause convergence problems. If noise is not activated in transient simulations, circuit simulators are generally not able to start oscillation and additional precautions must be taken to force-start the oscillation. On top of all these problems, the SRR architecture has the quenching operation which yields much longer simulation time. The proposed model also addresses these problems via its simplicity and improves simulation time without sacrificing accuracy.

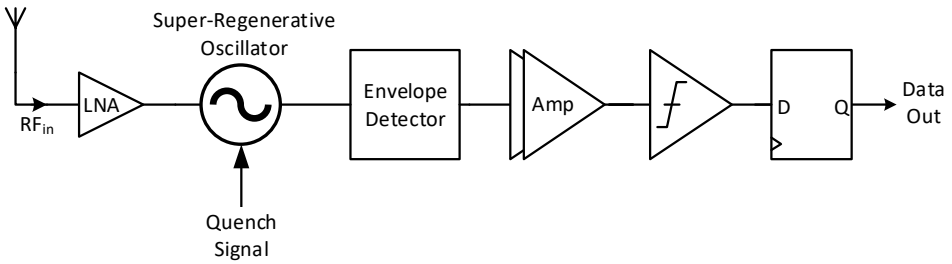


Figure 3.1. Block diagram of the SRR used in modeling.

Block diagram of the SRR to be modeled is depicted in Figure 3.1 for on-off keying (OOK) modulation which was chosen for the need of architectural simplicity. As mentioned previously, the output current of the LNA is injected into the output of the SRO. This operation eliminates the need for a separate inductor for the LNA and

the LC tank is commonly used by the SRO and the LNA. Especially when targeted operating frequencies are considered, the inductor is very bulky and being able to share an inductor among different sub-blocks is a great advantage to decrease area cost. The envelope of the regenerated signal is then obtained and further amplified in base-band and converted to digital by means of a comparator. The modeling effort focuses on the RF part which includes the LNA, the SRO, and the envelope detector.

3.1. Low-Noise Amplifier

LNA is the most critical block in a receiver in terms of noise performance. Additionally, it should provide enough reverse isolation to prevent any SRO leakage to the antenna, which will interfere with the environment and affect other wireless systems.

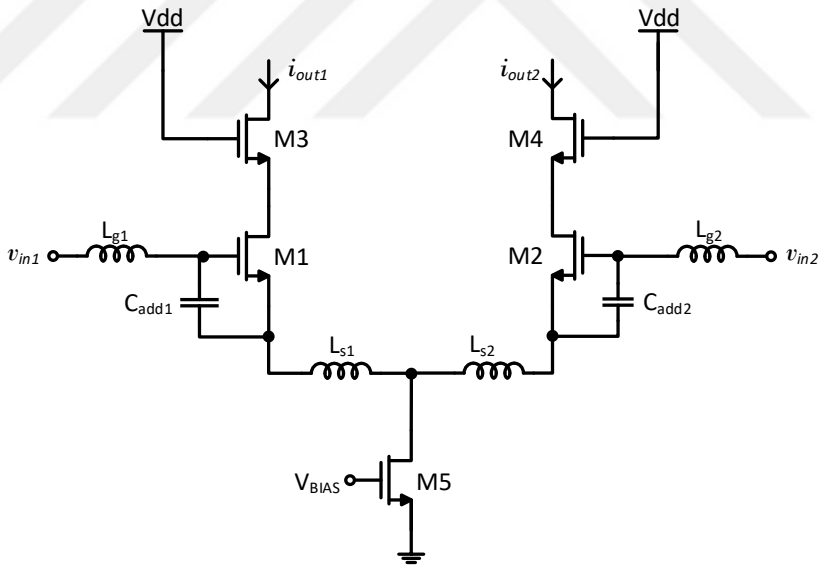


Figure 3.2. Schematic diagram of inductively degenerated fully differential low-noise amplifier.

Schematic diagram of the LNA is shown in Figure 3.2. This LNA has fully differential structure and high reverse isolation provided by the cascode stage and is suitable to directly connect the output to the LC tank of the SRO without degrading Q-factor of the tank. As will be supported with calculation and simulation results,

required C_{gs} values were too large to implement for the targeted specifications and power dissipation was also unfavorable for a good enough LNA performance at the frequency of interest. The required C_{gs} value is determined by noise specifications and cannot be modified. That is why, capacitors C_{add1} and C_{add2} were added between gate and source terminals of input transistors, which makes it possible to meet the required C_{gs} value with practical device sizes and power consumption. Additional capacitors connected between gate and source terminals of the input pair and source inductors make it possible to obtain noise and impedance matching at the same time. Thus, there is no need to sacrifice neither noise figure (NF) nor impedance matching for better performance. These characteristics of the architecture shown in Figure 3.2 make it a good choice for the SRR and successful implementations of the LNA are available in the literature [12, 26].

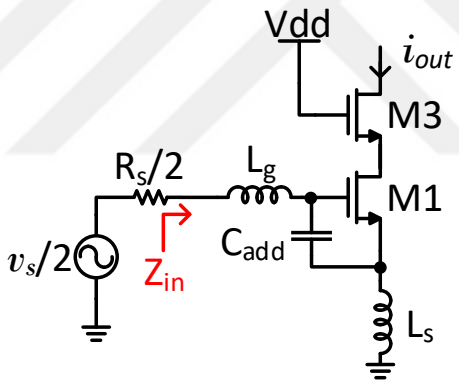


Figure 3.3. Half circuit schematic diagram of the LNA.

Since the LNA is fully differential, the half circuit shown in Figure 3.3 can be used in the analysis. The small-signal model is depicted in Figure 3.4. I_n models thermal noise of the input transistor. Input impedance R_s and input voltage v_s are divided by two in the half circuit because of the differential input. Z_{in} is the impedance seen from the input of the LNA. L_g is the gate inductance, C_{add} is the additional capacitor connected between the gate and source terminals of the input transistors, and L_s is the source degeneration inductor, all of which form the input matching structure.

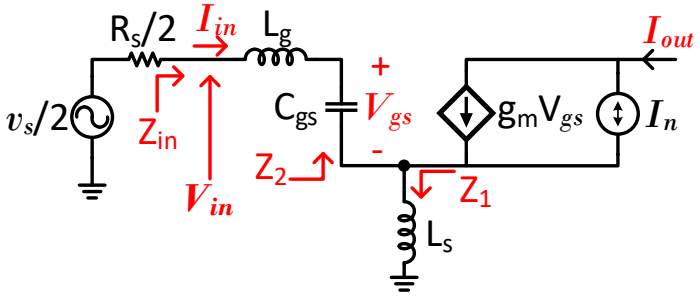


Figure 3.4. The small-signal model of the LNA.

Input impedance, Z_{in} can be determined by finding V_{in} in terms of I_{in} as [19]

$$V_{in} = j\omega L_g I_{in} + \frac{I_{in}}{j\omega C_{gs}} + \left(I_{in} + I_{in}\frac{g_m}{j\omega C_{gs}}\right) j\omega L_s \tag{3.1}$$

where

$$C_{gs} = C_{add1,2} + C_{gs,M1,M2} \tag{3.2}$$

By rearranging Equation 3.1, Z_{in} is obtained as

$$Z_{in} = \frac{V_{in}}{I_{in}} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{3.3}$$

In order to have the maximum power transfer at the input of the LNA at the operating frequency ω_0, Z_{in} must be equal to the complex conjugate of the source impedance R_s, which requires

$$j\omega_0\left(L_g + L_s\right) + \frac{1}{j\omega_0 C_{gs}} = 0 \tag{3.4}$$

$$\frac{R_s}{2} = \frac{g_m L_s}{C_{gs}} \tag{3.5}$$

Operating frequency is then obtained as

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{3.6}$$

Equation 3.4 and 3.5 are the input matching, in other words, impedance matching, conditions for the LNA.

Applying KVL around the input loop in the small-signal model and making rearrangements yield input-output relationship and noise transfer characteristic as

$$V_s = I_{out}\left(j2\omega_0 L_s + \frac{j\omega_0 C_{gs} R_s}{g_m}\right) - I_n \frac{j\omega_0 C_{gs} R_s}{g_m} \tag{3.7}$$

which consists of the superposition of signal and noise. In the above equation, coefficient of I_{out} corresponds to transconductance, and coefficient of I_n corresponds to noise transfer characteristic of the LNA. Rearrangement yields transconductance as

$$G = \left|\frac{I_{out}}{V_s}\right| = \frac{1}{2\omega_0\left(L_s + \frac{C_{gs}R_s}{2g_m}\right)} = \frac{\omega_T}{\omega_0} \cdot \frac{1}{2R_s} \tag{3.8}$$

where $\omega_T \approx g_m/C_{gs}$ and $R_s = 2g_m L_s/C_{gs}$ from Equation 3.5.

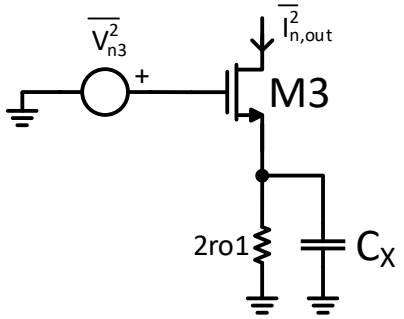


Figure 3.5. Equivalent circuit to analyze noise contribution of the cascode transistor.

Only M1 and M3 have noise contribution as other components generate no noise when they are assumed to be ideal. To analyze the noise contribution of the cascode transistor, the equivalent circuit shown in Figure 3.5 was used [27]. $\overline{v_{n3}^2}$ is the equivalent noise of transistor M3, $2r_{o1}$ is the impedance seen from the drain of transistor M1 as shown in Equation 3.24 and $C_X = C_{db1} + C_{gd1} + C_{sb3}$. The noise transfer function is

calculated as

$$\frac{I_{n,out}}{V_{n3}}(j\omega) = g_{m2}\frac{1 + j\omega 2r_{o1}C_X}{1 + 2g_{m2}r_{o1} + j\omega 2r_{o1}C_X} \tag{3.9}$$

and plotted in Figure 3.6 to visualize the response. Since targeted operating frequency is comparable with the zero frequency in the transfer function, noise contribution of the cascode transistor is negligible.

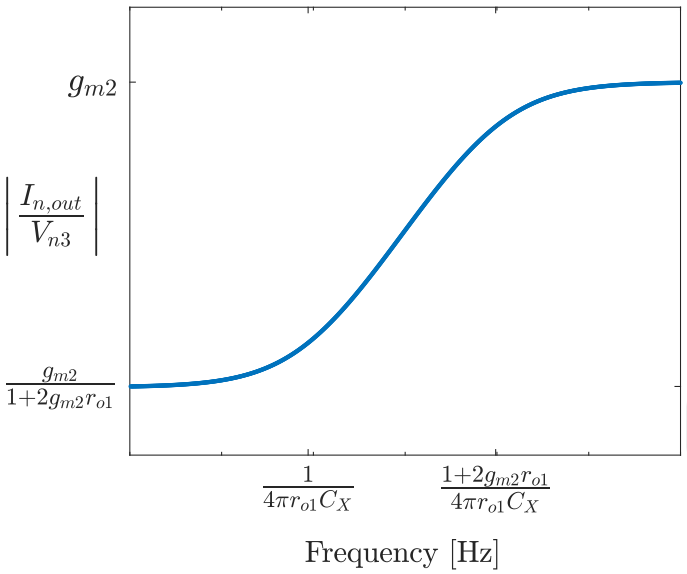


Figure 3.6. The noise transfer function of M3.

The noise transfer function of M1 can be found from Equation 3.7 as

$$|I_{n,out}|_{M1} = |I_n|\frac{R_sC_{gs}}{2g_mL_s + R_sC_{gs}} = \frac{|I_n|}{2} \tag{3.10}$$

Noise contribution of M1 to the output noise power can be expressed as

$$\overline{I_{n,out}^2}|_{M1} = \frac{\overline{I_n^2}}{4} = kT\gamma g_m \tag{3.11}$$

where

$$\overline{I_n^2} = 4kT\gamma g_m \tag{3.12}$$

for a long channel transistor operating in the saturation region. Noise factor of the LNA can be calculated as follows

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{N_{device} + |G|^2 \cdot N_{source}}{|G|^2 \cdot N_{source}} = 1 + \frac{N_{device}}{|G|^2 \cdot N_{source}} \tag{3.13}$$

where SNR_{in} is signal-to-noise ratio at the input, SNR_{out} is signal-to-noise ratio at the output, N_{device} is noise generated by the LNA at the output, and N_{source} is the noise stems from the source resistance. Inserting previously found values into 3.13 yields

$$F = 1 + \frac{\gamma}{2R_s g_m}\omega_0^2 \left(R_s C_{gs} + 2g_m L_s\right)^2 \tag{3.14}$$

$$= 1 + \frac{2\gamma R_s}{g_m}\omega_0^2 C_{gs}^2 \tag{3.15}$$

$$= 1 + \frac{8\gamma}{g_m R_s}\frac{1}{Q_{in}^2} \tag{3.16}$$

where

$$Q_{in} = \frac{2}{\omega_0 R_s C_{gs}} \tag{3.17}$$

All three forms of F stated above are useful for different approaches. For instance, Equation 3.14 is useful to find the optimum source impedance to obtain the best noise performance. To find this optimum impedance, we need to differentiate F with respect to R_s and equate to 0 as follows

$$\frac{\partial F}{\partial R_s} = \frac{\gamma\omega_0^2}{2g_m}\left(\frac{2C_{gs}\left(R_s C_{gs} + g_m L_s\right)}{Rs} - \frac{\left(R_s C_{gs} + g_m L_s\right)^2}{R_s^2}\right) \tag{3.18}$$

$$\frac{\partial F}{\partial R_s} = 0 \quad \Longrightarrow \quad R_{s,opt} = \frac{2g_m L_s}{C_{gs}} \tag{3.19}$$

As both Equation 3.5 and Equation 3.19 suggest the same input impedance, we can obtain impedance matching and noise matching at the same time. In addition to this crucial property of the proposed architecture, the gain of the proposed architecture is independent of g_m, L_s, and L_g as long as the input is matched as Equation 3.8

suggests. A disadvantage of this circuit is that it requires two inductors for the half of the circuit and L_g is generally too large to integrate and it may have to be off-chip.

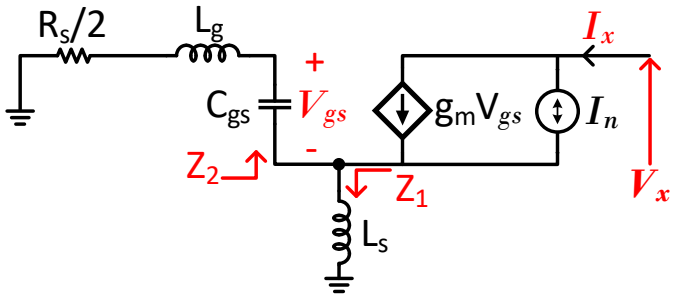


Figure 3.7. Input section small-signal model of the LNA for Z_{out} calculation.

Output impedance has to be modeled accurately since LNA output is directly connected to SRO output as shown in Figure 3.1. It loads the LC tank of the SRO and degrades quality factor and changes the resonant frequency because of the parasitic capacitances. The former affects power consumption as both affect the sensitivity of the whole system and must be taken into account while determining system specifications.

Figure 3.7 shows the small-signal model of the input transistor including additional components used to obtain matching. From this circuit, we can find the output impedance of the input transistor M1 as

$$Z_{out1} = \frac{V_x}{I_x} = \frac{\overbrace{r_{o1}(Z_1+Z_2)}^{\text{part 1}} + \overbrace{Z_1 Z_2}^{\text{part 2}} + \overbrace{g_m r_{o1} Z_1 \frac{1}{j\omega C_{gs}}}^{\text{part 3}}}{Z_1+Z_2} \tag{3.20}$$

At this point, to be able to simplify the above equation, the parts should be further investigated. Part 1 is simply equal to r_{o1}. Part 2, part 3, and the total output impedance are plotted via MATLAB and results are depicted in Figure 3.8. Results show that part 2 has a small contribution compared to the other parts and can be ignored.

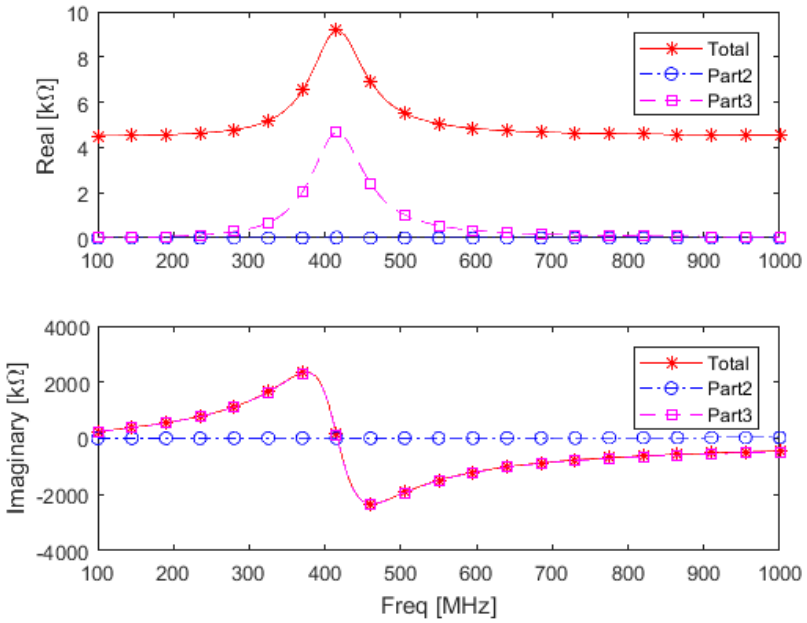


Figure 3.8. Contributions of different parts to the total output impedance.

At the operating frequency ω_0, we have

$$Z_1 + Z_2 = Rs = \frac{2g_m L_s}{C_{gs}} \tag{3.21}$$

$$Z_1 = j\omega_0 L_s \tag{3.22}$$

Substituting above equations into Equation 3.20 we obtain

$$Z_{out1} = r_{o1} + r_{o1}\frac{2g_m L_s}{R_s C_{gs}} \tag{3.23}$$

which is further simplified to

$$Z_{out1} = 2r_{o1} \tag{3.24}$$

The output impedance of the input transistor takes a very simple form. However, it is worth to mention that the calculation is only valid in the vicinity of the operating

frequency and given that the input matching is ensured. These conditions will make the model narrow band, yet it is acceptable when the targeted data rates are considered.

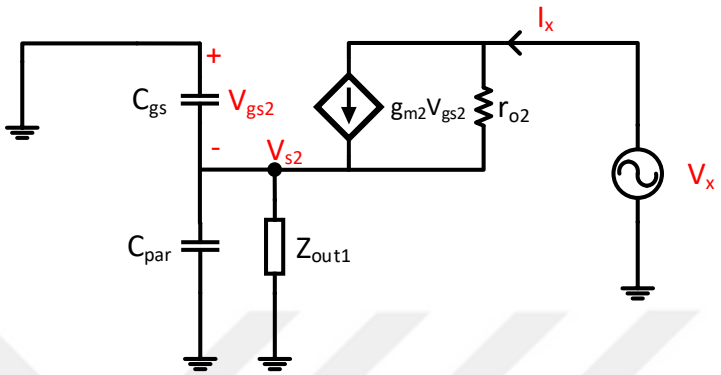


Figure 3.9. The small-signal model of the cascode transistor M3 for output impedance calculations.

Since we are using the cascode structure, we also need to calculate output impedance of the cascode transistor to obtain the final output impedance of the LNA. Figure 3.9 shows the small-signal model of the cascode transistor including parasitic capacitance at the source node. Here, C_{par} includes C_{db1}, C_{gd1}, and C_{sb2}. Z_{out1} corresponds to the output impedance of the input transistor. To calculate the output impedance, Z_x is defined as

$$Z_x = \frac{1}{j\omega C_x} \tag{3.25}$$

where $C_x = C_{gs2} + C_{par}$ is the total capacitance at node V_{s2}. Thus, we obtain

$$V_{gs2} = -I_x \cdot Z_x \parallel Z_{out1} \tag{3.26}$$

$$I_x = g_{m2}V_{gs2} + \frac{V_x - (-V_{gs2})}{r_{o2}} \tag{3.27}$$

Output impedance is then calculated as

$$Z_{out2} = r_{o2} + (1 + g_{m2} r_{o2}) (Z_x \parallel Z_{out1}) \tag{3.28}$$

Inserting previously calculated values for Z_x and Z_{out1} yields

$$Z_{out2} = r_{o2} + (1 + g_{m2} r_{o2}) \left(2r_{o1} \parallel \frac{1}{j\omega_0 C_x} \right) \tag{3.29}$$

which is the total output impedance seen from the output of the half-circuit.

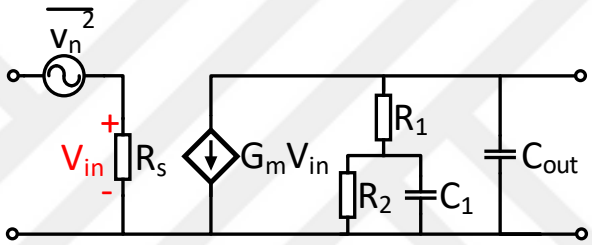


Figure 3.10. Model of the inductively degenerated differential LNA.

The final equivalent model of the LNA is shown in Figure 3.10. This is the model for the differential version of the LNA. Since Z_{out} is a complex impedance, it is divided into parts and implemented with R_1, R_2, and C_1. Parameters and component values used in the model are listed as

$$R_s = 50\Omega \tag{3.30}$$

$$G_m = 2G = -j\frac{\omega_T}{\omega_0}\frac{1}{R_s} \tag{3.31}$$

$$\overline{v_n^2} = \frac{2\overline{i_{n,out}^2}|_{M1}}{|G_m|^2} = 2kT\gamma g_m R_s^2 \left(\frac{\omega_0}{\omega_T} \right)^2 \tag{3.32}$$

$$R_1 = 2r_{o2} \tag{3.33}$$

$$R_2 = 4 (1 + g_{m3} r_{o3}) r_{o1} \tag{3.34}$$

$$C_1 = \frac{C_{par}}{2 (1 + g_{m3} r_{o3})} \tag{3.35}$$

$$C_{out} = \frac{C_{db2} + C_{gd2}}{2} \tag{3.36}$$

In order to verify the proposed model, an example design was performed. Targeted NF for the LNA was $1.2\,dB$ with minimum power consumption possible. To investigate the design space for the given specs, analytic calculations were implemented in Cadence ADE environment such that a single transistor is characterized with DC bias sweep and its characteristics are used in the calculations, and the required bias point, device sizing, and component values are derived. Calculation and simulation procedures are shown in Figure 3.11. The test bench takes the target NF and sweeps Q_{in} over a range to show the required component values and power consumption. From these results, one can choose any combination that suits to the given specs.

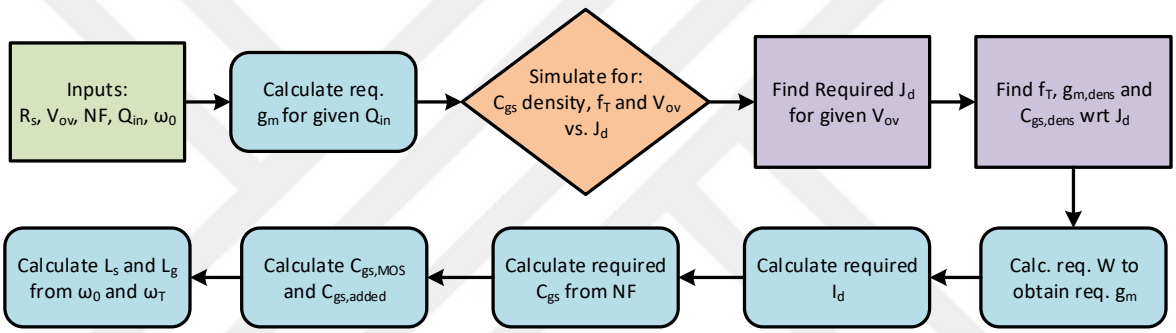


Figure 3.11. LNA design space calculation flow chart.

Figure 3.12 shows the design space for the given targeted specifications with respect to input matching network Q-factor. Minimum-power point was chosen for the LNA with an acceptable transconductance gain. As can be seen from the design space, added C_{gs} constitutes a great portion of the total C_{gs}, which improves power consumption as expected.

Simulation results of both the actual circuit and the model for the LNA are shown in Figure 3.13. Model simulation results fit the circuit behavior in the vicinity of the operation frequency which is due to the fact that the calculations were carried out at ω_0. Output impedance was simulated with the LC tank of the SRO which will be the load of the LNA in the completed system. Values of gain, noise factor, and output impedance are listed in Table 3.1 along with the error values between circuit and model simulation result at the operation frequency.

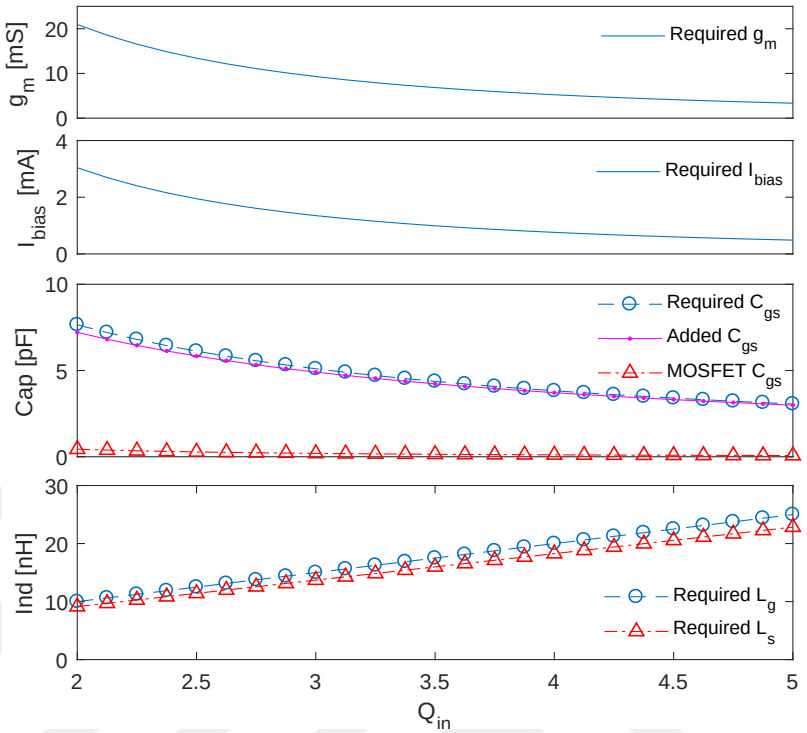


Figure 3.12. LNA design space for the given specifications.

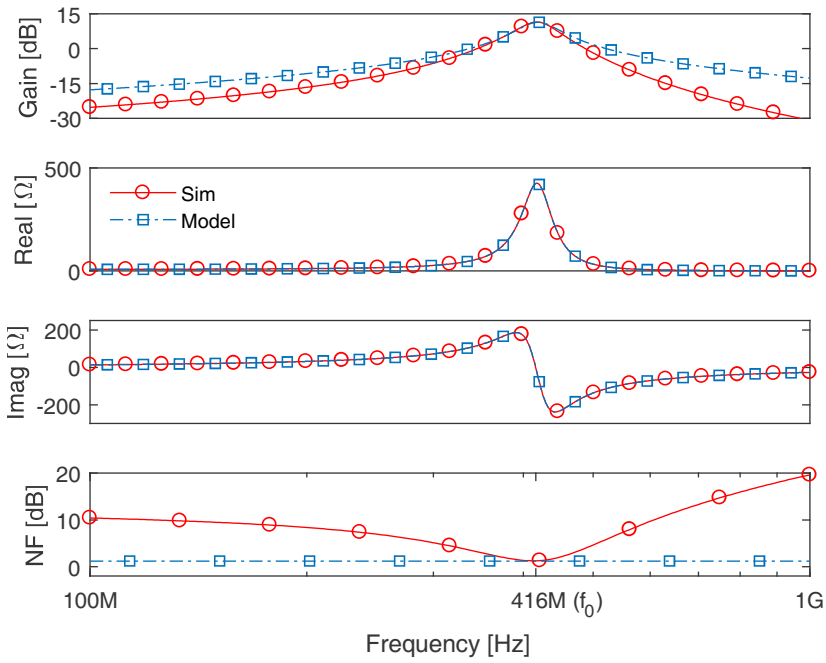


Figure 3.13. Simulation results of gain, real and imaginary part of the output impedance, and NF of the LNA and the proposed model.

Table 3.1. LNA circuit and model simulation results.

	Circuit	**Model**	**Error**
Gain	3.74 (11.46 dB)	3.68 (11.31 dB)	1.6%
F	1.34 (1.25 dB)	1.32 (1.20 dB)	1.5%
$\|\mathbf{Z_{out}}\|$	424.59 Ω	424.63 Ω	9.4m%

3.2. Super-Regenerative Oscillator

Analytic solution and operation of the SRO were presented in Chapter 2 on the small-signal model shown in Figure 3.14 which is given here again for ease of reading. Cross-coupled oscillator architecture was chosen because it provides superior phase noise performance compared to other typologies. Since we aim for low power, complementary pair architecture would be a better choice than only NMOS or only PMOS pair versions since it reuses current in PMOS and NMOS pairs and generates higher transconductance with the same current. However, since the bias current of the LNA is also drawn from the output of the SRO, using a PMOS pair would not be suitable when we take quenching into account. This fact leaves only the NMOS pair option. Schematic of NMOS pair cross-coupled oscillator is shown in Fig. 3.15. Resistors with value $R_s/2$ are not additional components, rather they are modeling the loss of inductors. Since this architecture employs inductors that are directly connected to the power supply, it is perfectly suitable to bias the LNA from its output.

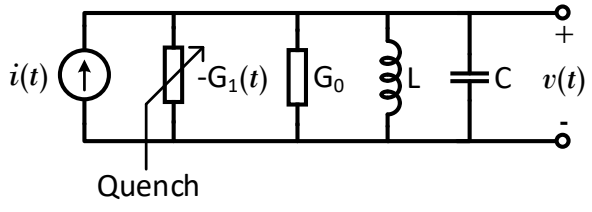


Figure 3.14. Model of the super-regenerative oscillator.

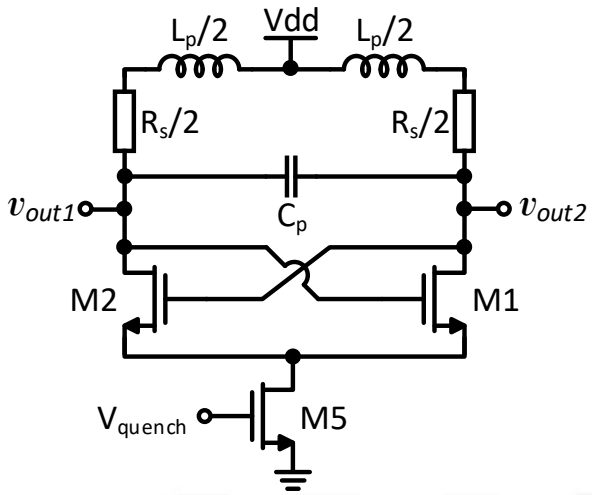


Figure 3.15. Schematic diagram of the cross-coupled oscillator.

In small-signal operation, the conductance seen from cross-coupled transistors is equal to $-g_m/2$. Therefore, the equivalent model for the circuit is obtained with a negative conductance as shown in Figure 3.14. There is no controllable negative conductance available in standard circuit simulators. Therefore, controllable negative conductance was modeled via Verilog-A which can be simulated by many different simulators (see Figure 3.16). Component values shown in the SRO model are obtained from the circuit as

$$G_0 = \frac{1}{Q^2 R_s} \tag{3.37}$$

$$L = L_p \tag{3.38}$$

$$C = Cp \tag{3.39}$$

where Q is the quality factor of the inductor at ω_0 and R_s is the loss of inductor.

Simulation results of the SRO model and actual circuit are provided along with the whole system results in Section 3.4.

```
module var_neg_cond(contP, contM, p, m);
inout contP, contM;
inout p, m;
electrical contP, contM;
electrical p, m;
parameter real gm = 4m from (0:inf);
parameter real Ilim = 10m from (0:inf);
real conductance = 0;
real Iout = 0;

analog begin
  conductance = (-gm * V(contP,contM));
  Iout = conductance * V(p,m);

  if (Iout > Ilim) begin
    Iout = Ilim;
  end
  else if (Iout < -Ilim) begin
    Iout = -Ilim;
  end

  I(p,m) <+ Iout;
end
endmodule
```

Figure 3.16. VerilogA code of the variable negative conductance.

3.3. Envelope Detector

The simplest and the lowest power solution to demodulate the OOK data is the envelope detector. It simply rectifies the RF signal and filters the high-frequency components, thus generating the envelope. MOSFETs are operated in weak inversion which has the most non-linear characteristics and is favorable to obtain the envelope of the signal.

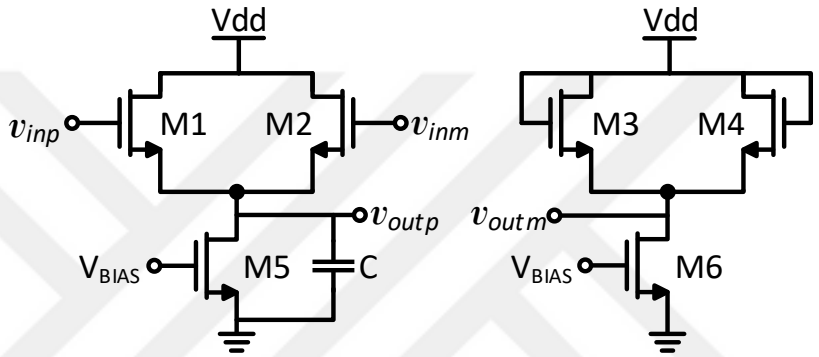


Figure 3.17. Schematic diagram of envelope detector.

Active pseudo-differential envelope detector [28] is the best choice for the given technology thanks to its low power consumption and simplicity. Schematic of the pseudo-differential envelope detector is shown in Figure 3.17. Transistors M1 and M2 are operated in weak inversion. Right-half of the circuit is just the replica of left-half to generate common-mode voltage for negative input of the subsequent block. Capacitor C shown in the schematic consists only of parasitic capacitances and the input capacitance of the subsequent block. No additional capacitor is needed at the output of the envelope detector because the bigger the capacitance at the output, the higher the power consumption. Tail current does not affect the gain of the circuit as suggested in Equation 3.49, thus the lowest possible current can be chosen, which is determined by the required cut-off frequency of the output low-pass characteristic with respect to the total capacitance appears at the output node.

Drain current formula for the MOSFET operated in weak inversion is given as [29]

$$i_D = \underbrace{I_0 e^{\frac{V_G - V_{th}}{nV_T}} \left(e^{-\frac{V_S}{V_T}} - e^{-\frac{V_D}{V_T}} \right)}_{I_Q} e^{\frac{v_g}{nV_T}} = I_Q e^{\frac{v_g}{nV_T}} \tag{3.40}$$

where $V_T = k\frac{T}{q}$, $I_0 = 2n\beta V_T^2$, $\beta = \mu_n C_{ox} \left(\frac{W}{L}\right)_1$, and n is the slope correction factor. I_Q is defined as shown in the above equation for the sake of simplicity in the rest of the analysis. For small v_g, we can express the drain current as

$$i_D \approx I_Q + \left(\frac{\partial I_d}{\partial V_g}\right) v_g + \left(\frac{\partial^2 I_d}{\partial V_g^2}\right) \frac{v_g^2}{2} \tag{3.41}$$

$$= I_Q + \frac{I_Q}{nV_T} v_g + \frac{I_Q}{(nV_T)^2} \frac{v_g^2}{2} \tag{3.42}$$

With the above results, drain currents of the input pair can now be calculated for $v_{inp} = -v_{inm} = v_{id}/2$ as

$$i_{D1} = I_Q + \frac{I_Q}{nV_T} \frac{v_{id}}{2} + \frac{I_Q}{(nV_T)^2} \frac{v_{id}^2}{8} \tag{3.43}$$

$$i_{D2} = I_Q - \frac{I_Q}{nV_T} \frac{v_{id}}{2} + \frac{I_Q}{(nV_T)^2} \frac{v_{id}^2}{8} \tag{3.44}$$

The output current is simply the sum of the drain currents and can be expressed as

$$i_{out} = i_{D1} + i_{D2} = 2I_Q + \frac{I_Q}{(nV_T)^2} \frac{v_{id}^2}{4} \tag{3.45}$$

If an RF signal of $v_{id} = A\cos\omega t$ is applied to the circuit

$$i_{out} = 2I_Q + \frac{I_Q}{4(nV_T)^2} \frac{A^2}{2} (1 + \cos 2\omega t) \tag{3.46}$$

Applying the low-pass characteristics of the envelope detector which stem from the output resistance and the capacitor C in Figure 3.17 output current is obtained as

$$i_{out} = \frac{I_Q A^2}{8(nV_T)^2} \tag{3.47}$$

The output amplitude can be calculated by multiplying output current with output resistance. The output resistance is given as

$$R_{out} = \frac{1}{g_{m1}} \parallel \frac{1}{g_{m2}} = \frac{1}{2g_m} = \frac{nV_T}{2I_Q} \tag{3.48}$$

Thus, the output amplitude is obtained as

$$v_{out} = \frac{A^2}{16nV_T} \tag{3.49}$$

3.4. Simulation Results and Conclusion

In simulations, Cadence Virtuoso was used for both the actual circuits and models. Although this is a highly integrated design environment, proposed models can also be used in simple circuit simulators. Designs were performed in UMC 180 nm fabrication technology. Standard 1.8 V power supply voltage for the process is used.

Simulation results for the LNA and the proposed LNA model are presented in Section 3.1. In this section, overall system simulations for both actual circuits and the proposed model are shown and explained. Finally, a brief conclusion is drawn including the performance comparison with the state-of-the-art.

For the SRO, traditional cross-coupled oscillator topology was chosen thanks to its decent phase noise performance and suitability for quenching (see Figure 3.15). The higher the oscillation amplitude, the better the phase noise performance [30, 31]. Oscillation amplitude is determined by the bias current and the Q-factor of the inductor. For a fixed oscillation amplitude, increasing inductance improves power consumption as increasing the Q-factor of the inductor does. The latter also improves the phase noise performance of the oscillator, directly.

Design procedure starts with choosing the most suitable inductor available. Oscillation amplitude is set to the maximum available value. Maximum tail current is

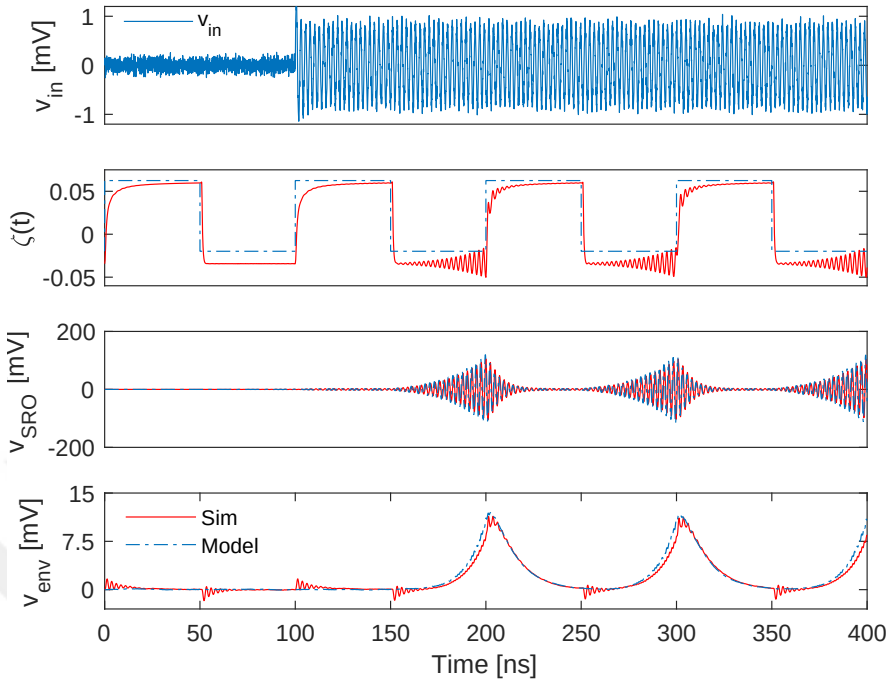
calculated according to the maximum allowable output swing. Transistor sizing is done such that transistors are ensured to stay in strong inversion during most of the quench period, thus the relation between tail current and transconductance of the devices does not change so much.

For this example design, the operating frequency is 416 MHz which is the center frequency of MedRadio band. 10 MHz quench signal is used in the simulations, which can sample the highest 10 Mbps data rate.

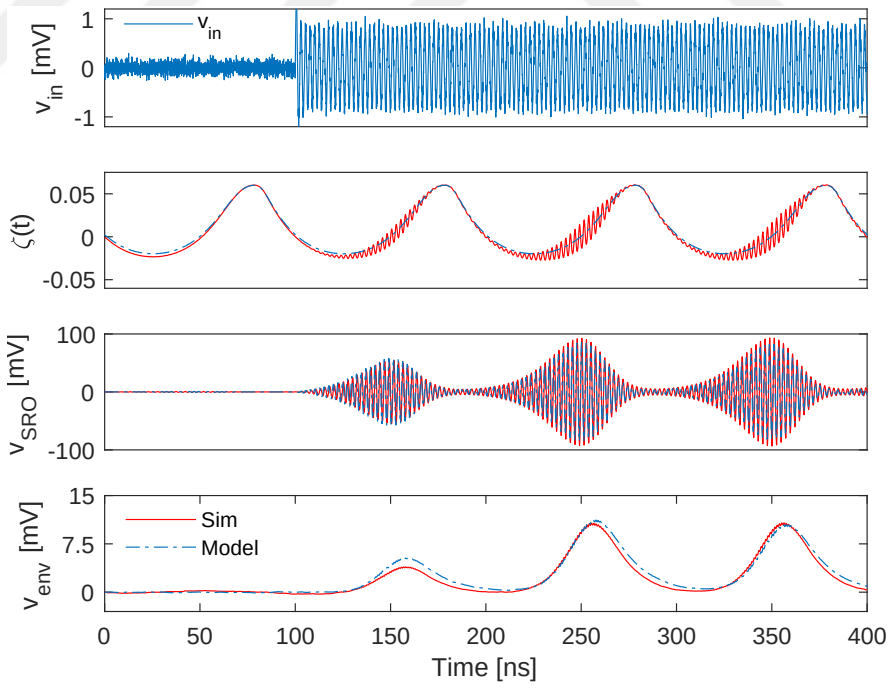
Simulation results of the whole receiver are shown in Figure 3.18a for both the model and the circuits under square-wave quench current. Transient noise bandwidth was set to 10 GHz. Damping factors were obtained from the calculated parameters and the difference between the model and the circuit stems from this fact. Small spikes seen at the envelope detector output in the circuit simulation results arise from the common-mode voltage fluctuations because of the quenching but they are small enough to be ignored. Equation 3.49 suggests 12.9 mV amplitude at output and simulation yields 12 mV which corresponds to 7 % error.

Simulation results for both the model and the circuits under sinusoidal quench current can be seen in Figure 3.18b. All the simulation conditions except quench signal shape were set the same as the previous case. Shape of the damping factor deviates from the sinusoidal shape since transconductance of the transistors is related to the square root of drain current. The first oscillation period is smaller in amplitude compared to the following periods since the input signal is given in the middle of the sensitivity period, which decreases the overall gain for that period and results in smaller oscillation amplitude. Since the tail current of the SRO is not quenched so sharply, no spikes occur at the output. Only power consumption of the SRO changes in this case as shown in Table 3.2.

Transient simulation elapsed time for the whole system simulation is shortened by at least an order of magnitude with the proposed models. Improvement changes from simulator to simulator as well as with different accuracy settings in the same simulator.



(a)



(b)

Figure 3.18. Simulation results of input voltage, damping factor, SRO and envelope detector outputs of the whole receiver and the model under (a) square and (b) sinusoidal quench current.

However, the model provides a very accurate system response within a much shorter time. Additionally, while determining the system specifications, the models help the designer to predict the system response with no additional circuit design effort, which is the biggest advantage of the model.

Table 3.2. Power consumption.

	Square Quench	**Sine Quench**
LNA	2.70 mW	2.70 mW
SRO	1.62 mW	1.64 mW
Env. Det.	2.7 μW	2.7 μW
Total	4.323 mW	4.343 mW

Power consumption of each sub-block and the whole system are shown in Table 3.2 for square and sinusoidal quench shapes, where the power supply voltage is 1.8 V. As can be seen from the results, the power consumption of the SRO is decreased such that it is even lower than the LNA power consumption. Power consumption of the LNA can also be further reduced by changing characteristic impedance R_s, yet for the sake of compatibility with other systems, the best practice is to use 50 Ω.

Table 3.3. Comparison with the previous work.

	Process	**Frequency**	**Data Rate**	$\mathbf{V_{supply}}$	$\mathbf{E_b}$
[12]	350 nm CMOS	402-405 MHz	2 Mbps	N/A	500 pJ
[14]	40 nm CMOS	800-980 MHz	1 Mbps	0.65 V	320 pJ
[26]	180 nm CMOS	402-405 MHz	1 Mbps	1.5 V	5.5 nJ
[32]	180 nm CMOS	402-405 MHz	120 Kbps	1.5 V	4.17 nJ
This Work	180 nm CMOS	416 MHz	10 Mbps	1.8 V	432 pJ[1]

Comparison with previous works is summarized in Table 3.3. Frequency shows the operating frequency of the receiver, the data rate is the bit rate at which power

[1] RF front-end only.

is measured, and E_b shows energy consumption per received bit. Energy consumption of this work includes only RF front-end. However, the base-band part consumes much lower power than RF front-end in almost all the receivers. Even though supply voltage is higher, this work performs similar to or better than previous works in terms of energy efficiency. [14] performs better because they used a more advanced 40nm node with 0.65V power supply. However, the circuits proposed here allow supply voltages as low as 1V which would improve energy efficiency much further with some performance trade-offs. The receiver proposed here also achieves much higher data rates compared to the previous work.

4. SUPER-REGENERATIVE RECEIVER WITH PASSIVE INDUCTORS

Circuits employing resistive loads exhibit low-pass characteristics as resistive loads together with parasitic capacitances create poles and limit the operation band. In the case of RF circuits, high-frequency operation is needed and resistive loads are not suitable for this purpose. Instead, inductive loads have been used in high-frequency applications to obtain resonant behavior at the frequency of interest by means of parasitic and additional capacitances. That is why the common practice to design a receiver is to make use of the architectures employing inductors.

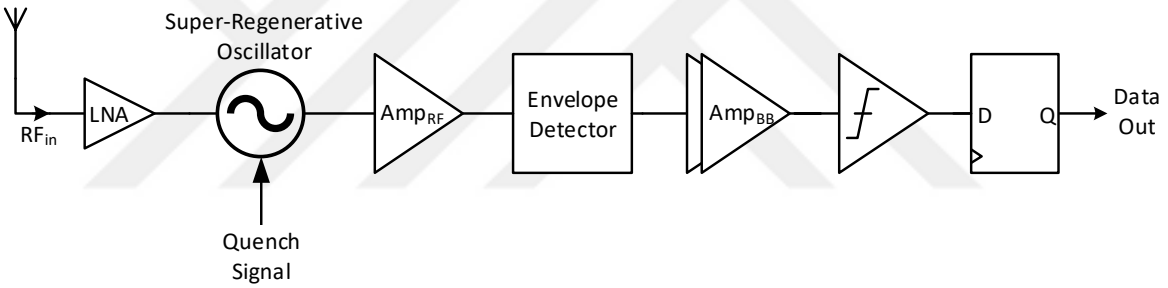


Figure 4.1. Block diagram of the SRR with inductors.

The first proposed super-regenerative receiver in this thesis employs inductors. To make use of the advantages of integration, inductors were integrated wherever possible. Block diagram of the final system is depicted in Figure 4.1. Amplifiers are divided between RF and base-band frequencies. As Equation 3.49 suggests, the output amplitude of the envelope detector is determined by the square of the input amplitude. This means that any amplification performed before the envelope detector will be squared by the envelope detector. To make use of this fact and to distribute power optimally among the sub-blocks, one amplifier stage is moved before the envelope detector (see Figure 4.1).

This chapter is organized as follows. Section 4.1 presents sub-blocks of the SRR. Sub-blocks are presented firstly with the analytic analysis and the design procedure is explained afterward. Finally, silicon measurement results are presented in Section 4.2 along with the discussion on the results.

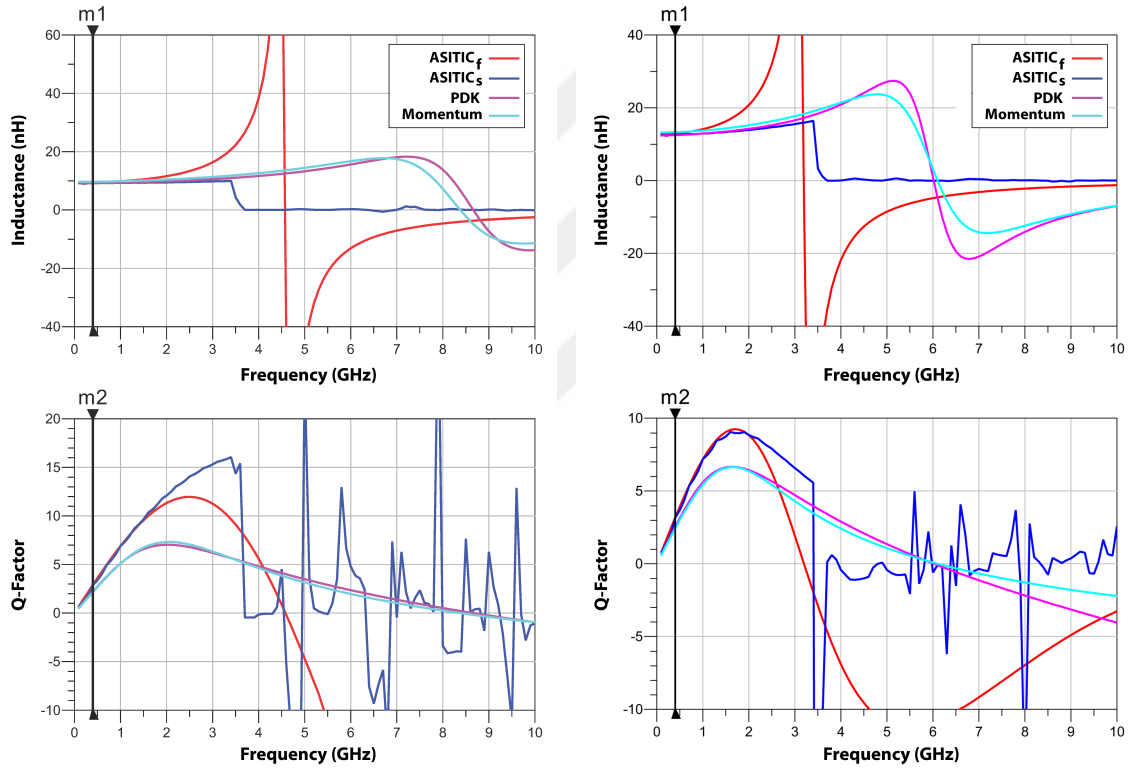
4.1. Analysis and Design

4.1.1. On-Chip Inductor

As MedRadio standards state, the operating band is located around 416 MHz frequency. At such low frequencies, the required inductance is generally too big to integrate. That is why only the inductor used in the LC tank of the SRO was decided to be integrated as it is the most critical inductor in the receiver. UMC 180 nm fabrication process is used in this design. Process design kits are provided with devices that have been fabricated, characterized and modeled. However, available components in PDKs are not always suitable for all the applications, which was the case here. This fact made it necessary to design a custom on-chip inductor for this project.

In differential circuit topologies, center-tapped symmetric inductors are favored as they provide higher Q-factor and higher inductance thanks to the mutual inductance between each half. A center-tapped symmetric inductor was chosen for this thesis work. However, as the structure of an integrated circuit is very complex and the substrate is lossy, a reliable method must be used in the design procedure. There are very accurate analytic formulations for integrated octagonal spiral inductors, which are used to determine dimensions for the targeted inductance value at the beginning of the design procedure [33, 34]. However, they are only limited to the inductance value, and quality factor and self-resonant frequency are not modeled, which are as crucial as the inductance value. On the other hand, there are commercially available simulators such as Keysight Momentum as well as free tools such as Analysis and Simulation of Spiral Inductors and Transformers for ICs (ASITIC), which are very accurate to determine all the characteristics thanks to electromagnetic simulations.

Firstly, Momentum and ASITIC were used to simulate some inductors provided in the PDK to characterize the accuracy of the simulation results. To do so, the chip structure was modeled in both simulators and dimensions of the selected inductors in the PDK were directly used without any change. There are two options for ASITIC simulations, namely *fast* and *slow*. The former runs for a few minutes whereas the latter takes hours to complete. Momentum runs faster than ASITIC *slow* option yet much slower than the *fast* option.



(a) (b)

Figure 4.2. Momentum and ASITIC accuracy comparison with respect to PDK results for (a) inductor-1 and (b) inductor-2.

Simulation results of both the simulators as well as the PDK model are shown in Figure 4.2a and Figure 4.2b for inductor-1 and inductor-2, respectively. Markers are located to 400 MHz which was the closest point to the operating frequency and marker values are depicted in Table 4.1. At low frequencies, all of the inductance results are close to each other. For higher frequencies, ASITIC *slow* predicts inductance accurately, yet its result is meaningless after a frequency. ASITIC *fast* shows self-

Table 4.1. Marker values.

	Inductor-1		Inductor-2	
	Inductance	**Q-factor**	**Inductance**	**Q-factor**
PDK	9.16 nH	2.20	12.48 nH	2.52
Momentum	9.66 nH	2.17	13.28 nH	2.43
ASITIC *fast*	9.45 nH	2.90	12.96 nH	3.18
ASITIC *slow*	9.24 nH	2.87	12.66 nH	3.18

resonance at much lower frequencies than others. Therefore, inductance prediction is the worst among others. Momentum is the most accurate simulator in determining inductance. Self-resonant frequencies determined by Momentum are closer to the UMC model than other simulators. In determining Q-factor, Momentum is again ahead with a great distinction. On the overall response, Momentum appears to be the most suitable option to perform inductor design.

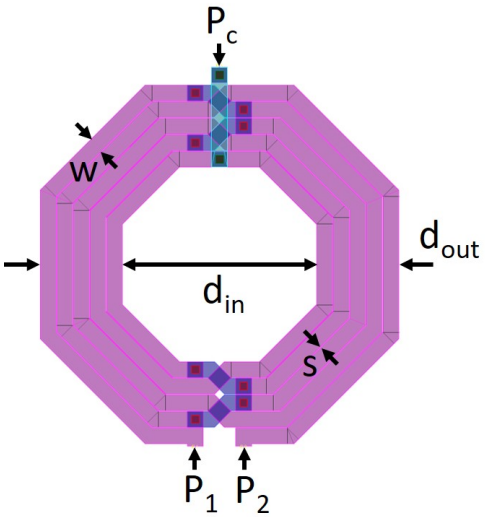


Figure 4.3. The layout of the center-tapped symmetric octagonal inductor.

Fabrication process allows using only integer multiples of 45° entries. Since the Q-factor is enhanced with the number of sides, octagonal spiral geometry was chosen (see Figure 4.3). Here, w is metal width, s is spacing between consequent turns, d_{in} is

inner diameter, and d_{out} is outer diameter. Although not visible in Figure 4.3, t and n are the thickness of the metal and the total number of turns, respectively. P_1 and P_2 are the ports at each end of the inductor and P_c is the center-tap port. Inductor layout was drawn to be symmetrical around the port P_c.

The aim was to design a 20 nH symmetric inductor with maximum output diameter of 500 μm and optimum Q-factor at 400 MHz. Analytic models are the fastest options to determine dimensions of the structure which gives the desired inductance. The following analytic models were used to determine inductance [33, 34]

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \tag{4.1}$$

$$L_{gmd} = \frac{\mu n^2 d_{avg} c_1}{w} \left(\log(\frac{c_2}{\rho}) + c_3 \rho + c_4 \rho^2 \right) \tag{4.2}$$

$$L_{mon} = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \tag{4.3}$$

$$L_{phy} = \frac{\mu_0}{2\pi} \left(\log \frac{l_{oct}}{n(w+t)} - 0.9 \right) + \frac{\mu_0}{2\pi} 1.21 l_{oct} \cdot \left(-0.47n + (n-1) \cdot \left(\log \left(\sqrt{1 + \left(\frac{1.21 l_{oct}}{4nd^+} \right)^2} + \frac{1.21 l_{oct}}{4nd^+} \right) - \sqrt{1 + \left(\frac{4nd^+}{1.21 l_{oct}} \right)^2} + \frac{4nd^+}{1.21 l_{oct}} \right) \right) \tag{4.4}$$

where the coefficients c_i, α_i, and β are geometry dependent coefficients, l_{oct} is the total spiral length, d^+ is the average distance for the constituting factor of positive mutual inductance and

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad , \quad d_{avg} = \frac{d_{out} + d_{in}}{2} \tag{4.5}$$

Generated geometries and corresponding inductance values are provided in Table 4.2. Low-frequency inductance values obtained from Momentum, as well as analytic formula calculations, are included in this table. Resultant inductance values are close to each other for each geometry.

Table 4.2. Properties of designed inductors.

Device	**W** (μm)	**D** (μm)	**N**	**S** (μm)	$\mathbf{L_{mw}}$ (nH)	$\mathbf{L_{gmd}}$ (nH)	$\mathbf{L_{mon}}$ (nH)	$\mathbf{L_{phy}}$ (nH)	**Momentum** (nH)
ind1	20	630	5	1.5	21.56	21.44	19.91	20.21	20.67
ind2	25	690	5	1.5	21.57	21.51	20.13	20.11	20.79
ind3	30	750	5	1.5	21.73	21.75	20.47	20.19	21.07
ind4	35	790	5	1.5	20.95	21.07	19.92	19.39	20.44
ind5	40	840	5	1.5	20.81	21.02	19.95	19.21	20.43
ind6	45	890	5	1.5	20.75	21.05	20.05	19.12	20.46
ind7	50	930	5	1.5	20.29	20.66	19.74	18.63	20.12

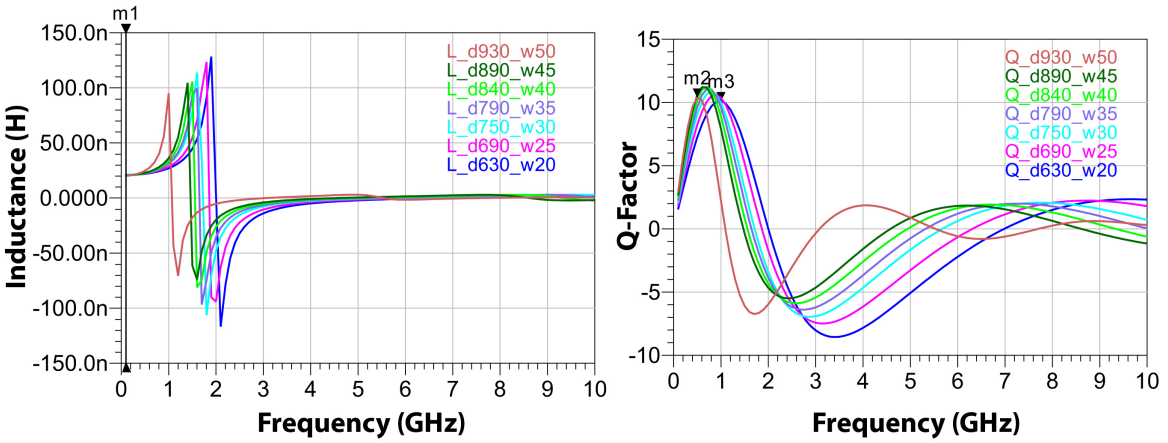


Figure 4.4. Inductances and Q-factors of all the devices.

Inductance and Q-factor of the devices were obtained via Momentum simulation and are shown in Figure 4.4. All of them have more or less the same inductance and the maximum Q values. The main difference is the peak frequency of Q-factor which is desired to be around 400 MHz for the targeted application. The lowest peak frequency obtained from the listed structures is 500 MHz. However, the layout of the corresponding device occupies a huge area that is not feasible to integrate. ind4 was chosen to be optimized for the targeted frequency since it is the one with the lowest Q-factor peak frequency within our dimension limitations.

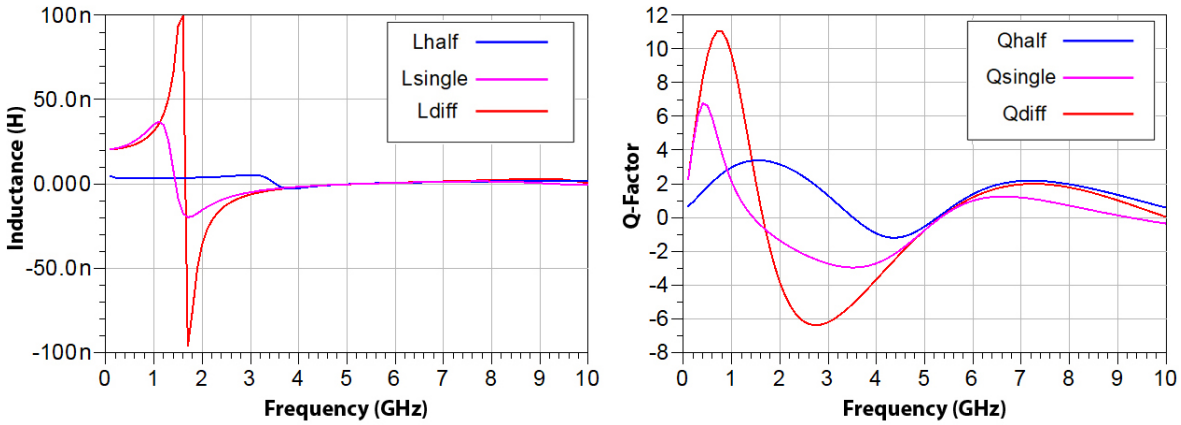


Figure 4.5. Inductances and Q-factors of ind4 with different excitations.

As mentioned previously, excitation of the inductor changes the inductance and the Q-factor values as well as the frequency behavior. Inductance and Q-factor of the chosen device ind4 is shown in Figure 4.5 under different excitation schemes. In half inductance simulation, P_1 was excited single-ended and P_2 and P_c were grounded. In single-ended inductance simulation, P_1 was excited single-ended, P_2 was grounded and P_c was left open. In differential excitation inductance simulation, P_1 and P_2 were excited differentially with a single port and P_c was left open. Although P_c was left open in the differential excitation case, because of the differential excitation, P_c will already be virtual ground. Results suggest that maximum Q-factor value and peak frequency of the Q-factor increases with differential excitation. The underlying reason is that parasitic capacitances appear in series because of the virtual ground generated at the center-tap. Total inductance is four times the half inductor value thanks to mutual inductance provided by the symmetric structure. As a result, the best option is to use the symmetric structure with differential excitation.

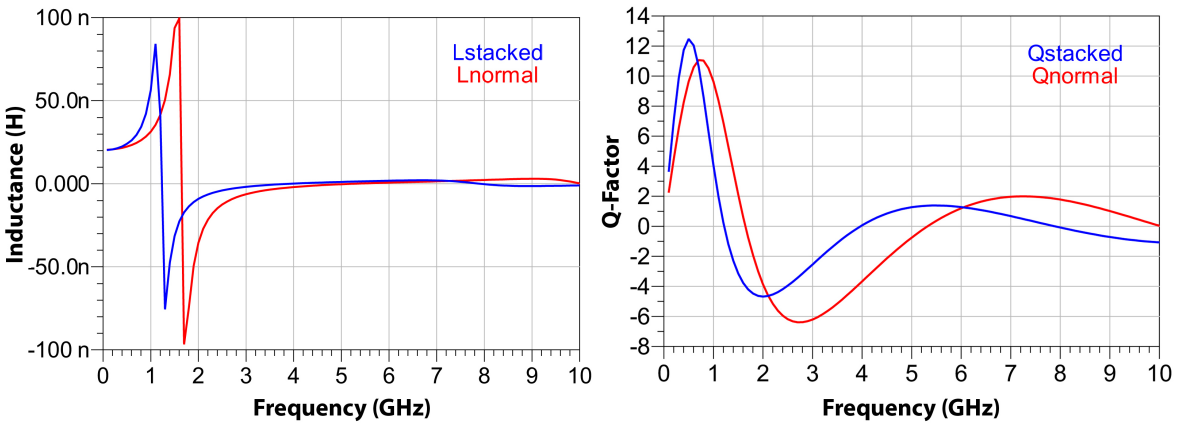


Figure 4.6. Inductance and Q-factor of ind4 with single layer and stacked structures.

Table 4.3. Single-layer and stacked structure performance comparison for ind4.

	L @ 400 MHz	**Q @ 400 MHz**	$\mathbf{f_{Qmax}}$	**Qmax**
Single-Layer	21.55 nH	8.25	700 MHz	11.06
Stacked	22.40 nH	11.74	500 MHz	12.47

Even though inductance value is very close to the target, the Q-factor needs to be optimized to peak at the operating frequency. As can be seen from the previous results Q-factor of the inductor ind4 peaks around 750 MHz. To decrease this peak frequency, self-resonant frequency of the inductor needs to be decreased. Minimizing s and increasing w helps to achieve this purpose. However, selected $s = 1.5\,\mu m$ is the minimum allowed spacing and increasing w further is not feasible in terms of area cost. To push the response further towards low frequencies, a stacked structure is used. The stacked structure uses three inner metal layers and shunts them with the last metal layer, which will increase the parasitic capacitance. This will also help to improve Q-factor since shunting more metal layers decreases DC resistance of the inductor. By using stacked structure, we can obtain higher Q-factor and lower peak frequency at the same time. Figure 4.6 shows the inductance and Q-factor of the inductor for single-layer and stacked structure. Important values are listed in Table 4.3. As can be seen from the results, Q-factor peak frequency was decreased towards the frequency of interest and as an additional effect, Q-factor was increased as explained above.

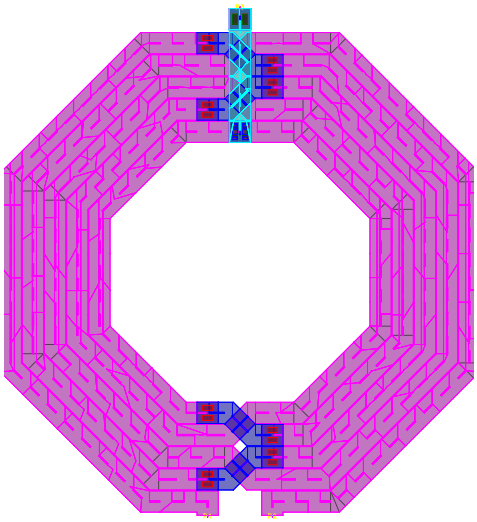


Figure 4.7. The layout of the inductor with slots.

Because of the thermal stress caused during fabrication processes, the metal line width is limited by the fab to prevent any problems during fabrication. Since we cannot achieve 400 MHz target with the limited width, wider metal lines needed to be used in the design. After the limit width, slots must be opened in metal lines to release the

thermal stress. The slotted layout of the inductor is shown in Figure 4.7. Effect of the slots was investigated with the single layer inductor and results are shown in Figure 4.8. Figure 4.9 shows the effect of slots in the stacked structure. Peak frequency of Q-factor did not change much since parasitic capasitances are not affected by slots. However, the maximum of Q-factor decreased because slots decrease the area through which current can flow, thus increasing the resistance.

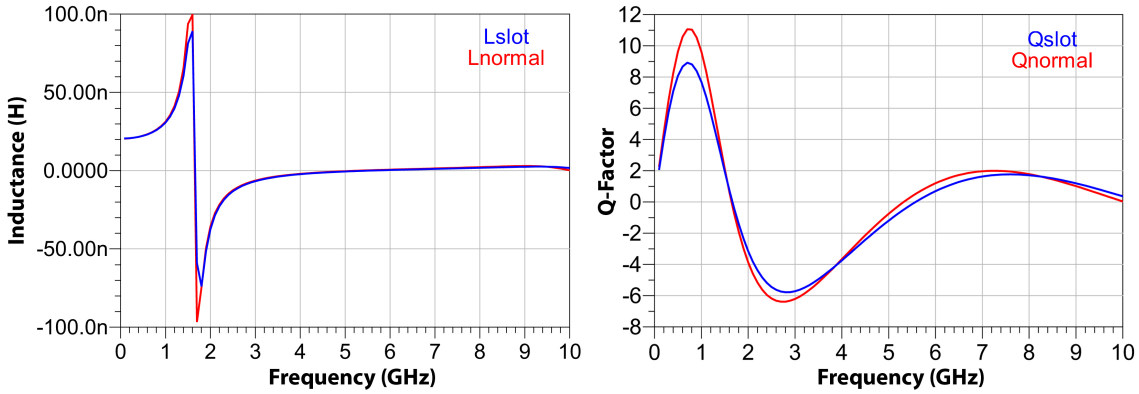


Figure 4.8. Inductances and Q-factors of single layer ind4 with and without slots.

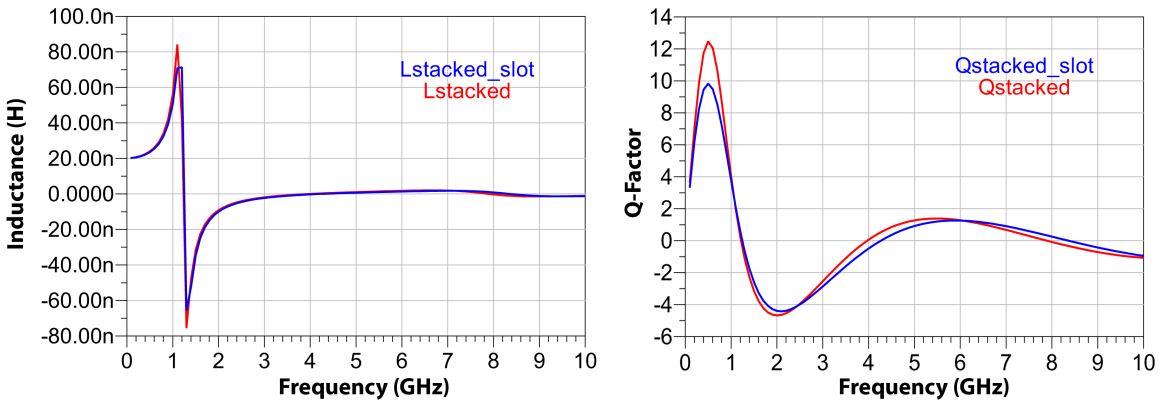


Figure 4.9. Inductance and Q-factor of stacked ind4 with and without slots.

Substrate losses play an important role in determining the quality factor of the inductor. Magnetically induced losses are minimized by using a lightly doped substrate. There is no other option available on the substrate to improve magnetically induced losses. However, electrically induced losses can be decreased via a ground plane under the inductor [35]. This prevents penetration of the electrical field into the

lossy substrate and decreases losses generated by this mechanism. As shown in [35], solid ground shield (SGS) prevents all the electric field penetration, yet eddy currents generated in the conductive solid shield heavily decreases inductance. On the other hand, patterned ground shield (PGS) prevents eddy currents while performing the desired effect on the electric field. Furthermore, the optimal layer for the PGS was found to be the poly layer [35]. The layout of the inductor with the the PGS is shown in Figure 4.10. Contacts were placed to the first metal layer. Additionally, in order to prevent eddy current in any layer around the inductor, closed loops must be avoided. Therefore, the frame in the first layer was split into many parts. Figure 4.11 shows the effect of ground shields on the single layer inductor. The SGS decreased inductance and Q-factor as expected. However, the PGS did not increase quality factor. On the contrary, the maximum Q-factor value decreased. Figure 4.12 shows the effect of the PGS on the stacked structure. No improvement was achieved in this structure, either.

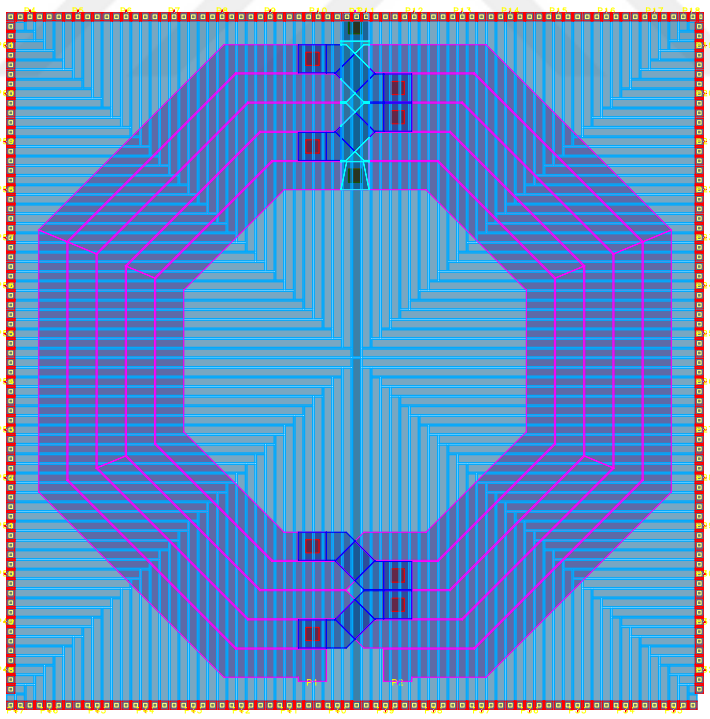


Figure 4.10. The layout of the inductor with slots and PGS.

To sum up, although it is known that PGS helps to improve the Q-factor, it could not be observed in simulations. Hence, the stacked structure with slots but without

PGS was decided to be used in the design. The final inductor has an inductance of 22.13 nH and a Q-factor of 9.45, and occupies an area of 0.493 mm^2

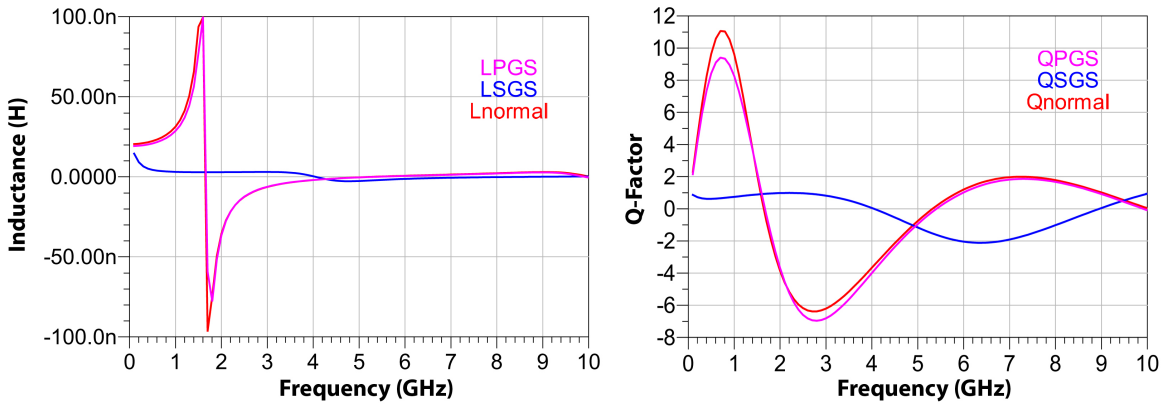


Figure 4.11. PGS and SGS effects on inductance and Q-factor of the single-layer inductor.

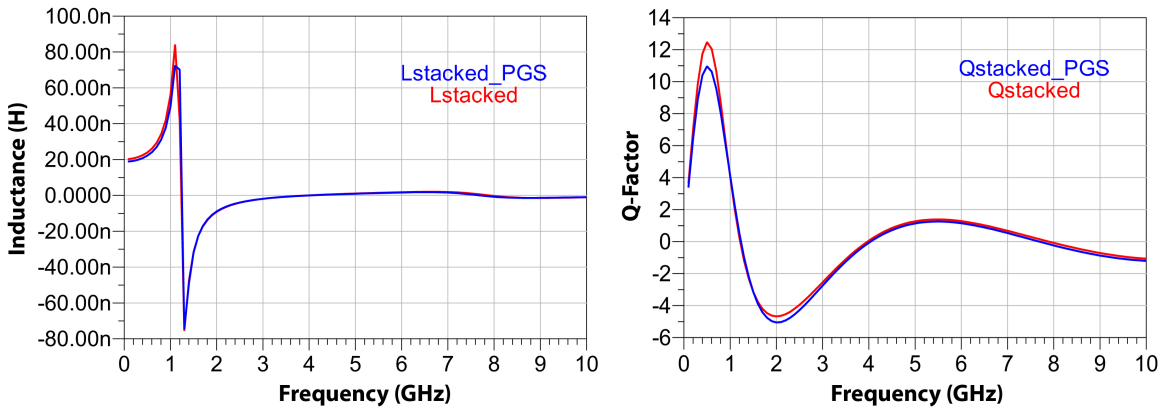


Figure 4.12. PGS effects on inductance and Q-factor of the stacked inductor.

To be able to use this inductor in circuit design, s-parameters should be turned into a lumped-element model. There are several models available in the literature [36–39] yet the model shown in Figure 4.13a which was proposed in [6] has strong advantages over others. It models the current crowding effect and distributed characteristics, as well as substrate losses, the magnetic coupling between each half of the inductor and more importantly it is a wide-band model. This model extends the region of model validity beyond the self-resonant frequency and fully supports both ac and transient circuit simulations.

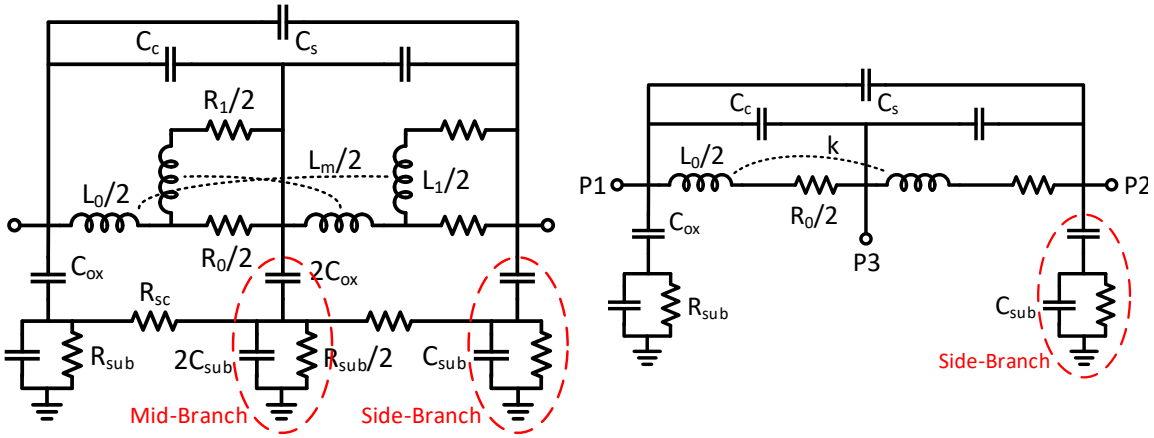


Figure 4.13. (a) 2-Π segment inductor model [6] and (b) simplified version of the model.

Element values were analytically calculated based on the inductor layout parameters for single-segment inductors in [6]. The fastest way to adapt the element values to another geometry is to use an optimizer such as the optimizer provided in ADS. Before starting optimizing, we can further simplify the model according to our needs. The targeted frequency is not very high thus the parts modeling very high-frequency effects were removed and the final model is depicted in Figure 4.13b. Simulations were performed with the model and the results are shown in Figure 4.14. Model simulation results are in a good agreement with 3D-EM simulations. However, Q-factor is deviating from the 3D-EM simulation results at high frequencies because of the modification made in the model. Yet, this has no effect on the operation of the oscillator and can be ignored.

4.1.2. Low-Noise Amplifier

Detailed analysis of fully-differential inductively-degenerated common-source LNA was presented in Section 3.1 and the schematic diagram is shown again here in Figure 4.15 for ease of reading.

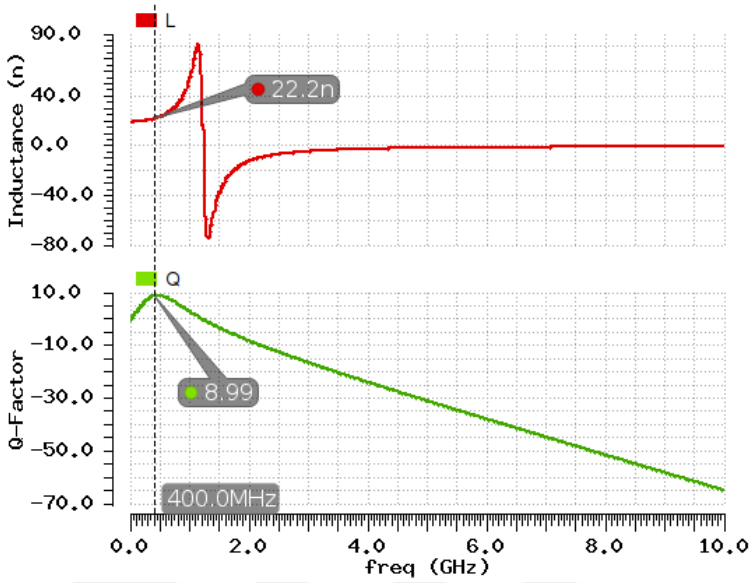


Figure 4.14. Simulation results of simplified 2-Π segment inductor model.

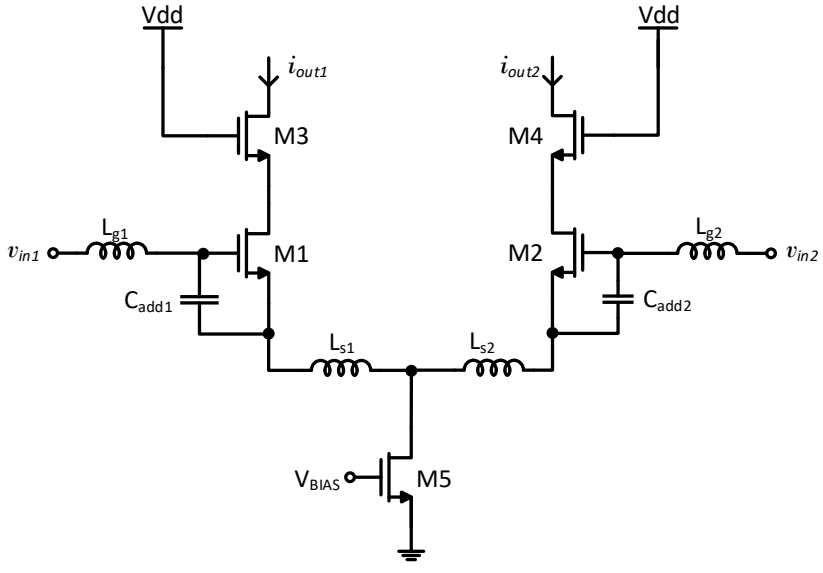


Figure 4.15. Schematic diagram of inductively degenerated fully differential low-noise amplifier.

As the inductor is presented in the foregoing section, we can now expand our noise factor analysis in Section 3.1 by including noise of the LC tank. The small-signal model use in noise analysis is depicted in Figure 4.16.

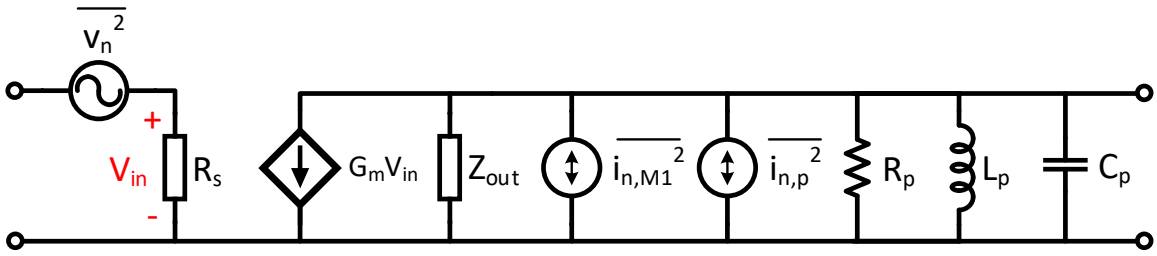


Figure 4.16. Schematic diagram of the model used in the noise analysis.

Noise current i_n is the noise current of the resistor R_p which stems from the loss of the inductor. Noise factor can be obtained as

$$F = 1 + \frac{N_{device}}{|G| \cdot^2 N_{source}} \tag{4.6}$$

where $N_{source} = 4kTR_s$ and

$$N_{device} = \overline{I_{n,M1}^2} + \overline{I_{n,p}^2} \tag{4.7}$$

$$= kT\gamma g_m + \frac{4kT}{R_p} \tag{4.8}$$

Inserting Equation 4.8 into Equation 4.6 yields,

$$F = 1 + \left(\frac{2\gamma R_s}{g_m} + \frac{1}{g_m^2} \frac{8R_s}{R_p} \right) \omega_0^2 C_{gs}^2 \tag{4.9}$$

Optimum R_s for the best noise performance can be found as

$$\frac{\partial F}{\partial R_s} = 0 \quad \Longrightarrow \quad R_{s,opt} = \frac{2g_m L_s}{C_{gs}} \tag{4.10}$$

which is the same resistance as the one found in Equation 3.19, which means that the input matching condition did not change. However, additional noise contribution from

the LC tank can be seen clearly in Equation 4.9. This suggests that the higher the gain, the less effect the LC tank noise has. To optimize the circuit, the design flow shown in Figure 3.11 was modified with new noise factor and used here as well.

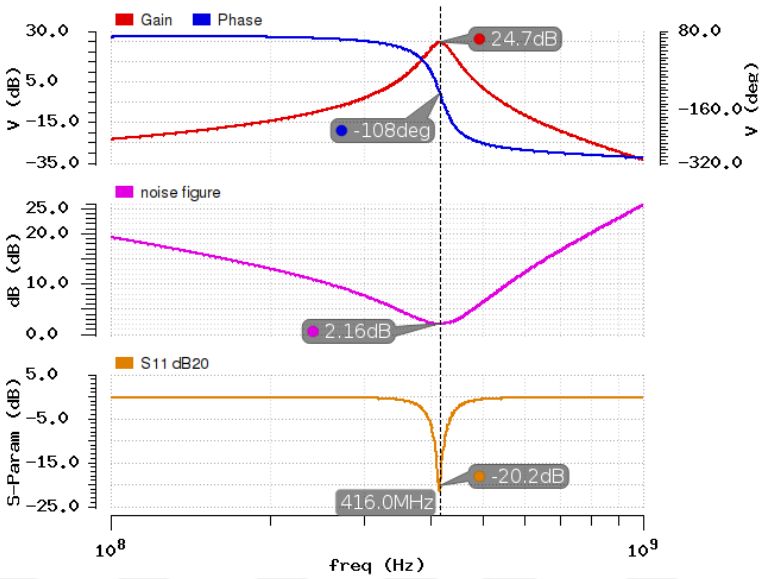


Figure 4.17. Schematic simulation results of designed LNA.

Component values for the final design are L_g=150 nH, L_s=2.7 nH, and C_{add}=351 fF. Schematic simulation results are depicted in Figure 4.17. The noise factor is not as low as the one in the modeling case as the LC tank noise is also included. At the frequency of interest, -20.2 dB S11 is reached that is well below -10 dB which is accepted as a good matching value.

The layout of the LNA is shown in Figure 4.18. MIM capacitor was used for C_{add}. Post-layout simulation results are shown in Figure 4.19. To obtain the same results as in the schematic simulations, component values in the layout were modified as L_g=133 nH, L_s=2 nH, and C_{add}=251fF. Parasitic capacitances made it necessary to decrease added capacitance. As L_g is determined such that resonance occurs at the targeted frequency, additional parasitic capacitances also made it necessary to decrease the inductance. There is a small degradation in noise performance and matching but they are still close enough to the targeted values.

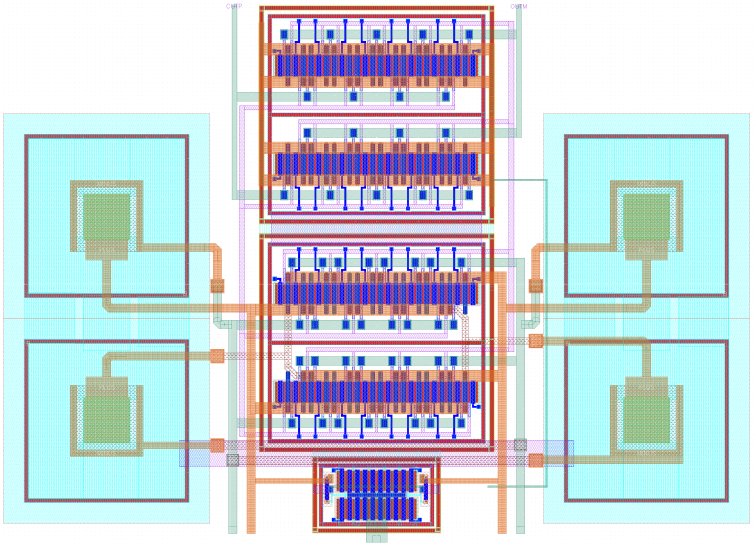


Figure 4.18. The layout of the LNA.

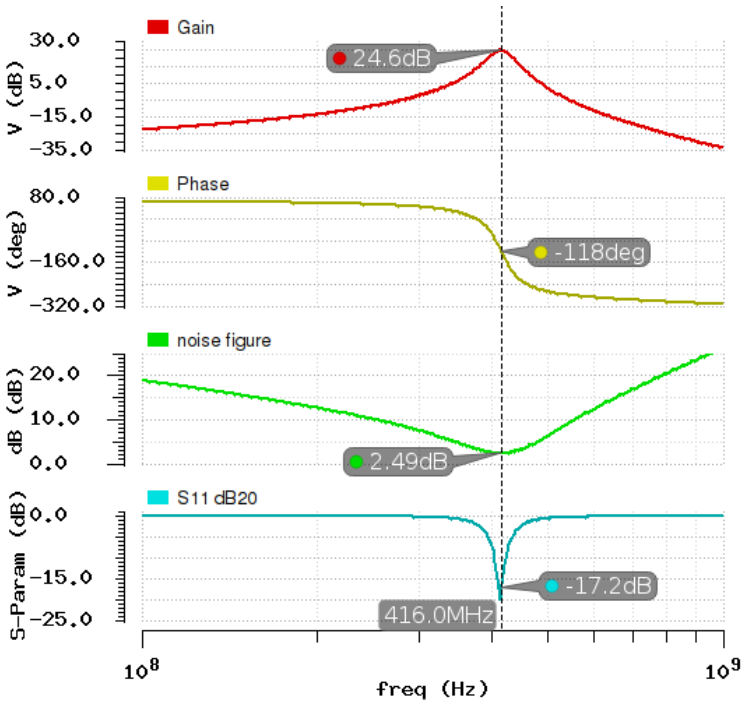
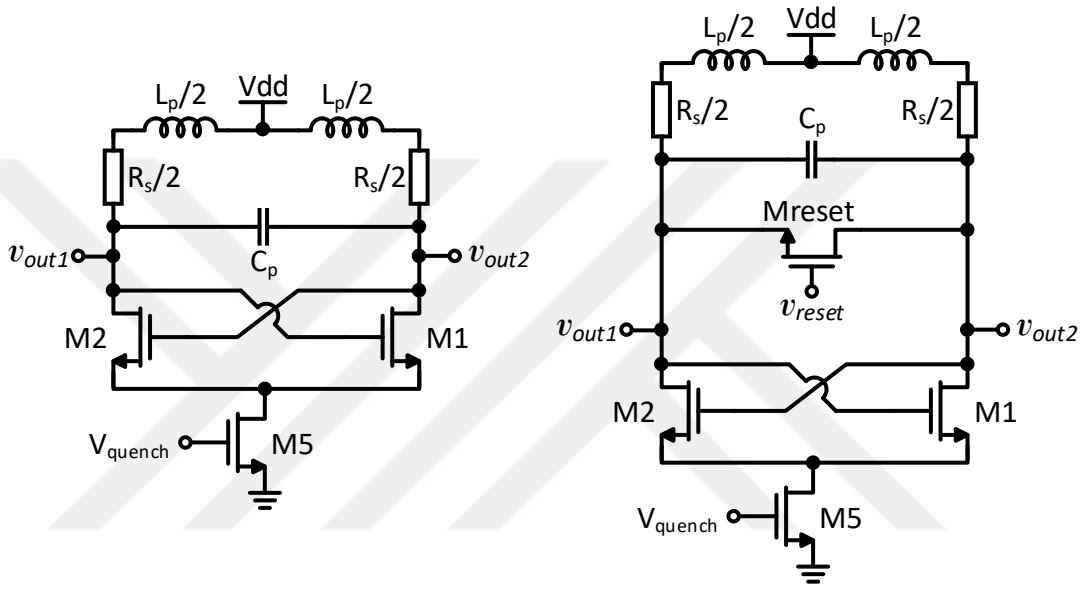


Figure 4.19. Post-layout simulation results of designed LNA.

4.1.3. Super-Regenerative Oscillator

The super-regenerative oscillator is nothing but a normal oscillator which is operated under quenched bias current. The operation was explained in Section 2.1 and Section 3.2 and the schematic of the SRO is shown in Figure 4.20a for ease of reading.



(a) (b)

Figure 4.20. Schematic diagram of the cross-coupled oscillator (a) without and (b) with reset transistor.

One of the most important performance measures in an oscillator is phase noise [30, 31]. The best phase noise is obtained with a bias current that is just enough to maximize oscillation amplitude. Further increase in the bias current increases phase noise, thus degrades the performance. Design procedure starts with determining the maximum oscillation amplitude that depends on voltage supply. DC level of the output is equal to the supply voltage in the chosen architecture. Therefore, the maximum allowed amplitude is limited by the supply voltage. However, there is another limitation to the oscillation amplitude, namely voltage stress that a transistor can withstand. During operation, gate-drain voltage of transistors in the cross-coupled pair rises up to twice the oscillation amplitude because of the differential operation. To prevent any damage to devices, this limitation must also be taken into account.

After determining the maximum oscillation amplitude, bias current can be found as the inductor value was determined earlier. Device sizing is done such that devices in the cross-coupled pair do not enter deep triode region and do stay in saturation as much as possible. The reason is to prevent parasitic capacitance at the source terminal of the pair from degrading the Q-factor of the LC tank as it is seen in series with the transistor operating in the triode region [27]. Oscillation start-up condition is

$$\frac{1}{R_p} \leq g_m \tag{4.11}$$

where $R_p = Q^2 R_s = Q\omega_0 L$. This condition states the limit where negative resistance seen from the cross-coupled pair compensates the LC tank loss. However, choosing g_m exactly as this value is not feasible because of the variations during fabrication and operation. Thus, g_m was chosen much higher than $1/R_p$ to ensure oscillation start-up.

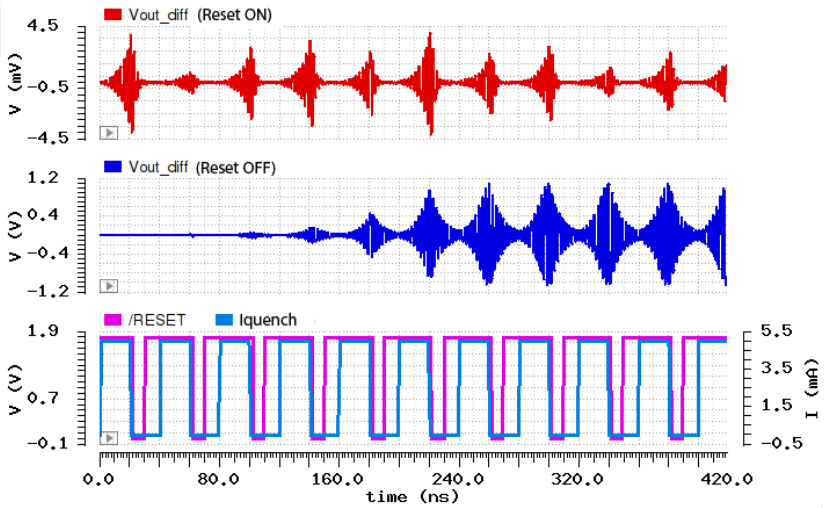


Figure 4.21. Hangover phenomenon and effect of the resetting operation.

Oscillations in each quench cycle must die out before the sensitivity period of the consequent cycle starts. At high data-rates, especially if the Q-factor of the LC tank is high, there is not enough time for the oscillation to be damped. In this case, the oscillation hasn't died out, but masks the weak input signal and reception fails. This phenomenon is called hangover [40, 41]. To prevent hangover from happening, a reset transistor is connected in parallel with the LC tank [42]. Final schematic diagram of

the SRO is shown in Figure 4.20b. This transistor is opened for a short time when the bias current is quenched to damp the oscillation quickly. To show the effect of the reset, schematic simulation results of the SRO with and without reset are shown in Figure 4.21. Although there is no input signal in simulations, oscillation grows in time and reaches to 1.2 V amplitude when reset is disabled. On the other hand, even though oscillation occurs when reset is activated, this oscillation is damped quickly in each cycle so that hangover does not happen and oscillation does not grow in time.

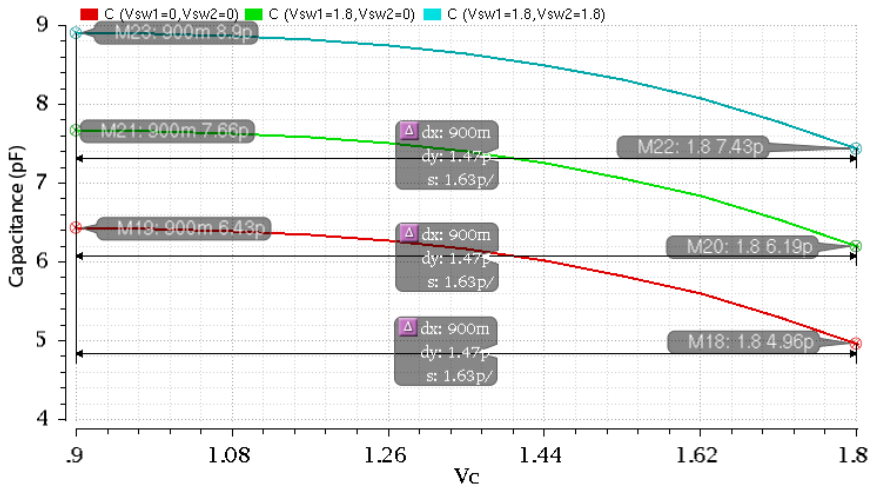


Figure 4.22. Tuning simulation results of the total capacitance in the LC tank.

Because of the variations that occur during fabrication and operation, resonant frequency of the LC tank must have programmability to ensure the operation at the frequency of interest. Varactors are one of the options to introduce programmability to the resonant frequency. However, varactors cannot be made too big since they degrade the phase noise by converting amplitude modulation at the output into phase modulation [30]. Another solution is to employ switchable capacitors to tune the resonant frequency. Although this solution does not introduce any degradation to phase noise, tuning can only be done in a discrete fashion. The best solution is to employ both of the aforementioned solutions together and use switchable capacitors for coarse-tuning and varactor for fine-tuning. Capacitance values under different configurations are depicted in Figure 4.22. Values were chosen according to the inductance value and the targeted frequency range such that there will be no dead frequency zone left.

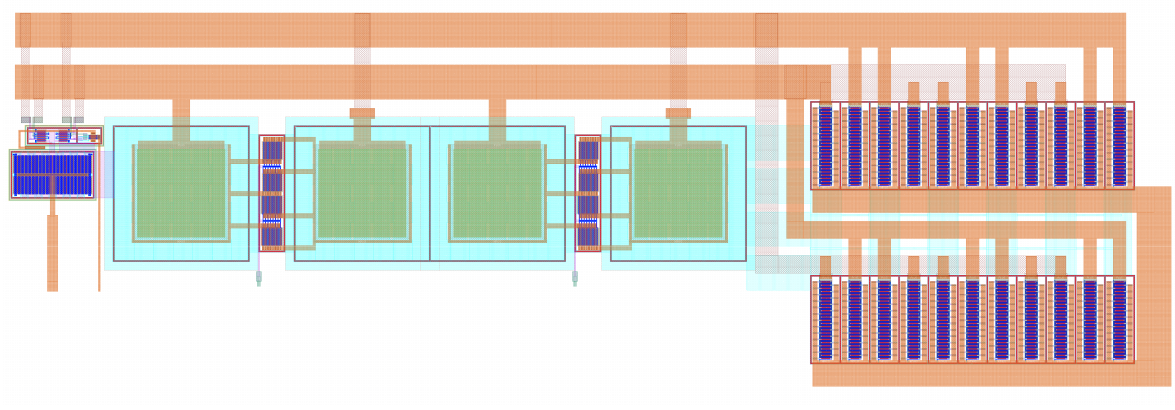


Figure 4.23. The layout of the SRO excluding the inductor.

The layout of the final design is shown in Figure 4.23. Layout of the inductor is not included and can be seen in Figure 4.7. The largest area is covered by the inductor, with varactors and capacitors coming in the second.

Operation of the SRO under square-wave quench is illustrated in Figure 4.24. Because of the square nature of the quench, sharp changes in the current causes common-mode oscillations. However, the chain is fully differential so that these common-mode oscillations are suppressed in the consequent blocks.

Schematic and post-layout transient simulation results of the SRO are shown in Figure 4.25a and Figure 4.25b, respectively. Oscillation start-up time is not very reliable because of the nature of the simulators and pseudo-random noise generation. Layout parasitics necessitate to change the bias voltage of the varactor to achieve the same oscillation frequency and degrade the overall Q-factor of the LC tank that the oscillation amplitude decreases, yet stays in the acceptable range.

Phase noise simulation results of the SRO are shown in Figure 4.25a and Figure 4.25b for the schematic and post-layout, respectively. There is a small degradation in phase noise response because of the aforementioned reasons. However, degradation is small and performance is as expected.

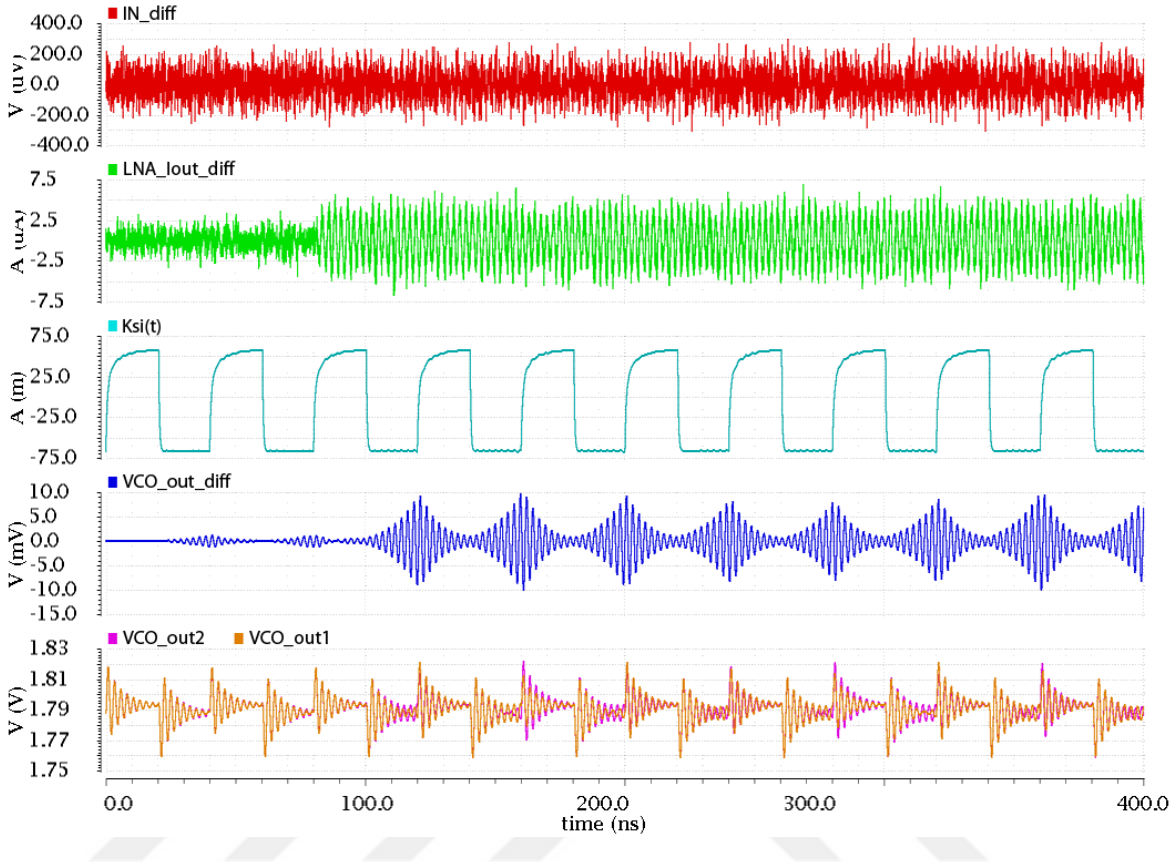
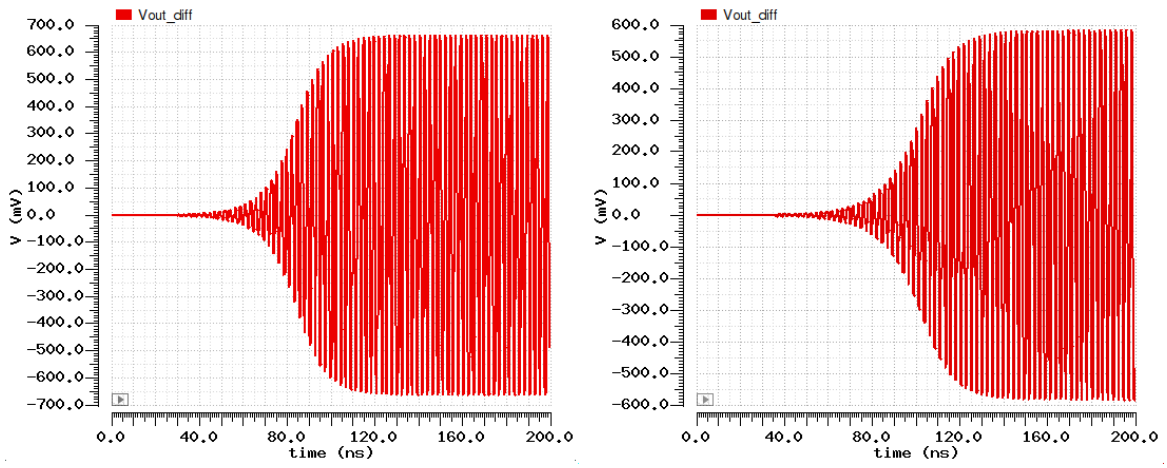
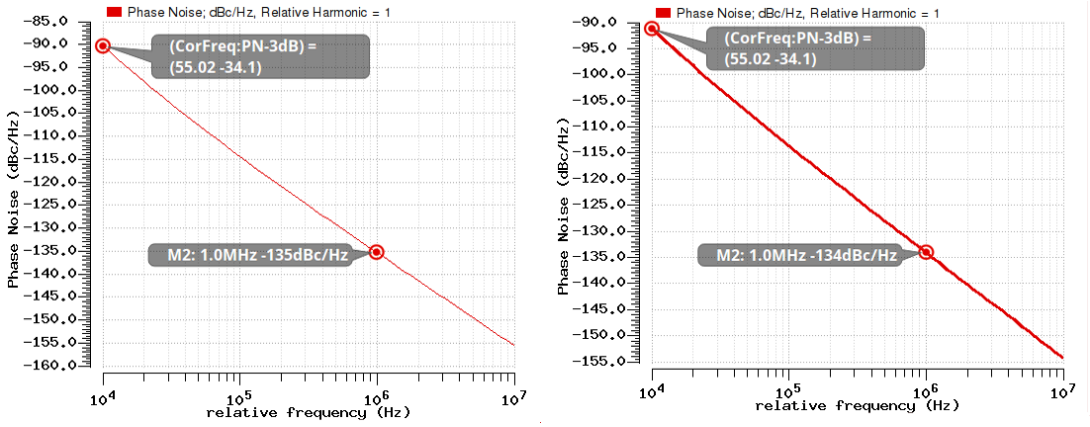


Figure 4.24. Transient simulation results of the SRO including the LNA under square quench signal.



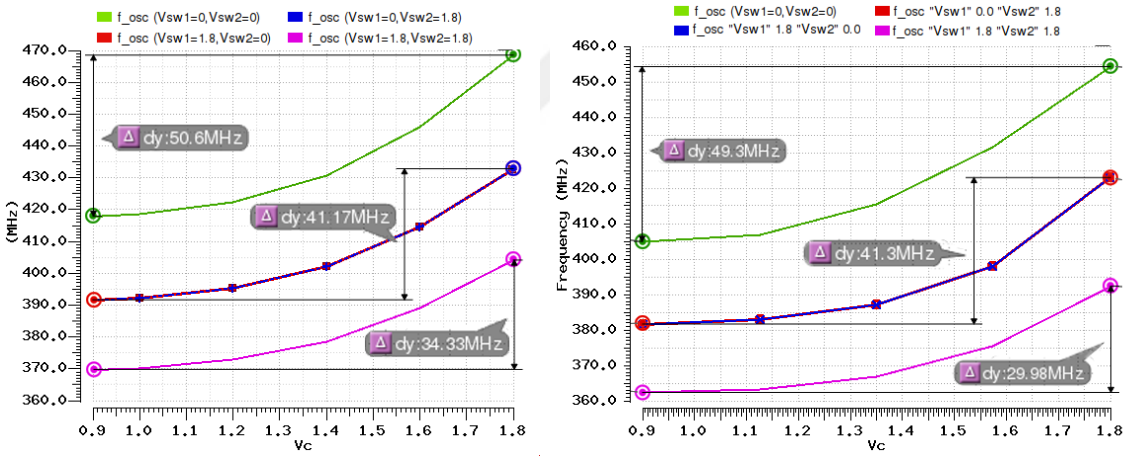
(a) (b)

Figure 4.25. (a) Pre-layout and (b) post-layout transient simulation result of the SRO.



(a) (b)

Figure 4.26. (a) Pre-layout and (b) post-layout phase noise simulation result of the SRO.



(a) (b)

Figure 4.27. (a) Pre-layout and (b) post-layout frequency tuning simulation results.

Schematic and post-layout simulation results for the oscillation frequency tuning are shown in Figure 4.27a and Figure 4.27b, respectively. Layout parasitic effects can be clearly seen from these results as the maximum oscillation frequency and tuning range decrease, yet the whole range is still covered.

4.1.4. RF Amplifier

As mentioned previously, the envelope detector takes the square of the incoming signal. Thus, employing an amplifier in advance of the envelope detector provides advantages. The main need for the amplifier before the envelope detector stems from the quenching operation. In each quench cycle, output common-mode voltage of the SRO changes. Because of the structure of the envelope detector, the common-mode change is directly transferred to the output, whereas the envelope of the RF signal is transferred to the output by being squared. As the signal amplitude is small, squared amplitude becomes smaller and the envelope of the RF signal is masked by common-mode voltage fluctuations. A differential amplifier solves common-mode voltage fluctuation problem as it blocks common-mode voltage and only amplifies the differential signal.

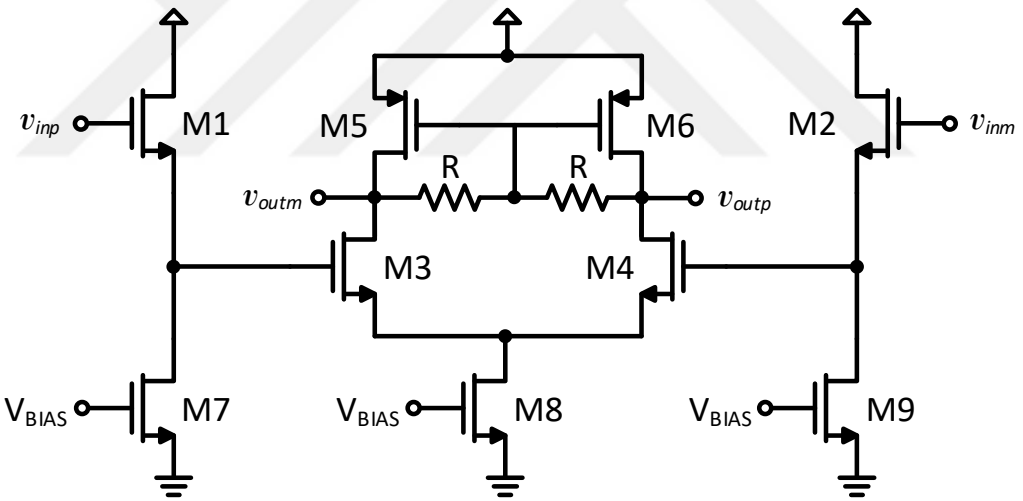


Figure 4.28. Schematic diagram of the RF amplifier.

Schematic diagram of the fully-differential active load RF amplifier is shown in Figure 4.28. Source follower stages at the input of the amplifier decrease common-mode voltage to leave enough margin for proper operation. Resistors at the output provide common-mode feedback to the active load and stabilize output common-mode voltage. This feedback voltage is also provided to the pseudo-differential envelope detector's one half which only generates common-mode voltage for the subsequent block.

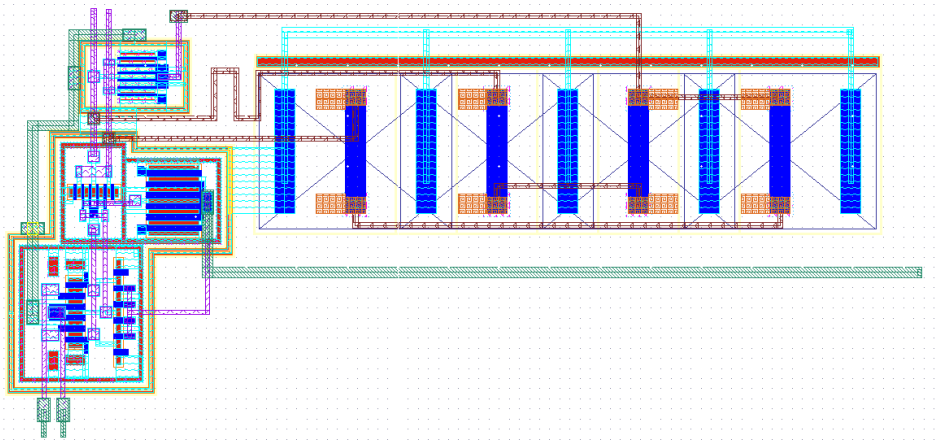


Figure 4.29. The layout of the RF amplifier.

Schematic and post-layout simulation results of the amplifier are provided in Figure 4.30a and Figure 4.30b, respectively. Since resistors were employed at the output, the main drawback was the parasitics caused by bulky resistor layouts. This effect can be seen from the difference in bandwidth in post-layout simulations. It is not a good practice to have bandwidths close the frequency of interest, however, the circuit still performs its first duty that is to suppress the common-mode voltage.

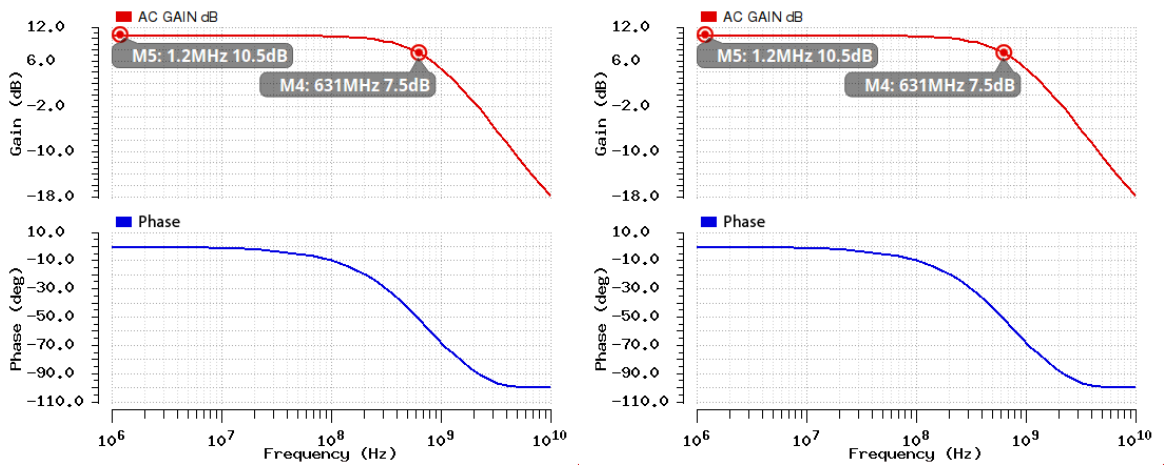
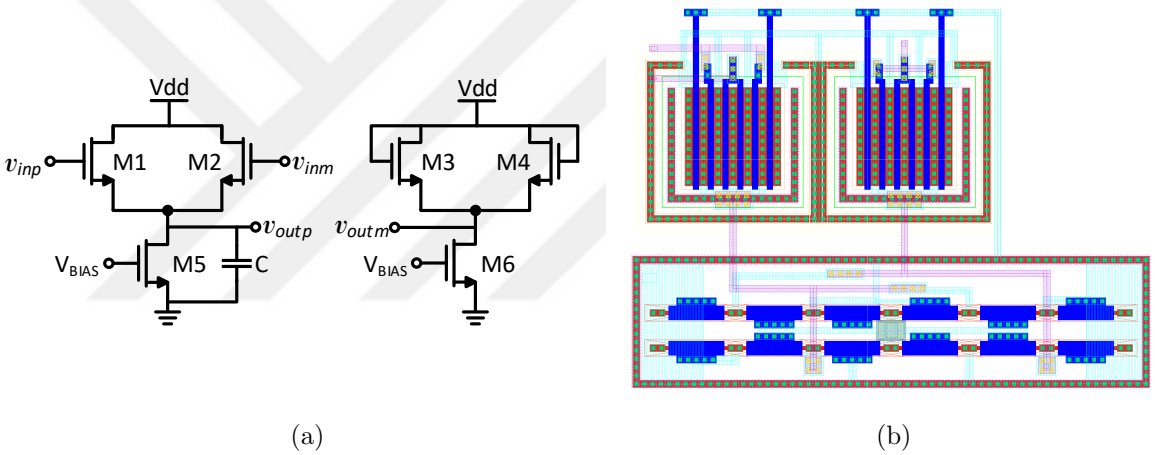


Figure 4.30. Bode diagrams of the RF amplifier (a) in schematic simulations and (b) in post-layout simulations.

4.1.5. Envelope Detector

Envelope detector operation is analyzed and explained in detail in Section 3.3. Schematic of the envelope detector is shown in Figure 4.31a again for ease of reading. As the voltage gain of the envelope detector is related only to the input amplitude as long as input transistors stay in the week-inversion region, bias condition is determined only by the frequency response of the circuit. Parasitic capacitance at the output together with the circuit's output resistor forms a pole and location of the pole can be arranged by the transconductance of input transistors.



(a) (b)

Figure 4.31. (a) Schematic diagram and (b) the layout of the envelope detector.

The layout of the envelope detector is depicted in Figure 4.31b. In order not to decrease common-mode voltage of the output and to leave enough margin for the subsequent blocks, bulk terminal of the input pair was connected to source terminal. In addition to that, thick gate-oxide transistors were employed for current mirrors to obtain better stability in DC bias.

As the transfer function of the envelope detector is non-linear, standard small-signal AC analysis cannot provide characteristics of the circuit. Instead, transient simulations were performed to analyze the behavior. Time-domain simulation results of the envelope detector are depicted in Figure 4.32a and Figure 4.32b for schematic and post-layout simulations, respectively. As can be seen from time-domain results,

there is almost no difference between schematic and post-layout simulations. The main reason behind this is that the circuit is too small to see any severe parasitic effects. After the layout of the whole receiver is completed and the subsequent blocks are connected, there will be additional parasitic effects. However, these parasitics will only affect the frequency response and can be compensated by modifying the bias current.

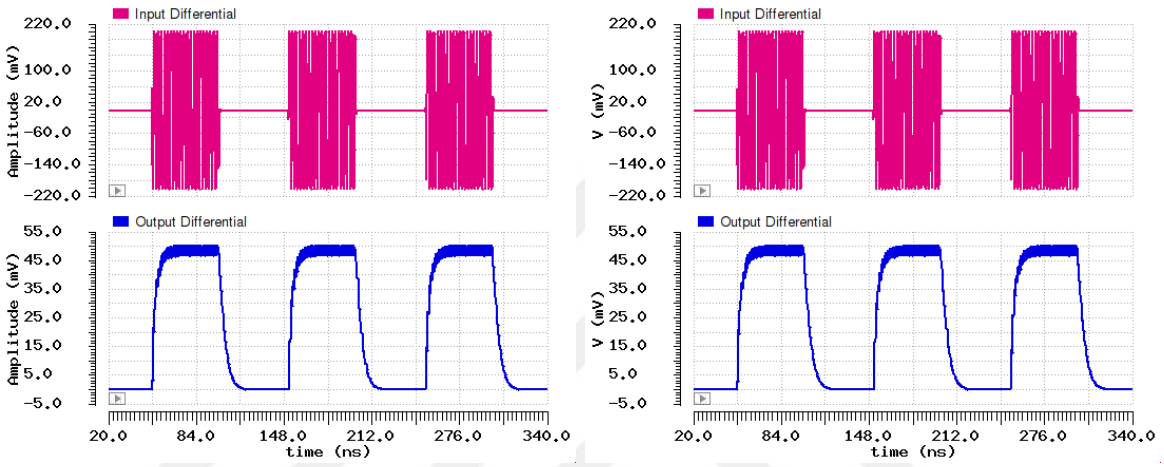


Figure 4.32. Time-domain operation of the envelope detector (a) in schematic simulations and (b) in post-layout simulations.

4.1.6. Base-Band Amplifiers

Analog-to-digital conversion at the end of the receiver chain will be performed by means of a comparator. In order to ease the specifications of the comparator, additional signal amplification is needed since the amplitude of the envelope signal is too small to be processed with high precision and accuracy in the comparator.

Since the low-power operation is the main bottleneck in the targeted applications, the lower the power supply voltage, the better the power efficiency. To be able to lower the power supply voltage, cascode structures should be avoided if there is no control over the threshold voltage of transistors. Therefore, two cascade gain stages were employed to obtain the targeted amount of amplification.

4.1.6.1. Active Load Amplifier. Differential operation is in favor of suppressing the common-mode fluctuations and even harmonics generated by non-linearities. Since low-power is targeted, the simplest fully-differential architecture is used. Schematic of the fully-differential active-load base-band amplifier is shown in Figure 4.33a. Passive common-mode feedback provides power efficiency and simplicity.

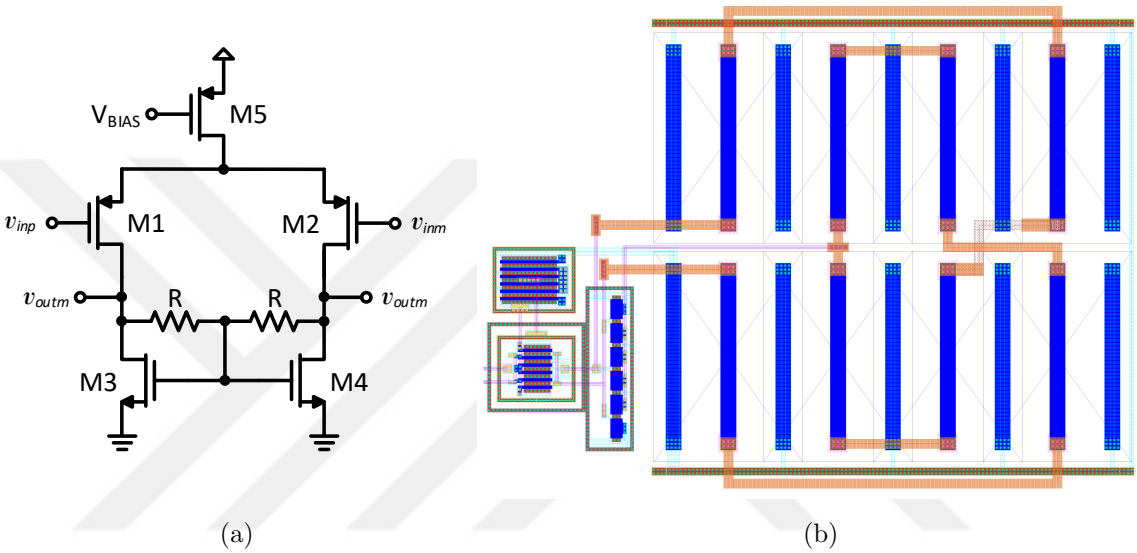
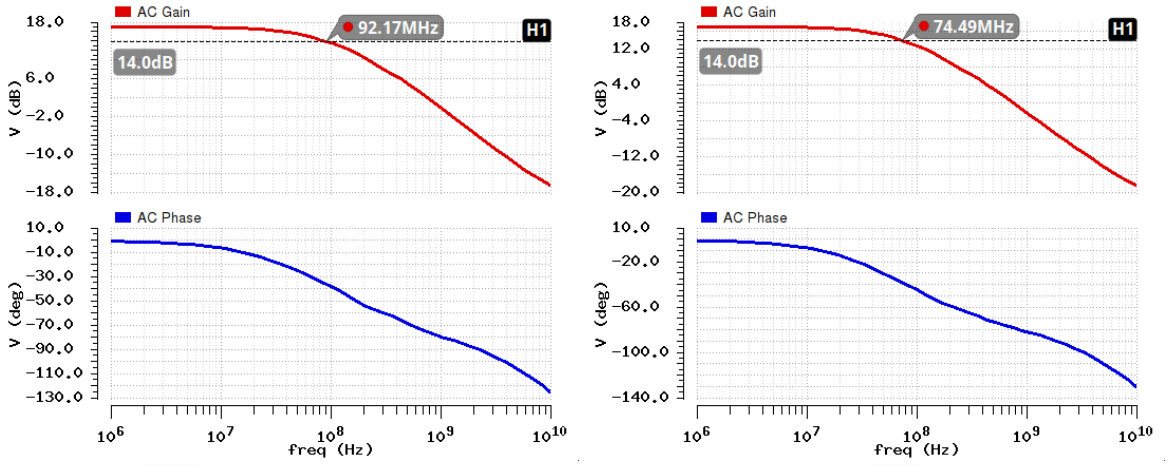


Figure 4.33. (a) Schematic diagram and (b) the layout of the active load amplifier.

The layout of the amplifier is shown in Figure 4.33b. The bulkiest part in the layout is resistors. They occupy a large area and bring high parasitic capacitances. However, the trade-off made here is the power and these drawbacks are acceptable as long as targeted performances are achieved.

Schematic and post-layout simulation results of the amplifier is provided in Figure 4.34a and Figure 4.34b, respectively. Since resistors were employed at the output, the main drawback was the parasitics caused by bulky resistor layouts. This effect can be seen from the difference in bandwidth in post-layout simulations. As the targeted base-band operation is at 10 MHz, the obtained bandwidth satisfies the requirements.

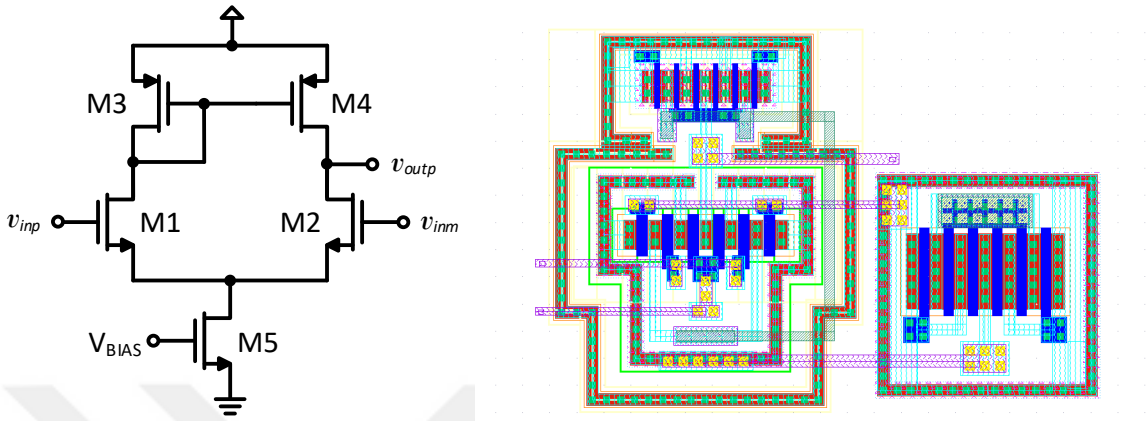


(a) (b)

Figure 4.34. Bode diagrams of the active load amplifier (a) in schematic simulations and (b) in post-layout simulations.

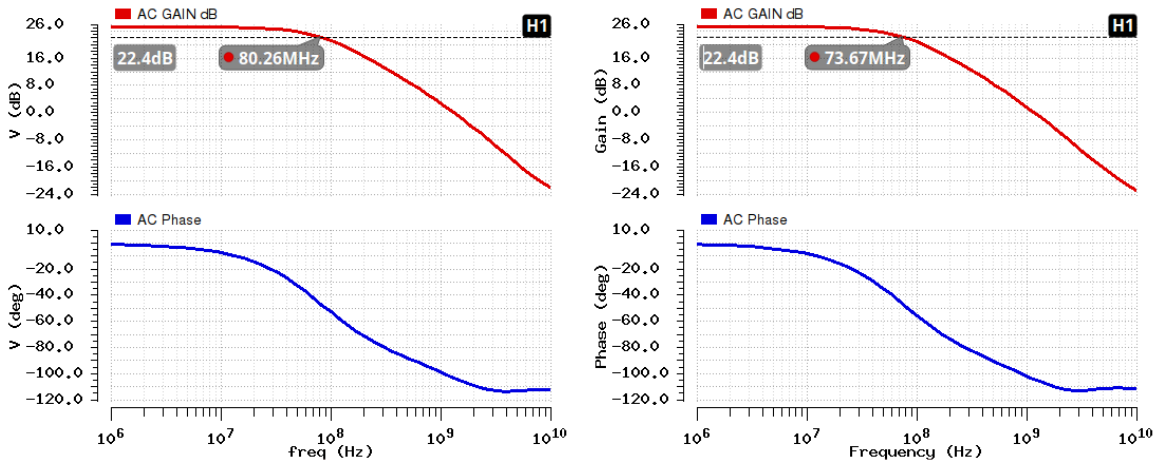
4.1.6.2. Current Mirror Load Amplifier. Comparator performs the comparison of a signal with a given reference which can be another signal or a fixed reference. Differential signal must be converted into single-ended before being fed to the comparator. The best choice to perform this conversion while maintaining the gain accumulated in the differential signal is to use current mirror load amplifier architecture. Schematic diagram of the amplifier is shown in Figure 4.35a. This structure maintains the advantageous of the differential amplification while converting the differential signal into the single-ended signal. Thanks to the current mirror load, this architecture does not need common-mode feedback for DC stability. The layout of the amplifier is shown in Figure 4.35b.

Bode plots obtained from schematic and post-layout simulation results are shown in Figure 4.36a and Figure 4.36b, respectively. Parasitic effects can be seen from bandwidth values. However, effects are not as severe as it was in the previous amplifier since there is no resistor used in this amplifier and the design does not occupy a large area that interconnects do not bring big parasitics.



(a) (b)

Figure 4.35. (a) Schematic diagram and (b) the layout of the current mirror load amplifier.

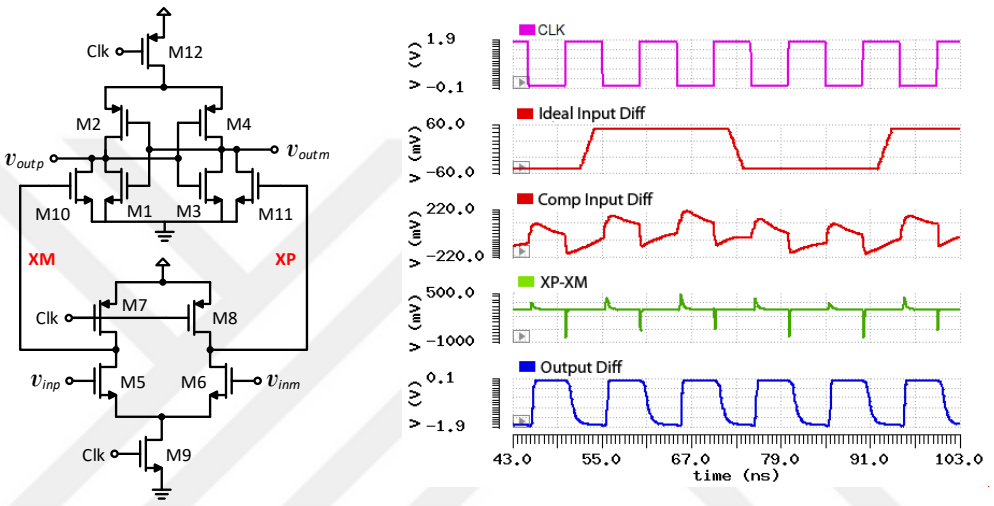


(a) (b)

Figure 4.36. Bode diagrams of current mirror load amplifier (a) in schematic simulations and (b) in post-layout simulations.

4.1.7. Comparator

Comparator is a very critical block in the chain since it directly affects the error rate in reception. Analog-to-digital conversion is performed in this block so that a possible inaccuracy in this stage directly makes output erroneous. Thus, the accurate operation of the comparator is of high importance.



(a) (b)

Figure 4.37. (a) Schematic diagram and (b) time-domain operation of the double tail comparator.

One of the most popular comparator structure is shown in Figure 4.37a. There are two branches in this architecture so that it is called as double-tail comparator [43]. The first stage is nothing but an amplifier which is reset periodically. In the comparison phase, PMOS pair in the comparator is turned-off and input pair drains parasitic capacitances at the output with a rate related to the input voltage. If the differential signal is positive, XM node is drained faster and vice verse. Second tail consists of a latch which regenerates the signal by means of transistors M10 and M11 and the voltage difference between XP and XM nodes. Thus, the input signal is converted into digital. However, XP and XM nodes are switched between the power supply and ground sharply in each cycle causing a severe kick-back noise problem. Time-domain simulation results are shown in Figure 4.37b. Kick-back problem can be clearly seen from the difference between the ideal input signal and the signal at the input of the

comparator. Kick-back problem is so severe that comparator generates faulty output. The main reason is very high output resistance of the preceding stage, yet it cannot be change since gain is obtained thanks to that high output resistance. Another solution can be to insert a buffer stage between the amplifier and the comparator. However, it needs to be operated continuously and causes additional power consumption.

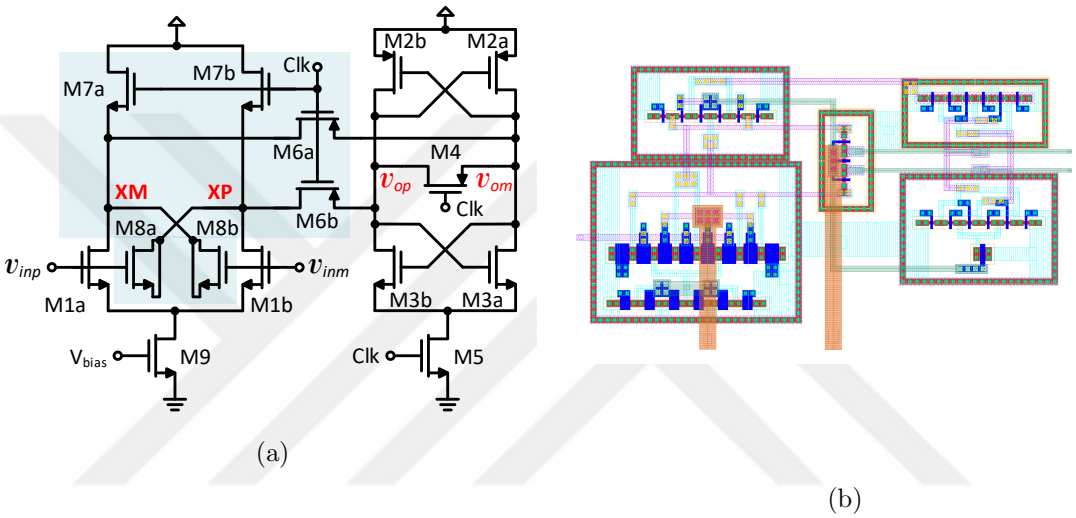
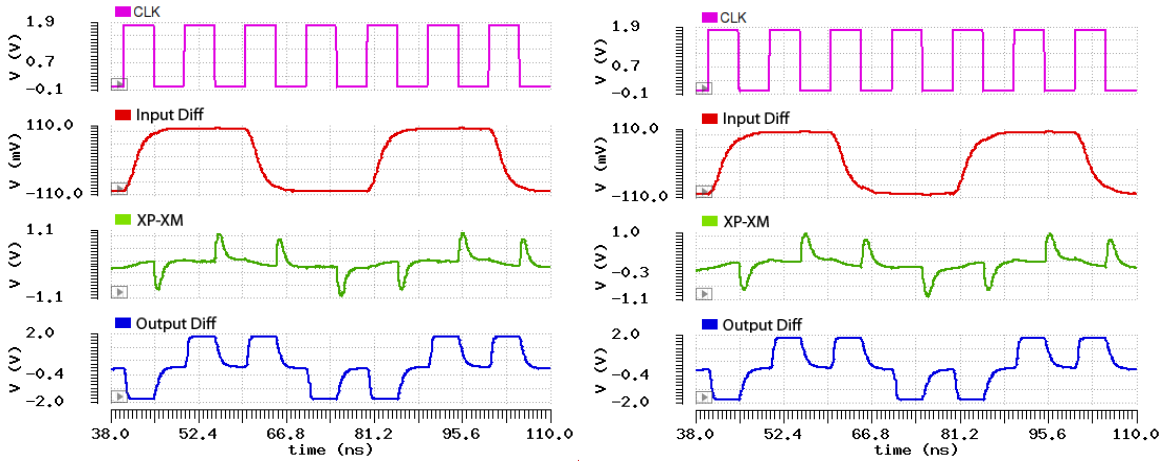


Figure 4.38. (a) Schematic diagram and (b) the layout of the class-AB latched comparator with kickback reduction.

To solve the kickback problem, the architecture shown in Figure 4.39a was utilized. This architecture is a modified class-AB latched comparator. Transistors in the shaded area are added to the classic class-AB latched comparator to suppress kick-back effect. Transistors $M6_{a,b}$ disconnect the input stage from the latch side in the decision phase so that XP and XM nodes are not affected by this switching activity. Transistors $M7_{a,b}$ provide bias current when the input stage is disconnected from the latch side. Transistors $M8_{a,b}$ are cross-connected and both drain and source terminals are connected together. These transistors are half the size of the input transistors to obtain the same parasitic capacitance since both drain and source terminals are used. As a result any residual fluctuations in XP an XM are canceled out by the parasitic capacitor currents. Layout of the comparator is shown in Figure 4.38b.



(a) (b)

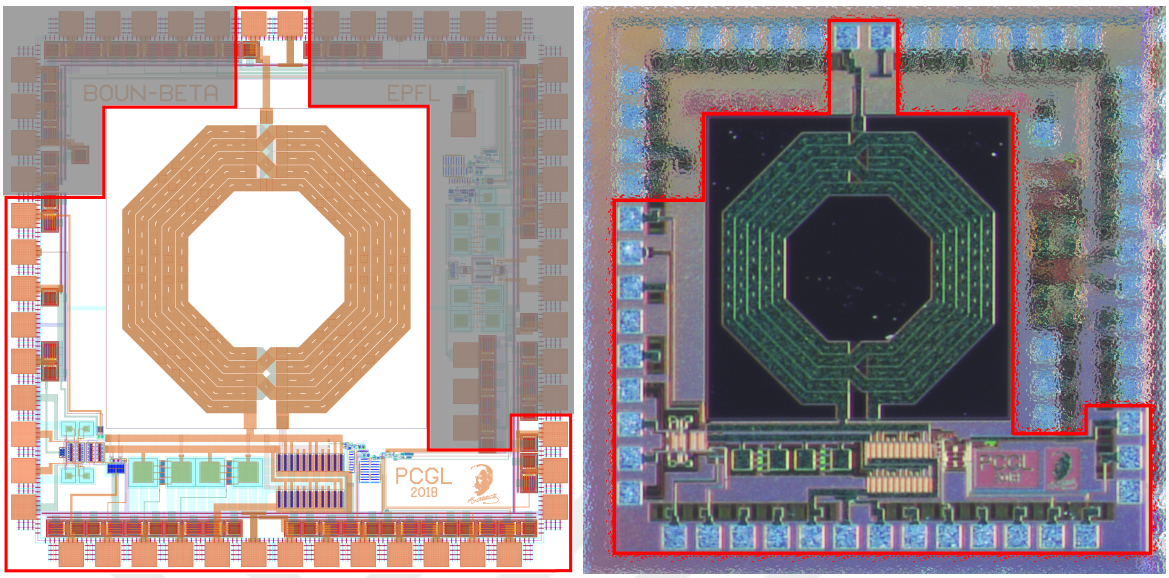
Figure 4.39. (a) Schematic and (b) post-layout simulation results of the class-AB latched comparator with kickback reduction.

Schematic and post-layout simulation results of the comparator are depicted in Figure 4.39a and Figure 4.39b, respectively. There is still fluctuation in XP and XM nodes at the falling edge of the clock, yet almost none is reflected to the input. Comparator operates correctly as there is almost no kick-back noise left at the input.

4.2. Measurement Results and Discussion

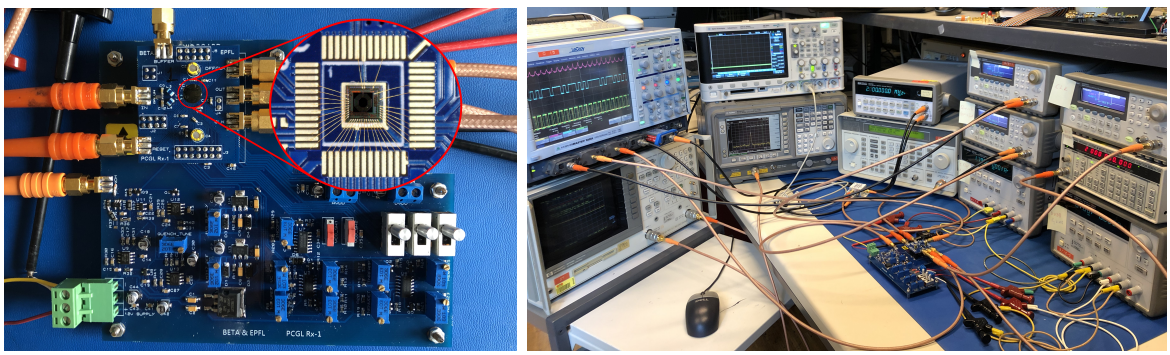
Layout and micro-photograph of the whole receiver including active area and pads are shown in Figure 4.40a and Figure 4.40b, respectively. The core of the receiver occupies 1.02 mm^2 area most of which is occupied by the inductor. Because of the low operating frequency, the inductor needs to occupy a large area to obtain the peak of the Q-factor at the frequency of interest. In addition to circuits, pads and ESD protection devices were designed since the PDK did not provide them.

Test boards including chip board and bias generator board are shown in Figure 4.41a along with wire-bond photograph. Bias board includes adjustable DC bias current generators as well as high-frequency voltage-to-current convertor. Voltage-to-current converter was designed since programmable current waveform generators were



(a) (b)

Figure 4.40. (a) The layout and (b) micro-photograph of the receiver employing inductors.



(a) (b)

Figure 4.41. (a) Test board and (b) test setup photographs of the receiver employing inductors.

not available. This was one of the limiting factors of performance in the measurements because it is hard to generate square current waveforms with sharp edges at high data-rates.

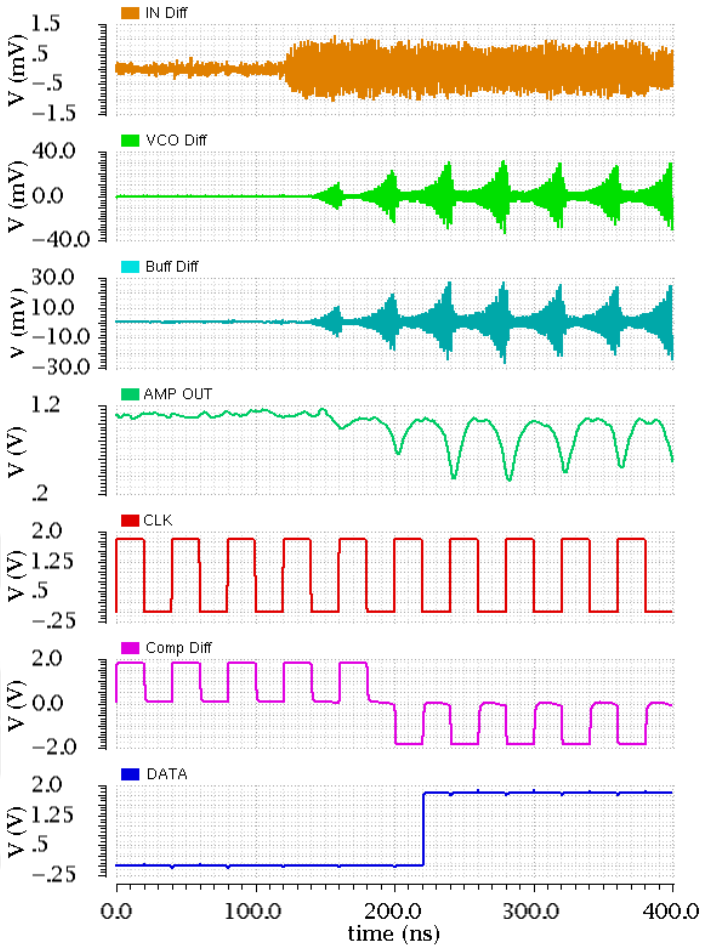


Figure 4.42. Post-layout simulation of the whole receiver on the final layout.

Post-layout simulation results are shown in Figure 4.42. These simulations were performed with the final layout including additional buffers for characterization, pads, ESD devices, antenna-effect protection diodes and all other additional components which were not included in previous simulations. In the first quench cycle, the regenerated signal amplitude is lower than the subsequent periods since the input signal is inserted in the middle of the sensitivity period of the corresponding quench cycle. This decreases the overall gain in regeneration and results in lower oscillation amplitude.

OOK data generation was achieved through an RF switch. Oscilloscope screenshot of the OOK data generated at -30 dBm power and 2 Mbps data-rate at 416 MHz is shown in Figure 4.43. Peaks at the beginning and end of the data period occur because of sharp switching however, does not affect the operation of the receiver.

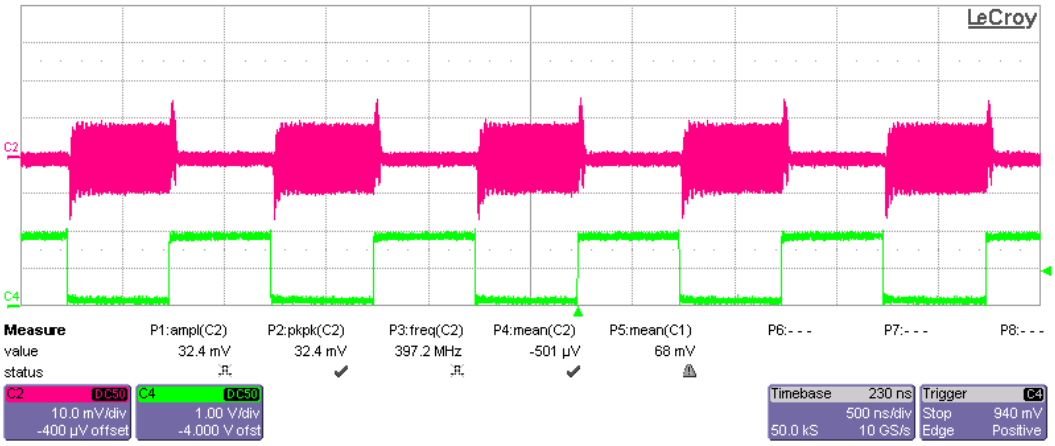
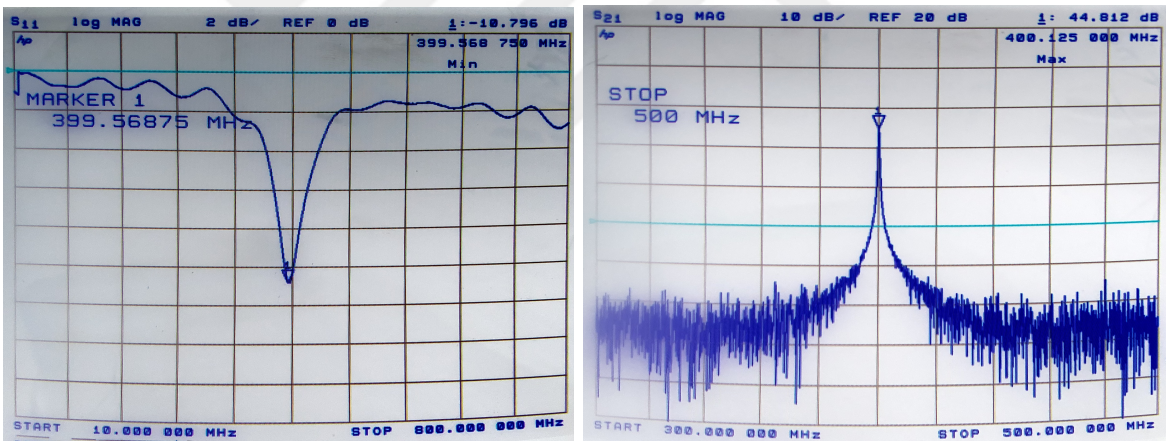


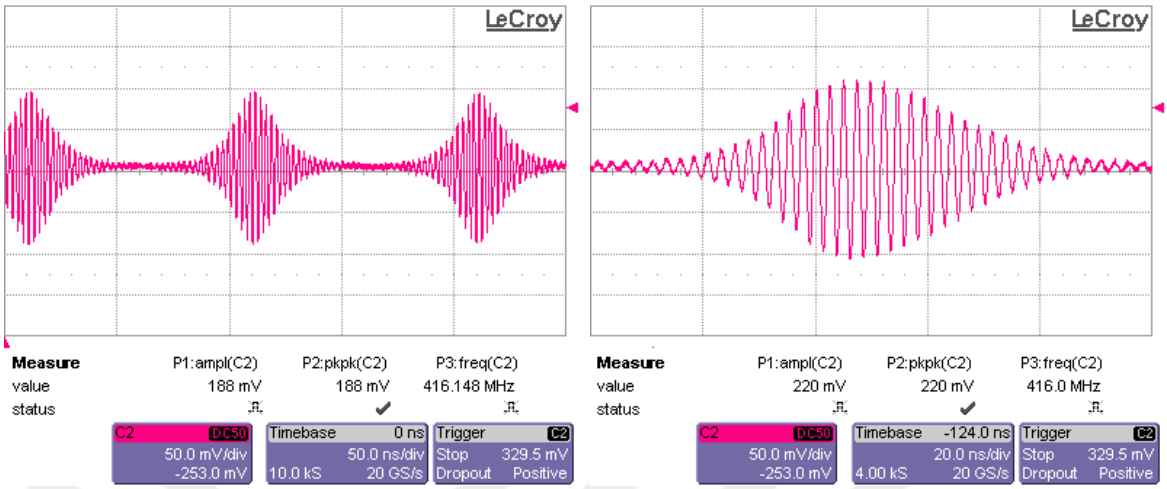
Figure 4.43. Oscilloscope measurements of OOK data generated at -30 dBm power and 2 Mbps data-rate at the operating frequency.



(a) (b)

Figure 4.44. Network analyzer screen photographs of (a) S11 and (b) S21 measurements of the LNA.

Network analyzer screen photos are shown in Figure 4.44a and Figure 4.44b for S11 and S21 measurements, respectively. In post-layout simulations, gate inductor L_g was set to 135 nH but in tests, 68 nH inductor needed to be used because of additional parasitic capacitances introduced by chip PCB. With this new inductance value, input matching was obtained at 400 MHz. Discrete inductance values are available only with fixed values. Thus, the operation was performed at 400 MHz hereafter.



(a) (b)

Figure 4.45. Oscilloscope measurements oscillation waveforms (a) for square-wave and (b) for sinusoidal quench signals.

The SRO was tested under different shape quench signals. Oscilloscope screenshots showing the output signal of the SRO are shown in Figure 4.45a and Figure 4.45b for 10 MHz square-wave and sinusoidal quench signals, respectively. Since the quench signal frequency is high, shapes are not very sharp yet square-wave quench generates exponential envelope whereas sinusoidal quench generates Gaussian-like envelope.

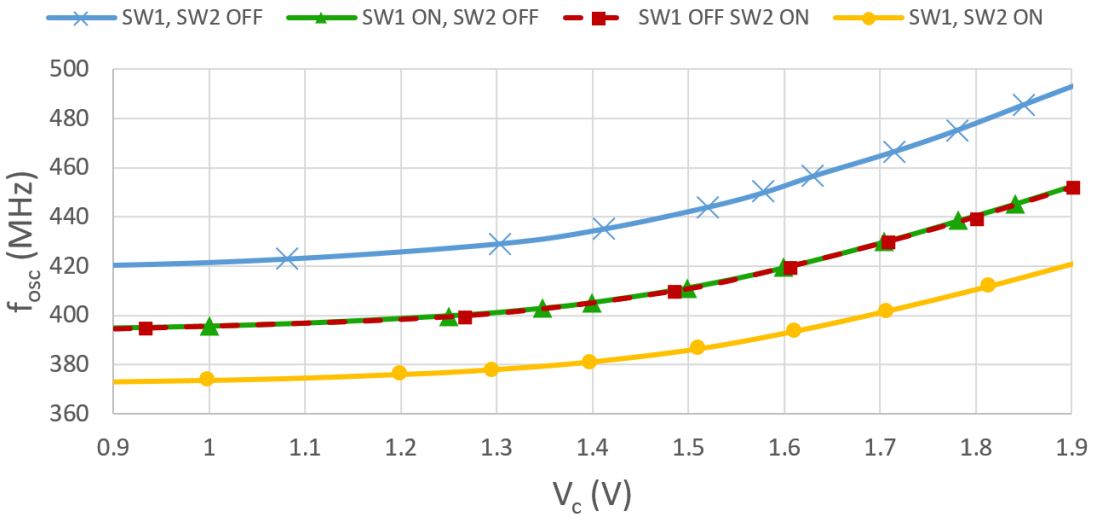
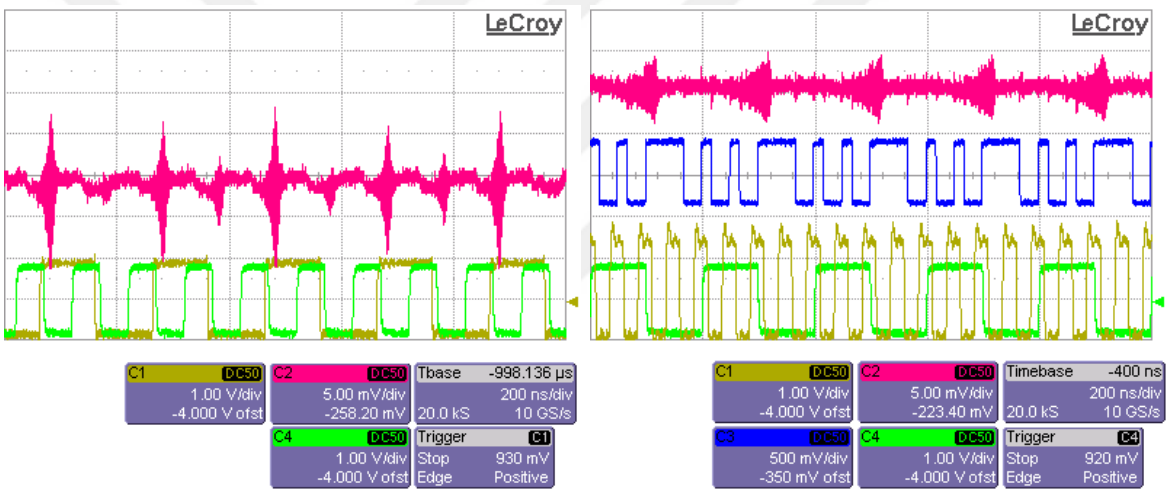


Figure 4.46. Frequency tuning measurements of the SRO.

Frequency tuning measurements were performed for all combinations of settings. Oscillation frequency with respect to the configuration was plotted and depicted in Figure 4.46. Results show the perfect symmetrical operation of the tuning for each switched capacitor, namely SW1 and SW2. Tuning range and tuning values are in perfect alignment with schematic simulations. It would be expected to obtain results close to the post-layout simulations. However, measurement results show less parasitic effects compared to the post-layout simulations. Moreover, oscillation frequency was measured in three different dice for the same bias conditions and oscillation frequency change among dice was 0.24% at 416 MHz center frequency.



(a) (b)

Figure 4.47. Oscilloscope measurements of the operation (a) showing the SRO output and (b) showing the data output.

Only three dice were bonded and all the measurements were performed on them. However, since there was no ESD protection in LNA inputs, the LNA did not work in two dice out of three. In the die in which the LNA worked, the rest of the chain did not work. Thus, reception results could not be taken on a single die as a whole. Therefore, one die was used to regenerate the received signal and another die was used to test the rest of the receiver chain. Figure 4.47a shows oscilloscope screenshot of the regeneration tests with -80 dBm 10 Mbps data input and 10 MHz square-wave quench signal with 4.6 mA amplitude. C2 shows the SRO output, C1 shows the data trigger (active-low), and C4 is the quench trigger. Regeneration was performed in one out

of two quench cycles as quench signal frequency is twice the input frequency. 20 mV regeneration amplitude was achieved. Figure 4.47b shows oscilloscope screenshot of the SRO output at 10 Mbps data-rate with 8.7 mV amplitude. C1 shows comparator clock trigger, C2 shows the SRO output, C3 shows the data output, and C4 shows the quench trigger. SRO output amplitude was held lower in this test to prove that data output can be generated in the worst case. Comparator and DFF clock frequency was set to 20 MHz. There was a problem with DFF that at the end of each cycle it was reset to logic high. Further tests with more dice must be performed to determine the cause of this problem. The data output is set to logic high once out of four cycles and the clock frequency is four times the data frequency.

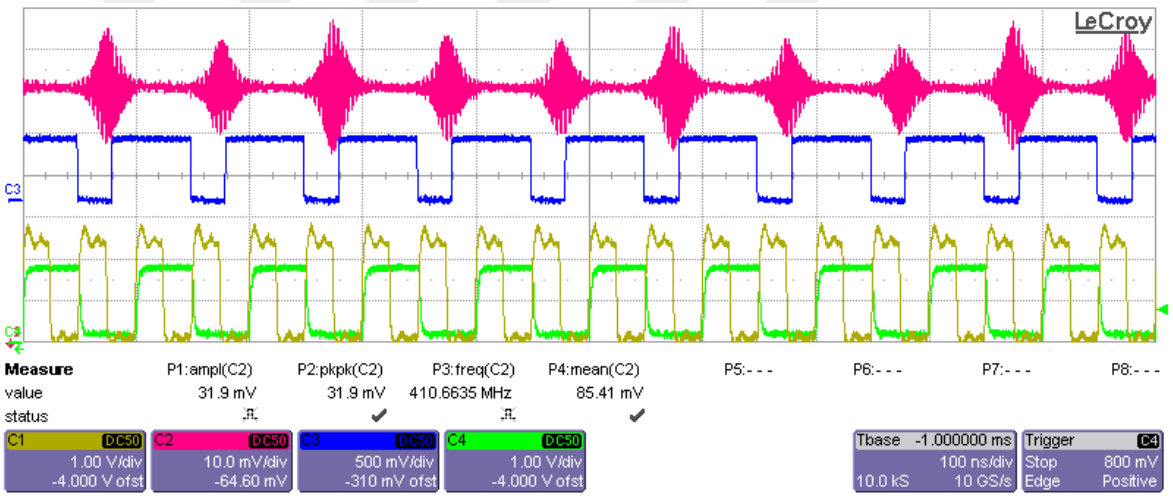


Figure 4.48. Operation of the system with 1.1 V power supply voltage.

The final test was aiming to lower the supply voltage. Unless transistors in circuits are not pushed into linear operation region, the receiver should work properly. Figure 4.48 shows the operation of the receiver under 1.1 V power supply. As no cascode architecture was used in the chain to be able to lower the power supply voltage to obtain lower power consumption, the operation was not disrupted.

Table 4.4. Comparison with the previous work.

	Proposed Receiver	**[26]**	**[44]**	**[45]**
Publication Year	2019	2010	2011	2013
Process	180 nm CMOS	180 nm CMOS	130 nm CMOS	90 nm CMOS
Active Area	1.02 mm^2	2.15 mm^2	0.69 mm^2	0.49 mm^2
Modulation	OOK	OOK	OOK	OOK
Freq. Band	375-415 MHz	402-405 MHz	495-505 MHz	392.16-416.94 MHz
Quench Shape	Square	2-Step Square	Square	Square
Data Rate (max)	10 Mbps	1 Mbps	10 Mbps	1 Mbps
Sensitivity	-90 dBm @ 1 Mbps -80 dBm @ 10 Mbps	-85 dBm @ 1 Mbps	-85dBm @ 10 Mbps	-80dBm @ 500 Kbps -65dBm @ 1 Mbps
Supply Voltage	1.1 V	1.3 V	1.2 V	0.8 V
Power	9.32 mW @ 10 Mbps	2.2 mW	0.96 mW	180 μW
Energy per Bit	0.93 nJ/b @ 10 Mbps	NA	NA	0.18 nJ/b @ 1 Mbps 0.256 nJ/b @ 500Kbps
FOM	210.3	201.9	215.2	204.4

Performance summaries of this thesis work and previous works are provided in Table 4.4. Figure-of-merit (FOM) was calculated from [14] as

$$\mathrm{FOM} = 10\log\left(\frac{\mathrm{DR}}{\mathrm{P_{DC}P_{Sens}}}\right) \tag{4.12}$$

where DR is the data rate, $\mathrm{P_{DC}}$ is average power consumption, $\mathrm{P_{Sens}}$ is the sensitivity level. Power consumption of this work includes biasing power as well. As can be seen from the comparison table, the receiver employing inductors performs better than [26] and [45]. However, [44] performs better than this work as they achieve better power consumption. Biasing consumes more than 30% of the overall power consumption in this work. To lower power consumption, biasing must be integrated. Since it was the first tape-out, bias currents were given from outside to have control over all the circuits individually.

5. INDUCTORLESS SUPER-REGENERATIVE RECEIVER

Inductors are almost always used in RF systems as they allow high-frequency operation while contributing no noise ideally as mentioned in Chapter 4. Despite these advantages, inductors are one of the components whose performance worsens when scaled. On the other hand, integration is inevitable for lower cost and higher functionality. Thus, passive inductors present a bottleneck in RF systems. Therefore, an inductorless super-regenerative receiver is proposed in this chapter.

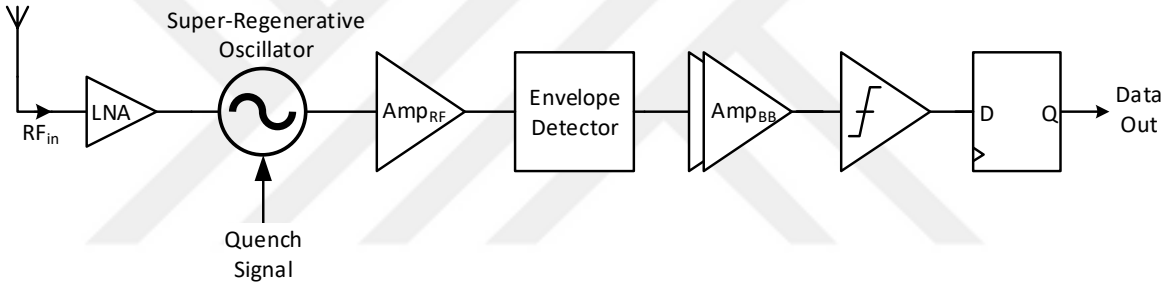


Figure 5.1. Block diagram of the inductorless SRR.

Block diagram of the inductorless SRR is depicted in Figure 5.1 which is the same as the previous receiver. The main difference is in the circuit level where inductorless architectures were employed for the LNA and the SRO. Stages after the SRO are reused here and were explained in detail in Chapter 4.

This chapter is organized as follows. Section 5.1 presents sub-blocks of the inductorless SRR. Sub-blocks are presented initially with the theoretical analysis with the design procedure explained afterwards. Finally, silicon measurement results are presented in Section 5.2 along with the discussion on the results.

5.1. Analysis and Design

5.1.1. Inductorless Low-Noise Amplifier

Common-gate architecture has been of high interest in LNA design for wide-band applications and applications which are not suitable to employ inductors [46–49]. The main drawback of this architecture is the high noise figure. There have been some improvements in the common-gate LNA where single or multiple negative and positive feedback loops were used to lower power consumption while decreasing noise figure. Although multiple feedback techniques are useful to obtain better performance, they increase the complexity and bring additional noise and power consumption since active components are used in feedback loops. On the other hand, capacitive cross-coupled common-gate LNA (CCC-CGLNA) uses capacitors to apply negative feedback and does not suffer from additional power consumption or noise contribution. These characteristics make CCC-CGLNA a very good candidate for the targeted application.

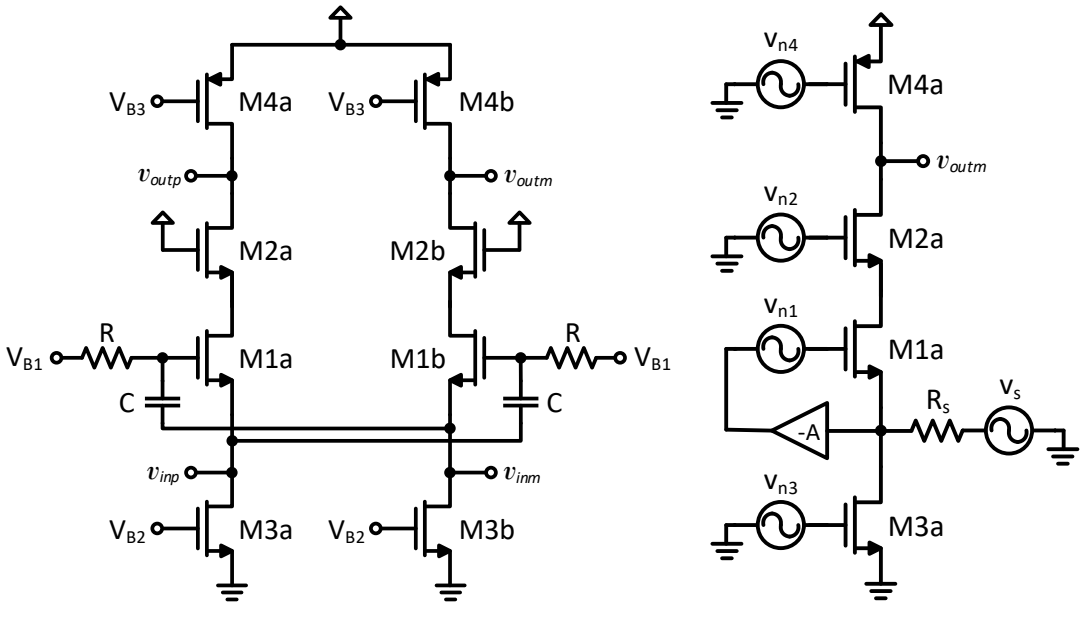


Figure 5.2. Schematic diagram of (a) capacitive cross-coupled common-gate low noise amplifier and (b) equivalent noise half-circuit.

Schematic of the CCC-CGLNA is shown in Figure 5.2a. This architecture is fully differential so that capacitive feedback can be applied without any additional active component. Cascode transistors improve reverse isolation while contributing almost no noise (see Section 3.1). Bias current is determined by transistors $M_{3a,b}$, and $M_{4a,b}$ form active loads.

Figure 5.2b shows the equivalent noise half-circuit. Half circuit analysis can be used as the architecture is fully differential. Feedback gain can be expressed as

$$A = \frac{C}{C + C_{gs}} \tag{5.1}$$

where for $C \gg C_{gs}$, A approaches to 1. v_{ni} represents the gate-referred thermal channel noise of transistor M_i. R_s is the source resistance and v_s is the thermal noise of the source resistance. The boosted transconductance of the LNA is found as

$$G_m = g_{m1}\,(1 + A) \tag{5.2}$$

Input impedance can be found as

$$R_{in} = \frac{1}{g_{m1}\,(1 + A)} \tag{5.3}$$

For impedance matching, input impedance must be equal to the complex conjugate of the source impedance. Thus,

$$R_s = \frac{1}{g_{m1}\,(1 + A)} \tag{5.4}$$

With the above results, the voltage gain of the LNA can be found as

$$A_v = G_m R_{out} \tag{5.5}$$

$$= g_{m1}\,(1 + A)\,R_{out} \tag{5.6}$$

$$= \frac{R_{out}}{R_s} \tag{5.7}$$

where R_{out} is the output resistance of the LNA and A_v is the voltage gain of the LNA and overall gain is

$$G_v = \frac{R_{in}}{R_s + R_{in}} A_v \tag{5.8}$$

for matched input impedance, overall gain simplifies to

$$G_v = \frac{R_{out}}{2R_s} \tag{5.9}$$

From the equivalent circuit shown in Figure 5.2b, total output noise can be found as

$$\overline{v_{no}^2} = \overline{v_{ns}^2} \left(\frac{R_{out}}{2R_s} \right)^2 + \overline{v_{n1}^2} \left(\frac{g_{m1} R_{out}}{2} \right)^2 + \overline{v_{n3}^2} \left(g_{m3} R_{out} \right)^2 + \overline{v_{n4}^2} \left(g_{m4} R_{out} \right)^2 \tag{5.10}$$

From the above result, it is clear that feedback attenuates the noise contribution of the input transistor by the square of the boosting factor. As a result, assuming matched input, noise factor can be found as

$$F = 1 + \frac{4kT\gamma g_{m1} \frac{R_{out}^2}{4} + 4kT\gamma g_{m3} R_{out}^2 + 4kT\gamma g_{m4} R_{out}^2}{4kTR_s \frac{R_{out}^2}{4R_s^2}} \tag{5.11}$$

$$= 1 + \gamma g_{m1} R_s + 4\gamma g_{m3} R_s + 4\gamma g_{m4} R_s \tag{5.12}$$

The layout of the CCC-CGLNA is shown in Figure 5.3. Schematic and post-layout simulation results of the LNA are depicted in Figure 5.4a and Figure 5.4b, respectively. Because of additional parasitic capacitances, the corner frequency of the LNA shifts to the left and gain decreases. This affects noise factor and input matching yet performance is still in acceptable limits. However, common-gate LNA cannot achieve noise figures as low as common-source LNA does. On the other hand, input matching is ultra wide-band and the best noise factor value is maintained over a decade of operating frequency values.

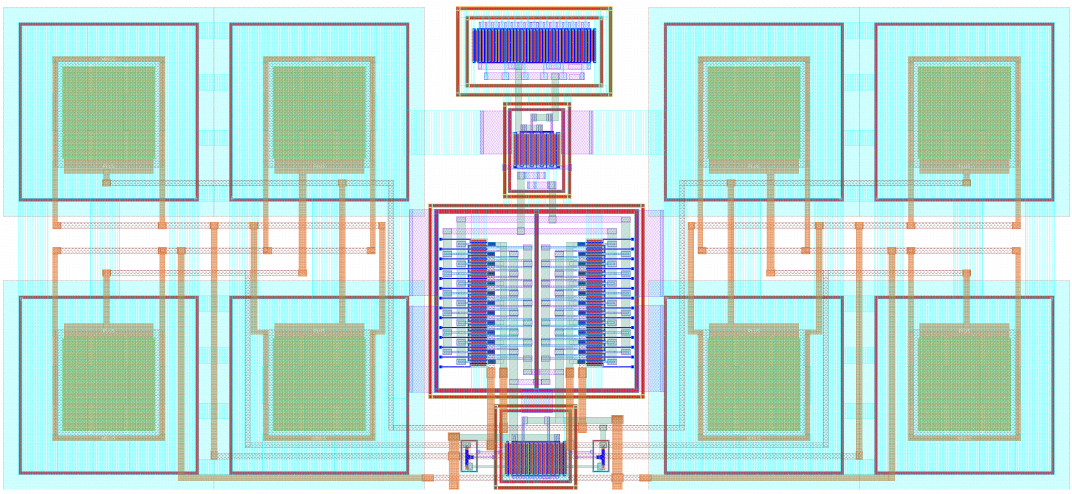
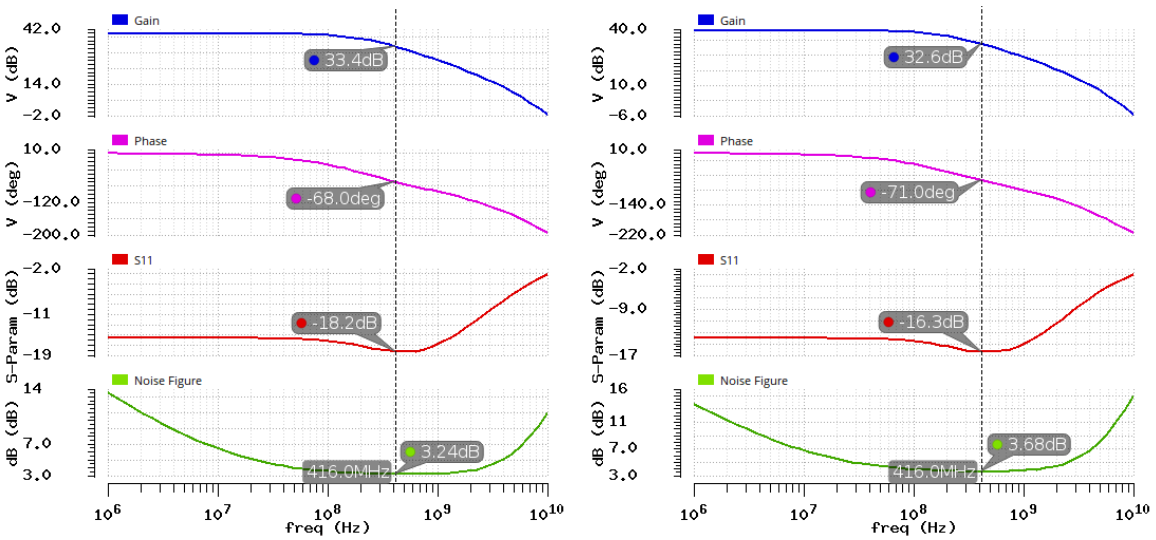


Figure 5.3. The layout of the CCC-CGLNA.

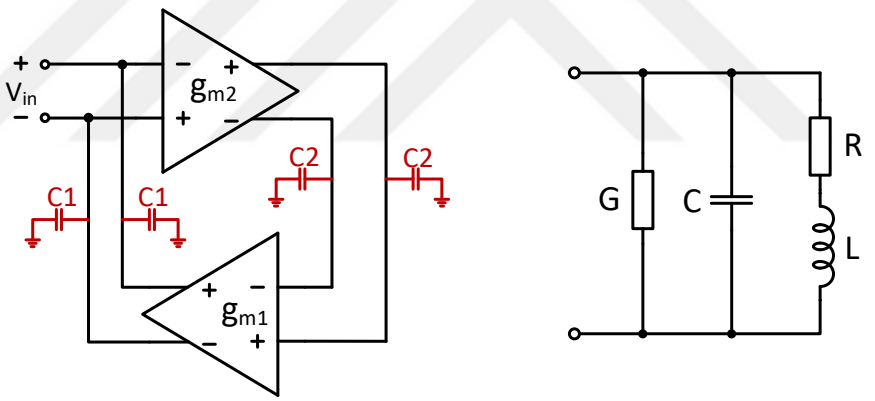


(a) (b)

Figure 5.4. (a) Schematic and (b) post-layout simulation results of the CCC-CGLNA.

5.1.2. Super-Regenerative Oscillator with Active Inductor

MedRadio frequency is too low to employ on-chip inductors easily. There are oscillator architectures in the literature that do not employ inductors (e.g. ring oscillator). However, these architectures are not suitable for quenched operation. Another solution is to use active inductors (AI) which emulate inductor behavior by means of capacitors and active circuits. AI have been used even in discrete designs since available inductor values are limited and the performance of the inductor is a problem itself. Therefore, there has been a lot of different AI examples in the literature [50]. For the targeted application, differential (floating) AI inductor is the best choice. Chosen architecture is proposed by Grozing et. al. in [51], and known as Grozing AI.



(a) (b)

Figure 5.5. (a) Block diagram and (b) equivalent model of the Grozing AI.

Gyrator-C topology is the most common technique to emulate an inductor with active circuitry. Figure 5.5a shows a generic schematic diagram of the Gyrator-C AI. C1 and C2 are parasitic capacitances at corresponding nodes. Input impedance is inductive and determined by C2 and transconductance of circuits. Output resistances of transconductor blocks cause loss and degrade Q-factor of the inductor, whereas C1 determines the self-resonant frequency. Small signal model of the AI is shown in Figure

5.5a. Component parameters of the model are calculated as [51]

$$L = \frac{2C_2}{g_{m1}g_{m2}} \tag{5.13}$$

$$R = \frac{2g_2}{g_{m1}g_{m2}} \tag{5.14}$$

$$G = \frac{g_1}{2} \tag{5.15}$$

$$C = \frac{C_1}{2} \tag{5.16}$$

where g_1 and g_2 are output conductances, g_{m1} and g_{m2} are transconductances and C_1 and C_2 are parasitic capacitances at the output of the transconductor stages 1 and 2, respectively.

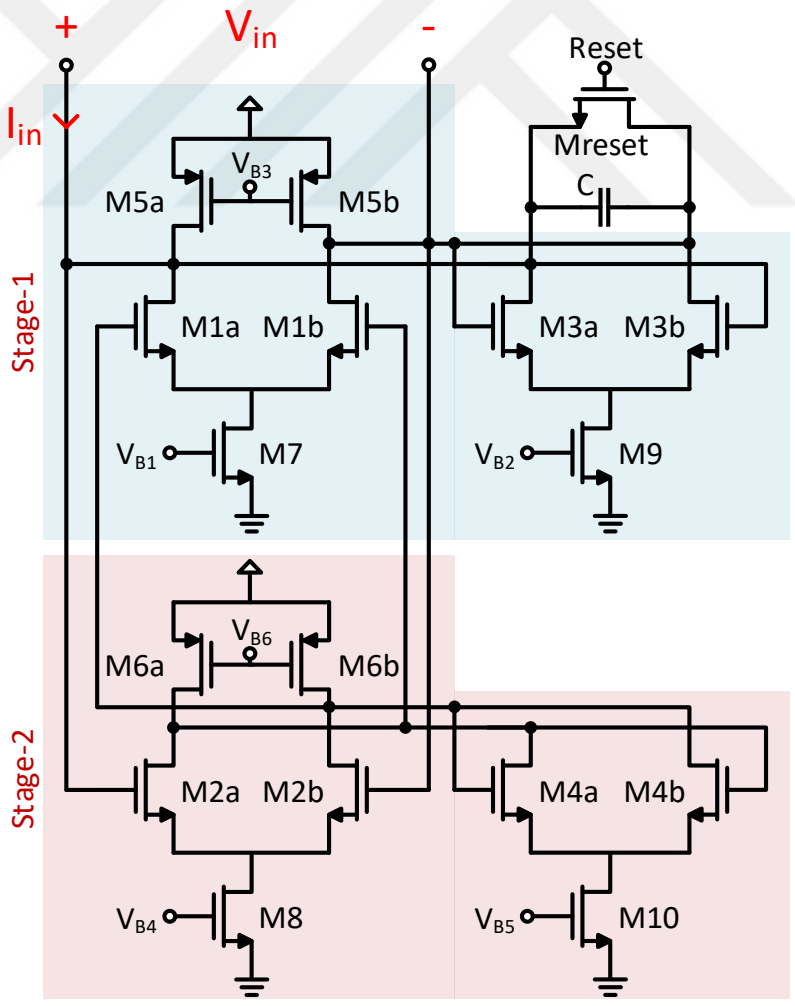


Figure 5.6. Schematic diagram of the inductorless SRO.

Schematic diagram of the Grozing AI and the oscillator is shown in Figure 5.6. C is the capacitor to form the LC tank with the AI and Mreset is the transistor used against hangover phenomenon. Transconductor stages are simple differential pairs. Cross-coupled pairs are used to cancel finite output conductance of each stage. Cross-coupled pair in the stage-1 is not only used for Q-factor improvement but also for the oscillator. In order to inject output of the LNA into the SRO, a differential g_m stage was used to convert LNA output voltage to current.

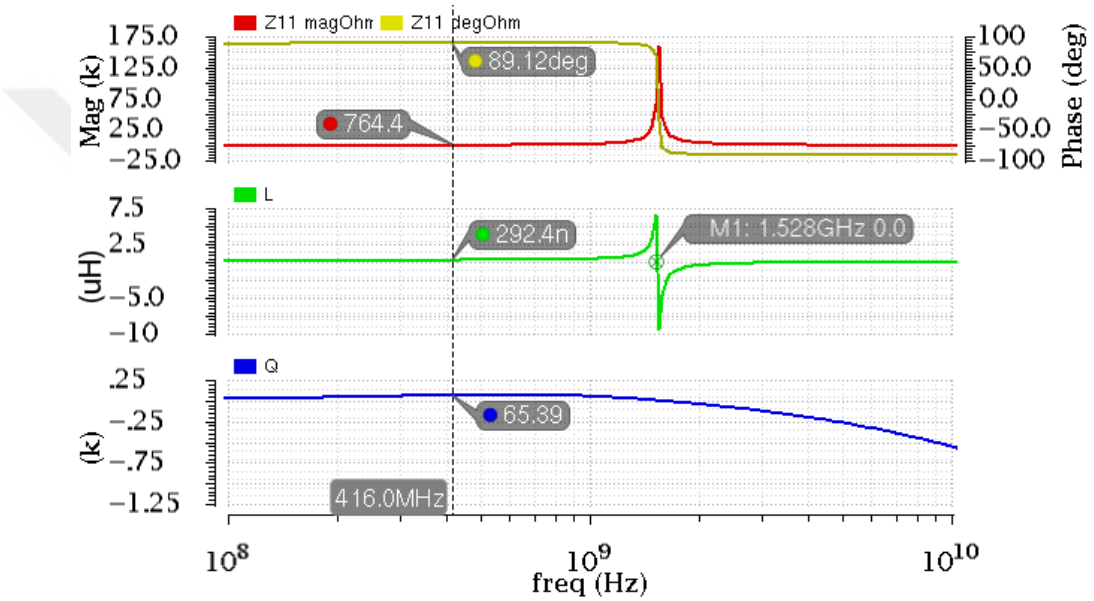


Figure 5.7. S-parameter simulation results of the Grozing AI.

The capacitor in the final LC tank was chosen to be 500 fF and required inductance for the targeted frequency was obtained as 292nH. Obtained inductance and Q-factor are shown in Figure 5.7 along with impedance and phase. Until the self-resonant frequency, impedance shows inductive behavior while the behavior changes to capacitive after the resonance as expected. Q-factors as high as 1000 can be achieved; however, in order to achieve this high Q-factors, negative impedance seen from cross-coupled pairs must be set very close to the loss. This brings the risk of free oscillation with variations occurring in fabrication or during the operation. Therefore, bias currents of cross-coupled pairs were decreased by 15% which covers average variations reported by the fab. Figure 5.8 shows the layout of the SRO employing Grozing AI along with the resonant capacitor.

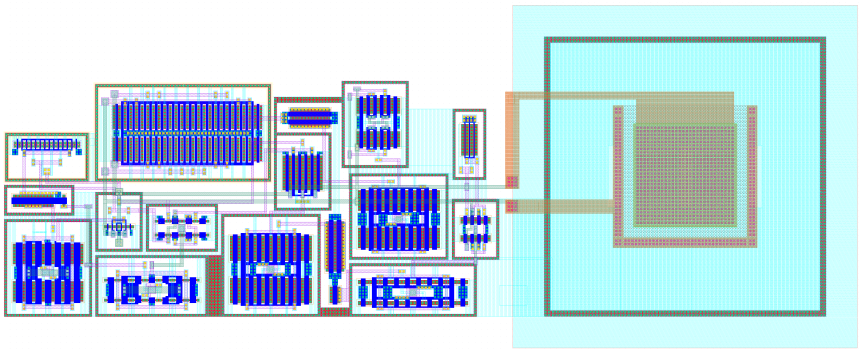
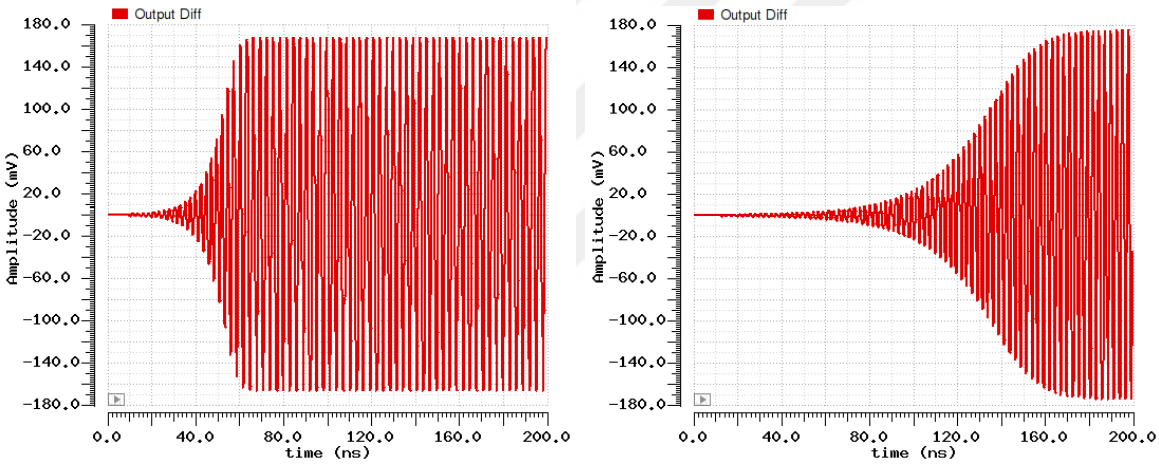


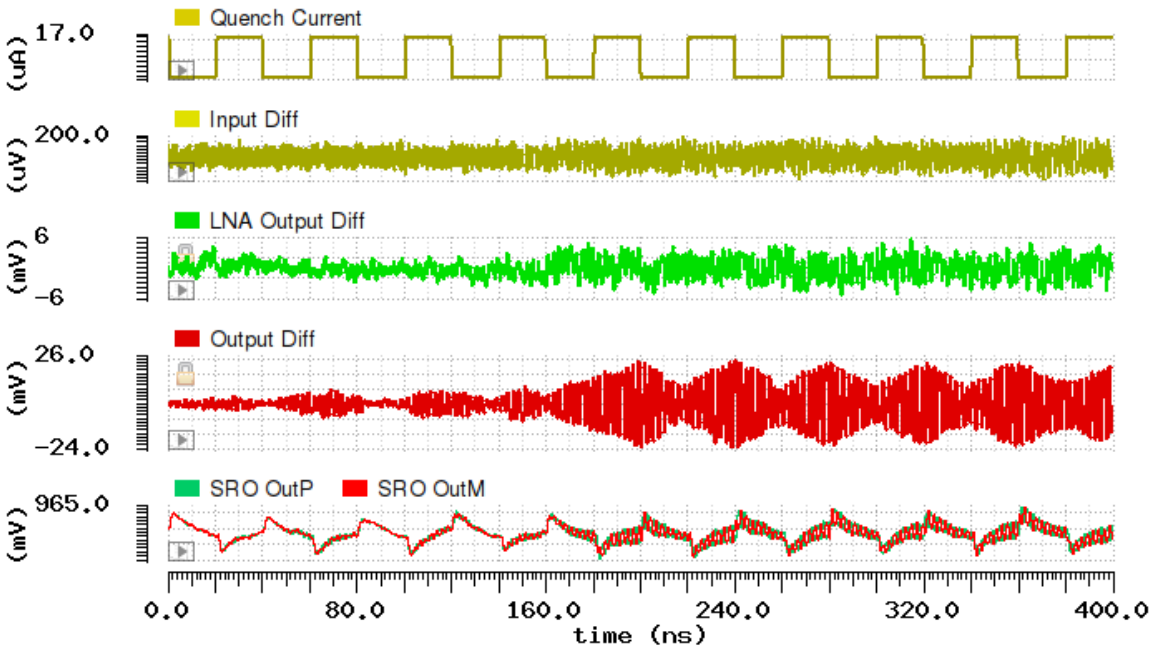
Figure 5.8. The layout of the inductorless SRO.



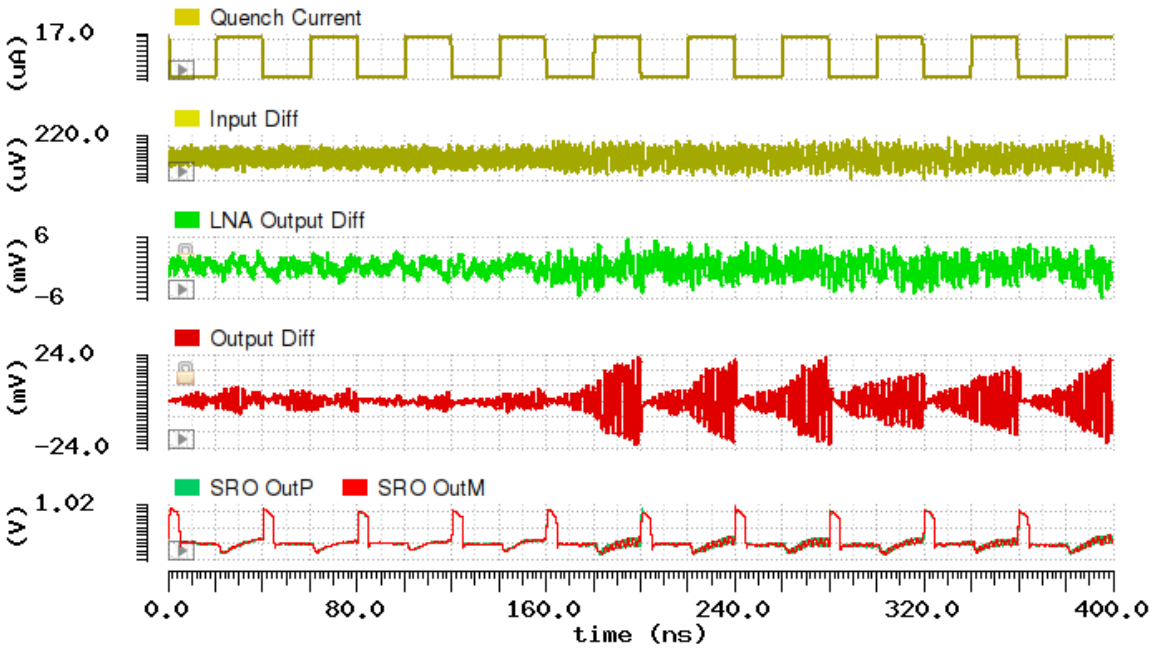
(a) (b)

Figure 5.9. (a) Schematic and (b) post-layout transient simulation results.

Schematic and post-layout transient simulation results are shown in Figure 5.9a and Figure 5.9b, respectively. Oscillation start-up time changes in post-layout since parasitics affect Q-factor of the SRO. It cannot be recognized from the time domain signals, yet high oscillation amplitudes cause non-linearities in the circuits. As transconductances decrease with high signal swing, equivalent inductance increases, and oscillation frequency decreases. This effect is only seen with the high signal swing. This is one of the main reasons why active inductors are not used widely in reference oscillators. However, thanks to quenched operation in the targeted application, oscillation amplitude does not reach to the values where non-linearities are seen. This makes AI a good candidate for the SRO architecture.



(a)



(b)

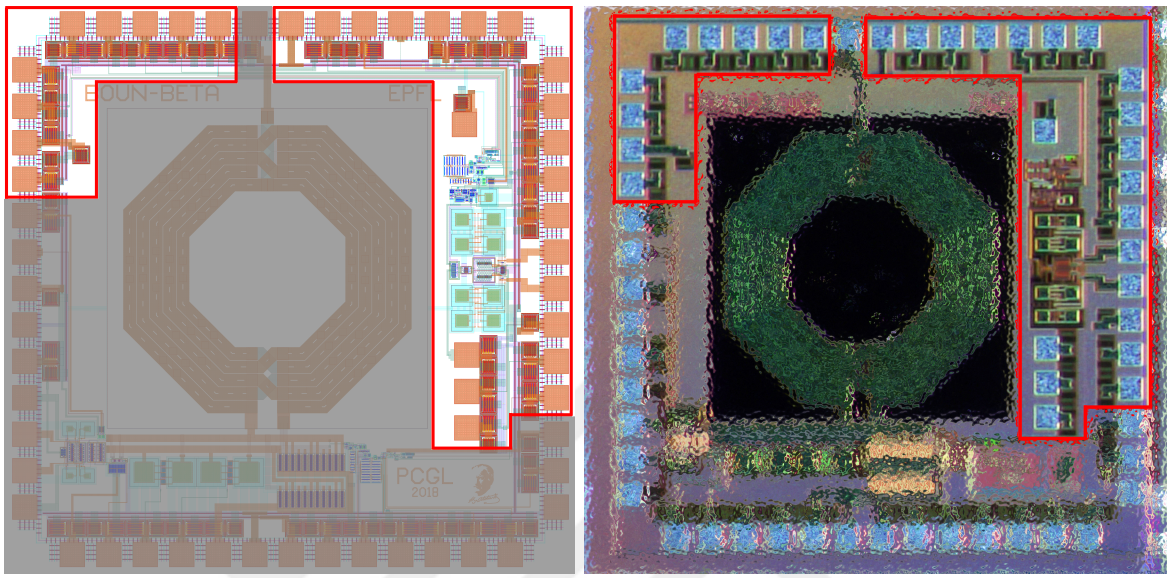
Figure 5.10. Operation of the inductorless SRO with reset (a) disabled and (b) enabled.

Normal operation of the inductorless SRO under square-wave quench is shown in Figure 5.10a. The first point needs to be mentioned is the common-mode fluctuation at the output of the SRO. These fluctuations stem from the quenched current of the cross-coupled pair. This effect is more severe here than the previous receiver, since in this SRO, transistors are used in series with the supply rail, whereas only the inductor was placed in series with the supply rail in the previous receiver. On the other hand, the RF amplifier used after the SRO suppresses these common-mode fluctuations and normal operation is not deteriorated. The second problem is the hangover phenomenon which can be seen from the figure clearly. The higher the Q-factor, the longer the oscillation damping time. As the Q-factor of the AI is very high, the hangover is very severe. Figure 5.10b shows the operation with the same configurations and reset is activated [42]. Results prove the importance of the reset function for the proper operation.

5.2. Measurement Results and Discussion

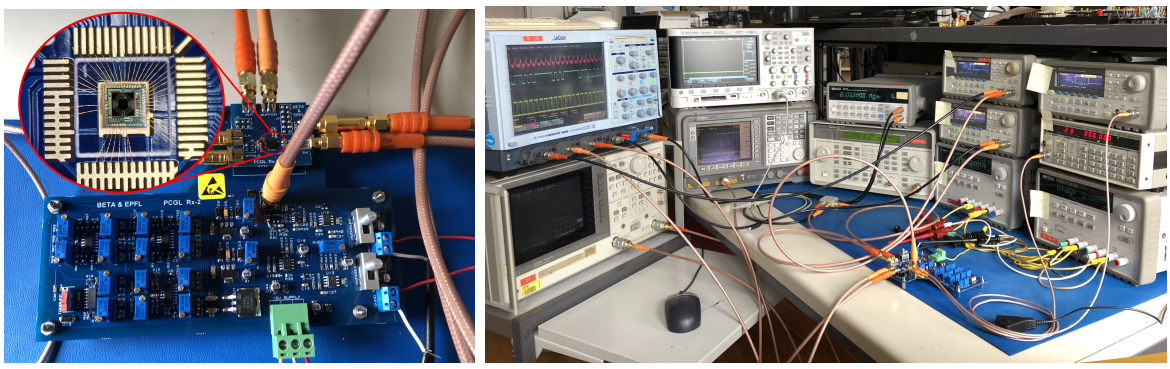
Layout and micro-photograph of the whole receiver including active area and pads are shown in Figure 5.11a and Figure 5.11b, respectively. The core of the receiver occupies only $0.072\,\mathrm{mm}^2$ which shows more than 14x reduction compared with the SRR employing inductors. Additionally, the previous receiver had four off-chip inductors, yet the inductorless SRR has no off-chip component, that makes it favorable for implant devices.

Test boards including chip board and bias generator board are shown in Figure 5.12a along with wire-bond photograph. Bias board includes adjustable DC bias current generators as well as high-frequency voltage-to-current convertor. Voltage-to-current converter was also designed for the inductorless SRR since programmable current waveform generators were not available. Sharp-edge square-wave current generation was again introducing some problems to the performance. However, as the current switched in the inductorless SRR was much lower than the SRR with inductors, quenching was not as problematic as the previous case.



(a) (b)

Figure 5.11. (a) The layout and (b) micro-photograph of the inductorless receiver.



(a) (b)

Figure 5.12. (a) Test board and (b) test setup photographs of the inductorless SRR.

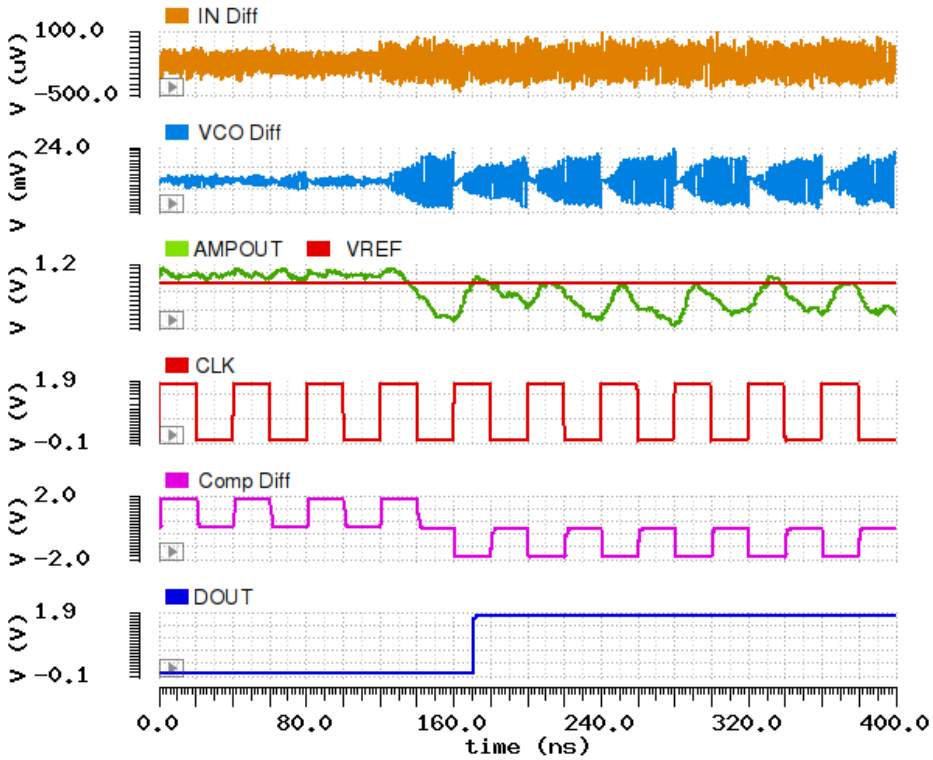
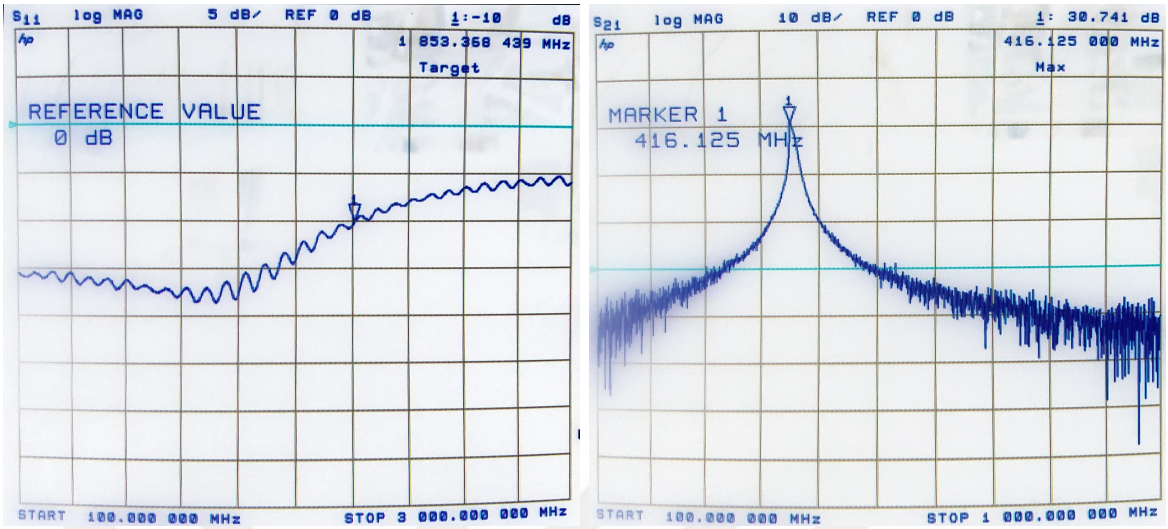


Figure 5.13. Post-layout simulation of the whole receiver on the final layout.

Post-layout simulation results are shown in Figure 5.13. These simulations were performed with the final layout including additional buffers for characterization, pads, ESD devices, antenna-effect protection diodes and all other additional components which were not included in previous simulations. Reset operation was activated in the simulation so that no hangover occurs. System was operated with 25 MHz quench frequency which supports more than 10 Mbps data-rate.

Network analyzer screen photos are shown in Figure 5.14a and Figure 5.14b for S11 and S21 measurements, respectively. Since input matching was obtained by means of the transconductance of the input pair, input matching is wide-band and well below the commonly accepted matching limit of -10 dB. Ringing in the S11 measurement stems from standing waves that were caused by the calibration issues of the network analyzer. However, measurements are still valid and show the same behavior as in the simulations.



(a) (b)

Figure 5.14. Network analyzer screen photographs of (a) S11 and (b) S21 measurements of the CCC CGLNA.

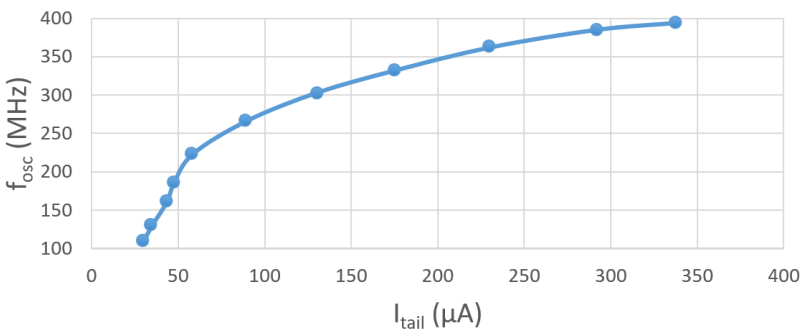


Figure 5.15. Frequency tuning measurements of the inductorless SRO.

Frequency tuning measurement results are shown in Figure 5.15. There is no variable capacitor in the inductorless SRO. Instead, the transconductance of stage-1 was changed and inductance value was varied as stated in Equation 5.13 to modify the oscillation frequency. There was a common-mode voltage problem in the inductorless receiver chain as explained later in this section. Because of this problem, oscillation frequency could not be increased beyond 400 MHz. However, with a better biasing combination in the whole receiver, this problem can be solved. Oscilloscope screenshot of the time domain oscillator measurement is shown in Figure 5.16.

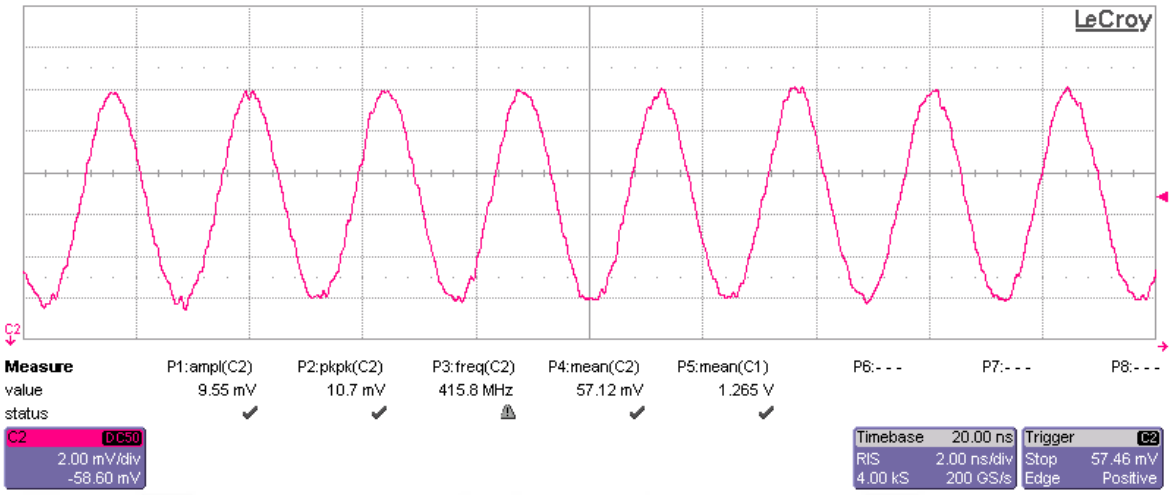


Figure 5.16. Oscilloscope screenshot of time-domain measurements of the inductorless SRO.

In the inductorless SRR, oscillator output common-mode voltage is around 0.9 V, whereas it is VDD in the SRR with inductors since the passive inductor has no voltage drop on it in DC. There was no common-mode voltage problem in the rest of the chain in the SRR with inductors. On the other hand, in the inductorless receiver, common-mode voltages of each block were close to limits. Hence, the operation of the chain was not as good as in simulations. Because of the tight schedule, there was no time to optimize bias points of individual blocks. With further tests, much better performance can be achieved. Because of these problems, the best performance of the SRO was achieved at 400 MHz and reception tests were performed at this frequency.

Oscilloscope screenshot showing the reception test with -60 dBm 4 Mbps input and 2 MHz quench and clock signal is depicted in Figure 5.17. C1 is the quench trigger, C2 is the SRO buffer output, C3 is the data output, and C4 shows the reset trigger. The aforementioned problem with the DFF occurs here as well since it is the same design as the previous receiver. At the negative level of each clock cycle, DFF output resets to logic high. Further tests are also needed to point out the reason behind this problem.

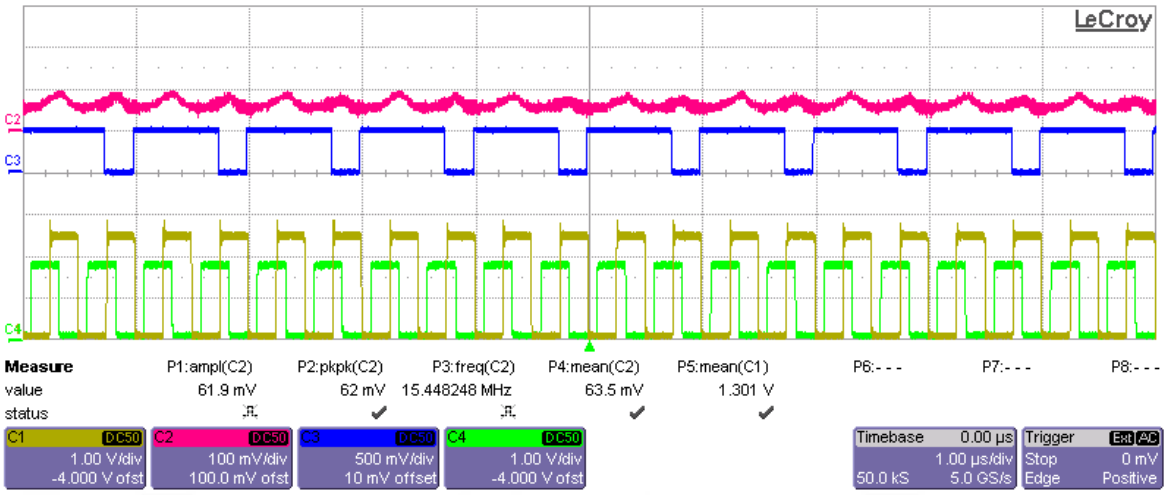


Figure 5.17. Operation of the system with -60 dBm 2 Mbps input under 266 μA square-wave quench signal.

Performance summaries of the inductorless receiver and previous works are provided in Table 5.1. Figure-of-merit (FOM) was calculated from [14] as shown in Equation 4.12. Power consumption of this work includes biasing power as well. Biasing consumes more than 30% of the overall power consumption in the receiver. To lower power consumption, biasing must be integrated. Since it was the first tape-out, bias currents were given from outside to have control over all the circuits individually, which causes high power consumption in biasing. Previous works perform better than the inductorless receiver because of the aforementioned issues. Further tests are needed to obtained better sensitivity and data-rate so that the overall performance would be on the levels achieved in the simulations. Despite all, the idea of the inductorless SRR employing AI is present here from theory to the application for the first time to the best of author's knowledge. The idea was proven to be very promising for the applications where integration is of high importance and area is limited. Medical implants require a small area, full integration, and only need close-range communication. These make the inductorless SRR a good candidate for implant devices.

Table 5.1. Comparison with the previous work.

	Proposed Receiver	**[26]**	**[44]**	**[45]**
Publication Year	2019	2010	2011	2013
Process	180 nm CMOS	180 nm CMOS	130 nm CMOS	90 nm CMOS
Active Area	0.072 mm^2	2.15 mm^2	0.69 mm^2	0.49 mm^2
Modulation	OOK	OOK	OOK	OOK
Freq. Band	392-408 MHz	402-405 MHz	495-505 MHz	392.16-416.94 MHz
Quench Shape	Square	2-Step Square	Square	Square
Data Rate (max)	4 Mbps	1 Mbps	10 Mbps	1 Mbps
Sensitivity	-70 dBm @1 Mbps -60 dBm @4 Mbps	-85 dBm @1 Mbps	-85dBm @10 Mbps	-80dBm @500 Kbps -65dBm @1 Mbps
Supply Voltage	1.8 V	1.3 V	1.2 V	0.8 V
Power	12.9 mW @10 Mbps	2.2 mW	0.96 mW	180 μW
Energy per Bit	3.22 nJ/b @4 Mbps	NA	NA	0.18 nJ/b @1 Mbps 0.256 nJ/b @500Kbps
FOM	184.9	201.9	215.2	204.4

6. CONCLUSION AND FUTURE WORK

Diagnosis and treatment ways are evolving with the advances in technology. Yet, the mystery about the brain, the most critical organ, remains unresolved. Thus, brain-related diseases attract attention from the research community. To solve the mystery, the first step is to observe the operations of the brain. There are solutions available in the literature to record neural activity in the brain. However, these solutions are lacking the comfort of the patient and ease of the operation.

In this work, the super-regenerative reception theory was explained in detail, a generic system-level model was proposed, and an on-chip inductor, a super-regenerative receiver employing inductors and an inductorless super-regenerative receiver were analyzed, designed, fabricated and characterized. The SRR architecture was proposed as a solution for the need of a low-power wireless data-link between the main station and the brain implant for the application to monitor and intervene epilepsy seizures. UMC 180 nm process node was used for the design and the fabrication.

The first SRR proposed consists of sub-blocks some of which contain passive inductors. Biggest drawbacks with these architectures are large area requirements and incompetent performance of passive inductors. Hence, only one inductor could be integrated. Despite the large area occupied by the receiver, targeted performance was achieved in tests and results were promising for the future work.

The second SRR proposed contains only inductorless architectures and employs an active inductor circuit to emulate the inductance needed for the frequency-selective circuitry. To the best of the author's knowledge, this is the first inductorless SRR proposed in the literature. The theory was proved by silicon measurements and performance comparison was provided in the corresponding section. There had been some biasing and common-mode voltage problems during the characterization so that the targeted sensitivity and data-rate could not be achieved in tests. However, the author believes that with further tests and a better combination of bias points in each stage,

the performance achieved in post-layout simulations could also be achieved in tests.

Further tests could not be performed because of the time schedule, yet in the future work, the first step to start with should be the detailed characterization of fabricated ICs. After the full characterization, problems degrading the performance should be listed, solved and a second tape-out should be performed. In the second version, common-mode voltage of each stage should be determined individually such that the highest voltage swing is ensured. This would increase the overall performance of the receiver while adding the least amount of complexity to designs performed in this thesis work. The next step should be to design an on-chip bias generation and distribution system. Because the external bias generation used in this work was consuming more than 30 % of the overall power, to integrate and modify this part would provide a great improvement in the energy efficiency.

The stage consumes the highest power was the LNA in both receivers as power consumption of the oscillator was decreased by the quench operation. Differential input impedance of each LNA was chosen to be 50 Ohm since a balun was planned to be used along with a commercial 50 Ohm single-ended antenna. However, there are baluns available in the market that transform 50 Ohm single-ended input impedance to higher differential impedances. The first option should be to use such a balun with a higher differential impedance for the LNA, which will directly decrease power consumption of the LNA, hence, of the whole receiver. The second and more preferable option should be to design a custom antenna with a custom impedance for the implant device. Since commercial antennas are not sized for the targeted application, a custom antenna design is inevitable for the final version of the system and using higher impedance would be wise to obtain better energy efficiency.

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