CURRENT MODE CONTINUOUS TIME SIGMA DELTA CONVERTER DESIGN

by

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ABSTRACT

CURRENT MODE CONTINUOUS TIME SIGMA DELTA CONVERTER DESIGN

Most sigma delta modulators are realized in the discrete-time domain using circuit techniques such as switched capacitor. In typical discrete time implementations, there are some speed constraints. For example, maximum clock rate is limited to op amp bandwidths. Therefore, high resolution can be achieved only for low bandwidth signals. However, continuous-time circuits do not suffer from such speed restrictions, hence, clock rates can be increased by building the loop filter out of continuous-time circuits and high resolution converters with wider bandwidths could be implemented.

Secondly, in most sigma delta modulators where input signal is current, quantizers are generally implemented in voltage-mode and a digital/analog converter is used in the feedback loop to convert voltage signals to current signals. However, if all blocks are designed in current-mode, an extra digital/analog converter requirement can be relaxed. Furthermore, current mode circuits have attractive features such as high speed and low voltage operation.

This thesis is mainly about designing current mode circuits for a first order continuous time sigma delta modulator. Main blocks of a modulator such as integrator, quantizer and comparator have been designed in current mode. Also, current mode design of digital circuits such as full adder and delay element which is widely used in digital filters has been made.

ÖZET

AKIM MODLU SÜREKLİ İŞARET SİGMA DELTA DÖNÜŞTÜRÜCÜ TASARIMI

Sigma delta modülatörler genellikle anahtarlanmış kapasitör gibi devre teknikleri kullanılarak tasarlanan ayrık zamanlı filtrelerle gerçeklenir. Tipik ayrık zamanlı yapıların belirli hız sorunları vardır. Kullanılan op ampların band genişlikleri sınırlı olduğundan, saat frekansı çok yüksek hızlara çıkamaz. Bu durumda, yüksek çözünürlüklü dönüştürücüler sadece dar bant genişlikleri için gerçeklenebilir. Sürekli işaret devre tekniği genelde bu tür hız problemleri göstermediğinden, modulatör filteresini gerçeklemek için kullanılabilir. Bu şekilde, daha yüksek saat hızlarına ulaşılabilir ve daha yüksek band genişliğine sahip işaretlerin yüksek çözünürlüklü çevrimi sağlanabilir.

Diğer taraftan, sigma delta modülatörlerde, giriş işareti akım iken, kuantalayıcılar gerilim modlu gerçeklenir ve geri besleme hattında bu gerilim bir sayısal/analog dönüştürücü yardımıyla tekrar akıma çevrilir. Fakat, bütün bloklar akım modlu tasarlanırsa, bu dönüştürücü gereksinimi ortadan kaldırılabilir. Ayrıca, akım modlu devreler yüksek hız ve düşük gerilimlerle çalışma gibi üstün özelliklere sahiptir.

Bu tez temel olarak birinci dereceden sürekli işaret bir sigma delta modülatörün akım modlu devrelerinin tasarımıyla ilgilidir. İntegratör, kuantalayıcı, karşılaştırıcı gibi modulatörü oluşturan bloklar akım modlu olarak tasarlanmıştır. Ayrıca, tam toplayıcı ve gecikme elemanı gibi sayısal filtrelerin temelini oluşturan elemanların da akım modlu tasarımları yapılmıştır.

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LIST OF SYMBOLS/ABBREVATIONS

B	Signal bandwidth
C_{gs}	Gate capacitance
e	Error signal
f_B	Baseband frequency
f_n	Nyquist frequency
f_s	Sampling frequency
f_T	Maximum transistor speed
g_m	Transistor transconductance
g_{ds}	Transistor output conductance
H	Filter transfer function
L	Transistor length
N	Number of bits
NTF	Noise transfer function
P	Power
Q	Number of quantization levels
STF	Signal transfer function
W	Transistor width
Δ	Quantization step size
σ	Variance

A/D	Analog to Digital
ADC	Analog to Digital Converter
BP	Bandpass
CIC	Cascaded Integrator-Comb
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
D/A	Digital to Analog
DAC	Digital to Analog Converter

DT	Discrete Time
FIR	Finite Impulse Response
LP	Lowpass
LSB	Least Significant Bit
OSR	Oversampling Ratio
SC	Sampled Capacitor
SNR	Signal to Noise Ratio
VLSI	Very Large Scale Integration

1. INTRODUCTION

"Real world signals are analog, however, it is often needed to convert them into the digital domain using an analog to digital converter." [1] When compared to analog signals, digital signals can be processed more efficiently. Generally, these converters are used in applications such as consumer and professional audio, industrial weight scales, and precision measurement devices [2]. "The key feature of these converters is that they are the only low cost conversion method which provides both high dynamic range and flexibility in converting low bandwidth input signals."[2]

In most conventional A/D converters, such as the successive approximation, subranging, and flash converters, signals are sampled at Nyquist rate. Therefore, these converters are called Nyquist rate converters. There are tradeoffs among signal bandwidth, output resolution, and the complexity of the analog and digital hardware for ADCs [1]. Bandwidth and resolution tradeoff of some A/D techniques, as well as sigma-delta conversion, is shown in Figure 1.1. Sigma-delta A/D converters have the highest resolution for low signal bandwidths [1].

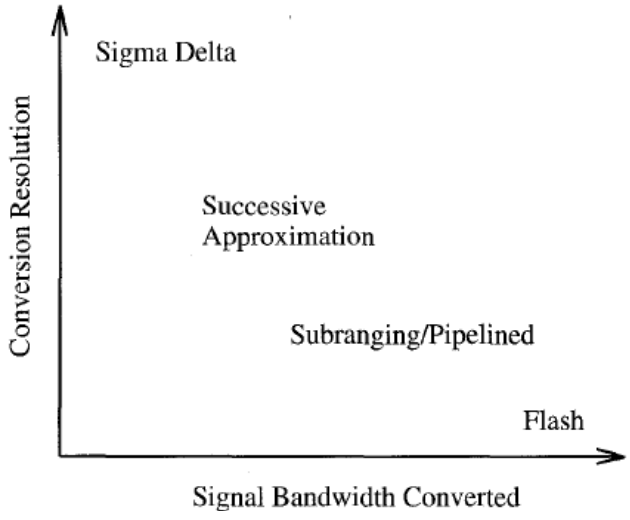

Figure 1.1 Bandwidth resolution tradeoffs

"Sigma-delta modulators can be realized in a DT (discrete-time) or in a CT (continuous-time) manner. The recent high demand for wideband, high resolution A/D converters for telecommunication applications requires very high sampling frequencies. Also the continuously decreasing supply voltage of recent CMOS technologies is causing important limitations to the performances of DT circuits. Some proposed techniques are rather complex and still limit the sampling frequency. CT circuits do not suffer from these limitations and are therefore capable of achieving higher performances in recent low-voltage CMOS processes. DT Sigma-delta converters are inherently simpler to model, simulate and design. Thus, people hesitated in using CT converters because lack of design automation methods for CT converters until recently, but now there is growing interest in the development of CT converters due to mentioned advantages like having low power consumption and high bandwidth." [21]

Most sigma delta modulators can be designed in voltage mode circuits. However, CMOS current mode circuits offer many attractive advantages over their voltage-mode counterparts, such as low voltage and high-speed operation. Thus, current mode design can be used in order to get high bandwidth conversion.

2. SIGMA-DELTA MODULATION THEORY

2.1. Sigma-Delta ADC

We can fall analog-to-digital converters into two categories in terms of sampling rate [3]. In the first type of converters, system is sampled at Nyquist frequency f_n which is defined by $f_s = f_n = 2B$, where f_s is the sampling frequency and B is signal bandwidth. The other type of ADCs samples the analog input at much higher frequencies than the nyquist frequency and are called oversampling ADCs [4]. Sigma-delta ADCs is an example of oversampling converter. In sigma-delta ADC, oversampling frequency can be expressed as $f_s = \text{OSR}.\ f_n$ where OSR is the oversampling ratio.

The block diagram of a sigma-delta ADC is shown in Figure 2.1. In the modulator, the analog input signal is sampled at much higher frequencies which is determined by the oversampling ratio and analog input signal is converted into a pulse density modulated digital signal containing both the original input signal and the unwanted out-of-band noise [4]. The out-of-band noise of modulator output is removed by a decimation filter. In Figure 2.1, the modulator consist of an one-bit quantizer and produces an one-bit output. The output of the decimator is N-bit digital data, where N is the output resolution of the ADC. The order of the decimator depends on the order of the modulator. Generally, the order of the decimator is one more than the order of the modulator [12].

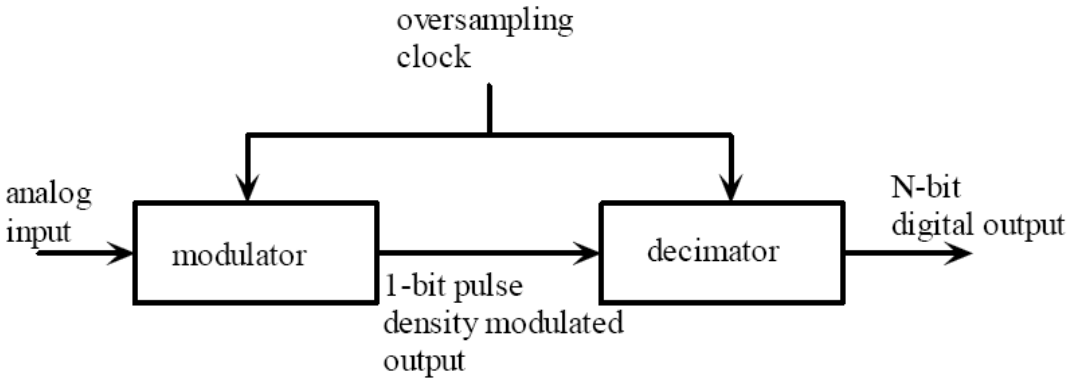

Figure 2.1 Block diagram of a sigma-delta analog to digital converter.

2.2. Modulator

The modulator is the analog part of a sigma-delta ADC. The final output resolution is set by oversampling ratio and the order of the modulator. Since the modulator is oversampled, the need for antialiasing filter which is usually used for nyquist rate converters is eliminated [4]. Due to oversampling of the analog signal, there is tradeoff between the accuracy of the analog circuitry and the speed [5]. Quantization noise is pushed to higher frequencies by the modulator and a digital low pass filter at the decimation stage removes this noise [12]. The modulator produces a 1-bit oversampled digital data, which is the input of the decimator. The basic block diagram of a first-order modulator is shown in Figure 2.2.

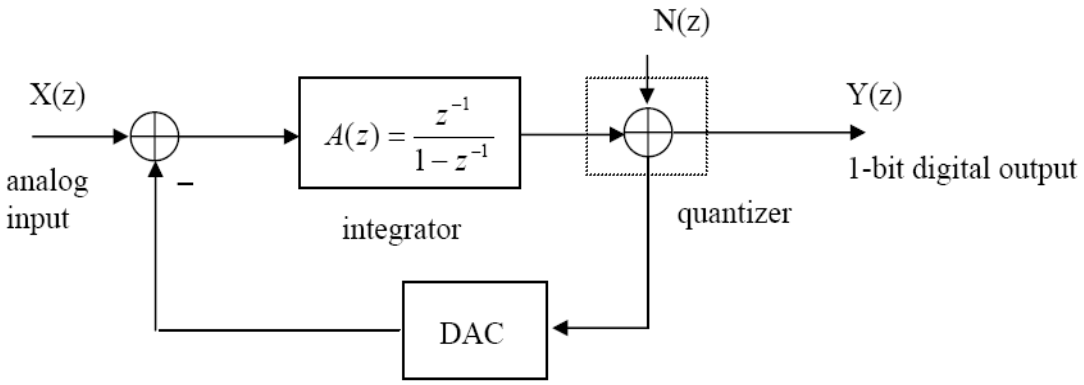

Figure 2.2 Block diagram of a first-order modulator [5].

Figure 2.2 shows that the input signal X(z) comes into the modulator via a summing junction. It then passes through the integrator. The output of the integrator feeds the quantizer. The quantizer output Y(z) is fed back to the input summing junction through a digital-to-analog converter (DAC), and it also passes through the digital filter which produces final output bits. Through feedback loop, the average of the DAC output signal is forced to be equal to the input signal X(z) [2]. It will be useful to review quantization noise theory and signal sampling theory before explaining the sigma delta converter in detail.

2.2.1. Sampling

"In the sampling process, a continuous time signal is sampled at uniformly spaced time intervals, T_s. The samples, $x[n]$, of the continuous time signal, $x(t)$ can be represented as $x[n] = x(nT_s)$. As the result of the sampling process, periodically repeated copies of the signal spectrum is produced at multiples of the sampling frequency $f_s = 1/T_s$. This relationship is written in equation 2.1, where $X_s(f)$ represents the spectrum of the sampled signal, and $X(f)$ is the spectrum of the original analog signal." [1]

$$X_s(f) = 1/T_s \sum_{k=-\infty}^{\infty} X(f - kf_s) \tag{2.1}$$

The sampling process is shown graphically in Figure 2.3 where $f_s = 2B$ and B is the bandwidth of the signal [1]. Generally, the signal can be reconstructed if there is no overlap between the repeated copies of the signal spectrum. Thus, a signal with bandwidth B must be sampled at a rate, $f_s \geq 2B$.

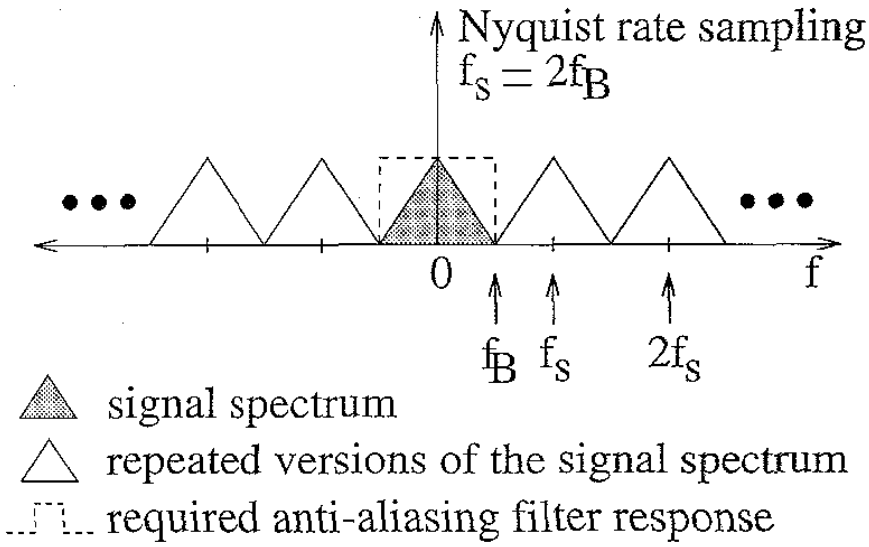

Figure 2.3 Nyquist rate sampling showing the original band limited signal spectrum, periodically repeated versions of the signal spectrum due to sampling, and the anti-aliasing filter response needed to band limit the signal.

"Interference between the repeated versions of the signal spectrum is known as aliasing and it prevents reconstruction of the signal." [1] Generally, an anti-aliasing filter is used before sampling. The anti-aliasing filter is a continuous time analog filter. If sampling frequency is chosen as two times of signal bandwidth, to prevent interference, anti-aliasing filter must have very shary cutoff at $f = f_s/2$ as shown in Figure 2.3. "Sampling is an invertible operation, since no signal information is lost and the original continuous time signal can be perfectly reconstructed." [1] Note that although Figure 2.3 shows the sampling process for the case where the signal spectrum has a bandwidth centered at DC frequency, equation 2.1 still holds if the signal spectrum is centered at some higher frequency f_c [1].

2.2.2. Quantization

"Once sampled, the signal samples must also be quantized in amplitude to a finite set of output values." [1] Typical transfer characteristics for some quantizers where x and y are input and output signals, respectively, are shown in Figure 2.4. "Quantization is a non-invertible process, since an infinite number of input amplitude values are mapped to a finite number of output amplitude values." [1] The quantized output signal is usually represented by a finite number of bits. For example, the output levels V and -V for the 1 bit A/D converter can be coded by "1" and "0."

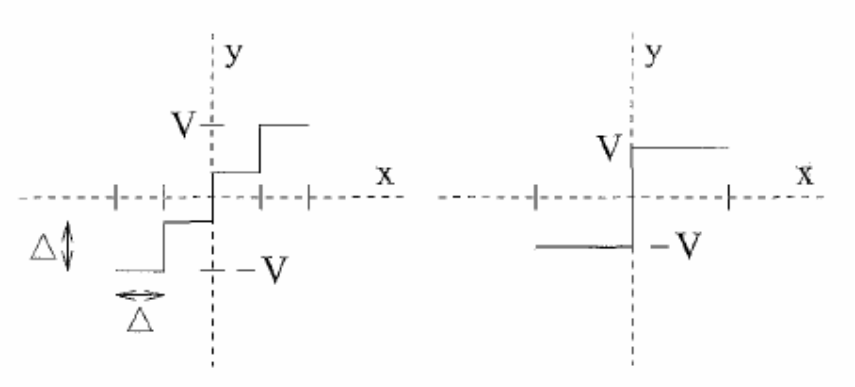

Figure 2.4 Transfer characteristics of typical quantizers

"An ADC or quantizer with Q output levels is said to have N bits of resolution where $N = \log_2 Q$." [1] As should be clear from Figure 2.4, input values should be separated by at least $\Delta = 2V/(Q-1)$ to have different output levels. For a Q level quantizer, N digital bits are needed to encode each output level. The difference between two adjacent output levels is one least significant bit (LSB).

2.2.3. Quantization Noise

"Quantization noise (or quantization error) is one limiting factor for the dynamic range of an ADC. This error is actually the "round-off" error that occurs when an analog signal is quantized. As an example, Figure 2.5 shows the output logic levels and corresponding input voltages for a 2-bit quantizer with a full scale of 3V. The input values of 0V, 1V, 2V, and 3V correspond to digital output levels of 00, 01, 10, and 11,

respectively. When an input of 1.75V is applied, the resulting output code would be 10 which corresponds to a 2V input. The 0.25V difference between output and input values is called the quantization error." [2]

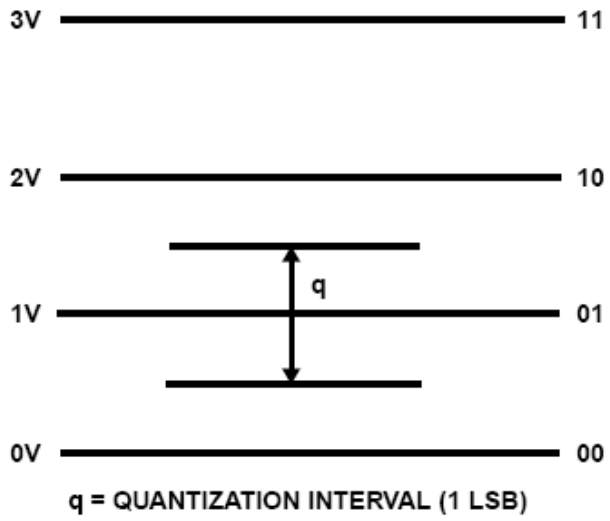

Figure 2.5 Code example of a 2-bit A/D converter

The quantizer embedded in any ADC is a non-linear system, which makes its analysis difficult. To make the analysis easier, we can linearize the quantizer and model it by a noise source, $e[n]$, added to the signal $x[n]$, to produce the quantized output signal $y[n]$ [1].

$$y[n] = x[n] + e[n] \tag{2.2}$$

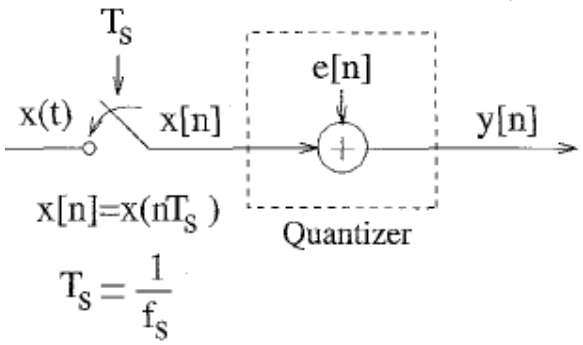

Figure 2.6 Block diagram and model of a conventional A/D converter

A block diagram of an A/D system showing the sampling process and the quantizer model is shown in Figure 2.6. In the linear model, the quantizer is replaced by an independent random noise source e[n]. Following assumptions about noise are generally made [6]:

- The error sequence, $e[n]$, is a sample sequence of a stationary random process
- $e[n]$ is uncorrelated with the sequence $x[n]$
- The probability density function of the error process is uniform over the range of quantization error, i.e., over $\pm \Delta/2$
- The random variables of the error process are uncorrelated, i.e., the error is a white noise process.

"Under certain conditions, such as when the quantizer is not overloaded, N is large, and the successive signal values are not excessively correlated, these assumptions are reasonable." [1] Consider an N bit ADC with $Q = 2^N$ quantization levels and 2V full-scale voltage. For a zero mean $e[n]$, its variance σ_e^2 or power is

$$\sigma_e^2 = \frac{\Delta^2}{12} = \left(\frac{2V}{2^N - 1}\right)^2 /12 \cong \left(\frac{2V}{2^N}\right)^2 /12 \tag{2.3}$$

We can calculate the Signal-to-Noise Ratio (SNR) which is a very important measure for the accuracy of the A/D converters. Assume that input is sinusoidal and the maximum input signal and power of signal are:

$$x_{max} = \mathrm{V} \text{ and } \sigma_x^2 = \frac{\mathrm{V}^2}{2}$$

then, SNR for Nyquist rate converter can be calculated as:

$$SNR = 10\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right) = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) \tag{2.4}$$

$$SNR = 6.02.N + 1.76(dB) \tag{2.5}$$

2.2.4. Oversampling and Noise Reduction

According to Nyquist Theorem, minimum sampling frequency is the twice the highest frequency component of the signal. On the other hand, "Oversampling is the process of sampling a signal with a sampling frequency significantly higher than the bandwidth or highest frequency of the signal being sampled."[7]

Oversampling ratio is defined as follows:

$$OSR \equiv \frac{f_s}{f_n} = \frac{f_s}{2B} \tag{2.6}$$

Oversampling improves the resolution obtained from Nyquist rate conversion. This improvement is achieved by oversampling the signal, that is, signal is sampled at a rate much higher than the Nyquist rate [1]. Then, every sample is digitized by an N bit quantizer. Equation 2.3 defines noise power σ_e^2 for Nyquist rate converter. The total noise power for oversampled converter is the same as Nyquist rate sampling case, however, because of the higher sampling rate, noise is distributed over wider area. Consequently, the amount of noise in signal spectrum is greatly reduced [1].

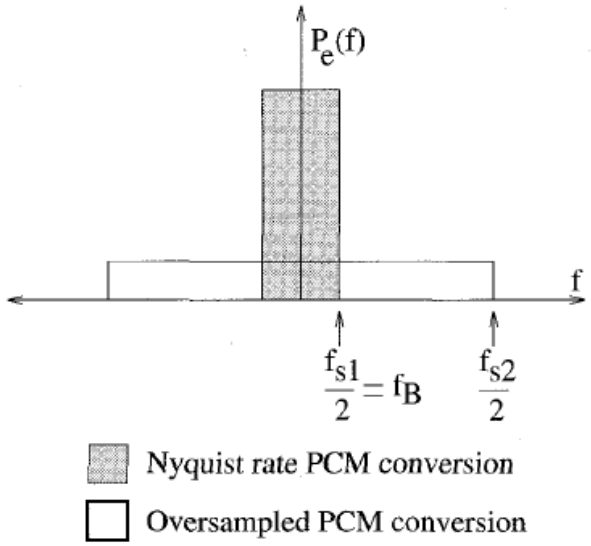

Figure 2.7 Quantization noise power spectral density for nyquist rate and oversampled conversion.

Figure 2.7 shows the power spectral density, $P_e(f)$, of the quantization noise for Nyquist rate sampling with rate f_{s1} and oversampling rate f_{s2}. "For Nyquist rate sampling where the signal band, $B = f_{s1}/2$, all the quantization noise power remains in the signal bandwidth. In the oversampled case, the same noise power distributes over a bandwidth equal to $f_{s2}/2$, which is much higher than the signal bandwidth, B. Therefore, only a relatively small part of the total noise power falls in the signal band, and the out-of-band noise power can be greatly attenuated with a digital low-pass filter." [1]

By taking the Z transform of equation 2.2, Z domain relationship between the input and output of an oversampled converter is obtained:

$$Y(Z) = X(Z) + E(Z) \tag{2.7}$$

Here, Y, X and E are the Z transforms of the output, input signal and the quantization error process, respectively. Based on the linear system model for the quantizer, equation 2.7 defines that, the output is the summation of input and the quantization error. X and E have a unity transfer function in this equation.

Equation 2.7 can be written again where X and E have transfer functions different from unity.

$$Y(Z) = X(Z).H_x(Z) + E(Z).H_e(Z) \tag{2.8}$$

Here, input signal is modulated by a signal transfer function, $H_x(z)$, and the quantization noise is modulated by a noise transfer function, $H_e(z)$, and summation of these two gives the output. It is necessary to find the signal and noise power at the output, to evaluate the performance of the converter [1]. We should find the power spectral densities, $P_{xy}(f)$ and $P_{ey}(f)$, of the signal and noise at the output in terms of the power spectral densities, $P_x(f)$ and $P_e(f)$ of the signal and noise at the input. "We can make use of the fact that if a stationary random process with power spectral density $P(f)$ is the input to a linear filter with transfer function $H(f)$, the power spectral density of the output random process is $P(f).|H(f)|^2$." [1] Consequently,

$$P_{xy}(f) = P_x(f).|H_x(f)|^2 \tag{2.9}$$

$$P_{ey}(f) = P_e(f).|H_e(f)|^2 \tag{2.10}$$

$|H_x(f)| = |H_e(f)| = 1$ for the oversampled case, and $P_e(f) = \sigma_e^2/f_s$ is assumed for white noise, therefore, $P_{ey}(f)$ is also σ_e^2/f_s. The noise power in the signal band, σ_{ey}^2 is [1],

$$\sigma_{ey}^2 = \int_{-f_B}^{f_B} P_{ey}(f)df = 2\int_0^{f_B} P_{ey}(f)df = \int_0^{f_B} \frac{2\sigma_e^2}{f_s}df = \sigma_e^2\left(\frac{2f_B}{f_s}\right) \tag{2.11}$$

Due to the oversampling, some of the noise power remained outside of the signal band, and so the in-band noise power σ_{ey}^2 is less than noise power in the Nyquist rate sampled converter (σ_e^2) [1]. The signal power at the output (σ_{xy}^2) is the same as the input signal power σ_x^2. The maximum achievable SNR in dB is then [1]:

$$SNR = 10\log\left(\frac{\sigma_x^2}{\sigma_{ey}^2}\right) = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) + 10\log\left(\frac{f_s}{2f_B}\right) \tag{2.12}$$

If the oversampling ratio $f_s/2B = 2^r$, signal-to-noise ratio for oversampled converter will be,

$$SNR = 6.02.N + 1.76 + 3.01r \tag{2.13}$$

For every doubling of the oversampling ratio, the SNR increases by about 3 dB, or the resolution improves by one-half bit [2].

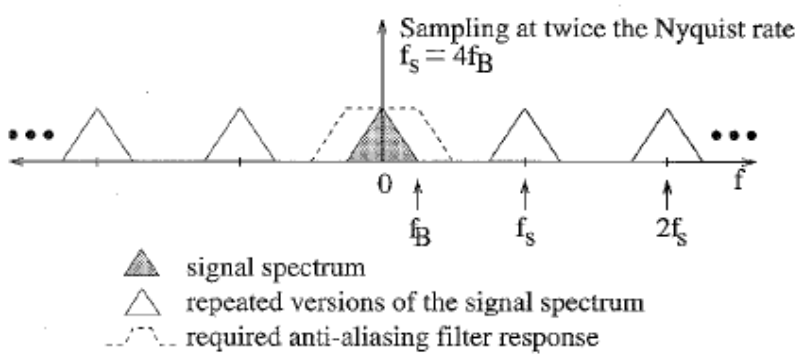

Figure 2.8 Sampling at twice the nyquist rate, showing the original band limited signal spectrum, repeated versions of the signal spectrum due to sampling, and an anti-aliasing filter that is sufficient to band limit the signal.

Oversampling provides another advantage. Since the repeated versions of signal band occurs at frequencies much higher than nyquist frequency, the analog anti-aliasing filter requirement has been relaxed [1]. This can be seen from Figure 2.8, where sampling frequency is four times the signal bandwidth. In this case, the anti-aliasing filter transition can be between B and $f_s/2$ as long as it provides very good attenuation beyond $f_s/2$.

2.2.5. Noise Shaping

The transfer function of the circuit in Figure 2.2 can be written as [21]:

$$Y(z) = STF(z).U(z) + NTF(z).E(z) \tag{2.14}$$

Where *STF* is input signal transfer function and *NTF* is noise transfer function.

$$STF = \frac{H(z)}{1+H(z)} \tag{2.15}$$

$$NTF = \frac{1}{1+H(z)} \tag{2.16}$$

The loop filter is a simple integrator with $H(z) = \frac{1}{z-1}$ (or $H(s) = \frac{1}{s}$ for s-domain). In this case, transfer functions of signal and noise will be [21]:

$$STF(z) = z^{-1} \text{ (or } \frac{1}{s} \text{ for s-domain)} \tag{2.17}$$

$$NTF(z) = 1 - z^{-1} \text{ (or } \frac{s}{s+1} \text{ for s-domain)} \tag{2.18}$$

"We can say that the sigma-delta modulator behaves as high-pass filter on the quantization noise therefore shaping the quantization noise. In other words, the quantization noise is pushed towards the high frequencies that leads to an increase in the SNR. In addition to these, increasing the order of the modulator could increase noise shaping." [21]

We can re-write the previous noise power formula for first-order sigma-delta modulator [2]:

$$\sigma_{ey}{}^2 = \sigma_e{}^2 \frac{\pi^2}{3} \left(\frac{2f_B}{f_s} \right)^3 \tag{2.19}$$

The SNR in dB is then [1]:

$$SNR = 10\log(\sigma_x{}^2) - 10\log(\sigma_e{}^2) - 10\log\left(\frac{\pi^2}{3}\right) + 30\log\left(\frac{f_s}{2f_B}\right) \tag{2.20}$$

Letting the oversampling ratio $f_s/2B = 2^r$, we obtain

$$SNR = 6.02.N - 3.41 + 9.03r \quad (dB) \tag{2.21}$$

We observe that noise shaping brought us 1.5 bit improvement for every doubling of oversampling which is better than the 0.5 bit improvement without noise shaping.

The generalized formula for the noise of an Mth order modulator can be written as below [2]:

$$\sigma_{ey}^{\ 2} = \sigma_{e}^{\ 2} \frac{\pi^{2M}}{2M+1} \left(\frac{2f_B}{f_s} \right)^{2M+1} \tag{2.22}$$

The in-band quantization noise reduces by 3(2*M*+1) dB by doubling the sampling frequency [2]. In Figure 2.9, noise shaping characteristics for modulators with different orders can be seen.

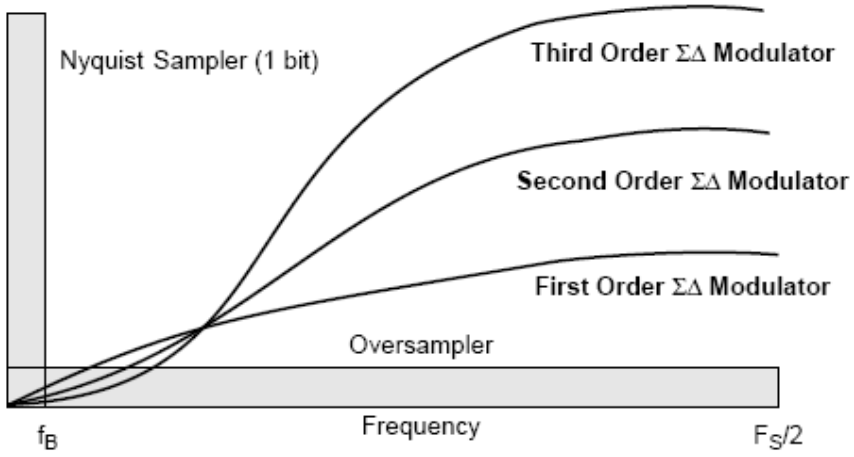

Figure 2.9 Multi-order sigma-delta noise shapers

Figure 2.10 depicts the relationship between quantization noise, OSR, and signal-to-noise ratio (SNR) for modulators with different orders varying from 1 to 5. [8]. The figure shows that as the OSR or the order of the modulator increases, the noise decreases, therefore, SNR increases.

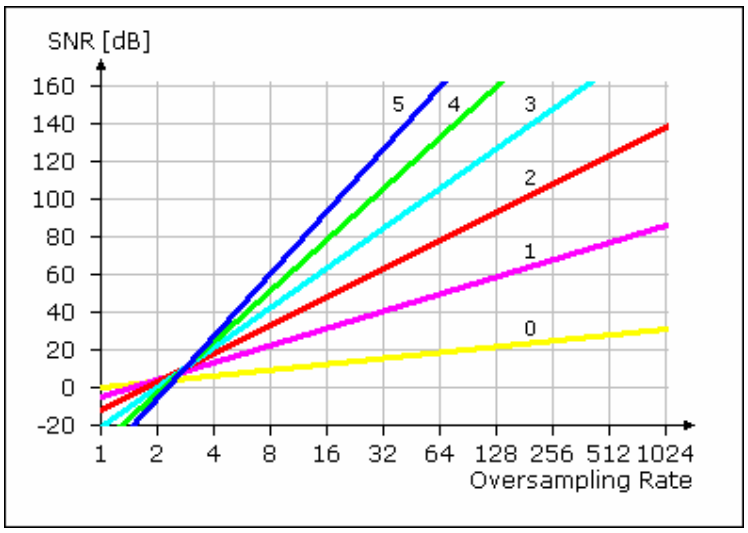

Figure 2.10 SNR vs Oversampling ratio for sigma-delta modulators

2.3. Design Choices

There is numerous design choices for sigma delta modulators. Some are explained below [9].

2.3.1. Discrete-Time vs Continuous-Time

The loop transfer function $H(z)$ is written in the discrete-time (DT) domain. Many sigma-delta modulators in the literature are implemented as discrete-time circuits such as switched-capacitor (SC) or switched-current (SI) circuits [9]. However, the loop filter can be built as a continuous-time (CT) circuit $H(s)$ for example with transconductors and integrators. The reasons of choosing CT method are [9]:

- In typical SC DT sigma-delta modulator, maximum clock rate is limited by opamp bandwidths and circuit waveforms need several clock periods to settle. On the other hand, waveforms in a CT modulator are continuous, and the restriction on opamp bandwidths are relaxed.
- In a DT modulator, large glitches appear on opamp virtual ground nodes due to switching transients. However, opamp virtual grounds can be kept very quiet in CT modulator.

- In the DT modulators, an extra anti-aliasing filter is needed to prevent aliasing between repeated versions of signal spectrum. But antialiasing is an inherent property of the CT modulators.
- For the same specifications, CT modulators will have low power consumption than their DT counterparts.

2.3.2. Low-Pass vs Band-Pass

Since integrators have poles at DC, $H(z)$ built from integrators will shape noise away from DC [9]. If the quantization noise is required to have a high-pass shape, modulators are built with low-pass loop filters and called low-pass (LP) converters. $H(z)$ can be also built out of resonators. In this case, the noise would be shaped away from the resonant frequency [9]. Because the loop filter is band-pass, modulators built from this loop filter are called band-pass (BP) converters.

2.3.3. Single Stage vs Multi Stage

"Many modulators employ a single quantizer with multiple feedback loops leading to various points inside the forward modulator path, and these are called single stage or multiloop modulators. It is possible to build stable high-order modulators out of two or more low order modulators where later modulators' inputs are the quantization noise from the previous stages. Thus, the first-order noise is canceled in the output and the modulator achieves second-order quantization noise shaping. In principle, this can be extended to *m*th order noise shaping." [9]

2.4. Digital Decimation Filtering

The process of decimation is used in a sigma delta converter to eliminate redundant data at the output [10]. According to the sampling theorem, sampling rate must be 2 times the input signal bandwidth in order to reliably reconstruct the input signal without distortion. However, there is some undesirable noise at high frequencies due to noise shaping. This redundant data can be eliminated without distortion.

The main aim of digital filtering is to prevent noise at high frequencies from folding into signal band. Its second task is to convert the low resolution, high sample rate data coming from quantizer into high resolution, low sample rate data. Consequently, decimation process contains both averaging filter function and sample rate reduction at the same time [10].

"High resolution is achieved by averaging over f_s/B data points to interpolate between the coarse quantization levels of the modulator." [10] The process of averaging is the same as low-pass filtering in the frequency domain. When the quantization noise at high frequencies is removed, sampling rate can be reduced to the Nyquist rate [10].

Three basic tasks are performed in the digital filter sections [10]:

- Low-pass filtering: The Sigma-delta modulators suppress quantization noise in the baseband and push most of the quantization noise to high frequencies. The digital filter removes this out-of-band quantization noise and leaves baseband quantization noise and input signal component.
- Sample rate reduction: The output of the sigma-delta modulator has high sampling rate. The amount of information can be reduced by decreasing the sampling rate down to the Nyquist rate.
- Anti-aliasing: Because averaging function in the frequency domain provides attenuation at the multiple points of signal bandwidth, aliasing due to the sampling process at those points will be removed.

There are some factors that make the implementation of digital filter difficult [10]:

- The input sampling rate of the modulator is very high, therefore, the digital decimation filter must perform computationally intensive signal processing algorithms in real time.
- Quantization noise is shaped better for higher order modulators. Thus, the low-pass filtering characteristic of decimation filter must be sharper for such modulators.
- For some special applications, magnitude and phase characteristics of the input signal in the baseband must not be distorted.

"The simplest and most economical filter to reduce the input sampling rate is a "Comb-Filter", because such a filter does not require a multiplier. A multiplier is not required because the filter coefficients are all unity [11]. This comb-filter operation is equivalent to a rectangular window finite impulse response (FIR) filter. However, the comb-filter is not sufficient for filtering the large portion of out-of-band quantization noise and usually used in practice with additional digital filters. Additionally, the frequency response of the comb-filter can cause some magnitude drooping at the baseband which can not be tolerated in some applications." [10]

2.4.1. Comb-Filter Design as a Decimator

A comb-filter of length N is a FIR filter with all N coefficients equal to one [10]. The transfer function of a comb-filter is:

$$H(z) = \sum_{n=0}^{N-1} z^{-n} = \frac{Y(z)}{X(z)} \tag{2.23}$$

For N = 4, equation 2.23 becomes:

$$y(n) = x(n) + x(n\text{-}1) + x(n\text{-}2) + x(n\text{-}3) \tag{2.24}$$

A comb filter is a simple accumulator which performs a moving average [10]. Equation 2.23 can be expressed in closed form as:

$$H(z) = \frac{1 - z^{-N}}{1 - z^{-1}} = \frac{Y(z)}{X(z)} \tag{2.25}$$

or, in the discrete-time domain for N = 4:

$$y(n) = x(n) - x(n\text{-}4) + y(n\text{-}1) \tag{2.26}$$

Equation 2.25 can be expressed as multiplication of two separate parts, namely integration and differentiation as shown in equation 2.27.

$$y(z) = \left[\frac{1}{1-z^{-1}}\right]\left[1-z^{-N}\right]x(z) \tag{2.27}$$

Since there is an N:1 down sampler after the integrator, differentiator can operate at a lower rate. This is shown in Figure 2.11 for a general N:1 comb-filter. In order to prevent the accumulator overflow from causing an error, two's complement or "wrap around" arithmetic must be used [12].

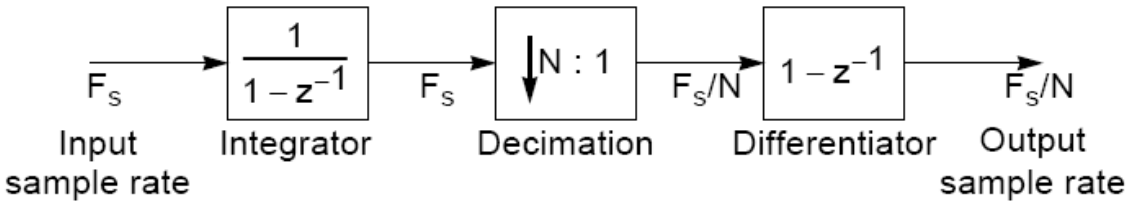

Figure 2.11 Block Diagram of One-Stage Comb Filtering Process

The transfer function and magnitude response of a comb-filter with the filter window length N = 16 followed by a 16:1 decimation process are shown in Figure 2.12. In summary, the comb-filter decimator has the following advantages [11]:

- No multipliers are required
- No storage is required for filter coefficients
- Intermediate storage is reduced by integrating at the high sampling rate and differentiating at the low sampling rate, compared to the equivalent implementation using cascaded uniform FIR filters
- The structure of comb-filters is very "regular" consisting of two basic building blocks
- Little external control or complicated local timing is required
- The same filter design can easily be used for a wide range of rate change factors, N, with the addition of a scaling circuit and minimal changes to the filter timing

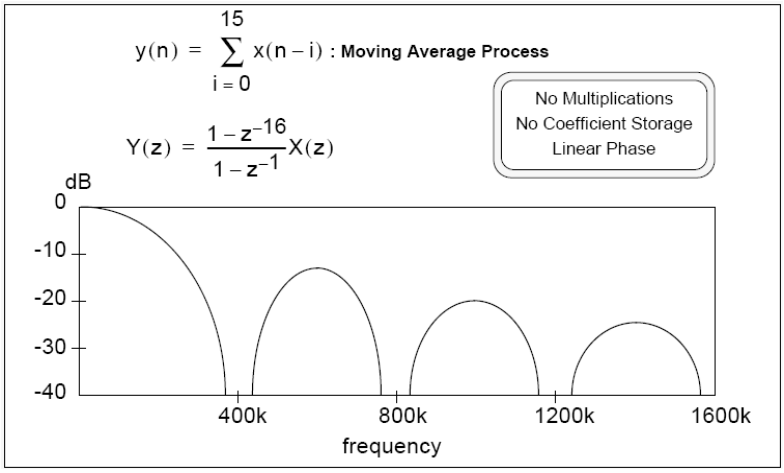

Figure 2.12 Transfer Function of a Comb-Filter

A single comb-filter stage may not be enough to attenuate aliasing occuring at the multiple points of signal band. In this case, comb-filters can be cascaded to increase attenuation at those points. Figure 2.13 shows a structure of four cascaded comb filters and the resulting spectrums for four different orders.

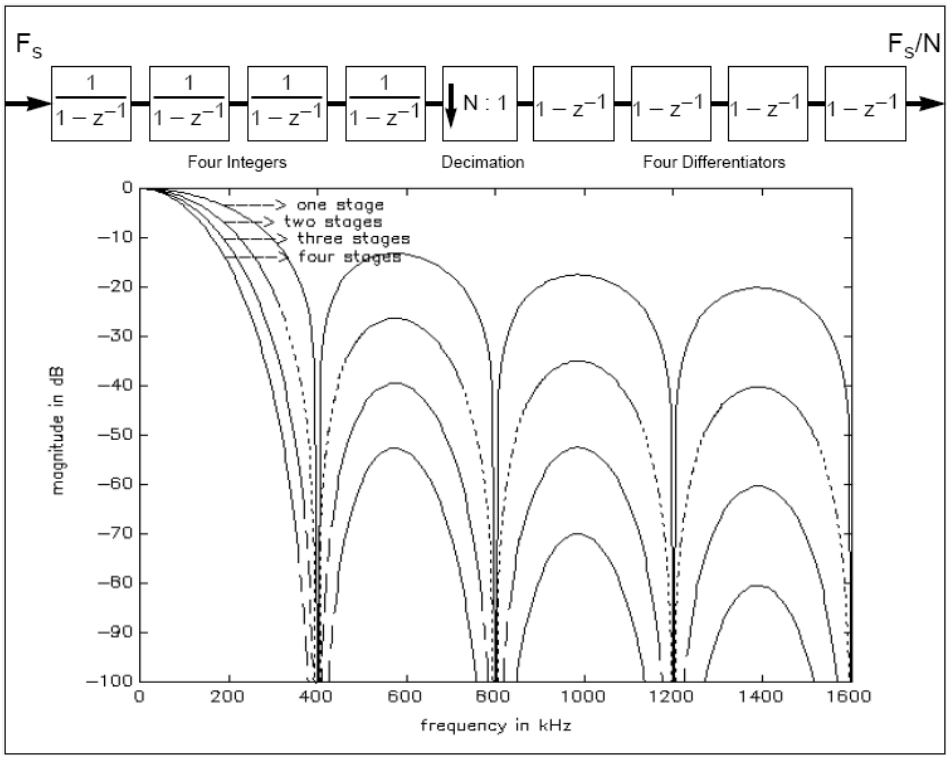

Figure 2.13 Cascaded Structure of a Comb-Filter

3. SIGMA-DELTA MODULATOR DESIGN

As can be seen from Figure 2.2, modulator consists of three blocks which are integrator, quantizer and DAC. Integrator is a low-pass filter which is used for constructing a noise shaping characteristic. Quantizer is used to convert continuous-time signals to discrete-time digital signals to be used by digital filter. Finally, a D/A converter is used in the feedback loop to convert digital outputs of quantizer to analog signals. In this section, we will focus on the design of those blocks.

3.1. Current-mode Integrator

Continuous-time current-mode integrators based on the current-mirror circuit are shown in Figure 3.1 [13]. When output conductances and parasitic capacitances are ignored, the transfer function of the current-mirror circuit from the small-signal equivalent circuit can be derived as [13],

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{-\frac{g_{m11}}{C}}{s + \frac{g_{m1}}{C}} \tag{3.1}$$

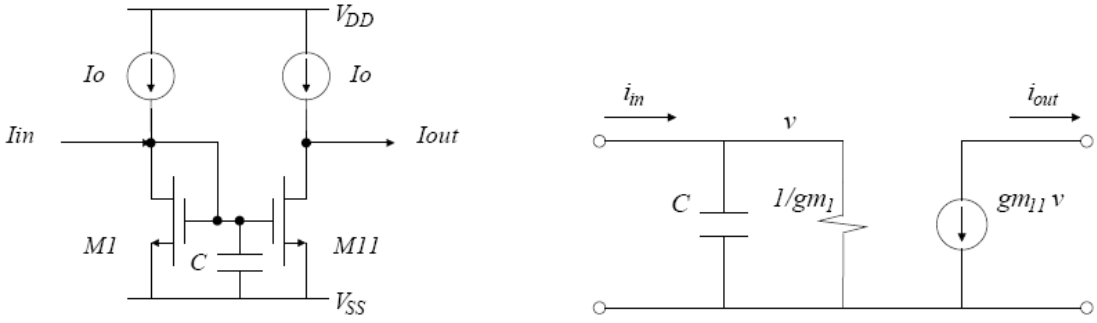

Figure 3.1 The simple current-mirror and its small-signal equivalent circuit.

The differential current-mode integrator is shown in Figure 3.2 [13]. The circuit is built by two cross-coupled current-mirrors. If $H_1(s)$ and $H_2(s)$ are the transfer functions of the two current-mirrors, the differential output current can then be described by [13].

$$i_{outp}(s)-i_{outn}(s)=\left[\frac{H_1(s)H_2(s)-H_1(s)}{1-H_1(s)H_2(s)}\right]i_{inp}(s)-\left[\frac{H_1(s)H_2(s)-H_2(s)}{1-H_1(s)H_2(s)}\right]i_{inn}(s) \quad (3.2)$$

Assuming $i_{in}(s) = i_{inp}(s) = -i_{inn}(s)$, the input-output relation is found to be [13],

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{in}(s)}=\frac{2H_1(s)H_2(s)-H_1(s)-H_2(s)}{1-H_1(s)H_2(s)} \quad (3.3)$$

by substitution from equation 3.1 into equation 3.3, we get [13],

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{in}(s)}=\frac{s\frac{g_{m11}+g_{m22}}{C}+\frac{g_{m1}g_{m22}+g_{m2}g_{m11}+2g_{m11}g_{m22}}{C^2}}{s^2+s\frac{g_{m1}+g_{m2}}{C}+\frac{g_{m1}g_{m2}-g_{m11}g_{m22}}{C^2}} \quad (3.4)$$

When all mirror transistors are selected to have the same transconductance g_m, the transfer function of the differential circuit shown in Figure 3.2 becomes [13]:

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{inp}(s)-i_{inn}(s)}=\frac{g_m}{sC} \quad (3.5)$$

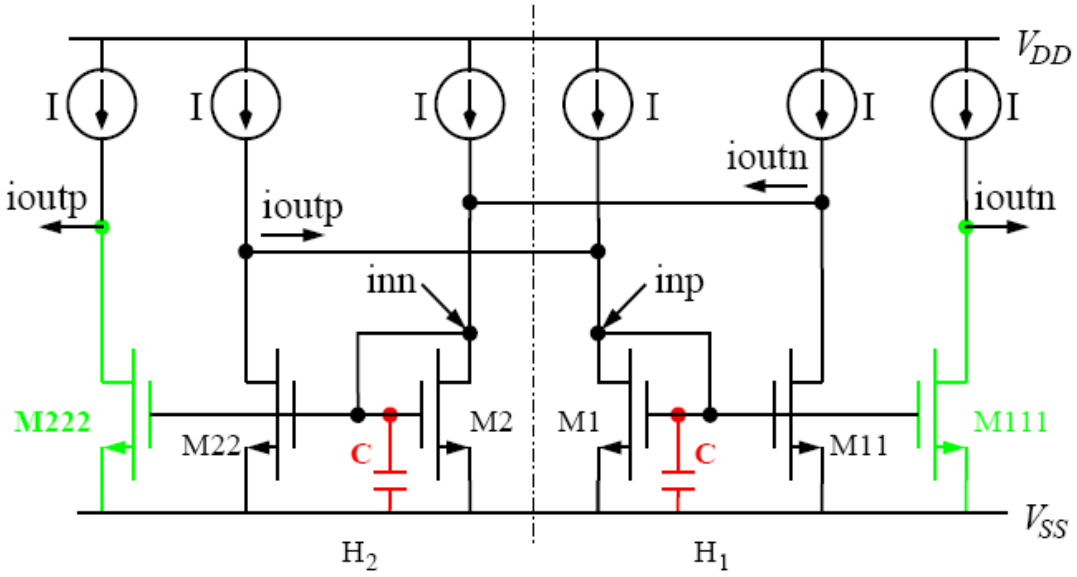

Figure 3.2 Differential current-mode integrator

In the derivation of equation 3.4, the output conductance of the mirror transistors has been neglected. When output conductances are considered, the transfer function of the differential current-mode integrator will be [13]:

$$\frac{i_{outp}(s)-i_{outn}(s)}{i_{inp}(s)-i_{inn}(s)}=\frac{\frac{g_m}{C}}{s+\frac{g_{ds}}{C}} \tag{3.6}$$

The DC gain of the integrator is dependent on g_{ds}. Cascode current-mirror configuration can be used to achieve low output conductance [13]. Cascode current-mirror-based integrator is shown in Figure 3.3,

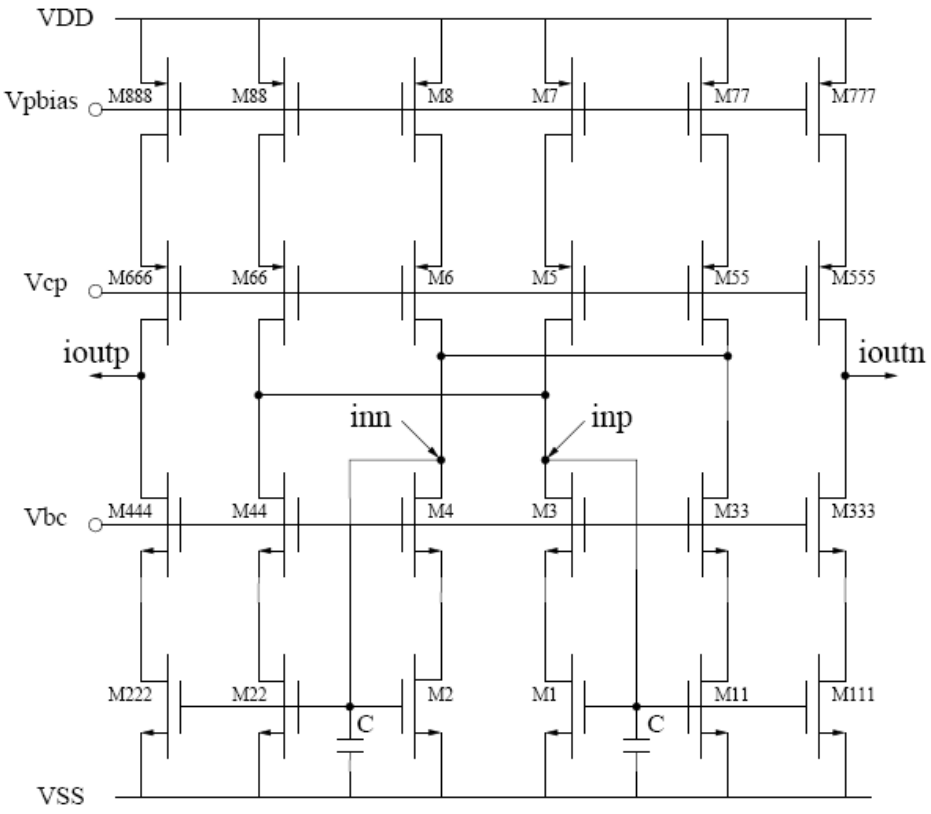

Figure 3.3 Differential cascode current-mode integrator.

3.2. Quantizer

In sigma-delta converters, quantizer converts analog signals to digital signals. In one-bit modulators, quantizer is simply a comparator. For this thesis, we design a three-bit modulator so we should design a three-bit A/D converter as quantizer. Due to its fast operation, we prefer Flash ADC structure. A typical current-mode three-bit A/D converter is shown in Figure 3.4 [14]. In Flash A/D converters, most important part is comparator. There are eight comparators whose outputs are current logic levels.

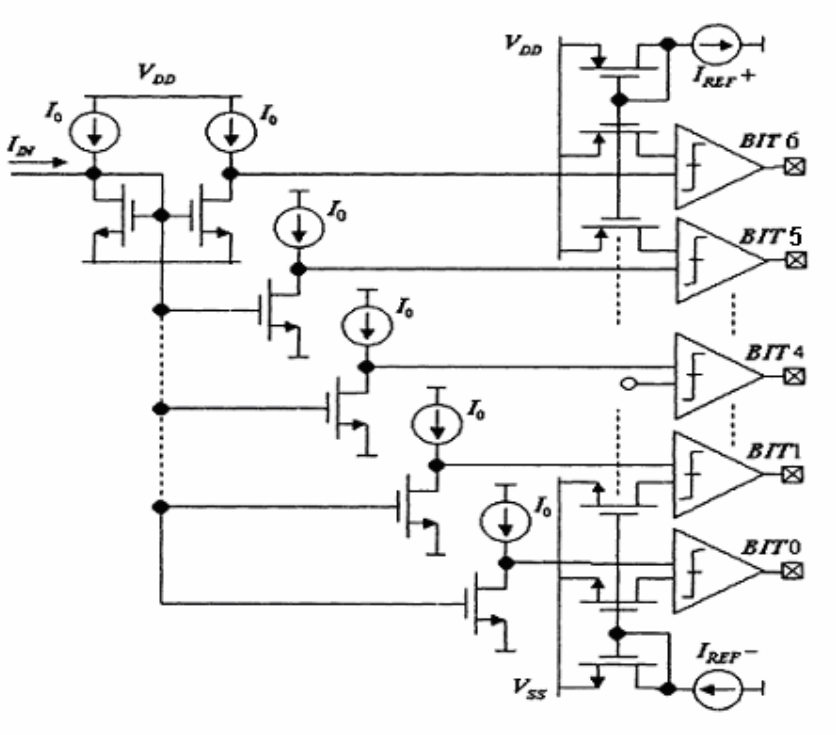

Figure 3.4 Current-mode A/D converter architecture

3.2.1. Current Comparator

Current comparators can be implemented by using transimpedance stages or positive feedback mechanism. Some comparators using those techniques are reported in [15] – [18]. However, these comparators give voltage output. A typical current-mode comparator has a transfer characteristic as shown below,

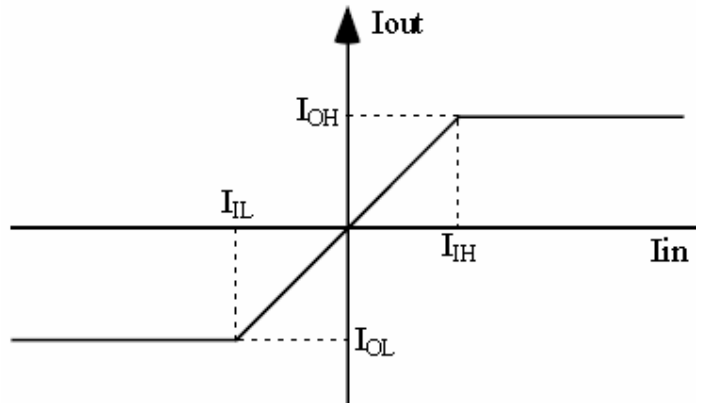

Figure 3.5 Transfer characteristic of a current-mode comparator

These characteristics can be considered as piecewise linear transfer characteristics and can be implemented with current mirrors [19]. The circuit below can be used for synthesis of these characteristics.

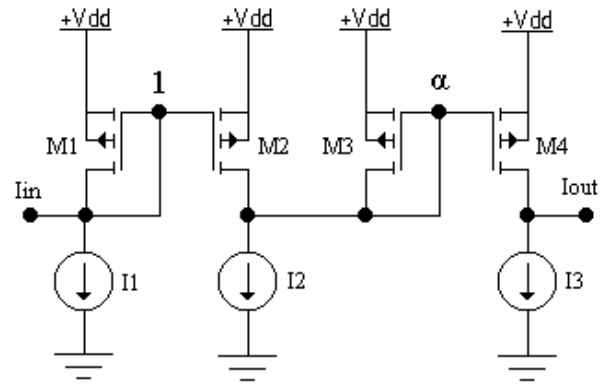

Figure 3.6 PMOS circuit which is used for the synthesis of comparator characteristic

In the circuit above, if Iin is greater than I1, M1 and M2 transistors will be turned off, thus I2 current will flow through M3. Current of M4 is determined by the ratio α which is expressed by W_4/W_3 for the same channel length. When Iin is lower than (I1-I2), M3 and M4 will be turned off since current of M2 can not exceed I2. In this case, output current will be -I3.

This structure has some problems to be used as a comparator. First, we should pick I1 current small to be able to have a characteristic close to ideal. Thus, we should increase the ratio α to get same output current level. Second, reducing I1 current increases input resistance, so speed of the circuit decreases. To eliminate those limitations, we can magnify input current. So we should use an amplifier before this circuit.

PMOS and NMOS current mirrors can be connected as below to form a current amplifier.

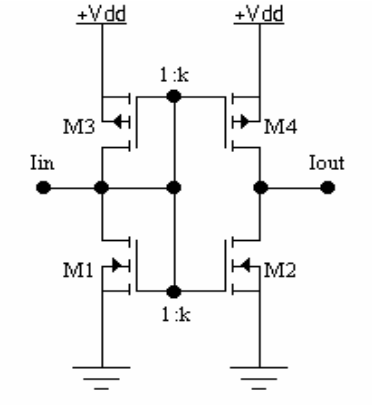

Figure 3.7 Current amplifier

In Figure 3.7, gain is determined by the ratio of W2/W1=W4/W3. Output resistance $r_{out} = \frac{1}{g_{ds1} + g_{ds2}}$ will be small for high gain and this reduces bandwidth. To increase bandwidth, several current mirrors with low gain can be cascaded. In this case, loading effect of next blocks will be smaller. The final comparator block diagram and circuit are shown below.

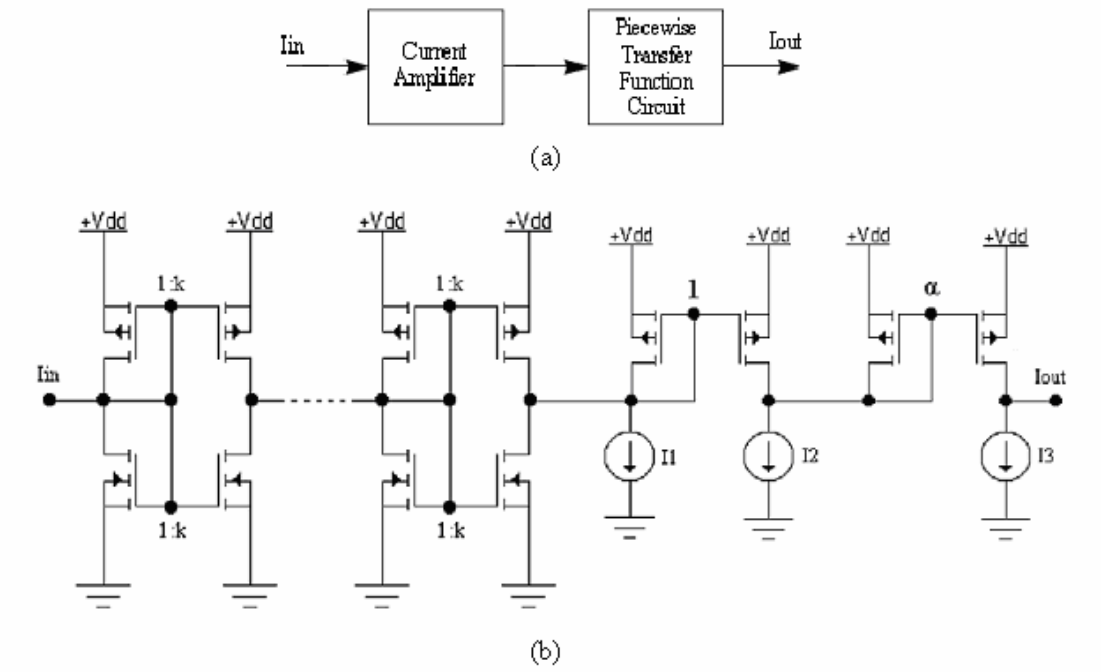

Figure 3.8 (a) Final current comparator block diagram (b) final schematic of the circuit.

3.2.2. Flash ADC

After designing comparator, we can use it to build ADC structure. We designed a circuit similar to structure shown in Figure 3.4. At the input, we used a simple sample-and-hold mechanism combining a transmission gate as a switch and a capacitor to hold the sampled voltage value [20]. Then, we use some reference currents at the inputs of comparators to form decision points of DAC characteristic. This structure is shown in Figure 3.9.

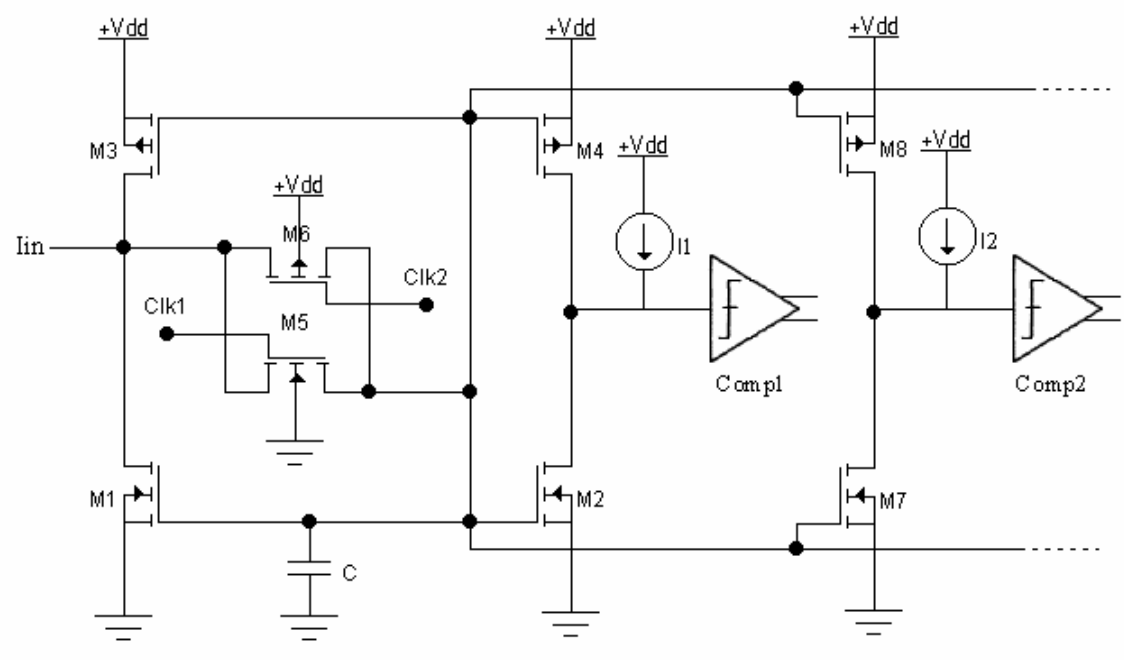

Figure 3.9 Current-mode Flash ADC

3.3. DAC

In the modulator loop, it is necessary to use a three-bit DAC. This D/A converter is used to convert digital output of A/D converter to an analog signal level and to feedback this analog output to the input. Normally, a three-bit ADC has seven comparators and seven-bit output of those comparators are thermometer code. This seven-bit digital signal should be converted to three-bit voltage output which will be used by DAC to form analog output levels. But this process can be made shorter using comparator outputs directly. Since ADC is designed in current-mode, comparator outputs are current; thus, those

currents can be summed to form DAC current levels. The necessity for a DAC in the feedback loop can be eliminated by this way.

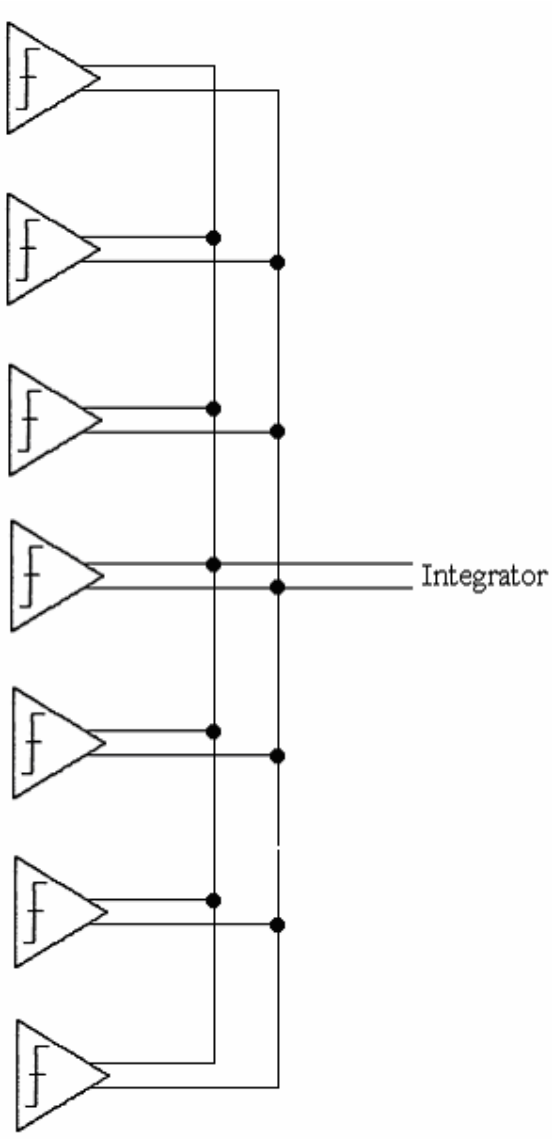

Figure 3.10 Acquisition of DAC levels by using comparator outputs

3.4. Differential/Single Converter

Integrator output is differential. However, the designed quantizer is a three-bit ADC which has a single input. So there is a necessity to obtain a single output from the differential integrator output [21].

Figure 3.11 shows the diagram of this mentioned circuit. Simply, it takes the integrator currents and takes the difference between them using cascode current mirrors.

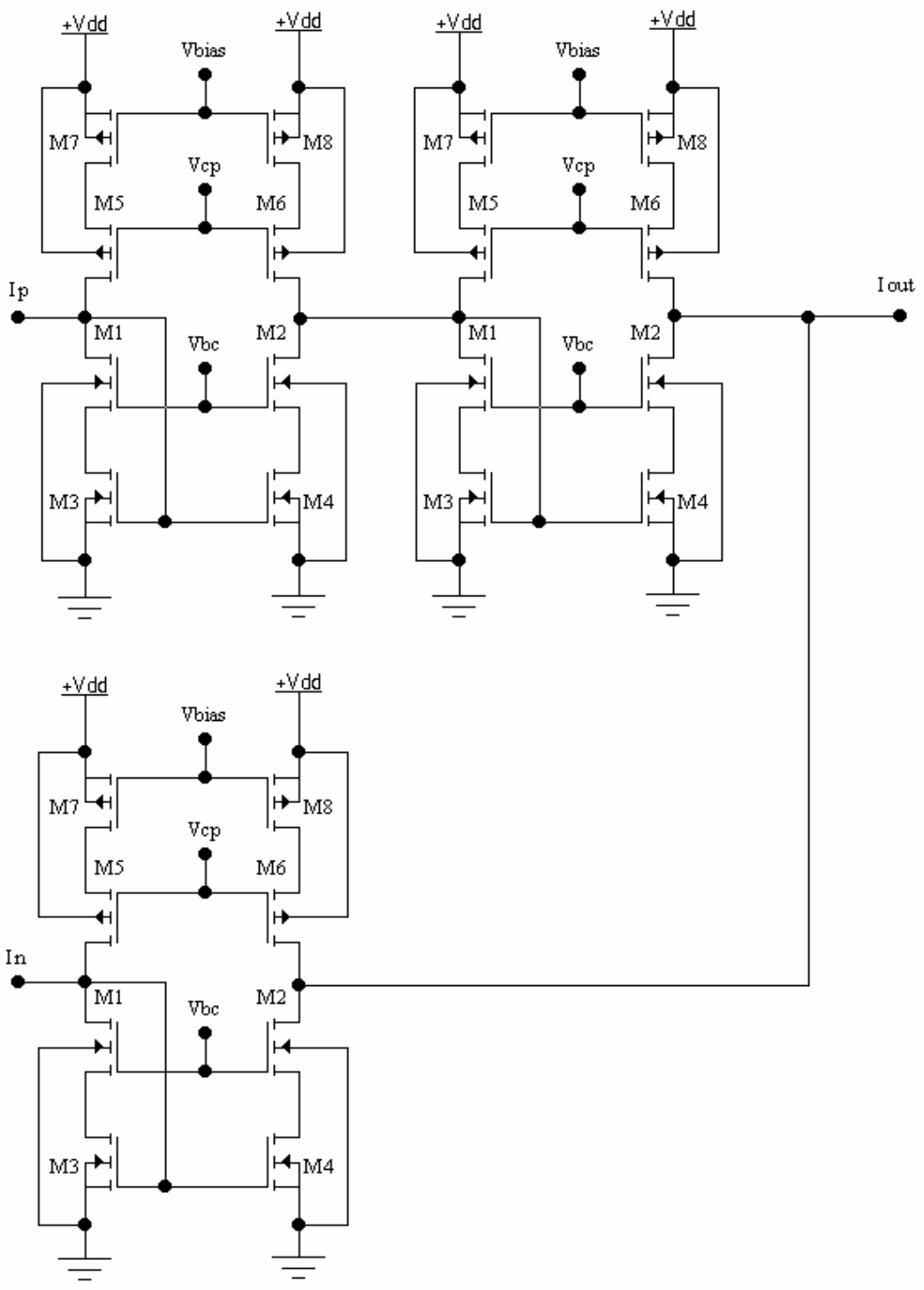

Figure 3.11 Differential/Single Converter circuit diagram

4. DIGITAL FILTER DESIGN

At the output of the modulator, a digital filter is used for increasing the bit number (resolution) of the modulator output, for reducing sampling rate, and for suppressing noise in high frequencies. Low-pass filter characteristics and reduction of sampling rate can be realized by an averaging circuit. Transfer functions of an averaging circuit in time and frequency domains are shown below [12].

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{k}\sum_{x=0}^{k-1} z^{-x} = \frac{1}{k}\frac{1-z^{-k}}{1-z^{-1}} \tag{4.1}$$

$$H(f) = \frac{\sin c(k\pi \frac{f}{f_s})}{\sin c(\pi \frac{f}{f_s})} \tag{4.2}$$

Those expressions are time and frequency transfer functions of a sync filter. Since CIC filter is the most economical sync filter, it is preferred for implementing digital filter. As in other filter types, there are some main digital blocks in CIC filter. Those are adders and delay elements. Thus, current-mode design of those elements will be explained in this section.

4.1. Building Blocks

The two basic building blocks of a CIC filter are integrator and comb.

4.1.1. Digital Integrator

"The integrator circuit is similar to an accumulator which is used to accumulate or store the sum of the input data. It is a single-pole Infinite Impulse Response (IIR) filter with a filter coefficient of one." [12] The transfer function of the integrator in time domain is shown in equation 4.3.

$$y[n] = y[n-1] + x[n] \tag{4.3}$$

The transfer function for an integrator on the z-plane is

$$H_I(z) = \frac{1}{1 - z^{-1}} \tag{4.4}$$

It is observed from equation 4.3 that the output of the integrator is the summation of the present input and the past output [12]. A data flow diagram representation of the digital integrator is shown in Figure 4.1.

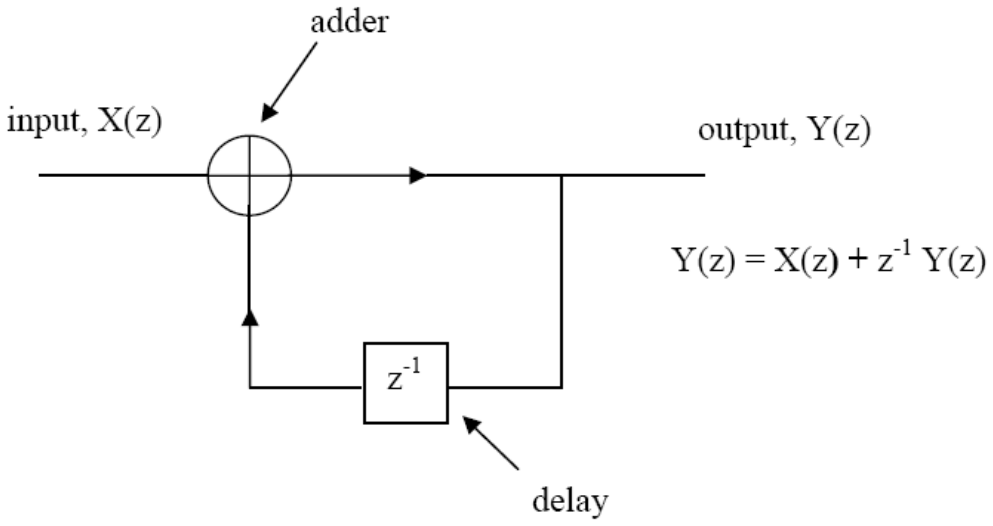

Figure 4.1 Block diagram of a digital integrator

4.1.2. Digital Differentiator (Comb)

A differentiator circuit also called comb filter is a Finite Impulse Response (FIR) filter [12]. Equation 4.5 shows the time domain behaviour of the differentiator. As can be seen from the time domain representation, the output of the differentiator is the difference between the present input and the past input [12].

$$y[n] = x[n] - x[n-1] \tag{4.5}$$

$$H(z) = \frac{Y(z)}{X(z)} = 1 - z^{-1} \tag{4.6}$$

The data flow diagram of the differentiator is shown in Figure 4.2. Both integrators and differentiators consist of full-adders and delay elements. Thus, current-mode design of those blocks is important.

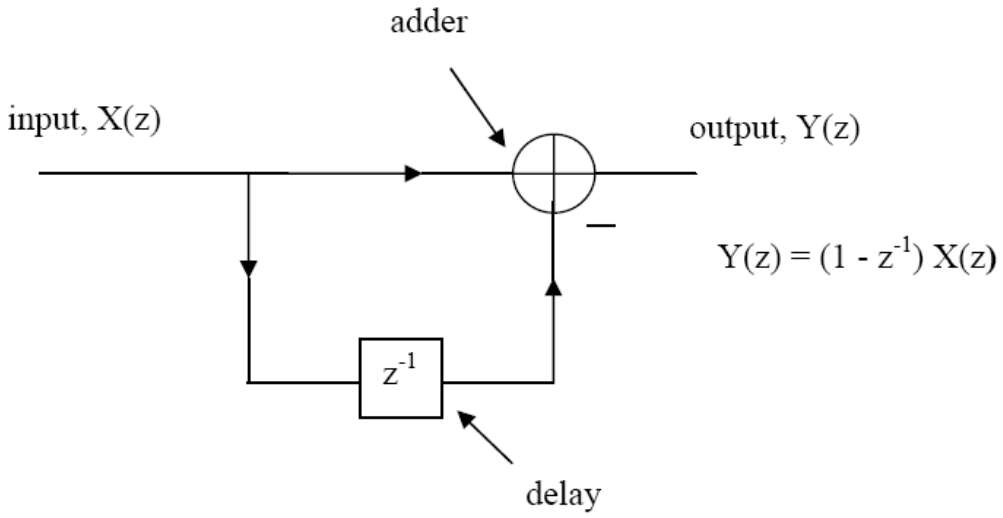

Figure 4.2 Block diagram of a digital differentiator (comb filter).

4.1.3. Full-Adder

In the literature, there is a limited number of current-mode full-adder designs. General approach is to make threshold detector circuits and combine them to construct transfer characteristics of full-adder outputs. Input/output characteristics for carry and sum outputs of a full-adder are shown in Figure 4.3 [22].

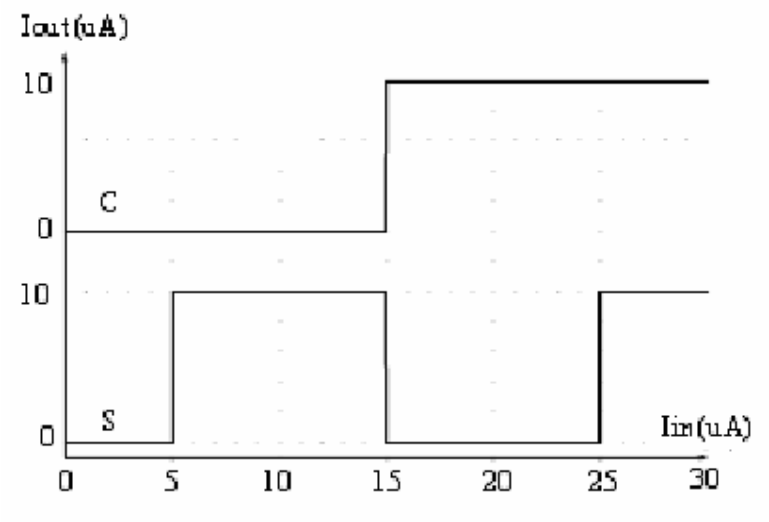

Figure 4.3 Carry and Sum outputs for a current-mode full adder

As a threshold detector, circuit in Figure 4.4 can be used [23]. If Iin is greater than Iref, Iout will be 10uA (logic1 is assumed to be this value) otherwise zero. This current comparator uses a buffer as the input stage and a CMOS inverter as the positive feedback, which offers lower input resistance and faster response time [23]. To form sum characteristics, we need three of those circuits for different reference currents. Those circuits can be combined to form full-adder as shown in Figure 4.5 with an extra inverter for second threshold detector. At the output, an 10 uA current source is used because summation of three threshold detectors' outputs varies between 10-20uA. Carry output can also be provided by second threshold detector.

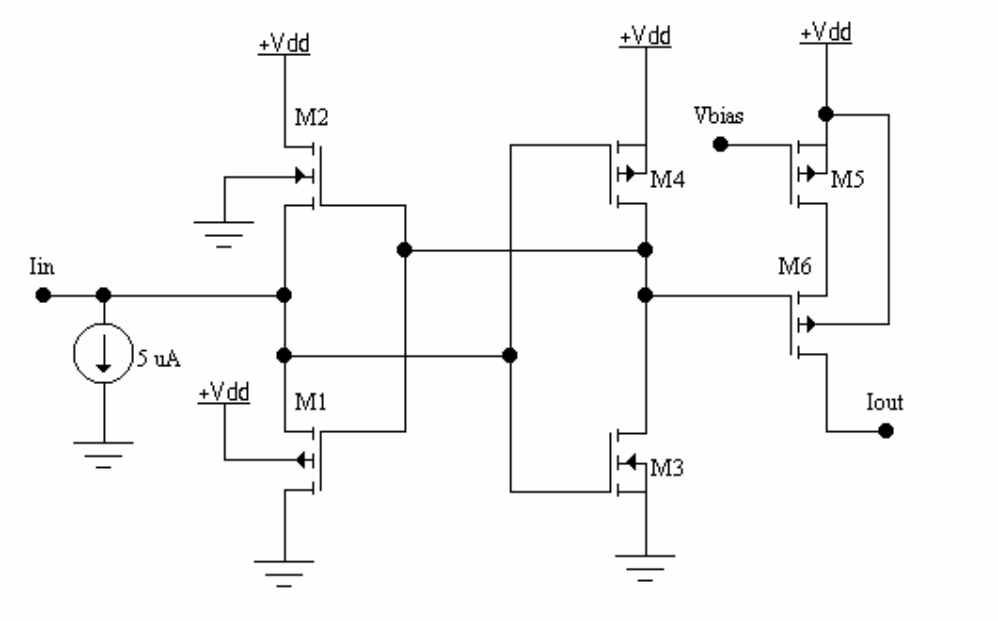

Figure 4.4 Current-mode threshold detector

Operation conditions of threshold detectors used in full-adder are shown in Table 4.1

Table 4.1 Operation conditions of threshold detectors used in full-adder

Threshold Detectors	Operating Conditions
Threshold Detector 1	Iin > 5uA → Iout = 10uA Iin ≤ 5uA → Iout = 0uA
Threshold Detector 2	Iin > 15uA → Iout = 0uA Iin ≤ 15uA → Iout = 10uA
Threshold Detector 3	Iin > 25uA → Iout = 10uA Iin ≤ 25uA → Iout = 0uA

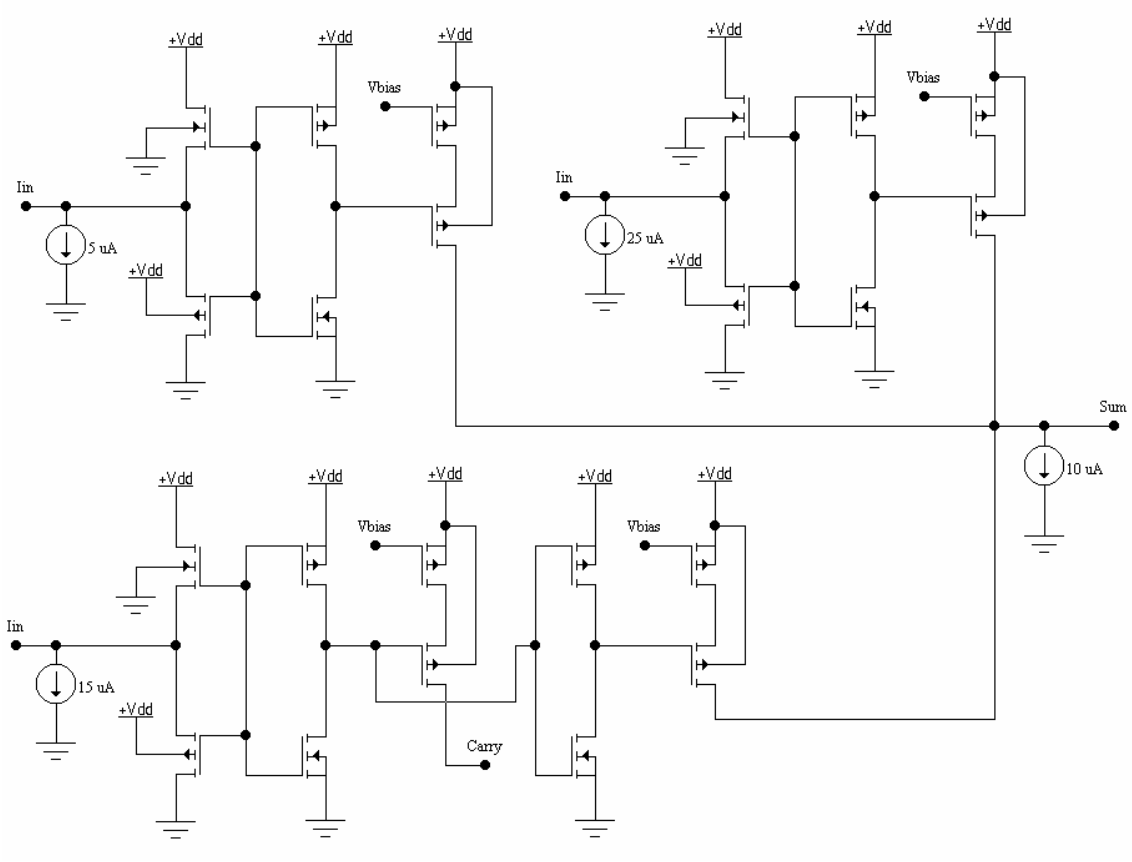

Figure 4.5 Current-mode full adder

4.1.4. Delay Element

The function of delay element is to shift input signal for one clock cycle. The circuit is shown in Figure 4.6. We used another CMOS inverter-based threshold detector circuit [24] here whose threshold current is determined by transistor sizes of inverter. There are two complementary clock signals controlling the circuit. While Clk1 is low and Clk2 is high, first transmission-gate switch turns on and M1, M4, M5 and M6 form threshold detector (threshold current is 5uA adjusted by M4 and M5 sizes). While Clk1 is high and Clk2 is low, first switch turns off and second switch turn on but same current keeps flowing from M6. When first switch is off, Cgs capacitance at the gate terminals of M4 and M5 holds the voltage on this node, but there will be some change on this voltage due to some effects such as charge injection, clock feed-through etc. Since threshold detector circuits used here have sharp characteristics, output currents of this circuit will not be affected by

this change. That is why threshold circuits are used in delay element. At second clock phase, second switch opens and current coming from first clock phase flows at output.

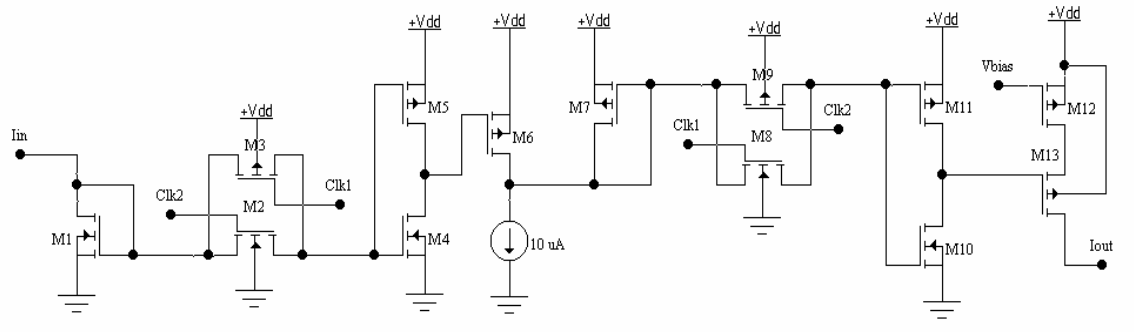

Figure 4.6 Current-mode digital delay element

4.2. Complete Digital Filter

After designing full-adder and delay element, we can form digital filter. Since we increase resolution in digital filter, each column has integrators (or combs) as much as the number of the final output bits. There is a down-sampling unit between integrator and comb parts. Sampling rate of the digital signal is reduced here. D type flip-flops can be used as down-sampling elements triggered by f_s/R (R is oversampling ratio) [25]. An example of second order CIC filter is shown in Figure 4.7.

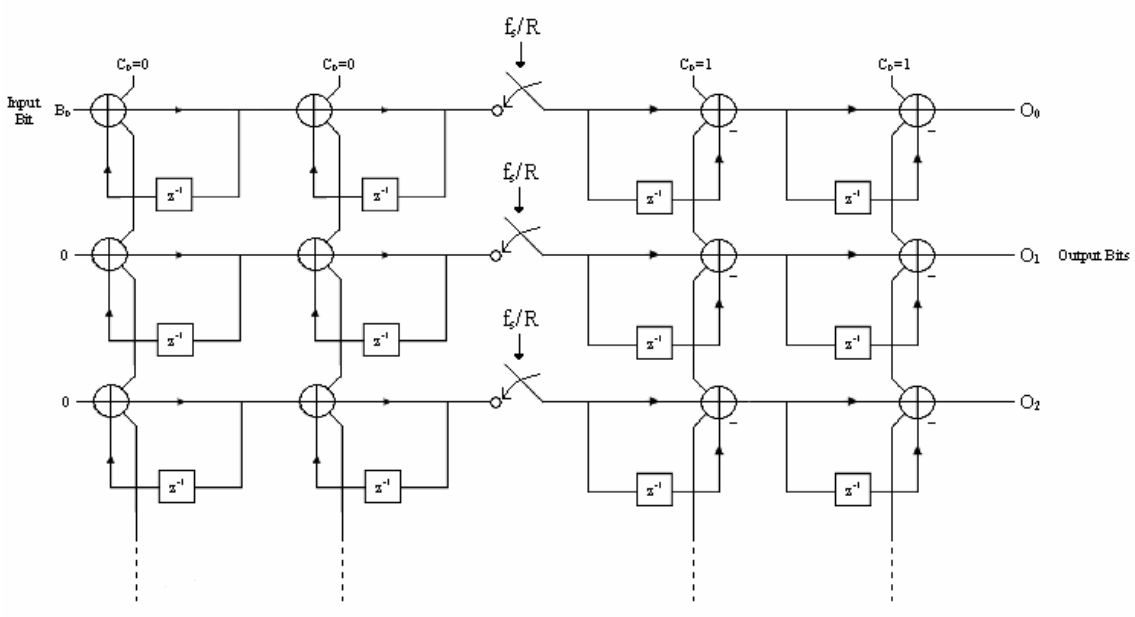

Figure 4.7 An example of second order, three bit CIC filter

Since integrator outputs are current, we should convert it to voltage before down-sampling unit. An current input, voltage output simple comparator can be used for this conversion process. This comparator is shown in Figure 4.8 [26]. In order to get rail-to-rail swing, cascaded inverters can be added at the output.

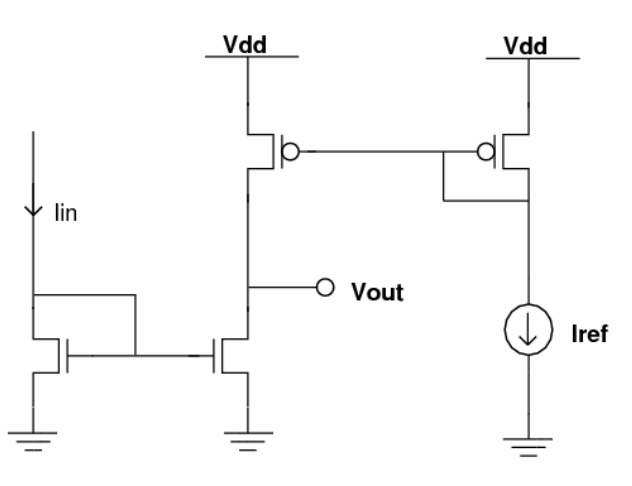

Figure 4.8 A simple current/voltage converter

5. REVIEW OF CURRENT COMPARATOR

Current comparator explained in third section has some drawbacks. Those drawbacks can be described as follows:

- Cascaded current mirror amplifier circuit used in comparator consumes high power and increases overall power consumption
- Lengths of output transistors have been selected small to boost bandwidth of comparator. However, small transistor lengths reduces output resistances and voltage variation over those transistors causes their saturation current to change. Thus, there will be misplaced DAC current levels in the feedback. DAC non-linearity is one of the main reasons of distorsion at output spectrum of modulators

Current-mode threshold detector depicted in Figure 4.4 can be used as comparator. Since threshold detector has a separate current source at the output, output conductances can be adjusted without affecting speed. Second reason to use threshold detector is that since it has no current amplifier, usage of threshold detector greatly reduces overall power consumption.

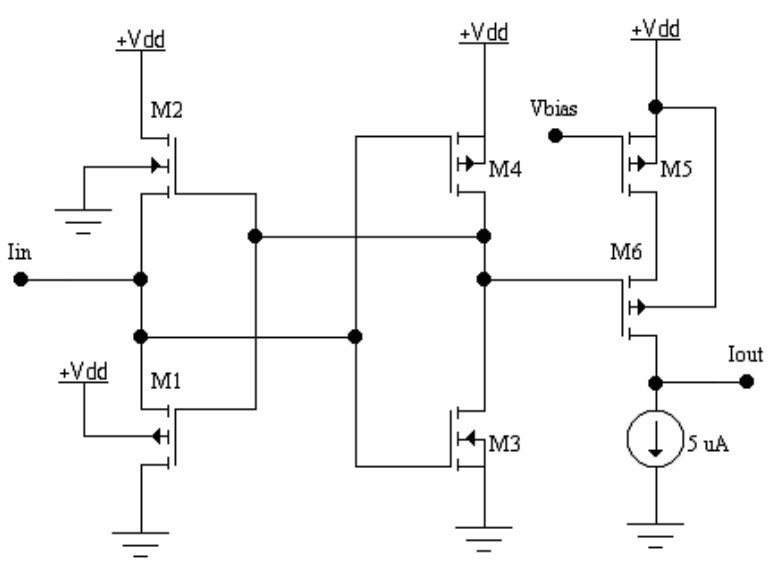

Figure 5.1 Usage of threshold detector as current comparator

6. SIMULATION RESULTS

All simulations have been made for 0.35 u CMOS technology and Vdd = 2.5 V.

6.1. Current Mode Integrator

First circuit which has been simulated is integrator. Integrator has a gain of g_m/sC. Due to output conductances, there is a DC gain for low frequencies. Cut-off frequency can be adjusted by output conductance and capacitor due to formula below.

$$f_{-3dB} = 2.\pi.R_{out}.C \tag{6.1}$$

Frequency result of current-mode integrator is shown in Figure 6.1.

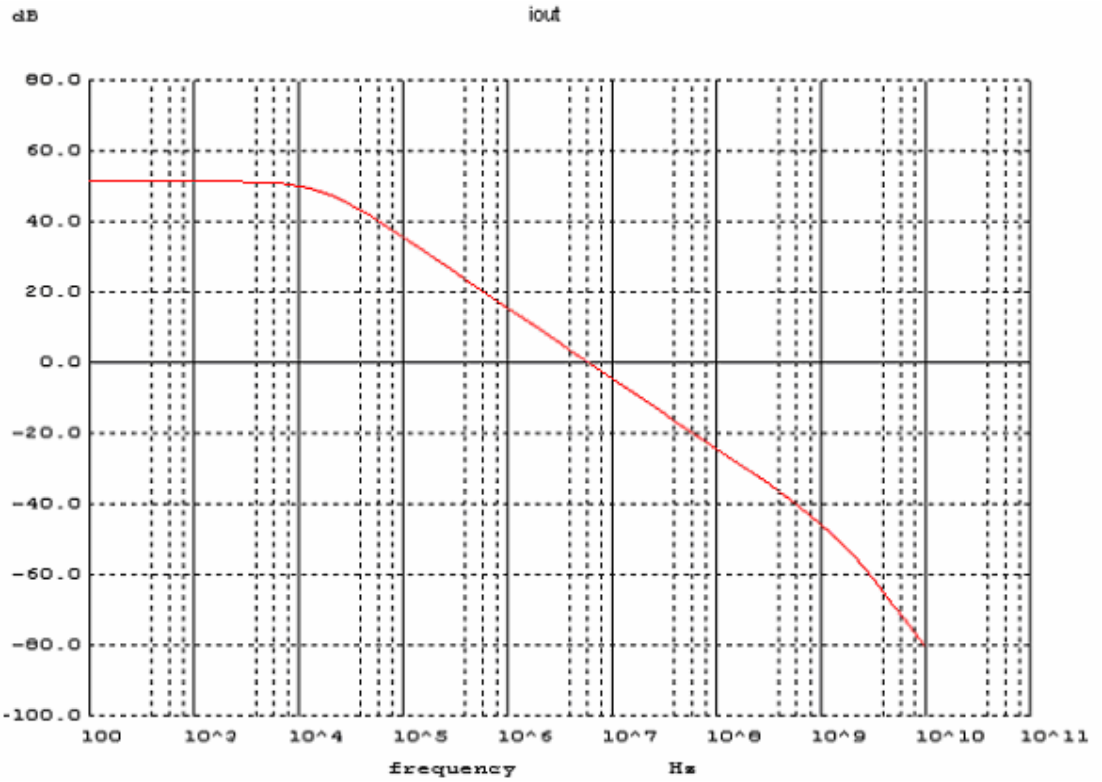

Figure 6.1 Frequency response of current-mode integrator

Table 6.1 Transistor dimensions and bias voltages for current-mode integrator

Variables	Values
$W_1/L_1, W_{11}/L_{11}, W_{111}/L_{111}, W_2/L_2, W_{22}/L_{22}, W_{222}/L_{222}$	7u/1.4u
$W_3/L_3, W_{33}/L_{33}, W_{333}/L_{333}, W_4/L_4, W_{44}/L_{44}, W_{444}/L_{444}$	56u/0.7u
$W_5/L_5, W_{55}/L_{55}, W_{555}/L_{555}, W_6/L_6, W_{66}/L_{66}, W_{666}/L_{666}$	43.05u/0.35u
$W_7/L_7, W_{77}/L_{77}, W_{777}/L_{777}, W_8/L_8, W_{88}/L_{88}, W_{888}/L_{888}$	35u/1.4u
Vbias	1.25 V
Vcp	1.8 V
Vbc	0.8 V
C	10 pF

According to AC analysis, gain of integrator at 1 MHz is 15.7 dB. Transient simulation result for 2 uA sine input waveforms with 180˚ phase difference is shown in Figure 6.2.

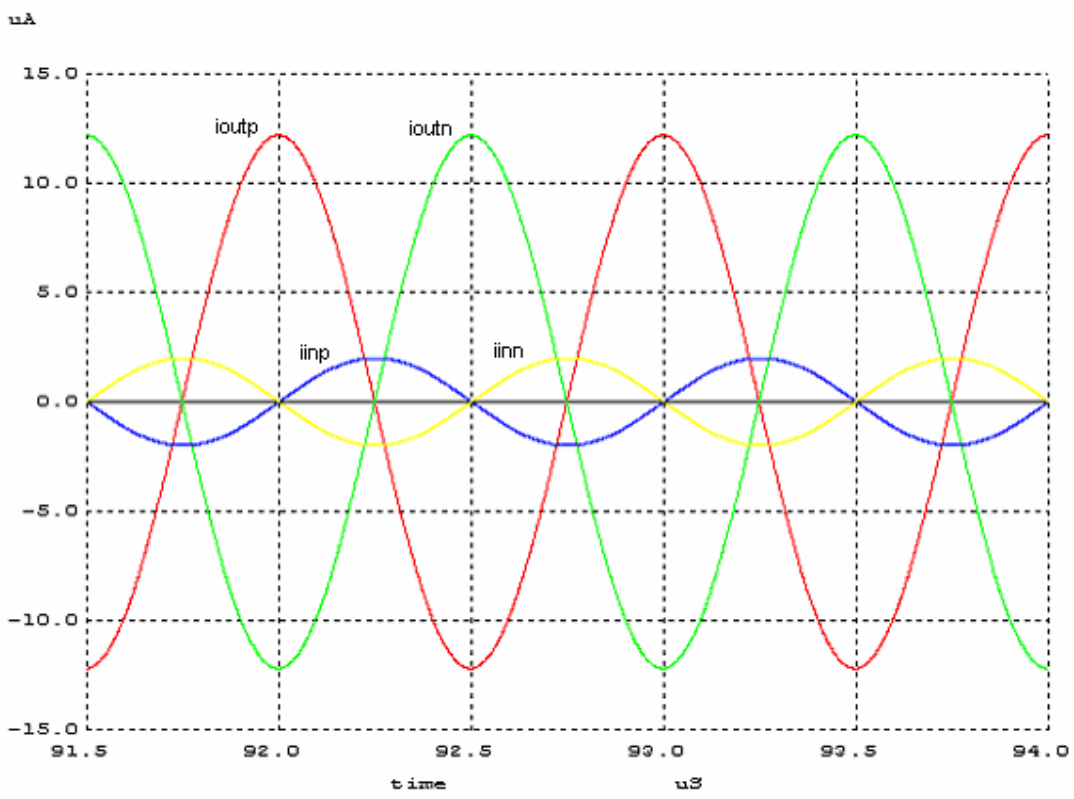

Figure 6.2 Transient response of the current-mode integrator for 2 uA sine input waveforms with 180˚ phase difference

6.2. Current Comparator

As mentioned before, current comparator consist of two parts: curent amplifier and PWL circuit. As a current amplifier, four of current mirror circuits in Figure 3.7 have been cascaded. Gain of each circuit has been picked as three. For amplifier in Figure 3.7, $W_1/L_1 = W_3/L_3$ = 0.7u/0.35u, $W_2/L_2 = W_4/L_4$ = 2.1u/0.35u values have been chosen. For PWL circuit in Figure 3.6, $W_1/L_1 = W_2/L_2 = W_3/L_3$ = 1.4u/0.35u, W_4/L_4 = 0.7u/0.35u, I1 = 10uA, I2 = 20uA, I3 = 5uA have been chosen. DC, AC and transient analysis results are shown in Figure 6.1, 6.2 and 6.3 respectively. In Figure 6.1, $I_{IL} = I_{IH}$ = 400 nA, $I_{OH} = I_{OL}$ = 5 uA and in Figure 6.2, gain = 24.69 dB and cut-off frequency ω_c = 370.4 MHz. For transient analysis, 10 uA sine input signal has been applied.

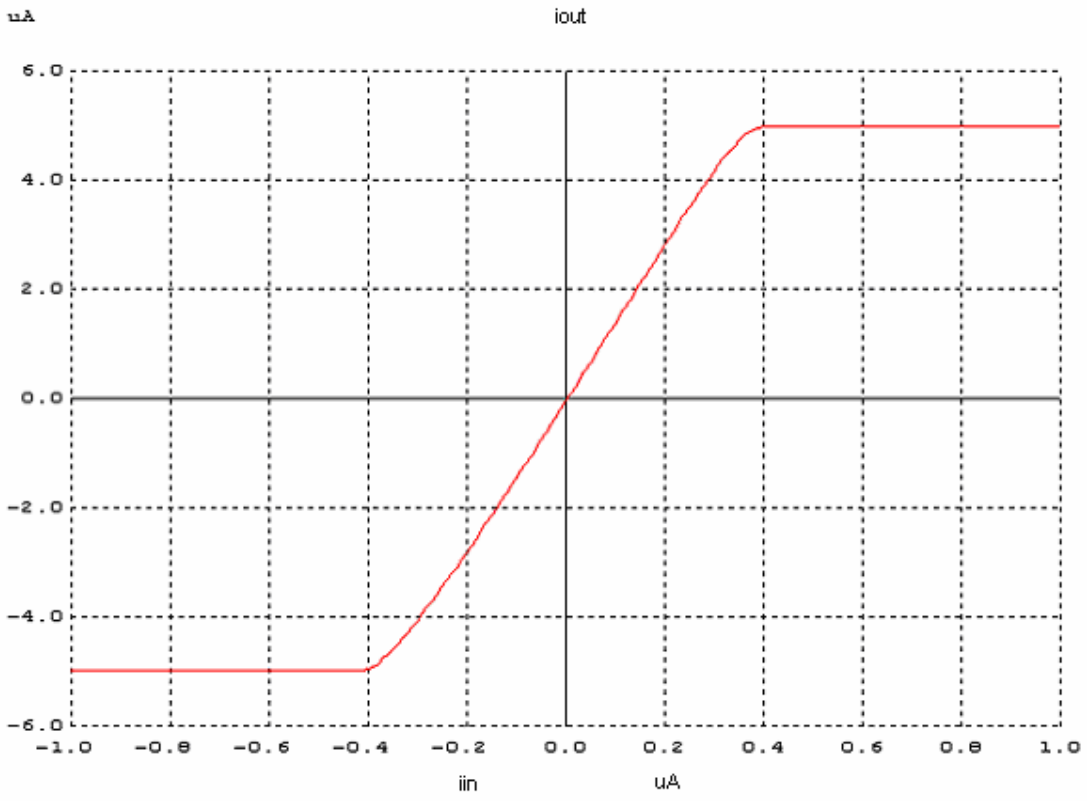

Figure 6.3 Transfer function of current comparator

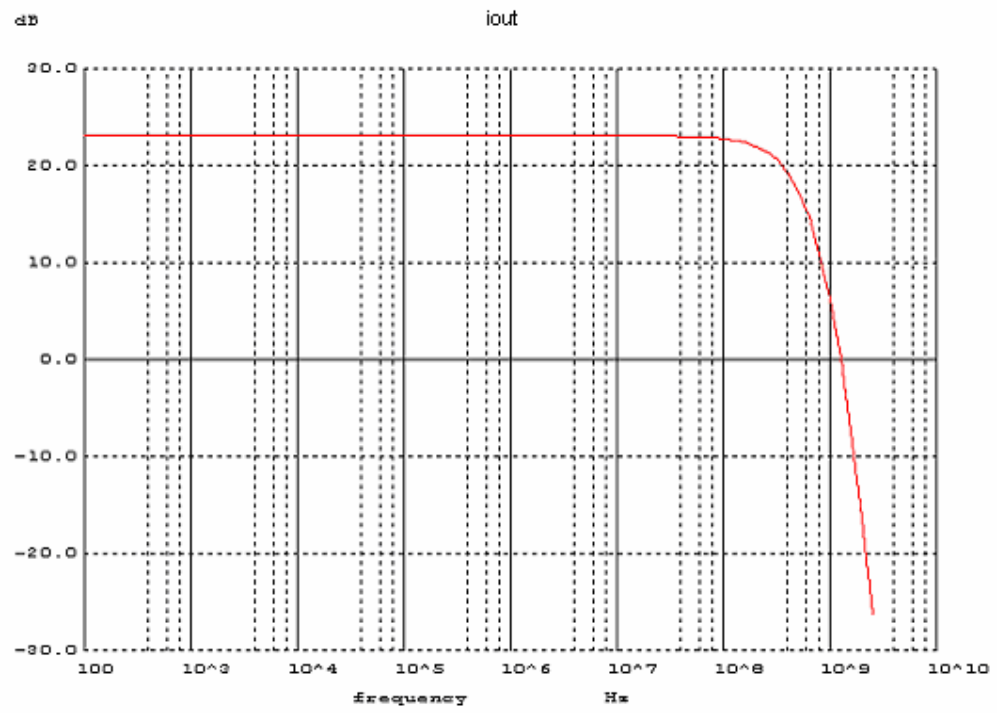

Figure 6.4 Frequency response of current comparator

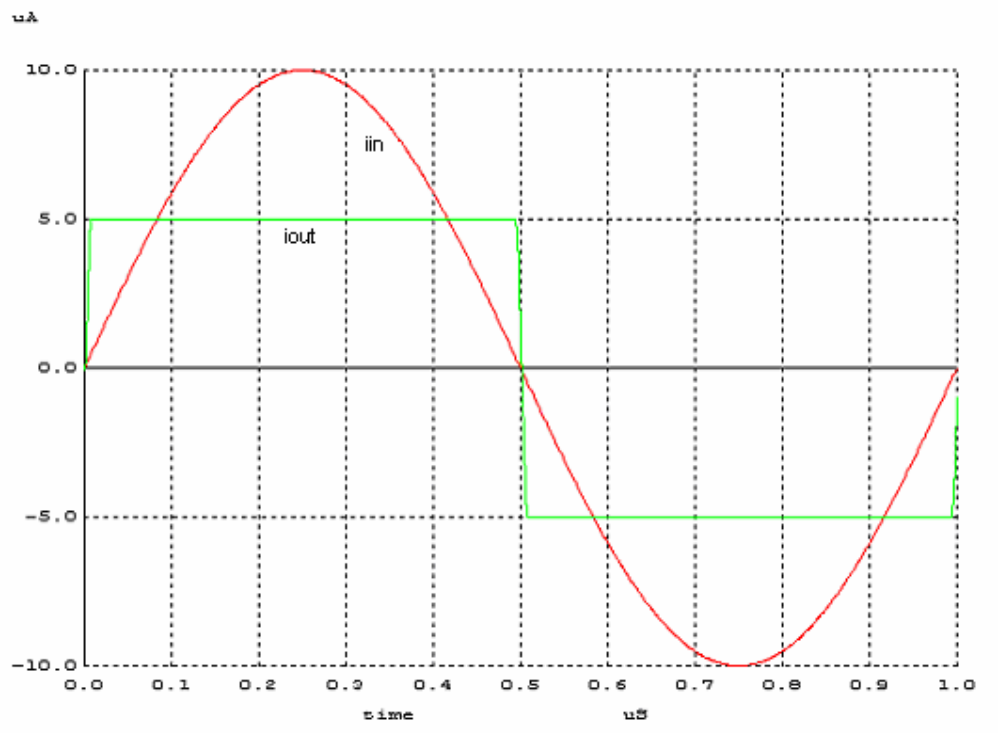

Figure 6.5 Transient response of current comparator for 10 uA sine signal

6.3. Flash ADC

DAC levels for modulator have been constructed via summing the output currents of comparators. Reference currents in quantizer have been chosen between ±30uA with 10uA intervals for a 3-bit modulator. For the circuit in Figure 3.9, $W_1/L_1 = W_2/L_2 = W_3/L_3 = W_4/L_4$ = 0.7u/0.35u, W_5/L_5 = 0.35u/0.35u, W_6/L_6 = 1.05u/0.35u and Ch=200 fF. Since comparator output levels are +/- 5uA, DAC levels are between +/- 35uA with 10 uA intervals. Simulation result is shown in Figure 6.6.

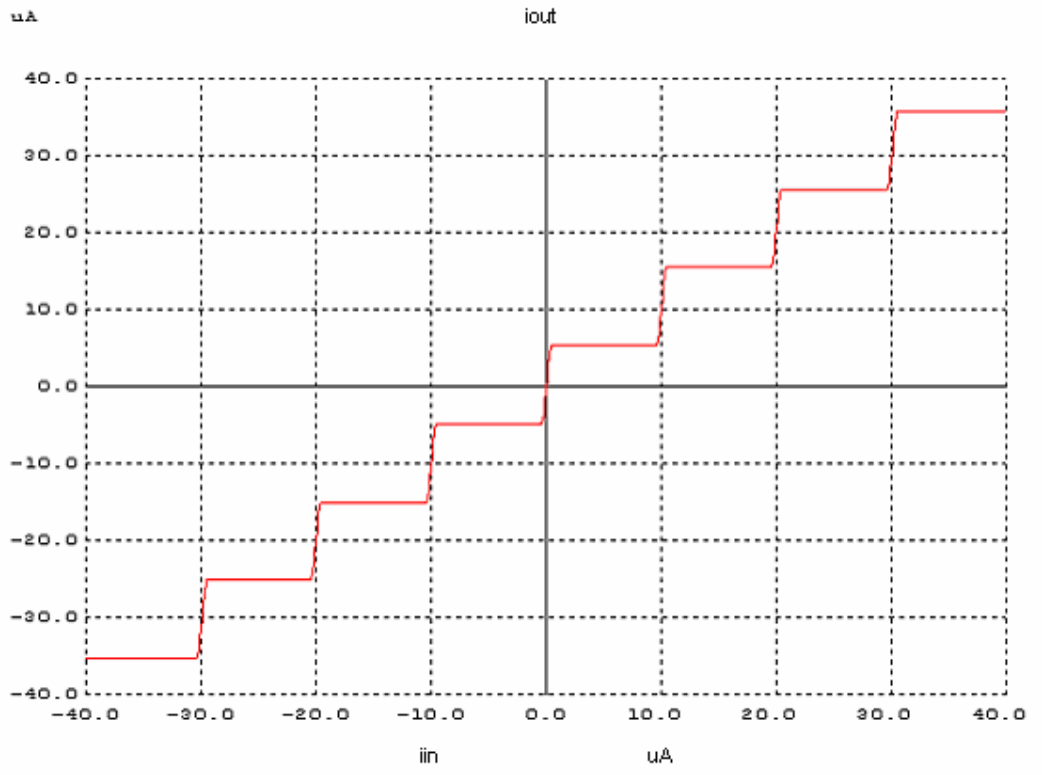

Figure 6.6 DAC levels of Flash ADC

6.4. Differential/Single Converter

For simulation, a differential input sine signal with amplitude 10 uA has been applied. We observe 20 uA difference sine output as it is expected.

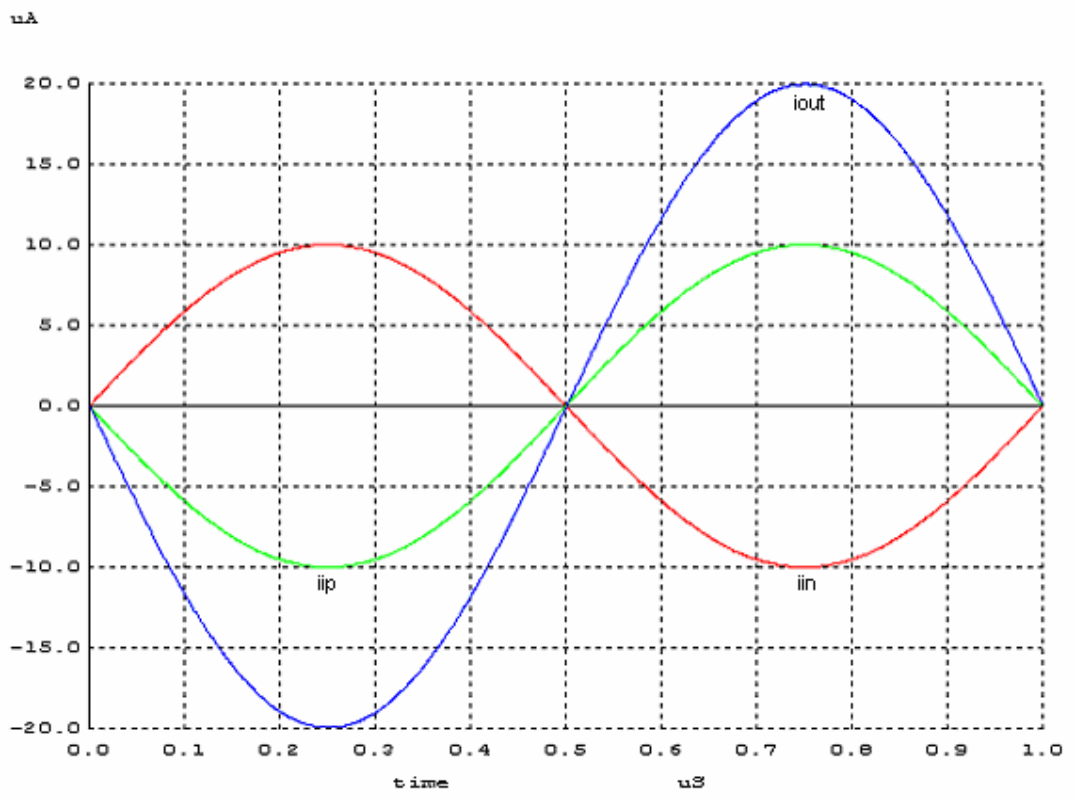

Figure 6.7 Transient response of differential/single converter for a differential input sine signal with amplitude 10 uA

Table 6.2. Transistor dimensions and bias voltages of differential/single converter

Variables	Values
$W_1/L_1=W_2/L_2$	14u/0.35u
$W_3/L_3=W_4/L_4$	4.2u/0.7u
$W_5/L_5=W_6/L_6$	43.05u/0.35u
$W_7/L_7=W_8/L_8$	35u/1.4u
Vbias	1.25 V
Vcp	1.8 V
Vbc	0.8 V

6.5. Modulator

After designing all blocks, we can simulate modulator. Modulator currents to be observed are shown in Figure 5.8. A differential input sine signal with amplitude of 30 uA and frequency of 100 KHz has been applied to the modulator. Clock frequency is 25 MHz.

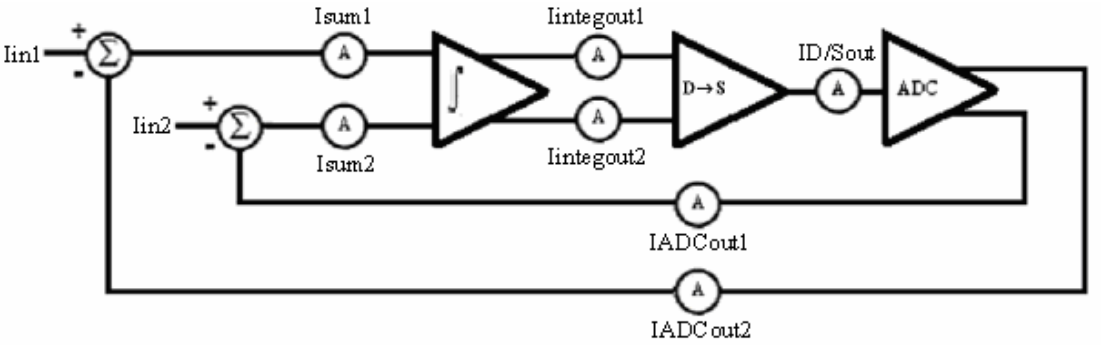

Figure 6.8. Modulator circuit diagram

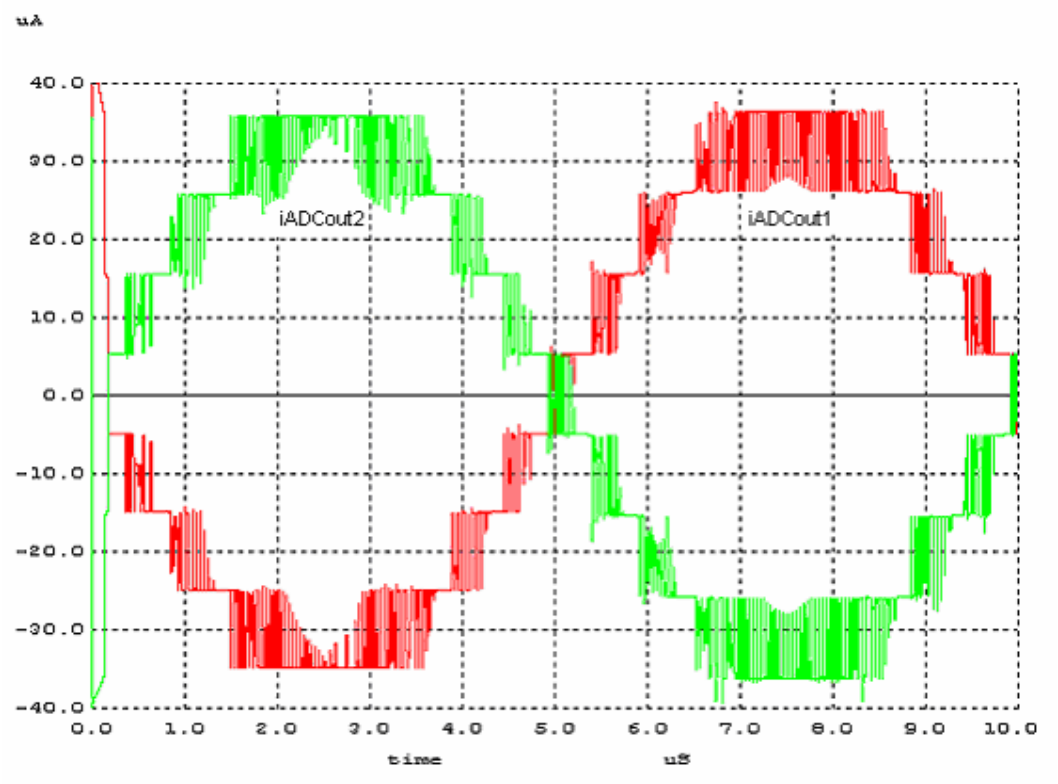

Figure 6.9. ADC output feedback currents

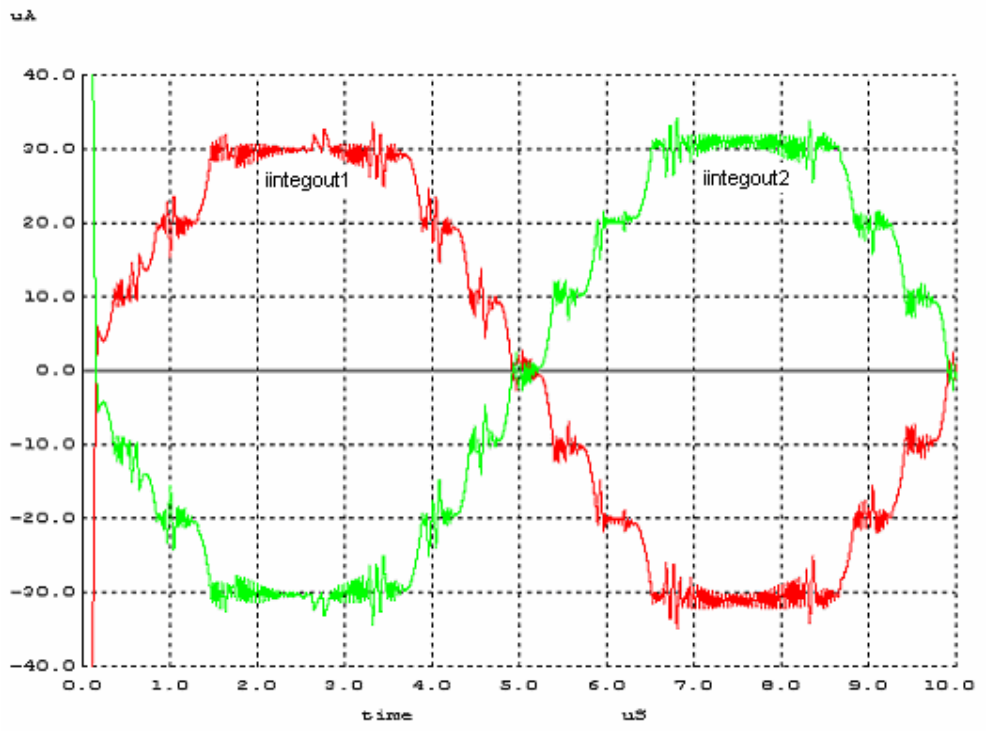

Figure 6.10. Integrator outputs

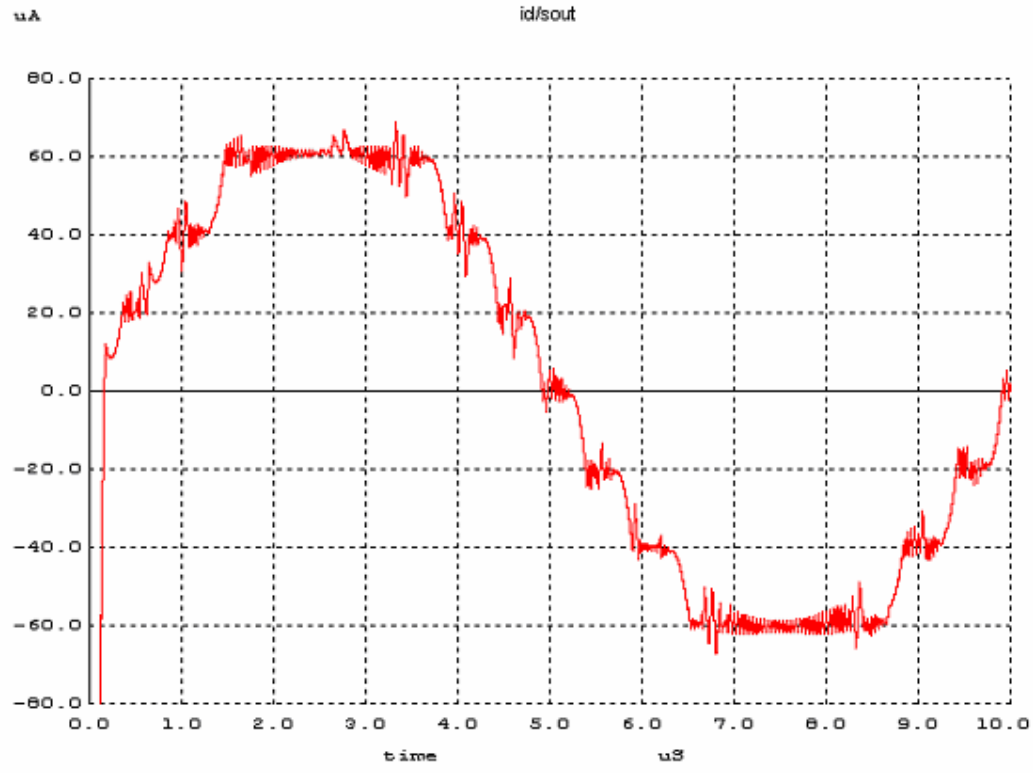

Figure 6.11. Differential/Single converter output

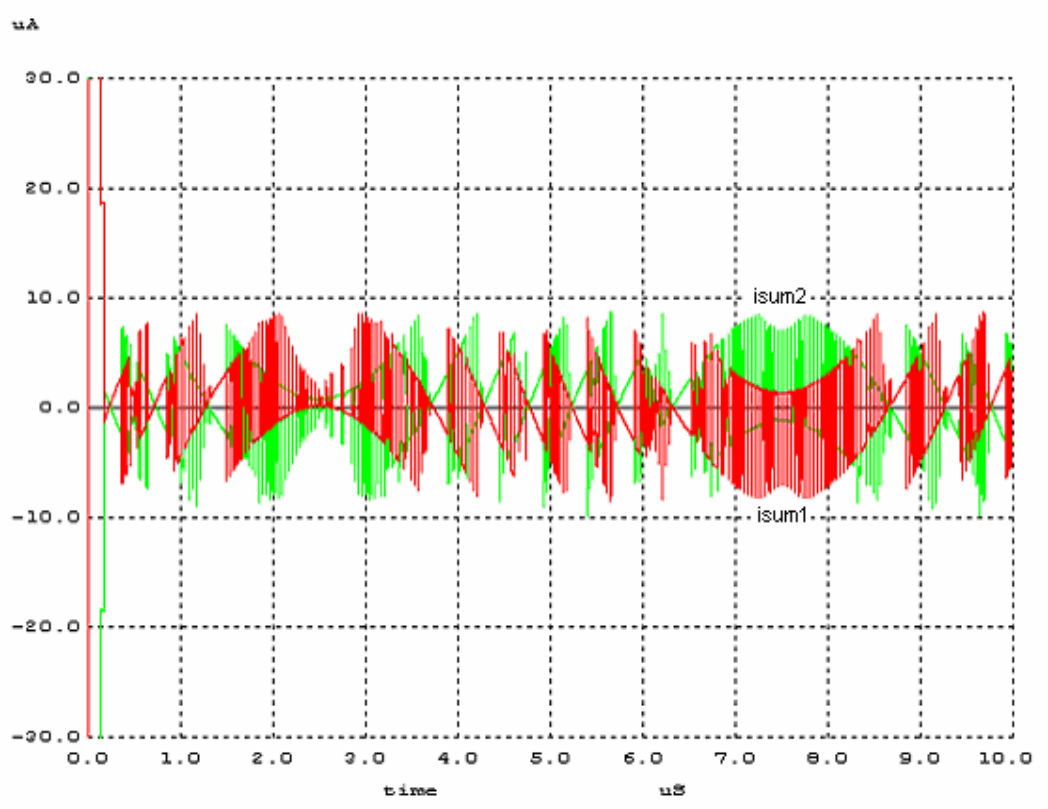

Figure 6.12. Sum currents

6.6. Threshold Detector

In Figure 6.13 transfer function of the threshold detector is depicted. Above 5 uA, output current is 10 uA, otherwise 0. For transient simulation of threshold detector, a square waveform of 100 MHz has been applied as input signal which is varying between 0 and 10 uA. Since threshold current is 5 uA, output current must be same as input current. Simulation result is shown in Figure 6.14.

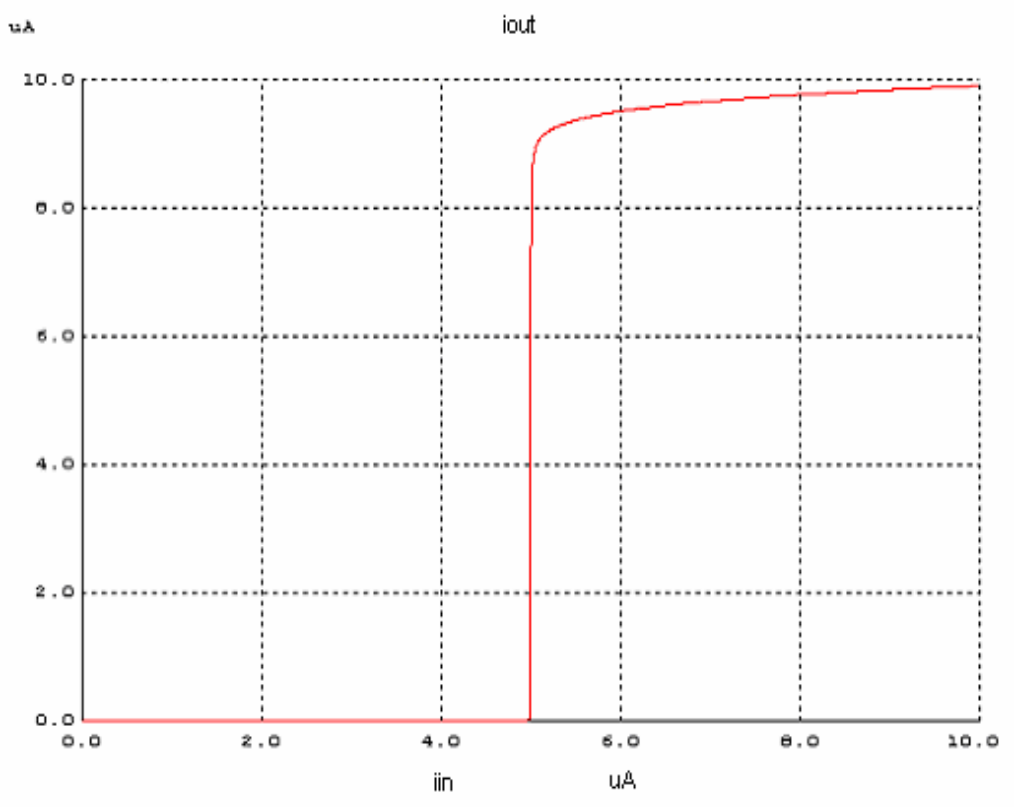

Figure 6.13 Transfer function of threshold detector

Table 6.3. Transistor sizes and bias voltages for threshold detector

Variables	Values
$W_1/L_1, W_4/L_4$	1.05u/0.35u
W_5/L_5	2.1u/1.75u
$W_2/L_2, W_3/L_3, W_6/L_6$	0.35u/0.35u
Vbias	1.134V

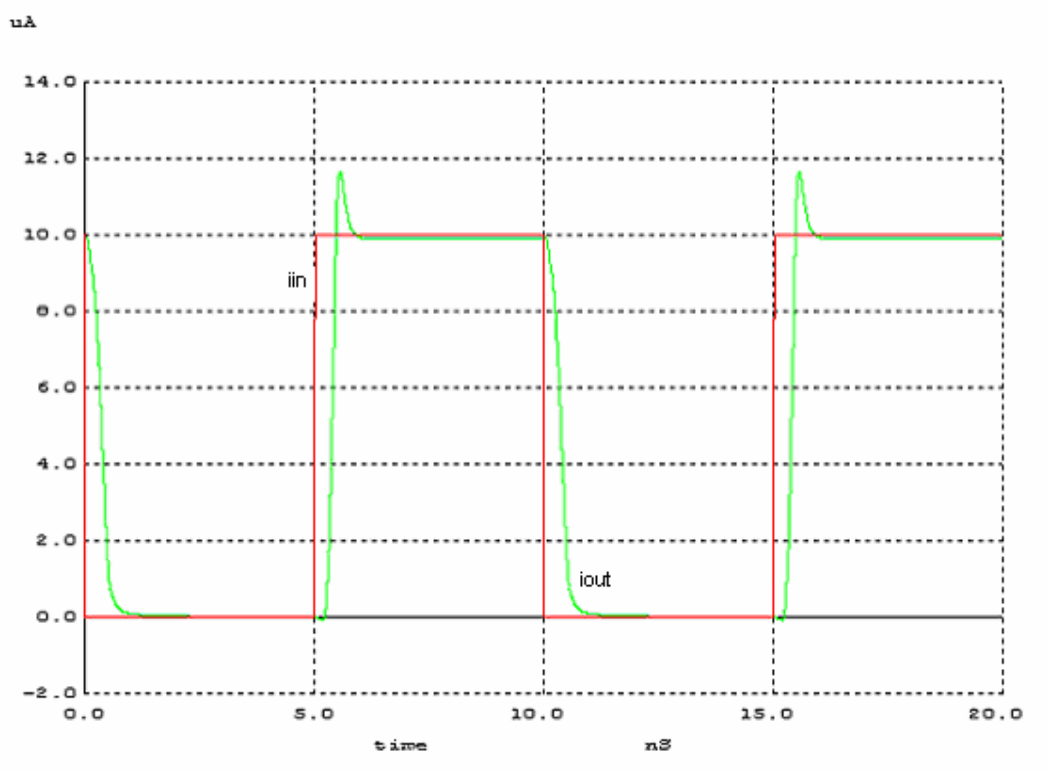

Figure 6.14. Transient response of threshold detector for 100 MHz square wave

6.7. Full Adder

In order to see sum and carry output responses of the full adder, the input signal below has been applied.

$$\mathrm{Iin}(t) = 10\mathrm{uA}.\,u(t - 5\mathrm{ns}) + 20\mathrm{uA}.\,u(t - 10\mathrm{ns}) + 30\mathrm{uA}.\,u(t - 15\mathrm{ns}) \qquad (6.1)$$

Simulation results are shown in Figure 6.15.

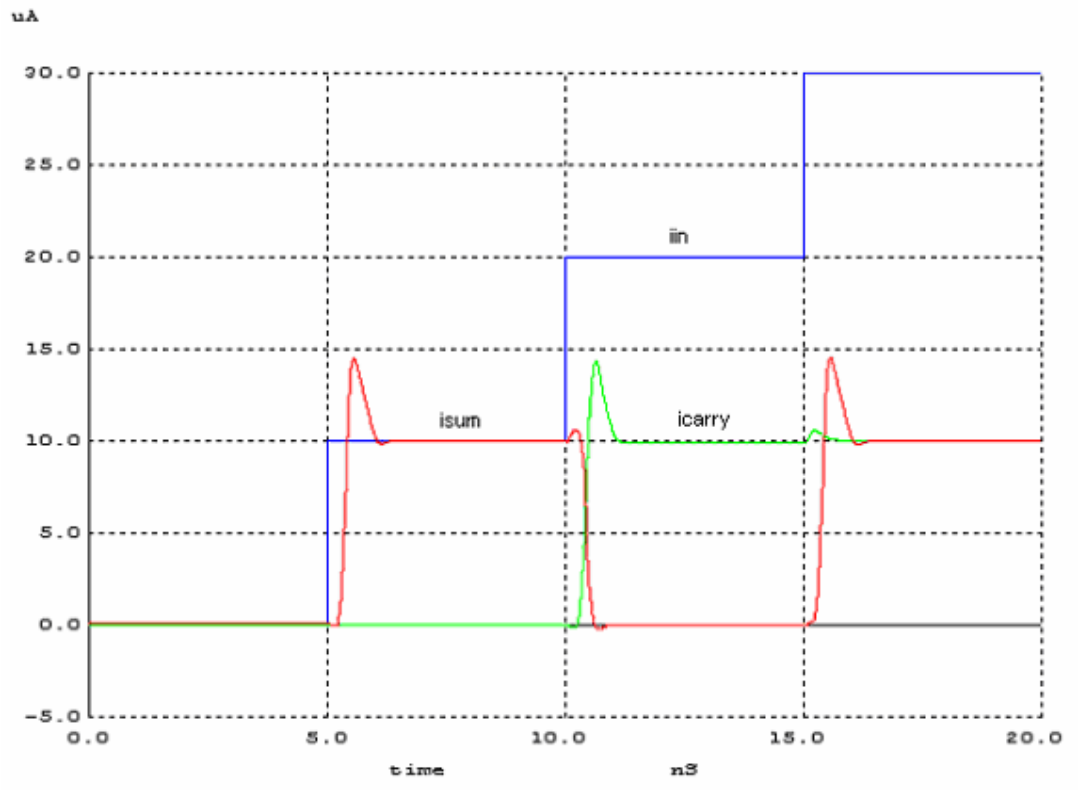

Figure 6.15. Full adder sum and carry outputs for the input current specified in equation 6.1.

6.8. Delay Element

Finally, for delay element, 50 Mhz pulse for input and 100 Mhz clock pulse have been applied. Simulation result is shown Figure 6.16. Output current is one clock cycle shifted as it is expected.

Table 6.4. Transistor sizes and bias voltages for delay element

Variables	Values
$W_1/L_1, W_2/L_2, W_3/L_3, W_6/L_6, W_8/L_8, W_9/L_9, W_{13}/L_{13}$	0.35u/0.35u
W_{12}/L_{12}	2.1u/1.75u
$W_4/L_4, W_{11}/L_{11}$	0.7u/0.35u
$W_5/L_5, W_{10}/L_{10}$	0.35u/0.7u
Vbias	1.134 V

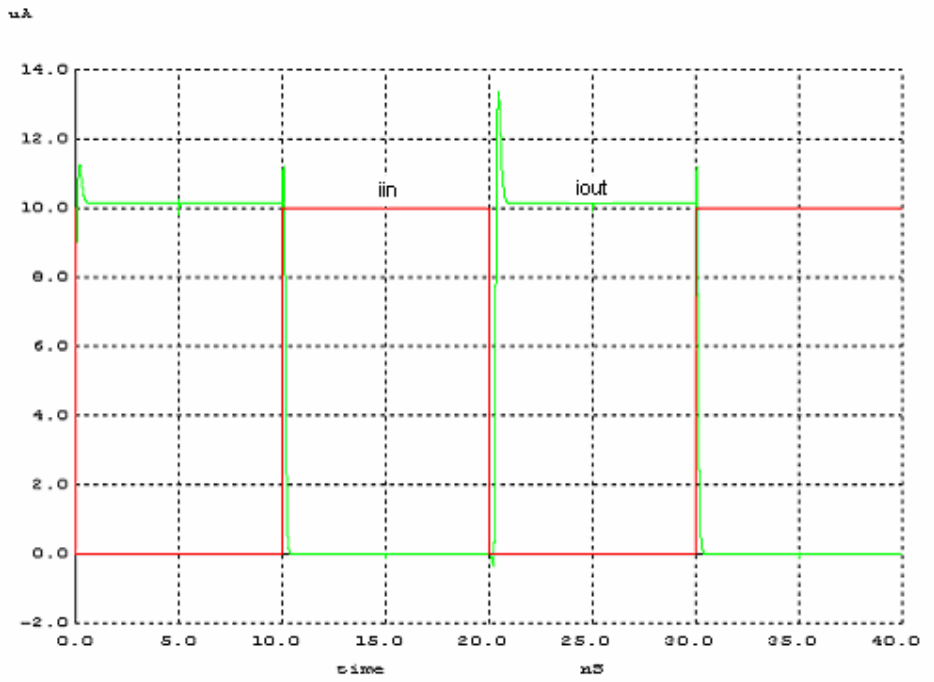

Figure 6.16. Delay element output for 50 MHz input and 100 MHz clock signal

6.9. Digital Integrator

In this section, an one-bit integrator has been simulated for 10 uA dc input current and 100 MHz clock rate. Circuit diagram is shown below. Sum and carry outputs are shown in Figure 6.18 and 6.19.

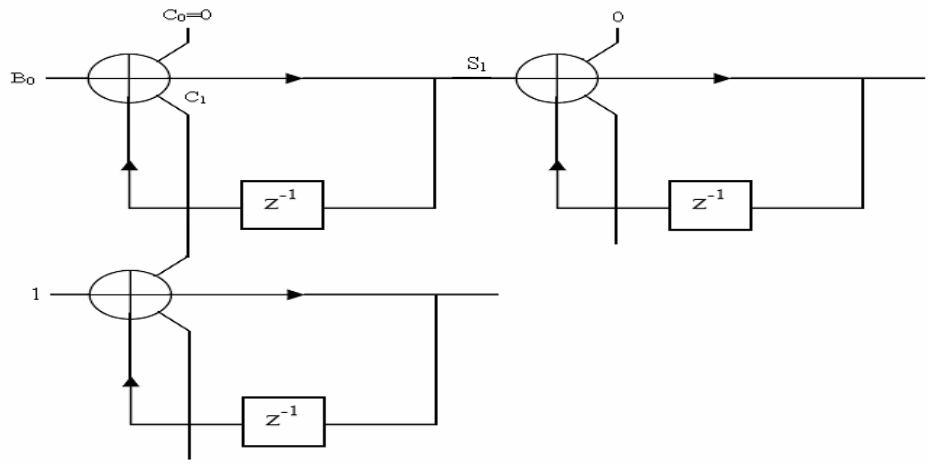

Figure 6.17. Circuit diagram for one-bit integrator simulation

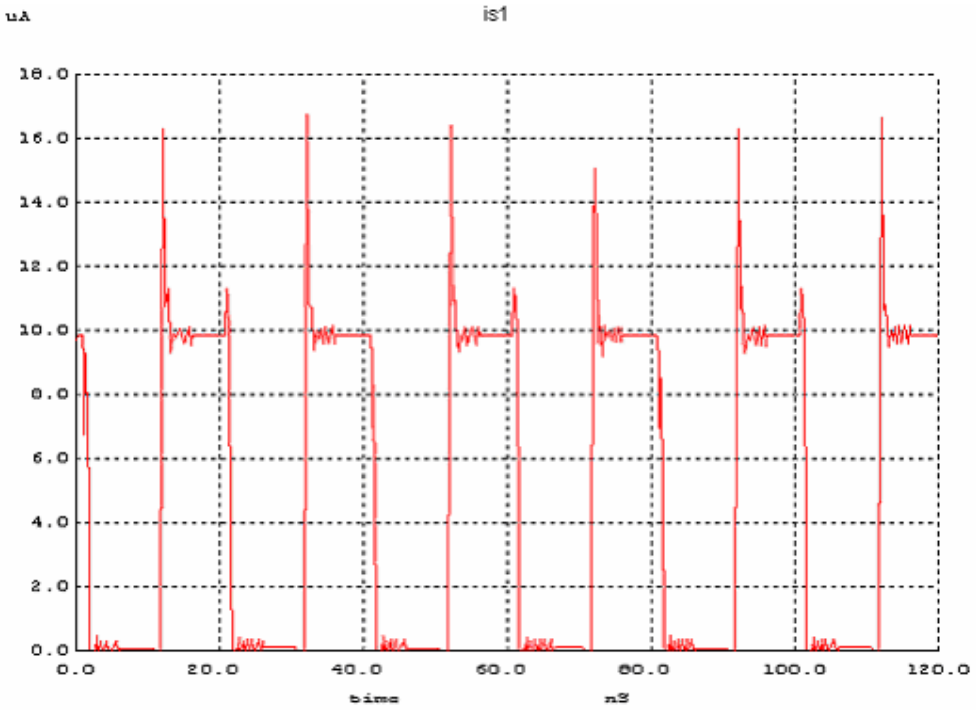

Figure 6.18. Sum output current of a one-bit integrator for 10 uA dc input

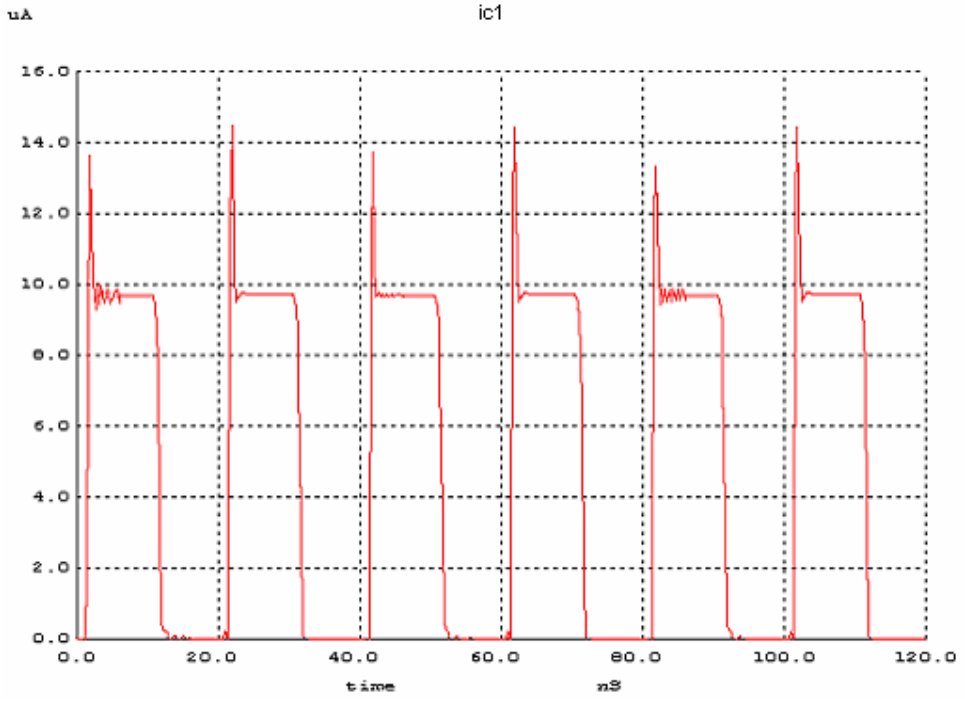

Figure 6.19. Carry output currents of a one-bit integrator for 10 uA dc input

6.10. Modulator with Threshold Detector

As mentioned before, threshold detector can be used as comparator. In this case modulator currents will be as following:

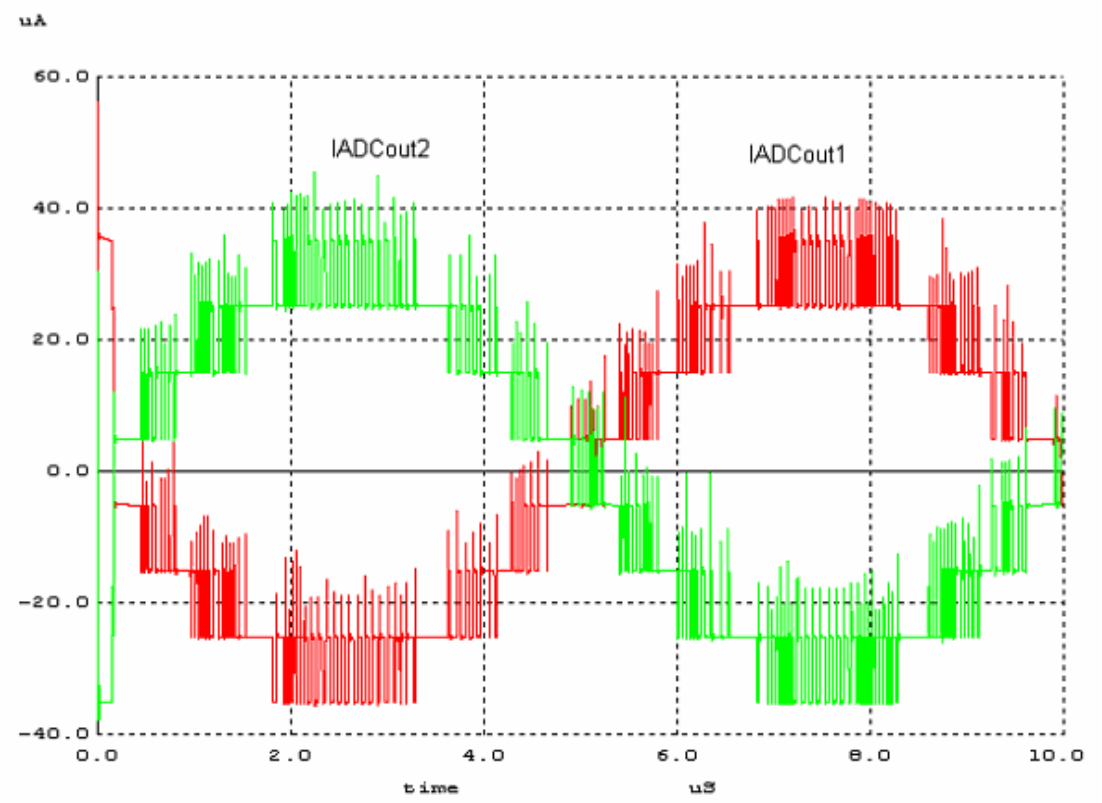

Figure 6.20 ADC output feedback currents

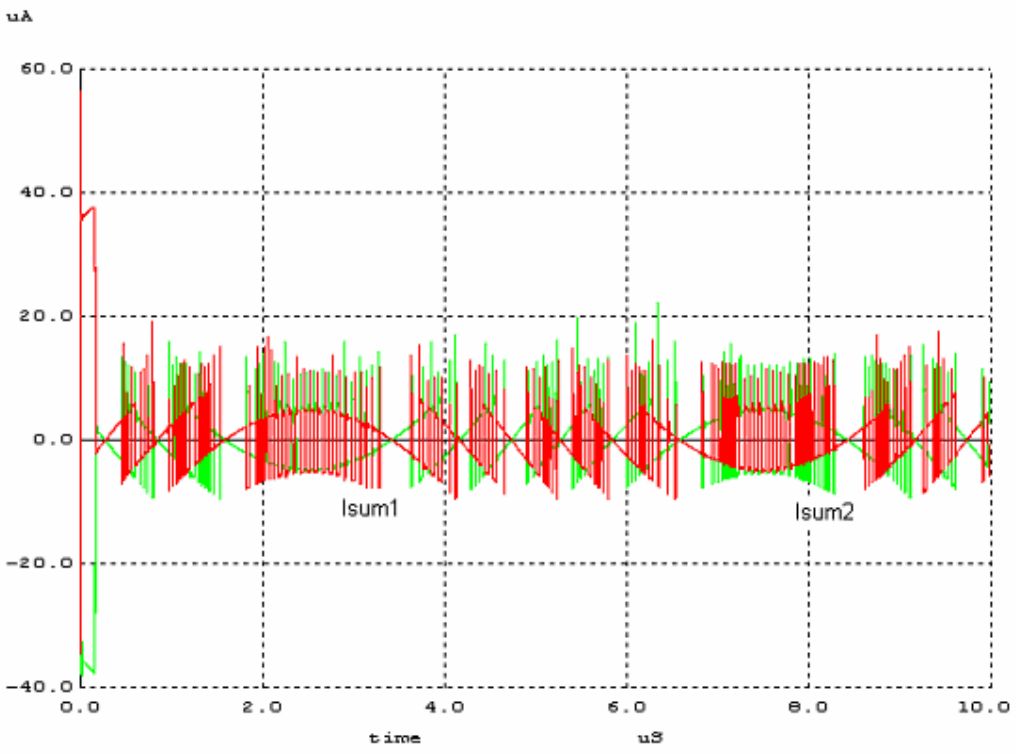

Figure 6.21. Sum currents

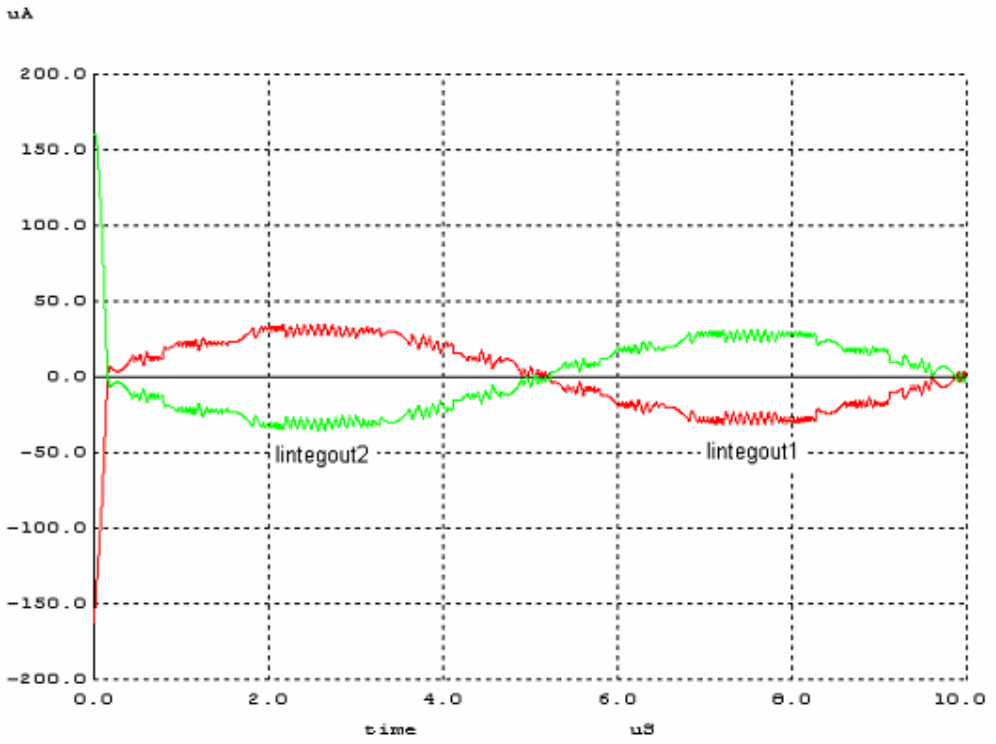

Figure 6.22. Integrator outputs

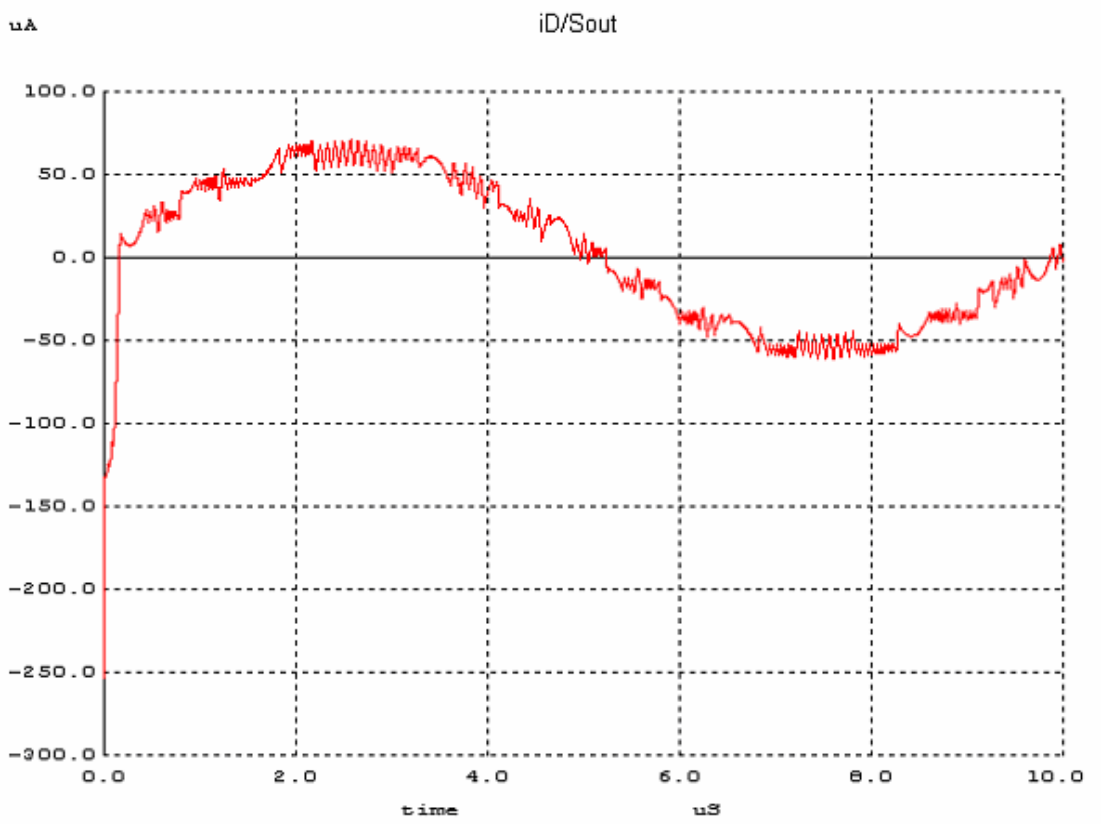

Figure 6.23. Differential/Single converter output

6.11. Power Spectrum Analysis

The best way to see performance of modulator is to look at output spectrum. Figure 6.24 shows the result of power spectrum analysis for the modulator with threshold circuit. According to Figure 6.24, noise shaping is quite well and SNR value at 200 KHz and 300 KHz are 56 dB and 54 dB, respectively. This means that nine-bit resolution can be achieved with this modulator.

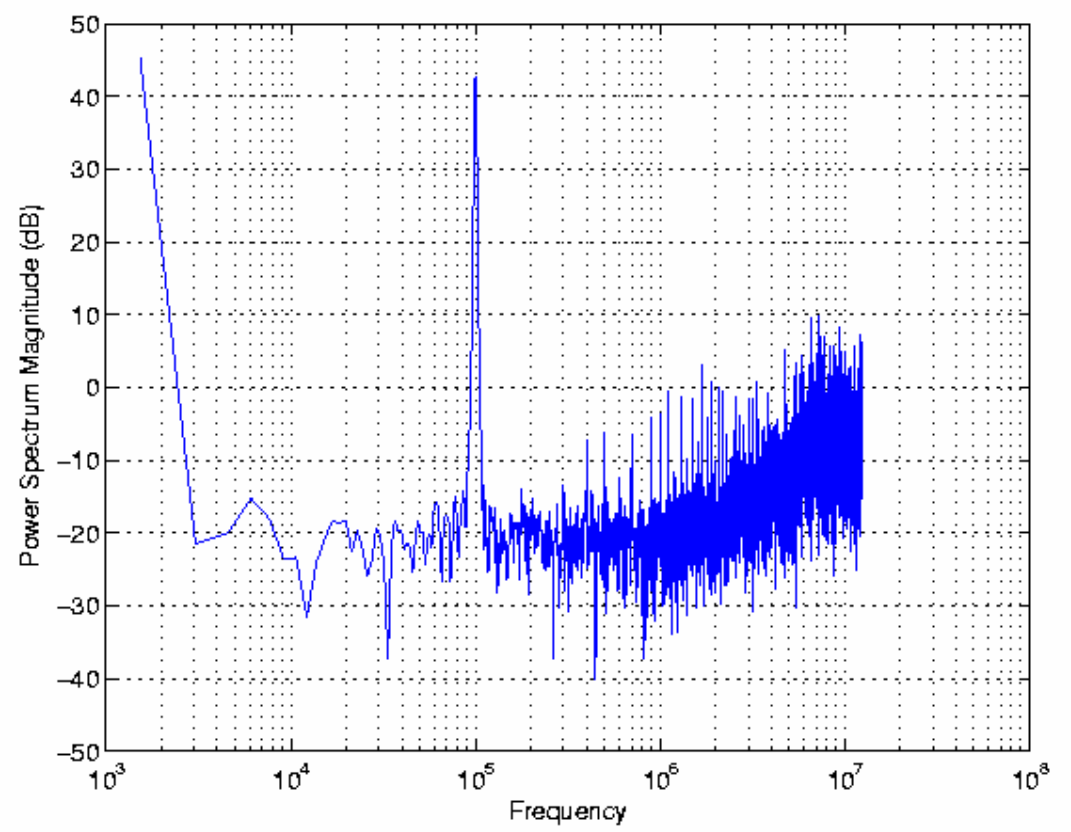

Figure 6.24. Power spectrum analysis of modulator output

6.12. Power Comparison with Voltage-mode Circuit

In order to see superiority of current-mode design over voltage-mode design, we compared current-mode modulator with circuit in [21] in terms of power for same input bandwidth. Results are given below in tabular form.

Table 6.5. Power Consumption of voltage-mode circuit in [21] and current-mode modulator for one clock period

Design Type	Power Consumption (mW)
Voltage Mode	20
Current Mode	6.5

7. CONCLUSION AND FUTURE WORK

Recently, sigma delta modulators have been receiving increased attention as an alternative to other conventional A/D converters. They provide high resolution conversion for low bandwidth signals. Sigma delta modulators are generally realized in DT domain. Due to speed constraints such as maximum clock rate limited by op amp bandwidths, DT modulators do not give good performance for high bandwidths.

In order to overcome clock rate restrictions, CT modulators can be used. Loop filter portion of modulator can be built by continuous-time circuits such as integrators. By CT modulators, high resolution conversion rates can be obtained for wideband signals.

Moreover, current mode design can be an alternative to voltage mode circuits used in modulators. Since current mode circuits have some advantages such as low supply voltage requirement, wide bandwidth, large dynamic range over their voltage mode counterparts, they can be used to achieve high bandwidth and low power conversion.

In this thesis, some current mode circuits used in sigma delta modulators and digital filters such as integrator, comparator, multi-bit ADC, full adder and delay element have been designed. They have been simulated for 0.35u CMOS technology. Simulation results for individual blocks and modulator have been presented.

All the work presented here was for a first order sigma delta modulator. However, higher order modulators are implemented for real applications to achive higher SNR values. As a future work, higher order continuous time current mode sigma delta modulators can be designed.

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