ACCURATE THERMAL CHARACTERIZATION AND OPTIMIZATION OF HIGH LUMEN LED ARRAY FIXTURES

by

Haluk Kundakçıoğlu

B.S., Mechanical Engineering, Yildiz Technical University, 2016

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Master of Science

Graduate Program in Mechanical Engineering
Boğaziçi University

2020

ACKNOWLEDGEMENTS

I want to especially thank my advisor Prof. Nazlı Dönmezer for her help and support throughout my study. It would not be possible to complete my thesis without the guidance of her. I would also like to thank Kunt Atalık and Ahmet Can Erten accepting to be jury members of my thesis regardless of their busy schedule.

I am especially grateful to my friends from Minth Laboratory: İlke Albar, Canberk Dündar, Emine Göktepe, Taher Meydando, and Onurcan Kaya. Also, I sincerely thank my friend Uğur Dinçer and Günay Züngör for their help.

My special thanks go to my family Mehmet, Sermin, Ömer, Gizem, and Selim Kundakçıoğlu for their precious love, supports and inspirations which have made this thesis possible.

And finally, I would like to thank Sırma Karaca, who is always with me and helps me whenever I have a hard time.

ABSTRACT

ACCURATE THERMAL CHARACTERIZATION AND OPTIMIZATION OF HIGH LUMEN LED ARRAY FIXTURES

High lumen light emitting diode (LED) arrays have been preferred in different applications due to their low energy consumption. To maintain the performance of LEDs, heat generated by the LED chips should be removed effectively. Junction temperature can be estimated by thermal models utilizing constant thermal resistances provided in LED datasheets. However, constant thermal resistance used in simulations often neglect the temperature and thickness dependent thermal conductivity of chip layers, which becomes more important at higher temperatures. To include this effect, a multiscale thermal model will be built via COMSOL. First step will include important package features such as LED array and the heat sink and the second step will include the detailed analysis of an LED chip by including temperature and thickness dependent thermal conductivity of chip. The model will be used to analyze junction temperature sensitivity. Today, heat sinks that provide passive thermal management with fin structures are commonly used for effective heat removal from LEDs. Optimization of the heat sink based on thermal needs is crucial for better design of LED arrays. The optimization model will be used to optimize the LED structure by using only three different inputs such as width and length of the fin, and the heat that is desired to spread. And the result of these optimization are applied to the multiscale thermal model to see the real effect of these optimizations on the junction temperature. The results of this study show that the junction temperature values with multiscale model are higher than using constant thermal resistance values from the product datasheet. In addition, to design a high lumen LED array, different priorities can be used according to user demand and different initial LED array designs are obtained from the optimization result.

ÖZET

Yüksek Lümenli LED Armatürlerinin Doğru Isıl Karakterizasyonu ve Optimizasyonu

Yüksek lümenli ışık yayan diyotlar (LED) düşük enerji tüketiminden dolayı tercih edilir. LED ışıkların performansını korumak için LED çipin oluşturduğu ısı, efektif bir şekilde uzaklaştırılmalı ve bağlantı sıcaklığı düşürülmelidir. LED çiplerin bağlantı sıcaklıkları termal model bilgi kitapçıklarından sağlanan sabit termal rezistans kullanılarak tahmin edilebilir. Ancak, simülasyonlarda kullanılan sabit termal rezistans genellikle katmanların sıcaklığa ve kalınlığa bağlı ısıl iletkenlikleri ihmal eder. Bu durum yüksek sıcaklıklarda daha önemlidir. Bu efekti eklemek için iki adımlı ısıl model sonlu eleman metodu ile oluşturulmuştur. İlk adımda LED dizisi ve soğutucu gibi önemli paket özellikleri vardır. İkinci adım ise tek bir LED çipin katmanlarının sıcaklığa ve kalınlığa bağlı ısıl iletkenliklerini dahil eden daha detaylı bir modelini içerir. Model yüksek lümenli LED dizilerinin bağlantı sıcaklıklarını soğutucu optimizasyonu sırasında analiz eder. LED ışıkları efektif bir şekilde soğutmak için genellikle pasif soğutucu olan kanatçık yapıları kullanılır. Daha iyi bir LED tasarımı için ısıl gerekliliklere bağlı olarak soğutucu ve kanatçık optimizasyonu gereklidir. Yüksek lümenli LED yapıları optimizasyonunda kütle, verim ve sıcaklık gibi farklı öncelikler vardır. Optimizasyon modeli bu önceliklere bağlı olarak ve sadece genişlik, uzunluk ve yayılmak istenen ısı miktarı gibi parametrelere göre LED yapılarını optimize eder. Ve bu optimizasyonların birleşme sıcaklığı üzerindeki gerçek etkisini görmek için iki adımlı ısıl model uygulanır. Bu çalışmanın sonuçları, katmanlı modelde elde edilen bağlantı sıcaklığının sabit rezistans değeri kullanılarak hesaplanan sıcaklıktan daha yüksek olduğunu gösterir. Katmanlı ısıl model kullanılarak bağlantı sıcaklığı daha kesin tahmin edilir. Ayrıca, yüksek lümenli LED yapısı tasarlamak için kullanıcı isteğine göre farklı öncelikler kullanılabilir ve başlangıç tasarımı optimizasyon modelinden elde edilir.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS . . . iii
ABSTRACT . . . iv
ÖZET . . . v
LIST OF FIGURES . . . viii
LIST OF TABLES . . . xi
LIST OF SYMBOLS . . . xii
LIST OF ACRONYMS/ABBREVIATIONS . . . xv
1. INTRODUCTION . . . 1
1.1. Light Emitting Diodes (LEDs) . . . 1
1.2. Structure of a GaN LED chip . . . 3
1.3. Thermal Issues of GaN LEDs . . . 6
1.4. High Lumen GaN LED Arrays . . . 10
1.5. Thermal Characterization of LEDs and LED Arrays . . . 11
1.6. Modelling . . . 13
1.7. Thermal Optimization of LED Arrays . . . 15
1.8. Problem Definition and Motivation . . . 17
1.9. Outline of the Thesis . . . 18
2. MULTISCALE THERMAL MODEL FOR HIGH LUMEN LED ARRAY FIXTURES . . . 19
2.1. Package Level Model . . . 20
2.1.1. Validation . . . 23
2.2. Chip Level Model . . . 26
2.3. Results . . . 29
2.3.1. Package Level Model . . . 29
2.3.2. Chip Level Model . . . 31
3. UNIVERSAL OPTIMIZATION MODEL FOR HIGH LUMEN LED ARRAYS 33
3.1. Optimization Algorithm and Correlations . . . 34
3.2. Results . . . 43
4. JUNCTION TEMPERATURE ANALYSIS OF THERMALLY OPTIMIZED

HIGH LUMEN LED ARRAY FIXTURES 51
5. CONCLUSION AND FUTURE WORKS 57
REFERENCES 59

LIST OF FIGURES

Figure 1.1. The first visible LED light 1

Figure 1.2. Circuit and band diagram 2

Figure 1.3. GaN LED chip structure. 3

Figure 1.4. Multiple quantum well (MQW) structure and its band diagram . . 4

Figure 1.5. LED package structure 5

Figure 1.6. CREE XP-G3 Data Sheet 6

Figure 1.7. Thermal path from junction to heat sink 7

Figure 1.8. Thermal resistance value in the product datasheet 8

Figure 1.9. Forward voltage and source current values from product datasheet 8

Figure 1.10. Junction temperature of the GaN LED chip vs. Lifetime 9

Figure 1.11. Luminous flux change with junction temperature 9

Figure 1.12. The longest bridge in Africa with GaN LED lights (Courtesy of Philips) 10

Figure 1.13. High lumen LED array for shipyard and buildings 11

Figure 1.14. (a) Infrared camera result (b) nematic liquid crystal thermal measurement 12

Figure 1.15. Thermal characterization for a single LED chip 14

Figure 1.16. Thermal characterization for a LED array structure 14

Figure 1.17. High lumen GaN based LED array structure 15

Figure 1.18. Fin structure from analytic work 16

Figure 2.1. Temperature distribution in the LED array 19

Figure 2.2. Package level model 20

Figure 2.3. Package level model boundary conditions 22

Figure 2.4. Mesh structure of the package level model 23

Figure 2.5. a) GPRONA simplified model with COMSOL b) Surfaces with convection coefficient 24

Figure 2.6. The location of measured LED chips 25

Figure 2.7. a) CREE XP-E LED chip b) CREE EZ1000-n LED die 26

Figure 2.8. Chip level model structure 27

Figure 2.9. CREE EZ1000 diagram 28

Figure 2.10. Mesh structure of the chip level model 30

Figure 2.11. Temperature distribution of the package level model 30

Figure 2.12. Temperature distribution of the chip level model 31

Figure 3.1. Optimization types 33

Figure 3.2. LED array configuration 34

Figure 3.3. Fin structure 35

Figure 3.4. Optimization algorithm 37

Figure 3.5. Base temperature vs. the heat generation of a single LED chip . . 46

Figure 3.6. Convection coefficient of the fins vs. distance between the LED chips 48

Figure 3.7. Base temperature vs. distance between LED chips 48

Figure 3.8. Base temperature vs. number of LED chip in y direction 49

Figure 3.9. Thermal boundary layer 50

Figure 4.1. Package level model according to optimization result 53

Figure 4.2. Temperature distribution of the solder with minimum temperature optimization 54

Figure 4.3. Solder temperature values along the x axis for minimum temperature optimization 55

LIST OF TABLES

Table 2.1. Convection coefficient values of the package level model. 25

Table 2.2. Solder temperature comparison between experimental and package level model. 25

Table 2.3. Thermal conductivity values of chip and die layers. 29

Table 2.4. Junction temperature in the package and chip level models. 32

Table 3.1. Junction temperature in the package and chip level models. 42

Table 3.2. Optimization results of the initial structure. 44

Table 3.3. Different configurations. 49

Table 4.1. Junction temperature values of the chip level and package level model. 52

Table 4.2. The junction temperature with Multiscale Thermal Model by applying the optimization results. 55

LIST OF SYMBOLS

A_c	Fin area
A_p	Profile area
c_p	Specific heat
c_x	Chip dimension in x direction
c_y	Chip dimension in y direction
d_x	Distance in x direction
d_y	Distance in y direction
El	Elenbaas number
g	Gravity
H	Height
h	Heat transfer coefficient
H_{fin}	Height of fin
$\bar{h}_{wall}$	Convection coefficient of fin walls
$\bar{h}_{fin}$	Heat transfer coefficient of the fin
I_f	Source current
k_{air}	Thermal conductivity of air
k_{fin}	Thermal conductivity of fin
k_{PCB}	Thermal conductivity of PCB
L	Length
m	Performance factor
M_{fin}	Mass of fin
n_{fin}	Number of fins
N_x	Number of LED chips in x direction
N_y	Number of LED chips in y direction
Nu	Nusselt number
P_{th}	Thermal power
Pr	Prandtl number
$Q_{desired}$	Desired heat dissipation

q_f	Heat transfer rate of a single fin
Q_t	Total heat transfer rate
q_w	Heat transfer from wall
R_{bs}	Thermal resistance between the base and the solder
R_{th}	Thermal resistance
R_{thj-s}	Thermal resistance value between junction and solder point
Ra_l	Reynold number based on length
Ra_s	Reynold number based on spacing
S_{fin}	Fin Spacing
S_{opt}	Optimum spacing
t	Thickness
$T_{ambient}$	Ambient temperature
T_{base}	Base temperature
T_{film}	Film temperature
T_j	Junction temperature
T_s	Solder temperature
T_{solder}	Solder temperature
t_{PCB}	Thickness of PCB
T_∞	Ambient temperature
V_{chip}	Volume og the chip
V_f	Forward voltage
V_{fin}	Volume of fin
W	Width

α	Thermal diffusivity
β	Thermal expansion coefficient
ε_{fin}	Effectiveness
η_{fin}	Single fin efficiency
η_{tot}	Total efficiency
θ_b	Temperature difference between the ambient and the base
μ_{air}	dynamic viscosity of air

ν	Kinematic viscosity
ρ_{fin}	density of fin

LIST OF ACRONYMS/ABBREVIATIONS

AlGaN	Aluminum Gallium Nitride
Au	Gold
AuSn	Gold/Tin annoy
GaAs	Gallium Arsenide
GaAsP	Gallium Arsenide Phospate
GaN	Gallium Nitride
GaP	Gallium Phospate
InGaN	Indium Gallium Nitride
IR	Infrared camera
LED	Light emitting diode
LEE	Light extraction efficiency
MQW	Multiple quantum well
PCB	Printed circuit board
RI	Refractive index
Si	Silicon
TEC	Thermoelectric cooler
TIM	Thermal interface material

1. INTRODUCTION

In the 21^{st} century, technology leads us to more practical and comfortable life than we had in the 20^{st} century, but when the technology is developing, energy consumption is increasing. Thus, we have consumed an enormous amount of energy and resources to improve our technology. Lighting has a big part of this consumption. According to the department of energy, lighting consumes 20% of electricity used in the U.S.A. This is a significant amount of energy and it is more than the consumption of computers and other electronics [1]. Therefore, decreasing the lighting energy consumption is an important issue in these days. Light emitting diodes (LEDs) decrease the energy consumption significantly and have been preferred in many lighting applications. Although quite mature, thermal problems of this technology still exist and is still being studied by researchers in the field.

1.1. Light Emitting Diodes (LEDs)

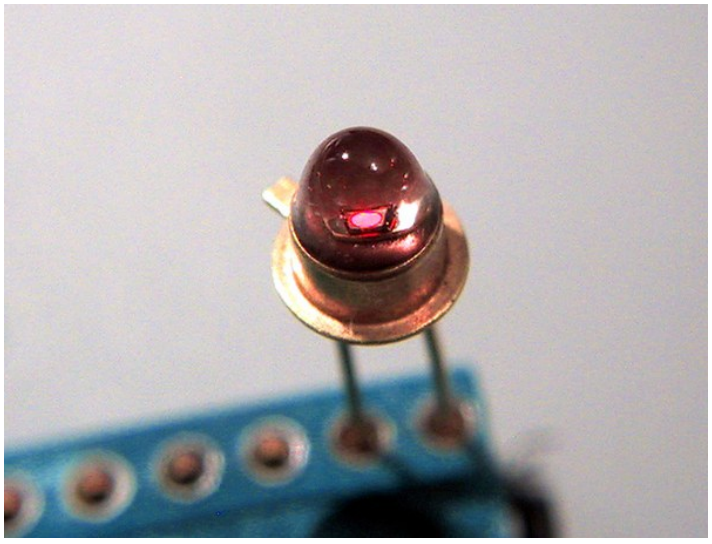


Figure 1.1. The first visible LED light [2]

In 1907, British scientist Henry Joseph Round realized for the first time that the silicon carbide crystals emit light when 10 volts of electrical potential is applied to it. Round called this crystal, “crystal detector” [3]. After this invention, first light emit-

ting diode (LEDs) was invented by Oleg Losev in 1927, yet it did not have a practical design. The first visible-spectrum LED is discovered by Nick Holonyak in 1962 while working at General Electric. He found the first yellow LED and increased the brightness of red LEDs shown in Figure 1.1. Holonyak reported his study in the Journal Applied Physics Letters [4]. Light emitting diodes (LEDs) are semiconductor devices that generate light via electroluminescence created by the electric current passing across the junction of a semiconductor chip [5]. To create a positive-negative or p-n junction to assist electroluminescence, these materials are doped or impregnated with impurities. Impregnated semiconducting material can be p-type or n-type. N-type semiconductor, also known as the cathode, has excess electrons and p-type semiconductor has deficiencies of valence electrons called holes acting as positive charge carriers. In n-type materials free electrons move from a negatively to positively charged area whereas in p-type materials electrons jump from one hole another causing positive charge movement in opposing direction. LED works only in forward voltage condition. When LED

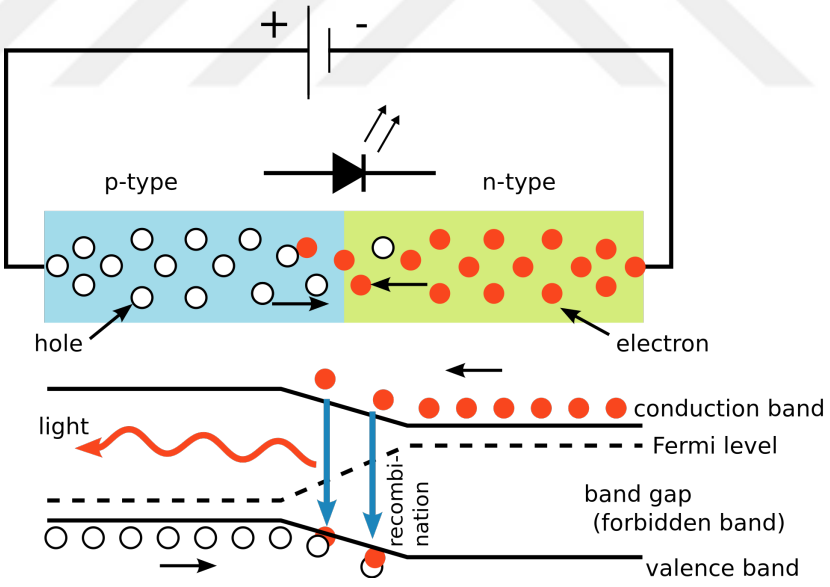


Figure 1.2. Circuit and band diagram [6]

is forward biased, the free electrons from n-type and the holes from p-type are pushed towards the junction point as shown in Figure 1.2 [3]. When free electrons reach the junction or depletion region, some of the free electrons recombine with the holes in the positive ions. In a similar way, holes from p-side recombine with electrons in the

depletion region [7]. Because of the recombination of free electrons and holes in the depletion region, the width of depletion region decreases. As a result, more charge carriers cross the p-n junction. Some of the charge carriers from p-side and n-side will cross the p-n junction before they recombine in the depletion region. Thus, recombination takes place in depletion region as well as in p-type and n-type semiconductor. The free electrons in the conduction band releases energy in the form of light before they recombine with holes in the valence band. In silicon and germanium diodes, most of the energy is released in the form of heat and emitted light is too small. However, in materials like gallium arsenide and gallium phosphide the emitted photons have sufficient energy to produce intense visible light [1]. Gallium Phospate (GaP), Gallium Arsenide (GaAs), and Gallium Arsenide Phospate (GaAsP) are examples of semiconductor materials used in LEDs [7]. Recently, Gallium Nitride (GaN) is also preferred due to its direct band gap energy and stronger chemical bonds. While direct band gap energy covers the spectra from ultraviolet to the entire visible spectrum, stronger chemical bonds makes the nitride very stable and resistant to degradation under strong electric current and high temperature [8].

1.2. Structure of a GaN LED chip

Gallium Nitride (GaN) is preferred due to its direct band gap energy and strong chemical bonds. While direct band gap energy covers the spectra from ultraviolet to

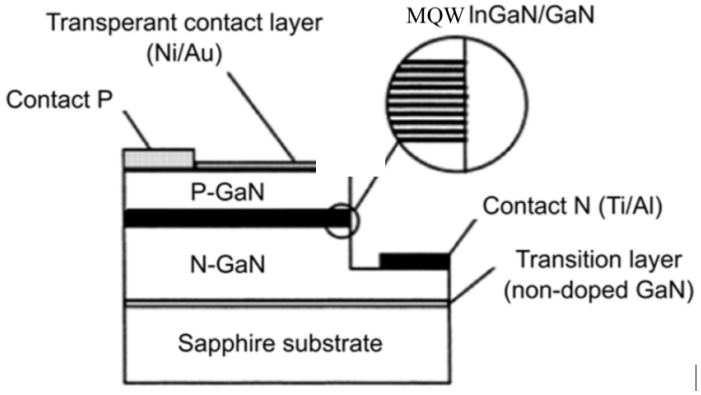


Figure 1.3. GaN LED chip structure [9]

the entire visible spectrum, stronger chemical bonds makes the nitride very stable and resistant to degradation under strong electric current and high temperature [8].GaN-based LEDs often come in special packages as shown in the Figure 1.5. Chip is the most important part of this package structure. N-type and P-type semiconductors are located in this component and light is generated at this region. The rest of the package may have variety of purposes such as protection, color selection, focusing, electrical interconnection, heat dissipation, mechanical strength, and reliability [10]. GaN LED chip structure is shown in the Figure 1.3. Contact P layer is a layer that is used for wire connection and it is a very thin layer consisting of Au or Ni. The N contact is used in wire connection and it is composed of Al and Ti layers. P-GaN is generally doped with Magnesium (Mg) and it is used as p-type semiconductor as shown in the Figure 1.2. N-GaN is generally doped with Silicon (Si) and it is used as n-type semiconductor. Transition layer with undoped GaN is located under the N-GaN layer. Sapphire substrate is located at the bottom of the structure and it is used as an electrical instructor. Finally, there is an active region between p type

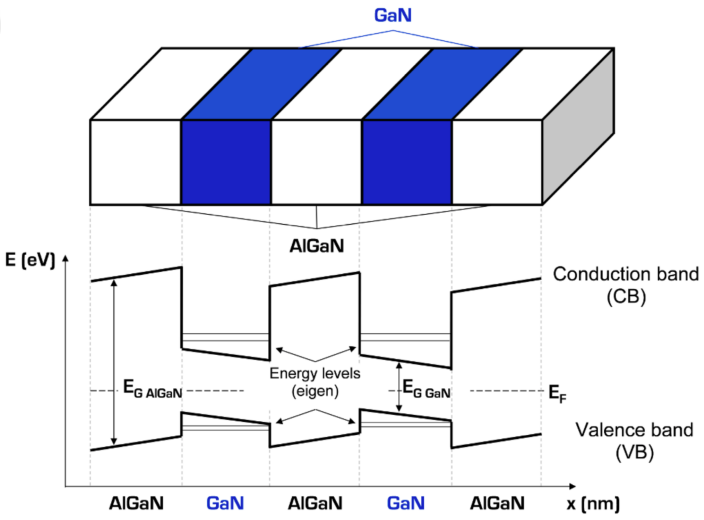


Figure 1.4. Multiple quantum well (MQW) structure and its band diagram [9]

and n type GaN. The active region consists of AlGaN/GaN or InGaN/GaN structures as shown in the Figure 1.4. The InGaN or AlGaN region is known as the bandgap and the GaN region creates the potential well which is created by the epitaxy of p type and n type materials. The transportation of the electrons is done with electrons

and holes. By using quantum wells, electron transition is promoted [9]. Generally, a LED package, similar to one illustrated in Figure 1.5, contains a substrate member with electrical wires which apply the electrical current to the LED chip [1]. In addition to the substrate, LED includes a lens positioned for receiving and emitting the generated light. The lens is generally attached to the LED by the use of an encapsulant. Encapsulants are commonly made of epoxy and silicone. Epoxy provides transparency and does not deteriorate at high temperatures. On the other hand, silicone is a thermally stable and flexible material thereby it reduces the mechanical and thermal stresses on the chip [3].

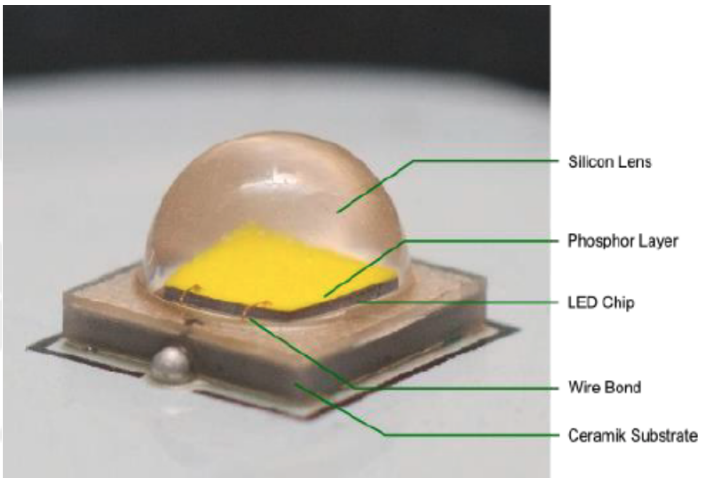


Figure 1.5. LED package structure [11]

Encapsulants not only provide mechanical and chemical protection increase the light extraction efficiency (LEE) by reducing the refractive index (RI) in LEDs [12]. Finally, LED package has a phosphor layer which is a substance that displays the property of luminescence. The phosphor is a solid material which emits visible light when exposed to radiation from a deep blue, ultra-violet, and electron beam source [13]. Through careful tuning of the phosphor composition and structure, the spectral content of the emitted light can be tailored to meet certain performance criteria. For example, GaN LEDs emits blue light. White LEDs are created by incorporating a layer of phosphor over the GaN-based blue emitter [14]. Shape, structure, luminous flux, and encapsulant material of commercial LED packages might differ from each other and different LED packages can be preferred for different applications. Data sheets published by top LED production companies such as Samsung and CREE mark those

differences, as shown in Figure 1.6 [15].



CREE

PRODUCT FAMILY DATA SHEET

Cree® XLamp® XP-G3 LEDs

XP-G3 White

XP-G3 Royal Blue

XP-G3 Photo Red

PRODUCT DESCRIPTION

XLamp® XP-G3 LEDs are optimized for directional, high-lumen lighting applications where efficacy and optical control are critical, such as roadway, portable and horticulture. The compact and proven 3.45-mm XP platform has an excellent ecosystem of optics and system solutions available, enabling lighting manufacturers to simplify their design process and shorten time-to-market.

XP-G3 LEDs are available in royal blue, photo red and two different white versions. White (Standard) delivers best-in-class TM-21 lifetimes and color stability over time. White (S Line) improves on the Standard version: better system-level reliability through switching and dimming cycles, improved resistance to sulfur exposure and higher efficacy. With this S Line version, Cree delivers high-power LED technology that is optimized for robust lighting applications where sensors and the internet-of-things (IOT) are becoming common.

FEATURES

- Available in no CRI minimum white, 70-, 80- and 90-CRI white, royal blue & photo red
- ANSI-compatible chromaticity bins
- 3-step and 5-step options
- White binned at 85 °C, royal blue & photo red binned at 25 °C
- Maximum drive current: white, royal blue: 2000 mA, photo red: 1500 mA
- Low thermal resistance: white: 3 °C/W, royal blue: 2 °C/W, photo red: 2.5 °C/W
- Wide viewing angle: 125°–130°
- Unlimited floor life at ≤ 30 °C/85% RH
- Reflow solderable - JEDEC J-STD-020C
- Electrically neutral thermal path
- RoHS and REACh compliant
- UL® recognized component (E349212)

Figure 1.6. CREE XP-G3 Data Sheet [15]

1.3. Thermal Issues of GaN LEDs

GaN based Light-Emitting Diode has some advantages such as lifetime, cost, efficiency, color variation, size, and on-off time. For example, while the lifetime of incandescent lamps and fluorescent lamps are between 1000-2000 hours and 10000-15000 hours respectively, lifetime of the LED lights is varying between 35000-50000 hours. Also, LEDs provide more light output per watt than incandescent lamps. The efficiency does not depend on the shape and size of the lamp, as in fluorescent lamp. Another feature is the color variation; which allows creation of different colors by the variation of forward current. It also has a very small structure and therefore can be used in many applications easily. In addition to these features, GaN LEDs can reach maximum brightness below a microsecond, thus their on-off time are short [3].

Although LEDs have many preferable features, they have thermal problems. While GaN based LEDs produce light using electrical energy, they also generate heat. Around 80% - 90% of the electrical energy is generally converted into heat [16]. Considering the power of modern LED systems like GaN-based LED systems, which is about P = 0.3 - 5 W and the small size of LED chips, heat flux of a single LED chip may reach 100-125 W/cm^2 which will result in high chip temperatures [17]. To define the temperature of the chip, junction temperature (T_j) is used. Junction temperature is the temperature of the hottest region inside the chip. This region is located between p-type and n-type semiconductors, i.e. p-n junction, where recombination occurs as shown in Figure 1.2.

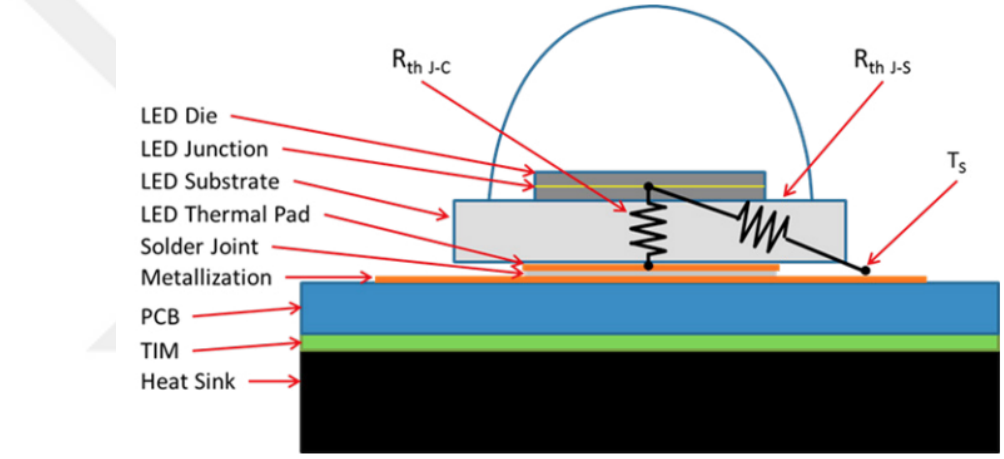
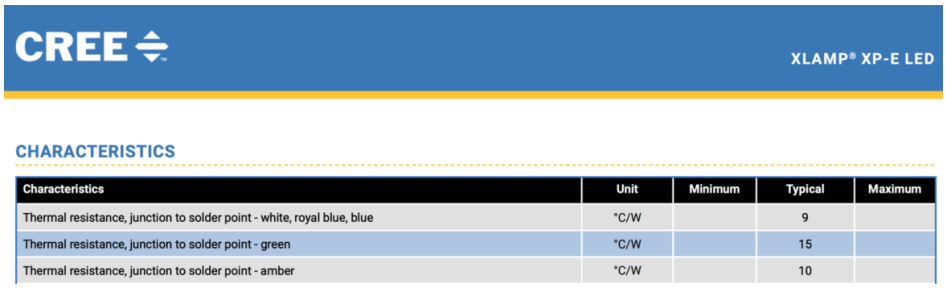


Figure 1.7. Thermal path from junction to heat sink [18]

Thermal resistance path as shown in the Figure 1.7 is used in order to estimate the junction temperature of the LED chip. From the solder temperature, junction temperature is found with following equation:

$$T_j = T_s + R_{th\ j-s} \times \ P_{th} \tag{1.1}$$

where T_j is junction temperature, T_s is solder temperature, R_{thj-s} is thermal resistance value between junction to solder point, and P_{th} is the thermal power. Thermal resistance value (R_{thj-s}) is given in the product datasheet as shown in the Figure 1.8 and it shows that the temperature difference between the junction and solder for 1W power.



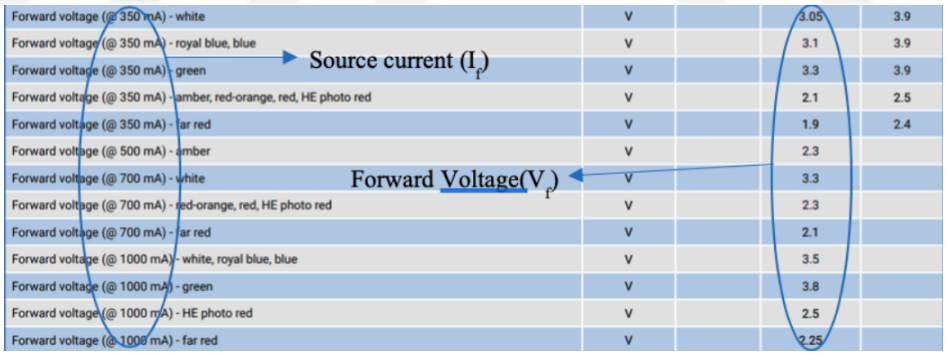
Characteristics	Unit	Minimum	Typical	Maximum
Thermal resistance, junction to solder point - white, royal blue, blue	°C/W		9	
Thermal resistance, junction to solder point - green	°C/W		15	
Thermal resistance, junction to solder point - amber	°C/W		10	

Figure 1.8. Thermal resistance value in the product datasheet [19]

Thermal power depends on the LED chip's feature. It is calculated with the following equation [20]:

$$P_{th} = 0.75 \times V_f \times I_f \tag{1.2}$$

where V_f is forward voltage and I_f is source current which are known from product datasheet as shown in the Figure 1.9.



Forward voltage (@ 350 mA) - white	V		3.05	3.9
Forward voltage (@ 350 mA) - royal blue, blue	V		3.1	3.9
Forward voltage (@ 350 mA) - green	V		3.3	3.9
Forward voltage (@ 350 mA) - amber, red-orange, red, HE photo red	V		2.1	2.5
Forward voltage (@ 350 mA) - far red	V		1.9	2.4
Forward voltage (@ 500 mA) - amber	V		2.3	
Forward voltage (@ 700 mA) - white	V		3.3	
Forward voltage (@ 700 mA) - red-orange, red, HE photo red	V		2.3	
Forward voltage (@ 700 mA) - far red	V		2.1	
Forward voltage (@ 1000 mA) - white, royal blue, blue	V		3.5	
Forward voltage (@ 1000 mA) - green	V		3.8	
Forward voltage (@ 1000 mA) - HE photo red	V		2.5	
Forward voltage (@ 1000 mA) - far red	V		2.25	

Figure 1.9. Forward voltage and source current values from product datasheet [19]

High temperature affects the LED chip negatively because the maximum light output, quality, reliability, and the lifetime of LEDs are mainly related to the junction temperature which restricts the LED light source's performance [16]. It has been shown that the lifetime of a GaN-based LED chip decreases with increasing the junction temperature as can be seen in Figure 10 [21].

After a certain junction temperature, LED will fail. For 1.5 A LED, a temperature increase of 30 °C decreases the life of a LED 50000 hours as can be seen in Figure 1.10.

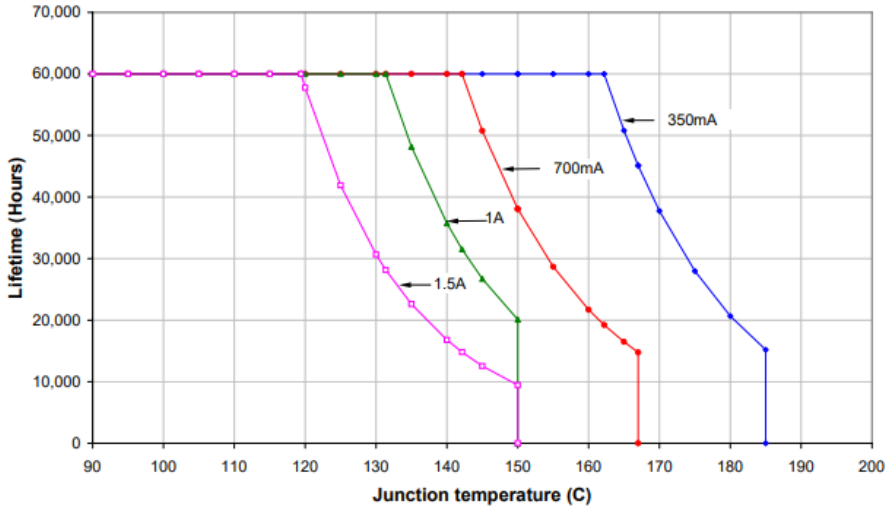


Figure 1.10. Junction temperature of the GaN LED chip vs. Lifetime [22]

In addition to lifetime relative luminous flux is also affected negatively from the high junction temperatures as shown in Figure 1.11. As the junction temperature increases, the light output of the GaN-based LED chip decrease but recovers when the LED cools. Relative flux is based on 100% light output at a 75 °C junction temperature.

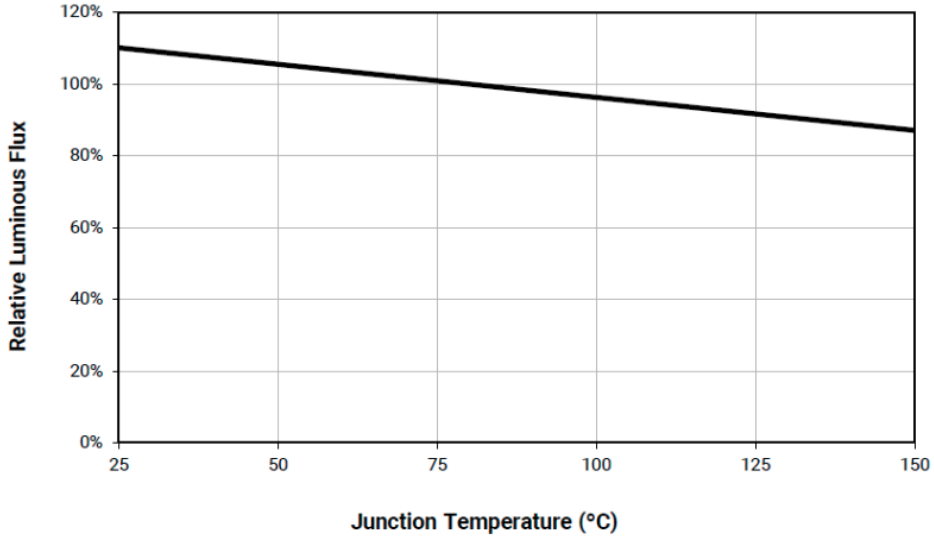


Figure 1.11. Luminous flux change with junction temperature [15]

Finally, the high junction temperature changes the wavelength of the light emitted by the LED, (i.e. light color of LED) [23]. Thus, thermal management of the junction temperature is a critical factor for the high performance of LEDs.

1.4. High Lumen GaN LED Arrays

With the improvement of the LED technology, the application areas of the LEDs have increased. As shown in Figure 1.12, GaN-based LEDs are seen in a variety of lighting applications including medical, automotive, building, bridges, and horticulture due to increased illumination, longer life, light output, and multi-color effects.



Figure 1.12. The longest bridge in Africa with GaN LED lights (Courtesy of Philips)

In high lumen LED lighting applications discussed above, often a group of LEDs are used together as an array and mounted on a fixture designed for thermal management. An example of a high lumen LED array fixture, composed of 1890 LED chips, is shown in Figure 1.13. In high lumen LED array, hundreds of LED chips are used together in order to emit desired light output. While a single LED chip generates a smaller amount of heat (0.8-4 W), when these chips are used together, a large amount of heat production occurs. The generated heat and the thermal crosstalk between the chips lead to higher junction temperatures. Therefore, accurate characterization of the junction temperature and the thermal optimization of the high lumen LED arrays are

essential for high performance and long lifetime of high lumen LED array structures.



Figure 1.13. High lumen LED array for shipyard and buildings [24]

1.5. Thermal Characterization of LEDs and LED Arrays

The junction temperature of the chip affects lifetime, luminous flux, and color of the devices as shown in Figure 1.10 and 1.11. Therefore, accurate temperature measurement is required to design an LED device and evaluate an existing device [22]. 1.5.1 Experimental There are several experimental techniques for the accurate junction temperature measurement of GaN-based LED devices in the literature. The most common experimental methods are thermocouples, infrared cameras (IR) [20], forward voltage method [25], micro-Raman thermography [26], and nematic liquid crystal methods [25]. A thermocouple is a temperature sensor which produces temperature dependent voltage as a result of the thermoelectric effect, and this voltage interprets to measure temperature. Infrared camera (IR) can be used for quick visualization of the heat spreading from an LED system and any potential hot spots as shown in Figure 1.14. For the absolute temperature measurement, knowing the exact emissivity of the material is crucial feature and it is not known generally [13]. Therefore, IR camera can be complex and lead to inappropriate results for the measurements.

Nematic liquid crystal method provides high temperature accuracy (1°C) and spatial resolution. This method is also easy, and its application cost is low. On the

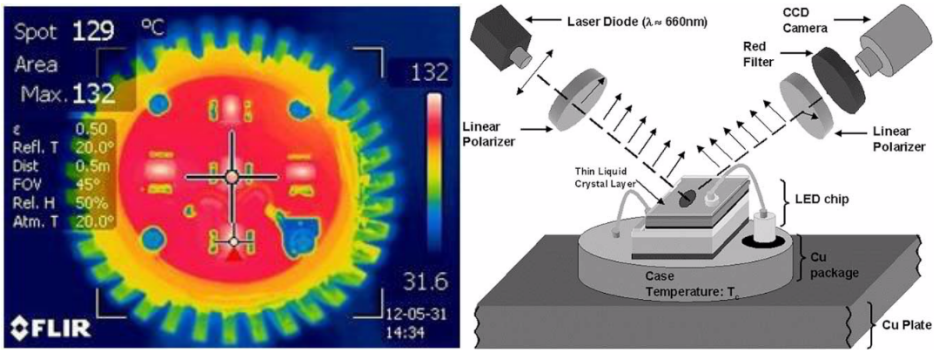


Figure 1.14. (a) Infrared camera result [20] (b) nematic liquid crystal thermal measurement [27]

other hand, implementation of this method is difficult because the microscope which carries the temperature information can be affected by the illumination light. By using laser illumination as shown in Figure 1.14(b), this disadvantage is eliminated. Therefore, this method is valuable method to study the thermal characterization of LEDs [27]. Raman spectroscopy is an optical scattering technique that is used to capture the vibrational energies of the optical phonons in Raman active materials. Due to the strong Raman scattering detected from the AlGaN layers, a volumetric averaged temperature across the device thickness can be estimated to determine the junction temperature. While junction temperature measurements for uncoated chip were successful with Raman thermometry, once it was coated with the phosphor–epoxy mixture, the excited broad emissions from the phosphor layer overlapped with the Raman emission from the underlying AlGaN chip. Thus, capturing the GaN Raman signature for phosphor-coated chips became challenging with the Raman spectroscopy. Finally, forward voltage is known as the most accurate way of thermal characterization of LEDs because measurements are based on using a pulsed driving current with a small duty cycle. Linear relation between the junction temperature and the forward voltage increases the accuracy. Also, it is the most straightforward way of measuring the thermal resistance of LEDs. On the other hand, forward voltage method has drawbacks which are the necessity of individual calibration of each LED and the variation in the forward voltage with exploitation time [25]. To summarize, direct and precise measurement of the junction temperature with the current experimental techniques is

difficult since most of these techniques measure average temperature of certain regions of the LED chip or package. Some of these methods require expensive experimental setups. Additionally, many times only the junction temperature of a single LED chip can be measured with techniques such as Raman spectroscopy, forward voltage, and nematic liquid crystal methods with desired resolution. It is often not as accurate and also difficult to use these methods for characterization of the junction temperatures of LEDs in high lumen LED array fixtures. Although, with techniques such as infrared camera surface temperature of the entire LED array can be obtained, as shown in the Figure 1.14 (a), accurate detection of the junction temperatures is not possible due to resolution and geometrical constraints. Therefore, numerical methods can be used for fast and cheap alternative to characterize junction temperature in LEDs and especially in LED arrays.

1.6. Modelling

To accurately characterize junction temperature numerical models are also developed in the literature such as Christensen and Graham 2009 [28], Ha and Graham 2012 [29], Han et al. 2010 [30], Hu, Yang, and Shin 2008 [31], Long, Liao, and Zhou 2012 [32]. In the model that generated by Ha and Graham the LED chip assumed as a uniform heat source and the chip details were not modeled, and constant junction-solder thermal resistance known from the product datasheets were used. Additionally, the model was generated only for a single LED chip as shown in Figure 1.15.

LED array model was generated by Christensen and Graham. In the following finite element analysis model, an array with 25 LED chips is used as shown in the Figure 1.16. In this model, constant thermal resistance value from datasheet was used.

By doing this temperature and thickness dependent thermal conductivity of the thin films in device structure on the junction temperature is neglected [28]. In some array models, chips are also modeled in these studies. However, it is difficult to model the chip in the LED array one by one due to the LED chip has very thin layers. Thus, the chip should be modeled in detail alone. There are not many studies on this subject

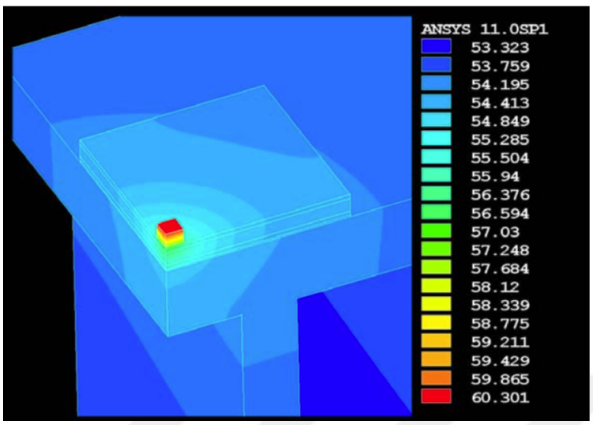


Figure 1.15. Thermal characterization for a single LED chip [33]

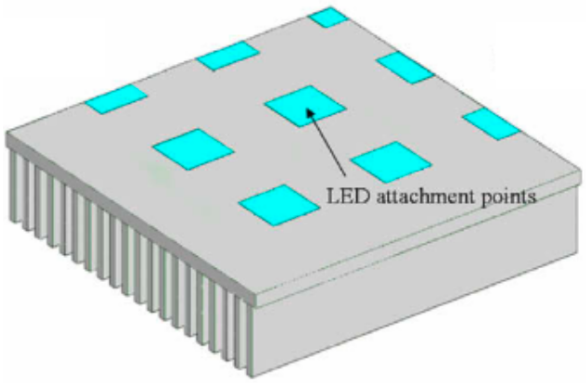


Figure 1.16. Thermal characterization for a LED array structure [28]

in the literature and more detailed chip models are needed to better estimate junction temperature. Multiscale thermal model is developed to model the chip detailed and to estimate junction temperature accurately.

1.7. Thermal Optimization of LED Arrays

With the use of multiple LED chips in a high lumen LED array system which has hundreds of chips on a printed circuit board (PCB) as shown in the Figure 1.17, higher heat loads are seen because of the number of LED chips and the thermal crosstalk between LED chips in the array. This heat load leads to high chip temperatures.

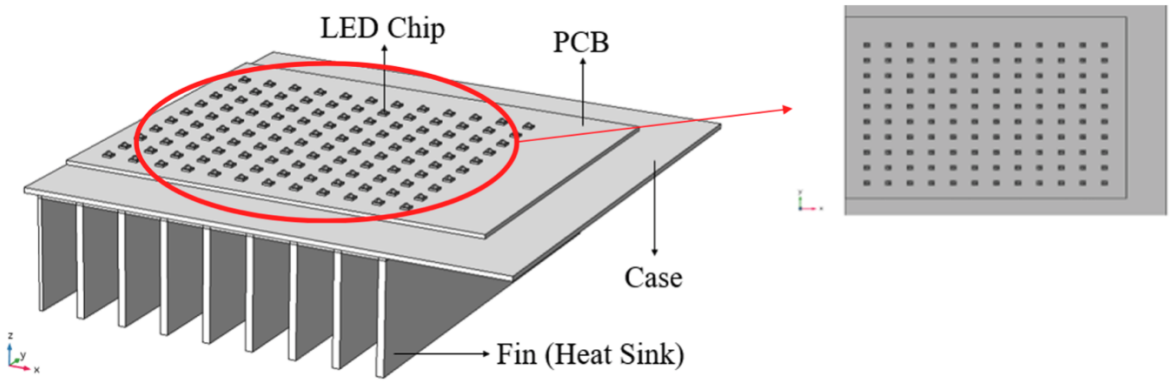


Figure 1.17. High lumen GaN based LED array structure

Junction temperature which is generally defined as chip temperature is the hottest temperature inside the chip. High junction temperature mainly affects LED chip negatively since this temperature is directly related to LED chip's efficiency, light output, performance and lifetime [16]. In order to solve these thermal problems for GaN-based LED arrays, different thermal management techniques such as: thermoelectric coolers (TECs) [34], heat pipes [35], liquid cooling methods [36], and finned heat sink [16] have been suggested in the literature. Among these methods, finned heat sinks are preferred the most since these do not require extra parts such as fan and/or pump as well as cooling liquid [37]. Today, heat sink arrays with rectangular plate fins are the most popular heat sink method [38]. It is used in different areas such as automotive [39], electronic cooling [38], and LED arrays. The optimization of the LED arrays with

finned heat sinks can be done in two parts: one of them is fin geometry optimization and the other one is LED array's optimization. For a fin geometry as shown in the Figure 1.18 optimization analytic [40]– [41], numerical [42], parametric [43], [44], and experimental [45] works have been performed.

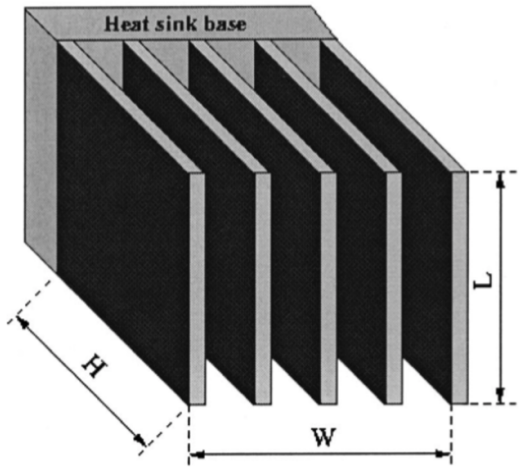


Figure 1.18. Fin structure from analytic work [46]

In previous analytical studies often the temperature difference and certain fin dimensions such as fin height (H), and fin thickness (t) were known, and the geometry optimization was done for a certain height and/or thickness [46]. In numerical methods, the height, thickness of the fin or spacing are changed simultaneously, while the temperature difference between the ambient and the base temperature was used as boundary conditions [42]. Therefore, the real effect of the optimization on the base temperature and the junction temperature cannot be observed since the base temperature is constant. On the other hand, it is not enough to optimize the fin structure since LED array structure optimization has different priorities such as mass, efficiency, and the solder (base) temperature of the LED arrays. After the fin optimization, the array optimization can be done. However, there is no study in the literature that does these two optimizations together. Some optimization methods were applied in the literature in order to optimize the heat sinks of LED arrays. Hongyu et al. investigated the effect of the number, thickness, and length of the fin separately [47]. Also, LiuYi showed the effect of the fin length and width on the junction temperature separately [48]. Hsieh

and Li are investigated the different fin types and the spacing between the fins [49]. Huang et al. made fin structure optimization for a single LED chip [50]. These optimizations were done based on a certain base temperature. Yet often base temperature should also be optimized, and therefore an unknown parameter. Moreover, optimizations were performed on only one variable such as fin thickness, height, and optimum spacing, while keeping all other parameters constant. Another problem with the optimization work in the literature is that it relies on the improvement of the initial design. Yet, if the initial design of the heat sink is not known, engineers will have to make an educated guess on the initial heat sink structure and start optimization from there. Thus, a universal optimization technique in which all geometrical variables and base temperature are varied is needed.

1.8. Problem Definition and Motivation

High lumen GaN LED array lights are designed and sold as replacements lights on roadways, tunnels, buildings, bridges, and vehicles. These LED arrays generally have many LED chips together and these chips consume 80 W – 500 W total power. 80% - 90% of the total power converts into heat. This high amount of heat leads to high junction temperatures inside the LED chip. Junction temperature which is the hottest temperature inside the chip is an important aspect of the LED array technology. High lumen LED array structures are designed according to lumen and lifetime values of the LED chip which are known from LED chip datasheets. These values are directly related to junction temperature. Therefore, accurate characterization of the junction temperature and the thermal optimization in order to decrease the junction temperature are essential for designing high lumen LED array. To estimate the junction temperature, a lot of work has been done in the literature. However, direct and precise measurement of the junction temperature was not possible with experimental and numerical methods. Experimental techniques are often used to measure solder temperature or average temperature of the LED chip. In addition, chip layers are not modeled detailed and the temperature dependent conductivities are not used in numerical models. On the other hand, different optimization methods are applied

to the fins and LED arrays in order to decrease the junction temperature. However, these optimizations are not covered all priorities of the high lumen LED arrays and these optimizations were done for only one variable such as fin thickness, height, and optimum spacing. Additionally, the starting point of the structure is not known in the literature. Therefore, this thesis aims to build multiscale thermal model and a universal optimization tool to accurately characterize and thermally optimize the GaN LED array fixtures, respectively. Finally, it is desired to characterize the real effect of these optimizations on the junction temperatures using both techniques proposed in this thesis.

1.9. Outline of the Thesis

This thesis is outlined in 5 main sections. LED technology is explained and the literature about thermal characterization and thermal management studies is investigated in the first chapter. Chapter 2 covers the multiscale thermal model, which consists of two stages which are package and chip level models. First, package level thermal model is explained in this section. Later, chip level model is explained according to temperature dependent thermal conductivities. Afterwards, the junction temperatures of the chips in different positions on the PCB in a simple LED array structure is analyzed. In chapter 3, a universal optimization method for high lumen LED array fixtures is described. To do that, natural convection in fins and the correlation of analytic equations are explained. Then, the optimization algorithm is described according to different optimization types. Finally, optimization results are shown with respect to different priorities of the high lumen LED arrays. Then the effect of the optimization on the junction temperature is shown with chip level model in chapter 4. In the last chapter, the findings of this study and the future research directions are discussed.

2. MULTISCALE THERMAL MODEL FOR HIGH LUMEN LED ARRAY FIXTURES

In the such high lumen LED light fixtures, LED chips are attached to the printed circuit board (PCB) with a solder material. PCB is then attached to the light fixture case using screws and often a proper thermal interface material (TIM) is used to enhance heat transfer between the PCB and the case. As seen in the Figure 1.7, heat generated between the n-type and p-type semiconductors (LED junction) is transferred to the heat sink through these layers. Each layer creates a thermal resistance to heat flow, R_{th}, which should be accounted in thermal analysis of LEDs. The thermal resistances on the LED array structure are shown in the Figure 1.7.

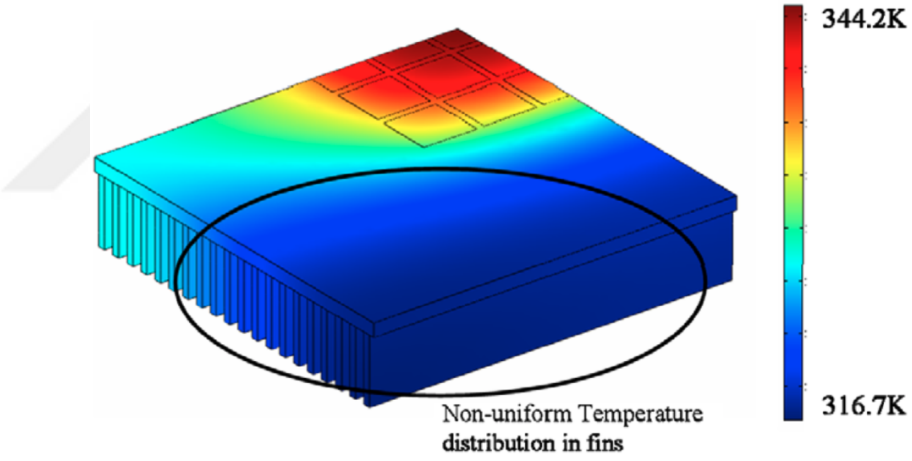


Figure 2.1. Temperature distribution in the LED array [28]

Maximum temperatures are observed in innermost chips where temperature measurements cannot be made easily as shown in the Figure 2.1. Moreover, the actual temperature of the hottest point in the devices might be different than the solder temperatures. Thus, to understand the real temperatures of the LED chips should be modeled in detail. However, for large LED fixtures, it will be computationally expensive to model each chip with its details. In thermal optimization studies where timing is especially important, this becomes a greater problem. To solve this problem a multiscale method is needed. Multiscale thermal model consists of two separate

models which are package level and chip level model. Both models are developed using COMSOL Multiphysics. Firstly, the package level model is investigated. Then, the information from the package level simulation is used as a boundary condition for a chip level simulation. The multiscale thermal model is applied to analyze the junction temperatures of a high lumen LED array fixture similar to one shown in Fig. 14. This fixture consists of 240 mid-power Cree EZ100-n LED chips with Cree® XLamp® XP-E [19] dies.

2.1. Package Level Model

A simplifided package level model shown in Figure 2.2 is built to analyze the LED array fixture in Figure 1.13. Total amount of power consumed by LED chips is P_{th}=192 W. It is known that approximately 75 % of this power is converted into heat in LEDs [20]. The dimension of the LED chips is 3.45mm×3.45mm×0.73mm. In addition to the chips, the package level has a printed circuit board (PCB) which has k_{PCB} =1 W/mK thermal conductivity, and the dimension of PCB is 175mm×145mm. Chips are distributed as a rectangular array and the distance between these chips horizontal and vertical spacing of the chips are represented with d_y and d_x respectively as shown in Figure 2.3. Finally, the package level has a fin structure which has 17 fins. Aluminum is used as fin material.

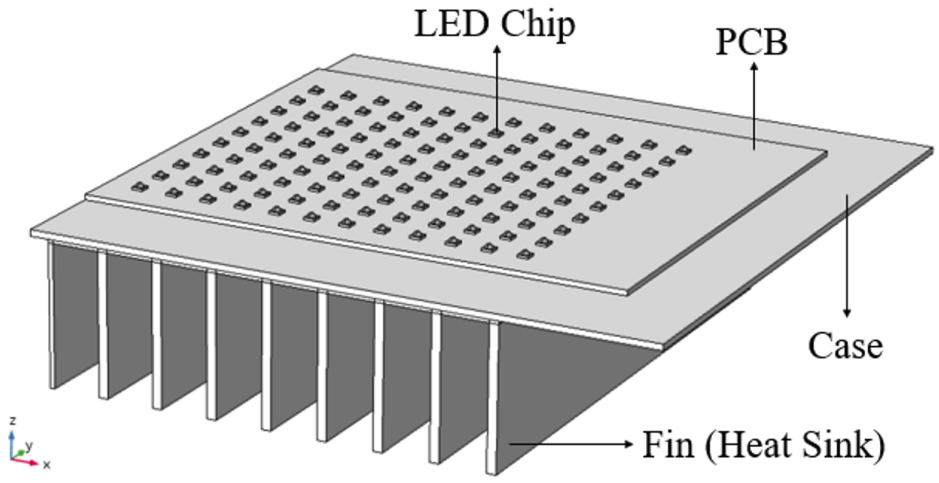


Figure 2.2. Package level model

The model is created in COMSOL Multiphysics and developed using "Heat Transfer in Solids" module by applying following steps;

- Geometry is generated in COMSOL according to the dimension of the LED array structure as shown in the Figure 21. The dimension of the PCB is 175mm×145mm and the base area of the fin just below the PCB is 240mm×170mm. The thickness of the base area is 5mm. The structure has 17 fins. The distance between the fins (S_{fin}) is 15mm and the height of the fins (H_{fin}) is 50 mm. The thickness of the fins is 5mm. This structure is taken from a real LED fixture which is used for industrial lighting [24].
- The material properties are defined to the structures. For the package level model, the constant thermal resistance value is used from the datasheet of the LED chip to decrease the computation time. The thermal resistance of the chip is 9 K/W [19]. Aluminum is used as fin material and the thermal conductivity of the fin is 196 W/mK. PCB has 1 mm thickness and its thermal conductivity is used as 1 W/mK.
- Boundary conditions are applied to the structure. Heat flux, heat source, symmetry, and insulation boundary conditions are applied as shown in the Figure 2.3. Heat flux is applied to the fin structures. For the heat flux value suitable convection coefficient, h, obtained using suitable empirical correlations as shown below [51]. Gravity is an important aspect of natural convection. The correlations are changed according to gravity direction. In this work, vertical fin structure is used, and the gravity direction is along the y-direction shown in the Figure 2.2 and 2.3.

  For the vertical plates [51]:

$$Nu = \left\{ 0.825 + \frac{0.387 \times Ra_L^{1/6}}{\left[1 + (0.492/Pr)^{9/16}\right]^{8/27}} \right\}^2 \tag{2.1}$$

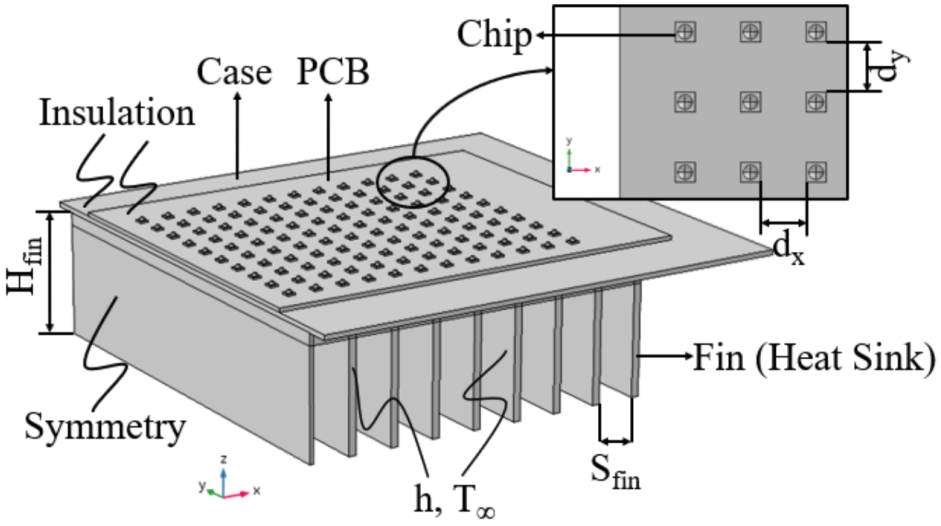


Figure 2.3. Package level model boundary conditions

$$h_w = \frac{Nu \times k_{air}}{L} \tag{2.2}$$

For the fins [52]:

$$Ra_S = \frac{g\beta\left(T_s - T_\infty\right) S_{fin}^3 Pr}{\nu^2} \tag{2.3}$$

$$Nu = \left[\frac{576}{(Ra_s S_{fin}/L)^2} + \frac{2.873}{\left(Ra_S S_{fin}/L\right)^{0.5}}\right]^{-0.5} \tag{2.4}$$

$$h = \frac{Nu \times k_{air}}{S_{fin}} \tag{2.5}$$

Heat source boundary condition is applied to the LED chips as it is calculated from the energy it uses. Thermal power for individual chip is found below equation:

$$P_{th=}0.75 \times \ V_f \times \ I_f \tag{2.6}$$

where V_f is forward voltage and If is the source current to the LED chip. These values are obtained from LED chip datasheet as shown in the Figure 1.9. For each LED chip, heat source value is determined by the ratio of the thermal power of an LED to its volume.

$$q''' = \frac{P_{th}}{V_{chip}} \tag{2.7}$$

By using above equations; thermal power is obtained as 0.8W and heat generation is found as Symmetry boundary condition is applied to the middle of the structure as shown in the Figure 2.3 in order to decrease the computation time. Insulation is applied to the upper faces of the LED array structure since the heat transfer direction is assumed to be towards the fin structure from the LED chips.

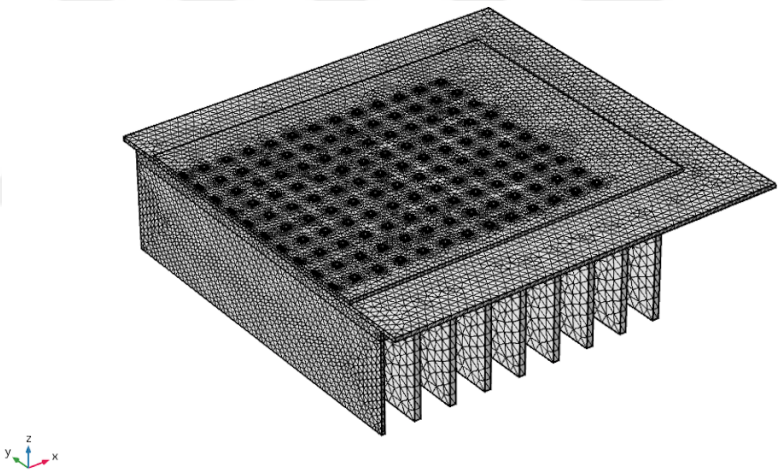


Figure 2.4. Mesh structure of the package level model

- Finally, tetrahedral mesh is applied to the structure and it has 122664 tetrahedral elements as shown in the Figure 2.4

2.1.1. Validation

To validate reliability of the model, an existing armature structure which is generated by EAE Lighting [52] was compared with the created model. The name of the LED armature shown in Figure 1.13 is GPRONA [53] and this armature is generally

used outdoors. GPRONA was simplified and created with steps explained in the package level model as shown in the Figure 2.5 (a). There are 1890 LED chips in the LED fixture and 202 W of heat is produced in this structure.

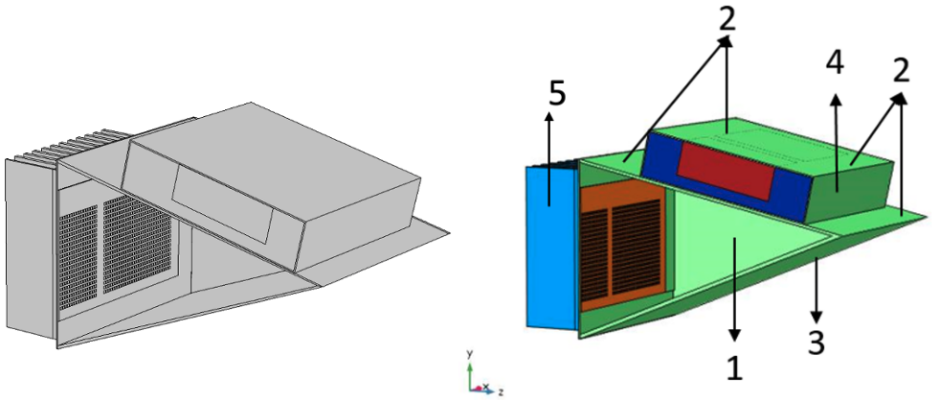


Figure 2.5. a) GPRONA simplified model with COMSOL b) Surfaces with convection coefficient

In the above model, volumetric heat generation was applied to every single LED chip. The model has 365319 tetrahedral mesh elements. In the model, the convection coefficient values used on the outer surfaces can be obtained through equations obtained from experimental data. For the vertical fins Equation 2.4 and for the remaining surfaces Equation 2.1 are used in the model [51]. There is natural convection in these regions, so the location of the surfaces according to gravity causes differences in the convection coefficients. For this purpose, surfaces are grouped according to gravity as shown in Figure 2.5 (b) and the convection coefficient values for these surfaces are obtained as shown in the Table 2.1.

When the model is analyzed, solder temperatures are obtained as shown in Table 2.2 In order to show the reliability of the model, the COMSOL analysis result was compared with the experimental test result of EAE Lighting company.

The experimental results of the 239th, 915th and 1354th LED chips shown in the Figure 2.6 were measured by the company. Table 2.2 shows the experimental results and the results obtained from the COMSOL analysis.

Table 2.1. Convection coefficient values of the package level model.

Surface Group	**Convection Coefficient (h) (W/m2K)**
1 (Side of the case)	4.2
2 (Upside of the case)	6
3 (Glass)	3
4 (Side of the case)	6
5 (Plate fins)	6

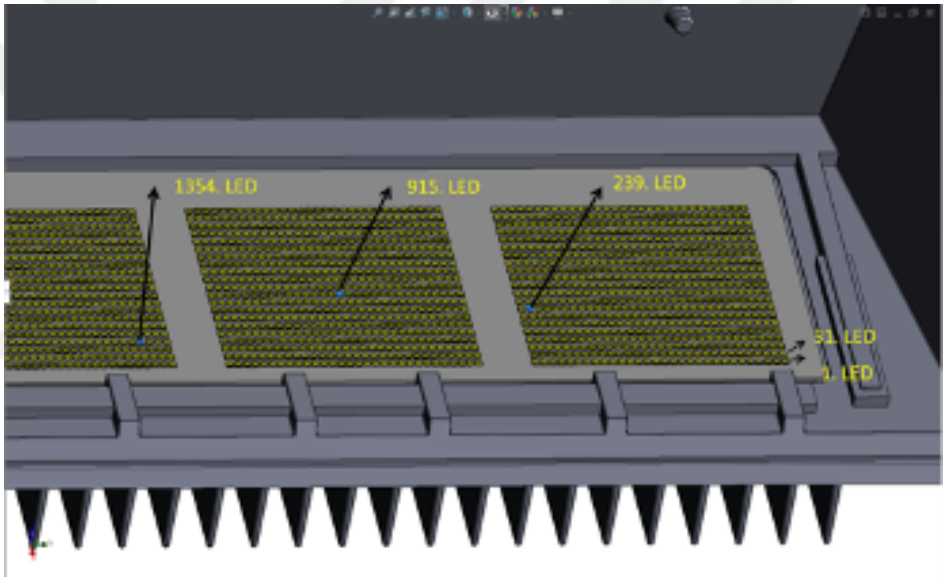


Figure 2.6. The location of measured LED chips

Table 2.2. Solder temperature comparison between experimental and package level model.

	Solder 239 (K)	**Solder 915 (K)**	**Solder 1354 (K)**	**Average PCB Temp. (K)**
Experimental (EAE)	353.04	359.54	353.71	344.33
COMSOL Package Level Model	355.8	357	355.96	343

As shown in the Table 2.2, the solder temperature values in package level model and the experimental method are very close to each other. Maximum 2,76 K temperature difference was obtained. This temperature difference shows that the reliability of the package level model.

2.2. Chip Level Model

In the chip level model, the layers of the chip are modeled in detail. Cree® XLamp® XP-E [19] is used as LED chip as shown in Figure 2.7 (a) and contains Cree EZ100-n [54] as die component as seen in Figure 2.7(b).

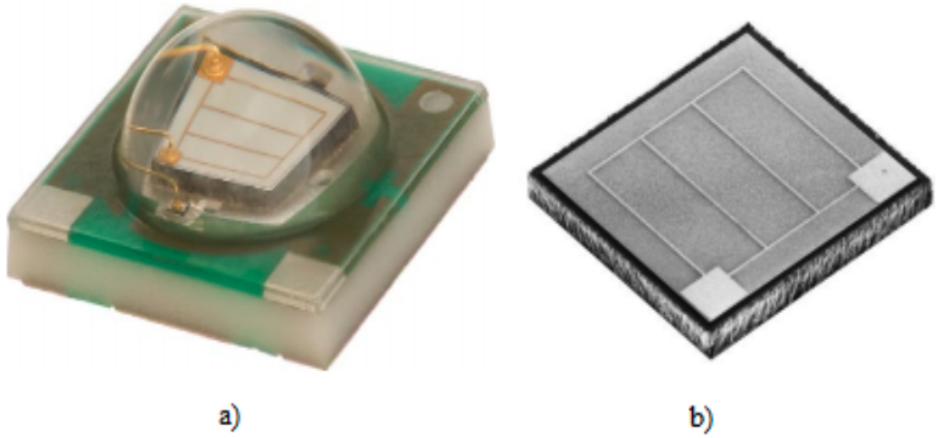


Figure 2.7. a) CREE XP-E LED chip [19] b) CREE EZ1000-n LED die [54]

This model has three main components; encapsulant, die, and the substrate as shown in the Figure 2.8. Encapsulant is used to protect and insulate the LED die. The material of the encapsulant is Silicone and it has very low thermal conductivity value. Die is the most important component in this model since it includes the multiple quantum well (MQW), i.e. the junction. The die has 7 different layers which are shown in the Figure 2.9 and is covered with the encapsulant.

The thermal conductivity values of these layers are important in this section since the conductivity values depend on thickness and temperature as shown in the Table 2.3. Bonding wires are connected to cathodes N plate. The die structure has two square

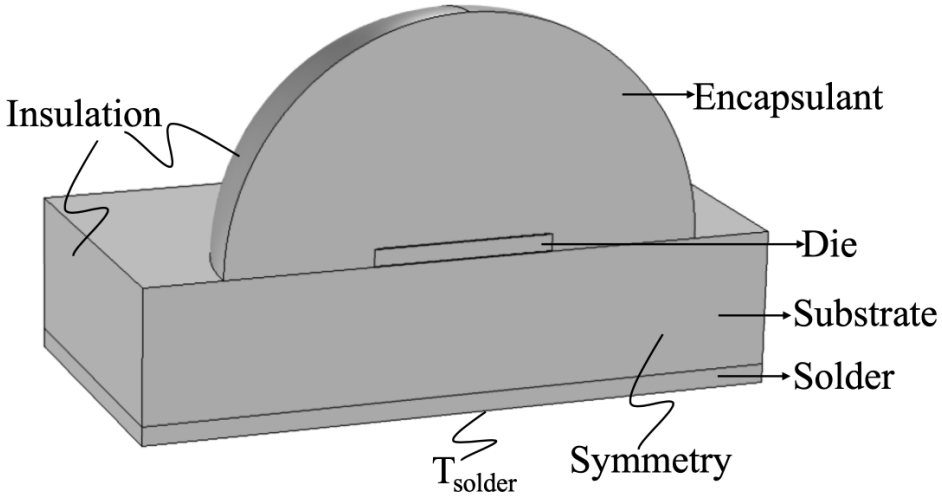


Figure 2.8. Chip level model structure

plate and their material is gold (Au) and it has 314 W/mK thermal conductivity. Anode plate is located at the bottom of the structure and the material of anode plate is Gold/Tin alloy (AuSn) and its thermal conductivity is 57 W/mK for 3μm thickness. The height of the N-doped GaN layer is 3μm and it's located under the cathode plates. Si doped bulk thermal conductivity is used for n-type GaN layer [55]. However, p-type GaN is only 200 nm thick, its thermal conductivity differs from the bulk conductivity. it is assumed that conductivity is 85 W/mK for 200 nm p-GaN at 300K and its change with temperature resembles bulk p-GaN [56]. Thermal conductivity of MQW layer which is located between n-type and p-type GaN layers, which consists of InGaN/GaN layers, is 11.9W/mK [57]. A metallic layer is located under the p-GaN and it prevents absorption of light by the substrate layer and it has 200nm height. Material of the substrate layer is silicon (Si) for die and alumina for the chip.

All the thermal conductivity values used in simulations are summarized in Table 2.3. When the model is simulated with these thermal properties at 300K, it was ensured that temperature difference calculated with the values given in the datasheet is the same with the temperature difference in the simulation.

The chip level model is developed in COMSOL by using "Heat Transfer in Solids"

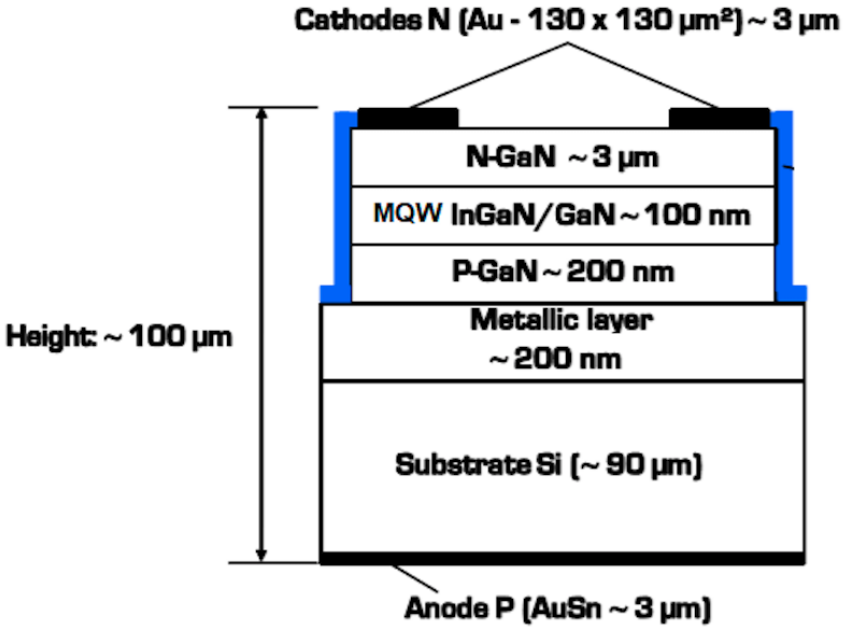


Figure 2.9. CREE EZ1000 diagram [9]

module by applying following steps:

- Geometry is generated in COMSOL according to dimension of the LED chip and die as shown in the Figure 2.8.
- The material properties are defined to the layers of the chip according to the values in the Table 2.3.
- Boundary conditions are applied to the structure as shown in the Figure 2.8. Heat source, insulation, symmetry, and temperature boundary conditions are used. Symmetry boundary condition is applied to the middle of the structure as shown in the Figure 2.9 in order to decrease the computation time. Insulation is applied to the upper faces of the LED chip, encapsulation, since the heat transfer direction is assumed to be towards the substrate from the LED die. For the temperature boundary condition, the result of the package level is needed. The package level temperature result is used as temperature boundary condition to the chip level model. It is applied to the bottom surface of the solder layer. As known from LED physics, the heat is generated in the MQW layer which is located between n-type and p-type GaN layers and heat source boundary condition defined as volumetric

Table 2.3. Thermal conductivity values of chip and die layers.

Material	**Thermal Cond. (W/mK)**	**Thickness**
Au	314	3 μm
n-GaN	$216\times(300/T)^{0.78}$ [54]	3 μm
InGaN/GaN	11.9 [56]	0.1 μm
p-GaN	-0.0002×T^2 + 0.263×T + 9.3312[55]	0.2 μm
Metallic layer	57	0.2 μm
Si	$148\times(T/300)^{-1.3}$ [57]	90 μm
Au80Sn20	57	3 μm
Alumina	$51571\times T^{-1.265}$	730 μm
SAC305 (Solder)	57	102 μm

heat generation is applied to this layer. The value of the heat generation is 8.33x10^{12} W/m^3

- Finally, tetrahedral mesh type is applied to the structure and it has 1326504 tetrahedral mesh elements as shown in the Figure 2.10. If every LED chip in the structure is modeled as explained above, it will take a long time to find the solution due to the number of mesh elements in the chip level model.

2.3. Results

2.3.1. Package Level Model

For the original device structure maximum temperature is obtained as 415 K and the maximum solder point temperature is seen as 413 K. The maximum temperature is obtained at the middle of the structure and the minimum temperature is obtained at outside of the structure as shown in the Figure 2.11. These temperatures are very close to the limit temperature of the LED chip.

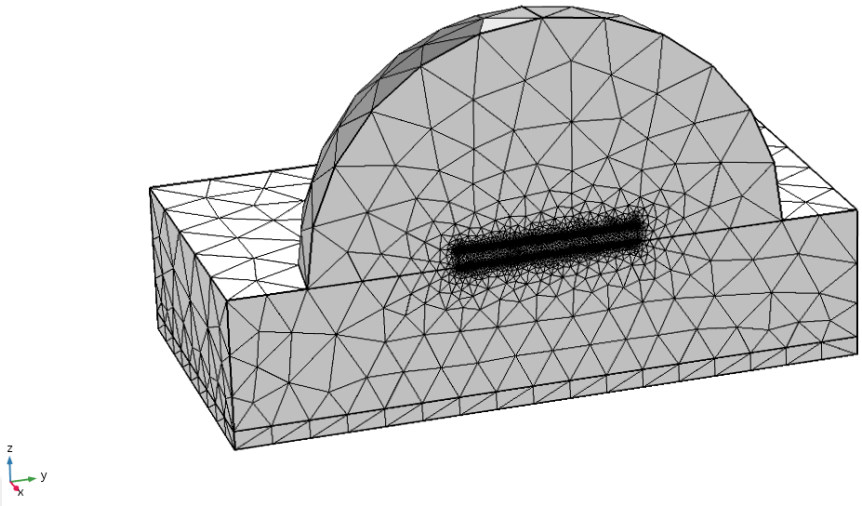


Figure 2.10. Mesh structure of the chip level model

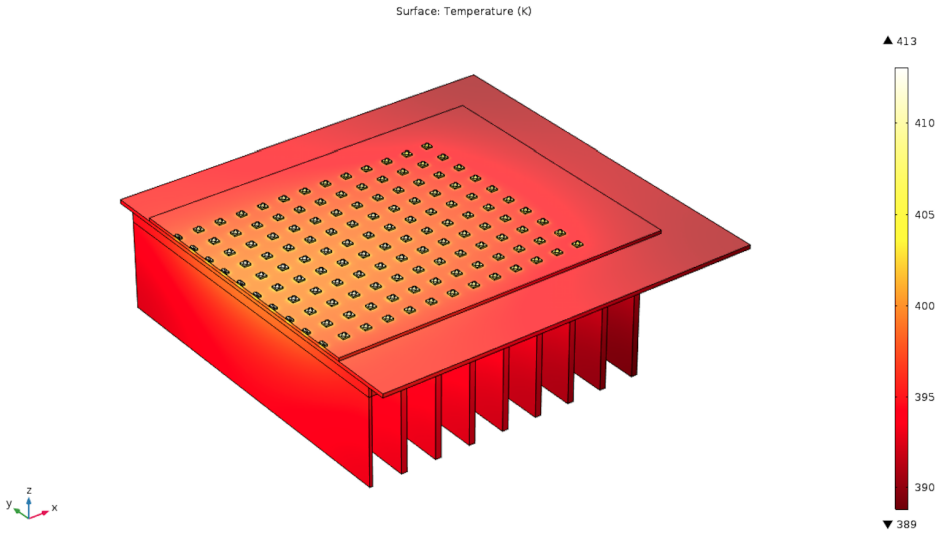


Figure 2.11. Temperature distribution of the package level model

In the package level model, solder temperature is important since it is used to obtain junction temperature with following equation:

$$T_j = T_{solder} + R_{th} \times \ P_{th} \tag{2.8}$$

where Tj is a junction temperature, Tsolder is solder temperature, Rth thermal resistance between solder and junction point and it is known from LED chip datasheet, and P_{th} is the LED chip power and it is also known from datasheet. Chip power is 0.8 W and thermal resistance is 9 K/W which are known from datasheet. Then, by using above equation, junction temperature is obtained as 420.32 K.

2.3.2. Chip Level Model

In the chip level model, the real junction temperature is analyzed. Figure 2.12 shows the temperature distribution inside the original LED chip which is the hottest chip inside the package level structure as shown in the Figure 2.11. Chip level model is estimated higher junction temperature than package level model since it includes temperature and thickness dependent thermal conductivities.

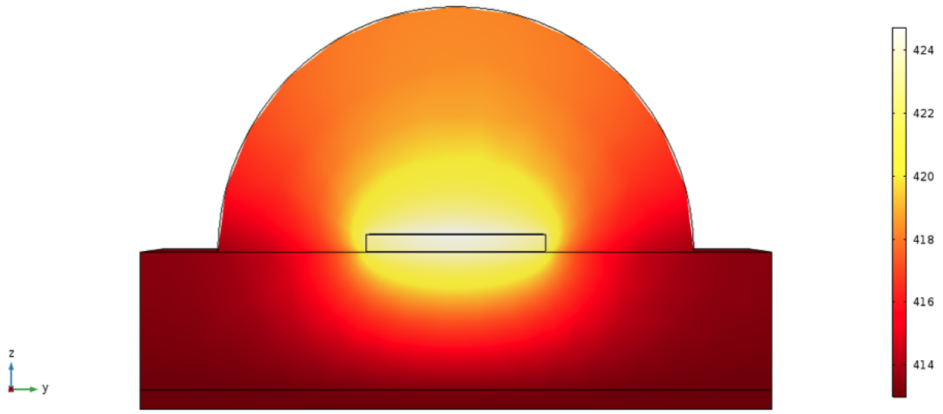


Figure 2.12. Temperature distribution of the chip level model

For the highest solder temperature value, junction temperature value is different between package and chip level model. 420.32 K is obtained from package level model.

Table 2.4. Junction temperature in the package and chip level models.

	T_{solder} (Package Level) (K)	T_j (Package Level) (K)	T_j (Chip Level) (K)
Maximum Junction Temperature	413	420.32	424.75
Minimum Junction Temperature	410	417.32	421.64

However, 424.75 K is obtained from chip level model. This difference may seem small difference but with this difference LED chip break down. Therefore, chip level model is important at high temperatures in the high lumen LED arrays especially. On the other hand, minimum solder temperature is obtained as 410 K from package level model. By applying this temperature to the chip level model as a boundary condition, 421.64 K is obtained from chip level model.

As seen in the Table 2.4, there is a temperature difference between the innermost (hottest) and the outermost (coldest) chip in the package level model. This temperature difference is different in the chip level model due to temperature dependent thermal conductivities. Additionally, thermal optimization is needed in order to decrease junction temperature values. Thermal optimization method will be described in the next chapter.

3. UNIVERSAL OPTIMIZATION MODEL FOR HIGH LUMEN LED ARRAYS

In high lumen LED array structure, heat load values are too high since the number of the chips in the structure and the thermal crosstalk between chips. These heat load leads to high junction temperature, and it affects the LED chip negatively or breaks down directly. To improve the efficiency and save the LED chips thermal optimization is needed. Manufacturers can have variety of priorities while thermally optimizing high lumen GaN LED array structures. These priorities can be divided into two main groups as shown in the Figure 3.1. First group of thermal optimization also has structural optimization goals such as minimizing mass or volume while keeping temperatures low. Second group, on the other hand only has thermal optimization goals such as reaching to highest total efficiency, minimum base temperature, maximum single fin efficiency, and maximum effectiveness. All optimization types are done by taking a certain interval (∼0.5 W) according to heat removal value ($Q_{desired}$) which is entered at the beginning of the optimization.

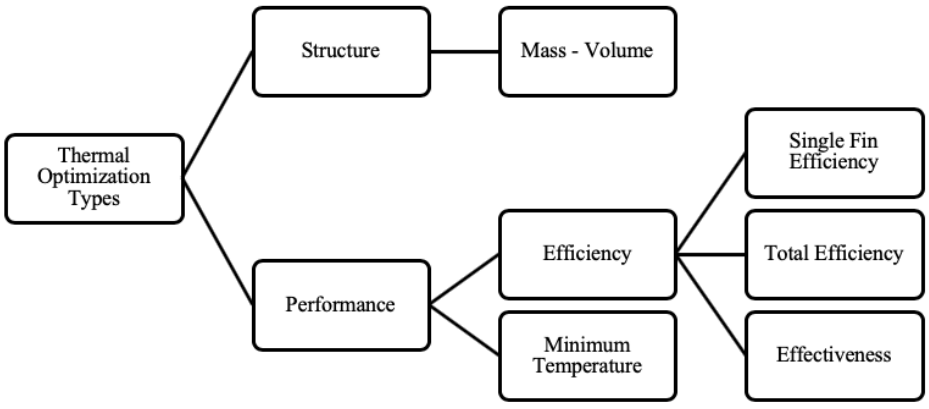


Figure 3.1. Optimization types

In addition to the fin structure the LED array can also be optimized. In order to optimize the LED array configuration, different distances between the chips, the number of the LED chip, and the power of the LED chip can be changed. The base

area of the structure is designed as shown in the Figure 3.2. In the figure, W is width of the base area, L is length of the base area, c_x and c_y values are the length of the chip in the x and y direction, d_x and d_y are the distance between the LED chips in the x and y direction, N_x and N_y are the number of the LED chips in the x and y direction.

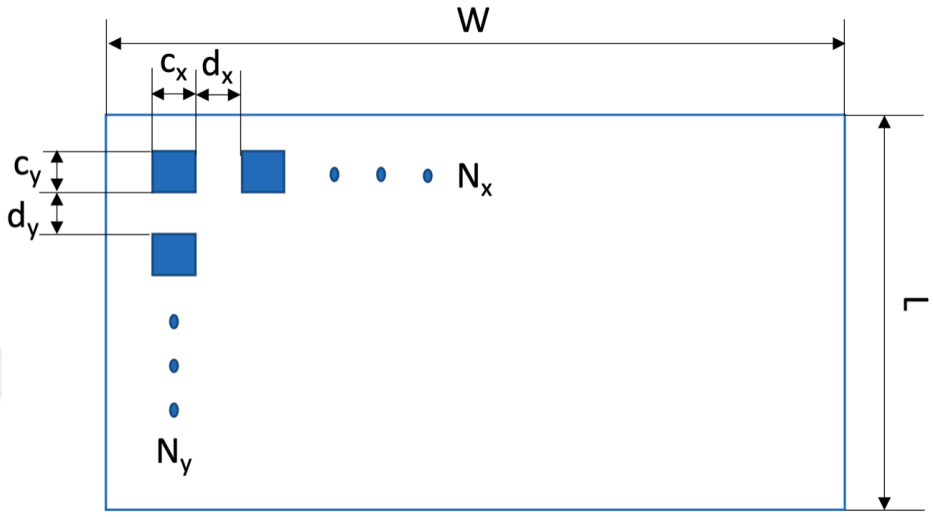


Figure 3.2. LED array configuration

In this chapter, different thermal optimization methods and the effect of these optimization on the solder temperature is analyzed. Additionally, a basic fin structure is created to start optimization for high lumen LED array structure.

3.1. Optimization Algorithm and Correlations

In order to optimize the geometry of heat sinks with rectangular fins for LED array structures appropriate optimization technique and input parameters should be known based on user demands. Regardless of the optimization type, input parameters: width (W) and length (L) of the fin base area shown in the Figure 3.3 are kept constant. Here, the aim is to find the height (H) and thickness (t) of the fins, the distance between the fins (S_{opt}), and the number of fins (n). In order to find these values, a database is created in this optimization method. The database is created according to base temperature and the thickness value since they are unknown, and these values are estimated.

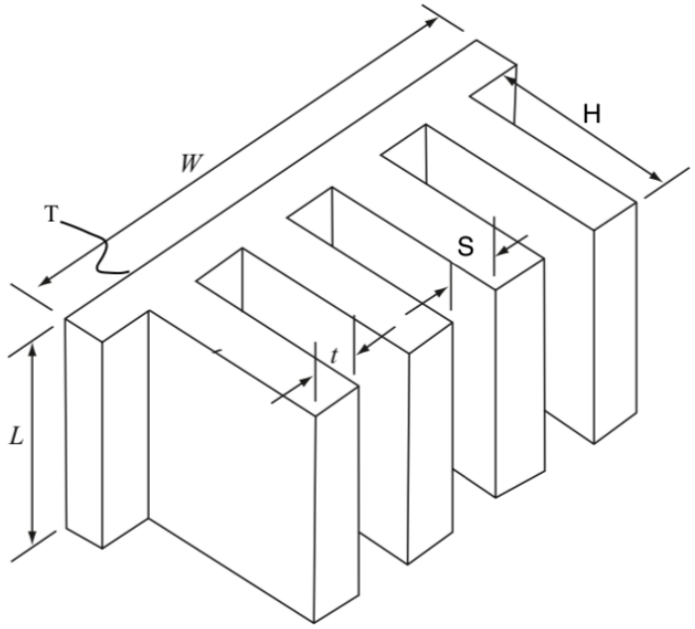


Figure 3.3. Fin structure

A new database is created for the desired Q value as entered at the beginning of the optimization from this database. Then, the method gets the results from the database for the desired optimization type. Optimization technique developed in MATLAB and consists of analytic equations and numerical methods shown in Figure 3.4 is explained next.

1) The first step of the optimization is to enter the width (W) and the length (L) of the heat sink and the total amount of the desired heat dissipation ($Q_{desired}$). The width (W) and length (L) of the heat sink depend on the number, dimension, and the spacing between the LED chips as shown in Figure 3.2. The desired heat dissipation is calculated by multiplying the number of the chips and single chip power, which can be obtained from the LED datasheets [13]. It is known that approximately 75% of the total power will convert into heat.

2) Pick a base temperature (T_{base}).

3) According to T_{base}, temperature difference between ambient temperature and

the base temperature is calculated with the following equation:

$$\theta_b = T_{base} - T_{ambient} \tag{3.1}$$

Temperature difference is used in the next steps to find the Rayleigh number. Film temperature (T_{film}) is also found using the base temperature and is used to calculate the material properties of the cooling fluid:

$$T_{film} = \frac{T_{base} + T_{ambient}}{2} \tag{3.2}$$

Air is used as the cooling fluid in this work. The material properties of the air such as thermal conductivity (k_{air}), dynamic viscosity (μ_{air}), and Prandtl number (Pr) are calculated in MATLAB. Temperature dependent material properties of air is uploaded to MATLAB then they are chosen according to film temperature. Aluminum is used as fin material in this study. Thermal conductivity of the aluminum (k_{fin}) is 196 W/mK and it doesn't depend on temperature. In addition, density of the aluminum (ρ_{fin}) is used as 2700 kg/m_3 and the specific heat (c_p) is used as 910 J/kgK.

4) Next step is to find the heat transfer coefficient (h) of the vertical walls between the fins [51], and for this Rayleigh number (Ra_L) has to be calculated:

$$Ra_L = \frac{g\beta\theta_b L^3}{\alpha\nu} \tag{3.3}$$

where g is the gravity, β is the thermal expansion coefficient, θ_b is the temperature difference between the ambient and the base, L is the length of the fin, α is the thermal diffusivity and ν is the kinematic viscosity. By using Rayleigh number, convection coefficient of the vertical fin wall shown in the Figure 31, ($\bar{h}_{wall}$) is calculated [51]:

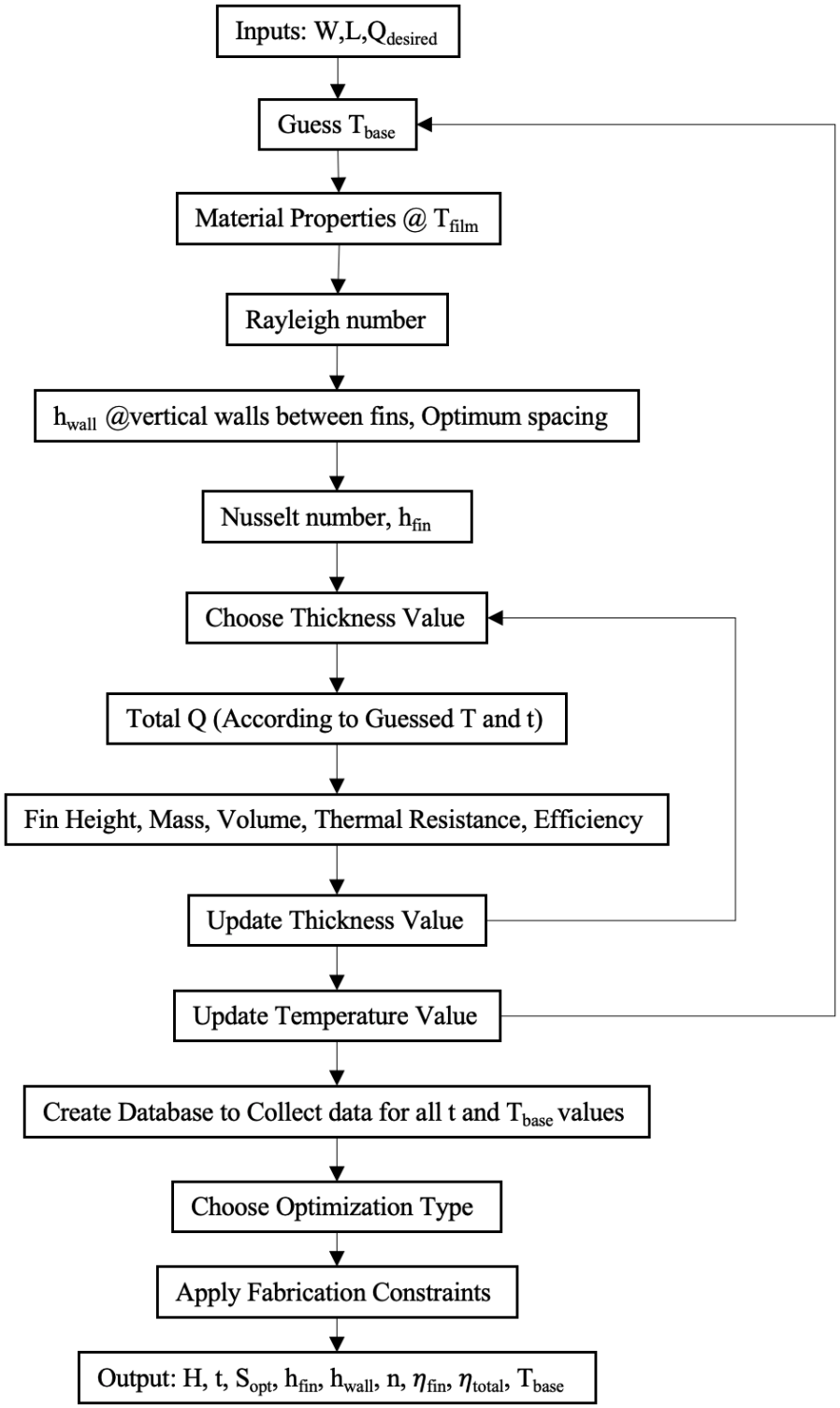


Figure 3.4. Optimization algorithm

$$\bar{h}_{wall}=\begin{cases}\frac{0.59Ra_L^{0.25}k_{air}}{L}\ ,\ 10^4<Ra_L<10^9\\ \frac{0.1Ra_L^{1/3}k_{air}}{L}\ ,\ 10^4<Ra_L<10^9\end{cases} \tag{3.4}$$

5) Natural convection between vertical flat plates was first examined by Elenbaas in 1942 [58]. Optimum spacing (S_{opt}) is calculated using the relations of Bar-Cohen and Jelinek [40] based on Elenbaas' relations as:

$$S_{opt}=2.714Ra_L^{-0.25}L \tag{3.5}$$

Rayleigh number according to optimum spacing is calculated with the following equation [59]:

$$Ra_S=\frac{g\beta\theta_b S_{opt}^3}{\alpha\upsilon} \tag{3.6}$$

Then Elenbaas number (El) is calculated with Ra_s, S_{opt}, and L with the below equation [60]:

$$El=\ Ra_S\frac{S_{opt}}{L} \tag{3.7}$$

Later Nusselt number is calculated to find the convection coefficient of the fins as [60]:

$$Nu=(\frac{576}{El^2}+\frac{2.873}{El^{0.5}})^{-0.5} \tag{3.8}$$

Then, the heat transfer coefficient of the fin is obtained using Elenbaas number and the optimum spacing.

$$\bar{h}_{fin}=\frac{Nu\times k_{air}}{S_{opt}} \tag{3.9}$$

6) Once convection coefficient on the fin surfaces and the walls between the fins are obtained one can continue to calculate total heat removal rate. For this fin thickness (t) is needed. In order to determine the correct fin thickness calculations are done for a variety of thickness (t) values thus at this step a fin thickness should be picked.

7) Assuming the heat loss at the fin tip is negligible, the heat transfer rate from a single fin with an adiabatic tip (q_f) is calculated using [60]:

$$q_f = \sqrt{2\bar{h}_{fin}k_{fin}t}\theta_b L tanh\,(mH) \tag{3.10}$$

where m is the performance factor of the fin and H is the height of the fin [60]. Performance factor (m) is calculated with [41]:

$$m = \left(\frac{2 \times \bar{h}_{fin}}{k_{fin} \times t}\right)^{0.5} \tag{3.11}$$

Later, heat transfer from the vertical walls (q_w) between the fins is calculated with [60]:

$$q_w = \bar{h}_{wall} \times\ L \times\ S_{opt} \times \theta_b \tag{3.12}$$

The total heat transfer rate (Q_t) is the sum of the heat transfer rate from the fin surfaces and the vertical walls between the fins [60].

$$Q_t = nL\theta_b \left[\sqrt{2\bar{h}_{fin}k_{fin}\frac{A_P}{H}}tanh\,(mH) + \bar{h}_{wall}\left(\frac{W}{n} - \frac{A_P}{H}\right)\right] \tag{3.13}$$

where H, A_p = H x t, n, W, and L are height, profile area, number, width, and the length of the fins, respectively. In order to get the maximum heat transfer rate, fin height that satisfy the following derivative should be used:

$$\frac{dQ_{tot}}{dH} = 0 \tag{3.14}$$

When applied to Equation 3.11 the above results in the following relation:

$$\beta \; tanh\beta - 3\beta^2 sech^2\beta = \frac{2\bar{h}_{wall}H}{k_{fin}} \tag{3.15}$$

From here β=mH ,array optimization parameter[59], can be obtained as:

$$\beta = mH = 1.4192 + 1.125\frac{\bar{h}_{wall}H}{k_{fin}} \tag{3.16}$$

By combining this information, the height of the fin is calculated with respect to thickness:

$$H\left(t\right) = \frac{1.4192\left(\frac{k_{fin}t}{2\bar{h}_{wall}}\right)^{0.5}}{\left[1 - 1.125\left(\frac{k_{fin}t}{2\bar{h}_{wall}}\right)^{0.5}\frac{\bar{h}_{wall}}{k_{fin}}\right]} \tag{3.17}$$

Finally, the number of fins (n) is found with respect to t and S_{opt}:

$$n = \frac{W + S_{opt}}{S_{opt} + t} \tag{3.18}$$

Volume (V_{fin}) and mass (M_{fin}) of the fins are calculated as below:

$$V_{fin} = L \times \; H \times \; t \times \; n \tag{3.19}$$

$$M_{fin} = V_{fin} \times \rho_{fin} \tag{3.20}$$

where ρ_{fin} is the fin density. Total efficiency is calculated as shown in the Equation X by dividing the maximum heat transfer rate by the total heat transfer rate which is $Q_{desired}$.

$$\eta_{tot} = \frac{Q_t}{Q_{max}} \tag{3.21}$$

Single fin efficiency (η_{fin}) is the ratio of the heat transfer from a single fin to the maximum possible heat transfer from the fin and it is calculated as below:

$$\eta_{fin} = \frac{\tanh(mH)}{mH} \tag{3.22}$$

Thermal resistance (R_{th}) shows the temperature difference between the ambient temperature and the base temperature for 1W heat transfer rate. It is calculated by the ratio of the temperature difference to the emitted heat as shown below:

$$R_{th} = \frac{\theta_b}{Q_{tot}} \tag{3.23}$$

Effectiveness is the ratio of the heat transfer with fin to the heat transfer with no fin. It is calculated as below:

$$\varepsilon_{fin} = \sqrt{\frac{k_{fin}P}{\bar{h}_{fin}A_c}} \tanh(mH) \tag{3.24}$$

where P=2(L+t) is the perimeter of the fin area and A_c=L×t is the fin area.

8) Change thickness and repeat step 7 until all desired thickness values are analyzed.

9) Change T_{base} and repeat steps 3 to 8 until all desired base temperature values are analyzed.

10) At the end of these steps a database similar to one shown in Table 3.1 is obtained. There are Q_t, H, S_{opt}, n_{fin}, ε_{fin}, η_{fin}, V_{fin}, M_{fin}, η_{tot}, R_{th}, $\bar{h}_{fin}$, $\bar{h}_{wall}$ etc. values for each thickness and temperature value in the database.

11) The optimization result of this work does not have any geometric limitations. However, there may be some restrictions such as the maximum and minimum fin thickness and fin length that can be produced or the ratio of the fin height to fin thickness

Table 3.1. Junction temperature in the package and chip level models.

Temperature (K)- Thickness (mm)	300 K	300.1 K	...	350 K
1 mm	Q_t, H, S_{opt}, n_{fin}, ε_{fin}, η_{fin}, V_{fin}, M_{fin}, η_{tot}, R_{th}, $\bar{h}_{fin}$, $\bar{h}_{wall}$	...	...	...
1.1 mm	...	...	...	...
...	...	...	...	...
20 mm	...	...	...	Q_t, H, S_{opt}, n_{fin}, ε_{fin}, η_{fin}, V_{fin}, M_{fin}, η_{tot}, R_{th}, $\bar{h}_{fin}$, $\bar{h}_{wall}$

during the production of these structures. All these are neglected in this work. Although, if desired, a new database can be created via removal of the values that do not comply with the limitations in this step.

12) The total heat removal rate (Q_t) values are filtered to be closest ($\pm$0.5 W) to the value $Q_{desired}$ which is entered at the beginning of the optimization. Then, based on the desired optimization type shown in-Figure 28 (minimum mass, minimum base temperature etc.), optimization results will be selected according to the priorities as explained next.

- Minimum Mass/Volume (M_{fin} / V_{fin}): Fin is chosen due to low cost generally [37] and the cost of the fin structure is reduced by decreasing the total mass of the structure. To decrease the mass of the fin structure, this optimization can be used. The mass of the fin is evaluated for a certain range of the temperature and thickness values. Then, the lightest one is chosen from filtered database.
- Maximum Total Efficiency (η_{tot}): Total efficiency is another selection criterion. Total efficiency shows that the most efficient fin structure. Efficiency is calculated

for all temperature and thickness values. Then, the most efficient fin structure is chosen among the filtered database.

- Maximum Single Fin Efficiency (η_{fin}): Single fin efficiency is the ratio of the heat transfer from a single fin to the maximum possible heat transfer from the fin [61]. It is found with the Equation 3.22. The aim of this priority is to reduce the number of the fins.
- Minimum base temperature (T_{base}): Minimum base temperature is obtained where the thermal resistance is smallest. Thermal resistance (R_{th}) shows the temperature difference between the ambient temperature and the base temperature for 1W heat transfer rate. Thermal resistance values for a certain range of heat transfer rate is calculated with Equation 3.23. After that, the minimum thermal resistance value is chosen among the filtered database because the minimum temperature difference is needed in the fin structure to get minimum temperature.
- Maximum Effectiveness: The ratio of the heat transfer with fin to the heat transfer with no fin is defined as effectiveness(ε_{fin}). It shows how necessary the fin structure is. Fin effectiveness is calculated with Equation 3.24.

3.2. Results

Optimization is made for a structure with 240 LED chips. Cree® XLamp® XP-E is used as a chip component. These chips generate 192W total heat load. The dimension of these chips is 3.45mm × 3.45mm and the spacing between the chips 2 mm for each direction. With these values input values is calculated as Q=192 W, W=138.8 mm, and L=56.5 mm. Aluminum is used as fin material and air is used as cooling liquid material. Using the new optimization method, a basic fin structure dimensions such as spacing, fin thickness and fin height are obtained. Also, some thermal properties of this structure for instance heat transfer coefficient values and heat transfer rate of the structure are calculated in the numerical model as shown in the Table 3.2.

Table 3.2. Optimization results of the initial structure.

Opt. Type	H(mm)	t(mm)	S(mm)	T_{base}(K)	n	R_{th}(K/W)	η_{fin}(%)	η_{tot}(%)	M_{fin}(kg)	ε_{fin}	$\bar{h}_{fin}$(W/m^2K)	$\bar{h}_{wall}$(W/m^2K)
η_{tot}	162.62	1.30	5.16	377.50	22.00	0.42	38.66	65.31	0.75	202.16	7.37	9.01
M_{fin}	147.58	1	5.13	383	24.00	0.44	34.15	65.10	0.53	229.64	7.48	9.17
R_{th}	268	3.15	5.23	369.5	17.00	0.37	56.37	62.21	2.22	125.43	7.20	8.82
η_{fin}	580	15.95	5.00	409.50	7.00	0.59	84.76	39.42	9.29	39.75	7.92	9.71
ε_{fin}	147.58	1	5.13	383	24.00	0.44	34.15	65.10	0.53	229.64	7.48	9.17

This table is generated for the initial structure which is described at the beginning of the chapter and the input values of the structure are Q=192 W, W= 138.8 mm, and L=56.5 mm. The need for the optimization is not decided by investigating above Table. The table only shows that the results of the different optimization types. According to results; - Maximum fin height is obtained by using single fin efficiency type. The dimension of the structure cannot appropriate to produce due to fin height. Also, the mass of the structure is highest in this type. Therefore, single fin efficiency type is not highly recommended. - The minimum mass optimization type has minimum fin height. The LED array structure can produce with the result of this optimization type. However, it is about 13K warmer than the minimum temperature type. - Maximum efficiency type has average values compared to other types. It has similar mass value with the minimum mass type, but base temperature value is lower than the minimum mass type. Thus, it can be used as an alternative to the minimum mass type. - Although the minimum temperature type has the lowest temperature, its mass and length are higher than the maximum efficiency type. The temperature difference between two types is only 7K. Therefore, maximum efficiency type can be an alternative to the minimum temperature type.

To compare the optimization priorities and optimize the LED array, different LED array cases are analyzed with the proposed optimization method.

1) LEDs Chips: Same Number, Same Layout, Same Spacing, Different Power The distribution of the LED chips on the base area and the number of the chips are the same with the base structure of this work, different LED chips are used to this structure which have different heat generation values. These values are 0.2 W, 0.4 W, 0.8W, 0.9 W, and 1 W. Thus, the total heat generation value is increased according to the heat generation value of the single LED chip since the number of LED chip is not changed. W= 138.8 mm and L= 56.5 mm since layout and chip number are the same with the initial structure. By applying different heat load values to the structure, different heat loads are generated and following results are obtained as shown in the Figure 3.5:

- The base temperature is directly proportional to the heat load value in the same optimization priority.
- Base temperature values are quite similar at low heat load values. In that case, the importance of the different optimization types is negligible. However, the base temperature is different at high heat loads. For example, the temperature difference between the low and high heat loads is 106.5 K for single fin efficiency case and the difference is 65.5 K for the thermal resistance case. This situation shows that the thermal resistance optimization is better than other priorities and the single fin efficiency type is not appropriate at higher heat load values.

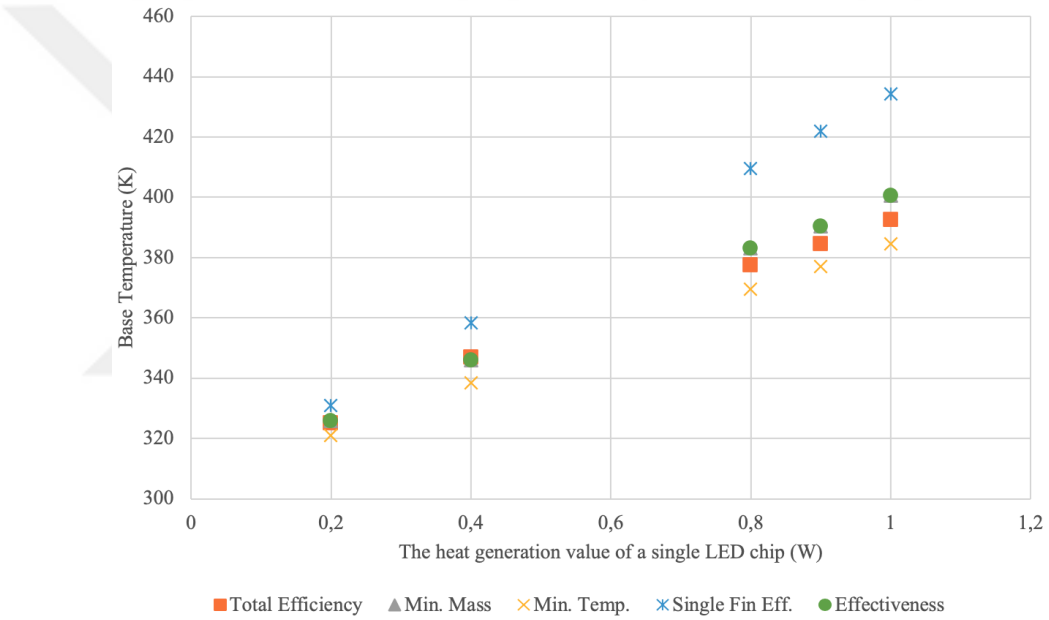


Figure 3.5. Base temperature vs. the heat generation of a single LED chip

2) LEDs Chips: Same Number, Same Power, Same Layout, Different Spacing The same number of the LED chip and different distance (d_x and d_y) between the LED chips are used. Thus, the base area of the structure is increased because the width and the length of the fin are calculated below:

$$W = c_x \times N_x + d_x \times (N_x - 1) \tag{3.25}$$

$$L = c_y \times \ N_y + d_y \times (N_y - 1) \tag{3.26}$$

However, the heat load is the same in this case due to the same power and same number. The distance between the chips is equal in x and y direction. 1, 2, 3, 4, and 5 mm are applied to the structure, the following results are obtained. The convection coefficient values which are shown in the Figure 3.6 are affected by applying different distances.

- The convection coefficient value is decreased when the distance is increased since convection coefficient is directly related to temperature difference between the base temperature and the ambient temperature.
- The base temperature and the temperature difference between the different optimization types is decreased by increasing the distance between the LED chips. It shows that the importance of the different optimization types can be negligible at higher distances and the importance of the thermal resistance type at small distances.

- Even if convection coefficient value is higher when the distance decreases, the base temperature values are higher since the area of the heat transfer and the number of the fins are decreased as shown in the Figure 3.6.

- If the LED chips are too close to each other (1 mm case), base temperature values exceed the maximum temperature of the LED chip, so it's not usable for the structure.
- By increasing the distance between the LED chips, thermal spreading enhances, and heat sources also enhances better. This situation leads to spread more heat and less base temperature of the structure.

3) LED Chips: Same Number, Same Power, Same Spacing, Different Layout The same number of the LED chip and different distribution (N_x and N_y) of the LED chips are used. Different base area structures generate same heat load. The distribution

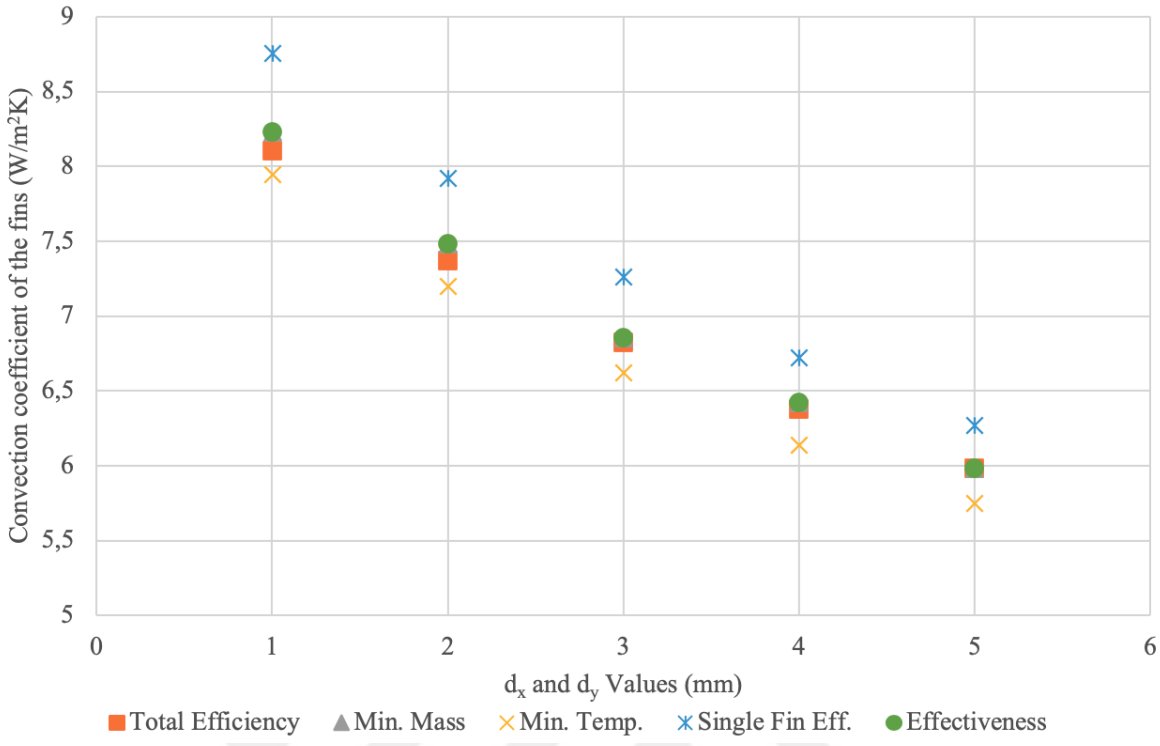


Figure 3.6. Convection coefficient of the fins vs. distance between the LED chips

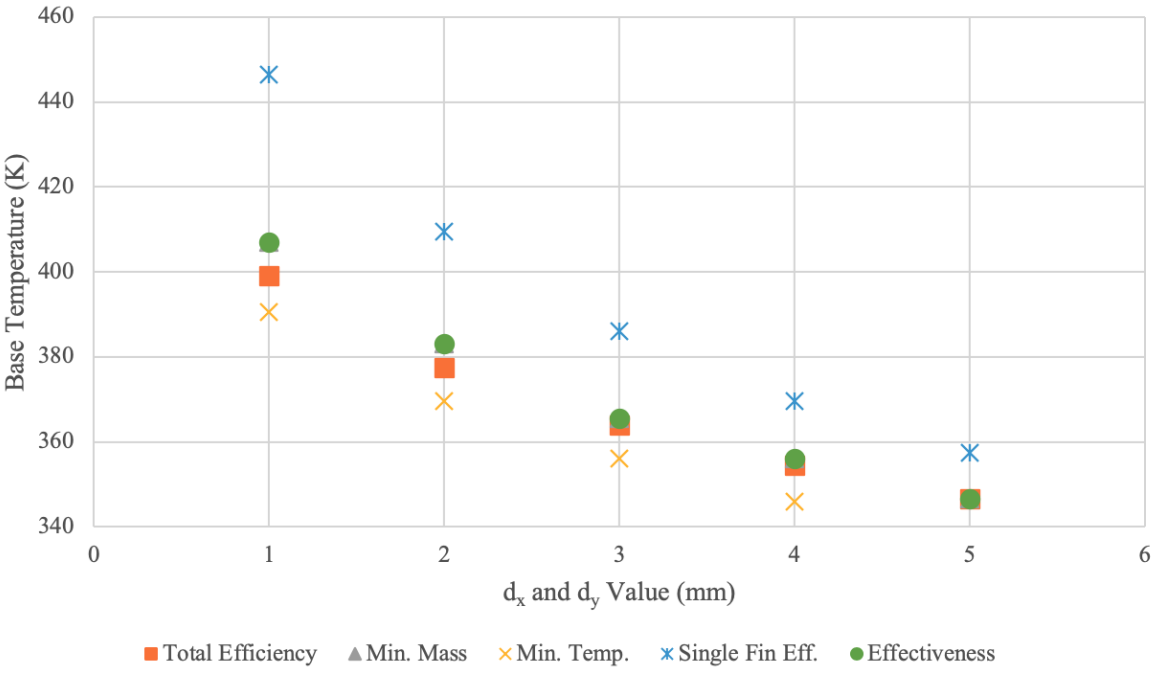


Figure 3.7. Base temperature vs. distance between LED chips

Table 3.3. Different configurations.

Configurations	N_x	N_y	W	L
1	48	5	269.6	29.25
2	24	10	138.8	56.5
3	16	15	95.2	83.75
4	12	20	73.4	111
5	10	24	62.5	132.8

values are shown in the Table 3.3. The following results are obtained:

- When we reduce the number of the chips in the y direction (N_y), W is increased, and L is decreased. In this case, n and $\bar{h}_{fin}$ increases due to optimum spacing. Thus, the heated air can leave the structure quickly and the base temperature are getting lower.

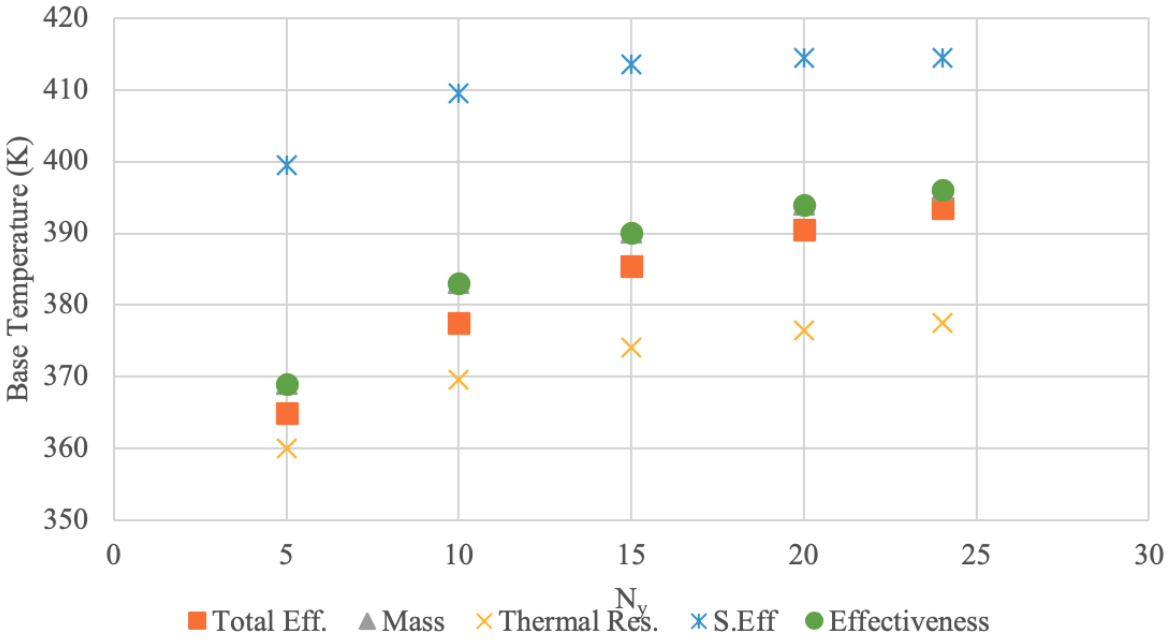


Figure 3.8. Base temperature vs. number of LED chip in y direction

- When we increase the number of the chips in y direction. The length of the fin is increased too much and the heated air cannot leave the structure quickly. This

behavior can be explained by thermal boundary layer as shown in the Figure 3.9. The temperature profile does not change after a certain length. Thus, the temperature does not decrease if the length of the fin is too high.

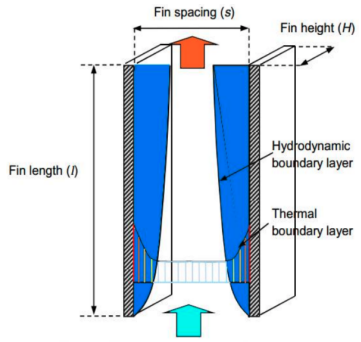


Figure 3.9. Thermal boundary layer [51]

4. JUNCTION TEMPERATURE ANALYSIS OF THERMALLY OPTIMIZED HIGH LUMEN LED ARRAY FIXTURES

In the 2^{nd} chapter, the junction temperature was estimated with temperature dependent thermal conductivities accurately. Then, the high lumen LED array optimization was done in the 3^{rd} chapter. However, no relationship has been established between two sections. In order to show the real effect of the optimizations which were done in the 3_{rd} chapter on the junction temperature, the results of the optimization are used in the package level model. Then, the result of the solder temperature from the package level model is applied to chip level model as a boundary condition. In the 3rd chapter, average base temperature value is obtained from the optimizations, but solder temperature is needed to use chip level model. There is two different way to find the solder temperature and then apply the solder temperature to the chip level model:

1) Find the junction temperature from the optimization result The thermal resistance of the printed circuit board (R_{bs}) is used as to find solder temperature and it's calculated as shown below:

$$R_{bs} = \frac{t_{PCB}}{k_{PCB} \times A} \tag{4.1}$$

where t_{PCB} is the thickness of the PCB, k_{PCB} is the thermal conductivity of the PCB, and A is the base area of the structure. In this structure, the thickness of the PCB is 1 mm and thermal conductivity of the PCB is 1 W/mK. The solder temperature is found with the following equation:

$$T_{solder} = T_{base} + R_{bs} \times \ Q_t \tag{4.2}$$

By using above equation, solder temperature is calculated from the base temperature which is obtained from optimization method in the Chapter 3. When the optimizations

Table 4.1. Junction temperature values of the chip level and package level model.

Optimization Type	Optimization	Calculated		Chip	Difference (K)
	T_{base}(K)	T_{solder} (K)	$T_{junction}$ (K)	$T_{junction}$ (K)	
Minimum Temperature (d_x=d_y=4 mm)	346	360	367.2	369.92	2.72
Minimum Temperature (d_x=d_y=2 mm)	369.5	394	401.2	405.08	3.88
Minimum Mass (d_x=d_y=2 mm)	383	407.48	414.68	419.03	4.35
Minimum Mass (d_x=d_y=4 mm)	356	370	377.2	380.26	3.06

are performed solder temperatures changed as in the third column of the Table 4.1. Thus, the solder temperatures in chip level model are varied and chip level simulations are performed to obtain the junction temperatures for each optimization step. These values are listed in the fourth column of the Table 4.1.

Chip level model estimated higher junction temperatures since it includes temperature dependent thermal conductivities. For the structure with the highest solder temperatures difference is approximately 4.35 K. Thus, using a chip level thermal model improves the junction temperature estimations. When the temperature decreases with the use of various optimization methods the difference between estimated junction temperatures decrease. For the final optimized structures for different priorities with the lowest solder temperature. This difference drops to 2.72 K.

2) Find the junction temperature with Multiscale Thermal Model by applying the optimization results All the parameters required to create an LED array can be obtained from the optimization method which is explained in the Chapter 3. To see the real effect of the optimizations, the LED array structure is generated with Multiscale Thermal Model using the result of the optimization method. The optimization results were shown in the Table 3.2 for a structure with input values are W=138.8 mm, L= 56.5 mm, and Q=192 W. The structure is created in the package level model for minimum

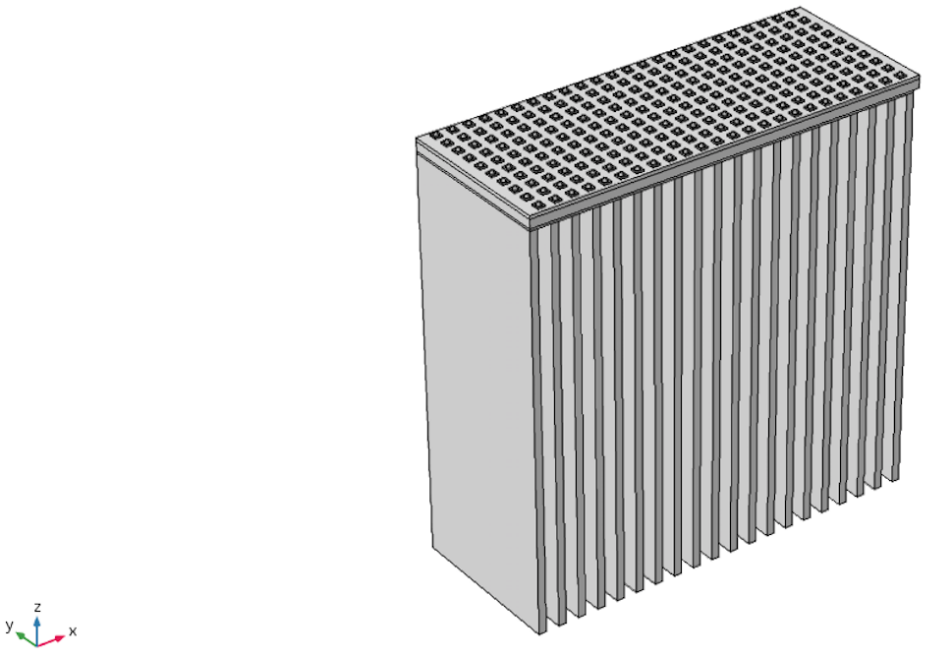


Figure 4.1. Package level model according to optimization result

temperature and minimum mass conditions as shown in the Figure 4.1.

- For minimum temperature case: The temperature distribution of the base area is shown in the Figure 4.2 and the base temperatures along the x-axis at the middle of the structure is shown in the Figure 4.3. Maximum solder temperature is obtained as 394 K, but the surface average temperature is obtained as 390 K. Average temperature is lower than the maximum temperature because the temperature distribution is not uniform in the package level model. In the middle of the LED array, the solder temperatures are higher due to the temperature effect of the chips on each other. The solder temperatures are lower at the outsides of the structure due to lower interaction between the chips.

- For other cases such as minimum mass, minimum temperature with d_x=d_y=4mm and minimum mass with d_x=d_y=4mm; the similar temperature distributions are obtained. However, the maximum and the surface average temperatures are different from each other. The results of these cases are shown in the Table 7.

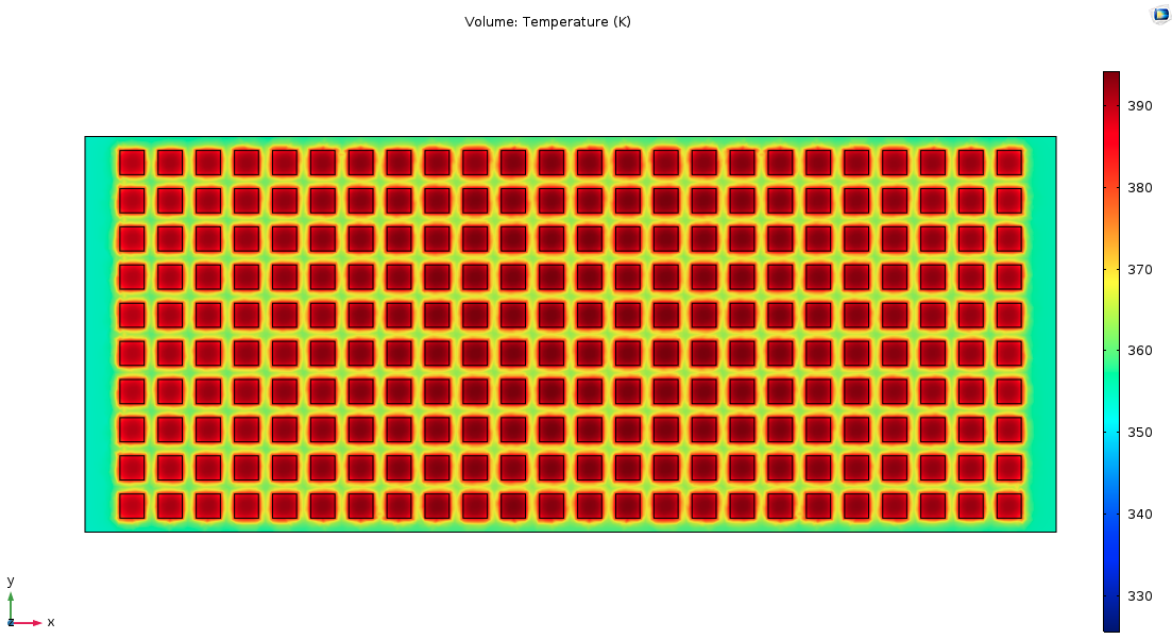


Figure 4.2. Temperature distribution of the solder with minimum temperature optimization

Average solder temperatures, maximum solder temperatures, and junction temperature results are shown in the Table 4.2. As seen in the table, the solder temperature in the optimization model as shown third column of the Table 4.2 is different from the solder maximum solder temperature result in the package level model. This situation is caused by the optimization model, the model finds the average base temperature. Thus, the solder temperature is quite similar to average solder temperature in the package level model as shown in the Table 4.2. Different solder temperatures are obtained using different optimization methods as shown in the Table 4.2. According to maximum solder temperature, junction temperatures are obtained in the chip level model according to these optimizations. Higher junction temperatures are obtained in the chip level model compared to the calculated junction temperature result.

For the structure with highest solder temperatures difference is approximately 5.68 K. Thus, using a chip level model improves the junction temperature estimation. When the temperature decreases with some optimizations, the difference between es-

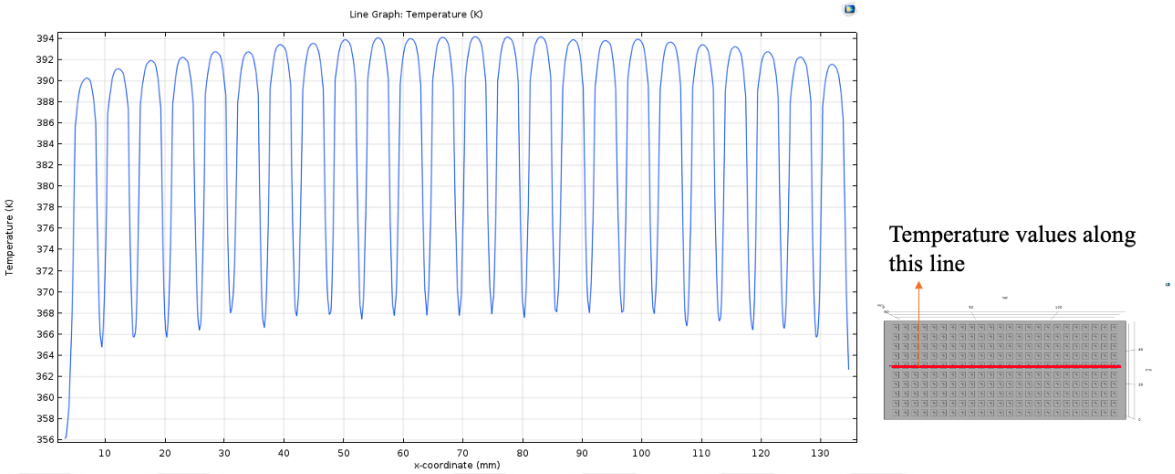


Figure 4.3. Solder temperature values along the x axis for minimum temperature optimization

Table 4.2. The junction temperature with Multiscale Thermal Model by applying the optimization results.

Optimization Type	Optimization result with Chip Level Model			Multiscale Thermal Model			Difference (K)
	Optimization Result		Chip Level	Package Level	Package Level	Chip Level (Max.)	
	T_{base} (K)	T_{solder} (K)	$T_{junction}$ (K)	Average solder (surface) temperature - T_{solder} (K)	Maximum Solder Temperature - T_{solder} (K)	$T_{junction}$ (K)	
Min. Temp. (d_x=d_y=2 mm)	369.5	394	405.08	392.63	397	408.19	3.11
Min. Temp. (d_x=d_y=4mm)	346	360	369.92	360.22	363.5	373.54	3.62
Min. Mass (d_x=d_y=2 mm)	383	407.48	419.03	408.67	412	424.71	5.68
Min. Mass (d_x=d_y=4mm)	356	370	380.26	371.65	374.5	384.79	4.53

timated junction temperatures decrease. For the minimum solder temperature, the difference drops to 2,84 K. This shows the temperature dependent conductivity importance at high temperatures and power outputs. Additionally, this situation indicates that thermal optimization is needed more at high lumen LED array structures.

5. CONCLUSION AND FUTURE WORKS

GaN based LED lights have been preferred in many fields such as roadways, buildings, and factories because they are good at energy efficiency, lifetime, and luminous flux. However, it has advantages, thermal problem is the main disadvantage of the LED technology. Heat generation is the main cause of this situation. In high lumen LED arrays generate high amount of heat and this causes elevated junction temperature which can decrease the lifetime and performance of the devices. Therefore, accurate characterization of the junction temperature and the thermal optimization in order to decrease the junction temperature are essential for designing high lumen LED array. Direct and precise measurement of the junction temperature was not possible with experimental and numerical methods. To estimate the junction temperature accurately, multiscale thermal model is developed in this work. Thermal model consists of two separate models which are package level and chip level model. Firstly, the package level model is investigated. Then, the information from the package level simulation is used as a boundary condition for a chip level simulation. Then, to improve the efficiency and save the LED chips thermal optimization is needed. Manufacturers can have variety of priorities such as minimum temperature and maximum efficiency while optimizing high lumen GaN LED array structures. To optimize the high lumen LED array structure, an optimization method is developed in the Chapter 3. This method needs only three input which are base width, length, the desired heat dissipation values, and the optimization type. According to these information, high lumen LED array structure values are obtained in 4 seconds with the optimization model. Finally, to observe the effect of these optimizations on the junction temperature, the optimization results were applied to the package level and chip level model. When temperature dependent thermal conductivities are used higher junction temperatures are obtained. The difference between junction temperatures obtained using constant Rj-s vs. the chip model with temperature dependent thermal conductivity is more than 5 K. This difference decreases as the device temperatures are reduced by proper optimization methods. For devices operating near their limit temperatures this difference can be important. Therefore, using temperature dependent thermal conductivity

and detailed model are important to obtain junction temperatures accurately and to see the effects of the optimization and make better thermal LED array design. Future research directions can be shown below:

- In the chip level model, which is located in the Multiscale Thermal Model, there is no electrical simulation and the heat generation was considered as uniform heat source. This situation can change the temperature distribution inside the chip. Thus, the electrical simulation can be applied to the chip level model structure to better estimation of the junction temperature.
- In the optimization model, the rectangular plate fin structure was used. However, there are some other fin types and these types have also similar analytic equations. Therefore, by using the other fin types, the optimization model can be developed more universally.
- Both package level model and optimization model, distances between all chips were used the same due to ease of production. However, the distance between the chips can be increased in the inner chips, where the temperatures are higher, and the distance can be reduced in other chips, where the temperatures are lower, to better array optimization.

REFERENCES

1. Zissis, G., *LEDs for Lighting Applications*, John Wiley and Sons, Inc., Hoboken, NJ, USA, 2010.

2. Baldwin, R., *50 Years of LED Technology*, 2012, `https://www.wired.com/2012/10/the-history-of-led`, Aug 2012.

3. Schubert, E. F., *Light-Emitting Diodes*, Cambridge University Press, Troy, NY, USA, 2006.

4. Holonyak, N. and S. F. Bevacqua, "Coherent (Visible) Light Emission From Ga(As1−xPx) Junctions", *Applied Physics Letters*, Vol. 1, No. 4, pp. 82–83, 1962.

5. Kückmann, O., "High-power LED arrays: special requirements on packaging technology", K. P. Streubel, H. W. Yao and E. F. Schubert (Editors), *Light-Emitting Diodes: Research, Manufacturing, and Applications X*, Vol. 6134, pp. 32 – 39, International Society for Optics and Photonics, SPIE, 2006.

6. Wikipedia, *Band Diagram*, 2020, `https://en.wikipedia.org/wiki/Band_diagram`, Last accessed on 2020-07-11.

7. Held, G., *Introduction to Light Emitting Diode Technology and Applications*, Auerbach Publications, Boca Raton, FL, USA, 2016.

8. Nguyen, X. L., T. N. N. Nguyen, V. T. Chau and M. C. Dang, "The fabrication of GaN-based light emitting diodes (LEDs)", *Advances in Natural Sciences: Nanoscience and Nanotechnology*, Vol. 1, No. 2, pp. 1–5, 2010.

9. Baillot, R. and Y. Deshayes, "Reliability Investigation of LED Devices for Public Light Applications", Elsevier, Kidlington, Oxford, UK, 2017.

10. Ban P. Loh, Peter Scott Andrews, Nicholas W. Medendorp, *Light emitting device packages, light emitting diode (LED) packages and related methods*, US Patent US20120223351A1, March 06 2007.

11. Schütt, E., *Thermal management and design optimization for a high power LED work light*, Ph.D. Thesis, Arcada University of Applied Sciences, 2014.

12. Tuan, C., Z. Lin, Y. Liu, K. Moon, S. Yoo, M. Jang and C. Wong, "Ultra-high refractive index LED encapsulant", *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, pp. 447–451, 2014.

13. Pust, P., V. Weiler, C. Hecht, A. Tücks, A. S. Wochnik, A.-K. Henß, D. Wiechert, C. Scheu, P. J. Schmidt and W. Schnick, "Narrow-band red-emitting Sr[LiAl3N4]:Eu2+ as a next-generation LED-phosphor material", *Nature Materials*, Vol. 13, No. 9, pp. 891–896, 2014.

14. Narendran, N., Y. Gu and R. Hosseinzadeh, "Estimating junction temperature of high-flux white LEDs Estimating Junction Temperature of High-Flux White LEDs", *Light-Emitting Diodes: Research, Manufacturing, and Applications VIII*, Vol. 5366, pp. 1–3, 2004.

15. Cree, *Cree ® XLamp ® XP-G3 LEDs Product Description*, 2016, `https://www.cree.com/led-components/media/documents/dsXPG3.pdf`, Last accessed on 2020-07-07.

16. Ye, H. and G. Zhang, "A review of passive thermal management of LED module", *Journal of Semiconductors*, Vol. 32, No. 1, pp. 1–4, 2011.

17. Wang, J., X. jie Zhao, Y. Cai, C. Zhang and W.-W. Bao, "Experimental study on the thermal management of high-power LED headlight cooling device integrated with thermoelectric cooler package", *Energy Conversion and Management*, Vol. 101, pp. 532–540, 2015.

18. Philips-Lumileds, *How to measure thermal resistance of light emitting diodes emitters and LED Arrays*, 2016, https://www.ee.co.za/article/measure-thermal-resistance-led-emitters-led-arrays.html, Last accessed on 2020-07-11.

19. Cree, *Cree ® XLamp ® XP-E LEDs Product Description*, 2008, https://www.cree.com/led-components/media/documents/XLampXPE.pdf, Last accessed on 2020-07-13.

20. Cree, *Thermal Management of Cree ® XLamp ® LEDs*, 2004, https://www.cree.com/led-components/media/documents/XLampThermalManagement.pdf, Last accessed on 2020-07-18.

21. Narendran, N. and Y. Gu, "Life of LED-Based White Light Sources", *Journal of Display Technology*, Vol. 1, No. 1, pp. 167–177, Sep 2005.

22. Lumileds Holding B.V, *Understanding power LED lifetime analysis*, 2007, http://www.climateaction.org/images/uploads/documents/Philips_Understanding-Power-LED-Lifetime-Analysis.pdf, Last accessed on 2020-08-18.

23. Liu, S., J. Yang, Z. Gan and X. Luo, "Structural optimization of a microjet based cooling system for high power LEDs", *International Journal of Thermal Sciences*, Vol. 47, No. 8, pp. 1086 – 1095, 2008.

24. EAE Aydınlatma, *GPRONA Aydınlatma Armatürü*, 2020, https://www.eaeaydinlatma.com/tr/urun, Last accessed on 2020-06-09.

25. Xi, Y., T. Gessmann, J. M. Shah, J. K. Kim, E. F. Schubert, A. J. Fischer, M. H. Crawford, K. H. A. Bogart and A. A. Allerman, "Junction and carrier temperature measurements in deep-ultraviolet light-emitting diodes using three different methods", *Applied Physics Letters*, Vol. 86, No. 3, pp. 1–8, 2005.

26. Tamdogan, E., G. Pavlidis, S. Graham and M. Arik, "A Comparative Study on the Junction Temperature Measurements of LEDs With Raman Spectroscopy, Microinfrared (IR) Imaging, and Forward Voltage Methods", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 8, No. 11, pp. 1914–1922, 2018.

27. Lee, C. C. and Jeong Park, "Temperature measurement of visible light-emitting diodes using nematic liquid crystal thermography with laser illumination", *IEEE Photonics Technology Letters*, Vol. 16, No. 7, pp. 1706–1708, 2004.

28. Christensen, A. and S. Graham, "Thermal effects in packaging high power light emitting diode arrays", *Applied Thermal Engineering*, Vol. 29, No. 2, pp. 364 – 371, 2009.

29. Ha, M. and S. Graham, "Development of a thermal resistance model for chip-on-board packaging of high power LED arrays", *Microelectronics Reliability*, Vol. 52, No. 5, pp. 836 – 844, 2012.

30. Han, B., C. Jang, A. Bar-Cohen and B. Song, "Coupled Thermal and Thermo-Mechanical Design Assessment of High Power Light Emitting Diode", *IEEE Transactions on Components and Packaging Technologies*, Vol. 33, No. 4, pp. 688–697, 2010.

31. Hu, J., L. Yang and M. W. Shin, "Thermal and Mechanical Analysis of High-Power LEDs With Ceramic Packages", *IEEE Transactions on Device and Materials Reliability*, Vol. 8, No. 2, pp. 297–303, 2008.

32. Long, X.-M., R.-J. Liao and J. Zhou, "Numerical Simulation on Electrical-Thermal Properties of Gallium-Nitride-Based Light-Emitting Diodes Embedded in Board", *Advances in Optoelectronics*, Vol. 2012, pp. 1–6, 2012.

33. Ha, M. S., *Thermal Analysis of High Power LED Arrays*, Ph.D. Thesis, Georgia Institute of Technology, Nov. 2009.

34. Li, J., B. Ma, R. Wang and L. Han, "Study on a cooling system based on thermoelectric cooler for thermal management of high-power LEDs", *Microelectronics Reliability*, Vol. 51, No. 12, pp. 2210 – 2215, 2011.

35. Lu, X.-Y., T.-C. Hua and Y.-P. Wang, "Thermal analysis of high power LED package with heat pipe heat sink", *Microelectronics Journal*, Vol. 42, No. 11, pp. 1257 – 1262, 2011.

36. Deng, Y. and J. Liu, "A liquid metal cooling system for the thermal management of high power LEDs", *International Communications in Heat and Mass Transfer*, Vol. 37, No. 7, pp. 788 – 791, 2010.

37. Feng, S., M. Shi, H. Yan, S. Sun, F. Li and T. J. Lu, "Natural convection in a cross-fin heat sink", *Applied Thermal Engineering*, Vol. 132, pp. 30 – 37, 2018.

38. An, X., M. Arora, W. Huang, I. Paul, W. C. Brantley and F. Hassanipour, "Numerical analysis of rectangular channel heat sink performance for supercomputing applications", *Second Thermal and Fluids Engineering Conference*, pp. 141–148, 2018.

39. Taler, D., "Mathematical modeling and control of plate fin and tube heat exchangers", *Energy Conversion and Management*, Vol. 96, pp. 452 – 462, 2015.

40. Bar-Cohen, A. and M. Jelinek, "Optimum Arrays of Longitudinal, Rectangular Fins in Corrective Heat Transfer", *Heat Transfer Engineering*, Vol. 6, No. 3, pp. 68–78, 1985.

41. Elenbaas, W., "The Dissipation of Heat by Free Convection from Vertical and Horizontal Cylinders", *Journal of Applied Physics*, Vol. 19, No. 12, pp. 1148–1154, 1948.

42. H.R.Goshayeshi, M. inia and M.M.Naserian, "Numerical Modeling of Natural Convection on Various Configuration of Rectangular Fin Arrays on Vertical Base

Plates", *International Journal of Mechanical and Mechatronics Engineering*, Vol. 5, No. 1, pp. 90 – 96, 2011.

43. Walunj, A., V. Daund and D. D. Palande, "Parametric Analysis of Plate-Fin Heat Sink Over Heat Transfer", *International Journal of Research in Advent Technology*, Vol. 1, No. 4, pp. 80 – 89, 2013.

44. Patel, H. and V. K. Matawala, "Performance Evaluation and parametric optimization of a Heat Sink for Cooling of Electronic Devices with Entropy Generation Minimization", *European Journal of Sustainable Development Research*, Vol. 3, No. 4, pp. 1–20, 2019.

45. Yüncü, H. and G. Anbar, "An experimental investigation on performance of rectangular fins on a horizontal base in free convection heat transfer", *Heat and Mass Transfer*, Vol. 33, pp. 507–514, 1998.

46. Bar-Cohen, A., M. Iyengar and A. D. Kraus, "Design of optimum plate-fin natural convective heat sinks", *Journal of Electronic Packaging, Transactions of the ASME*, Vol. 125, No. 2, pp. 208–216, 2003.

47. Hongyu Tang, Dongzhe Li, Meng Pan, Tong Yang, Cadmus Yuan and Xuejun Fan, "Thermal analysis and optimization design of LED streetlight module", *2013 10th China International Forum on Solid State Lighting (ChinaSSL)*, pp. 193–197, 2013.

48. Bing, L. Y., "On Thermal Structure Optimization of a Power LED Lighting", *Procedia Engineering*, Vol. 29, pp. 2765 – 2769, 2012.

49. Hsieh, C. C. and Y. H. Li, "The study for saving energy and optimization of led street light heat sink design", *Advances in Materials Science and Engineering*, Vol. 2015, pp. 1–6, 2015.

50. Huang, Y., S. Shen, H. Li and Y. Gu, "Improved thermal design of fin heat sink for

high-power LED lamp cooling", *2016 17th International Conference on Electronic Packaging Technology (ICEPT)*, pp. 1069–1074, 2016.

51. Incropera, F. P., *Fundamentals of Heat and Mass Transfer*, John Wiley and Sons, Hoboken, NJ, USA, 2006.

52. EAE Lighting, *EAE Aydınlatma — Işık Mühendisliği*, 2020, `https://www.eaeaydinlatma.com/tr-tr/`, Last accessed on 2020-08-09.

53. EAE Lighting, *GPRONA Lighting Armature*, 2020, `https://eaelighting.com/en/product/gprona-v-2-p1526`, Last accessed on 2020-08-11.

54. CREE, *Cree® EZ1000-n^{TM} Gen 2 LEDs Data Sheet (Cathode-up)*, 2010, `https://www.cree.com/led-chips/media/documents/CPR3EC.pdf`, Last accessed on 2020-08-09.

55. Paskov, P. P., M. Slomski, J. H. Leach, J. F. Muth and T. Paskova, "Effect of Si doping on the thermal conductivity of bulk GaN at elevated temperatures – theory and experiment", *AIP Advances*, Vol. 7, No. 9, pp. 1–15, 2017.

56. Jeżowski, A., B. Danilchenko, M. Boćkowski, I. Grzegory, S. Krukowski, T. Suski and T. Paszkiewicz, "Thermal conductivity of GaN crystals in 4.2–300 K range", *Solid State Communications*, Vol. 128, No. 2, pp. 69 – 73, 2003.

57. Su, Z., J. A. Malen, J. H. Melby and R. F. Davis, "Thermal Transport in LEDs for Solid State Lighting", *ASME/JSME 2011 8th Thermal Engineering Joint Conference*, pp. 1–5, ASME, 2011.

58. Elenbaas, W., "Heat dissipation of parallel plates by free convection", *Physica*, Vol. 9, No. 1, pp. 1 – 28, 1942.

59. Lee, H., *Thermal Design; Heat Sinks, Thermoelectrics, Heat Pipes, Compact Heat Exchangers, and Solar Cells*, John Wiley and Sons, Hoboken, NJ, USA, 2010.

60. Kraus, A., A. Aziz and J. Welty, *Extended Surface Heat Transfer*, Wiley, New York, NY, USA, 2002.

61. Cengel, Y. A. and G. Afshin, *Heat and Mass Transfer: Fundamentals & Applications*, McGraw-Hill, New York, NY, USA, 2006.