NOVEL POSITIVE AND NEGATIVE ACTIVE INDUCTOR CIRCUIT DESIGNS

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I could have never imagined that what it would be like to write a thesis during a pandemic but it is what happened to me. The last two years have been quite challenging for me and all people around the world. I hope that we will get over the pandemic soon and return our normal life as before.

ABSTRACT

NOVEL POSITIVE AND NEGATIVE ACTIVE INDUCTOR CIRCUIT DESIGNS

Inductor is one of the main passive elements in electronics. It has a significant role in designs and are being used in electrical circuits widely. However, physical inductors have considerable drawbacks which limit their usage in low scale such as on-chip large die area consumption and magnetic filed creation. As an alternative solution, circuits that partly shows inductive behavior have been started to be proposed over the last decades. This types of proposed circuits could be seperated in two categories: grounded and floating active inductor circuits. Grounded active inductors are not as desirable as floating type of active inductors due to the fact that one the input ports should be grounded. Therefore, usage of the grounded active inductors is severely limited. On the other hand, floating inductors could possibly replace a passive inductor in any application, which makes them appealing.

In this work, floating type positive and negative active inductor circuits are presented and their mathematical and simulation results are shared. In addition, the effect of the parasitic components of the devices on the behavior of the circuit is examined. In order to show the circuits' usability, application instances and their results are shared and they are compared to a situation where an ideal inductor is employed. Overall, it could be said that the proposed circuits partly show inductive behavior over a limited frequency band.

ÖZET

ÖZGÜN POZİTİF VE NEGATİF AKTİF İNDÜKTÖR DEVRE TASARIMLARI

Elektronik biliminde indüktör birincil pasif devre elemanlarından biridir. Bu eleman devre tasarımlarında önemli bir yer tutar ve elektrik devrelerinde geniş kullanım alanları vardır. Fakat, fiziksel indüktörler çip üzerinde geniş alan tüketimi ve manyetik alan oluşturma gibi düşük ölçek kullanımlarını sınırlayan önemli dezavantajlar barındırmaktadır. Alternatif bir çözüm olarak, geçen on yıllarda kısmen indüktif davranış gösteren devreler sunulmaya başlanmıştır. Bu tip devreler iki ana grup altında toplanabilirler: topraklanmış ve yüzen aktif indüktör devreleri. Topraklanmış aktif indüktör devreleri bir giriş bağlantılarının topraklanmış olması gerektiğinden yüzen aktif indüktör devreleri kadar arzulanmamaktadır. Bu yüzden topraklanmış aktif indüktör devrelerinin kullanımı şiddetli bir şekilde kısıtlanmıştır. Diğer tarafta, yüzen aktif indüktör devreleri istenilen herhangi bir uygulamada pasif indüktör yerine kullanılabilir ve bu sebepten dolayı bu tip indüktör devreleri çekicidir.

Bu çalışmada, yüzen tip positif ve negatif aktif indüktör devreleri sunulmuştur ve bunların matematiksel ve simülasyon sonuçları paylaşılmıştır. Ek olarak, devredeki cihazların parazitik elemanlarının devre davranışı üzerindeki etkisi incelenmiştir. Devrelerin kullanılabilirliğinin gösterilmesi için kullanım örnekleri ve bunların sonuçları paylaşılmıştır ve bu sonuçlar ideal indüktör kullanım durumuyla karşılaştırılmıştır. Toparlanacak olursa, sunulan devrelerin belirli bir frekans aralığında kısmen indüktör davranışı gösterdiği söylenebilir.

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LIST OF SYMBOLS

C_{gs}	Gate to source capacitance of the MOSFET
C_{gd}	Gate to drain capacitance of the MOSFET
f_{c}	Cutoff frequency of the filter
$f_{\mathrm{max(Z_{eq})}}$	Frequency that maximum value of the input impedance of the circuit is determined
$f_{\mathrm{op.}}$	Operating frequency of the circuit
$f_{\mathrm{Q_{max}}}$	Frequency that maximum Q value is measured
g_{ds}	Drain to source channel conductance of the MOSFET
g_{m}	Transconductance of the MOSFET
$\mathrm{I_D}$	DC drain to source current of the MOSFET
i_{inpp}	Peak to peak small signal input current of the circuit
L	Channel length of the MOSFET
$L_{\mathrm{app.}}$	Approximated inductance value of the circuit
$L_{\mathrm{sim.}}$	Simulated inductance value of the circuit
L_{x}	Inductance of the circuit according to the ideal analysis results
$\max(Z_{\mathrm{eq}})$	Maximum value of the input impedance of the circuit
$\min(Z_{\mathrm{eq}})$	Minimum value of the input impedance of the circuit
Q	Quality factor of the circuit
Q_{max}	Maximum Q value of the circuit
V_1, V_2	Input connection ports of the circuit
v_1, v_2	Input connection ports of the AC equivalent circuit
V_{DD}	Positive supply voltage
v_{gs}	Gate to source small signal voltage of the MOSFET
v_{inpp}	Peak to peak input voltage of the circuit (realized as a result of i_{inpp})
V_{os}	Input offset voltage of the circuit
V_{SS}	Negative supply voltage
W	Channel width of the MOSFET

Y_{eq}	Input admittance of the circuit
Y_{id}	Input admittance of the circuit when the matching condition of the circuit is not full-filled
Z_{eq}	Input impedance of the circuit

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
AI	Active Inductor
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal–Oxide–Semiconductor
DC	Direct Current
IC	Integrated Circuit
JFET	Junction-Gate Field-Effect Transistor
LNA	Low-Noise Amplifier
LP	Low-Pass
LPF	Low-Pass Filter
MOS	Metal–Oxide–Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
NAI	Negative Active Inductor
PMOS	P-type Metal-Oxide-Semiconductor
TF	Transfer Function
TSMC	Taiwan Semiconductor Manufacturing Company
VAPAR	Variable Active-Passive Reactance
VCCS	Voltage Controlled Current Source

1. INTRODUCTION

1.1. Overview

Imitation of high value assets, especially for the rare ones, have always been a matter with high importance to humans. For instance, through out the history, humans have been quite interested in turning base metals into gold. The topic was so popular that people assumed that there was a stone that called Philosopher's Stone, which was able to carry out the metal transformation process and Alchemists were the ones that were interested in the subject. Unfortunately, such process never came to realization yet this particular case does not mean that different types of imitations cannot be achieved. It has only been a very short period of time that we, as humans, really are interested in electronics. However, the development speed in this scientific area is fascinating. Yet, the first transistor was presented in the 20^{th} century and was more than thousand times bigger than recent transistors, today almost everybody has billions of transistors in their pockets and there is almost no place that an electronics component is not being presented. Every year new electronic gadgets are presented with new properties and it has become normal that people expect better products, which are in some ways better than their older counterparts. These expectations drive scientists and engineers to come up with new inventions that enable developments in technology. Electronic components are grouped in two categories: active and passive elements. Active elements defined as the elements that supply energy to the system. On the other hand, passive elements said to be consume energy in the system. Compared to transistors, passive electronic components are in general large and sometimes producing a passive component precisely with a low value is challenging. To overcome these issues people started to create virtual passive components, i.e., they create an element that in some way it acts as it was a specified passive component. For example, the resistance value from a MOSFET's channel can be utilized instead of a real resistor when transistor in active region, at the same time, it is possible to use parasitic capacitance of a MOSFET -C_{gs}- instead of a real capacitor. This imitation process of

the circuit elements is quite important for one particular passive circuit component: inductor.

1.2. MOS Only Circuits

Transistor family includes many electronic devices with different working principle and character. Each element's importance and popularity have changed from time to time. For instance, in the very beginning, vacuum tubes were used for amplification process, then JFETs became popular and replaced the vacuum tubes and for the last decades MOSFETs have become an outstanding member of the transistor family. Low supply voltage and power are favored in electronics because it improves quality of the products. Therefore, to meet this demand, over the time, MOSFETs got steadily smaller and their quality improved. Designs that contains abundant amount of MOSFETs along with other circuit components are called "Integrated Circuits." Technological improvements on MOSFETs affected ICs and they got smaller too. However, at some point, the improvements that were made on MOSFETs did not start to yield expected results and other restrictions started to dominate the performance. Some of these restrictions are the presence of real resistor and capacitors. Resistors and capacitors are utilized frequently in electronic circuits and almost no circuit exist without them. However, real resistors and capacitors have some real drawbacks. For instance, they occupy an important space in a chip and they could limit operation frequency. To overcome these issues, MOSFETs are utilized to achieve a resistance and capacitance value. [1] has discussed about implementing frequency selective circuits with MOS only circuits. The parasitic capacitance, C_{gs}, and MOS channel resistance, g_{m}, were utilized, where a capacitor and a resistor were need. As a result, reduced chip area and operation at high frequencies are presented as some of the benefits of using the MOS only design technique.

1.3. Active Inductors

Inductors are one of the passive circuit elements and they are utilized frequently in filter designs. However, a real inductor is a problematic element when used in ICs because, first, it is hard to realize and, second, it is lossy. An inductor consumes an important amount of space on a chip while it does not yield a high inductance value and quality factor. An alternative way to realize an inductance value is to implement so-called active inductor. Active inductors do not fully achieve an inductor's properties, they only simulate the inductor, i.e., they yield an inductance value but, for instance, they cannot store energy in the form of magnetic field. [2] presented many basic active inductors. Active inductors have some outstanding properties over real inductors. For instance, they consume very small area, their quality factor is very high, the inductance value can be tuned and they allow for high frequency operation.

In this work, six active inductor circuits are presented. The design procedure of the circuits are explained in detail in each chapter. Multiple types of simulations are run to test the circuits and the transistor parameters that are used in simulations are shared for the people's interest in APPENDIX A. It is seen that the presented active inductor circuits are working well and they meet the expectations. Along with their compelling qualities, these circuits have several drawbacks such as noise and heat dissipation. Nevertheless, it is thought that the advantages of the proposed circuits shadow their disadvantages and could possibly be utilized as alternatives to the passive inductors in case of a need.

2. A NOVEL MOS ONLY TYPE FLOATING INDUCTOR

This chapter presents a novel floating type active inductor based on MOS-Only technique. The circuit is analyzed from considering nonidealities and various comparisons are made in order to quantify the circuit's functionality. 0.18 μm TSMC MOS technology has been used for transistor realization. Overall, the circuit meets expectations and shows promising results and consumes only 380-μW power under 3.3 V supply voltage.

2.1. Introduction

MOS-Only circuits have received significant attraction in the past decades because of various advantages over other circuitries that used to perform the same or a similar task [2 - 4]. Inductors are essential when implementing filters, oscillators, LNAs and many other important circuitries. Passive inductors are not compelling circuit elements for real life usage because of many disadvantages that they own. In real life utilization, active inductors can be considered as a solution for the problem. Although the term "active inductor" is widely used in the literature the correct description is perhaps active realization of the inductor since the inductor itself is a passive element. In this context with active inductor we mean its realization. They usually offer high quality factor, occupy low area on a chip, tunability, high operation frequency [5 - 7]. However, some of the active inductor designs that were proposed in the past are either single-ended or suffer from various drawbacks such as high power consumption and low inductance value [8, 9]. Floating type of active inductor circuits are more versatile since they can also be used in grounded configurations. In this chapter a novel floating active inductor is proposed. The simplest form of the proposed active inductor circuit employs three transistors, which leads to a low power consumption. Plus, all of the transistors in the proposed circuit are n-channel MOSFETs, which is an important performance boost. Starting from an initial core circuit, the design is made step by step by biasing the core and hence adding an additional transistor. The proposed final

active inductor circuit employs only four transistors and meets the expectations.

2.2. A Novel Floating Active Inductor

Passive inductors are not charming elements in circuit applications because of their obvious problems [10]. Therefore, using them on a chip is not favorable in many applications. On the other hand, active inductors are able to overcome some of important shortcomings of passive inductors as mentioned in [11]. A novel active inductor circuit is proposed in this chapter and it shows promising performance in an application.

2.2.1. The Structure and Ideal Analysis of the Circuit

The basic form of the first proposed floating AI circuit is shown in Fig. 2.1 and it only has three transistors. Replacing the MOS transistor with its small signal model one can show that the admittance matrix of this two port has the following form

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sL_{\mathrm{x1}}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{2.1}$$

which validates that this circuit is a simulated inductor with the inductance value of L_{x1}. The ideal analysis of the circuit is carried out considering the transistor as a voltage controlled current source and taking the transconductances of the transistors into account but ignoring parasitics of the MOSFET such as C_{gs}, C_{gd} and g_{ds}. According to the routine analysis results, the inductance value that the circuit realizes is found to be as following

$$L_{\mathrm{x1}} = \frac{C(g_{m2} + g_{m3})}{g_{m1}g_{m2}g_{m3}}. \tag{2.2}$$

It is seen that the realized inductance value is dependent on C, g_{m1}, g_{m2} and g_{m3}. By changing the value of one or more of these parameters, the inductance value can be

modified. Therefore, it is said that the inductance is tunable. It is seen that, this circuit can replace a passive inductor and it has important advantages over its passive counterpart such as tunability of inductor and low space consumption. An important point that should be mentioned in Fig. 2.1 is that the arrows in the figure indicate the sources of the transistors, but not the type of the transistor so, the transistor can be either n-channel or p-channel type. This is because the small signal equivalent model of both n-channel and p-channel transistors are identical. The circuit should be biased properly so that the ideal AC model could fit to the presented circuit.

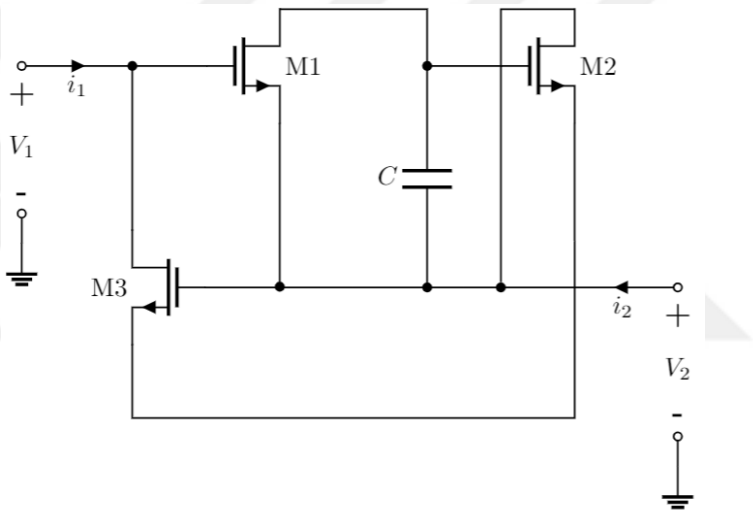


Figure 2.1. Active inductor circuit without bias.

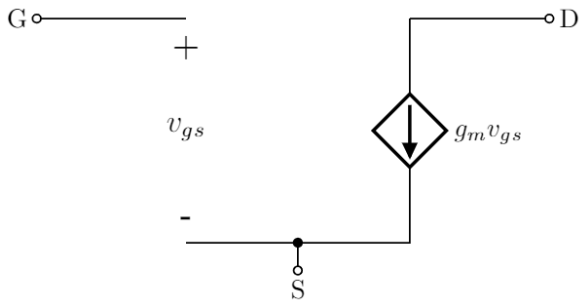


Figure 2.2. AC equivalent of the ideal MOSFET.

2.2.2. Nonideal Analysis of the Active Inductor Circuit

In section 2.2.1, ideal analysis of the circuit was performed. In ideal analysis, ideal AC equivalent of the MOSFET were utilized, where a transistor is replaced by a VCCS as shown in Fig. 2.2. In non-ideal analysis, parasitic elements of the MOSFET are taken into account. The parasitic elements that are taken into account are C_{gs}, C_{gd} and g_{ds} and they are shown in Fig. 2.3. The non-ideal analysis is carried out in order to understand the deviations from ideal behavior of the circuit at extreme frequencies. It is thought that drawing non-ideal equivalent circuit of the presented circuit might give some information about the circuit. Hence, non-ideal equivalent circuit of the active inductor is drawn and could be observed in Fig. 2.4.

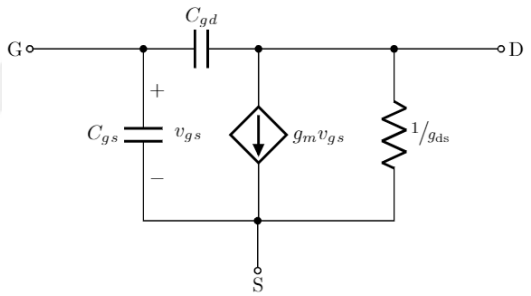


Figure 2.3. AC equivalent of the non-ideal MOSFET, with parasitic elements.

The admittance matrix of the circuit was given previously in Equation (2.1) and it has four elements. Now, since the admittance matrix is present, it is straightforward to calculate the admittance of the circuit. The input admittance of the circuit equals, I_1/V_1 while V_2 is grounded. Equations (2.3) and (2.4) present together admittance expression of the circuit, where the last subscript of the terms denote the number of the transistor. In the expressions to come some simplifications are made. For instance, C_{gd2} and C_{gd3} are omitted because they are parallel to C_{gs1} and C respectively and it is assumed that they are quite inferior when compared to the big capacitors. In addition, since C_{gs3} and g_{ds2} are parallel, they are denoted as y_{13} (one impedance component).

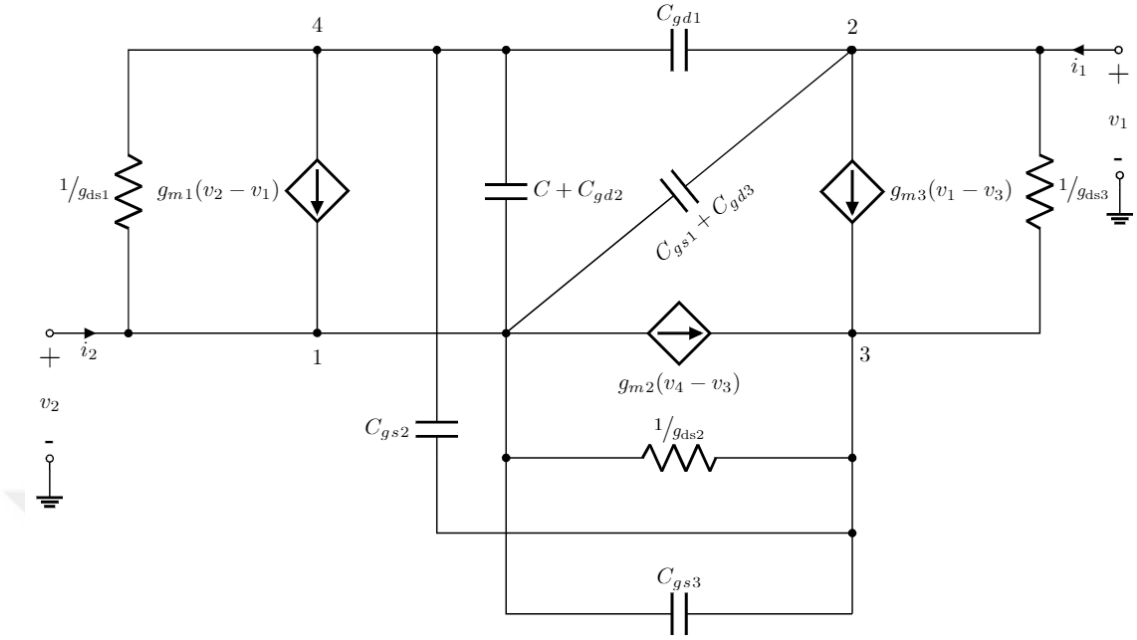


Figure 2.4. Non-ideal equivalent circuit of the active inductor.

Following the routine analysis, the admittance of the circuit could be expressed as

$$Y_{\text{eq1}} = \frac{m_3 s^3 + m_2 s^2 + m_1 s + m_0}{n_2 s^2 + n_1 s + n_0}, \tag{2.3}$$

where coefficients are shown as follows

$$m_3 = C_{\text{gs2}}(C_{\text{gd1}}C_{\text{gs1}} + C(C_{\text{gs1}} + C_{\text{gd1}})) \tag{2.4a}$$

$$\begin{aligned} m_2 = {} & CC_{\text{gs2}}g_{\text{ds3}} + C_{\text{gs1}}C_{\text{gs2}}(g_{\text{ds1}}g_{\text{ds3}}g_{\text{m3}} - y_{13}) \\ & + CC_{\text{gs1}}(g_{\text{ds3}} + g_{\text{m2}} + g_{\text{m3}} - y_{13}) \\ & + C_{\text{gd1}}(C + C_{\text{gs1}})(g_{\text{ds3}} + g_{\text{m2}} + g_{\text{m3}} - y_{13}) \\ & + C_{\text{gd1}}C_{\text{gs2}}(g_{\text{ds1}} + g_{\text{m1}} + y_{13}) \end{aligned} \tag{2.4b}$$

$$\begin{aligned} m_1 = {} & C_{\mathrm{gs2}}g_{\mathrm{ds1}}g_{\mathrm{ds3}} + C_{\mathrm{gs2}}g_{\mathrm{ds3}}g_{\mathrm{m1}} + Cg_{\mathrm{ds3}}g_{\mathrm{m2}} + Cg_{\mathrm{ds3}}g_{\mathrm{m2}} + C_{\mathrm{gs2}}g_{\mathrm{m1}}g_{\mathrm{m3}} \\ & + C_{\mathrm{gs1}}g_{\mathrm{ds1}}(g_{\mathrm{ds3}} + g_{\mathrm{m2}} + g_{\mathrm{m3}} - y_{13}) + Cg_{\mathrm{ds3}}y_{13} + C_{\mathrm{gs2}}g_{\mathrm{ds3}}y_{13} - 2C_{\mathrm{gs2}}g_{\mathrm{m1}}y_{13} \\ & + C_{\mathrm{gd1}}(g_{\mathrm{m1}}g_{\mathrm{m2}} + g_{\mathrm{m1}}g_{\mathrm{m3}} - g_{\mathrm{m2}}g_{\mathrm{m3}} + g_{\mathrm{ds1}}(g_{\mathrm{ds3}} + g_{\mathrm{m2}} + g_{\mathrm{m3}} - y_{13}) \\ & - g_{\mathrm{m1}}y_{13} + 2g_{\mathrm{m2}}y_{13} + g_{\mathrm{ds3}}(g_{\mathrm{m1}} + y_{13})) \end{aligned} \tag{2.4c}$$

$$m_0 = g_{\mathrm{m1}}g_{\mathrm{m2}}(g_{\mathrm{ds3}} + g_{\mathrm{m3}} - 2y_{13}) + g_{\mathrm{ds1}}g_{\mathrm{ds3}}(g_{\mathrm{m2}} + y_{13}) \tag{2.4d}$$

$$n_2 = C_{\mathrm{gs2}}(C + C_{\mathrm{gd1}}) \tag{2.4e}$$

$$n_1 = C_{\mathrm{gs2}}(g_{\mathrm{ds1}} + g_{\mathrm{ds3}} + g_{\mathrm{m3}} - y_{13}) + (C + C_{\mathrm{gd1}})(g_{\mathrm{ds3}} + g_{\mathrm{m2}} + g_{\mathrm{m3}} - y_{13}) \tag{2.4f}$$

$$n_0 = g_{\mathrm{ds1}}(g_{\mathrm{ds3}} + g_{\mathrm{m2}} + g_{\mathrm{m3}} - y_{13}). \tag{2.4g}$$

The resulted expression is quite complicated. Moreover, it would be better to have impedance expression rather than admittance because with impedance expression magnitude response of the circuit could be observed. Therefore, impedance expression is obtained by inversing admittance. However, it is seen that the resulted expression is quite complicated. In order to simplify matters a first order approximation is applied. Hence, any term containing a product of two or more parasitic elements are omitted. All terms with a single parasitic element remains but in order to preserve high order term's presence, s^3 terms with two parasitic elements are allowed at most. Element y_{13} is replaced C_{gs3} and g_{ds2}. The simplified expression for impedance expression could be observed in following

$$Z_{\mathrm{eq1}} = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}, \tag{2.5}$$

where coefficients could be observed through

$$a_2 = C(C_{\mathrm{gs2}} - C_{\mathrm{gs3}}) \tag{2.6a}$$

$$a_1 = C_{\mathrm{gs2}}g_{\mathrm{m3}} + C_{\mathrm{gd1}}(g_{\mathrm{m2}} + g_{\mathrm{m3}}) + C(g_{\mathrm{m2}} + g_{\mathrm{m3}} + g_{\mathrm{ds3}} - g_{\mathrm{ds2}}) \tag{2.6b}$$

$$a_0 = g_{\mathrm{ds1}}(g_{\mathrm{m2}} + g_{\mathrm{m3}}) \tag{2.6c}$$

$$b_3 = C(C_{\mathrm{gs1}} + C_{\mathrm{gd1}})(C_{\mathrm{gs2}} - C_{\mathrm{gs3}}) \tag{2.6d}$$

$$b_2 = C(g_{m2} + g_{m3})(C_{gs1} + C_{gd1}) \tag{2.6e}$$

$$b_1 = Cg_{ds3}g_{m2} - 2C_{gs3}g_{m1}g_{m2} + C_{gs2}g_{m1}g_{m3} + C_{gd1}(g_{m1}g_{m2} + g_{m1}g_{m3} - g_{m2}g_{m3}) \tag{2.6f}$$

$$b_0 = g_{m1}g_{m2}(g_{m3} + g_{ds3} - 2g_{ds2}). \tag{2.6g}$$

After all, it is seen that the inductance value that is realized by the circuit is quite dependent of operating frequency. Therefore, one can elaborate on what type of behavior that will circuit show in low- mid- and high-frequencies by examining the mathematical expression. For low frequency operation $s \to 0$, according to the resulted expression, a resistive behavior is expected from the circuit, as operating frequency is kept increasing, the expression starts showing inductive behavior. At last, when s becomes high enough, capacitive behavior is expected from the circuit.

2.3. Biasing the Active Inductor

A biasing arrangement is necessary such that all transistors operate in saturation region, which means that their small signal model is a voltage controlled current source. First, the type of the transistors are chosen, n-channel or p-channel. Since both have identical small signal models one has eight different combinations with three transistors. For the given active inductor circuit, it is decided that choosing all transistors as n-channel would be the most suitable choice. It is also possible to choose all transistors p-channel but, p-channel transistors are quite inferior when compared to n-channel transistors [12]. Next, DC current sources with 100 μA, a reasonable value, are connected to the circuit nodes. Placing diode connected MOS transistors in the circuit for DC shift will move all transistors into saturation region. For this circuit, it is enough to add only one diode connected MOS transistor between drain of M1 and gate of M2. Biased circuit is shown in Fig. 2.5. It is also important that this diode connected MOS transistor should be working so, 100 μA current is passed through the diode connected n-channel MOS transistor. There may be other possibilities with different transistor type selections or with DC level shift transistors however this task

is left to the interested reader. Finally, sizes of the each transistor is given in Table 2.1 and supply voltage for V_{DD} is chosen as 1.65 V and -1.65 V for V_{SS}.

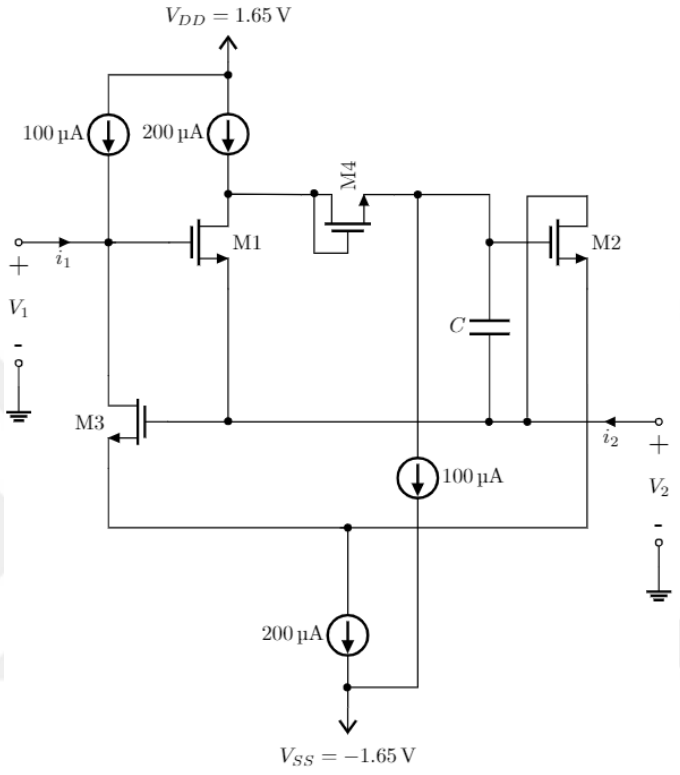


Figure 2.5. Biased active inductor circuit.

Table 2.1. Transistor types and sizes of the presented active inductor circuit.

Transistor name	**Transistor type**	**W (μm)**	**L (μm)**
M1	NMOS	5	0.36
M2	NMOS	10	0.56
M3	NMOS	5	0.76
M4	NMOS	5	0.76

2.4. Simulation Results

To test the functionality of the presented inductor, time domain and frequency domain simulations are performed. In the following simulations, the capacitor C value is chosen as 360 pF. Although this value of capacitance is not integrable, it is useful to test the functionality of the circuit. One can test the functionality of the circuit by connecting a triangular AC current source to either V_1 or V_2 port and grounding the other input port. According to the current voltage relationship given as

$$v = L\frac{di}{dt}, \tag{2.7}$$

one expects to observe high level of voltage when current has positive slope and low level voltage when current has negative slope. Therefore, a square waveform of voltage is expected to be seen.

Fig. 2.6 and Fig. 2.7 show the time domain simulation results of the active inductor circuit when a current source that has triangular waveform with 1 MHz frequency and 20 µA peak-to-peak current is applied to the inputs of the circuit. Specifically, Fig. 2.6 presents time domain simulation results when input current is connected to the V_1 port and Fig. 2.7 presents simulation results when input current source is connected to the V_2 port (while grounding the other input port each time). In both of the figures "Input Current" label plots the applied input current over the time and "Input Voltage" plots the input voltage that is produced on the input when the input current is applied to the circuit.

The simulation results present one obvious issue of the active inductor circuit and that is the presence of the very high V_{os} and this offset voltage limits the usage of the proposed circuit in electronic circuit applications. Therefore, a diode is placed on the circuit in order to shift voltage level of the proposed circuit to a more reasonable level so that when an application of the circuit is carried out the active inductor circuit could function successfully. Fig. 2.8 shows the circuit after the diode placement.

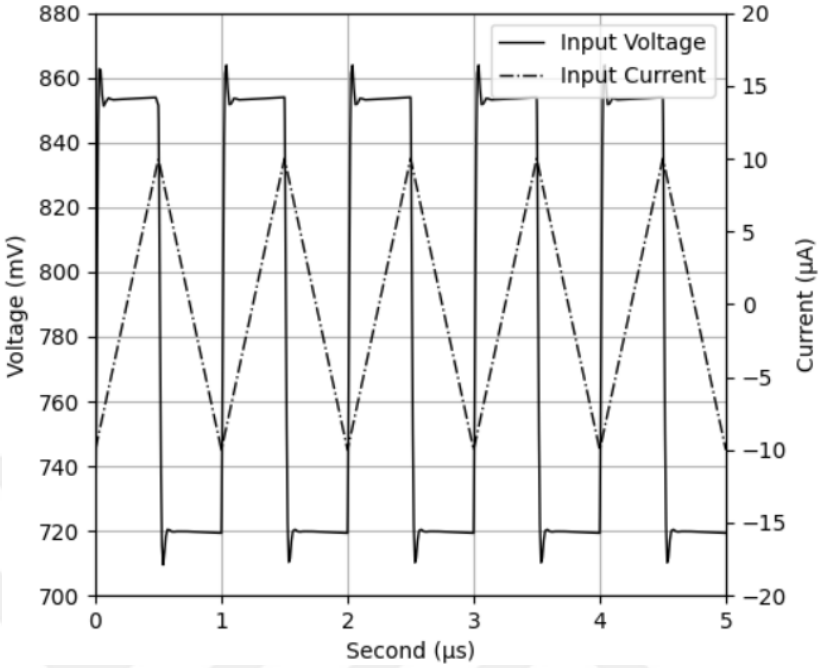


Figure 2.6. Time domain analysis of the AI with input connected to V_1 port.

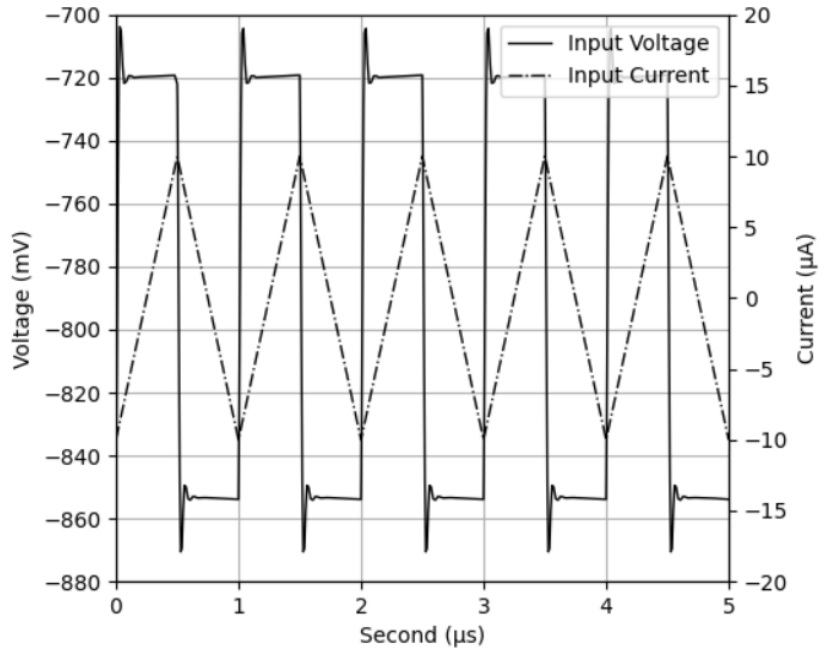


Figure 2.7. Time domain analysis of the AI with input connected to V_2 port.

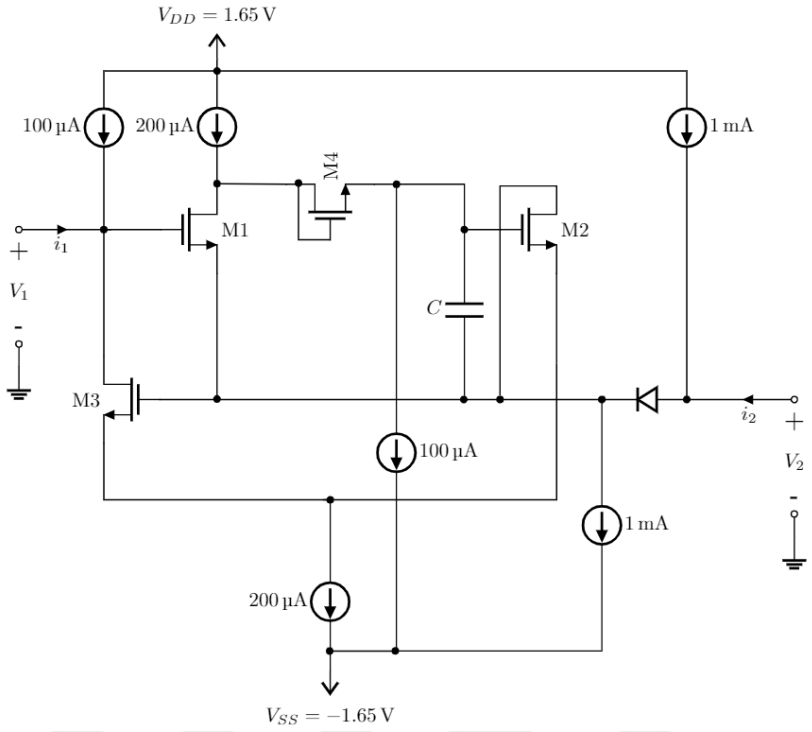


Figure 2.8. The circuit schematic after the diode placement.

Fig. 2.9 and Fig. 2.10 show time domain simulations of the circuit after diode is placed. In Fig. 2.9, the input source is applied to V_1 port of the circuit and in Fig. 2.10 the input source is applied to V_2 port of the circuit. It is seen that the expectations from Equation (2.7) are fulfilled. The affect of the diode replacement could be clearly seen in both of the circuit. The very high level of voltage shift is dramatically reduced and now the circuit could be utilized in various applications. One very important aspect of the inductor circuit is that it has high swing voltage (130 mV). The inductance value of this active inductor is found to be 1.65 mH. In the following sections all analyses are made for the active inductor circuit that has a diode placement.

In order to fully characterize the circuit, frequency domain analysis of the circuit is also carried out. In order to perform the frequency domain analysis in LTSPICE, one could set "AC Amplitude" parameter to 1 in current source's variables. Fig. 2.11 shows the results of the frequency domain analysis of the circuit. The simulation results are valid when the input source is connected to both of the input ports V_1 and V_2.

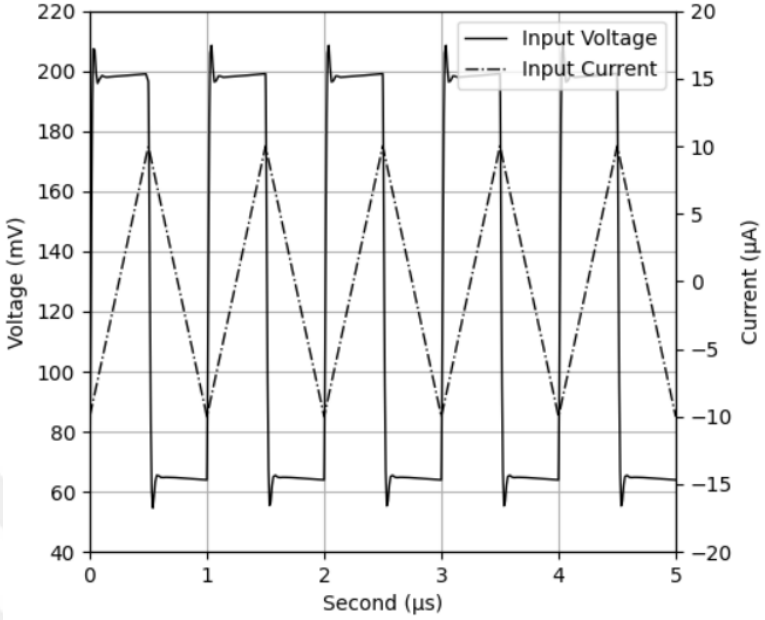


Figure 2.9. Time domain analysis of the AI with input connected to V_1 port (after diode).

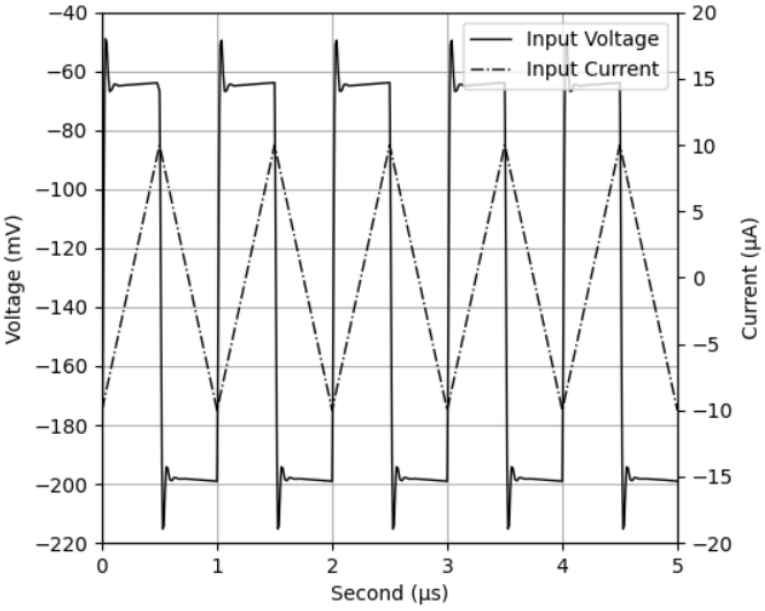


Figure 2.10. Time domain analysis of the AI with input connected to V_2 port (after diode).

To compare the simulated active inductor and an ideal inductor, the magnitude and phase responses of an ideal inductor are also plotted in Fig. 2.11. Here, in Fig. 2.11, "Simulated Magn. Resp." label plots the magnitude response of the active inductor circuit and "Ideal Magn. Resp." plots the ideal inductor's magnitude response. Similarly, "Simulated Phase Resp." shows the active inductor circuit's phase reponse over the frequency spectra. Finally "Ideal Phase Resp." plots the phase response of the ideal inductor. Simulation results indicate that the constructed circuit does not shows inductance behaviour all over the frequency spectra. The proposed active inductor circuit has three main different behaviors at different frequency ranges. At low frequency, the circuit shows resistive behaviour, at mid-level frequency it becomes inductive and, finally, at very high frequencies the circuit shows capacitive behaviour. According to simulation results, the circuit's inductive behaviour could be observerd between 5 kHz - 20 MHz as of the inductive behaviour description of [2]. Overall, it could be said that the presented active inductor circuit shows the inductance behavior over a relatively long frequency spectrum band.

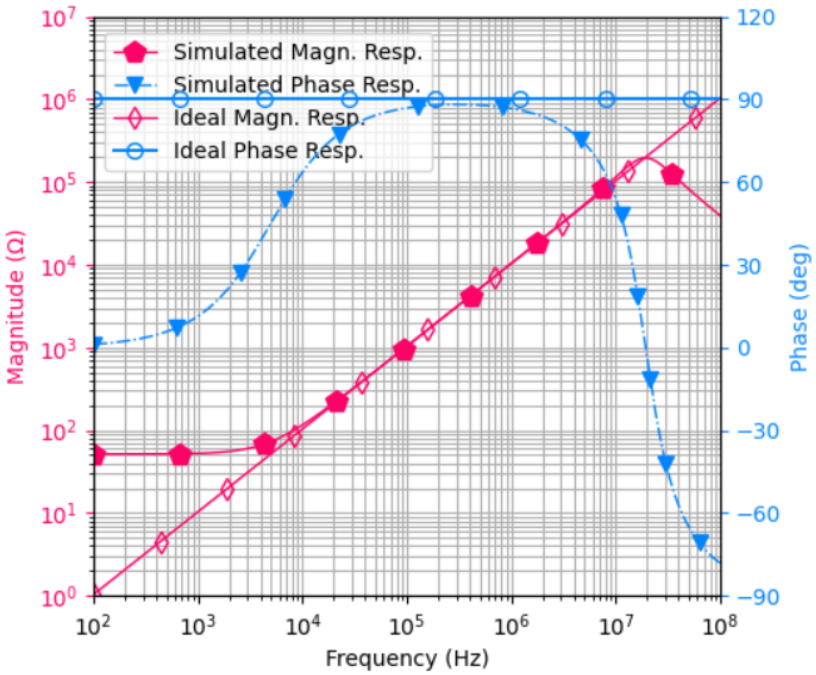


Figure 2.11. Frequency domain analysis of the circuit.

Magnitude response of the ideal and non-ideal theoretical impedance of the circuit, which were presented in Equations (2.4) and (2.5) are plotted in order to compare simulation results and theoretical results. Fig. 2.12 presents ideal vs. non-ideal -Z_{eq1}- theoretical input impedance magnitude response comparison and the g_m values and parasitic component values of the transistors could be seen in Table 2.2. According to the results, it is seen that theoretical non-ideal approximation and simulation results are showing a lot of similarities. To be more precise, various qualities of the non-ideal theoretical calculation results and simulation results are given in Table 2.3. It is seen that although there are differences, results are close to each other. More detailed analysis of the theoretical analysis is made in APPENDIX B.

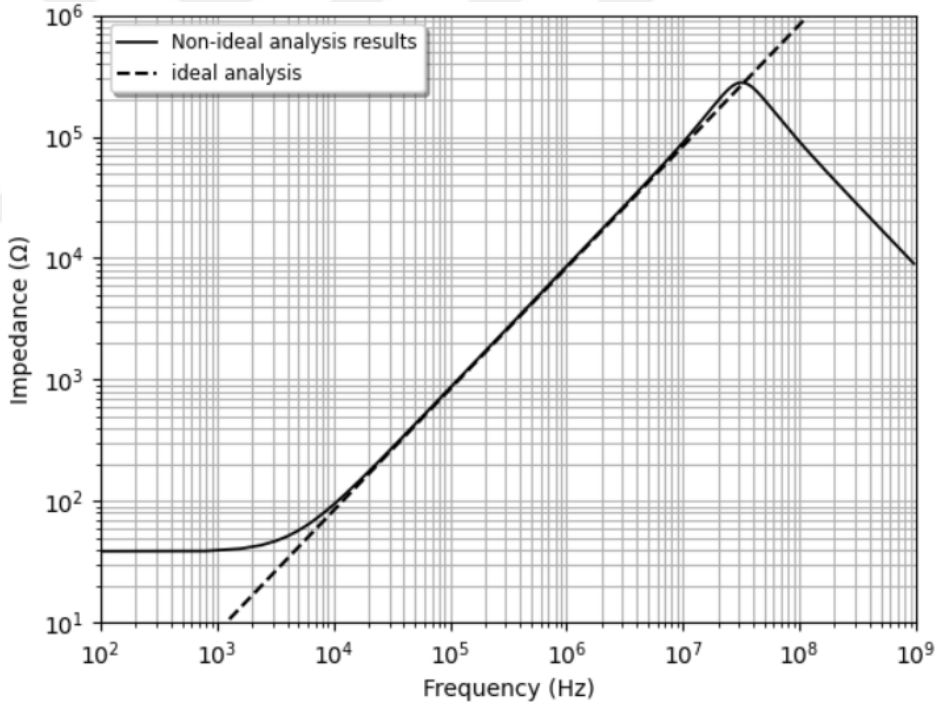


Figure 2.12. Magnitude response comparison of the ideal vs. non-ideal theoretical impedance expression (Z_{eq1}).

Table 2.2. Transistor parameters of the presented active inductor circuit.

Transistor name	g_m **(mA/V)**	C_{gs} **(fF)**	C_{gd} **(fF)**	g_{ds} **($\mu\Omega^{-1}$)**
M1	0.837	14.4908	3.95	10.1
M2	0.864	40.6936	7.9	8.69
M3	0.516	26.2028	3.95	5.79
M4	0.517	28.9816	7.9	5.51

Table 2.3. Comparison between non-ideal and simulation results.

Analysis type	L **(mH)**	$\max(Z_{eq1})$ **(kΩ)**	$f_{max(Z_{eq1})}$ **(MHz)**	$\min(Z_{eq1})$ **(Ω)**
Simulation results	1.65	278.6	31.79	38
Theoretical calculation	1.33	195.6	19.5	52

Additionally, Q value of the active inductor is plotted along with inductance value of the circuit. Fig. 2.13 shows inductance and Q value of the presented circuit. The inductance value that is presented in Fig. 2.13 is calculated according to Equation (2.8). As it is observed there is (or are) capacitor(s) in the circuit. At low frequencies the imarginary part of the input impedance will be equal to the inductance's impedance because the inductor's impedance will be too small so that capacitor(s)'s impedance will not be able to manifest their presence. Inductance of the circuit is estimated as

$$L_{\text{app.}} = \frac{mag(IM\{1/Y_{\text{eq}}\})}{\omega}. \tag{2.8}$$

To plot quality factor, the description for Q in [2] is utilized. The quality factor is described in the quoted source as the ratio of imaginary part of the input impedance to reel part of the input impedance. Quality factor of the circuit is expressed as follows

$$Q = \frac{mag(IM\{1/Y_{\text{eq}}\})}{RE\{1/Y_{\text{eq}}\}}. \tag{2.9}$$

Simulation results indicate that the highest Q value is achieved at close to 300 kHz. Also, Fig. 2.13 shows that the inductance behavior does not quite change between 10 kHz and 10 MHz and its value is close to 1.65 mH. Simulation results validate that the inductance behavior of the circuit diminishes at high frequencies.

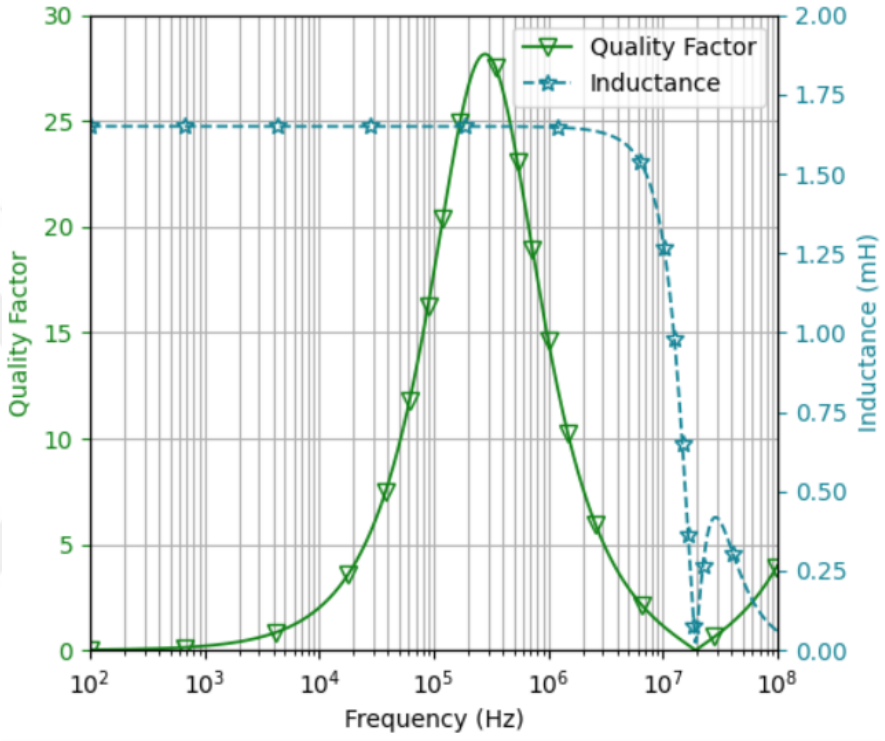


Figure 2.13. Quality factor and inductance of the circuit.

Monte Carlo and temperature analysis of the given active inductor circuit are also performed in order to see how will circuit behave when produced with some error margin on various circuit elements or diverse environment temperatures. For the designed circuit Monte Carlo simulations are made with 200 runnings to see the circuit's behavior, where 5% and 10% errors are introduced into the mobility of the electrons and capacitor value as Gaussian function respectively. Fig. 2.14 shows Monte Carlo simulation results. Temperature analysis of the circuit is performed between -40° and 100° celcius with 10° difference at each step. Fig. 2.15 shows temperature analysis of the AI. Simulation results prove that the circuit performs well under different temperatures and results are valid for the circuit's both inputs.

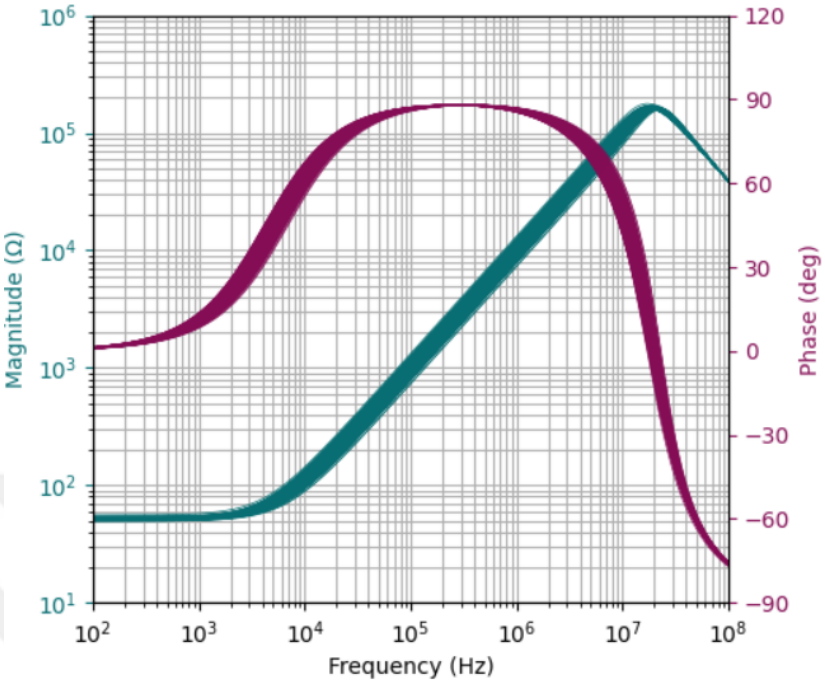


Figure 2.14. Monte Carlo simulation results of the active inductor circuit.

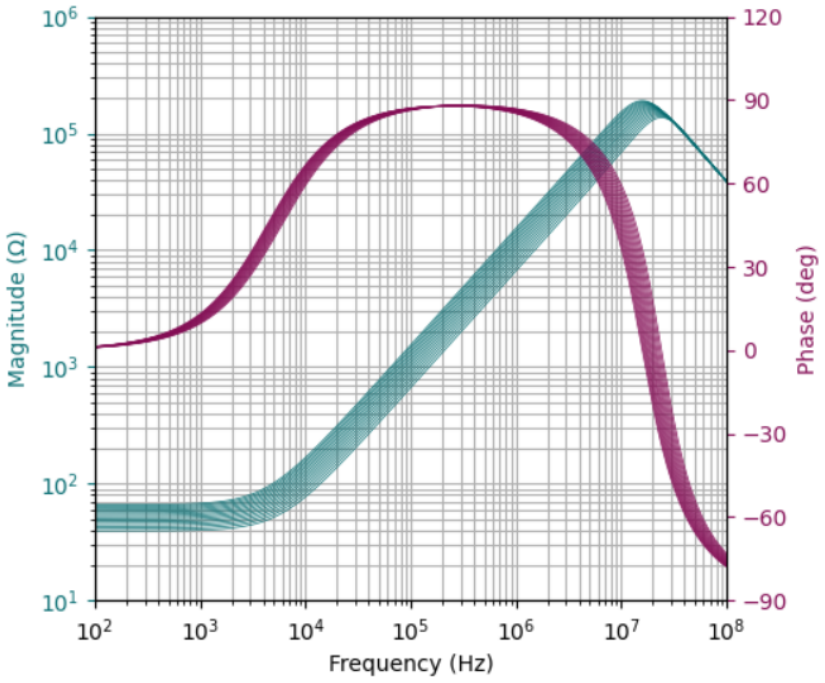


Figure 2.15. Temperature analysis of the circuit.

2.5. Application Instance

The proposed active inductor can replace the inductors in a passive elliptic filter circuit. In many filter applications, inductors are essential. To test the functionality of the active inductor a simple passive 3rd order Elliptic LP filter is constructed with the standard values that are presented in [13]. Fig. 2.16 shows the construction of the filter. The constructed Elliptic filter has the following specifications: 200 kHz cutoff frequency, 2 dB pass band ripple and stop band attenuation 60 dB.

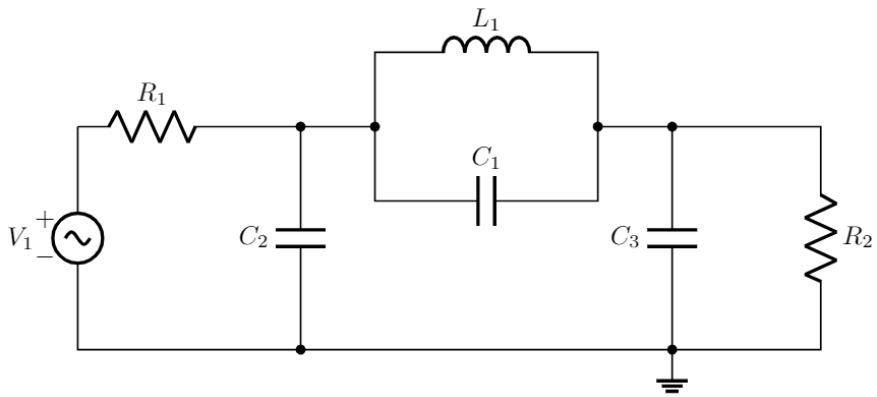


Figure 2.16. 3rd order Elliptic Low-Pass Filter.

Filters have an interesting feature and it is that their impedances and frequencies could be scaled. This means that while preserving the filter's identity some of its qualities could be altered. For instance, the component values of the filter and the cutoff frequency of the filter are the two things that could be changed. Now, in order to match passive and active inductor's inductances, element scaling operation is done on the Elliptic Filter circuit. The impedance and frequency of an filter could be scaled according to following scaling rules

$$C = \frac{C_n}{K_{\mathrm{f}} K_{\mathrm{m}}} \tag{2.10}$$

$$L = \frac{K_m L_n}{K_f}, \tag{2.11}$$

where L and C present final values for the inductor and capacitor elements. L_n and C_n denote the initial inductor and capacitor values. K_{f}=ω_{c}'/ω_{c}, where ω_{c}' is the target cutoff frequency of the filter and ω_{c} is the initial cutoff frequency of the filter. K_{m}=R'/R, where R' is the final resistor value and R is the initial resistor value (for R_1 and R_2). Here, all elements are scaled according to 1.65 mH inductance while still preserving the filter's specifications. The scaled values of the components are found as in the following: R_1 = 1.96 kΩ, R_2 = 4.27 kΩ, C_1 = 14.98 pF, C_2 = 759.8 pF and C_3 = 865.3 pF. Fig. 2.17 shows comparison results between ideal circuit and the circuit with active inductor. In Fig. 2.17, "Mag. Res. with Ideal Ind." plot describes the original circuit's magnitude plot -the Elliptic filter circuit that is constructed with an ideal inductor. "Mag. Res. with Active Ind." plot shows the magnitude response of the filter circuit that employs the proposed active inductor circuit. Similarly, "Phase Res. with Ideal Ind." plot shows the original circuit's phase response -the circuit that employs ideal inductor. Finally, "Phase Res. with Active Ind." shows phase response of the filter that is constructed with the active inductor circuit. Results indicate that the active inductor shows very promising performance and can indeed imitate a floating inductor behavior.

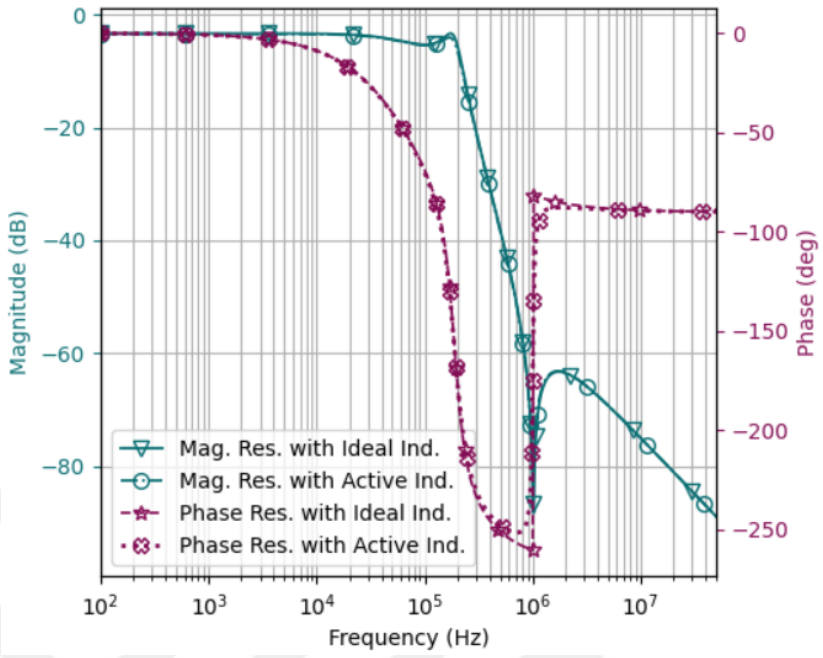


Figure 2.17. Simulation results of the Elliptic LPF with ideal vs. active inductor.

2.6. Conclusion

In this chapter a novel floating active inductor is proposed. The proposed active inductor is realized by using MOS-Only technique. The analysis and the building of the circuit are explained step by step until the circuit's final state, which is the biased version of the circuit where all transistors work in saturation region. According to the simulation results, the circuit fulfills expectations and shows reliable performance. It has been proven that the realized active inductor is capable of achieving 1.65 mH of inductance value and is able to reach 1 MHz of operating frequency. The inductor is also tested in a Elliptic LPF design in order to check its functionality. Results indicate that the inductor circuit functions as expected. On the other hand, like many active inductors it has some drawbacks such as power dissipation and noise, mainly due to MOSFET utilization.

3. A SYMMETRICAL FLOATING ACTIVE INDUCTOR CIRCUIT DESIGN

In this chapter, a novel symmetrical floating active inductor is presented. The core design itself implements a floating inductor. However, an augmented structure is constructed by mirror symmetry connecting two of them for improved performance (in this case the basic inductor topology that was presented in detail in Chapter 2). The designed inductor has utilized MOS-Only technique and simulations are carried out in LTSPICE simulation environment with 0.18 μm TSMC MOS parameters. Simulation results show that the proposed circuit can work up to moderately high frequencies such as 20 MHz while generating 19 μH inductance value and consuming nearly 1.242 mW power. Also, usability of the circuit is tested in a 3rd order Low-Pass Butterworth Filter application example.

3.1. Introduction

Inductors are widely used in various circuit designs [14-17]. However, as pointed out before, passive inductors suffer from tunability problem, large chip area consumption, low Q, low inductance value or sensitivity to magnetic interference. Active realizations present an alternative solution. In many applications passive inductors can be replaced by active inductor circuits. They are in fact realizations of inductors, which is itself a passive element with help of active circuits. In active realizations, magnitude and phase responses of voltage and current will be similar to its passive counterpart, whereas active inductors do not induce any magnetic field when the current is flowing between their terminals. In past many active inductor circuits are proposed [18-21], some are of grounded type [20, 21], which limits their use in electrical circuit designs. Symmetrical connections to obtain differential circuits are highly popular in IC designs because they have various advantages over their single-ended counterparts. For instance, in such circuits, noise is reduced, voltage swing is doubled, second order nonlinearities are reduced etc. [22]. However, they achieve these advantages over some cost.

For instance, the cost could be that the total area and consumed power are doubled in symmetrical circuits but still one can easily claim that the benefits of symmetrical connections outweigh single-ended connection. This chapter presents a floating type active inductor that is realized by VCCS model of MOS transistors, where several additional current sources are employed for biasing purposes. Many early works on this technique are presented in [2], where AI instances are realized with MOS transistor utilization and many of the realized inductors are simple grounded type. The presented core design here itself realizes a floating inductor. However, a symmetrical connection two of these floating inductors is preferred to obtain the above mentioned advantages. The inductance value of the presented circuit is tunable, it works up to 20 MHz frequency, occupies reasonable area on an integrated circuit. Nevertheless, like all active inductor circuits, it consumes power and also increased noise is a well-known drawback of such circuits. On the other hand, since their operation is not based on magnetic field creation, interference type of noise reduction can be expected.

3.2. Basic Topology and Symmetrical Version of the Circuit

Basic Topology: In this section, the actual core of the circuit is presented and analyzed. The basic core topology, which is a floating inductor itself is shown in Fig. 2.1. Here, it should be noted, once again, that the arrows on the transistors indicate the source connection of the transistor, not the type of the transistor. For instance, the arrow on the M1 transistor indicates the source connection of the M1 but the type of the M1 could be n-channel or p-channel transistor since both n-channel and p-channel MOS transistors have identical small signal AC models. In order to analyze the basic topology, the MOSFETs are replaced with their ideal small signal equivalent circuit, which is simply a voltage controlled current source. Routine analysis gives admittance matrix of this two port in the form that is presented in Equation (2.1), where L_{x1} is presented in Equation (2.2).

. Equation (2.1) is the matrix equation describing a floating inductor. Moreover, the realized inductance value can electronically be adjusted by transconductances of transistors or by changing value of the circuit capacitor C as it could be observed from Equation (2.2). Transconductances of the inductors could be easily adjusted by changing the values of the bias current sources. Note that ideally the circuit does not require any matching condition of transconductances. Using this topology, many floating inductor realizations are possible. In order to evaluate the circuit's behaviour in detail and determine its response at high frequencies, non-ideal analysis of the circuit is carried out. Here, for all transistors parasitic elements are added to their small signal model such as g_{ds}, C_{gs} and C_{gd}, where they denote well-known parasitics suitable for a first order non-ideal analysis. The sL_{x1} element of admittance matrix is calculated as it could be observed in Equations (2.3) and (2.4), which equals I_1/V_1 while V_2 port is grounded. The nonideal expression for $1/sL_{\mathrm{x1}}$ is found to be too complicated and it is more convinient to have impedance expression rather than the admittance. Therefore, impedance expression is obtained by inversing the admittance and a first order simplification is performed, where any term that contains product of two or more parasitic elements are omitted. Equations (2.5) and (2.6) present the finalized expression for sL_{x1}, impedance of the circuit, where the last subscript of the variables denote the transistor number.

Symmetrical version: It is well known that differential circuits result increased linearity and reduced even order distortion in addition to several other advantages. The proposed symmetrical connection is constructed as in Fig. 3.1 by mirroring the circuit in Fig. 2.1. All of the inductor core circuit transistors are p-channel MOSFETs. In order to bias the proposed circuit, on-chip current sources are utilized. Five p-channel MOSFETs are used in order to supply required amount of currents in to the circuit nodes. The M13 transistor's W/L ratio is adjusted along with R_1 to make $\mathrm{I_D}$ of M13 to be 100 μA. The drain currents of M12, M11, M10 and M9 are set by changing W/L ratios of each transistor. Similarly, another current source is used in order to draw required amount of currents that would set transistor currents desired. To do this five n-channel MOSFETs are used. The M18's drain current is set to be 100 μA and other

transistor currents are set by adjusting W/L ratios of the M14, M15, M16 and M17. The circuit is supplied with symmetric power supply and the supply voltages are +0.9 V for V_{DD} and -0.9 V for V_{SS}. It should also be noted that the resistance values for R_1 and R_2 are 3.4 kΩ and 1.5 kΩ respectively while $C = 5$ pF. Transistor W/L ratios are as follows (μm/μm): M1: (50/0.76), M2: (55/0.56), M3: (50/0.36), M4: (55/0.76), M5: (50/0.76), M6: (55/0.56), M7: (50/0.36), M8: (55/0.76), M9: (10/0.3), M10: (21/0.3), M11: (10/0.3), M12: (21/0.3), M13: (10/0.3), M14: (66/0.3), M15: (33/0.3), M16: (33/0.3), M17: (66/0.3), M18: (30/0.3).

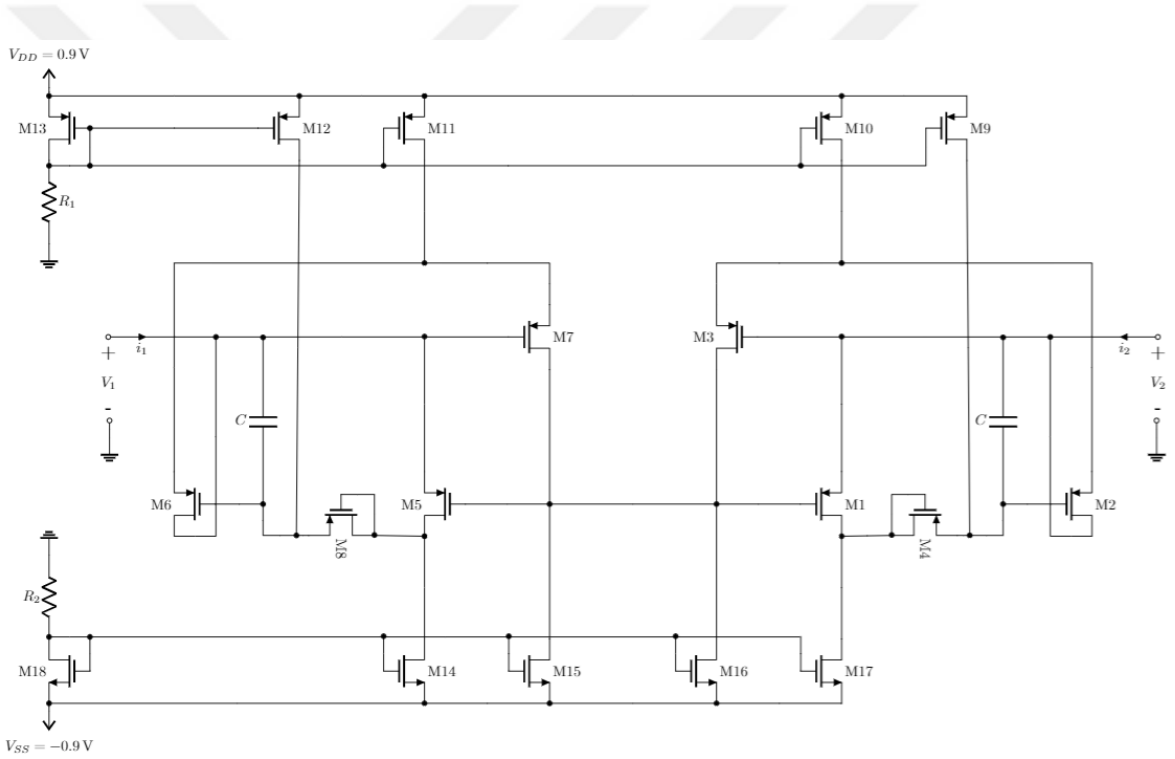


Figure 3.1. The proposed symmetrical connected circuit.

3.3. Simulation Results

In order to evaluate the performance of the circuit in Fig. 3.1, simulations are carried out in LTSPICE simulation environment. The time domain analysis, frequency domain analysis and Monte Carlo analysis of the circuit with 200 runs are performed.

Finally, to observe the circuits behavior at various temperatures, a temperature analysis of the circuit is performed. For time domain analysis a triangular waveform of 20 MHz frequency and 20 μA peak to peak value of a current source is applied to the inductor. A square wave voltage signal is expected between inductor terminals due to $v = L(di/dt)$ relation. According to the simulation results shown in Fig. 3.2, the circuit produces almost 40 mV peak-to-peak voltage. The limited slew rate observed due to undesired parasitics. The inductance value of the symmetrical circuit is found to be 19 μH at 20 MHz.

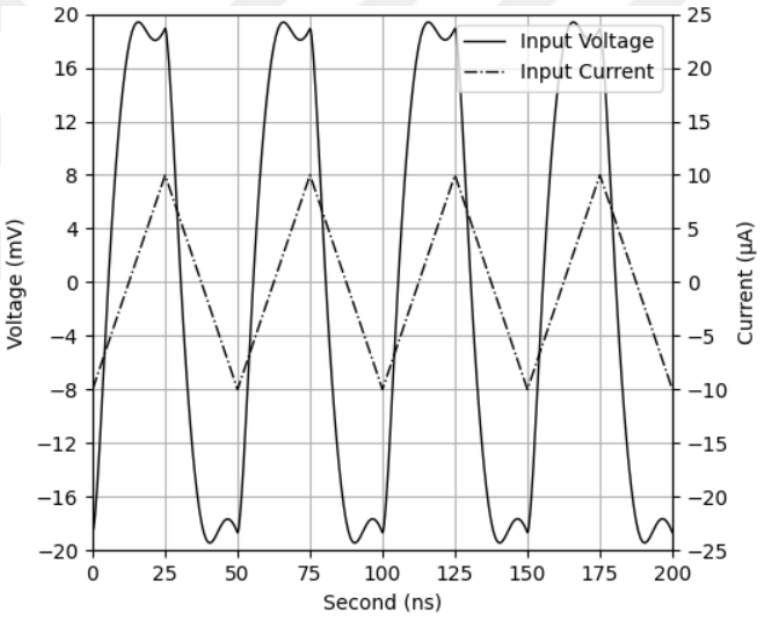


Figure 3.2. Time domain response of the active inductor circuit to a triangular current waveform.

An ideal inductor's frequency domain analysis would result a constant 90° in phase response and linearly increasing magnitude response. The aim for the presented inductor circuit is to imitate this behavior as wide as possible over the frequency spectrum. Fig. 3.3 shows the simulation results of the proposed circuit. The magnitude and phase responses of the circuit are plotted with an ideal inductor that has same inductance value with the presented circuit. According to the simulation results, the circuit shows inductance behavior between 3.5 MHz and 44 MHz; moreover, the quality

factor and inductance value of the circuit are also plotted on a separate figure. Fig. 3.4 shows the quality factor and the inductance value of the circuit over the frequency spectra. The inductance value that is plotted over the frequency is calculated according to Equation (2.8) as shown in the same figure. Equation (2.8) is a valid equation when a circuit's input impedance is composed of only resistive and inductive elements. The presented active inductor has parallel capacitor or capacitors to the inductor. This can be seen from frequency domain analysis of the circuit. Equation (2.8) will be assumed to be valid at reasonably low frequencies because at low frequencies the capacitor will have high impedance that will be connected in parallel to the inductor. Hence, the input impedance will be mostly equal to the impedance of the inductor then by dividing impedance to 2πf the inductance value could be estimated.

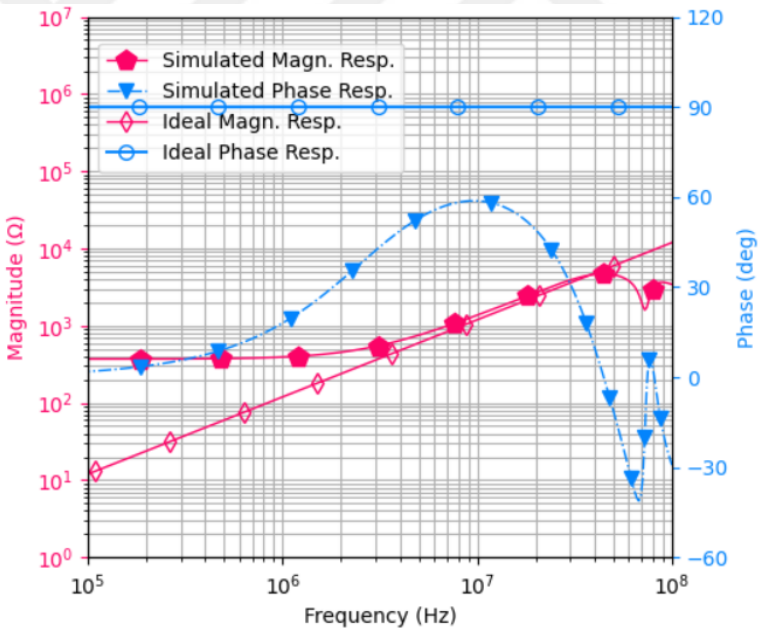


Figure 3.3. Frequency domain analysis of the presented circuit.

To plot the quality factor, the description of the quality factor in [2] is used again. According to the description, the quality factor is the ratio of the imaginary part of the input impedance of the circuit to reel part of the impedance of the circuit. Equation (2.9) presents the equation for the quality factor. It is seen that the highest quality factor is achieved at 10 MHz frequency close to 1.7. Also, it is seen that the inductance

value of the circuit is same up to 10 MHz frequency. Note that Equation (2.8) and Equation (2.9) are used for a rough estimate of inductance values and quality factors. They should be used with care since the most general impedance equation for such circuits may even have higher order representations if additional but less dominant parasitic capacitors are included in the model. The values of the parasitic capacitors could be observed from Table 2.2.

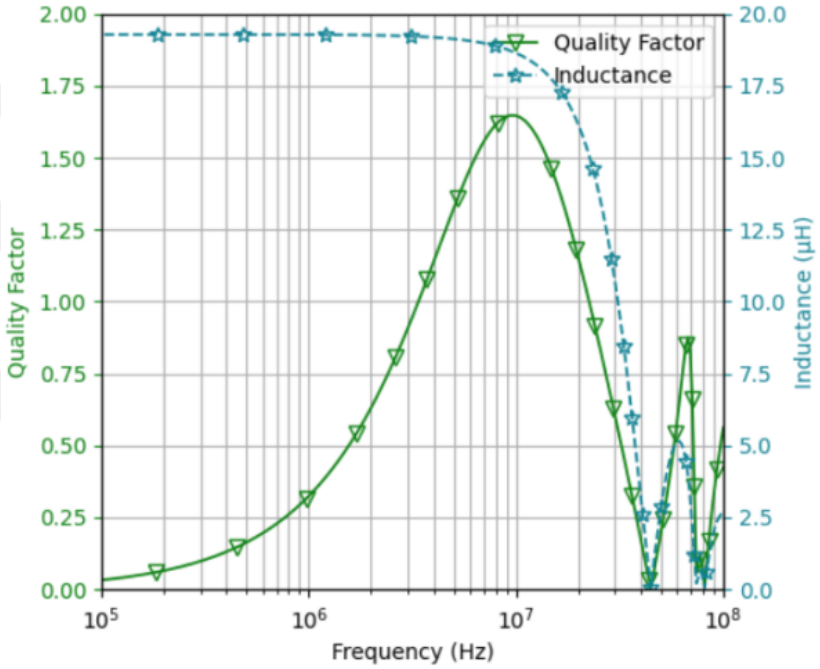


Figure 3.4. Inductance value and quality factor of the circuit.

In order to compare single-ended (the circuit that is presented in Chapter 2) and symmetrical connected versions of the circuit, Table 3.1 could be observed. L is the realized inductance value by the circuits, i_{inpp} and v_{inpp} indicate applied input current and consequently realized voltage at the very same node respectively in the table. $f_{\text{op.}}$ is the operation frequency and Q_{max} is the maximum Q value realized by the circuit at $f_{\text{op.}}$ and, finally, f_{Qmax} is the frequency, where Q_{max} is achieved. According to the results, it is seen that while single-ended version offers higher peak-to-peak voltage and inductance, its operation frequency is quite inferior than the symmetrical connected version of the circuit. Similarly, maximum Q value of the single-ended version of the

circuit is superior than the symmetrical connected version of the circuit but it offers it at a quite low frequency compared to where symmetrical connected circuit offers its maximum Q value.

Table 3.1. Single-ended vs symmetrical connected comparison of the circuit.

Version	$L_{\text{sim.}}$ **(mH)**	C **(pF)**	i_{inpp} **(μA)**	v_{inpp} **(mV)**	$f_{\text{op.}}$ **(MHz)**	Q_{max}	$f_{\text{Q}_{\text{max}}}$ **(MHz)**
Single-ended	1.65	360	20	133	1	28.15	0.277
Symmetrical connected	0.019	5	20	36	20	1.65	9.5

Producing identical electronic elements that have all identical parameters is not possible because even if the electronic elements are produced from same wafer die, the wafer has different properties at its different locations. Therefore, it is important to take into account these errors and Monte Carlo analysis is used in order to simulate these types of errors. In this analysis, the errors are set on the MOSFETs and the two capacitors and 200 Monte Carlo simulations are run in order to see the circuit behavior with the errors. It is thought that setting 5% error margin on the MOSFET mobility and 10% error margin for the capacitors would be an appropriate choice in order to simulate the errors. An important detail about the errors is that in LTSPICE errors are introduced as functions and the errors that are set on the MOSFETs and capacitors are Gaussian function type of errors. Fig. 3.5 shows the simulations results of the Monte Carlo simulation. According to the simulation results, one can say that there is no significant deviation in the responses with the presented error margins. It is seen that the deviations on the MOSFET mobility and capacitor value does not disturb the circuit performance dramatically. In order to evaluate the performance of the circuit for different temperatures the environment temperature changed from -40° Celsius to 100° Celsius with 10° Celsius steps at each time. Fig. 3.6 shows the mentioned temperature analysis of the active inductor circuit.

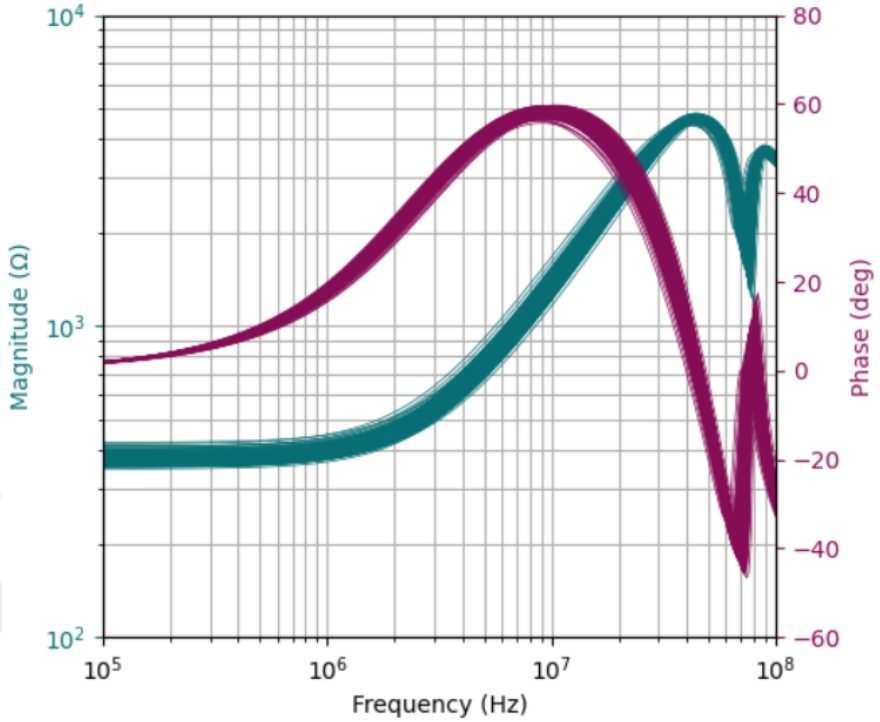


Figure 3.5. Monte Carlo analysis of the circuit.

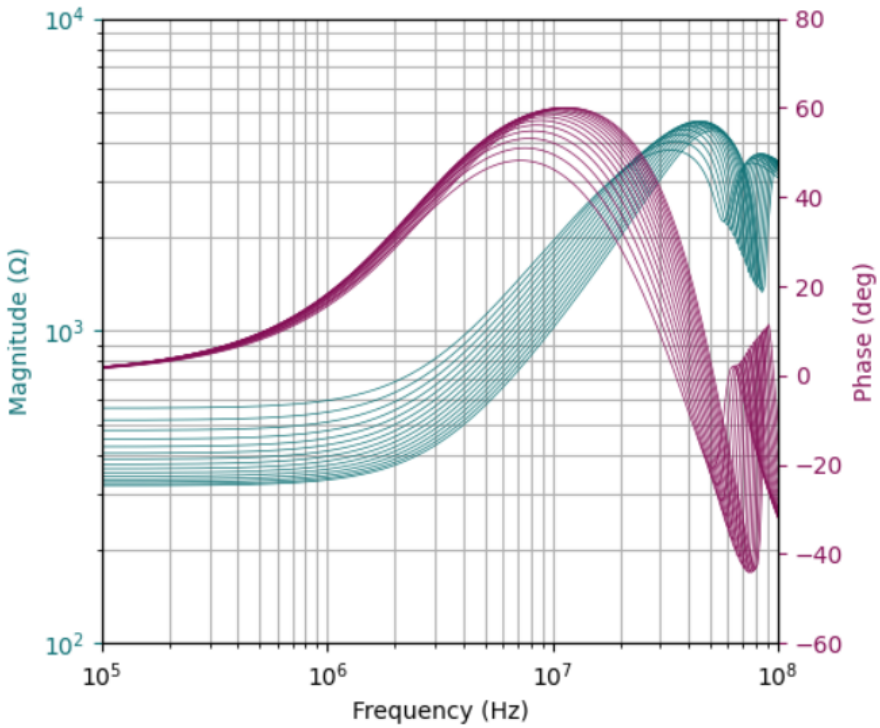


Figure 3.6. Temperature analysis of the circuit.

3.4. Application Example for the Floating Inductor Circuit

The performance of the circuit is evaluated on a 3rd order Low-Pass Butterworth Filter circuit. The passive prototype is shown in Fig. 3.7. The denominator polynomial of the filter transfer function denotes the Butterworth polynomial. In order to identify component values, normalized third-order low-pass polynomials are utilized that are correspond to a cutoff corner frequency of 1 radian/sec. Normalized -for 1 radian/sec- denominator polynomial in factored form is written as

$$A(s) = (s+1)(s^2+s+1). \tag{3.1}$$

Equation (2.10) and Equation (2.11) present general frequency and component scaling formulas. These equations enable to change a filter's component values and cutoff frequency while preserving the filter's qualities, where L_n and C_n present the initial capacitor and inductor values. L and C stand for final values of the inductor and capacitor elements. Additionally, K_{m}=R'/R, where R' and R are the final and initial resistor values respectively (for R_1 and R_2) and K_{f}=ω_{c}'/ω_{c}, where ω_{c}' and ω_{c} are the target and initial cutoff frequency of the filter respectively as explained before. The initial component values are found from Equation (3.1) then, by utilizing Equation (2.10) and Equation (2.11) the filter's f_{c} is scaled. Since the value of the inductor is 19 μH, it is also necessary that all component values should be scaled to match the active inductors inductance value while preserving the cutoff frequency. Standard values for the prototype circuit components are as following: $R_1 = R_2 = 1\ \Omega$, $C_1 = C_2 = 1$ F and $L_1 = 2$ H. After performing scaling operation, the following component values are found: $R_1 = R_2 = 1197\ \Omega$ and $C_1 = C_2 = 6.63$ pF.

Fig. 3.8 shows simulation results of the 3rd order Butterworth LPF with ideal inductor based prototype and with the presented active inductor circuit. Simulation results show that the phase response of the two circuits are almost identical. However, the active inductor circuit is seen to be lossy. Therefore, magnitude responses of the two circuits do not quite match. One straightforward way to compansate the

loss of inductor could be increasing R_2 resistance. By this way, the problem could be solved easily. The cutoff frequency for the LPF with active inductor circuit is 17 MHz. It is clear that the proposed symmetrical active inductor circuit performs well when it replaces the passive inductor and could possibly take its place in various applications.

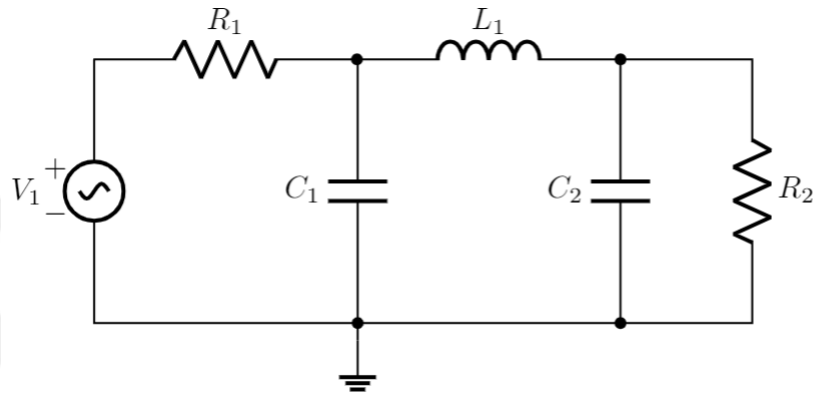


Figure 3.7. 3rd order Low-Pass Butterworth filter.

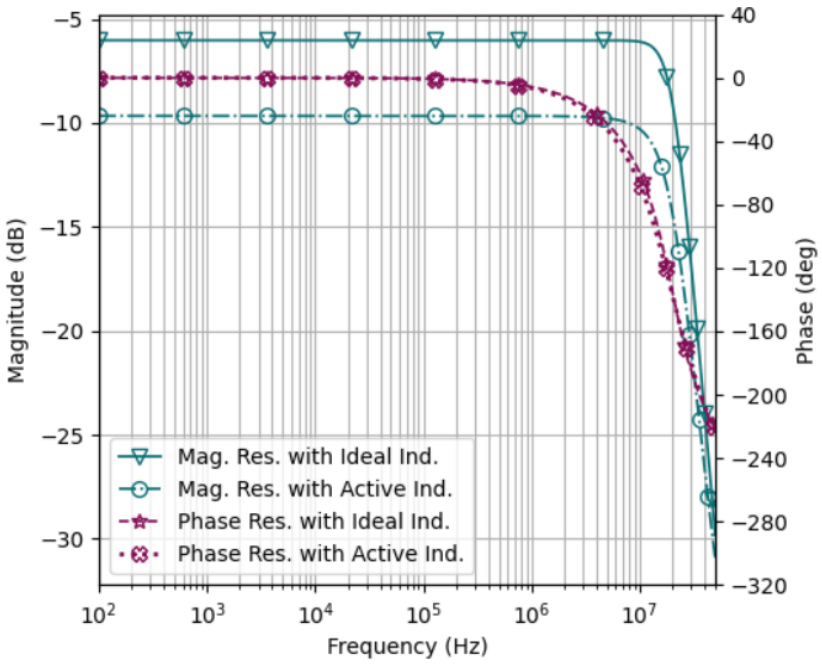


Figure 3.8. Simulation results of the Low-Pass Filter (original prototype and active inductor based magnitude and phase responses).

3.5. Conclusion

In this chapter, a novel symmetrical structure active inductor circuit is presented. The basic core itself is also a floating inductor in other words the floating inductor property is not obtained by symmetry. The presented circuit bias current is supplied with on-chip current sources. The simulations are carried out in LTSPICE simulation environment with 0.18 μm TSMC MOS parameters and simulation results indicate that the circuit generates 19 μH inductance value at 20 MHz operation frequency; moreover, the Q value at 20 MHz is found to be around 1 and maximum Q is achieved at 10 MHz with 1.7.

4. A SINGLE-ENDED SIMULATED INDUCTOR WITH ITS SYMMETRICAL VERSION

By utilizing MOS-Only technique two novel active inductors circuit are presented in this chapter. The presented single-ended version of the circuit employs seven transistors. The circuit simulations are carried out by using 0.18 μm TSMC CMOS parameters. According to the simulation results, pros and cons of the circuit are discussed; moreover, along with single-ended version, symmetrical configuration of the circuit is also presented. The presented circuit's single-ended configuration realizes 0.285 mH inductance value at 10 MHz frequency while consuming close to 470-μW power and the symmetrical version of the circuit realizes 0.566 mH inductance and increases power consumption significantly.

4.1. Introduction

Inductors are critical elements in designing electrical circuits [14, 23, 24]. Passive inductors are not desirable circuit elements in integrated circuited design because of their well known ineffectiveness. As a result, instead of using these elements in circuits, researchers are trying to come up with new circuit designs that realize synthetically an equivalent inductance employing capacitance. A very simple but inefficient active inductor circuit can be constructed by a capacitor and two transconductors [25]. In order to improve the qualities of the AIs, new active inductor circuits, both grounded and floating type, have been proposed by researchers [26 - 35] over the time. In this chapter a new floating seven transistor active inductor is proposed by MOS-Only technique along with its symmetrical version and simulation results of the circuits are given. The proposed active inductors meet expectations and work at moderately high frequencies.

4.2. A New Floating Active Inductor Design

Floating active inductors are in more of a need than grounded active inductors in on chip designs because most of the inductors that are utilized in the circuits are of floating type. Besides that simulated inductors do not create magnetic flux like passive inductors therefore, when using simulated inductors, shielding is not required. The active inductor circuits that are presented in this chapter result an inductance value that is tunable.

4.2.1. Core Circuit of the Proposed Active Inductor and Its Analysis

The proposed active inductor's basic schematic is shown in Fig. 4.1. The schematic is the very raw version of the proposed circuit, where the transistors represent controlled sources and before being converted to a functioning circuit, there are many steps that should be taken to reach desired final design of the circuit. The circuit implements a floating inductor impedance function. Replacing the transistors with their small signal AC models and applying the matching condition for transistor transconductances, the admittance matrix of this two port could be written as in following

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sL_{x2}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{4.1}$$

where realized inductance value of the circuit is shown as

$$L_{x2} = \frac{C}{g_{m2}g_{m3}}, \tag{4.2}$$

which indicates that the circuit implements a floating active inductor between ports V_1 and V_2 with L_{x2} being the realized inductance value. The matching condition of

the circuit is presented in following as

$$g_{\mathrm{m2}}g_{\mathrm{m3}} + g_{\mathrm{m1}}g_{\mathrm{m4}} = g_{\mathrm{m1}}g_{\mathrm{m3}}. \tag{4.3}$$

When the matching condition is not met, the circuit does not behave as a pure inductor rather, it acts like a positive or negative resistor in series with an inductor, and the sign of the resistance depends on the values of g_{m} of the transistors. The general expression representing the corresponding admittance is given as

$$Y_{\mathrm{id2}} = \frac{g_{\mathrm{m2}}g_{\mathrm{m3}}g_{\mathrm{m4}}}{sCg_{\mathrm{m4}} + g_{\mathrm{m2}}g_{\mathrm{m3}} + g_{\mathrm{m1}}(g_{\mathrm{m4}} - g_{\mathrm{m3}})}. \tag{4.4}$$

In Equations (4.2) and (4.4) the effect of the matching condition on the circuit's behavior can be seen. Obviously, in the design phase this should be taken into account. However, for applications, where a lossy inductor is desired, this matching condition can be relaxed or modified accordingy. According to the inductance expression in Equation (4.2), L_{x2} is dependent on three variables when matching condition is satisfied: directly proportional to C and inversely proportional to g_{m2} and g_{m3}. It is also crucial to emphasize that the arrows on Fig. 4.1 do not indicate the types of the transistors, they indicate source connection of the transistors. When biasing the circuit, the types of the transistors will be chosen.

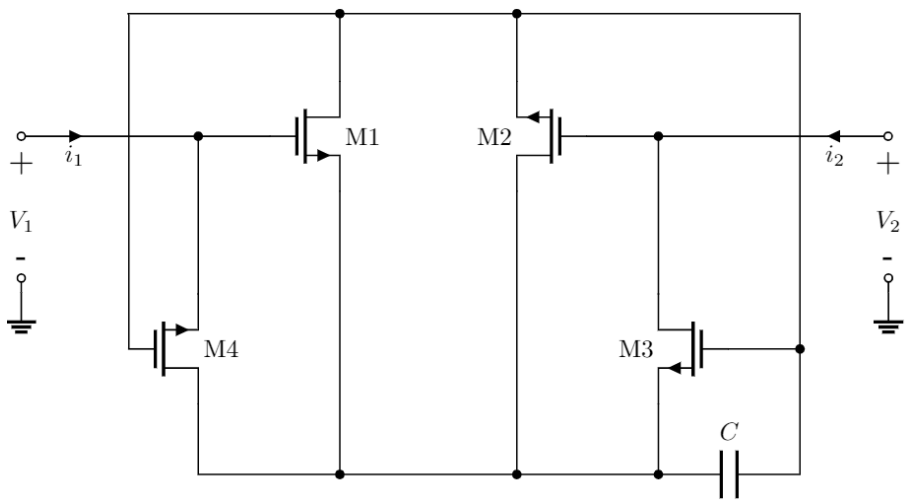


Figure 4.1. Core topology of the floating inductor circuit.

4.2.2. Non-ideal Analysis

Non-ideal analysis, by taking the most critical elements in this sense into account, is important in order to deepening one's understanding about the circuits behavior. Therefore, in this section, non-ideal analysis of the circuit is carried out in order to see how the circuit behaves at extreme frequencies. For this, non-ideal model of the MOSFET is utilized. Fig. 2.3 shows simplified non-ideal AC model of the MOSFET.

Equations (4.5) and (4.6) together present the admittance equation for the circuit, where the last subscript of the terms in Equation (4.6a-g) denote the number of the transistor. Also, parallel capacitors and resistors are combined to y elements for simplicity. For instance, C_{gs1} and g_{ds4} are combined and denoted as y_{14}, C_{gd2} and g_{ds3} are merged and denoted as y_{24} and two parallel conductances g_{ds1} and g_{ds2} are simplified as y_{34} (or as g_{34} followingly); moreover, C_{gd1} and C_{gd3} are omitted because they are parallel to C_{gs4} and C_{gs2} respectively and it is assumed that gate-to-drain capacitances are too small than gate-to-source capacitances and, therefore, could be omitted. The admittance expression of the circuit is written as

$$Y_{\mathrm{eq2}} = \frac{k_3 s^3 + k_2 s^2 + k_1 s + k_0}{l_2 s^2 + l_1 s + l_0}, \tag{4.5}$$

where coefficients are shown as

$$k_3 = C C_{\mathrm{gs2}} C_{\mathrm{gs4}} g_{\mathrm{m1}} \tag{4.6a}$$

$$\begin{aligned} k_2 = {} & C C_{\mathrm{gs4}} g_{\mathrm{m1}} y_{24} + C_{\mathrm{gs2}} (C g_{\mathrm{m1}} (g_{\mathrm{m3}} + y_{14}) - C g_{\mathrm{m2}} g_{\mathrm{m3}} \\ & + C_{\mathrm{gs4}} g_{\mathrm{m1}} (g_{\mathrm{m1}} + g_{\mathrm{m3}} + y_{14} + y_{24} + y_{34})) \end{aligned} \tag{4.6b}$$

$$\begin{aligned} k_1 = {} & C y_{24} (g_{\mathrm{m1}} (g_{\mathrm{m3}} + y_{14}) - g_{\mathrm{m2}} g_{\mathrm{m3}}) \\ & + C_{\mathrm{gs4}} g_{\mathrm{m1}} (g_{\mathrm{m2}} (g_{\mathrm{m3}} + y_{24}) + y_{24} (g_{\mathrm{m1}} + y_{14} + y_{34})) \\ & + C_{\mathrm{gs2}} ({g_{\mathrm{m1}}}^2 g_{\mathrm{m3}} - g_{\mathrm{m1}} g_{\mathrm{m2}} g_{\mathrm{m3}} - g_{\mathrm{m2}} g_{\mathrm{m3}} (g_{\mathrm{m3}} + y_{24} + y_{34}) \\ & + g_{\mathrm{m1}} (g_{\mathrm{m3}} + y_{14}) (g_{\mathrm{m3}} + y_{24} + y_{34})) \end{aligned} \tag{4.6c}$$

$$k_0 = {g_{\mathrm{m1}}}^2 g_{\mathrm{m3}} y_{24} + g_{\mathrm{m1}} g_{\mathrm{m2}}(g_{\mathrm{m3}}(g_{\mathrm{m3}} + y_{14}) + y_{14} y_{24}) + g_{\mathrm{m1}} y_{24} y_{34}(g_{\mathrm{m3}} + y_{14}) - g_{\mathrm{m2}} g_{\mathrm{m3}}(g_{\mathrm{m2}}(g_{\mathrm{m3}} + y_{24}) + y_{24} y_{34}) \tag{4.6d}$$

$$l_2 = C g_{\mathrm{m1}}(C_{\mathrm{gs2}} + C_{\mathrm{gs4}}) \tag{4.6e}$$

$$l_1 = C g_{\mathrm{m1}}(g_{\mathrm{m3}} + y_{14} + y_{24}) + C_{\mathrm{gs2}} g_{\mathrm{m1}}(g_{\mathrm{m1}} + g_{\mathrm{m3}} + y_{14} + y_{24} + y_{34}) + C_{\mathrm{gs4}} g_{\mathrm{m1}}(g_{\mathrm{m1}} + g_{\mathrm{m3}} + y_{14} + y_{24} + y_{34}) - C g_{\mathrm{m2}} g_{\mathrm{m3}} \tag{4.6f}$$

$$l_0 = g_{\mathrm{m1}} g_{\mathrm{m2}}(y_{14} + y_{24}) - g_{\mathrm{m2}} g_{\mathrm{m3}} y_{34} + g_{\mathrm{m1}} y_{34}(g_{\mathrm{m3}} + y_{14} + y_{24}). \tag{4.6g}$$

The reciprocal of the admittance expression gives the impedance of the circuit. Further simplifications are made using a first order approximation. In other words, expressions that contain products of two or more parasitic elements are discarded. The remaining elements have either none or only one parasitic element but in order to conserve and to observe the effect of s^3 terms, at most two parasitic elements are allowed with s^3 terms. The simplified equation has put into a rationalized form as

$$Z_{\mathrm{eq2}} = \frac{x_2 s^2 + x_1 s + x_0}{w_3 s^3 + w_2 s^2 + w_1 s + w_0}, \tag{4.7}$$

where simplified coefficients are presented as (also, in the following equations, y elements are replaced with their previously mentioned equivalent elements)

$$x_2 = C g_{\mathrm{m1}}(C_{\mathrm{gs1}} + C_{\mathrm{gs2}} + C_{\mathrm{gs4}} + C_{\mathrm{gd2}}) \tag{4.8a}$$

$$x_1 = C(g_{\mathrm{ds3}} g_{\mathrm{m1}} + g_{\mathrm{ds4}} g_{\mathrm{m1}} + g_{\mathrm{m3}}(g_{\mathrm{m1}} - g_{\mathrm{m2}})) + g_{\mathrm{m1}}(g_{\mathrm{m2}}(C_{\mathrm{gs1}} + C_{\mathrm{gd2}}) + C_{\mathrm{gs2}}(g_{\mathrm{m1}} + g_{\mathrm{m3}}) + C_{\mathrm{gs4}}(g_{\mathrm{m1}} + g_{\mathrm{m3}})) \tag{4.8b}$$

$$x_0 = g_{\mathrm{m1}} g_{\mathrm{m2}}(g_{\mathrm{ds3}} + g_{\mathrm{ds4}}) + g_{34} g_{\mathrm{m3}}(g_{\mathrm{m1}} - g_{\mathrm{m2}}) \tag{4.8c}$$

$$w_3 = C g_{\mathrm{m1}}(C_{\mathrm{gs2}} + C_{\mathrm{gd2}})(C_{\mathrm{gs1}} + C_{\mathrm{gs4}}) \tag{4.8d}$$

$$w_2 = C g_{\mathrm{m3}}(g_{\mathrm{m1}} - g_{\mathrm{m2}})(C_{\mathrm{gs2}} + C_{\mathrm{gd2}}) \tag{4.8e}$$

$$w_1 = g_{\mathrm{m3}}(C g_{\mathrm{ds3}}(g_{\mathrm{m1}} - g_{\mathrm{m2}}) + C_{\mathrm{gs2}} g_{\mathrm{m1}}(g_{\mathrm{m1}} - g_{\mathrm{m2}}) + g_{\mathrm{m1}} g_{\mathrm{m2}}(C_{\mathrm{gs1}} + C_{\mathrm{gs4}}) + C_{\mathrm{gd2}}(g_{\mathrm{m1}} - g_{\mathrm{m2}})(g_{\mathrm{m1}} + g_{\mathrm{m2}}) + C_{\mathrm{gs2}} g_{\mathrm{m3}}(g_{\mathrm{m1}} - g_{\mathrm{m2}})) \tag{4.8f}$$

$$w_0 = g_{\mathrm{m3}}(g_{\mathrm{m1}} g_{\mathrm{m2}} g_{\mathrm{ds4}} + g_{\mathrm{ds3}}(g_{\mathrm{m1}} - g_{\mathrm{m2}})(g_{\mathrm{m1}} + g_{\mathrm{m2}}) + g_{\mathrm{m2}} g_{\mathrm{m3}}(g_{\mathrm{m1}} - g_{\mathrm{m2}})). \tag{4.8g}$$

According to the results, one could see that the impedance of the circuit alters with frequency. Therefore, it is predicted that the circuit will not show the inductance behavior over the whole frequency spectrum. For instance, from Equation (4.7) and Equation (4.8a-g) it is obvious that the circuit will show a capacitive behavior at sufficiently high frequencies due to s^3 term in the denominator. Like most active inductance simulators this circuit also behaves inductively only at a certain frequency range and therefore, one should ensure that the circuit is operated in this frequency range to obtain inductive response.

4.3. Biasing of the Circuit

Biasing of the presented circuitry is crucial in order to satisfy the condition that all transistors work saturation region. As it was mentioned earlier, the arrows on each transistor do not indicate the type of the transistor in Fig. 4.1 rather; they indicate where the source connection of the each transistor should be placed. Therefore, one should choose the type of the transistors together with biasing process. For this chapter, it is thought that when the following type of transistors are chosen, the most suitable choice had been made out of 16 possible combination: M1: n-channel, M2: p-channel, M3: n-channel and M4: p-channel. First of all, current sources with 100 μA value are connected all nodes of the circuit in order to check whether all transistors work in saturation region. It is seen that there are transistors that do not operate in saturation region so; now, one should come up with design techniques that will allow all of the transistors to work in the saturation region. For this circuit two different techniques are used in implementation. First, diode connected MOSFETs are placed in different locations in the circuit as DC level shifters. For instance, two diode connected MOSFETs are connected back to back between gate connection of M4 and drain connection of M1. Another diode connected transistor is connected between gate connection of M3 and source connection of M2 then, a new capacitor C_1 is added to the circuit in order to hold current division balance; moreover, the matching condition that was mentioned in Section 4.2.1 has to be fulfilled in order to obtain a pure inductance. If the matching condition is not satisfied then, the outcome of the given circuit would

be a negative or positive resistor in series with an inductor. Therefore, current values that are flown through the MOSFETs are critical since they are closely tied up to the g_{m} values of the transistors. In addition, W/L ratios are important in order to make adjustments in the matching condition. Therefore, a final arrangement on the current sources' value has been made. In the circuit C and C_1 capacitor values are chosen as 50 pF and 100 nF respectively. Bias voltages for the circuit are chosen as +1.65 V and -1.65 V for V_{DD} and V_{SS} respectively. Final version of the biased circuit can be seen in Fig. 4.2. In addition, transistor sizes are shown in Table 4.1.

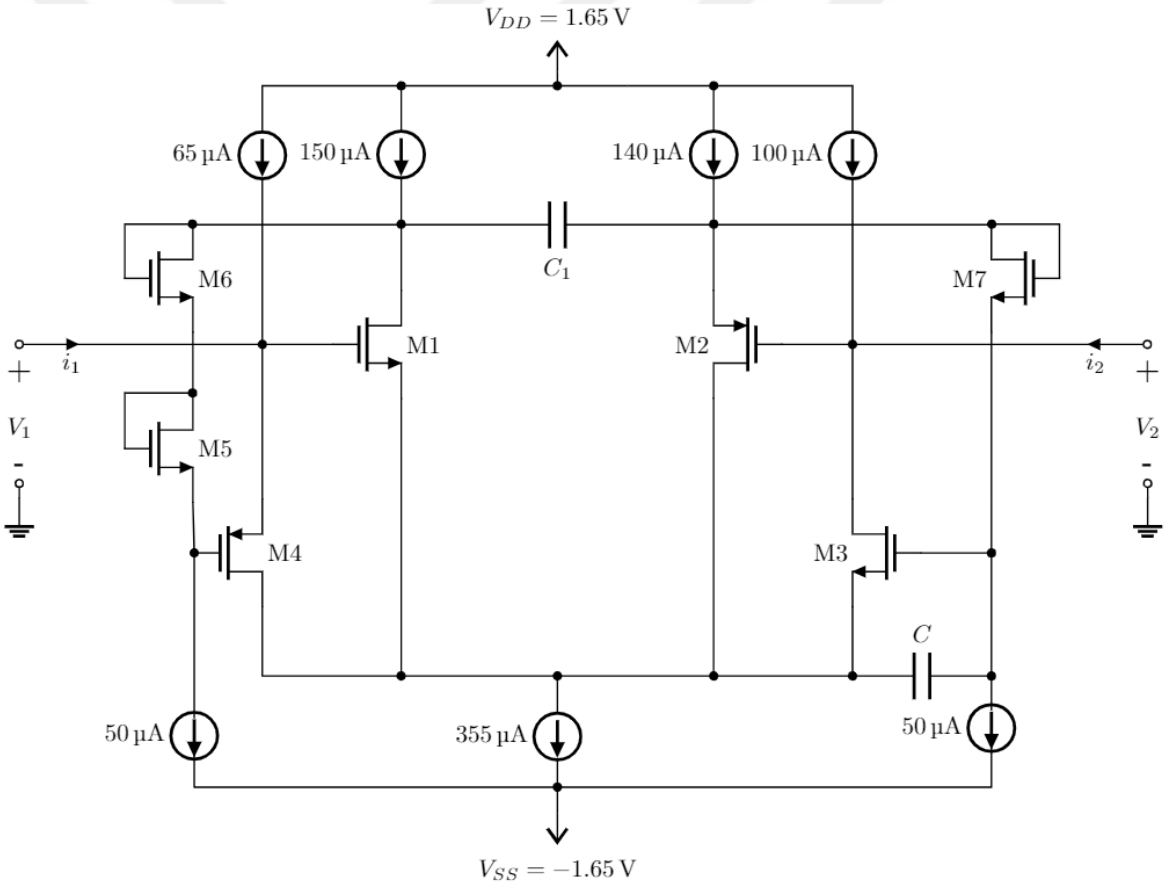


Figure 4.2. The circuitry after biasing.

Table 4.1. Transistor types and sizes of the presented circuit.

Transistor name	**Transistor type**	**W (μm)**	**L (μm)**
M1	NMOS	6	0.36
M2	PMOS	10.7	0.36
M3	NMOS	6	0.36
M4	PMOS	10	0.36
M5	NMOS	3.6	0.36
M6	NMOS	3.6	0.43
M7	NMOS	3.16	0.36

4.4. Simulation Results

In this section simulation results of the biased circuit are presented. The simulation platform that the simulations were carried is LTSPICE. First, the time domain analysis is performed and importance of the results are discussed. Second, frequency domain analysis is carried out in order to dive into the circuit's behavior at different frequencies.

To test the time domain response a triangular current waveform is applied to the inductor. According to inductors current voltage relationship *v=L(di/dt)*, a square voltage waveform is expected between the terminals. Fig. 4.3 and Fig. 4.4 show time the domain simulation results when a current source that has triangular waveform with 10 MHz frequency and 5-μA peak-to-peak current is applied to V_1 and V_2 terminals, where each time the other terminal is grounded. "Input Current" denotes applied input current and "Input Voltage" shows observed voltage on the input node. Fig. 4.3 shows simulation results when input current is connected to the V_1 port in Fig. 4.2 and Fig. 4.4 shows simulation results when input current source is connected to the V_2 port in Fig. 4.2. Both simulation results show same results except that there are different voltage offsets in each figure. According to the simulation results, the input swing voltage is more than 60 mV.

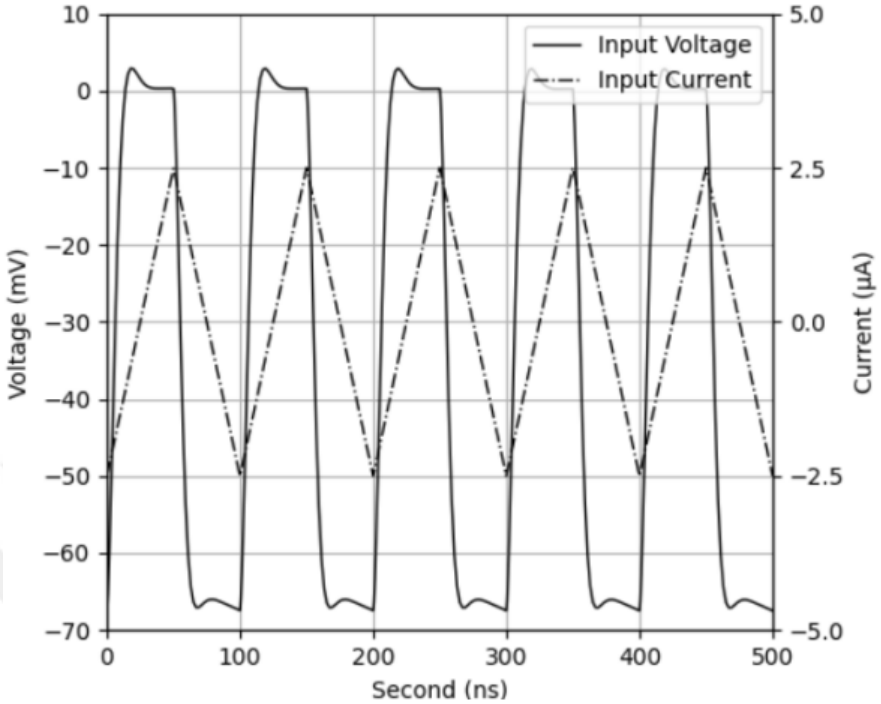


Figure 4.3. Time domain response when input current source is connected to V_1 port. Input voltage denotes the observed voltage on the input node.

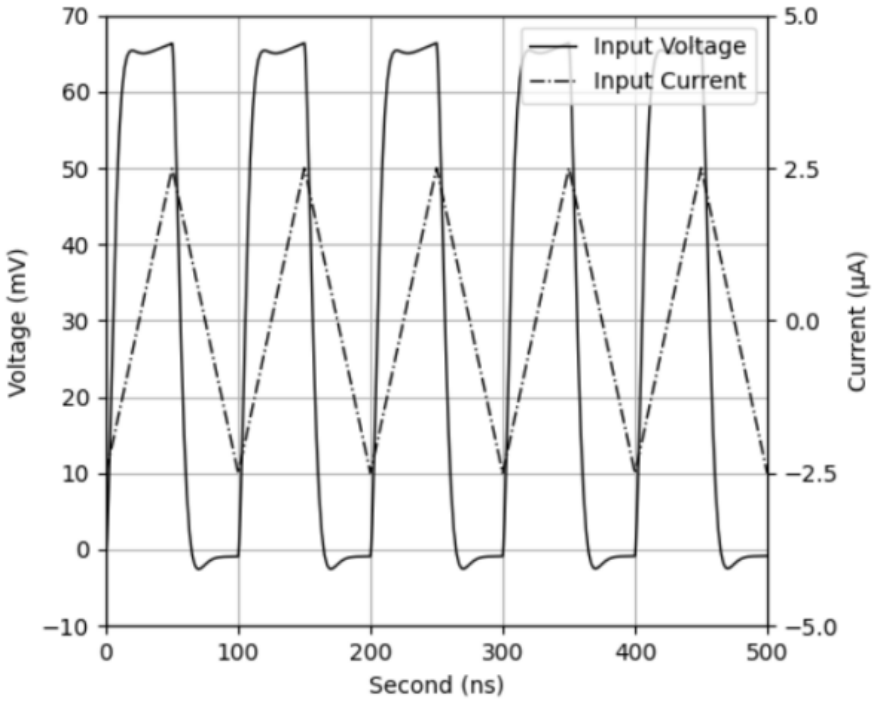


Figure 4.4. Time domain response when input current source is connected to V_2 port. Input voltage denotes the observed voltage on the input node.

Frequency domain simulations are necessary to evaluate the behavior of the circuit at various frequencies. Fig. 4.5 demonstrates the circuit's frequency response. The analysis results are valid when frequency domain analyses are made from both of the input connections. It can be seen that at low frequency, the circuit behaves as a resistive circuit, and when frequency is increased to a certain value the circuit starts to implement an inductive behavior and finally at very high frequencies the circuit imitates a capacitor behavior. In order to make comparison between the ideal inductor and the simulated inductor, an ideal inductor's frequency domain analysis with 0.285 mH inductance value is put –the same inductance value that active inductor circuit realizes. The frequency range that the circuit works as an inductor is between 350 kHz and 45 MHz. Here, the circuit is said to be inductive according to the definition in [2] as stated before. To sum up, it can be said that the proposed circuits operation frequency is sufficiently high for many applications.

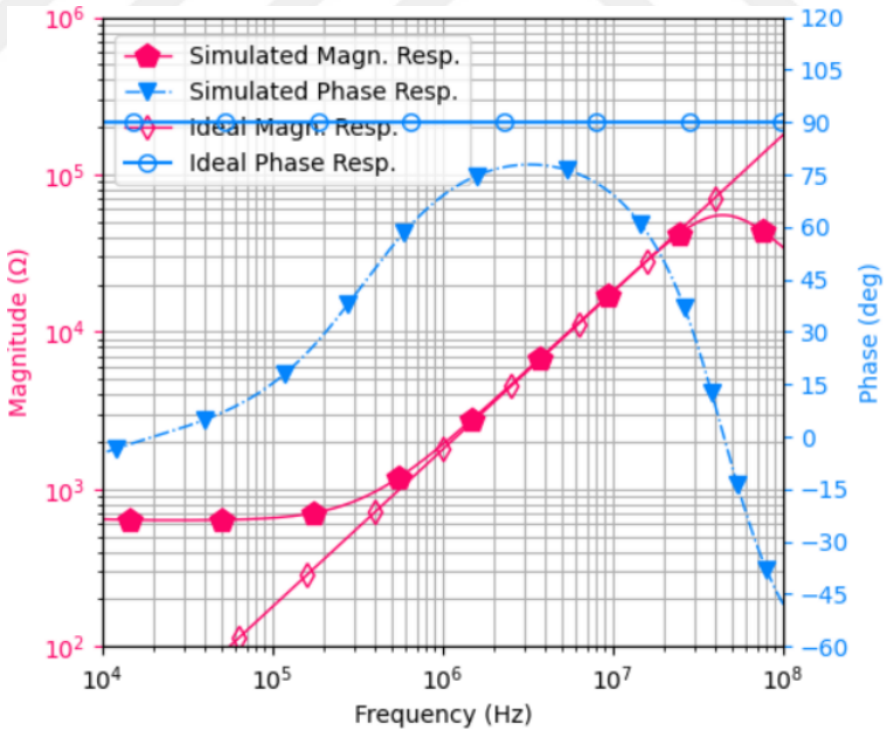


Figure 4.5. Frequency domain response of the circuit.

Moreover, Fig. 4.6 presents calculated results of the non-ideal input impedance -Z_{eq2}- magnitude vs. frequency. To observe the effect of the parasitics more clearly,

the ideal input impedance is plotted. In addition, the perfect matching condition is assumed when calculating the input impedances. APPENDIX C gives more detailed information about which parasitic component effects significantly magnitude response at low and high frequencies. Also, Table 4.2 presents transistor parameters of the AI circuit.

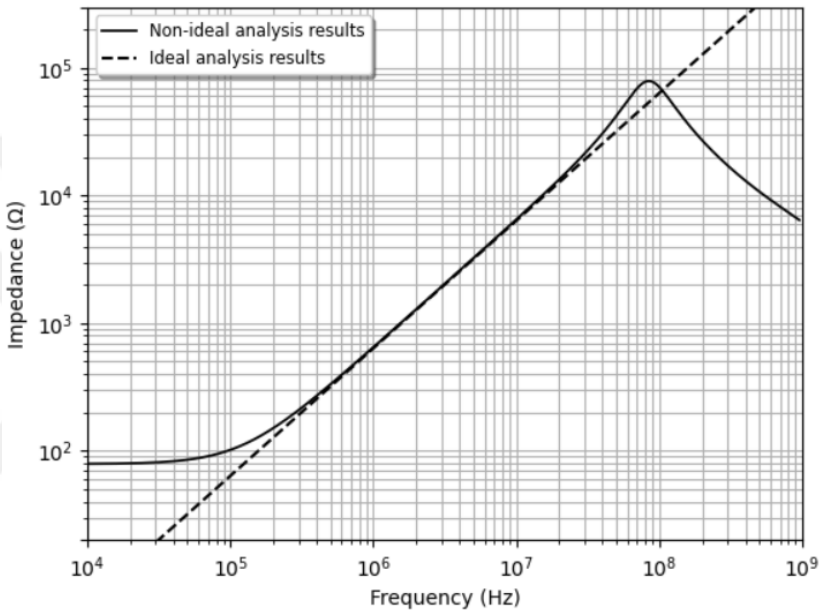


Figure 4.6. Theoretical non-ideal (Z_{eq2}) and ideal input impedance magnitudes of the circuit vs. frequency.

Table 4.2. Transistor parameters of the active inductor circuit.

Transistor name	g_m **(mA/V)**	C_{gs} **(fF)**	C_{gd} **(fF)**	g_{ds} **($\mu\Omega^{-1}$)**
M1	0.885	17.389	4.74	10.6
M2	0.567	31.0103	8.453	7.18
M3	0.871	17.389	4.74	12.5
M4	0.478	28.9816	7.9	7.95
M5	0.494	10.4334	2.844	6.75
M6	0.448	12.5415	2.844	5.43
M7	0.458	9.15819	2.4964	6.35

Table 4.3 presents outputs of the simulation results and non-ideal analysis of the circuit. It is seen that theoretical calculation of the inductance has important difference than what simulation results. Also at the low frequencies, simulation results show stronger resistive behavior than what is expected by the calculations. Maximum impedance results are similar and their occurance frequencies are relatively close to each other.

Table 4.3. Outputs of the simulation and non-ideal analysis.

Analysis type	***L*** **(mH)**	$\mathbf{max(Z_{eq2})}$ **(kΩ)**	$\mathbf{f_{max(Z_{eq2})}}$ **(MHz)**	$\mathbf{min(Z_{eq2})}$ **(Ω)**
Simulation results	0.285	55.2	44.67	633
Theoretical calculation	0.1	79	84.5	38

Quality factor is an important parameter when evaluating inductors. Fig. 4.7 plots quality factor and inductance of the active inductor circuit over the frequency spectra. In order to plot quality factor, the definition of quality factor that is described in [2] is re-referenced. The definition of the quality factor is presented as in Equation (2.9). It is seen that the highest Q value is achieved around 3.3 MHz with 4.7. At 10 MHz the Q value is found to be close to 2.6. For plotting inductance value Equation (2.8) is utilized as before. The reason behind using Equation (2.8) to plot inductance value is that the inductance has capacitor(s) at parallel. This could be observed from frequency domain analysis of the circuit. In the frequency domain of the circuit, it is seen that after 45 MHz the magnitude response of the circuit starts to decay. This is a sign of a capacitive behavior. Since the capacitor is parallel with inductance, at low frequencies, the overall impedance will be equal to the impedance of the inductor since the impedance of capacitor(s) will be too high. Using this idea the inductance of the circuit could be estimated by dividing the imaginary part of the impedance to 2πf as it is done in Equation (2.8).

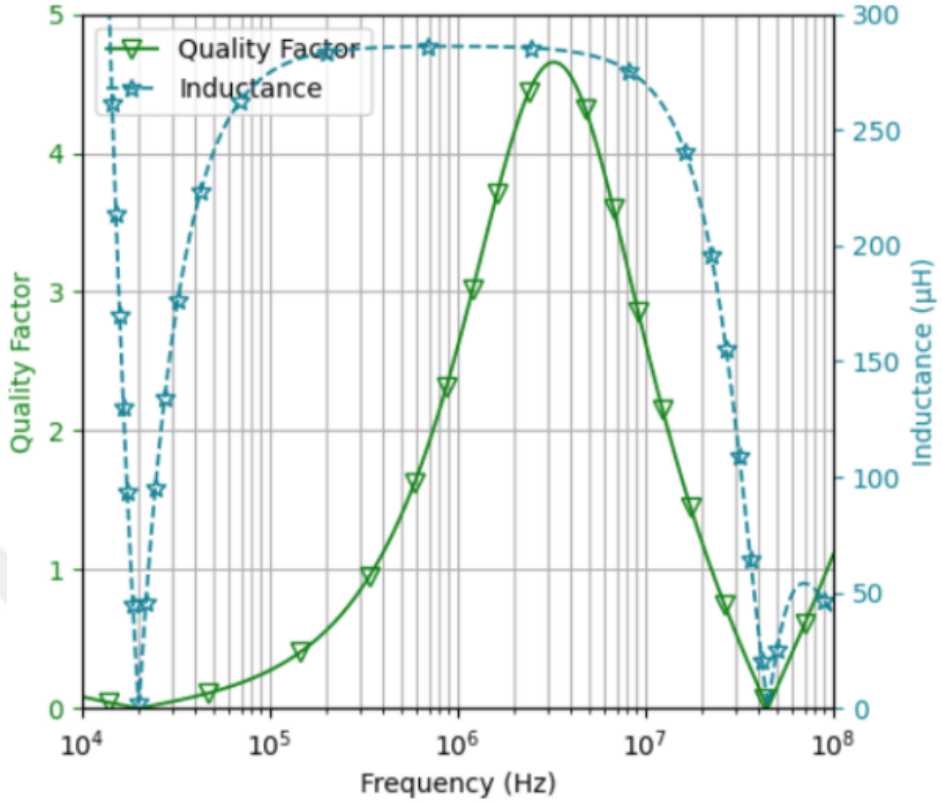


Figure 4.7. Quality factor and inductance value of the circuit.

It is also important to see the circuit performance when some error is presented into the components of the circuit. Here 5% error is introduced to MOSFETs mobility and capacitor values of C and C_1. Fig. 4.8 shows simulation results of the Monte Carlo analysis when 200 runs are performed. The results are valid for both of the circuit's input ports. According to the simulation results, it could be said that the circuit performs well in the region, where inductive operation is expected. In addition to Monte Carlo analysis, temperature analysis of the circuit is also performed on both of the circuit's input ports. Here, the temperature is changed from -40° Celsius to 100° Celsius with 10° steps. Fig. 4.9 demonstrates simulation results of the temperature analysis of the circuit. The simulation results are valid for the circuit's both input ports. Unlike, temperature analysis, simulation results indicate that the circuit is quite sensitive to the component quality variations at low frequencies in Monte Carlo analysis.

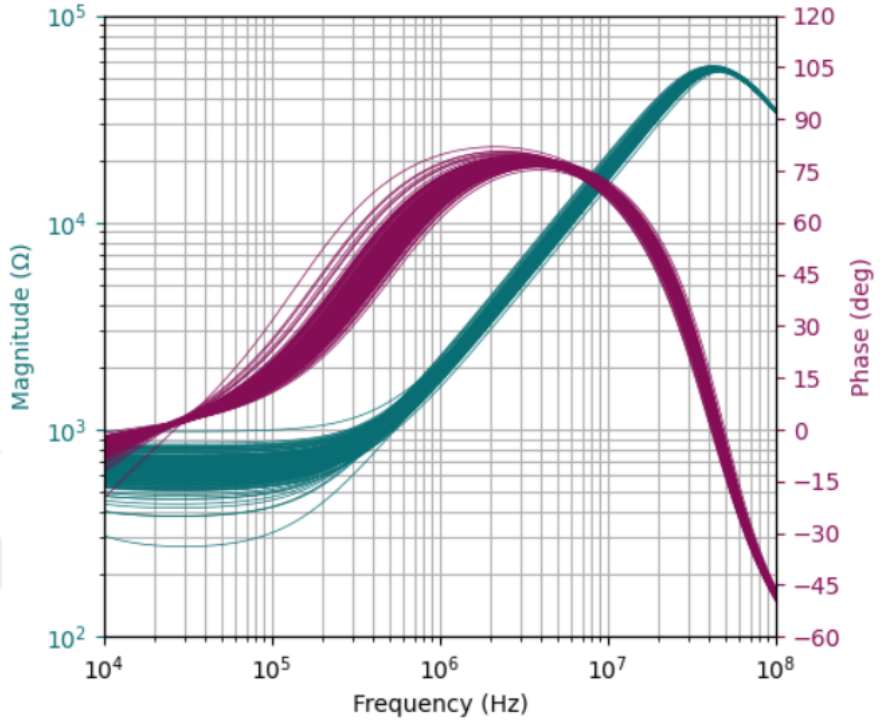


Figure 4.8. Monte Carlo analysis of the circuit.

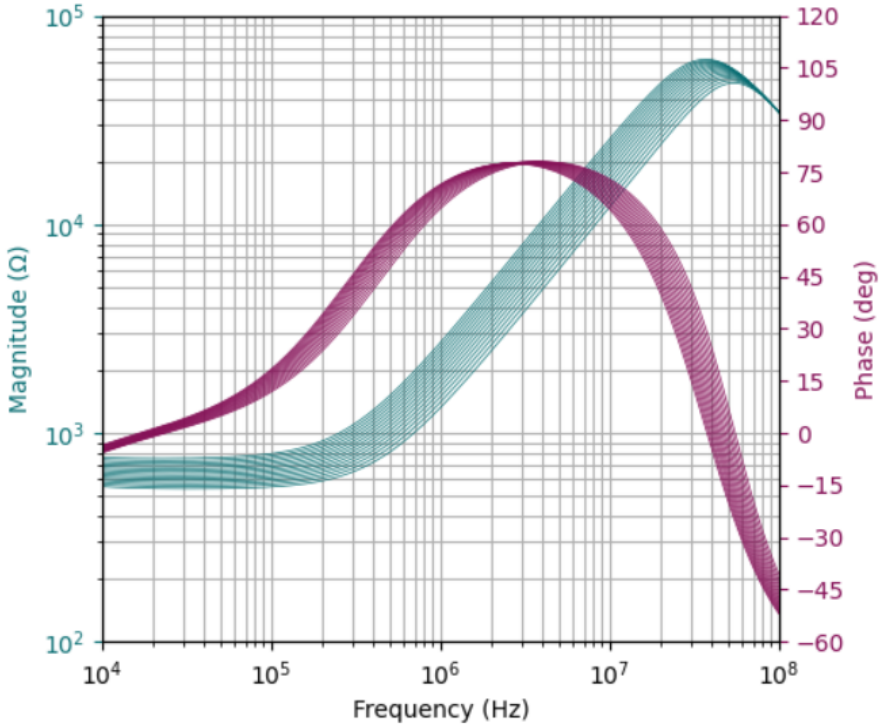


Figure 4.9. Temperature analysis of the active inductor.

4.5. Symmetrical Configuration of the Active Inductor

Differential or symmetrical circuits have many advantages over their single-ended version. Doubling peak-to-peak voltage, reduction in non-linearity, improvement in circuit stability are some of the benefits of differential configuration. In this work, mirror symmetrical configuration is achieved. Fig. 4.10 shows the symmetrical configuration of the single-ended circuit. It is obvious that the number of the transistors are doubled. Therefore, an increase in power consumption is clear. Since this circuit employs mirror symmetry, one could clearly say that the power consumption and chip area consumption will double but the outstanding advantages symmetrical configuration easily shadows its disadvantages and is much more desired in the usage of electrical circuit design.

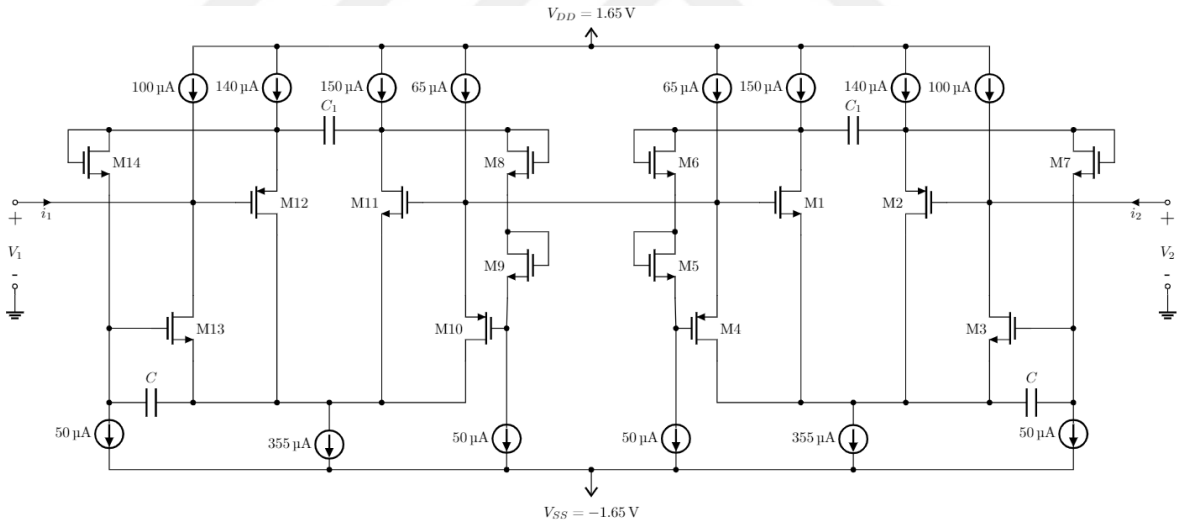


Figure 4.10. Symmetrical configuration of the circuit.

4.6. Simulation Results of the Symmetrical Circuit

In order to prove the circuit's abilities time and frequency domain analyses of the symmetrical circuit are done. The simulation settings and component values are exactly same with the single-ended configuration. Fig. 4.11 and Fig. 4.12 show time and frequency domain simulation results of the circuit respectively. The results are

valid for both of the input ports of the circuit.

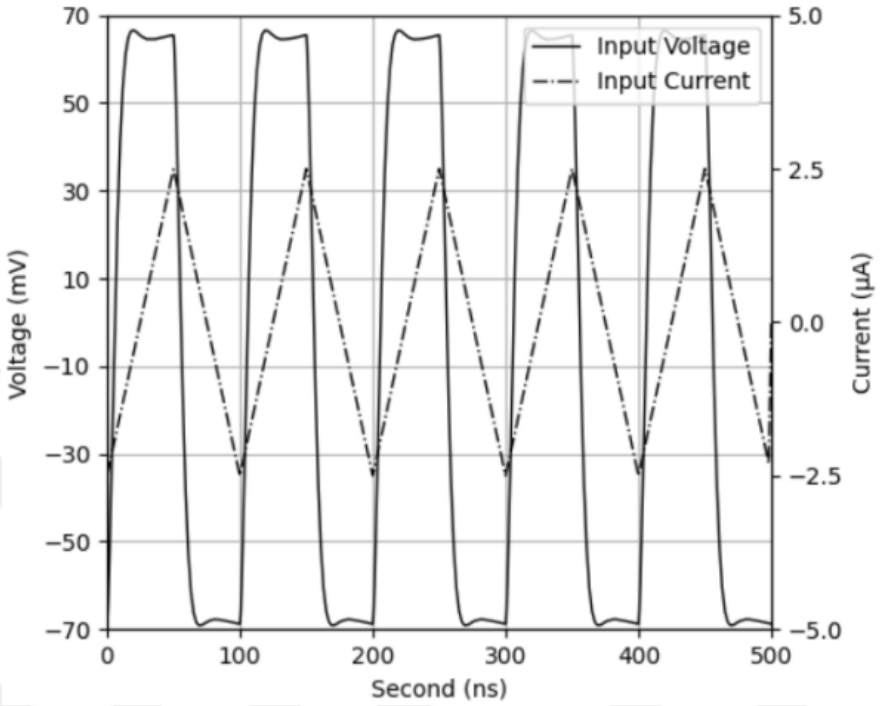


Figure 4.11. Time domain analysis of the symmetrical circuit.

Fig. 4.11 verifies expectations and shows that peak-to-peak voltage is doubled when input current is kept same and distortion is reduced in square waveform. Doubling peak-to-peak voltage indicates that the inductance value of the circuit is doubled; moreover, the voltage offsets that were presented in Fig. 4.3 and Fig. 4.4 disappeared thanks to the symmetrical configuration. The inductance value that is realized by the symmetrical configuration is found to be 0.566 mH –doubling the single-ended version. The frequency responses of the active inductor and ideal inductor circuit are in match. Overall, as it could clearly be seen from the results, symmetrical configuration is much more appealing than single-ended configuration. Similar to the single-ended version, Q value and inductance value of the symmetrical configuration is plotted in Fig. 4.13. In order to plot these values Equations (2.8) and (2.9) are used. Results validate again the doubling inductance value while resulting similar quality factor value. The highest Q value achieved around 3.3 MHz with roughly 4.5 and at 10 MHz Q value is close to 2.4.

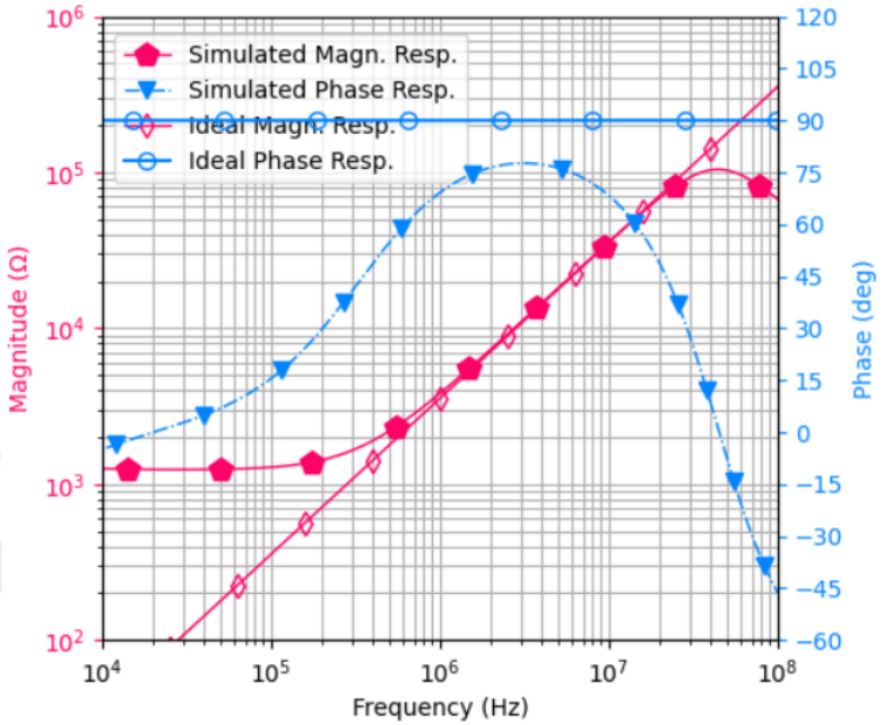


Figure 4.12. Frequency response of the symmetrical circuit.

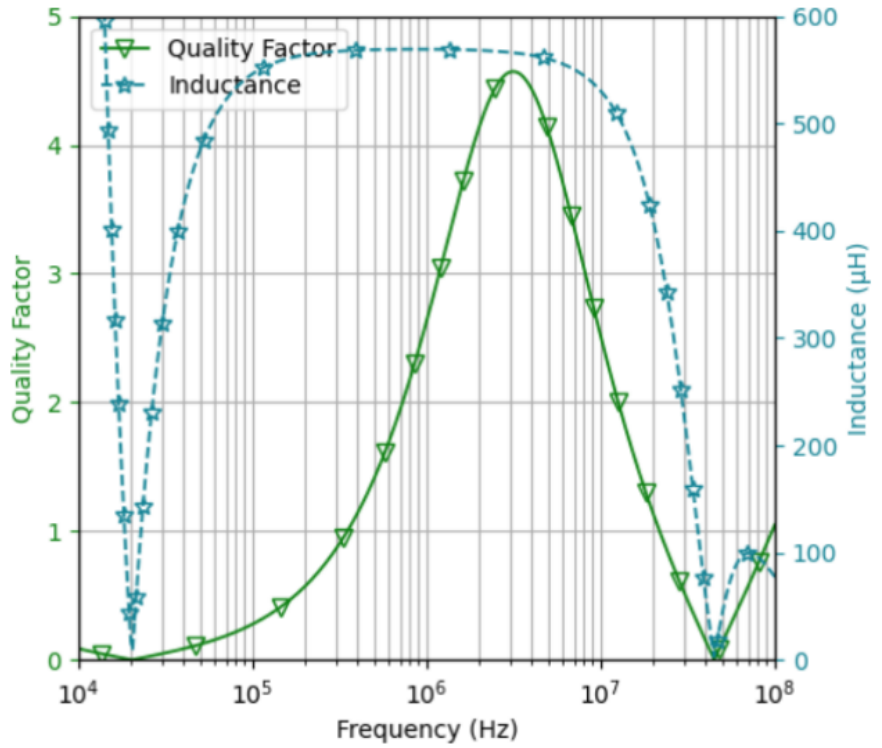


Figure 4.13. Inductance and quality factor of the symmetrical configuration.

Table 4.4 presents various qualities of the single-ended and symmetric connected circuit. The meanings of the variable are same and they were explained in the previous section in Table 3.1. Here, it could be clearly seen from the table that the main advantage of the symmetrical connected circuit is the doubling inductance value and peak-to-peak realized input voltage (there is one hidden benefit that could not be seen from the table, which is the removal of the offset voltage). Other than these benefits, operation frequency and Q related properties are pretty much same for both of the circuits.

Table 4.4. Single-ended vs symmetrical connected comparison.

Version	$L_{\mathbf{sim.}}$ **(mH)**	C **(pF)**	$i_{\mathbf{inpp}}$ **(μA)**	$v_{\mathbf{inpp}}$ **(mV)**	$f_{\mathbf{op.}}$ **(MHz)**	$Q_{\mathbf{max}}$	$f_{\mathbf{Q_{max}}}$ **(MHz)**
Single-ended	0.285	50	5	66	10	4.65	3.25
Symmetrical connected	0.566	50	5	132	10	4.57	3.15

Finally, Monte Carlo and temperature analyses of the symmetrical configuration of the active inductor circuit are performed. For the Monte Carlo analysis, the very same conditions that were used in single-ended configuration applied to the symmetrical circuit also. Fig. 4.14 shows Monte Carlo simulation analysis results of the symmetrical circuit. Monte Carlo analysis results for both of the circuit configurations, single-ended and symmetrical connected, seem quite similar. Temperature analysis of the differential circuit is also performed. Similar to single-ended configuration, temperature sweep from -40° Celsius to 100° with 10° steps is done. Fig. 4.15 shows temperature analysis simulation results of the symmetrical circuit. It is seen that the circuit performs similar performance compared to the single-ended version which is a well behavior, in different environment temperatures.

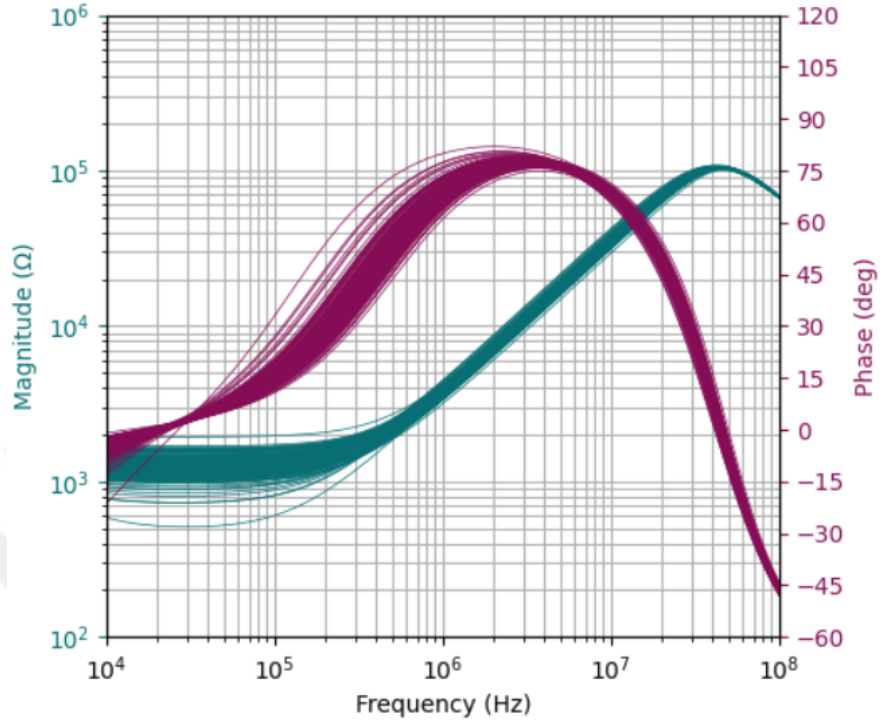


Figure 4.14. Monte Carlo analysis of the symmetrical configuration.

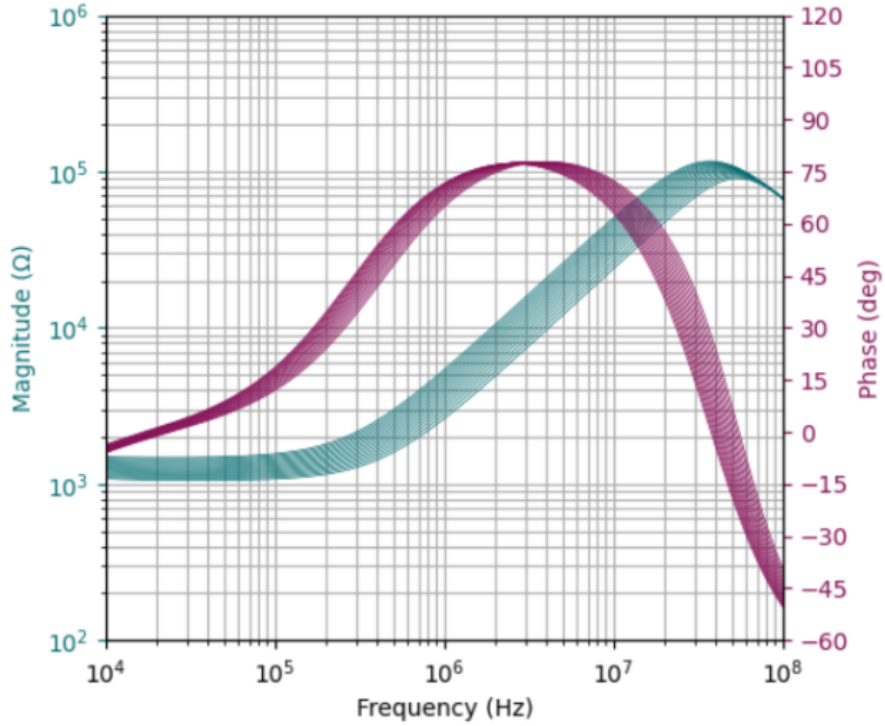


Figure 4.15. Temperature analysis of the symmetrical configuration.

4.7. Inductor Replacements of the Proposed Circuits

It is also important seeing that whether the given circuits fit well into a working system. For this reason, a 5^{th} order Low-Pass Butterworth Filter is constructed –Fig. 4.16. The normalized denominator polynomial in factored form is given as

$$A(s) = (s+1)(s^2 + 1.618s + 1)(s^2 + 0.618 + 1). \tag{4.9}$$

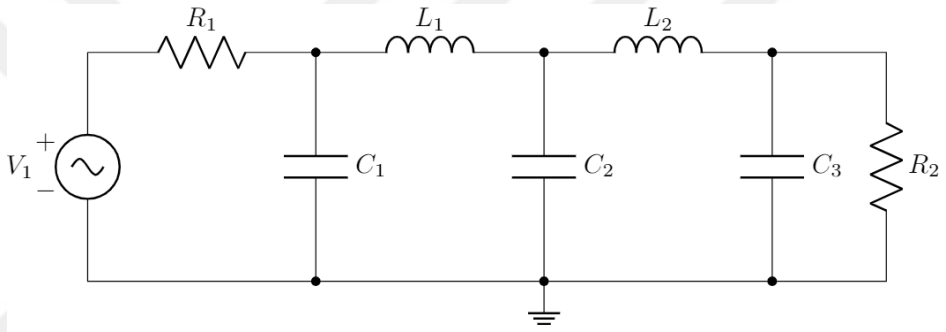


Figure 4.16. 5^{th} order Butterworth Low-Pass Filter.

From this polynomial coefficients of each term could be obtained and these coefficients are the normalized component values for 1 rad/s cutoff frequency. In order to reach target cutoff frequency and match the inductance values of the RLC circuit and the active inductor, frequency and impedance scaling operations are performed. The performed operations are done with respect to Equation (2.10) and Equation (2.11). The variables were explained in detail in previous chapters' related sections and could be seen if needed. Since single-ended and differential configurations of the active inductor circuit realize different inductance values two different filter circuits are constructed. The first filter circuit is constructed for the single-ended version and has following 10 MHz cutoff frequency and following component values: $R_1 = R_2 = 11029\ \Omega$, $C_1 = C_3 = 0.887$ pF, $C_2 = 2.87$ pF and $L_1 = L_2 = 0.285$ mH. The second filter circuit is constructed for the symmetrical configuration and has following component specifications (still 10 MHz cutoff frequency): $R_1 = R_2 = 21678\ \Omega$, $C_1 = C_3 = 0.45$ pF, $C_2 = 1.462$ pF and $L_1 = L_2 = 0.566$ mH. First, the filters are tested with ideal inductors and it is

seen that the circuits work without any problem then, the ideal inductors are removed from circuit and the simulated inductors are placed in their place. In both of the circuits when active inductors are placed instead of ideal inductors, the replacement was made for both L_1 and L_2 at the same time and simulation results will represent this replacement.

Fig. 4.17 and Fig. 4.18 show simulation results of the 5^{th} order Butterworth Low-Pass Filter with single-ended and symmetrical version of the active inductor circuit. Fig. 4.17 plots the comparison results of the filter circuit when constructed with ideal inductor and active inductor circuit for the single-ended version of the proposed AI circuit. If it is explained once more, "Mag. Res. with Ideal Ind." plots the filter's magnitude response when its constructed with an ideal inductor and "Mag. Res. with Active Ind." plots the filter's magnitude response when its constructed with the active inductor circuit. Similarly, "Phase Res. with Ideal Ind." plots the ideal inductor utilized filter's phase response and "Phase Res. with Active Ind." plots the active inductor utilized filter's phase response. The active inductor filter's cutoff frequency is found to be almost 7.2 MHz and the phase responses of the two circuits are matching quite fine until the targeted cutoff frequency.

Fig. 4.18 plots simulation results of the 5^{th} order filter when symmetrical version of the active inductor is employed. Notations of the labels in Fig. 4.18 are same with Fig. 4.17 as explained for it previously. Here, the cutoff frequency is found to be 7 MHz. The cutoff frequency difference is not found to be significant between single-ended and symmetrical active inductor employment in the filters. Similar to the single-ended case, the phase responses of the ideal and active inductor used filters are almost identical up to the targeted cutoff frequency.

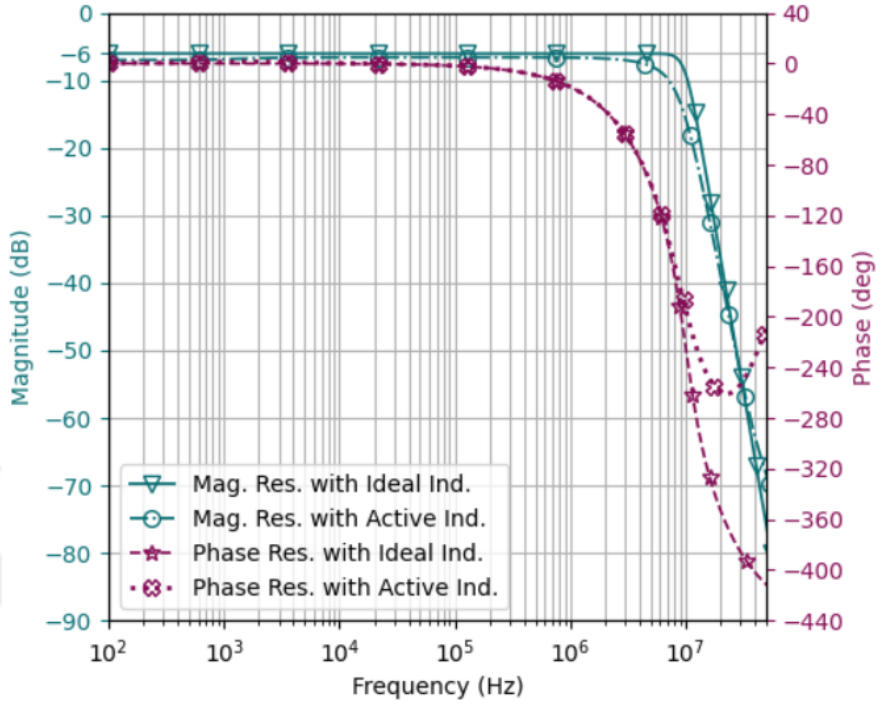


Figure 4.17. 5th order Low-Pass Butterworth filter response with the single-ended active inductor.

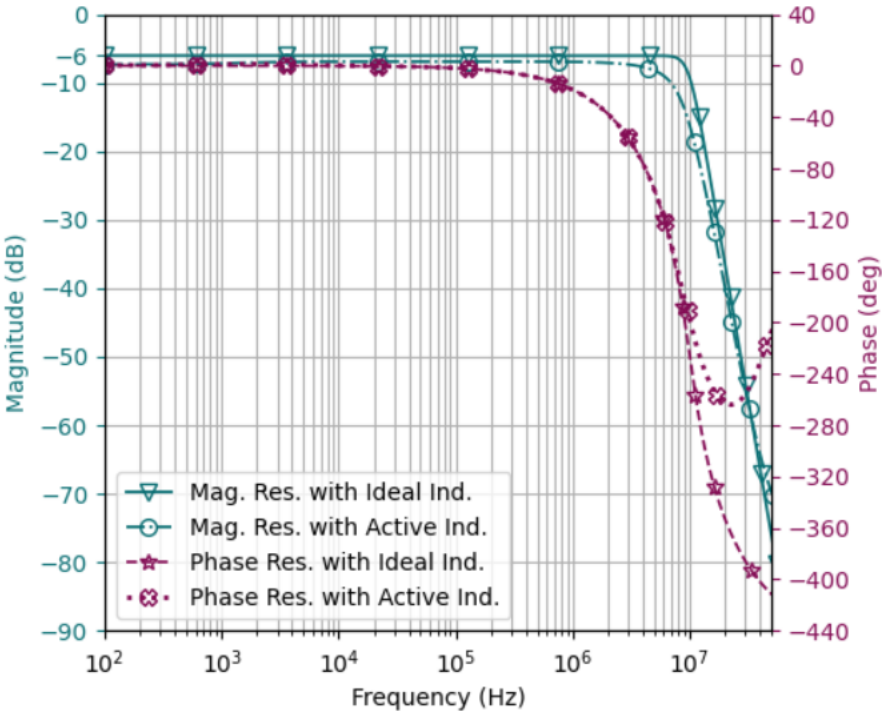


Figure 4.18. 5th order Low-Pass Butterworth filter response with the symmetrical active inductor.

4.8. Conclusion

A new simulated inductor is presented along with its symmetrical configuration. The simulated integrators are constructed by MOS-Only technique. Both of the circuits' analyses, biasing and simulation results are shown step by step. The single-ended circuit realizes 0.285 mH inductance and symmetrical configuration achieve 0.566 mH inductance value and both circuits work as an inductor at 10 MHz without any problem. The inductance values are tunable for both of the circuits. However, tuning inductance value requires tidy work because of the matching condition of the circuits. Like all active inductors, the proposed active inductors suffer from noise, and power consumption. Nevertheless, if used in an analog filter application for example as a band pass filter the noise problem is insignificant since noise is also reduced with decreasing bandwidth. Therefore the presented circuit is an alternative to existing active inductors when considering its tunability and high operation frequency.

5. TWO NOVEL NEGATIVE ACTIVE INDUCTOR REALIZATIONS

In this chapter two novel negative active inductor circuits are proposed. First, a three transistor negative active inductor circuit is designed and analyzed step by step and then simulations are carried out on LTSPICE simulation environment with 0.18 μm TSMC MOS technology. It is seen that the presented circuit shows poor performance. In order to boost the performance of the circuit, in the following sub-chapter, a symmetric connection technique is carried out by mirroring the core circuit. It is experienced that the symmetric connected circuit has superior performance than the single-ended version of the circuit. Simulation results of the symmetric connected circuit meet the expectations and the presented circuit result negative inductance value on the order of mH and it could be tuned. An application instance, for the symmetric connection, is given in order to cancel parasitic positive inductance at the end of the chapter.

5.1. Introduction

Passive inductors and their actively realized forms are widely used in analog electronic circuit applications. However, its undesired and unavoidable that parasitic inductances cause deterioration of performance in many cases. One solution to the problem is shortening of wires or reducing the physical size of the circuit which may not be possible in many circuits. In such problems negative inductor realizations may be a partial solution. Negative inductance can be realized by an active circuit and the concept appeared in the literature long ago [36]. A circuit could be labeled as a negative inductance circuit when its magnitude response increases linearly over the frequency spectrum and, in that very same frequency sprectra, the phase response of the circuit is negative 90°. Negative inductors represent nonfoster elements and this behavior can be obtained with help of active elements, for instance, in past, realization of negative inductor is achieved by using VAPAR [37]. The negative inductor circuits can be used

to cancel unwanted positive inductance values or to boost positive inductance value that is already available. Design of such negative inductor circuits is easy by using VCCS, and instead of VCCS, MOSFETs could be utilized in such applications due to their resemblance to VCCS in saturation region [12]. MOS-only technique is one possibility for the design due to the simplicity of obtained circuits [2, 38, 39]. This type of circuits are especially useful when reduction of chip area is desired. Note that such active realizations of inductors do not create magnetic flux, therefore, shielding is not needed. On the other hand these circuits dissipate power in contrast to ideal inductance behavior due to MOSFET usage and heating could be problem if not taken into account. In the following sections two negative inductor circuits are introduced and their analyses are carried out and their performances are presented in LTSPICE simulation environment. Active realization of negative inductance will be denoted as NAI in this chapter.

5.2. Novel Negative Active Inductor Circuits

The idea behind NAI is quite similar to positive active inductor. They have similar magnitude response but they differ in the phase response behavior. The phase response of NAI is -90° while positive active inductor has +90° of phase response. This behavior could be observed easily when an input source with sinusoidal waveform applied to the both elements. In the (pure) NAI the current will lead voltage by 90° whereas in the (pure) positive active inductor current will lag voltage by 90°.

5.2.1. Structure and Ideal Analysis of the Negative Active Inductor

The presented negative active circuit have only three transistors in the raw form. Fig. 5.1 shows the proposed circuit. In order to find the admittance matrix of the provided circuit, MOSFETs are replaced with their ideal AC equivalent model, which is a VCCS and routine analysis is carried out. It is proved that two port admittance

matrix of the presented circuit could be presented as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sL_{\mathrm{x3}}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{5.1}$$

According to the admittance matrix of the circuit, it is proved that the circuit presents a floating type active inductor circuit between ports V_1 and V_2. The realized inductance value by the circuit could be simplified and is presented as following

$$L_{\mathrm{x3}} = \frac{C(g_{\mathrm{gm2}} - g_{\mathrm{gm3}})}{{g_{\mathrm{gm3}}}^2 g_{\mathrm{gm2}}}. \tag{5.2}$$

The presented equation only holds when a certain condition is satisfied among circuit parameters. This certain condition is called as the matching condition of the circuit and found as

$$g_{\mathrm{m1}}g_{\mathrm{m2}} + g_{\mathrm{m2}}g_{\mathrm{m3}} = g_{\mathrm{m1}}g_{\mathrm{m3}}. \tag{5.3}$$

In the case that the matching condition is not satisfied, the inductance value that the circuit realizes deviates from Equation (5.2) and becomes as

$$Y_{\mathrm{id3}} = \frac{Cg_{\mathrm{m1}}g_{\mathrm{m2}}s + Cg_{\mathrm{m2}}g_{\mathrm{m3}}s - Cg_{\mathrm{m1}}g_{\mathrm{m3}}s - g_{\mathrm{m1}}g_{\mathrm{m2}}g_{\mathrm{m3}}}{Cg_{\mathrm{m2}}s}. \tag{5.4}$$

In a situation where the matching condition is not satisfied, Equation (5.4) indicates that the circuit will not be a pure inductive circuit and it will have a resistive component in series. Moreover, when Equation (5.2) is observed it is seen that this circuit could realize both negative and positive inductance value. The circuit realizes a negative inductance value in the case that g_{m3} is bigger than g_{m2} and in the other case when g_{m2} becomes bigger than g_{m3} a positive inductance value is resulted from the circuit topology. However, various tests are made in order to achieve positive inductance value but in LTSPICE environment the circuit did not realize a positive inductance value. The inductance value of the circuit could be tuned by changing values of C, g_{m2} and

g_{m3}. Note that the all analyses that are made in this section are ideal analysis without bias. Before moving forward, it is important to mention that the arrows that are on Fig. 5.1 only indicate source connections of the MOSFETs.

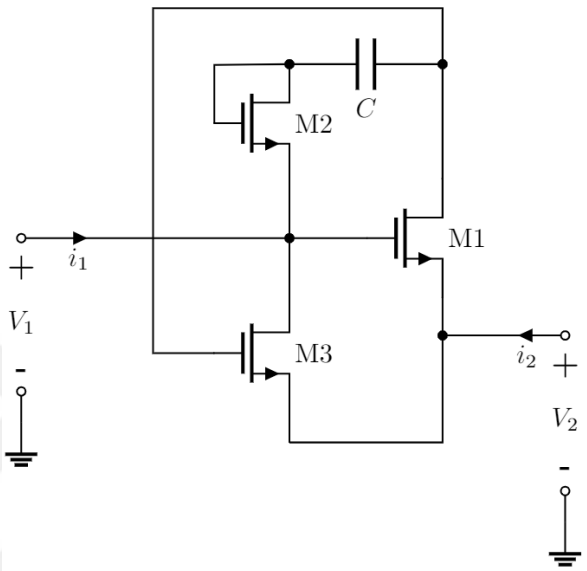


Figure 5.1. The proposed negative active inductor circuit.

5.2.2. Non-ideal Analysis of the Circuit

As mentioned in Sec. 5.2.1, ideal model of the MOSFET were used in ideal analysis of the circuit which means that the parasitics of the MOSFET, C_{gs}, C_{gd} and g_{ds} were omitted. Therefore, the results of Sec. 5.2.1 holds probably under a certain operation frequency range. Above or below this frequency range the behavior of the circuit could change. In other words outside of this frequency range the parasitic elements can no longer be omitted. Therefore, non-ideal analysis of the given circuit is required in order to fully characterize the behavior of the presented circuit. In this section non-ideal analysis of the proposed circuit is presented. To do this parasitics of the MOSFET, C_{gs}, C_{gd} and g_{ds} are included. The admittance of the circuit should be recalculated in order to analyze the circuit's behavior in more detail. The admittance of the circuit could be obtained by I_1/V_1 while grounding V_2. The admittance expression is found to be quite complicated for the presented circuit; moreover, the impedance

expression of the circuit is more attractive and useful than the admittance because one could plot magnitude response of the circuit with the impedance expression. Therefore, admittance expression of the circuit is inversed in order to obtain the impedance. In order to simplify the impedance expression a first order simplification is made, where a sub-expression that has the product of two or more parasitic element is omitted in the circuit. However, in order to not to lose high order terms, two parasitic terms are allowed in the denominator for s^4 terms in Equation (5.5). The expression for the impedance of the circuit could be presented as

$$Z_{\text{eq3}} = \frac{r_3 s^3 + r_2 s^2 + r_1 s + r_0}{p_4 s^4 + p_3 s^3 + p_2 s^2 + p_1 s + p_0}, \tag{5.5}$$

where coefficients are presented as following (the last subscript of the terms denote the number of the transistor)

$$r_3 = C(C_{\text{gd1}} + C_{\text{gd3}})(g_{\text{m2}} - g_{\text{m3}}) \tag{5.6a}$$

$$r_2 = (C(C_{\text{gs2}} + C_{\text{gs3}}) + (C_{\text{gd1}} + C_{\text{gd3}})g_{\text{m2}})(g_{\text{m2}} - g_{\text{m3}}) \tag{5.6b}$$

$$r_1 = (C_{\text{gs3}}g_{\text{m2}} + C(g_{\text{ds1}} + g_{\text{ds2}} + g_{\text{m2}}))(g_{\text{m2}} - g_{\text{m3}}) \tag{5.6c}$$

$$r_0 = g_{\text{ds1}}g_{\text{m2}}(g_{\text{m2}} - g_{\text{m3}}) \tag{5.6d}$$

$$p_4 = C(C_{\text{gd1}} + C_{\text{gd3}})(C_{\text{gs1}} + C_{\text{gs3}})(g_{\text{m2}} - g_{\text{m3}}) \tag{5.6e}$$

$$p_3 = -C(C_{\text{gd1}} + C_{\text{gd3}}){g_{\text{m3}}}^2 \tag{5.6f}$$

$$\begin{aligned} p_2 = &-((C_{\text{gd1}} + C_{\text{gd3}})g_{\text{m2}}{g_{\text{m3}}}^2) + C(C_{\text{gs1}}g_{\text{m2}}(g_{\text{m2}} - g_{\text{m3}}) \\ &+ C_{\text{gs3}}g_{\text{m2}}(g_{\text{m2}} - g_{\text{m3}}) - C_{\text{gs2}}{g_{\text{m3}}}^2) \end{aligned} \tag{5.6g}$$

$$p_1 = C_{\text{gs2}}g_{\text{m2}}{g_{\text{m3}}}^2 + C({g_{\text{ds1}}}{g_{\text{m2}}}^2 + g_{\text{ds3}}g_{\text{m2}}(g_{\text{m2}} - g_{\text{m3}}) - g_{\text{ds2}}{g_{\text{m3}}}^2) \tag{5.6h}$$

$$p_0 = g_{\text{m2}}(g_{\text{ds2}} + g_{\text{m2}}){g_{\text{m3}}}^2. \tag{5.6i}$$

The impedance expression shows that the frequency response is quite complicated and changes over the frequency spectra. It is strongly probable that the inductive behavior of the circuit will be available for limited frequency range. In addition, it is clear that at very high frequencies the circuit will show capacitive behavior because the degree

of denominator is higher than the degree of the numerator.

5.3. Biasing of the Circuit

In order to make proposed circuit work as expected, the type of the transistors should be chosen and then the circuit should be biased. It is desired that all transistors to work in saturation region so that they could act as a VCCS. Also, it is highly desired to maximize the number of the n-channel MOSFETs due to well-known reasons. Theoretically eight different transistor combinations could be chosen for the given circuit since there are three transistors. However, since the aim is to make all transistors work in saturation region, the appropriate biasing combination must be found that will make all transistors work in saturation region, if possible without using an extra design technique. For the transistors that are shown in Fig. 5.1, it is predicted that choosing all transistors the same type would make all transistors in saturation region; moreover, n-channel selection is preferred as mentioned before. Next, the necessary current sources are connected to the nodes of the circuit to run a DC analysis and check if indeed all transistors are operating in saturation region. If not, necessary iterations should be applied. Also, the matching condition as it was mentioned in Sec. 5.2.1 must be taken into account. Fig. 5.2 shows modifications in schematics of Fig. 5.1 after biasing is applied. The circuit is supplied with +0.9 V and -0.9 V supply voltages for V_{DD} and V_{SS} respectively. Table 5.1 provides the transistor sizes for the circuit. Also, the value for C is chosen as 1 nF in all of the following sections and simulations (until a new circuit design is proposed).

Table 5.1. Transistor types and sizes of the NAI circuit.

Transistor name	**Transistor type**	**W (μm)**	**L (μm)**
M1	NMOS	10	0.5
M2	NMOS	4	0.5
M3	NMOS	10	0.5

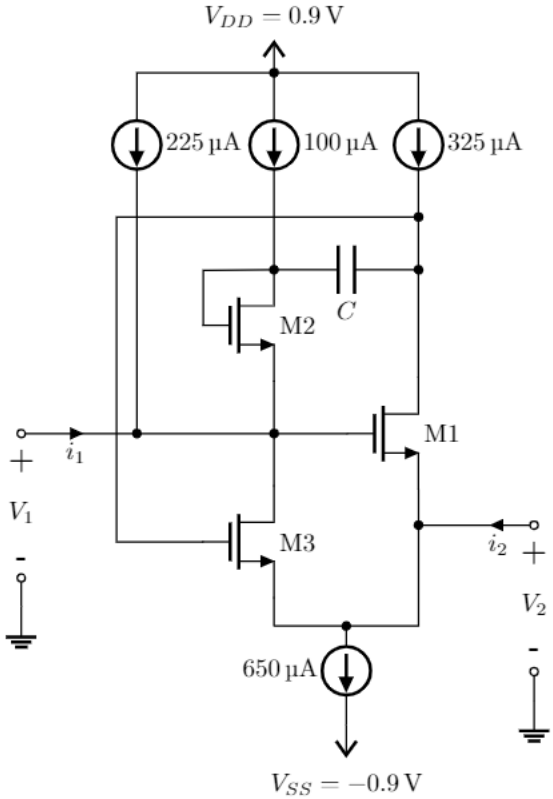


Figure 5.2. The circuit after biasing.

5.4. Simulation Results

In order to fully characterize the circuits, various simulations should be carried out. First, time domain analysis of the circuit is performed and then, frequency domain analysis of the circuit is performed. Time domain analysis of the negative inductance circuit is similar to time domain analysis of a positive inductance circuit. For the input of the circuit, a current source that has 100 μA peak-to-peak current and 10 kHz frequency with triangular waveform is applied and a square wave is expected at the input voltage node. However, when current has positive slope, it is expected that input voltage should be at low level instead of high level. This difference stems from the negative inductance that the circuit provides instead of positive inductance, as previously explained. Fig. 5.3 and Fig. 5.4 provide time domain analysis results of the negative inductive circuit when input current source is connected to the V_1 and V_2 ports respectively. In the figures, "Input Current" plots applied input current and "Input Voltage" plots the resulted voltage at the same input node. In the following

figures same notations will have same meaning.

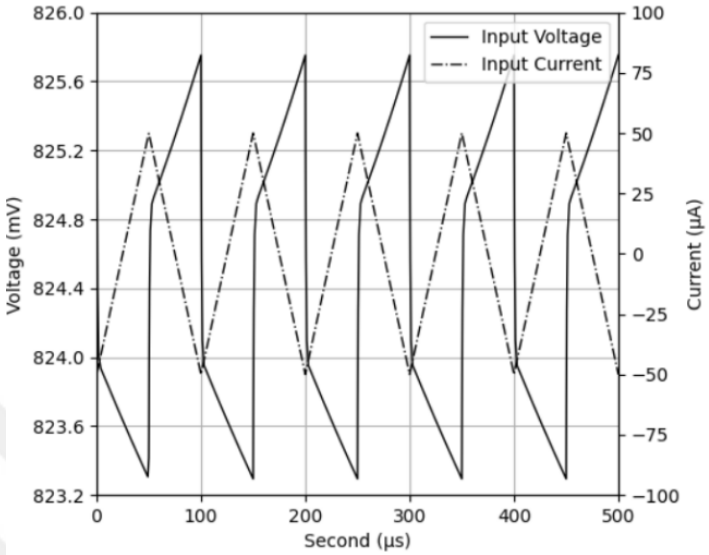


Figure 5.3. Time domain analysis of the NAI when input is connected to V_1.

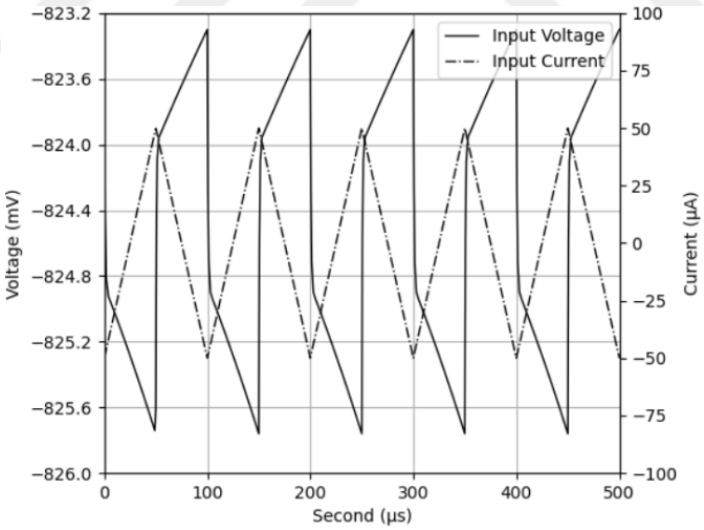


Figure 5.4. Time domain analysis of the NAI when input is connected to V_2.

Simulation results indicate that the smooth square wave is not being able to be achieved. This stems from not fulfilling matching condition. Also, there is very high V_{os} that makes the circuit's usage quite challenging. Therefore, it is seen that this circuit is not suitable for usage in this form. It is also important to see how wide is the frequency range that allows the presented circuit to work as a negative inductor.

Fig. 5.5 shows frequency domain analysis of the presented circuit. The results are valid for the circuit's both of the input ports. For the circuit, it can be said that the operation frequency region with inductive behaviour is quite low.

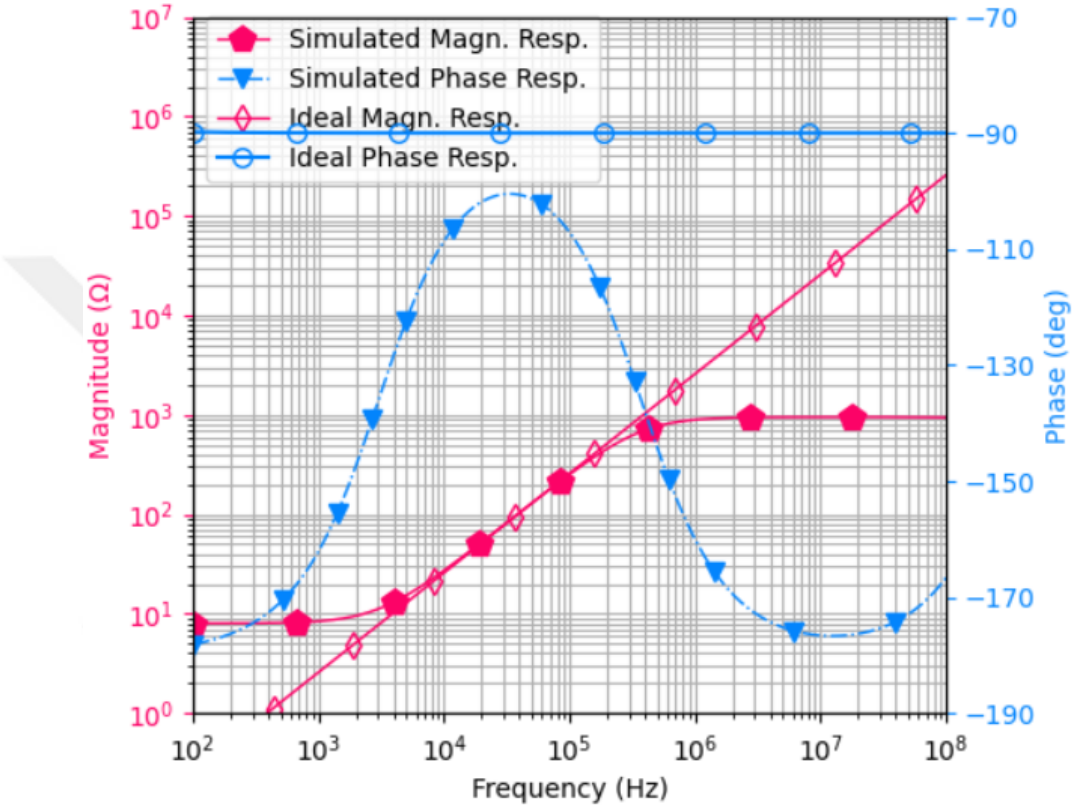


Figure 5.5. Frequency domain analysis of the circuit.

Theoretical impedance expressions that were presented in Equations (5.2), (5.5) and (5.6a-i) for ideal and non-ideal -Z_{eq3}- cases are also plotted over frequency and could be seen in Fig. 5.6. The simulation results and theoretical analysis show similarity but there is one important difference that manifests itself. Theoretical results show that the circuit has weaker resistive behavior at high frequencies in non-ideal analysis when compared with the simulation results. Other than this difference, theoretical results and simulation results are quite in match. The transistor parameters that are used in order to plot Fig. 5.6 could be observed in Table 5.2. These parameters are utilized along with Equations (5.5) and (5.6a-i) to plot theoretical input impedance of the circuit. A detailed analysis that presents the parasitic components, which have the strongest impact at extreme frequencies is given in APPENDIX D.

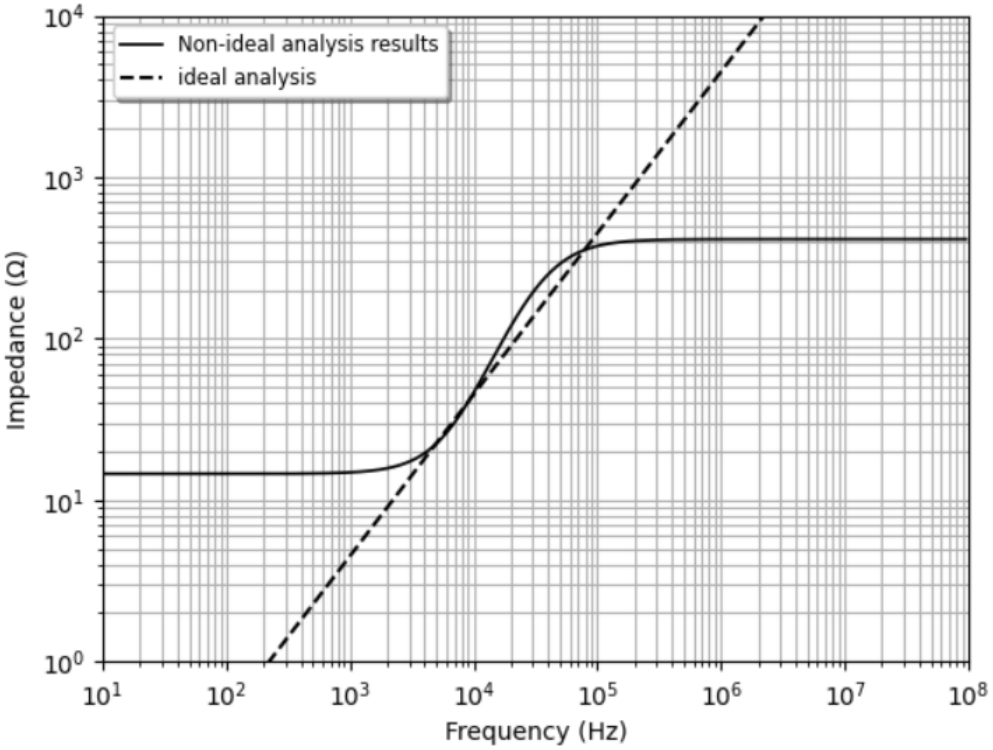


Figure 5.6. Theoretical non-ideal (Z_{eq3}) and ideal input impedance magnitudes of the circuit vs. frequency.

Table 5.2. Transistor parameters of the NAI circuit.

Transistor name	g_m **(mA/V)**	C_{gs} **(fF)**	C_{gd} **(fF)**	g_{ds} **($\mu\Omega^{-1}$)**
M1	1.58	37.18	7.9	20.5
M2	0.575	14.872	3.16	7.03
M3	1.48	37.18	7.9	17.8

Table 5.3 presents comparison results between simulation results and non-ideal analysis. According to the theoretical calculation, realized inductance is bigger (magnitude wise) than what simulation is resulted. Other results are close to each other; moreover, it is seen from Fig. 5.5 and Fig. 5.6 that the shapes of the magnitude response look quite alike in simulation and non-ideal analysis.

Table 5.3. Results of the simulation and non-ideal analysis.

Analysis type	***L*** **(mH)**	**max(Z_{eq2})** (Ω)	**$f_{max(Z_{eq2})}$** **(MHz)**	**min(Z_{eq2})** (Ω)
Simulation results	-0.41	950	100	8
Theoretical calculation	-0.72	413	100	14

In addition, quality factor and inductance value of the circuit are plotted over the frequency spectra in order to obtain more information about the circuit. Fig. 5.7 presents the inductance and quality factor values over the frequency range. The inductance value of the circuit is plotted by using Equantion (2.8) once more. Equation (2.8) holds-on mostly for inductive and resistive circuits. When the circuit's theoretical routine analysis and simulation results are examined it is clear that inductor circuit does not only implement an inductor, rather as it is seen that it realizes inductor, resistor and capacitor. Therefore, it could be stated that overall the equivalent circuit is a possible combination of these elements. At low frequencies enough, the capacitor impedance will be quite high and the impedance that will seen will be roughly equal to the inductor's impedance and by dividing this impedance to ω, the inductance value of the inductor could be found as mentioned before. Hence, Equation (2.8) will be valid only at low frequencies enough for the given circuit. This low frequency could be predicted from Fig. 5.7 and could be estimated as 100 kHz. To calculate quality factor of the circuit, the explanation for quality factor that is presented by [2] is reutilized. Equation (2.9) presents the quality factor formula. In both of the Equations (2.8) and (2.9), $IM\{1/Y_{eq}\}$ is the imaginary part of the input impedance of the active inductor circuit. Likewise, $RE\{1/Y_{eq}\}$ is the reel part of the input impedance of the circuit. According to the results, it could be observed that quality factor peaks at nearly 30 kHz frequency with nearly 5.4 and the inductance value for is roughly equal to -0.41 mH up to 100 kHz.

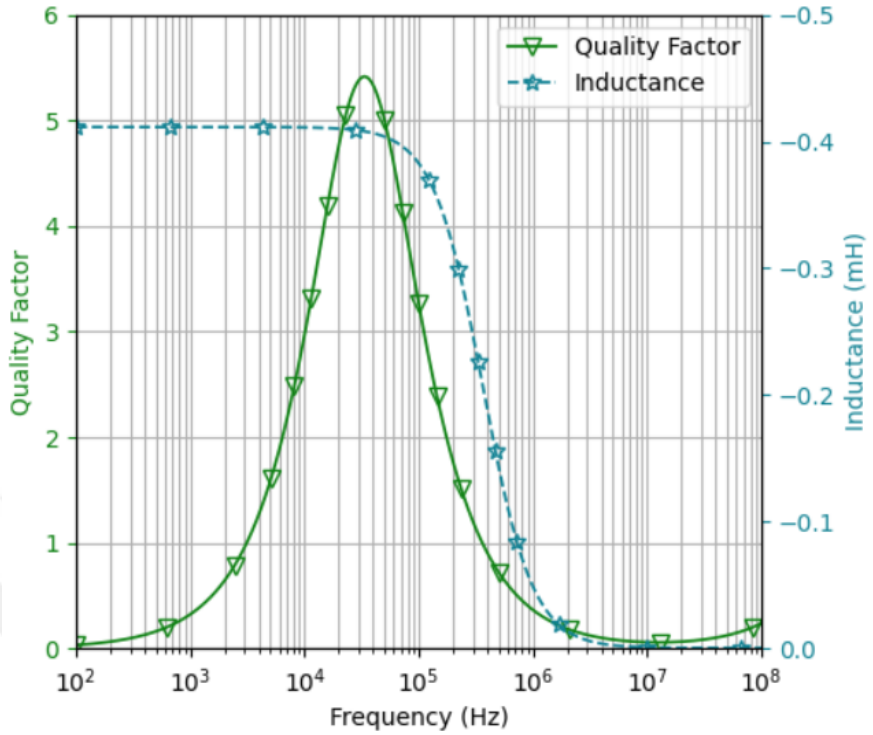


Figure 5.7. Inductance and quality factor of the circuit.

5.5. Symmetric Connection of the Proposed Circuit

Fig. 5.3. and Fig. 5.4 clearly show that the proposed circuit is not suitable for usage in applications because of the circuit's various drawbacks. The very first disadvantage of the circuit is very high offset voltage. Time domain analysis of the circuit indicates that the circuit has more than 800 mV V_{os}. In addition, the circuit does not realize pure negative inductor, it realizes a negative inductor that has a negative resistance in series. Therefore, the proposed circuit should be improved. Here, symmetric connection of the circuit is examined in order to boost the circuit's performance. The symmetric connection of the is achieved by mirroring the circuit. Fig. 5.8 shows the circuit's schematic. The transistor sizes are kept same with the single-ended version. Finally, a resistor R with 16 Ω is placed between the core circuits when connecting the circuits in order to cancel the negative resistance that was realized in the single-ended version. Also, capacitor value C is lowered to 0.15 nF in the new configuration.

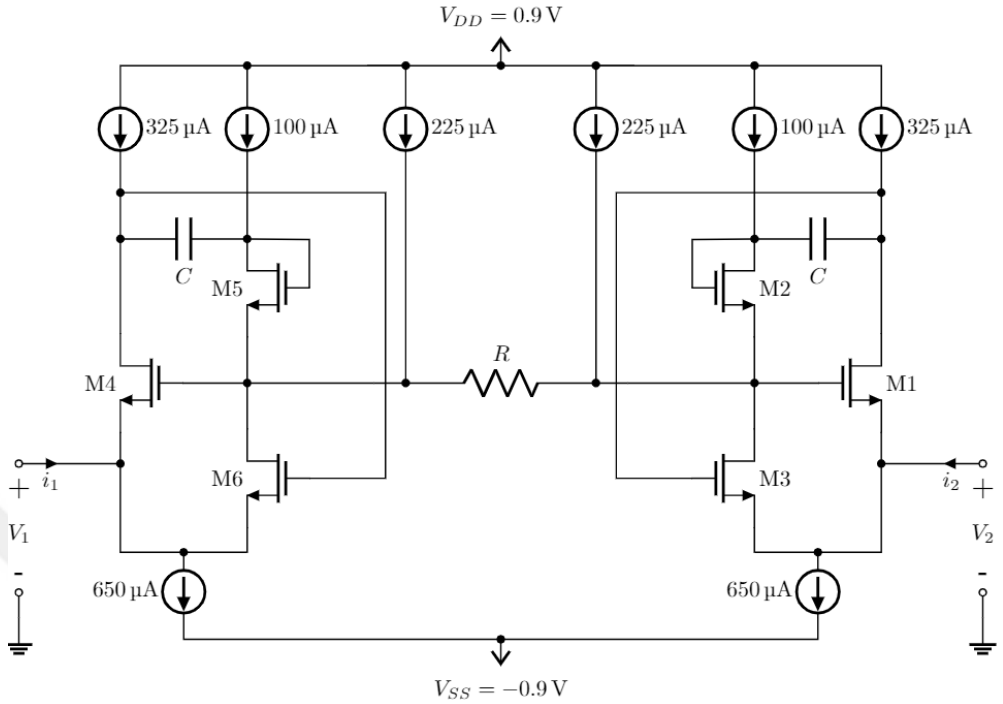


Figure 5.8. The symmetric connection of the circuit.

5.6. Simulation Results

In order to see the symmetric circuit's performance, similar simulations are performed. First, time domain analysis of the circuit is carried out. Fig. 5.9 shows the symmetric circuit's time domain simulation results. According to the results, it is clear that the symmetric circuit is superior than the single-ended version. The low swing voltage and high offset voltage problems are solved. Simulation results indicate that, with the new configuration, high swing voltage is achieved while removing offset voltage. The swing voltage is more than 30 mV. On the other hand, the swing voltage that was offered by single-ended version was around 2 mV; moreover, the operation frequency is improved dramatically by lowering the main capacitor value C. While offering these fruitful benefits, the circuit works at moderately high frequency, 333 kHz. The presented time domain analysis results are valid when input signal is connected to both of the possible input ports of the circuit.

Frequency domain analysis of the new circuit is performed to gain more information about the circuit. Fig. 5.10 shows simulation results of the analysis of the new

circuit topology. It is seen that the symmetrical circuit works as a negative inductance over a longer frequency spectra than the single-ended version. In addition, The realized inductance value of the new configuration is found to be -0.13 mH and this value could be adjusted by changing the circuit's component values and the impact of the circuit component effects on the realized inductance value could be seen in Equation (5.2).

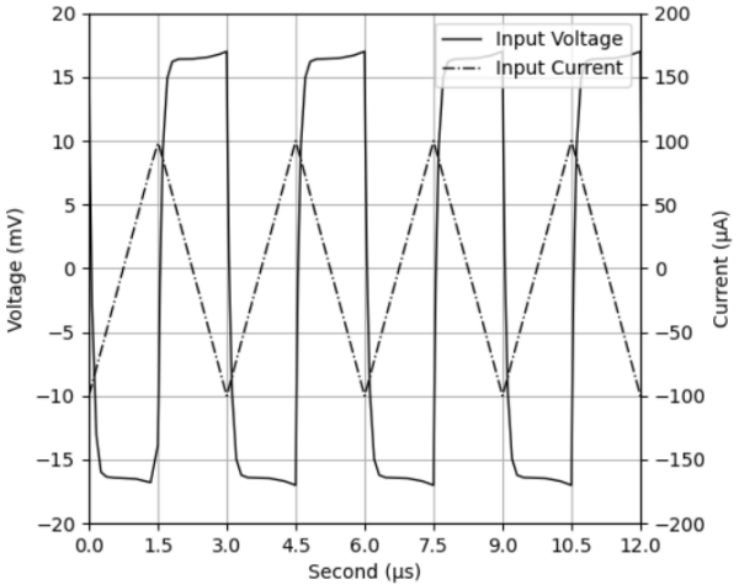


Figure 5.9. Time domain analysis of the circuit.

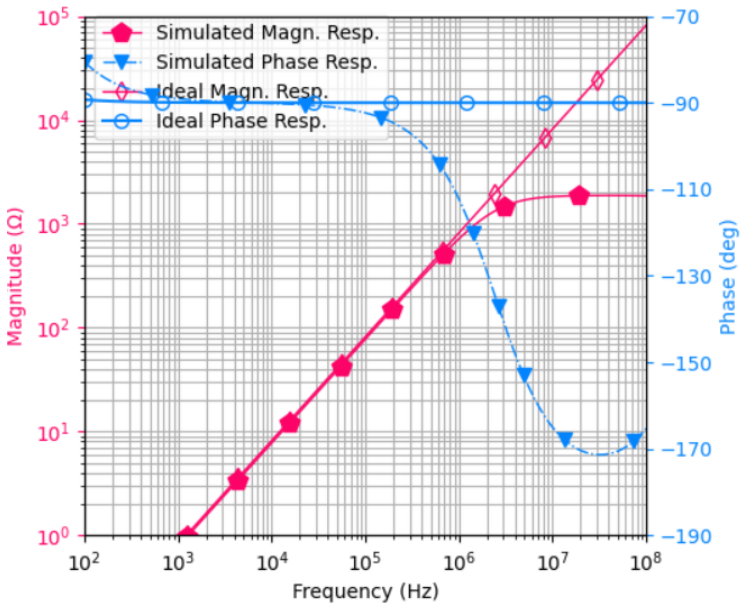


Figure 5.10. Frequency domain analysis of the symmetric circuit.

The inductance value and quality factor of the circuit are again plotted in order to see the new circuit's quality. Fig. 5.11 shows quality factor and inductance value over the frequency spectra. The formulas in Equation (2.8) and Equation (2.9) are utilised again in order to plot inductance value of the circuit. It is seen that the circuit reaches the quality factor of 18.810 at 6.3 kHz and at 333 kHz the quality factor is found to be 7.34. The inductance value is seen to be -0.13 mH from the figure, which verifies the previous foundings.

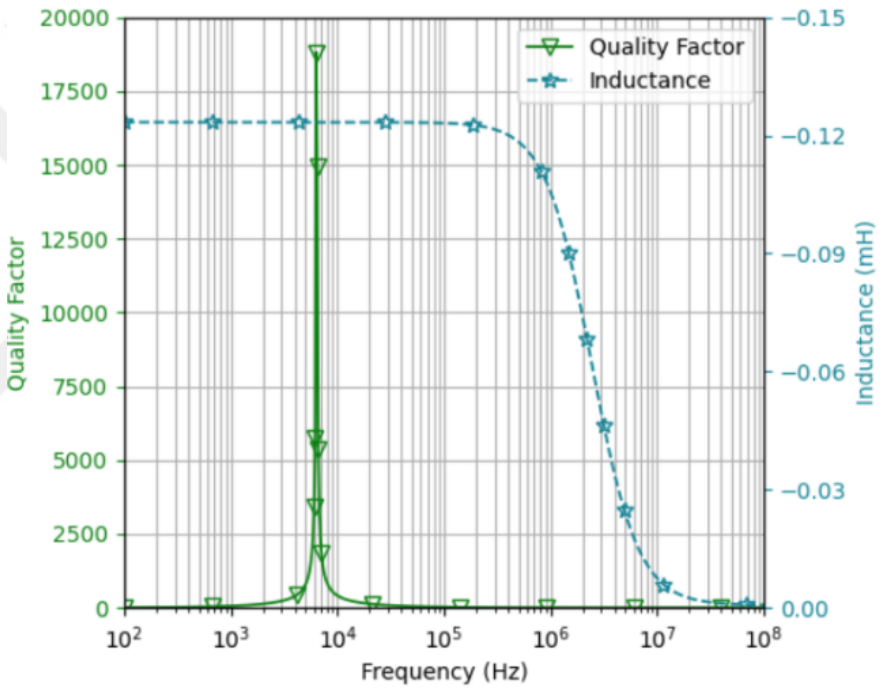


Figure 5.11. Quality factor and inductance of the symmetric circuit.

Table 5.4 presents the properties of the both single-ended and symmetrical connected circuit. The meanings of the variables are same as in Table 3.1 and their meanings were explained in Sec. 3.3. According to the numbers, it is seen that symmetric connected circuit realizes lower (in magnitude) inductance value than the single-ended version of the circuit. Nevertheless, realized peak-to-peak input voltage is much higher than the single-ended version but it doubles the input current. In addition, operating frequency of the symmetric connected circuit is much higher than the single-ended configuration. It is seen that the maximum offered Q value by symmetric circuit is extraordinarily high but it is achieved at a quite low frequency. However, at 333 kHz,

symmetric circuit has a Q value of 7.34, which is higher than the best offering of the single-ended configuration.

Table 5.4. Single-ended vs symmetrical connected comparison of the NAI circuit.

Version	$L_{\text{sim.}}$ **(mH)**	C **(nF)**	i_{inpp} **(μA)**	v_{inpp} **(mV)**	$f_{\text{op.}}$ **(kHz)**	Q_{max}	$f_{\text{Q}_{\text{max}}}$ **(kHz)**
Single-ended	-0.41	1	100	2.4	10	5.4	32.5
Symmetrical connected	-0.13	0.15	200	34	333	18810	6.309

Monte Carlo and temperature analyses are performed to test the symmetric circuit configuration's performance. Fig. 5.12 shows Monte Carlo analysis simulation results with 200 iterations while adding 5% error into the transistors' electron mobility and the circuit's capacitor value. The simulation results are valid for both of the input measurements. According to the simulation results, with variations, the circuit's magnitude response shows good stability. On the other hand, the circuit's phase response degrades dramatically at low frequencies. Fig. 5.13 demonstrates the symmetrical connected circuit's performance when a temperature sweep between -40° Celsius and 100° Celsius is performed with 10° Celsius steps. It is seen that the magnitude response of the circuit is stable but, likewise Monte Carlo simulation results, phase response of the circuit suffers at low frequencies. The presented simulation results hold true when input signal is applied V_1 or V_2 input port of the circuit.

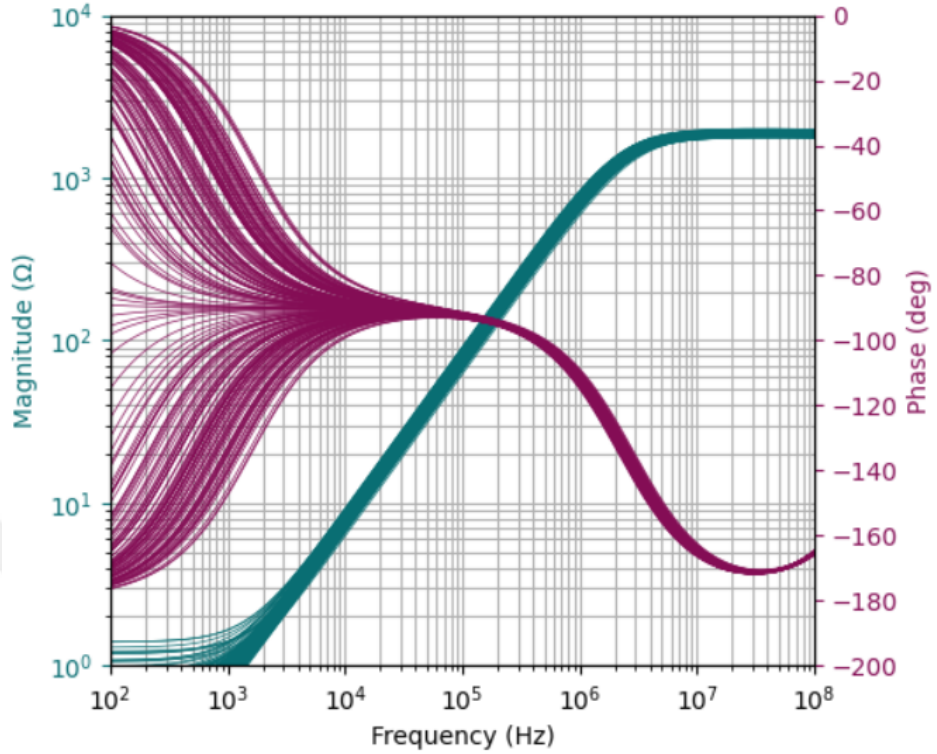


Figure 5.12. Monte Carlo analysis of the symmetric circuit.

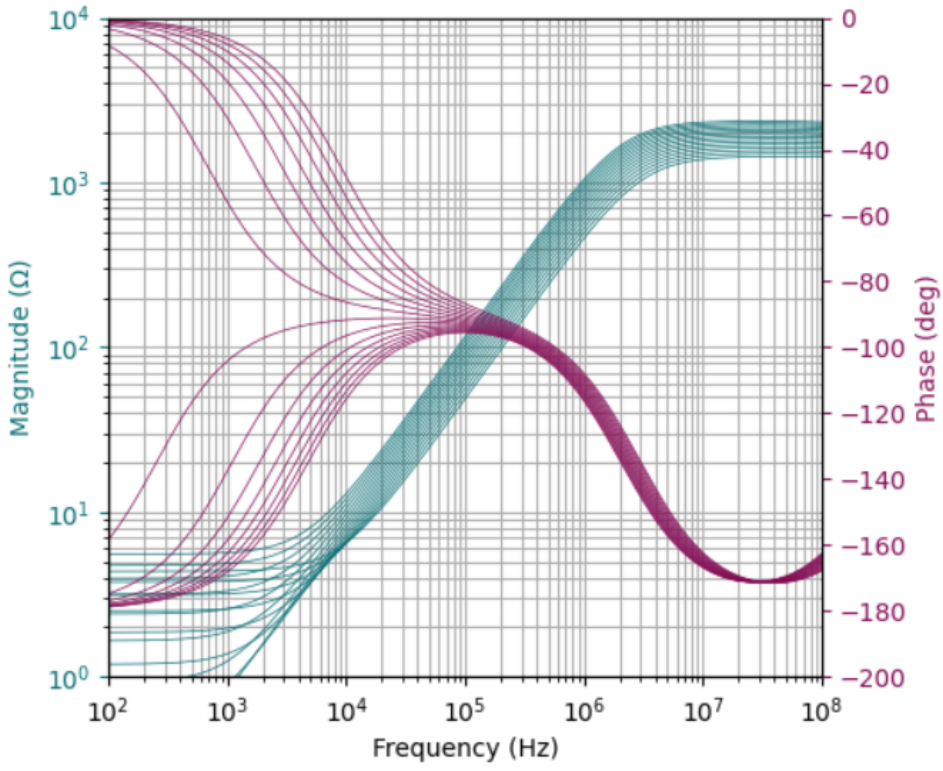


Figure 5.13. Temperature analysis of the symmetric circuit.

5.7. Utilization of the Negative Active Inductor Circuits

Stability is an important checkpoint and negative active inductor circuit can be unstable if not utilized properly with other circuit elements [40, 41]. In this section proper utilization of the symmetric connected negative active inductor is presented. It is seen that these types of circuits cannot be used directly in some complex circuits because of instability problem. As a simple application, positive inductance cancellation for the circuit is performed. For instance, in real life, generating perfect electrical wires is not a straightforward task. Therefore, most of the wires have parasitic elements such as inductors. These parasitic inductors are quite small in value but it is important to take them into account because in some applications they could have important impact on the output signal behavior and cause significant distortion. In this section such effect is observed and its cancellation is made with the presented symmetric connected circuit. The effectiveness of the circuit has tested with two different input waveforms, for sine and triangular wave input signals. First, for two different cases necessary circuits should be constructed. There are four circuits, which are needed for each of the test case. The first circuit is constructed with an AC source and a resistance. Fig. 5.14 presents this case. This case will be the ideal case because there is no inductance presented.

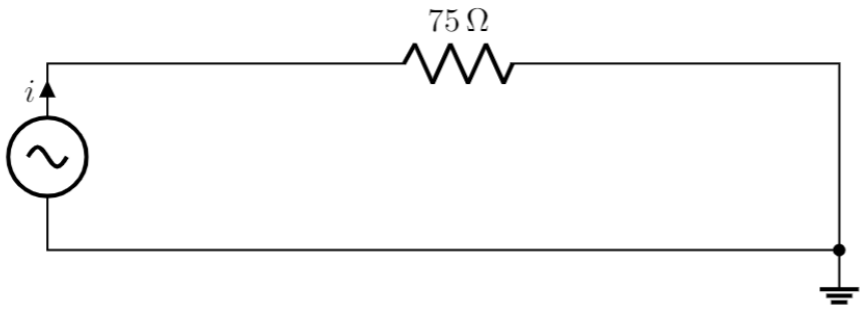


Figure 5.14. The construction of the first circuit.

The second circuit is constructed with an AC source, a resistance and a positive inductor and this case is shown in Fig. 5.15. This situation is set to observe the inductive effect that is brought by long cable. The resistor and inductor are connected in series as it is shown in the figure.

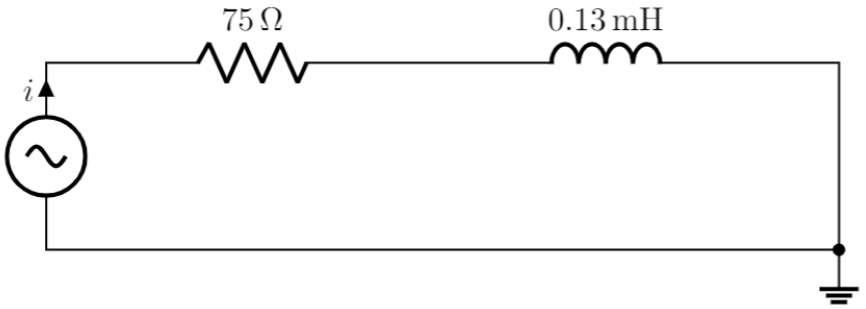


Figure 5.15. The construction of the second circuit.

The third and the fourth circuits are constructed with an AC source, a resistance, a positive inductance and the designed NAI circuit and is shown in Fig. 5.16. The reason why two of these circuits are constructed is to test whether reversing the connection ports of the NAI circuit causes any problem.

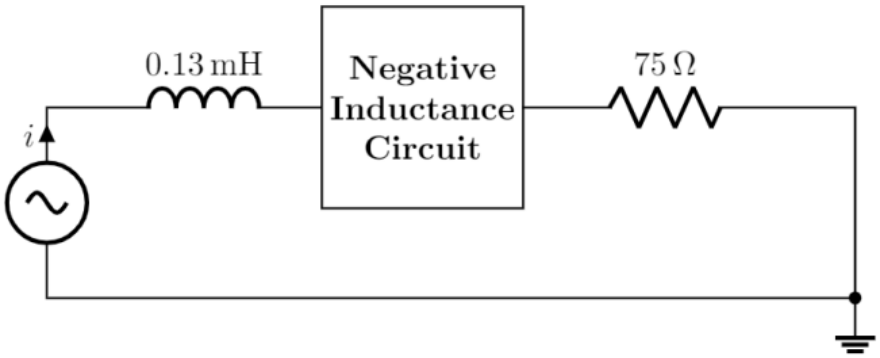


Figure 5.16. Constructed schematic of the third and fourth circuit.

The effect of the NAI will be observed on the circuit and it is expected that the effect of the positive inductance will be erased. As it is stated previously this cancellation is tested in two different cases. In the first case a current source that has peak-to-peak 200 μA current with triangular wave is applied to the circuit's input and in the second case a sinusoidal current source with similar peak-to-peak value is applied to the circuit's input. As the resistor 75 Ω is used in all of the circuits.

Fig. 5.17 shows the input node voltages on the first and second circuits (Fig. 5.14 and Fig. 5.15) when a current source with triangular waveform is applied. The effect of the inductor could be clearly observed in the circuit. "Ideal Voltage" shows

the input node voltage of Fig. 5.14 and "Nonideal Voltage" presents the input node voltage of Fig. 5.15.

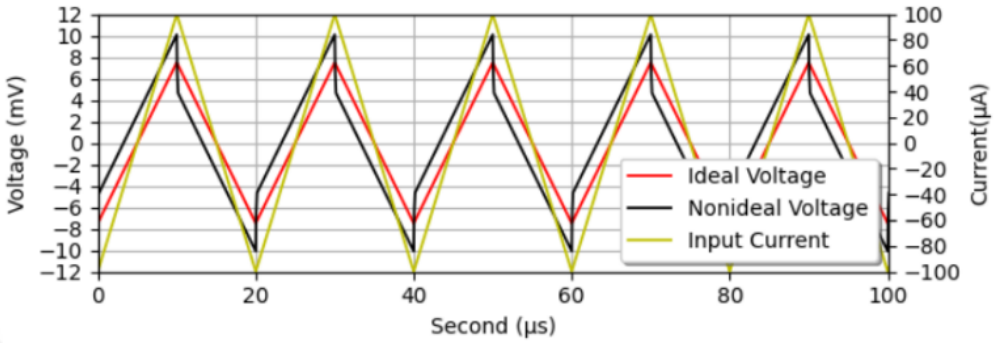


Figure 5.17. Input voltage results for the circuits in Fig. 5.14 and Fig. 5.15.

Fig. 5.18 shows the input voltages for Fig. 5.14 and Fig. 5.16. There, "Constructed Voltage" is the input voltage that is observed on the input node of Fig. 5.16. It is seen that the constructed NAI works well.

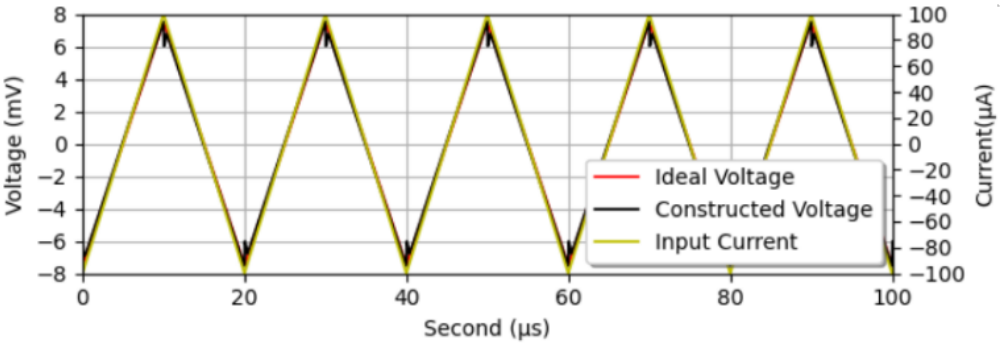


Figure 5.18. Input voltage results for the circuits in Fig. 5.14 and Fig. 5.16.

Same tests are made with a current source with sinusoidal waveform. Fig. 5.19 and Fig. 5.20 present the test results on the constructed circuits. The effect of the inductance could again be observed in Fig. 5.19, there is a clear phase shift in the inductive circuit. Finally, Fig. 5.20 shows the results for first and third circuits (also fourth). It is clear that, again, the NAI is able to cancel the effect of the positive inductor. There is also one important weakness of the circuit that should be noted. The circuit could not be driven with a pure voltage source, which means that when a pure AC voltage source is applied to the circuit's one of the inputs, the operating point

of one transistor moves to resistive region that alters the circuit operation. Therefore, as a simple solution, one could connect a resistance in series with input source when the circuit is driven with a AC voltage source.

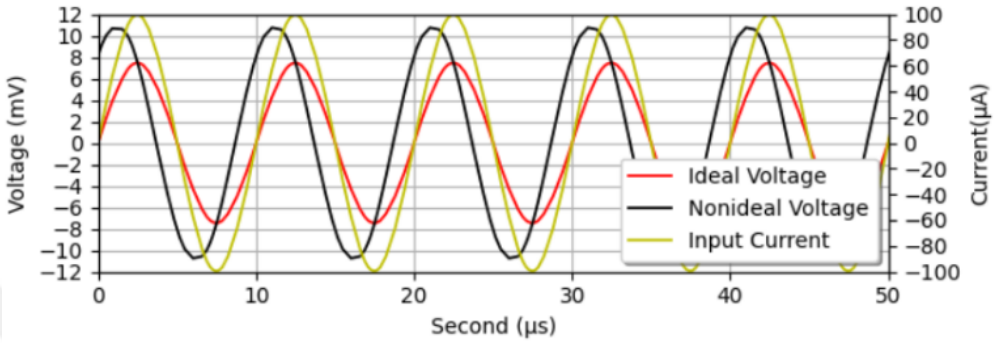


Figure 5.19. Input voltage results for the circuits in Fig. 5.14 and Fig. 5.15.

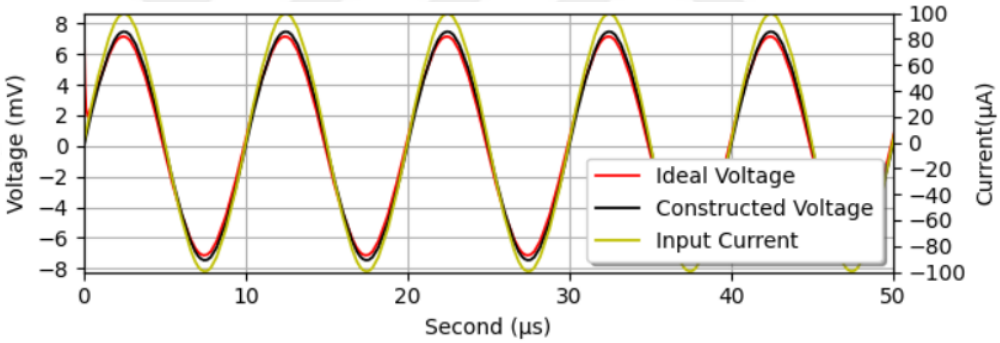


Figure 5.20. Input voltage results for the circuits in Fig. 5.14 and Fig. 5.16.

5.8. Conclusion

In this research work, two negative inductor circuits are presented. Both of the circuits are constructed by utilizing MOS-Only technique. The simulations of the circuits are carried out with 0.18 μm TSMC parameters and according to the results, it is seen that the circuits achieve a negative inductance value successfully. However, the proposed basic topology is not suitable for usage. Therefore, a symmetric connected version of the circuit is presented. The symmetric connection of the circuit presents important boosts to the performance. For instance, high offset voltage is eliminated and inductance value is doubled. In addition, by adding a small resistor, the matching

problem of the circuit is solved. The realized inductance value is in mH range and could be adjusted by changing circuit parameters. Finally, application instances for the circuit are performed. Power dissipation of the circuits are 561 μW and 1223 μW for the single-ended and symmetric connected circuits respectively.

6. PERFORMANCE COMPARISON

In the previous chapters six active inductor circuits, both positive and negative, are proposed. The circuits showed promising results and it was proven that the circuits could be utilized for replacements of ideal inductors in electrical circuits. However, in previous chapters no reference point or no detailed information about previous works were presented, which is noteworthy when it comes to see the strengths and the weaknesses of the presented circuits. In this chapter, performances of the presented circuits are compared to the AI circuits that were reported in the past. The comparisons are made for several qualities such as realized inductance, inductive bandwidth, quality factor, peak-to-peak realized input voltage, supply voltage and power consumption.

6.1. The Previous Works

Active inductors has been one of the hot topics for the couple of past decades in electronics and, as a result, there are plenty instances of active inductor works in the literature. In addition to the published articles, there is a book that is dedicated for this specific subject [2]. In order to compare the qualities of the circuits that are presented in this work, six different works are chosen from literature. While choosing works from past, the most recent works are prioritised. Four of the six chosen works are the instances of positive type realization and the other two are of negative type. The first four AI circuits are reviewed in [42, 43, 44, 45] and will be denoted as same, i.e., the circuit in [42] will named as [42], respectively in the following parts. The other two cicuits are reported in [46, 47] and will be denoted as [46] and [47] respectively. The chosen works differ as much as possible in their circuit qualities.

6.2. Comparison of the Positive Active Inductor Circuits

The circuits that are presented in this work will also be coded to simplify comprehension. Fig. 2.8 will be denoted as “circuit 1”, Fig. 3.1 as “circuit 2”, Fig. 4.2

and Fig. 4.10 as “circuit 3” and “circuit 4” respectively. Table 6.1 presents active inductor circuit aspects for the circuits that are chosen from literature. Likewise, Table 6.2 demonstrates qualities of the active inductor circuits that are introduced in this work. Together Table 6.1 and Table 6.2 indicate that proposed circuits realize much higher inductances than the previous works. Nevertheless, some of other circuit factors that are reported in the literature are better than what is obtained such as inductive bandwidth and quality factor. In general, it could be stated that the presented circuits are much more suitable for usage in cases, where big inductance value is prioritised with moderately high frequency.

Table 6.1. Qualities for the circuits that are chosen from literature.

Quality	**[42]**	**[43]**	**[44]**	**[45]**
Inductance (nH)	3.55-26	33	5-12	0-0.9
Ind. Bandwidth (GHz)	5.5	5.5	1.5	3
$Q_{\mathbf{max}}$	895	68	70	1852
Supply Voltage (V)	1	1.8	3.3	1.8
Power Con. (mW)	0.515	3.6	16	54-57.6
Process (CMOS) (μm)	RF 0.09	RF 0.18	0.18	0.13

Table 6.2. Qualities for the presented circuits.

Quality	**cir. 1**	**cir. 2**	**cir. 3**	**cir. 4**
Inductance (mH)	1.65	0.019	0.285	0.566
Ind. Bandwidth (MHz)	20	40.5	44	44
$Q_{\mathbf{max}}$	28.15	1.65	4.65	4.57
Supply Voltage (V)	3.3	1.8	3.3	3.3
Power Con. (mW)	0.38	1.242	0.47	0.923
Process (CMOS) (μm)	0.18	0.18	0.18	0.18

6.3. Comparison of the Negative Active Inductor Circuits

Similar to the namings in the above, negative type active inductor circuits are also enumerated. Fig. 5.2 will be renamed as "circuit 5" and Fig. 5.8 as "circuit 6". Table 6.3 presents qualities for the negative type active inductor circuits -both from the literature and from the presented work. It is seen that, in the literature, some of the negative type active inductors are realized with bipolar transistors. Because of their operation principle, BJTs inject current into their base terminal, which consequently increases power consumption and, therefore, causes them to be regarded as inferior to MOSFETs in the IC design. Another value of the AI circuits that are laid in the chapters is their realization with CMOS technology, which is a critical upper hand.

Table 6.3. Quality comparison for negative type of AI circuits.

Quality	**[46]**	**[47]**	**cir. 5**	**cir. 6**
Inductance (mH)	-85	-1.3	-0.41	-0.13
Q	-	-	5.4	18810
p.p. Vol. (mV)	20	10	2.4	34
Supply Voltage (V)	3	3	1.8	1.8
Power Con. (mW)	3.42	1.48	0.561	1.223
Process	ALA400	ALA400	CMOS 0.18 (μm)	CMOS 0.18 (μm)

6.4. Conclusion

This chapter discusses performances of the AI circuits that are presented in the previous chapters. As a reference point, diverse papers are chosen from the literature for both type of active inductors. For positive type of AI circuits, it is seen that proposed circuits realize high inductance value but come short of inductive bandwidth and maximum quality factor. In the case of negative type of circuits, proposed circuits are possibly good fit when compared to the works that are introduced in the literature.

7. CONCLUSION

Active inductor circuits are strong candidates in order to fill the gap in the absence of passive inductors in many on-chip applications. By utilizing resemblence of the MOSFET's small signal model to VCCS, in saturation region, in total, six positive and negative active inductor circuits are presented in this work.

In Chapter 2, a four transistor active inductor circuit is presented. It is seen that the circuit results in a very high input offset voltage. This offset voltage does not allow circuit to work properly when employed in a practical application. In order to compensate this offset voltage, a diode is placed in one of the input ports. It is seen that placing a diode dramatically reduces offset voltage and this compansation allows the active inductor circuit work properly in a practical application. Lastly, a 3^{rd} order Elliptic LPF is constructed in order to investigate functionality of the circuit and it is seen that the circuit works well as an inductor replacement.

Differential circuits offer bountiful advantages over their single-ended counterparts. Starting from this point, in Chapter 3, a test was made in order to see the effect of symmetrical connection of the circuit that was presented in the previous chapter by mirroring it. It is noticed that symmetric connection could totally remove the offset voltage problem. In addition, it is observed that the terminal voltage swing is doubled with symmetric connection. Also, when the symmetric connection was tested, all of the transistor types were changed from NMOS to PMOS (whereas in the previous chapter all transistors were N-type), along with other circuit parameters. Additionally, rather than using ideal current sources, real current sources are implemented in order to supply circuit. As a result, it is seen that the circuit meets the expectations and could be used in many applications.

Keeping the benefits of the symmetric connection in mind, a new seven transistor active inductor circuit is introduced in Chapter 4. The prenseted circuit has a high

input voltage swing possibility with low offset voltage at the input. Such qualities make the presented circuit appealing. Furthermore, symmetric connected version of the circuit is also presented and its advantages are discussed. It is observed that the offset voltage is removed and inductance value of the circuit is doubled, as it was the case in the previous chapter. In order to compare the effectiveness of the single-ended and symmetric connected circuits, 5^{th} order Butterworth LP filters are constructed. It is experienced that both of the circuits have similar performance when they are utilized in an application.

Chapter 5 discusses two new negative active inductor circuits. The primary difference between positive and negative inductors stems from their phase response. In this chapter, first, a three transistor NAI circuit is presented. It is seen that presented circuit does not work as expected. Hence, in order to improve its performance, symmetric connected version of the recommended circuit is formed. It is observed that the performance of the circuit is boosted. With symmetric connection of the circuit, input voltage swing capability is increased more than tenfold. Lastly, the circuit's usability is tested and it is seen that the circuit could cancel parasitic positive inductances.

Finally, a quality comparison of the presented works are made in Chapter 6 by referencing past works. Comparison results indicate that no circuit demonstrates supreme performance. Each circuit has its own strengths and weaknesses in certain aspects.

As a summary, in this work various positive and negative inductor circuits are presented. Active inductor circuits that are proposed rely on MOSFET utilization and their resemblance to VCCS in saturation region. In this way the input impedance functions of the circuits are calculated and the artificial inductors are obtained. The ideas that are presented in this work could be a good reference for the ones who would like to inform themselves about active inductor circuits.

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APPENDIX A: TSMC 180 μm TRANSISTOR PARAMETERS

*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Jul 29/05
* LOT: T55U WAF: 3003
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+VERSION = 3.1    TNOM = 27    TOX = 4.1E-9
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+K1 = 0.5847845    K2 = 1.987508E-3    K3 = 1E-3
+K3B = 3.846051    W0 = 1.00001E-7    NLX = 1.66359E-7
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+U0 = 276.4769418    UA = -1.287181E-9    UB = 2.249816E-18
+UC = 5.695845E-11    VSAT = 1.050018E5    A0 = 1.8727159
+AGS = 0.4223855    B0 = -8.460618E-9    B1 = -1E-7
+KETA = -6.583564E-3    A1 = 0    A2 = 0.8925017
+RDSW = 105    PRWG = 0.5    PRWB = -0.2
+WR = 1    WINT = 0    LINT = 1.509138E-8
+XL = 0    XW = -1E-8    DWG = -3.993667E-9
+DWB = 1.211844E-8    VOFF = -0.0926198    NFACTOR = 2.4037852
+CIT = 0    CDSC = 2.4E-4    CDSCD = 0
+CDSCB = 0    ETA0 = 2.64529E-3    ETAB = -1.113687E-5
+DSUB = 0.0107822    PCLM = 0.7114924    PDIBLC1 = 0.1861265
+PDIBLC2 = 2.341517E-3    PDIBLCB = -0.1    DROUT = 0.708139
+PSCBE1 = 8E10    PSCBE2 = 9.186022E-10    PVAG = 5.128699E-3
+DELTA = 0.01    RSH = 6.5    MOBMOD = 1
+PRT = 0    UTE = -1.5    KT1 = -0.11
```

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 7.9E-10 CGSO = 7.9E-10 CGBO = 1E-12

+CJ = 9.604799E-4 PB = 0.8 MJ = 0.3814692

+CJSW = 2.48995E-10 PBSW = 0.8157576 MJSW = 0.1055989

+CJSWG = 3.3E-10 PBSWG = 0.8157576 MJSWG = 0.1055989

+CF = 0 PVTH0 = -4.358982E-4 PRDSW = -5

+PK2 = 2.550846E-4 WKETA = 1.466293E-3 LKETA = -7.702306E-3

+PU0 = 23.8250665 PUA = 1.058432E-10 PUB = 0

+PVSAT = 1.294978E3 PETA0 = 1.003158E-4 PKETA = -3.857329E-3)

*

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+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3955237

+K1 = 0.5694604 K2 = 0.0291529 K3 = 0.0997496

+K3B = 13.9442535 W0 = 1.003165E-6 NLX = 9.979192E-8

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+DVT0 = 0.5457988 DVT1 = 0.2640392 DVT2 = 0.1

+U0 = 118.0169799 UA = 1.591918E-9 UB = 1.129514E-21

+UC = -1E-10 VSAT = 1.545232E5 A0 = 1.6956519

+AGS = 0.3816925 B0 = 4.590751E-7 B1 = 1.607941E-6

+KETA = 0.0142165 A1 = 0.4254052 A2 = 0.3391698

+RDSW = 168.2822665 PRWG = 0.5 PRWB = -0.5

+WR = 1 WINT = 0 LINT = 3.011839E-8

+XL = 0 XW = -1E-8 DWG = -4.05222E-8

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+PDIBLC2 = 0.022477 PDIBLCB = -1E-3 DROUT = 1.228009E-3

+PSCBE1 = 1.245755E10 PSCBE2 = 3.598031E-9 PVAG = 15.0414628

+DELTA = 0.01 RSH = 7.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 6.34E-10 CGSO = 6.34E-10 CGBO = 1E-12

+CJ = 1.177729E-3 PB = 0.8467926 MJ = 0.4063096

+CJSW = 2.417696E-10 PBSW = 0.851762 MJSW = 0.3387253

+CJSWG = 4.22E-10 PBSWG = 0.851762 MJSWG = 0.3387253

+CF = 0 PVTH0 = 1.406461E-3 PRDSW = 11.5261879

+PK2 = 1.718699E-3 WKETA = 0.0353107 LKETA = -1.277611E-3

+PU0 = -1.4642384 PUA = -6.79895E-11 PUB = 1E-21

+PVSAT = 50 PETA0 = 1.003152E-4 PKETA = -3.103298E-3)

APPENDIX B: EFFECT OF THE PARASITIC ELEMENTS ON THE CIRCUIT'S BEHAVIOR FOR CHAPTER 2

It is important to understand how impactful is each parasitic component of the circuit so that one could try to design the circuit according to the wish. In this part, the most impactful components at low and high frequencies are searched for the circuit that is presented in Chapter 2. Firstly, it is obersed that at low frequencies g_{ds1} has very strong impact on the circuit's magnitude response. Figure B.1 shows that how the circuit's magnitude response alters at low frequencies when g_{ds1} became zero.

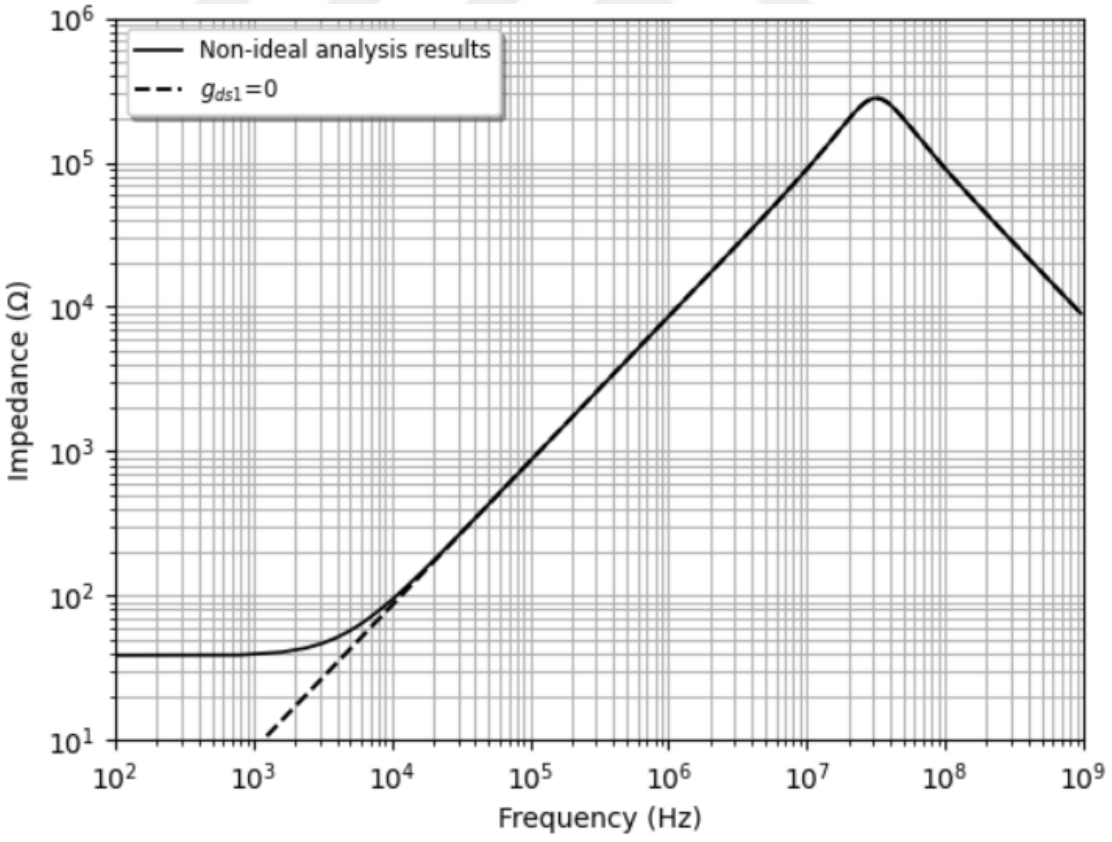


Figure B.1. Non-ideal analysis results when g_{ds1} is nulled.

Similar analysis is made for high frequencies and it is seen that at high frequencies three components play strong role shaping the circuit's magnitude response at high frequencies. These parasitic components are g_{ds3}, C_{gs1} and C_{gd1} and when they are nulled, the capacitive behavior of the circuit is suppressed at high frequencies. It is seen from Fig. B.2 that when these components are nulled the circuit's magnitude response continues to increase linearly.

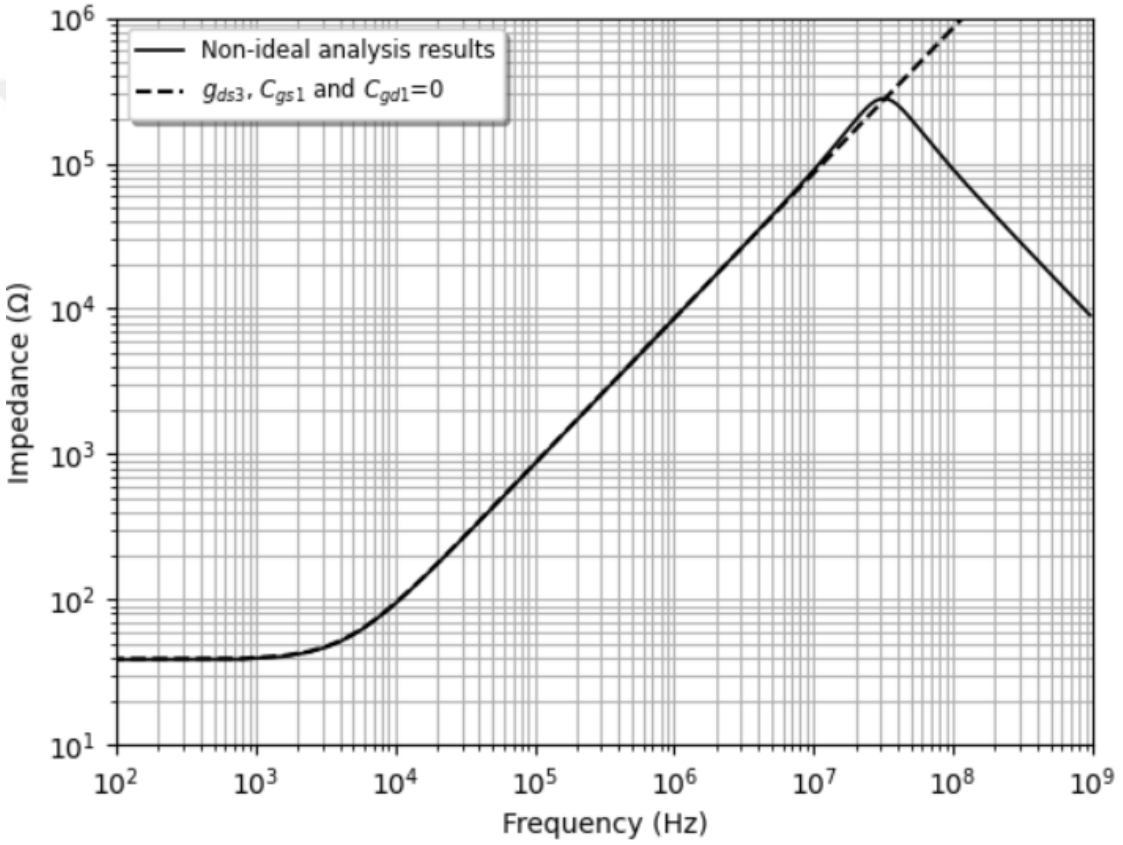


Figure B.2. The result of g_{ds3}, C_{gs1} and C_{gd1} nulling in non-ideal analysis.

Lastly, g_{ds1}, g_{ds3}, C_{gs1} and C_{gd1} are zeroed at the same time in order to observe changes on the non-ideal analysis. Fig. B.3 shows results of the analysis. It is seen that nulling these four parasitics result in the ideal ideal inductor behavior (magnitude response wise). Therefore, focusing on these four components will make much more sense for changing the behavior of the circuit at extreme frequencies.

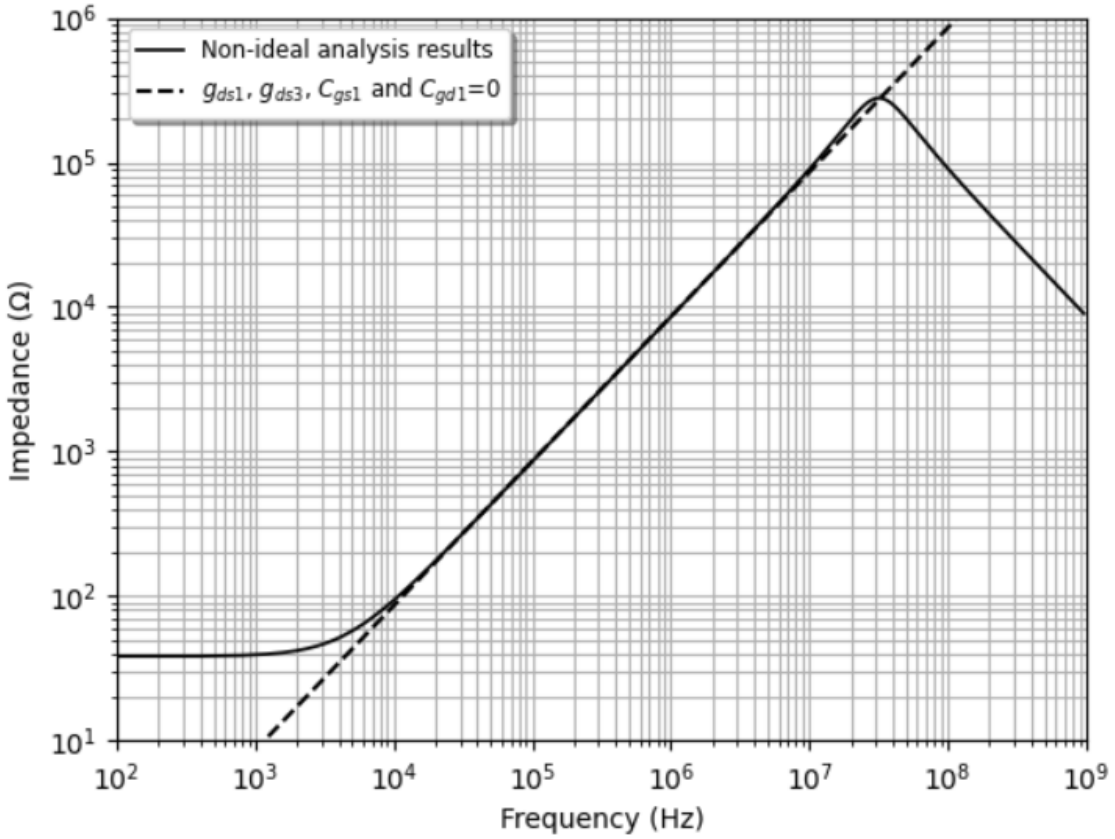


Figure B.3. The impact of g_{ds1}, g_{ds3}, C_{gs1} and C_{gd1} in non-ideal analysis.

APPENDIX C: EFFECT OF THE PARASITIC ELEMENTS ON THE CIRCUIT'S BEHAVIOR FOR CHAPTER 4

In this section, the most impactful parasitic components are observed at extreme frequencies for the circuit that is presented in Chapter 4. First, low frequencies are analized and it is seen that nulling g_{ds3} and g_{ds4} removes resistive behavior of the proposed circuit and it could be seen from Fig. C.1. Therefore, when one does not want to see resistive behavior at low frequencies, one could try to minimize the values of g_{ds3} and g_{ds4}.

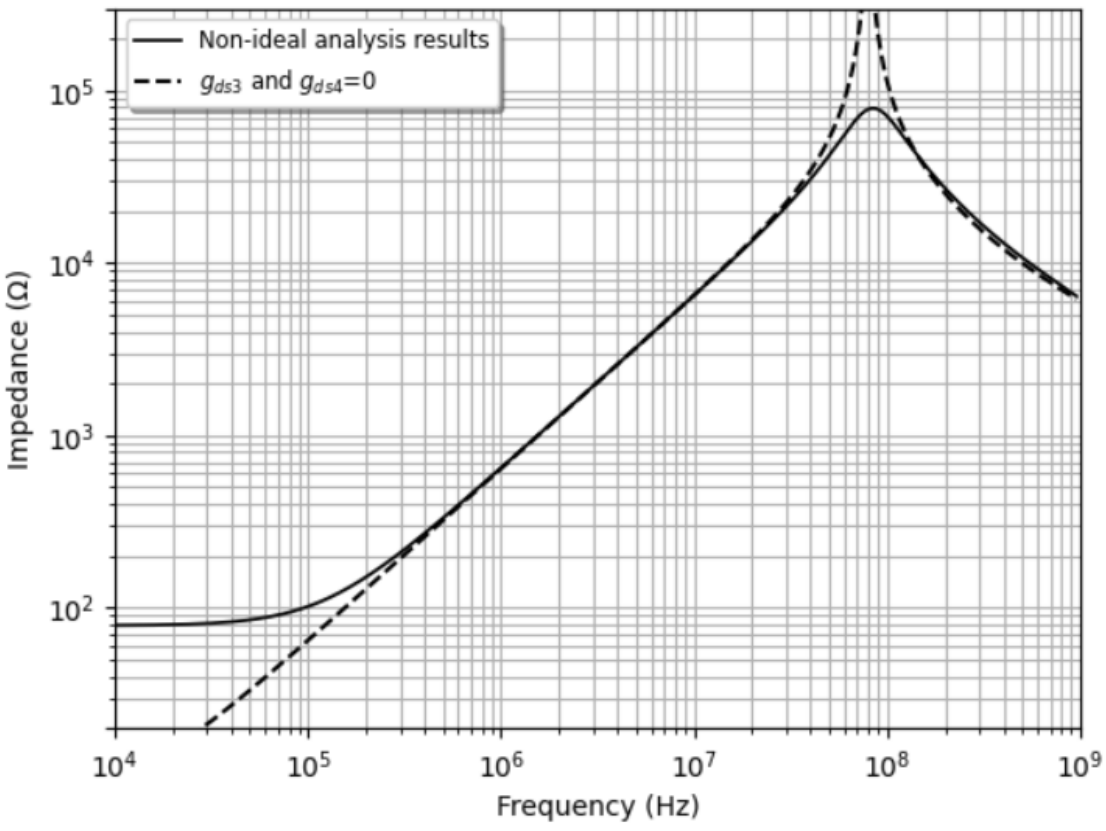


Figure C.1. Non-ideal analysis results when g_{ds3} and g_{ds4} are zeroed.

Next, high frequencies are examined. It is experienced that in order to remove capacitive behavior at high frequencies, one should try to minimize the values of three different parasitic compenents which are g_{ds3}, C_{gs2} and C_{gd2}. Fig. C.2 indicates that when these components are nulled, capacitive behavior of the frequency is severely diminished.

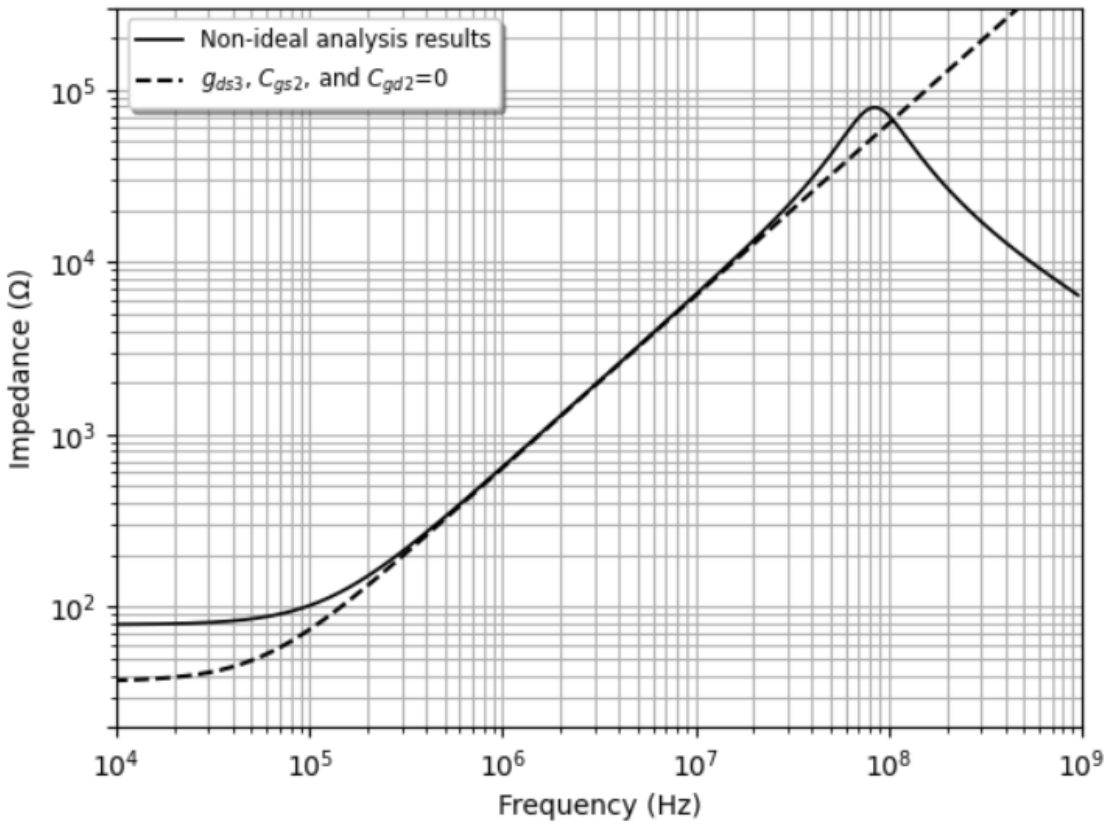


Figure C.2. Results of non-ideal analysis when g_{ds3}, C_{gs2} and C_{gd2} are nulled.

As of the last step, g_{ds3}, g_{ds4}, C_{gs2} and C_{gd2} are all zeroed simultaneously. Figure C.3 shares results of the removal. It is obvious that only nulling these components at the same time will result in the ideal inductor behavior. Hence, playing with these parameters in order to alter behavior of the circuit is the key.

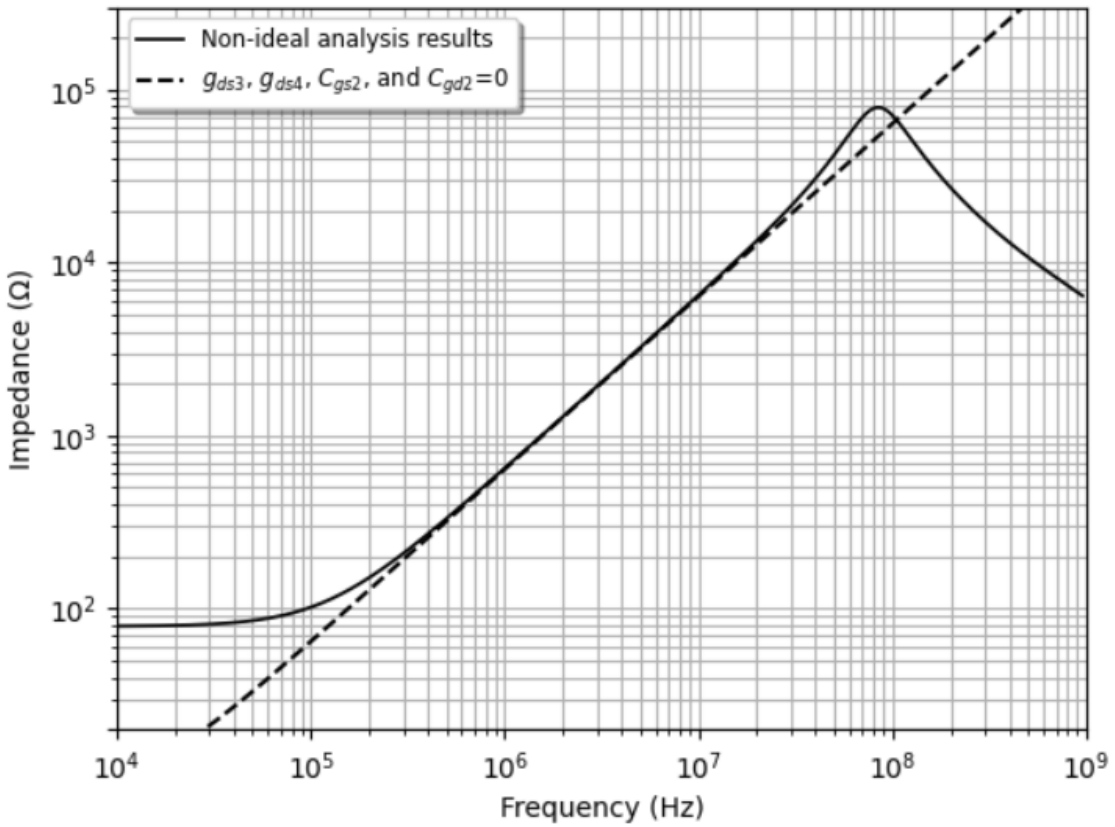


Figure C.3. Results of non-ideal analysis when g_{ds3}, g_{ds4}, C_{gs2} and C_{gd2} are nulled.

APPENDIX D: EFFECT OF THE PARASITIC ELEMENTS ON THE CIRCUIT'S BEHAVIOR FOR CHAPTER 5

In this section similar parasitic analyses to APPENDIX B and APPENDIX C are carried out in order to see which parasitic component is dominant at extreme frequencies for the circuit that is presented in Chapter 5. As a starting point, low frequencies are examined. It is seen that at low frequencies g_{ds1} is mainly responsible for the resistive behavior and when g_{ds1} is nulled, resistive behavior of the circuit is removed. Fig. D.1 presents how non-ideal results would change when this parasitic is removed.

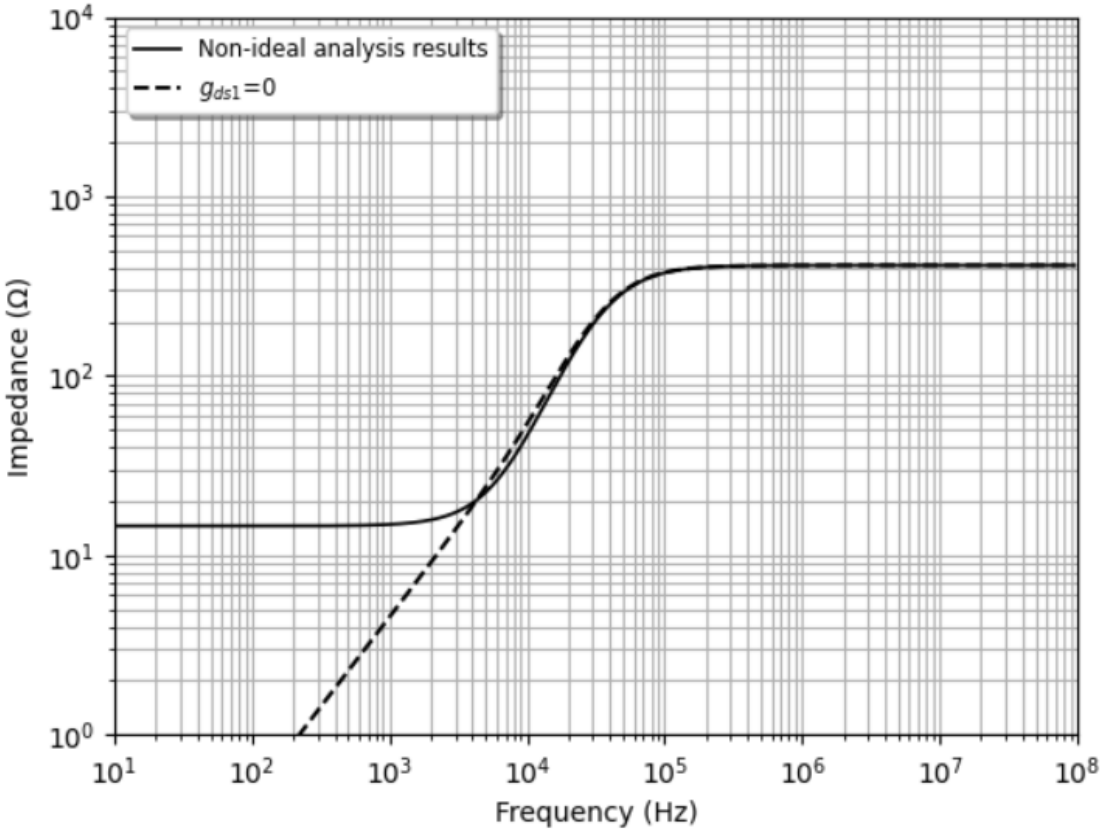


Figure D.1. The impact of g_{ds1} nulling in non-ideal analysis.

As a next step, high frequencies are observed. It is seen that at high frequencies two parasitic components C_{gd1} and C_{gd3} are mainly responsible for the curving of the magnitude response of the input impedance. Fig. D.2 shows the effect of C_{gd1} and C_{gd3} removal. It is seen that when these components are nulled, bending of the curve is shifted towards higher frequencies.

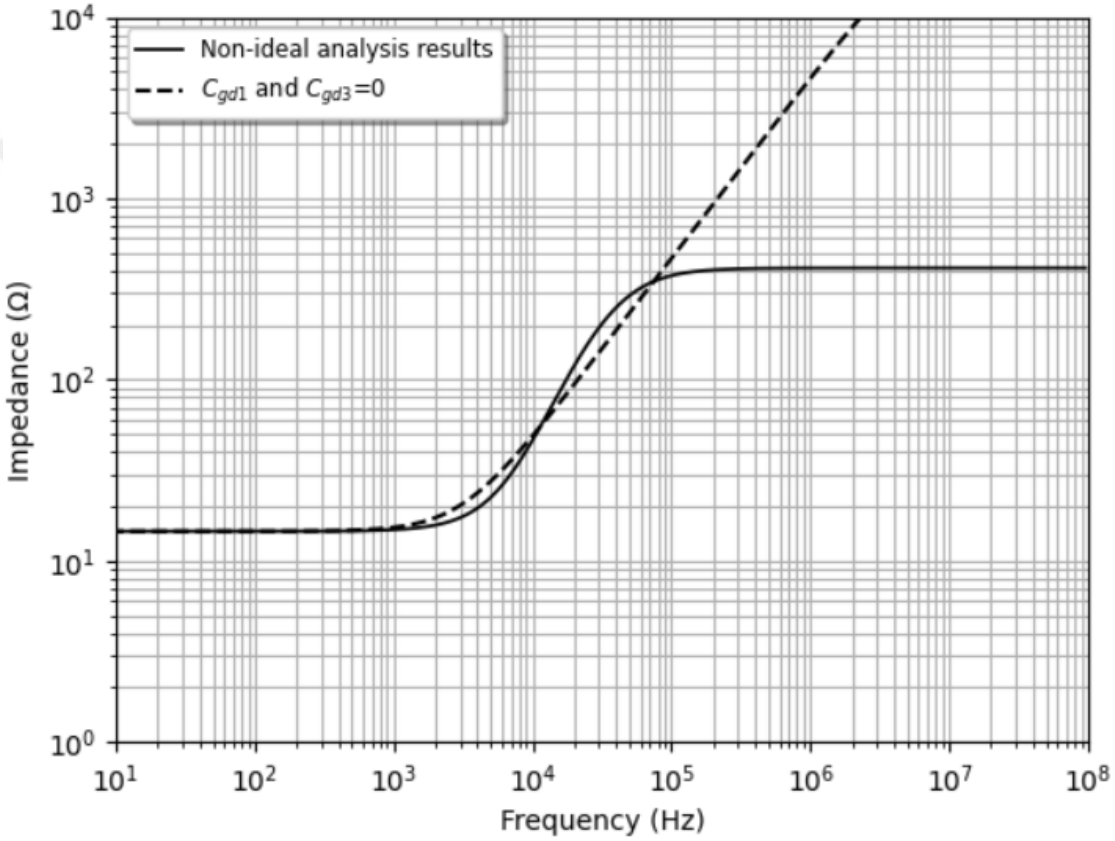


Figure D.2. The result of C_{gd1} and C_{gd3} nulling in non-ideal analysis.

Finally, as the last case, the result of g_{ds1}, C_{gd1} and C_{gd3} removal is observed. Fig. D.3 presents results of the process. It is experienced that these three components play major role when it comes to shape magnitude response of the input impedance. To achieve desired aspects, one should select values of the components according to the desire. For instance, if resistive behavior is not desired at low frequencies, g_{ds1} could be minimized or if band curving of the magnitude response is not desired at high frequencies, C_{gd1} and C_{gd3} could be selected as small as possible.

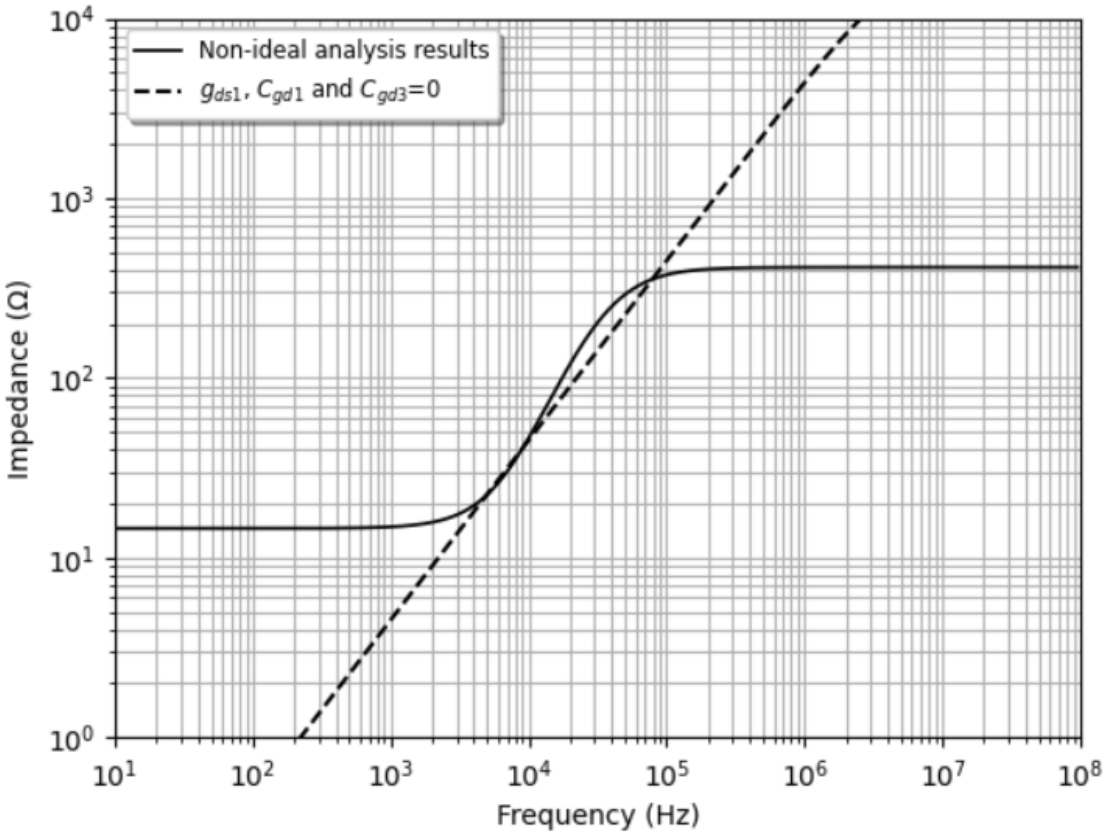


Figure D.3. Non-ideal analysis results when g_{ds1}, C_{gd1} and C_{gd3} are nulled.