ANALOG CIRCUIT DESIGN AUTOMATION AGAINST PROCESS VARIATIONS AND AGING PHENOMENA

by

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ABSTRACT

ANALOG CIRCUIT DESIGN AUTOMATION AGAINST PROCESS VARIATIONS AND AGING PHENOMENA

Reliability of CMOS circuits has become a major concern due to substantially worsening process variations and aging phenomena in deep sub-micron devices. As a result, conventional analog circuit sizing tools have become incapable of promising a certain yield whether it is immediately after production or after a certain period of time. Thereby, analog circuit sizing tools have been replaced by better ones, where reliability is included in the conventional optimization problem. Variation-aware analog circuit synthesis has been studied for many years, and numerous methodologies have been proposed in the literature. On the other hand, as far as we know, there has not been any tool that takes lifetime into account during the optimization. Besides, there are a number of different issues with lifetime-aware circuit optimization, where aging analysis is still quite problematic due to modeling and simulation deficiencies. Furthermore, both tools suffer from the challenging trade-off between efficiency and accuracy. Reconfigurable analog circuit design is another way of designing analog circuits against aging. However, design of a such complicated system is highly time consuming process to be performed by hand. Even though reconfigurable circuit design has been studied in the literature, there has been no attempt to automatize the design process to reduce the design time. With regard to aforementioned these problems, this study addresses all of these problems under a general title of reliability-aware analog circuit design automation, severally discusses them in detail, and proposes novel solutions to deal with not only existing but also not addressed problems.

ÖZET

YAŞLANMA VE PARAMETRE SAÇILIMINA KARŞI ANALOG TÜMDEVRE TASARIM OTOMASYONU

Mikron-altı teknolojilerinde önemli artış gösteren parametre saçılımı ve yaşlanma olayları nedeniyle CMOS devrelerin güvenilirliği başlıca bir tartışma konusu haline gelmiştir. Sonuç olarak, geleneksel analog devre sentezleyiciler gerek hemen üretim sonrası gerekse belli bir çalışma zamanı sonrası belirli bir verim vaad edemez hale geldiler. Dolayısıyla, analog devre sentezleyiciler güvenilirliliği de hesaba katan daha yetkin araçlarla değiştirildi. Parametre saçılımına karşı analog devre tasarım otomasyonu konusu yıllardır çalışılmakta olup, literatürde çeşitli yöntemler önerilmiştir. Diğer taraftan, bildiğimiz kadarıyla, devrelerin yaşam süresini eniyileme sırasında hesaba katan herhangi bir araç bulunmamaktadır. Bununla birlikte, yaşlanma modellemesi ve benzetimleri eksikliklerinin yol açtığı yaşlanma analizi problemleri nedeniyle yaşam süresi duyarlı devre eniyilemesi çeşitli sorunlara sahiptir. Dahası, her iki araç da etkinlik ve doğruluk arasındaki zorlu ödünleşimden mustariptir. Yeniden yapılandırabilir devre tasarımı yaşlanmaya karşı analog devre tasarım yollarından bir diğeridir. Fakat, böyle karmaşık bir sistemin el yordamıyla tasarlanması oldukça zaman alıcıdır. Her ne kadar yeniden yapılandırabilir devreler yıllardır çalışılan bir konu olsa da, literatürde tasarım sürecini otomatize edecek herhangi bir girişim mevcut değildir. Bahsedilen bu problemler göz önüne alınarak, bu çalışma bu problemlerin hepsine güvenilirlik duyarlı analog devre tasarım başlığı altında değinmekte, konuların hepsini ayrı ayrı tartışmakta ve yalnızca varolan değil daha önce hiç değinilmemiş problemler için yeni çözümler sunmaktadır.

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LIST OF SYMBOLS

$E_{\perp}$	Vertical Electric Field
$E_{\parallel}$	Parallel Electric Field
E_{ox}	Oxide Electric Field
g_{m}	Transconductance of a MOSFET
I_{d}	Drain current of MOSFET
I_{g}	Gate current of MOSFET
I_{sub}	Substrate current of MOSFET
I_{submax}	Maximum substarte current of MOSFET
J_{avg}	Average Current Density
J_{peak}	Peak Value of Current Density
J_{rms}	RMS value of Current Density
q_{bd}	Charge Breakdown
R_{g}	Post Breakdown Resistance
$T_{\mathrm{B}}(E_{\mathrm{ox}})$	Tunnel probability of hot electrons
V_{d}	Drain voltage of MOSFET
V_{ds}	Drain to source voltage of MOSFET
V_{dsat}	Drain voltage of MOSFET at saturation
V_{g}	Gate voltage of MOSFET
V_{gs}	Gate to source voltage of MOSFET
V_{th}	Threshold voltage of MOSFET
$\Delta \mathrm{N}_{\mathrm{it}}$	Interface Trap Density
φ_s	Surface potential
ϕ_{b}	Energy barrier
ϕ_{it}	Critical energy for device damage
γ	Noise factor of a FET
μ_0	Mobility of MOSFET

LIST OF ACRONYMS/ABBREVIATIONS

AAT	Accelerated Aging Test
CHC	Channel Hot Carrier
CHE	Channel Hot Electron
CAD	Computer Aided Design
CDCCO	CMOS Differential Cross Coupled Oscillator
CMOS	Complementary Metal Oxide Semiconductor
DAHC	Drain Avalanche Hot Carrier
EDA	Electronic Design Automation
EM	Electro Migration
FN	Fowler-Nordheim
HBD	Hard Breakdown
GIDL	Gate Induced Drain Leakage
HCI	Hot Carrier Injection
ISE	Infeasible Solution Elimination
KL	Kullback Leibler
LDS	Low Discrepancy Sequence
LEM	Lucky Electron Model
LHS	Latin Hypercube Sampling
MC	Monte Carlo
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTTF	Mean Time To Failure
MVE	Multiple Vibrational Excitation
NDCCO	NMOS Differential Cross Coupled Oscillator
NBTI	Negative Bias Temperature Instability
OTA	Operational Transconductance Amplifier
PBTI	Positive Bias Temperature Instability
PTM	Predictive Technology Modeling
QMC	Quasi Monte Carlo

SBD	Soft Breakdown
SEM	Scanning Electron Microscope
SGHE	Secondary generated hot electron
SHE	Substrate Hot Electron
SHH	Substrate Hot Hole
SILC	Stress Induced Leakage Current
SoC	System on Chip
TDDB	Time Dependent Dielectric Breakdown
VCO	Voltage Controlled Oscillator

1. INTRODUCTION

Before the development of electronic design automation (EDA) tools, integrated circuits (IC) were designed by hand, and manually laid out. Then, the design process was automated through drafting and the first placement and routing were developed by the end of 70s. The most important breaking point in EDA starts with the concept of VLSI systems at the beginning of the 80s, where computer aided design (CAD) was enhanced remarkably with the programming languages. As a result of the improved access to design and simulation tools, the design time has exponentially decreased while the complexity of IC has also exponentially increased. Over the years, CAD tools have become inevitable for design, simulation, analysis, verification, and manufacturing preparation processes. Afterwards, to minimize the requirement of human effort and to reduce the time to market, design automation tools have been developed and have achieved considerably higher revenues. EDA revenue history from 1996 to the present and the percentage by categories for the fourth quarter of 2015 are provided in Figure 1.1, where computer aided engineering (CAE), IC synthesis, and semiconductor intellectual property (SIP) have a portion of almost 90% of the EDA revenue. Furthermore, revenues in CAE, SIP, and IC synthesis have been rapidly increasing in the last five years, which clearly indicates the increasing demand for EDA.

Design automation/IC synthesis refers to automatic design of circuits without human effort by solving physical/electrical level circuit design problems by utilizing computers and intelligent algorithms. Thanks to the increased computational capacity of computers, EDA systems have become very popular over the last two decades. Recently, mixed-signal designs have started to occupy a large fraction of integrated circuits. The design of the digital section of the IC has been fully automated with powerful digital circuit synthesis tools, which are based on minimizing chip area and power consumption while increasing speed and satisfying timing constraints. However, mixed signal ICs also require an interface part in order to communicate with the continuous-valued world, where analog circuits meet this requirement in mixed-signal ICs [1].

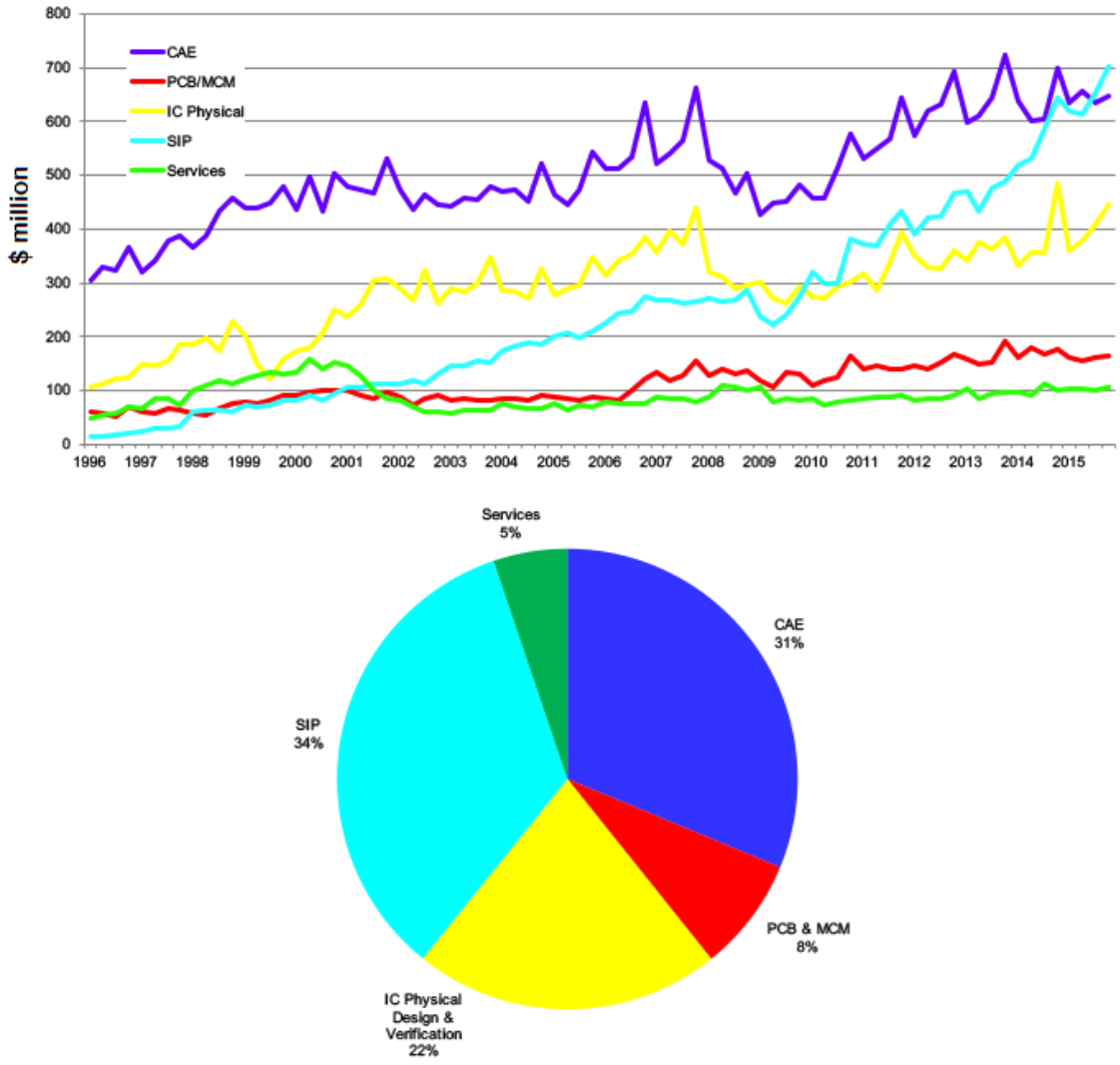

Figure 1.1. Electronic Design Automation revenue history and reveune percentage by catogories for the last quarter of 2015 [1].

The case of analog synthesis is quite problematic compared to digital synthesis due to nonlinearity and the requirement of comprehensive analyses for the complicated trade-offs among various aspects of performances. Analog circuit synthesis refers to automatic sizing of transistors in order to achieve the targeted performances. Several analog circuit synthesis tools have been proposed in the literature. The earlier approaches required a designer expertise during synthesis, but this requirement has been reduced thanks to very high speed computers and advanced simulator tools.

Consequently, the whole design loop from circuit sizing to layout preparation has been fully automated at the circuit level. A comprehensive discussion for such tools is presented in Figure 2.1. A SPICE-based analog circuit synthesis tool is utilized as optimization engine for all reliability-aware synthesis tools in this thesis. In addition to that, a mixed domain RF circuit synthesis tool is also proposed, where layout induced parasitics are considered during the sizing process. Thus, the discrepancy between schematic level and layout level is mitigated, which also reduces the layout iterations.

Beside many advantages of rapidly developing technology, reliability of ICs has worsened due to increasing variability and aging problems. Variability problems occur as a result of scaling differences between transistor dimensions and process tolerances in sub-micron technologies. Therefore, variations in different fabrication steps, such as line-edge roughness (LER) that is induced by gate etching and the lithography process, oxide thickness fluctuations (OTF) that cause the fluctuation of the voltage drop across the oxide layer, and random dopant fluctuations (RDF) are drastically increased [2, 3]. Hence, if a circuit is designed to achieve a specific set of nominal performance values, a discrepancy occurs between the expected and the actual performances in a population of manufactured ICs. Thus, some circuits violate the design constraints after fabrication as depicted in Figure 1.2.

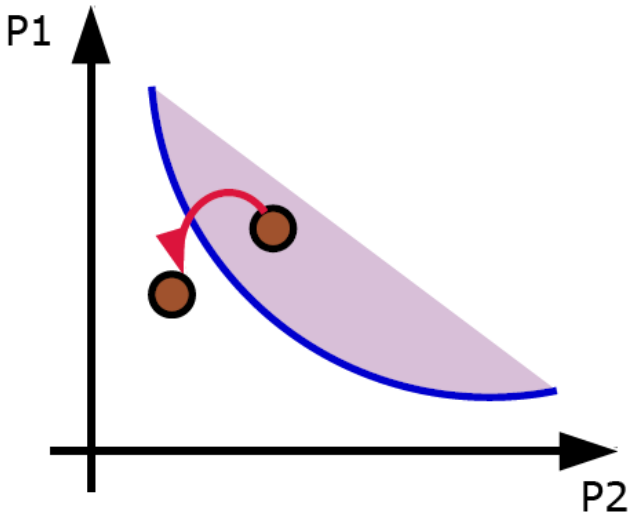

Figure 1.2. Variation causes performance space violation.

On the other hand, scaling factor of transistor dimensions is larger than the scaling of supply voltage, which results in an increase in local electric fields on deep sub-micron devices. This scaling difference between transistor dimensions and supply voltages aggravates a time-dependent problem called aging. According to ITRS roadmap provided in Table 1.1, the effective channel length reduces from 49 nm to 9 nm between 130 nm and 22 nm technologies; however, corresponding supply voltages are 1.2 V and 0.8 V, respectively. Meanwhile, the effective oxide thickness reduces from 1.2 nm to 0.8 nm.

Table 1.1. Technology specifications from 130 nm to 22 nm.

Technology Node (nm)	130	90	65	45	32	22
Effective Channel Length (nm)	49	37	25	18	13	9
Effective Oxide Thickness (nm)	1.5	1.2	0.9	0.7	0.6	0.5
Supply Voltage (V)	1.2	1.2	1.1	1.0	0.9	0.8

Considering the electric field formula given in Equation 1.1, vertical and horizontal electric fields over the channel become considerably larger for advanced technology nodes.

$$E = -\frac{\Delta\phi}{d} \tag{1.1}$$

Here $\Delta\phi$ denotes the potential difference between two nodes, which corresponds to V_{ds} for horizontal electric field and V_{gs} for vertical field, respectively. Consequently, aging phenomena have become more severe for advanced technology nodes and cause a time-dependent performance degradation as shown in Figure 1.3.

Conventionally, the bathtub curve given in Figure 1.4 is used to examine the lifetime of a product in many areas [4], which is also applicable for the lifetime of ICs. As seen from the figure, there are three distinct phases in the lifetime of an IC.

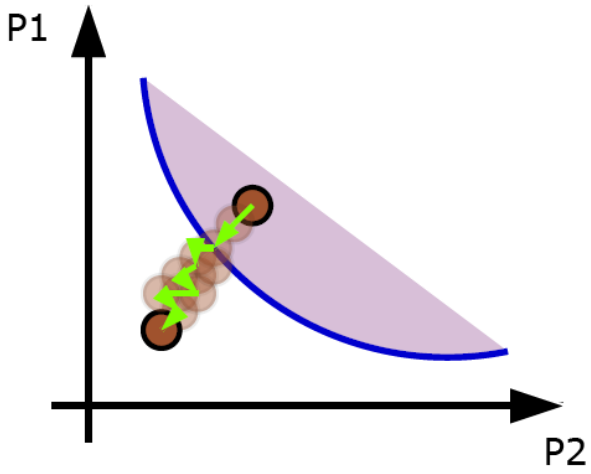

Figure 1.3. Aging causes a time-dependent performance degradation.

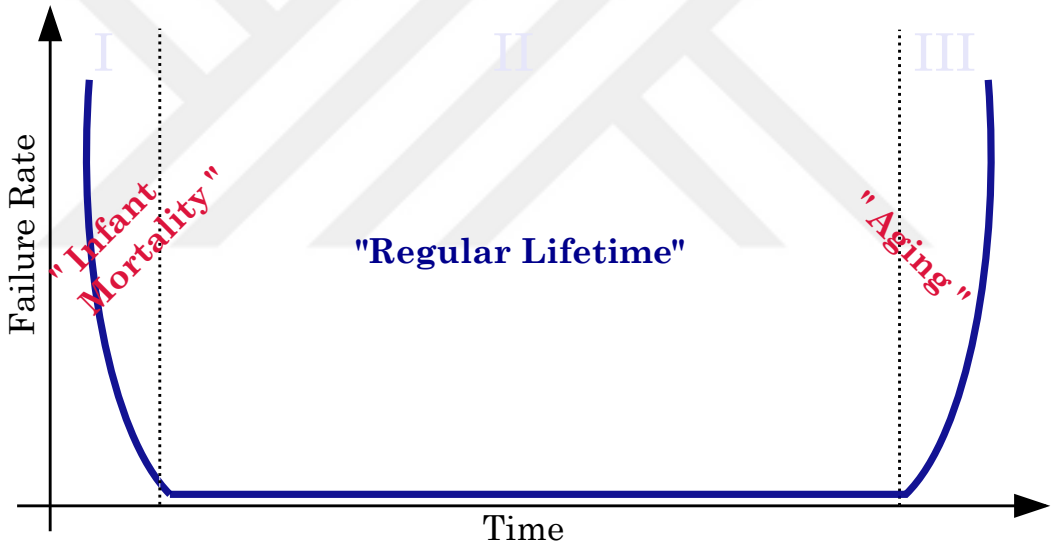

Figure 1.4. The bathtub curve.

The first period that is called "Infant Mortality" corresponds to circuits, where a wide range of process defects lead to high failure rates and to circuits that would never reach the normal operating period in their lifetime. Thereby, IC foundries should catch these devices before they are released to the market. At the end of this period, failure rate diminishes, thus a certain yield is guaranteed after the fabrication. The second phase called "Regular Period" represents circuits, which successfully pass the burn in tests and come out to the market. Regular period should be the longest period among

all life period of products because the efficiency of the product reaches the maximum value at this period. At last, circuits reach the third phase called “Aging”, where their behavior starts to worsen, finally resulting in circuit malfunction after a certain time.

The first major aim of reliability-aware circuit design is to reduce the failure rate at the end of the first phase. Conventionally, variability analysis is performed and the design is revised in order to reduce the effect of variation, thus achieving high yield. Although yield analysis increases the total design time, numerous enhanced variability analyses have been proposed in order to decrease the design time. Furthermore, analog circuit sizing tools have been replaced by variation-aware ones, where yield is defined as a new constraint and included into the conventional optimization problem and optimized as well as electrical constraints. However, the integration of yield estimation with an analog circuit synthesis tool is quite problematic, where the trade-off between accuracy of yield estimation and efficiency of the synthesis tool challenges this integration process.

Three different variation-aware analog circuit synthesis tools are proposed in this thesis. Both inter and intra-die variation models should be utilized during variability simulations and these were verified on silicon via design and characterization of a test chip using 130 nm. The first tool utilizes a sensitivity-based approach for the variability analysis, where two different integration scenarios are proposed for the integration of variability analysis with analog circuit synthesis: Over-design and Robust-design approaches. The second tool utilizes a Quasi-Monte Carlo (QMC) based variability analysis. In this approach, an infeasible solution elimination approach is proposed for the integration process, where a simulation budget allocation algorithm is also used to distribute a simulation budget among candidate circuits depending on their yield. The last tool uses a hybrid QMC, where an additional scrambled QMC is assigned to create artificial variance and obtain a confidence interval for the yield estimation, which is impossible for QMC due to its deterministic nature. To keep the tool efficient, a two level infeasible solution elimination is performed. Results of this last tool were verified on silicon.

The second aim of reliability-aware circuit design is to increase the regular lifetime of ICs, where aging induced performance degradation takes place at the end of the regular period. Aging in CMOS circuits stems from four major physical phenomena: Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), Time Dependent Dielectric Breakdown (TDDB), and Electromigration (EM). HCI affects NMOS transistors and is effective only while transistors are conducting current. Negative BTI (NBTI) affects PMOS transistors and is effective when the transistor is on. Positive BTI (PBTI) seen in NMOS transistors isn't as effective as NBTI, so its effects can be neglected compared to the other reliability issues. Both NBTI and HCI effects manifest themselves as a reduction in the drain current as the devices age. TDDB, on the other hand, causes the dielectric to break down and become electrically shorted after some operation time. Another aging mechanism occurring in CMOS circuits is EM, which is an interconnect degradation phenomenon and can be avoided by limiting current density in the wires to safe limits. A further discussion on degradation mechanisms is provided in Section 2.3.

In contrast to variability, aging is a more recent problem, which is considered as a major reliability problem for technologies below 180 nm. Furthermore, aging analysis (modeling, simulating, and observing the aging effects) is relatively difficult to be performed compared to variation analysis due to time dependency. Similar to variation-aware circuit synthesis, the trade-off between efficiency and accuracy is also a challenging problem for lifetime aware analog circuit synthesis. To overcome the model inaccuracy problem, a semi-empirical model for 130 nm technology was developed via acceleration aging test (AAT) performed on silicon. Furthermore, a deterministic aging simulator tool with adjustable step-size is proposed in this thesis. The adjustable step-size approach promises determination of step-size considering both accuracy and efficiency, thus, unnecessary simulations are avoided, which is highly crucial for lifetime-aware circuit synthesis. By integrating this simulator with an analog circuit synthesis tool, a lifetime-aware circuit synthesis tool is developed, which is the first tool to our best knowledge that considers lifetime during synthesis process.

Reconfigurable circuit design is another way to design robust analog circuits. Conventionally, lifetime-aware circuit design depends on designing circuits considering aging effects and revise the design, if necessary. Typically, circuits are overdesigned for the sake of lifetime, where power consumption and area occupation are sacrificed. On the other hand, reconfigurable circuit design approaches depend on healing circuits when they age by activating ad hoc recovery operations. Typically, recovery blocks are dormant until an external enable signal awakens them, thus, they do not consume any additional power. In addition to that, area occupation of a typical reconfigurable system would not be very large since most of the circuits are digital, so device sizes are considerably smaller. Another important advantage of reconfigurable circuit design is that the degraded circuit performance can be fully recovered by a proper recovery operation. Sense and React (S&R)approach is the well-known reconfigurable design approach, in which the design is monitored and the degradation on circuit performances is sensed via a sensor circuit. If any degradation occurs, the recovery is activated and circuit performance loss is compensated. A challenging problem arises during the sense operation, where it is not possible to measure the degradation on any circuit performance directly. Therefore, indirect measurements are preferred, where measurable electrical quantities (voltage, current, frequency etc.), which are called signatures, are used to detect the degradation. The problem with indirect measurement is that a correlation between circuit features and aging signatures is necessary to determine the efficient signature. Considering a large number of candidate signatures, determination of the signature manually would be very time consuming and expensive. On the other hand, the design of the react operation is application specific, where an expert designer can determine a proper recovery operation for a given circuit. However, a large number of iterations are needed to do this, which is a very time consuming process to perform manually.

Main contributions of this thesis are as follows;

A SPICE-based single objective analog circuit synthesis tool proposed in [5] is implemented to be used as the optimizer engine in reliability-aware synthesis. Furthermore, a novel mixed domain sizing approach for RF circuit synthesis is proposed, which

promises more accurate results at the SPICE level simulations by including layout-induced parasitics of passive devices. Thus, the discrepancy between the schematic and post-layout simulations is substantially reduced.

A test chip including differently sized single transistors was designed and measured in order to obtain technology variation model parameters for 130 nm technology. In addition to that, a semi empirical NBTI model is also developed for the utilized technology by performing AAT on the test chip. The proposed model is verified by comparing simulation and measurement results.

Variation-aware analog circuit optimization is discussed in detail and two different approaches are utilized during variability analysis: Sensitivity and QMC. Two different integration scenarios are proposed for sensitivity optimization: Over-design and Robust-design approaches. On the other hand, two different approaches are developed for QMC-based synthesis. In the first one, a conventional Quasi-Monte Carlo (QMC)-based variability analysis is utilized while the second tool uses a scrambled QMC for the yield estimation. Furthermore, results of this last tool were verified on silicon.

A deterministic aging simulator with adaptive step size is proposed in this thesis as to be used in lifetime aware synthesis. By using this simulator and analog circuit synthesis tool, a lifetime-aware analog circuit synthesis tool is proposed in this thesis. To our best knowledge, this is the first implementation example of aging-aware analog circuit synthesis.

As the last part of this thesis, S&R systems are studied in detail. At first, an efficient aging signature selection approach is proposed, where all necessary properties of an efficient signature are clearly described and taken into account during the selection process. Furthermore, a semi-automatic recovery operation determination process is described in order to keep the design time of recovery operation at minimum. Finally, two different S&R systems are proposed and realized for two different circuits.

This thesis is organized as follows. In Section 2, a detailed background on analog circuit synthesis, variability problem, aging in CMOS circuits, reliability-aware circuit synthesis and reconfigurable analog circuit design is provided. In Section 3, the utilized analog/RF circuit synthesis tools are introduced and explained in detail with synthesis examples. In Section 4, measurements for variation models are explained, the developed variation-aware analog circuit synthesis tools are introduced and thoroughly discussed. In Section 5, semi-empirical model development process is explained, the developed aging simulator and lifetime-aware circuit synthesis tools are presented and discussed. In Section 6, the design of a S&R system is examined, from signature selection to determination of recovery operation and two different S&R approaches are proposed by providing the whole system design process and simulation results. Finally, Section 7 concludes this thesis by providing the conclusion and future work.

2. BACKGROUND

It is commonly believed that a scientist should be able to explain her/his study to anyone regardless of her/his knowledge on the subject. The first step would be giving some fundamental knowledge about the work before starting a detailed discussion. Therefore, a typical Ph.D. thesis includes a background chapter in order to provide the essential knowledge to interested readers. As introduced in the previous chapter, this thesis has four main topics, which are:

- Analog circuit synthesis/optimization
- Variability phenomenon and yield-aware circuit synthesis
- Aging phenomena and lifetime-aware circuit synthesis
- Reconfigurable circuit design methodologies

In this chapter, essential background behind these topics are provided. Hence, anyone who has little or even no knowledge in these different topics would be familiar with them before the more involved discussion on the main work.

2.1. Analog Circuit Synthesis/Optimization

Conventionally, analog design flow can be decomposed into three different levels, which are system, circuit, and layout levels, respectively. A flow chart including all these sub-levels and intermediate steps is provided in Figure 2.1. The design starts at the highest level by determining the system requirements. Commonly, a behavioral description of the system is initially performed in order to mimic the system behavior and determine the circuit level specifications. Then, a feasibility check is performed for these specifications to determine whether they are feasible or not. At the circuit level, each sub-circuit is designed and evaluated via SPICE simulators. At the layout level, the physical layout of each circuit is drawn and individually re-evaluated by post-layout simulations.

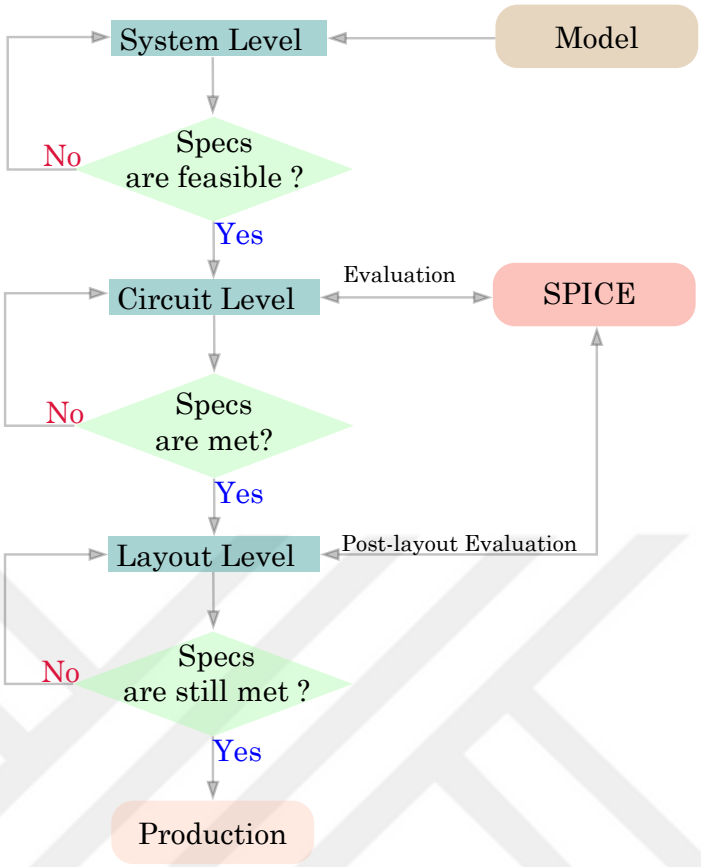

Figure 2.1. Analog design flow.

However, increased design complexity and challenging trade-offs between different circuit specifications in the advanced technology nodes have complicated the flow resulting in an excessively long time to market. To deal with this problem, circuit sizing and layout generation have been automated via design automation systems in order to manage the design flow more efficiently and ultimately reduce the time to market.

2.1.1. Analog Circuit Sizing

Circuit sizing or more generally analog design automation approaches are classified under three categories: knowledge-based approaches, simulation-based approaches, and equation-based approaches.

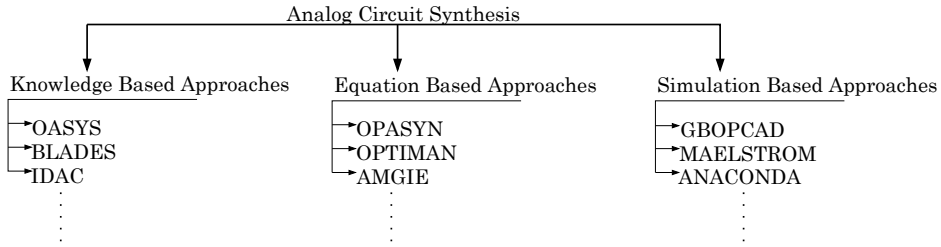

Figure 2.2. Analog circuit sizing approaches.

Knowledge-based approach was the earliest approach, which requires designer expertise and design strategies for each different circuit topology during the construction of the automatic synthesis process. Typically, designer insight is included into the computer programs via simplified equations and heuristics [5]. A number of different knowledge-based approaches have been proposed in the literature, such as OASYS [6], BLADES [7], and IDAC [8]. Even though such tools promise relatively fast synthesis, the results may not be reliable due to excessively simplified device/circuit models. Additionally, topology dependency and initial designer effort during the model generation also degrades the efficiency of those approaches, where model generation has become a very challenging and time consuming process, considering the increased non-linearity and complexity of the advanced technology nodes.

Equation-based optimization tools such as OPASYN [9], OPTIMAN [10], and AMGIE [11] are also used for analog circuit sizing, which utilizes analytical equations to evaluate the circuit performance. Similar to the knowledge-based approaches, these equation-based tools also suffer from the accuracy problem due to the simplified models. Even though using more complicated models improve the reliability of the synthesis, the optimizer efficiency degrades due to sophisticated higher order equations. The construction process of such complicated models is also very time consuming, where each circuit topology requires a particular model generation process.

As a result of the increased non-linearity effects through the rapidly developing CMOS technology, analog circuit analysis and design has become a very challeng-

ing and time consuming process. Therefore, constructing models for equation-based approaches have become impractical since they require particular model generation for each circuit topology. Even if the model is generated via CAD tools, the accuracy of the developed model may cause problems at the implementation level. Together with this bottleneck of the equation-based approach, availability of very high speed computers and sophisticated circuit simulators has resulted in a trend towards simulation-based circuit synthesis approaches. Simulation-based approach promises a SPICE-level accuracy, where some commercial SPICE-based optimization tools are presented in [12], [13], and [1].

2.1.2. Hierarchical Analog Circuit Synthesis

A further problem manifests itself during the optimization of a complicated system rather than a single block/circuit. Traditionally, an expert IC designer designs such a system within a hierarchical manner rather than a flat design by mostly using top-down approach shown in Figure 2.1. The idea behind the hierarchical approach is dividing large-scale systems into sub-blocks, searching for a proper solution for each sub-block, and assembling these sub-solutions at the highest level. A hierarchical synthesis approach similar to that applied by human designers can also be performed to deal with the complex system designs. Top-down approaches are commonly used for hierarchical design due to their manageable simulation and optimization complexity at each hierarchical level [14–18]. The synthesis starts at the system-level with system design variables (design parameters and sub-block specifications). In general, sub-blocks are represented by behavioral models. Once the optimal solution at a given level is achieved, the required sub-block specifications are transmitted to the lower level. Then, the lower level optimizer tries to meet the specifications sent by the higher level and finds its optimal solution. Thanks to the application of behavioral modeling techniques, the computational effort is acceptable at higher hierarchical levels. However, conventional top-down approaches also have some limitations. The first one is that specifications are transmitted from the top-level to the bottom-level without knowing if such specifications are feasible or not. If the lower level optimizer

cannot satisfy these specifications, redesign iterations would be needed, which delays the synthesis process. The second limitation of top-down approaches is that specifications are transmitted at higher levels without sufficient information about essential parameters like area and power consumption. Very frequently a different specification transmission may lead to better global power and area figures. Furthermore, parallelization of a hierarchical optimization is also feasible and will decrease optimization time further. In conjunction with this thesis, two different hierarchical analog circuit synthesis approaches are proposed in [19]. They are based on the concurrent design at higher and lower hierarchical levels and appropriate communication between the different processes to address the limitations of the conventional top-down approach.

2.1.3. Automatic Layout Generation

On the other hand, layout generation is a considerably different problem, where the area is tried to be minimized for a given circuit using different templates, floor planning, placement, and routing scenarios by utilizing an optimization engine. Actually, layout-generation is not a part of this thesis; however, one should consider that the integration of the sizing and layout generation tools is another difficult problem. There are several CAD tools supporting layout-aware circuit sizing [20–30]. The main idea behind most of these tools are quite similar, in which layout-parasitics are analytically estimated and these estimations are then taken into account during circuit sizing without any layout realization. Even though such approaches show better computational performances, severe accuracy problems occur due to estimation errors, which lead to re-iterations, thus increasing the total synthesis time. Contrary to the others, [20] and [30] generate a layout and minimizes the layout area by extracting the parasitics at each iteration. Efficiency is the main problem of this type of integration, where generation of the layout at every iteration is highly expensive. These tools either suffer from long run times or limited accuracy of the utilized parasitic model. In conjunction with this thesis, a complete layout-aware design automation tool for analog circuits is proposed in [31]. The proposed tool combines a simulation-based circuit sizing tool with a template-based layout generation tool. The layout-induced

parasitics are automatically extracted via a commercially available extractor. To reduce the run time cost originating from parasitic extraction, a two step methodology is followed, where infeasible solutions are prohibited from the costly extraction process.

2.2. Process Variation and Mismatch

The scaling of feature size has progressed more rapidly than the scaling of process tolerances in CMOS technology. As a result, the variation in different fabrication steps such as line-edge roughness (LER), oxide thickness fluctuations (OTF), and random dopant fluctuations (RDF) in sub-micron technologies have become difficult to control during the fabrication. These worsening variation problems lead to undesired parameter shifts on devices, which ultimately create unexpected side effects after the fabrication. More obviously, if a circuit was designed to achieve specific nominal values of performances, a dispersion between the desired and actual performances can be expected in a population of fabricated chips [32]. The physical uncertainties occur after the fabrication process, where fundamental sources of variations are depicted in Figure 2.3.

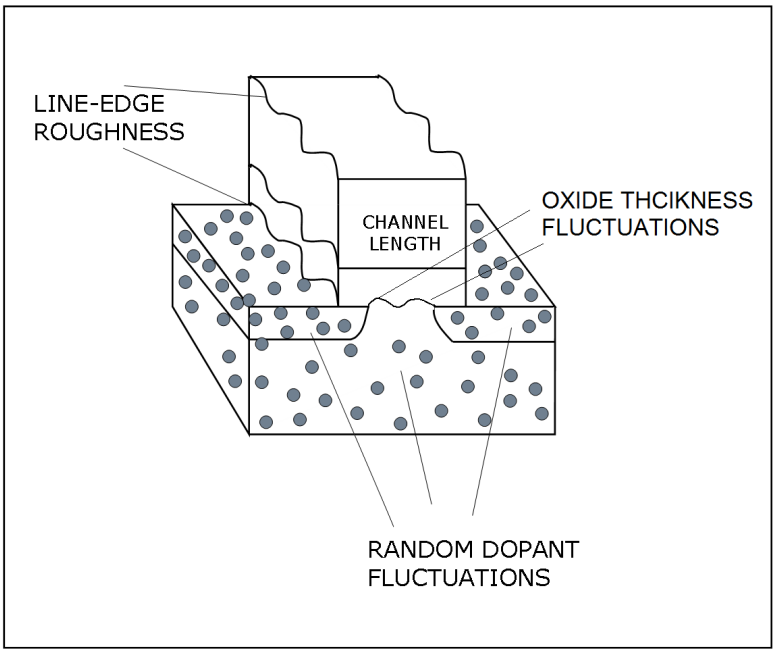

Figure 2.3. Fundamental variations in a CMOS device [32].

- RDF is caused by the uncertainty at charge location and numbers such as the discrete placement of dopant atoms following a normal distribution. As the device sizes scale down, the total number of channel dopants decreases resulting in the increased variation of dopant numbers, which ultimately change the threshold voltage [33].
- LER is the distortion of the gate edge, which is induced by gate etching and the lithography processes [2]. Even though the etching technology has been enhanced, the trend of LER induced V_{th} variation can not scale due to increasingly severe short-channel effects. LER contributes to a significant amount of V_{th} variation [2] as well.
- OTF is induced by the atom-level interface roughness between silicon and gate dielectric [3]. Such a surface roughness lead to the fluctuation of the voltage drop across the oxide layer and changing V_{th}. OTF have become more pronounced as gate dielectric thickness (t_{ox}) becomes thinner.

Conventionally, variation in ICs is classified into two different mechanisms. Typically, two identically designed transistors are assumed to have the same electrical parameters; thus, they have the same drain currents under identical bias conditions. However, this case is not always valid in practice since there is always a mismatch between any two transistors located at different places on a wafer, due to the variations [34]. As a result, the current of a transistor is directly related to its location on the wafer because of the non-idealities over the whole wafer. This is called "intra-die" variations. On the other hand, dies including the same circuits can also be different from each other because of global variations. This type of variations is called "inter-die variations".

Stochastic mismatch can only be mitigated with better process control and larger transistor areas [35]. The effect of W/L ratio also influences transistor mismatch. In [36] it was shown how matching can be improved without changing the layout area. Better matching can be obtained with more suitable ratios. This, however, reduces the switching speed due to using larger channel lengths [35].

On the other hand, systematic mismatch can be reduced to a great extent with proper layout. For the best matching of two equally designed devices, they should be placed in the layout as close as possible with their wider side in parallel. In Figure 2.4, the transistor pairs 1-3 and 2-4 match better than 1-2 and 3-4. Much better results can be achieved by dividing a transistor in smaller devices connected in parallel (inter-digitated devices) that are arranged in different patterns [37].

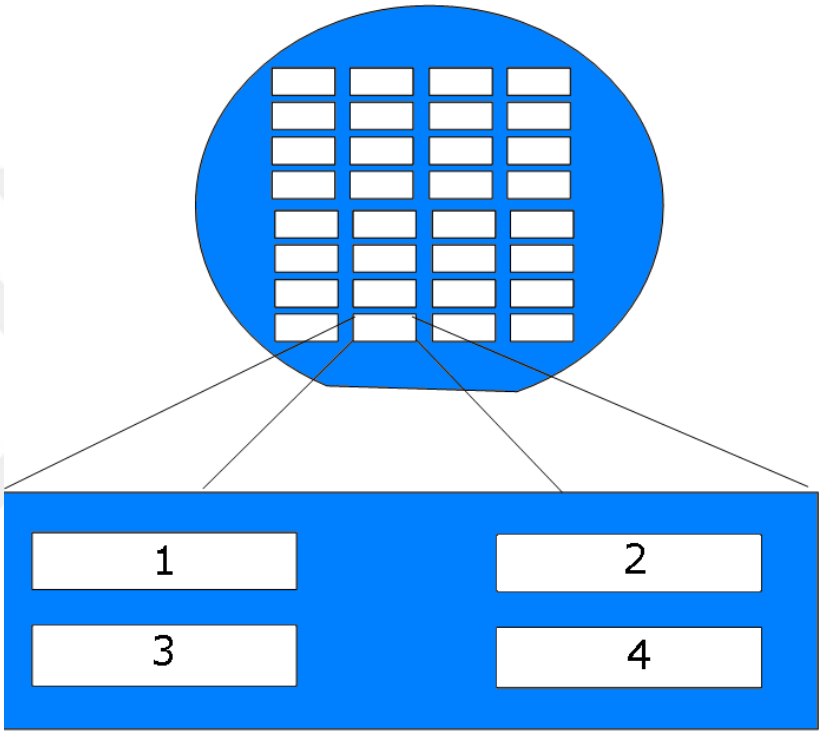

Figure 2.4. The distance between two transistors reduces the systematic mismatch.

In general, parametric variations are modelled by two different ways;

- Modelling of Electrical Parameters
- Modelling of Physical Parameters

The first successful electrical model was proposed by Pelgrom [38] as given in Equation 2.1 and Equation 2.2. Considering this model, the mismatch between two transistors is modelled via modelling the variance of threshold voltage (V_{th}) and current factor (β).

$$\sigma^2_{V_{th}} = \frac{A^2_{\sigma_{V_{th}}}}{W.L} + S^2_{\sigma_{V_{th}}} D^2 \tag{2.1}$$

$$\frac{\sigma^2_\beta}{\beta} = \frac{A_{\sigma_\beta}}{W.L} + S^2_{\sigma_\beta} D^2 \tag{2.2}$$

The terms $A_{\sigma_{V_{th}}}$, A_{σ_β}, $S_{\sigma_{V_{th}}}$ and S_{σ_β} are technology dependent constants and D is the distance between two transistors. $A_{\sigma_{V_{th}}}$ and A_{σ_β} values for different technology nodes were reported in [39] as given in Figure 2.5.

However, this model is not valid for short-channel devices. Furthermore, considering the variations in device geometries, it was shown that using effective channel lengths rather than the designed ones provides more accurate results. As a result, considering both short channel device and effective dimensions, the variance of the threshold voltage and current factor were modelled as [36, 40];

$$\sigma^2_{V_{th}} = \frac{{A_1}^2_{\sigma_{V_{th}}}}{W_{eff}.L_{eff}} + \frac{{A_2}^2_{\sigma_{V_{th}}}}{W_{eff}.L^2_{eff}} - \frac{{A_3}^2_{\sigma_{V_{th}}}}{W^2_{eff}.L_{eff}} + S^2_{\sigma_{V_{th}}} D^2 \tag{2.3}$$

$$\sigma^2_\beta = \frac{{A_1}^2_{\sigma_\beta}}{W_{eff}.L_{eff}} + \frac{{A_2}^2_{\sigma_\beta}}{W_{eff}.L^2_{eff}} - \frac{{A_3}^2_{\sigma_\beta}}{W^2_{eff}.L_{eff}} + S^2_{\sigma_\beta} D^2 \tag{2.4}$$

By combining these equations, the total variation in the drain current can be modeled as;

$$\frac{\sigma^2 \Delta I}{I^2} = \frac{\sigma^2 \Delta\beta}{\beta^2} + \frac{4\sigma^2 \Delta V_{th}}{(V_{GS} - V_{TH})^2} \tag{2.5}$$

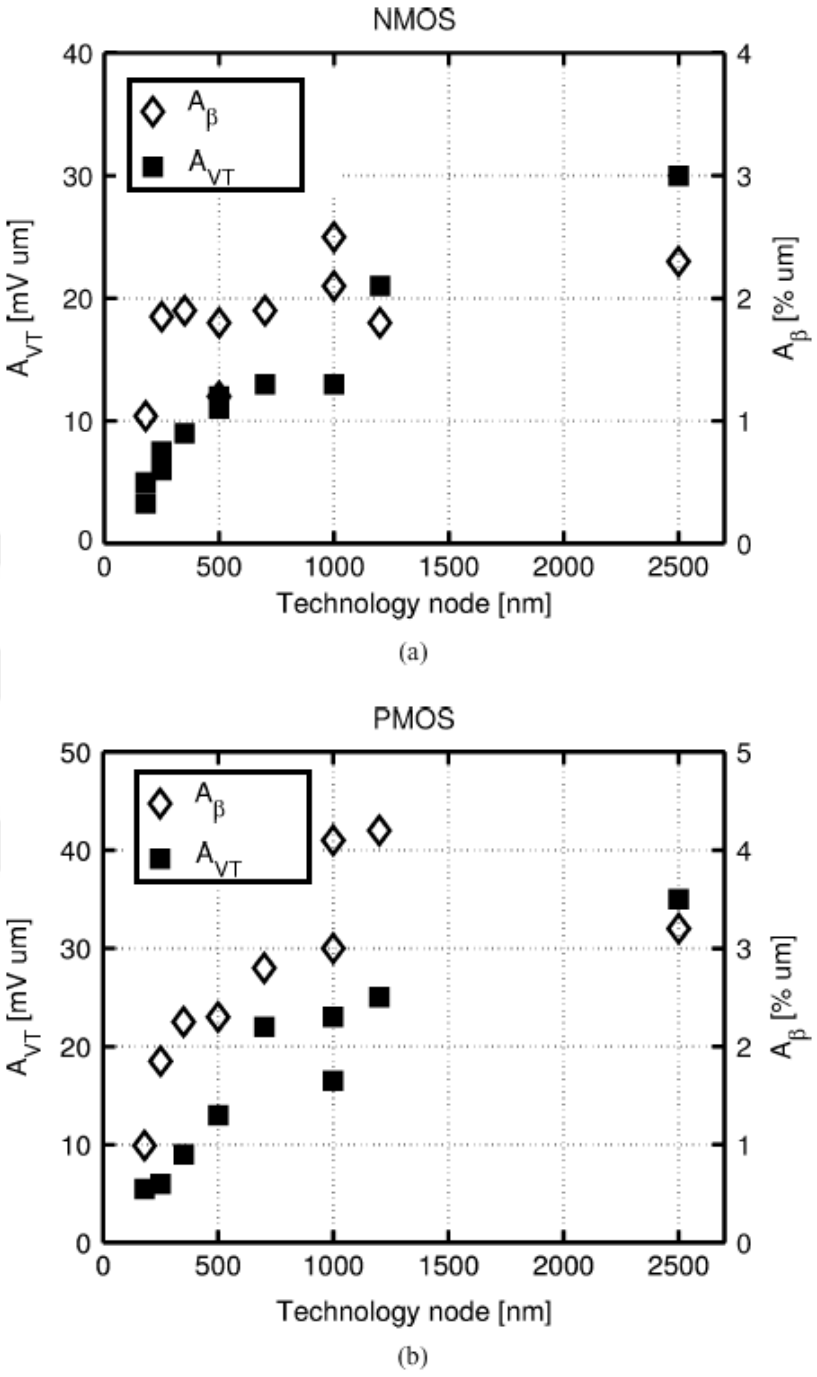

Figure 2.5. Technology dependent constants for n and p type devices [39].

Pelgrom model has been widely used to model the mismatch phenomenon. However, variations on the wafer arise from two different sources of process non-uniformity. These are random (local) and systematic (global) variations. The Pelgrom model assumes that both components are random. This can be true for small regions on the

die. However, considering the entire die, global variation must contain a systematic component instead of being fully random [34]. One should consider this problem in order to make reliable estimations of variation effects.

Physical parameters can also be used to model the mismatch effect. Since most electrical parameters can be expressed as functions of physical parameters, electrical parameters are directly related to the physical parameters. Figure 2.6 summarizes the relationship between the physical and electrical models.

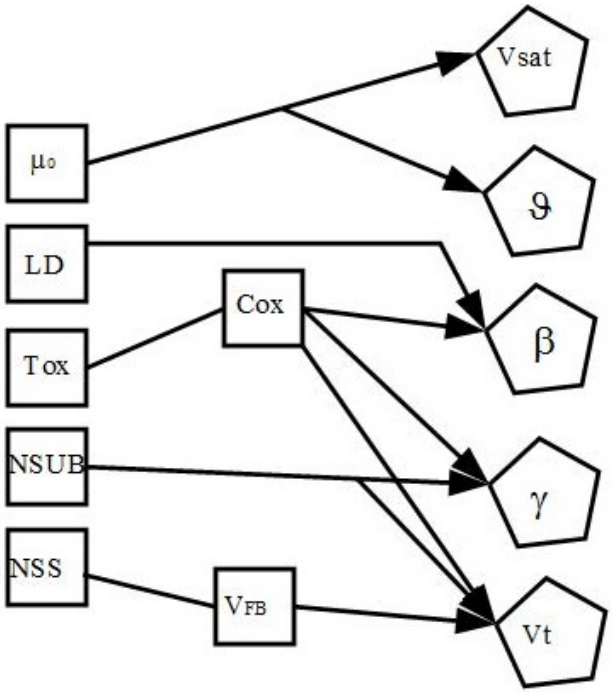

Figure 2.6. Relationship of physical and electrical parameters [34].

Sensitivity method is highly useful for physical modelling of the mismatch rather than directly characterizing the variance of electrical parameters [41]. Mismatch in the drain current is measured over geometry and bias, and variance of any parameter can be calculated from backward propagation of variance(BPV) [42, 43]: measure $\sigma^2_{I_d}$, simulate $\delta I_d/\delta p_j$, and calculate $\sigma^2_{p_j}$, where the sensitivities are computed from the SPICE models for each bias and geometry.

$$\sigma^2_{I_d} = \Sigma(\delta I_d/\delta p_j)^2 \sigma^2_{p_j} \tag{2.6}$$

$$\begin{pmatrix} \sigma^2_{I_{d_1}} \\ \sigma^2_{I_{d_2}} \\ \sigma^2_{I_{d_3}} \\ \sigma^2_{I_{d_4}} \\ \vdots \\ \sigma^2_{I_{dn}} \end{pmatrix} = \begin{pmatrix} \frac{\delta I_1}{\delta \Delta W} & \frac{\delta I_1}{\delta t_{ox}} & \frac{\delta I_1}{\delta V_{fb}} & \frac{\delta I_1}{\delta \mu_0} & \frac{\delta I_1}{\delta \Delta_L} & \frac{\delta I_1}{\delta V_{tl}} & \frac{\delta I_1}{\varphi_{SH}} & \frac{\delta I_1}{N_{sub}} \\ \frac{\delta I_2}{\delta \Delta W} & \frac{\delta I_2}{\delta t_{ox}} & \frac{\delta I_2}{\delta V_{fb}} & \frac{\delta I_2}{\delta \mu_0} & \frac{\delta I_2}{\delta \Delta_L} & \frac{\delta I_2}{\delta V_{tl}} & \frac{\delta I_2}{\varphi_{SH}} & \frac{\delta I_2}{N_{sub}} \\ \frac{\delta I_3}{\delta \Delta W} & \frac{\delta I_3}{\delta t_{ox}} & \frac{\delta I_3}{\delta V_{fb}} & \frac{\delta I_3}{\delta \mu_0} & \frac{\delta I_3}{\delta \Delta_L} & \frac{\delta I_3}{\delta V_{tl}} & \frac{\delta I_3}{\varphi_{SH}} & \frac{\delta I_3}{N_{sub}} \\ \frac{\delta I_4}{\delta \Delta W} & \frac{\delta I_4}{\delta t_{ox}} & \frac{\delta I_4}{\delta V_{fb}} & \frac{\delta I_4}{\delta \mu_0} & \frac{\delta I_4}{\delta \Delta_L} & \frac{\delta I_4}{\delta V_{tl}} & \frac{\delta I_4}{\varphi_{SH}} & \frac{\delta I_4}{N_{sub}} \\ \vdots & \vdots & \ddots & \vdots & & & & \\ \frac{\delta I_n}{\delta \Delta W} & \frac{\delta I_n}{\delta t_{ox}} & \frac{\delta I_n}{\delta V_{fb}} & \frac{\delta I_n}{\delta \mu_0} & \frac{\delta I_n}{\delta \Delta_L} & \frac{\delta I_n}{\delta V_{tl}} & \frac{\delta I_n}{\varphi_{SH}} & \frac{\delta I_n}{N_{sub}} \end{pmatrix}^2 = \begin{pmatrix} \frac{\sigma^2_{\Delta W}}{L} \\ \frac{\sigma^2_{t_{ox}}}{WL} \\ \frac{\sigma^2_{V_{fb}}}{WL} \\ \frac{\sigma^2_{\mu_0}}{WL} \\ \vdots \\ \frac{\sigma^2_{N_{sub}}}{WL} \end{pmatrix} \tag{2.7}$$

The advantage of physical models is that the correlation between different parameters is automatically inserted into the device electrical parameters while electrical models do not provide correlations between parameters. However, due to the increased nonlinearities, only small changes can be converted into the electrical changes. The variation of the physical parameters has a Gaussian distribution, whereas the distribution may be deteriorated after conversion as depicted in Figure 2.7.

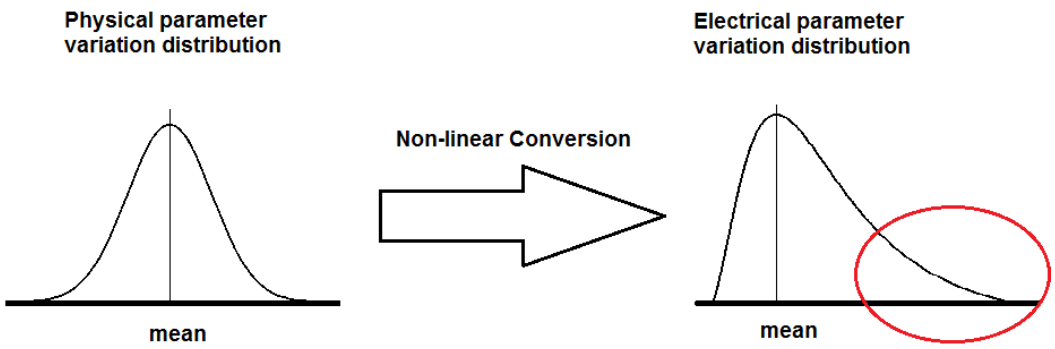

Figure 2.7. Sensitivity approach loses functionality due to non-linear effect of higher order equations on the parameter variation probability disturbution function.

2.3. Aging: Time Dependent Reliability Issues In CMOS Technology

As a result of the combination of high electrical field and thermal stress on CMOS devices with channel lengths 180 nm and below, aging has become more pronounced in integrated circuits. Conventionally, four different aging mechanisms cause aging in CMOS circuits [44]. These are;

- Hot Carrier Injection (HCI)
- Bias Temperature Instability (BTI)
- Time Dependent Dielectric Breakdown (TDDB)
- Electromigration (EM)

2.3.1. Hot Carrier Injection

Hot Carrier Injection (HCI) is a degradation mechanism that is usually considered for N-type devices. The term "hot carriers" refers to either holes (for P-type) or electrons (for N-type) accelerated by a lateral electric field [45]. Because of high energy at the drain extension, impact ionization occurs above the pinch-off region and hot carriers get trapped into the oxide and create interface states, while holes move downwards and constitute a substrate current as depicted in Figure 2.8.

Traps cause an increase in the threshold voltage and reduce the channel mobility due to scattering along the channel [46]. The maximum hot carrier damage has traditionally been associated with the peak I_{sub} region, where $V_{gs} \approx V_{ds}/2$ and the substrate current is exponentially proportional to $V_{ds} - V_{dsat}$ [47]. The longitudinal electric field responsible for primary impact ionization generates hot carriers with energy around 1.5 eV, whereas secondary impact ionization generates hot carriers with energy values of 3 to 3.5 eV. Conventionally, it has been assumed that HCI is negligible in p-channel devices [48]. This is due to lower hole mobility. The effects of gate and drain voltage waveforms on the hot carrier induced MOSFET degradation are studied in [49]. According to the results [49], the pulsing of drain voltage has been shown to introduce no perceivable difference in device degradation. On the other hand, it has been found

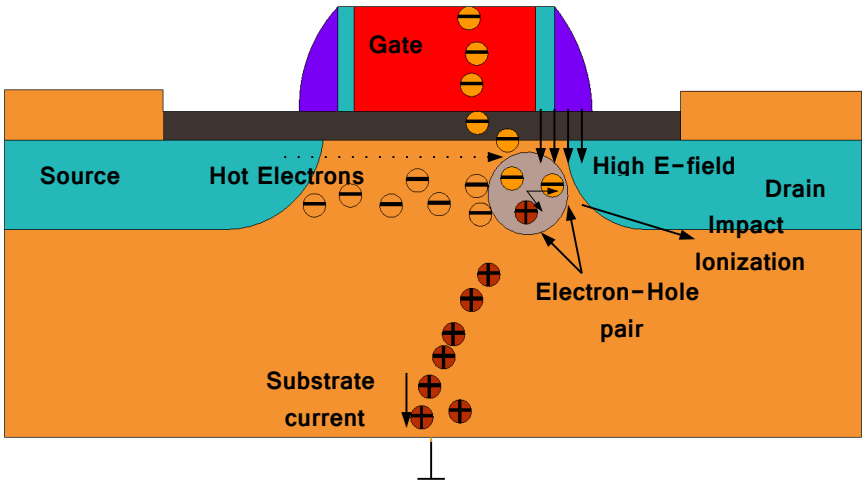

Figure 2.8. Hot Carrier Injection occurs at the drain extension due to high electric field causing interface states that trap charges that increases V_{th}.

that the falling edge of the gate pulse in the presence of high drain voltage is the main source of the enhanced degradation rates [49]. In the light of these observations, it can be concluded that the HCI effect is more severe for digital circuits, where the device is periodically exposed to such a stress condition.

There are two main contributors behind HCI: Drain Avalanche Hot Carrier (DAHC) and Channel Hot Electron (CHE). DAHC occurs at the maximum substrate current condition (I_{submax}), where interface trap generation causes increase in the threshold voltage and decrease in the drain current [50–53]. At stress conditions with higher V_{ds} and lower V_{gs}, (DAHC) injection becomes important [54]. The acceleration of the carriers cause them to collide with silicon atoms, creating electron-hole pairs (impact ionization). In NMOS transistors, this primary impact ionization takes place at the drain, where the carriers achieve the saturation velocity [55]. Under the influence of drain-to-gate field, hot carriers that surmount the substrate-gate oxide barrier get injected into the gate oxide. Hot carriers can be trapped at the Si/SiO_2 interface (hence referred to as "interface states") or within the oxide itself, forming a space charge that increases over time as more charges are trapped. Contrary to DAHC, CHE regime reaches the maximum value when the gate voltage is equal to the drain

voltage. Electrons, which are called "lucky" [56, 57], are attracted by the high gate voltage by means of gaining sufficient energy from the electric field across the channel to overcome the Si/SiO_2 barrier at the drain side [58]. The effect of the drain voltage (V_d) on the surface potential (φ_s) reduces the conductivity of the channel near the drain side, thus increasing the lateral potential drop in the drain region. Therefore, the hot electrons near the drain region have enough energy to pass over the Si/SiO_2 energy barrier ($\phi_b = 3.15eV$) and they are injected into the gate, accelerated by the oxide electric field E_{ox}. The injection efficiency is strongly based on the lateral electric field that heats the channel electrons and E_{ox} in proximity of the drain that influences the tunnel probability $T_B(E_{ox})$ for the hot electrons. Near the drain region, the V_d influence on φ_s reduces the available potential drop in the oxide (V_{ox}), hence E_{ox} and $T_B(E_{ox})$.

2.3.2. Negative Bias Temperature Instability

In contrast to HCI, Negative Bias Temperature Instability (NBTI) occurs dominantly in p type devices. Charge trapping that is the main contribution of BTI is known to be considerably less for n-type devices than p-type devices, so PBTI effect can be neglected. However, due to increasing usage of high κ devices, in which charge trapping is more severe compared to conventional SiO_2, PBTI has become important especially for technologies beyond 45 nm [59, 60]. The high electrical field across the gate oxide in combination with an elevated temperature leads to an electrochemical reaction in the region of the interface between silicon and gate oxide [61]. Figure 2.9 represents a schematic of the interface. Due to different lattice structures of monocrystaline silicon and the amorphous oxide, an interface region that consists of a few atomic layers and many dangling bonds, which acts as interface states, occurs after gate oxide processing [61]. They can catch carriers, trap them for a certain time, and emit them back into the channel. Filled interface states shift the threshold voltage [61].

There are two different mechanisms associated with BTI. One is the direct breaking of Si-H bonds in the oxide. When a PMOS transistor is biased in inversion, the dissociation of Si-H bonds along the silicon-oxide interface causes the generation of

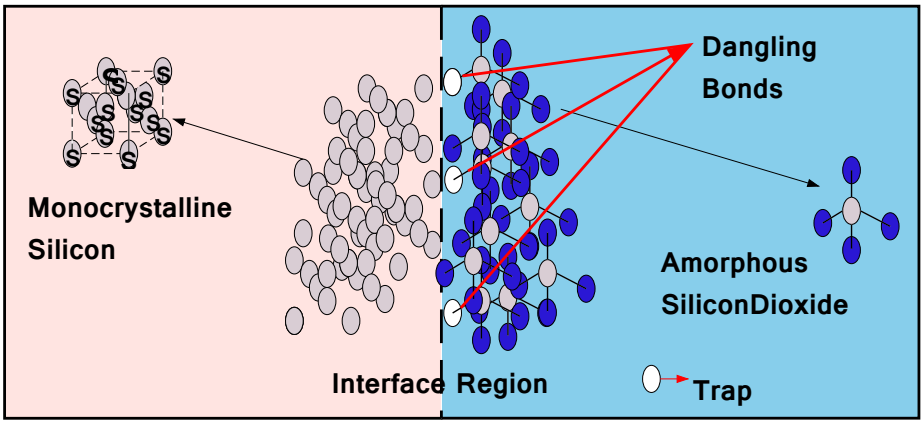

Figure 2.9. Schematic of the interface region of MOSFETs.

interface traps. The second event contributing to BTI is trapping. In addition to interface state generation, some preexisting traps located in the bulk of the dielectric are filled with holes originating from the channel of the PMOS. Absence of stress can recover some of the interface traps resulting in a partial relaxation [61]. The obvious consequence of NBTI on PMOS transistor is the increase in the threshold voltage and it is directly proportional to interface density as modeled in [46, 62]. Additionally, NBTI is categorized according to stress conditions: Static NBTI and Dynamic NBTI. Static NBTI corresponds to the case when the PMOS is under constant stress and this degradation can not be recovered. Dynamic NBTI corresponds to the case where the PMOS transistor undergoes alternating stress.

2.3.3. Time Dependent Dielectric Breakdown

Time-dependent gate oxide breakdown (or time-dependent dielectric breakdown, TDDB) is a failure mechanism in MOSFETs, when the gate oxide breaks down as a result of long-time application of electric field over the oxide. The breakdown is caused by formation of a conducting path through the gate oxide to the substrate due to electron tunneling current, when MOSFETs are operated close to or beyond their specified operating voltages. Defects in the gate oxide are usually called traps; they are called traps because the degraded oxide can capture charges [63]. Traps are generally neutral, but quickly become positively charged near the anode, and negatively charged

near the cathode [63]. Gate-oxide breakdown begins when the traps start to form in the gate-oxide. At the beginning, the number of traps is very low and conduction does not occur, but as the number of traps increases, they start to form a conduction path [64]. Once these traps form a conduction path from the gate to the channel, a breakdown occurs [64], which is called Soft Breakdown (SBD). Once there is conduction, new traps are generated by thermal damage allowing increased conductance [65]. The cycle of conduction causes excessive heat that results in thermal runaway and finally to a lateral propagation of the breakdown spot [65, 66]. The silicon-oxide within the breakdown region starts to melt, and oxygen gets released, and a silicon wire is formed in the breakdown region [65]. This type of breakdown is called Hard Breakdown (HBD) [67]. All these processes are depicted in Figure 2.10.

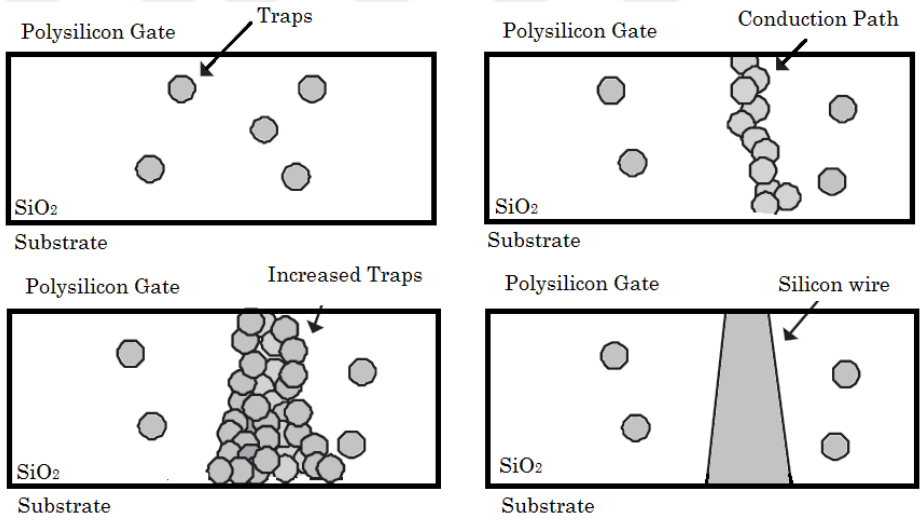

Figure 2.10. TDDB develops over time and oxide breaks down after a conduction path occurs.

2.3.4. Electromigration

Electromigration is another mechanism that can cause aging, which is the result of the diffusion of metal atoms along the conductor in the direction of electron flow. This directional diffusion process occurs because of the momentum transfer between the electrons and the metal atoms, which increases the probability that an aluminum atom will move in the direction of the electron flow shown in Figure 2.11 [68,69]. This

diffusion process will preferentially fill metal ion vacancies found in crystal defects, leaving a vacancy at the location from which the metal atom came. All metal films have micro-structural variations that cause the atomic flow rates through them to be non-uniformly distributed. This non-uniform atomic flow rates through different sections of the conductor result in mass depletion causing voids and mass accumulation causing hillocks as the mass transport mechanism occurs during electromigration. Electromigration is actually not a function of current, but a function of current density [70]. It is also accelerated by elevated temperature. Thus, electromigration is easily observed in Al metal lines that are subjected to high current densities at high temperature over time. As more general comments, HCI and BTI cause degradation

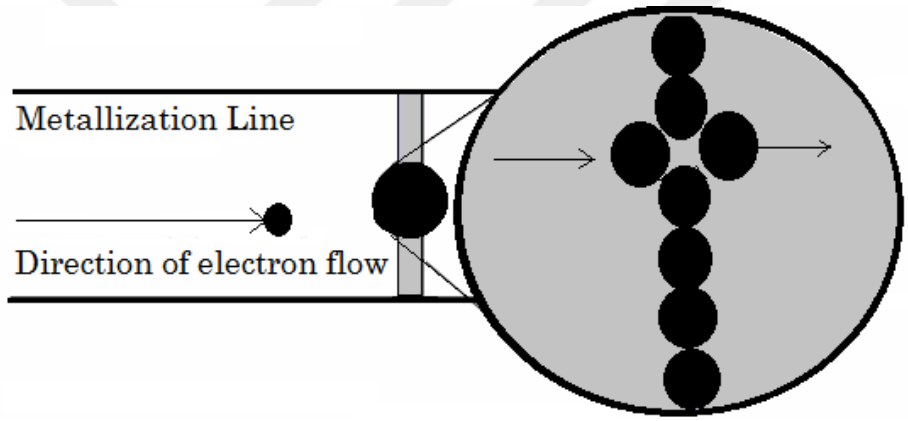

Figure 2.11. Electromigration occurs due to the momentum transfer of electrons to the metal ions.

in device parameters such as threshold voltage and mobility. This continuous degradation follows a saturated-power law behavior shown in Figure 2.12, which means most of the degradation occurs in the initial period of the lifetime of devices. This is due to decreasing number of interface states in HCI and decreasing probability of trapping in BTI, respectively. Changing device parameters degrades device current, transconductance, and some other electrical properties of devices, which turn out to be performance losses of circuits. Therefore, these two mechanisms have been commonly pronounced as the most critical degradation mechanisms in CMOS technology.

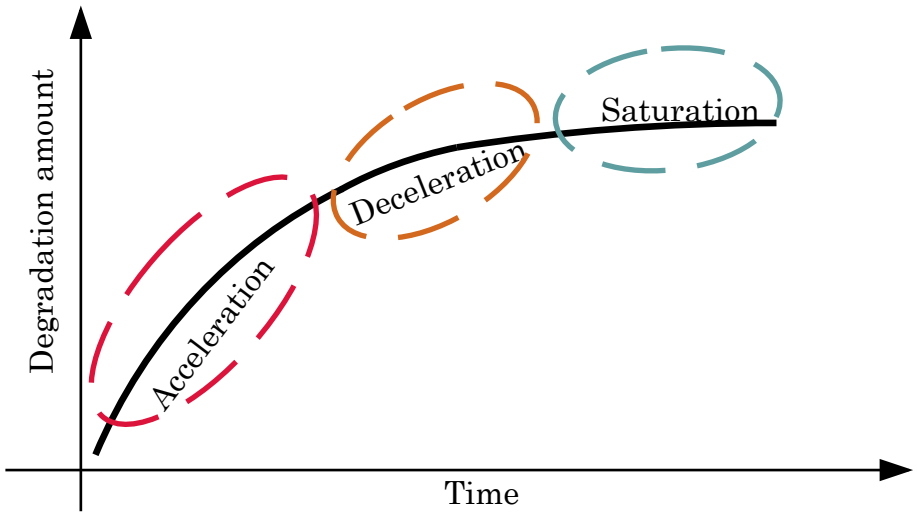

Figure 2.12. Aging exhibits a saturated-law behavior over time.

2.4. Reliability-aware Analog Circuit Design/Synthesis

Worsening process variations and aging effects over rapidly developing CMOS technology cause severe reliability problems in ICs. Process variation leads to a discrepancy between the expected and the actual performances in a population of manufactured ICs; thus, the yield is dramatically decreased. The case for aging is quite different, since it causes a time dependent degradation and manifests itself after a certain working period. After this regular period, circuits begin to lose their functionality, resulting in circuit malfunction. The aim of reliability aware circuit design is to design circuits robust to process variations and aging phenomena. Therefore, the analog design flow given in Figure 2.1 has been changed as given in Figure 2.13.

As seen from this revised flow, reliability analysis should be performed in order to estimate reliability information (yield and lifetime) of the design and revise the design, if necessary. As a result of increased complexity and expensive reliability issues, the total design time has become excessively longer to be performed manually. Even though automatic circuit sizing helps designers to reduce the design time, there is no guarantee that the solution is reliable, which results in re-optimization iterations and limits the efficiency. To palliate this problem, reliability analysis should be included

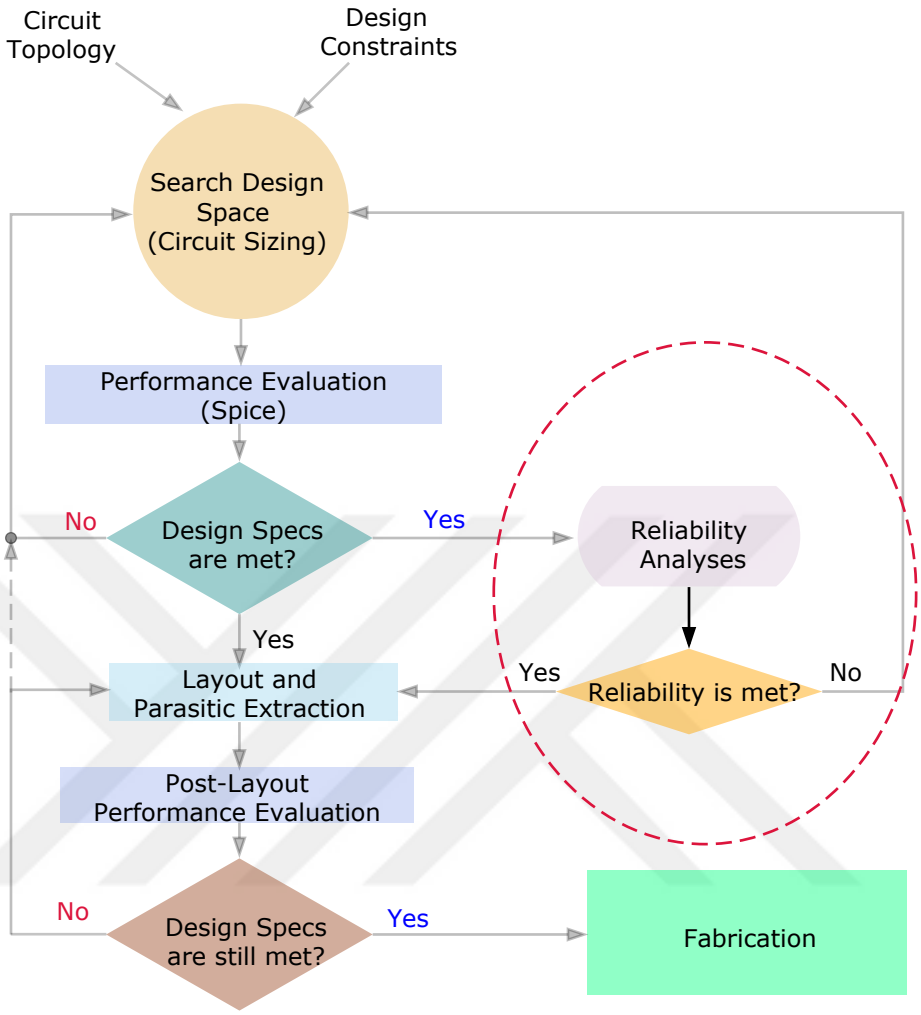

Figure 2.13. Reliaiblity aware circuit design.

into the circuit sizing loop as illustrated in Figure 2.14 by defining the reliability as a new design constraint as well as electrical design constraints.

On the one hand, variation-aware analog circuit synthesis has been studied during the last decade, and several tools have been developed in the literature. Even though automation of the analog sizing part improves the design time, expensive yield analysis still limits the total synthesis time. One should consider that there is a challenging trade-off between the accuracy and the efficiency, where a reliable yield analysis mostly requires a large number of simulations, thus degrading the efficiency. Therefore, an efficient yield analysis is required to manage this trade off. Nevertheless, the compu-

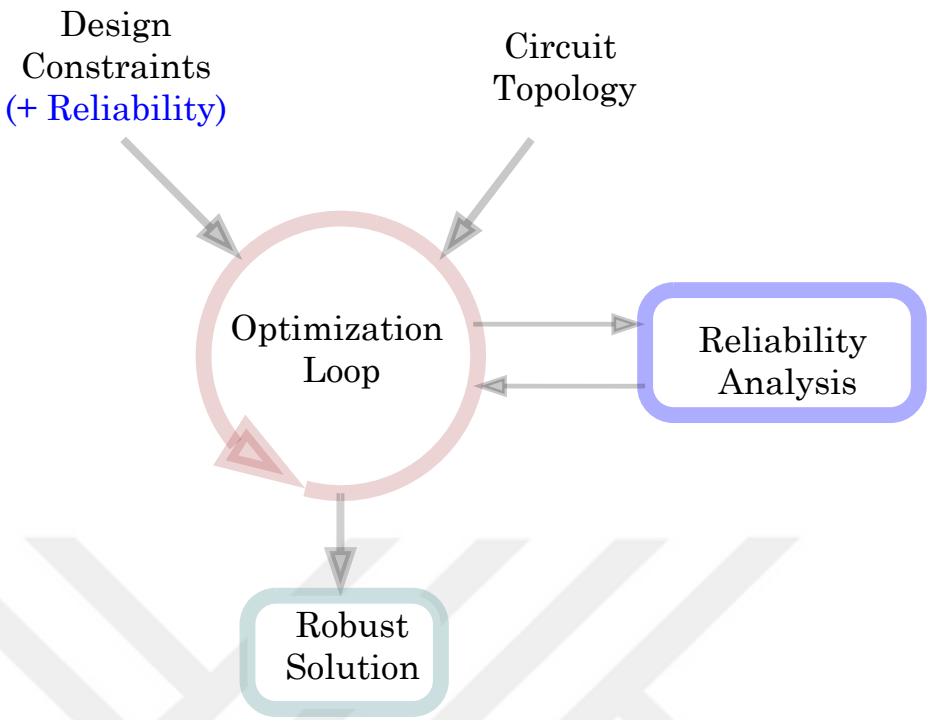

Figure 2.14. Reliaiblity aware circuit optimization.

tational effort may still be very high due to numerous iterations during optimization. Namely, performing yield analysis for each candidate is still expensive despite using an efficient yield analysis approach. Therefore, inclusion of the yield analysis into the optimization loop is another important problem.

On the other hand, lifetime-aware circuit synthesis has not been studied in the literature. Similar to the variation-aware circuit synthesis, a reliable and efficient aging analysis is required to develop an efficient tool. Conventionally, the accuracy of the aging analysis strongly depends on the model that is used. In addition to the model accuracy, aging analysis methodology also affects the accuracy. Performing aging analysis within a single step for the entire lifetime may result in severe prediction errors. Traditionally, the total simulation time is divided into sub-periods by a certain number of steps, and partial simulations are carried out. Hence, substantial changes in the stress amount on devices can be captured, and are taken into account during the calculation of parameter shifts for the next step. However, another problem arises dur-

ing the determination of the number of steps, where using a static step count results in a challenging trade-off between performance and accuracy. Namely, keeping the step size relatively small results in expensive simulation workload, whereas the use of larger steps may cause estimation errors. Consequently, reliability-aware circuit synthesis can be categorized into two subsets: variation-aware and lifetime-aware, which considerably enhance the total design time. However, integration of these two reliability problems with circuit sizing is not a trivial problem due to the very challenging trade-off problem between accuracy and efficiency.

Typically, there are two different circuit level reliability-aware circuit design approaches: Over-design and Robust-design approaches can be utilized for both of these reliability issues.

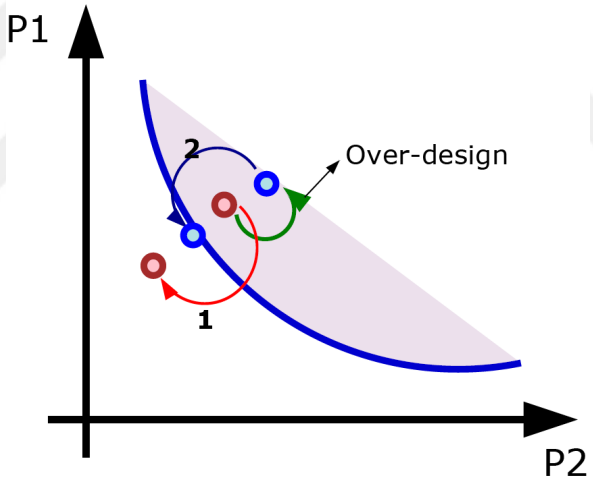

Figure 2.15. Over-design approach provides robustness by increasing the constraints.

Over-design approach is a possible solution to make a circuit more reliable, in which the design is guard-banded anticipating the worst case performance degradation. In other words, design specifications are satisfied with a large margin, thus, even if transistor parameters change, circuit performance can still be maintained to exist within the design specifications as depicted in Figure 2.15.

Over-design approach has two major drawbacks. The first one is that power consumption and chip area are sacrificed for the sake of reliability in this approach.

In conjunction with this problem, a second disadvantage arises due to the use of larger devices during overdesign, which restricts the use of this approach in some particular applications such as low-power and high frequency circuits.

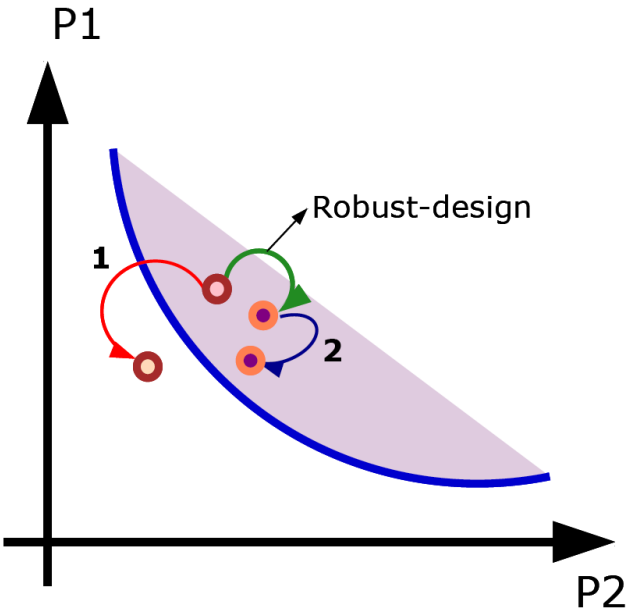

Figure 2.16. Robust-Design approach utilizes robust solutions in the solution space.

Robust-design approach is based on finding a robust design point in the design space. As a result of considering the reliability as a design constraint, the solution should satisfy not only electrical objectives, but also reliability. Although there is no guarantee to find the optimal solution in this method, it may possible to obtain more robust circuits by sacrificing a small amount from the electrical objectives. The disadvantage of this method is that searching for a satisfied solution for both electrical and reliability objectives would take longer time. Therefore, this method becomes efficient only by using automatic sizing algorithms that promises a wide scan of the whole solution space. Robust-design approach is depicted in Figure 2.16.

In addition to these circuit level design approaches, topology selection [71, 72], which is a system level solution, can also be utilized during the reliability-aware circuit design synthesis. Topology selection approach is demonstrated in Figure 2.17.

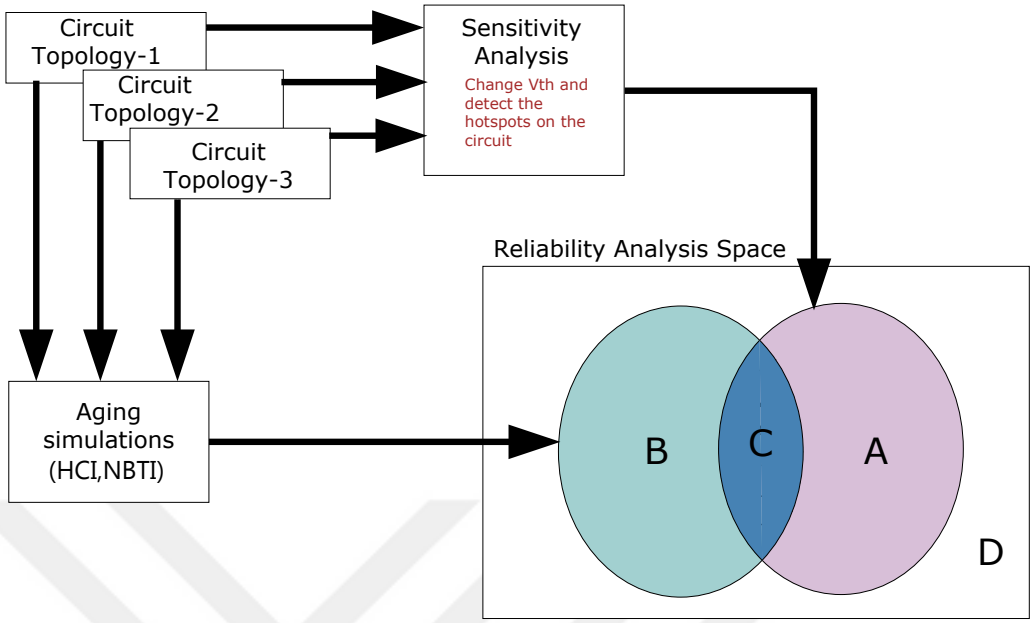

Figure 2.17. Topology selection approach.

As illustrated in the figure, sensitivity and aging analyses are performed for each circuit topology, which performs the same function, and a reliability space is constructed. In this space, solutions existing only in the D set are the most robust solutions in terms of reliability. Solutions existing only in the A set are sensitive to change in uncertain parameters, but are not affected by aging and the case is vice versa for B set solutions. At last, the intersection of sets A and B (set C) consists of solutions that are sensitive to parameter change and aging. According to the scenario, the first aim of the designer to use a topology existing in the D set. If any solution is found in the D set, which has a high probability, B and A solutions are preferred considering the variability problem, respectively. In the case of any solutions found in D or A or B (solutions only in C set), topology selection loses its validity due to all possible solutions suffer from aging and variability. Over-design and Robust-design approaches can be utilized in reliability-aware analog design automation systems. On the other hand, topology selection needs system level reliability information for each

circuit topology, so it is not applicable for design automation systems yet. However, this case will change with the developing of Analog Intellectual Property (IPs). An analog IP includes a number of different solutions for many circuit topologies with their electrical specifications. If the reliability information is obtained and stored in an analog IP, it would be possible to combine topology selection with design automation system.

2.5. Reconfigurable Analog Circuit Design Against Aging Phenomena

Lifetime-aware circuit optimization promises reliable solutions utilizing over-design and robust-design approaches. However, some design constraints, such as power and area, are sacrificed in that case. Therefore, it would not provide an appropriate solution for problems with hard design constraints. To overcome this bottleneck, reconfigurable circuit design approaches are commonly utilized. The idea behind reconfigurable circuit design is sensing the degradation and activating the healing mechanism to maintain the circuit performance despite aging effects. Hence, the circuit performance can be fully recovered as illustrated in Figure 2.18 with a properly designed reconfigurable system.

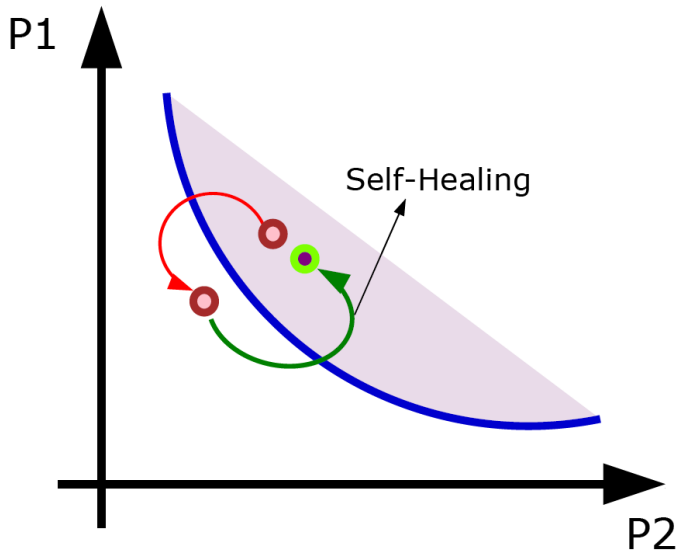

Figure 2.18. Sense and React approach can fully recover circuit performance.

A well-known reconfigurable design approach is called "Sense and React" as shown Figure 2.19. The first operation is called "Sense", in which a change in a certain circuit signature is detected via a sensor circuit [73]. In general, the type of the sensor depends on the application. Since it is expensive to measure the changes on circuit performances directly, indirect measurements are preferred, in which electrical quantities, such as node voltages, branch currents, and phase/frequency of a signal are measured, which are called signatures. These changes are then mapped to the circuit performance changes. However, determining efficient signatures is not trivial, and even quite complicated, since an efficient signature should have some properties such as applicability, measurability, and relevancy.

Traditionally, signature selection is performed by the designer in an iterative manner. However, performing this analysis manually is a highly inefficient and time consuming process.

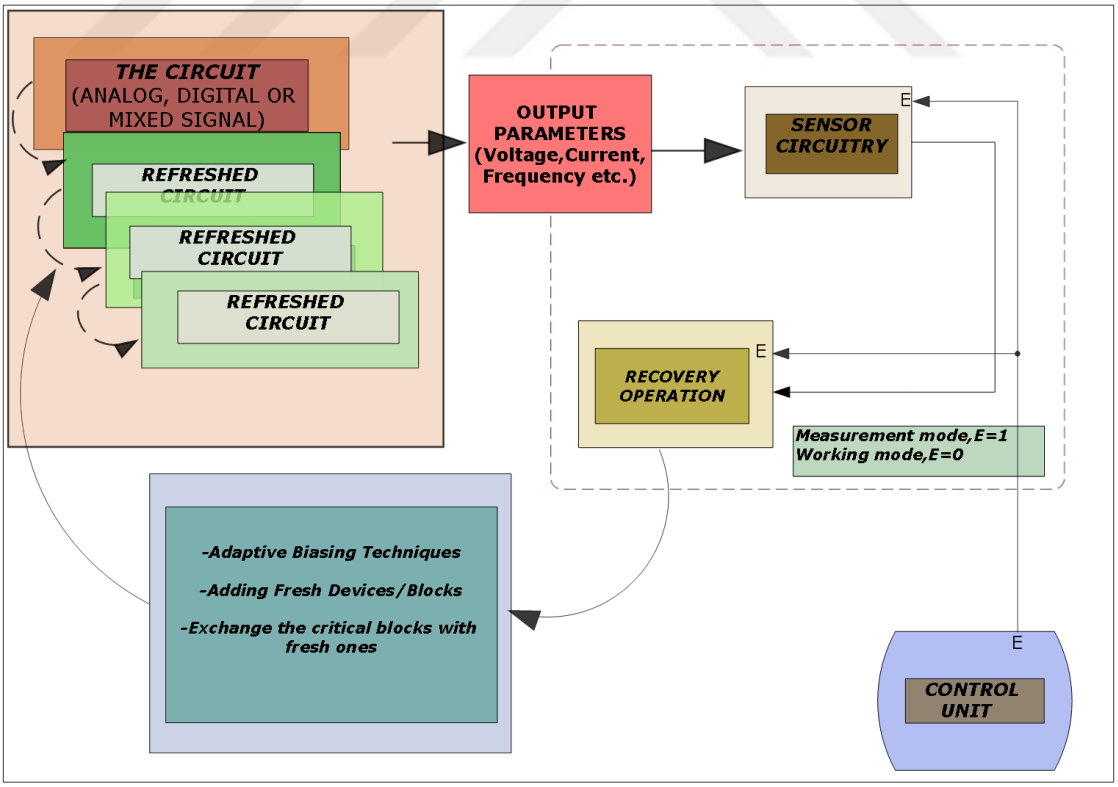

Figure 2.19. A general scheme for Sense and React approch.

While voltage and phase/frequency quantities are detected directly, a sampling circuit is required to sense the change in the current. Typically, current mirrors are used to sample the current flowing in a branch. However, the design of a current sampling circuit is highly critical since the aging of the mirroring transistor causes inaccurate sampling, which disrupts the whole recovery mechanism. Therefore, current detection is not preferred as a sensing method. Another parameter that can be detected is the threshold voltage. The threshold voltage monitoring approaches for a single device [74–76] are intended to test and measure the aging for each technology node, but can not provide recovery. There are several studies on monitoring and healing for a single device. However, recovery operations are quite problematic in complicated circuits and it is not possible to sense changes in all devices and heal all of them. Therefore, system/block based solutions should be developed to deal with aging phenomena in integrated circuits.

There are three different recovery operations for the "React" part of the approach, which are;

- Adaptive biasing
- Adding supplementary transistors/blocks
- Replacing aged transistors/blocks with fresh ones

In "Adaptive Biasing" approach, the activation signal generated by the sensor circuit is converted to some pre-determined voltages and applied to the hot spots to compensate for the aging effects. Thus, the current provided by the aged transistors is recovered. However, this approach is quite difficult and expensive since both evaluation and conversion of change in circuit output to bias voltages are highly challenging problems and need additional circuits. In addition to its difficulty, a further problem arises due to the nature of aging for adaptive biasing approach, where the stress on the device is increased with recovery of the degradation in the current, which may accelerate the aging process for long term operations [77]. In the second approach, some supplementary devices are placed in the chip during the design process, which are not active at the beginning and activated by the control signals generated via sensor

circuitry. This approach is highly advantageous for circuits that age rapidly such that even small degradations can be sensed and recovered in shorter time periods by high resolution circuits in terms of change of output parameters. However, adding extra devices may cause some performance deterioration in some particular applications such as increase in the device noise for RF applications. Furthermore, an additional analysis and circuitry are required to manage the recovery operation. In the last approach, rather than adding supplementary devices, aged transistors/blocks are replaced with fresh ones; thus, a full recovery is realized. This approach does not suffer from any performance degradation. However, in general, the replacement operation can only be performed for a limited number of times due to the area occupation of fresh devices on the chip.

A sense and react system can be designed in two different manners: continuous time and discrete time. The continuous time approach provides immediate response capability and recovery. This is important especially for devices exposed to unexpected extreme environmental conditions (aerospace applications, etc). However, such a continuous time evaluation brings additional power consumption since all the supplementary circuits will always be active as well as the actual circuit. On the other hand, the discrete time approach requires an external enable signal to activate the sense and recovery blocks and has a delayed response to instantaneous changes. Since circuits are active only for a short duration, there would be almost no extra power consumption in this case.

In the light of this fundamental background, contributions of this thesis will be explained and discussed in the following chapters.

3. ANALOG/RF CIRCUIT OPTIMIZATION TOOL

Both variation- and aging-aware analog circuit synthesis approaches require an optimization engine. In this thesis, a SPICE-based analog circuit synthesis tool is utilized, which is a modified version of the tool proposed in [5]. Moreover, a novel RF analog circuit synthesis tool is also proposed in this thesis, where a mixed domain circuit sizing is utilized by considering layout-induced parasitics. The chapter is organized as follows. In Section 3.1, Section 3.2, and Section 3.3, the analog synthesis tool is explained, implementation of the tool is explained in detail, and synthesis results are provided for an example design problem, respectively. In Section 3.4, the proposed mixed-domain RF circuit synthesis tool is presented and demonstrated via two synthesis examples. This chapter is concluded by providing general remarks in Section 3.5.

3.1. A SPICE-based Analog Circuit Synthesis Tool

A single objective simulation-based analog sizing tool is utilized in this thesis, where evolutionary strategies (ES) and simulated annealing (SA) algorithms are used in the search and selection parts, respectively. The main algorithm of the optimizer is proposed in [5]. Optimization is based on the minimization of a function, which is defined as *cost*. In Figure 3.1, the pseudo-code of the optimizer is listed. Optimization starts with an initialization process. The initialization is followed by cross-over and mutation operators. Then, all individuals are separately evaluated via SPICE simulations and cost calculation is performed. Finally, a selection process takes place to determine the surviving individuals for the next generation and this loop continues until either the maximum iteration number or the convergence is achieved.

3.1.1. Search Algorithm

A $(\mu+\lambda)$ ES algorithm is utilized in this thesis, where μ and λ denote the number of the individuals of the parent and offspring, respectively. Each individual's chromo-

begin

% Initialization

g $\Leftarrow$ 0

$P_\mu \Leftarrow P_{\mu 0}$

while convergence **or** maximum iteration **not** reached **do**

% Cross−over

for i= 1 **to** $\lambda/2$ **do**

$[I_{parent1}, I_{parent2}] \Leftarrow choose(P_\mu, 2)$

$[I_{\mu+i}, I_{\mu+i+1}]_x \Leftarrow recombine_x(I_{parent1}, I_{parent2})$

$[I_{\mu+i}, I_{\mu+i+1}]_s \Leftarrow recombine_s(I_{parent1}, I_{parent2})$

end

% Mutation

for i= 1 **to** $\mu + \lambda$ *do*

if I_i is selected **for** mutation

$I_{i_x} \Leftarrow mutate_x(I_i)$

$I_{i_s} \Leftarrow mutate_s(I_i)$

end

$I_{icost} \Leftarrow evaluate(I_i)$

end

% Selection

$P_\mu^{g+1} \Leftarrow select(P_{\mu+\lambda}^g, \mu, T)$

$g \Leftarrow g + 1$

$T \Leftarrow update\ temperature()$

end

output $\Leftarrow$ *best solution*

end

Figure 3.1. Pseudo code of the optimization algorithm.

some has two major genes: circuit variable gene X (transistor widths, lengths, resistor, capacitor, inductor, biasing current and voltage values) and strategy parameter gene S (cross-over coefficient and mutation step-size), which are given as

$$I = [X, S] \tag{3.1}$$

where X and S are

$$\begin{aligned} X &= \{W_i, L_i, V_j, I_k, C_m, l_n, R_q\} \\ S &= \{a_{i=1...\mu} + \lambda_{i=1...\mu}, \sigma_{i=1...\mu} + \lambda_{i=1...\mu}\} \end{aligned} \tag{3.2}$$

W_i and L_i denote transistor widths and transistor lengths, V_j and I_k denote biasing voltages and currents, C_m denotes capacitors, l_n denotes inductors, and R_q denotes resistors. Considering the strategy gene, a_i denotes cross-over coefficient and σ_i denotes mutation step-size for each individual.

3.1.2. Initialization

The initialization process is composed of generating μ individuals with search variables generated according to the variable ranges given by the user. Contrary to [5], which utilizes a random initialization process, a quasi-random initialization was preferred in order to homogeneously distribute the design parameters over the search space. Homogeneous distribution of the initial population is highly important, where diversity of the design parameters over the design space enhances the evolution. Therefore, a Low Discrepancy Sequence (LDS) is assigned in order to sample the design space homogeneously. In Figure 3.2, the distributions of 1000 conventionally generated random numbers and 1000 quasi-random numbers on a 2D space are visually illustrated, where it is clearly seen that quasi-random numbers have a highly uniform distribution while the conventional random numbers are more prone to clusters or vacancies. A further discussion on initialization with quasi-random numbers can be found in [78].

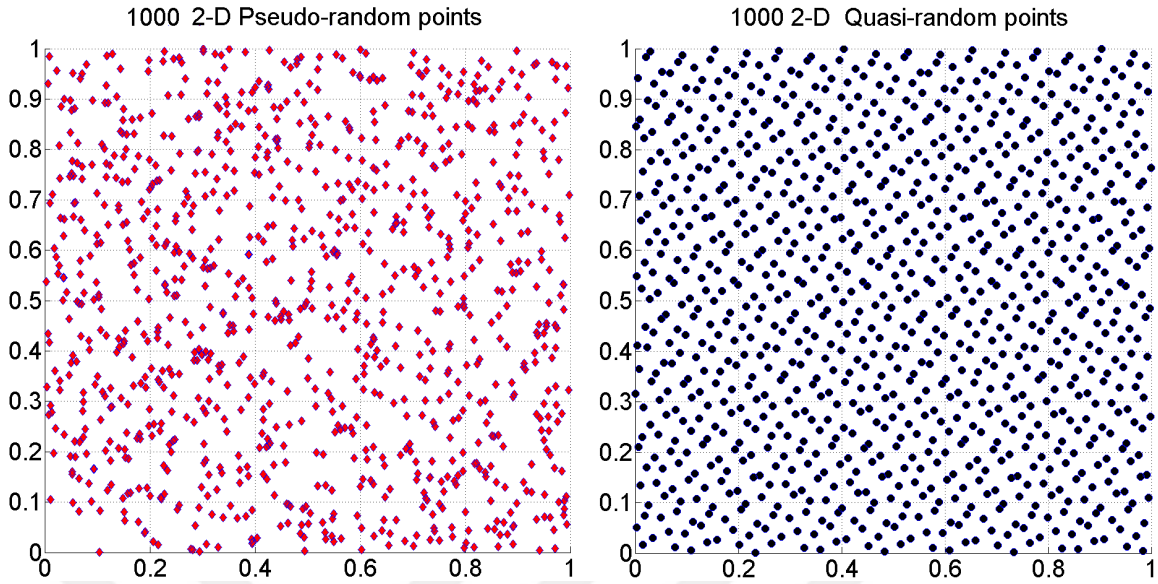

Figure 3.2. 2-D projections for pseudo-random and quasi-random numbers.

3.1.3. Recombination: Cross-Over

In recombination, two parents are randomly chosen and two offspring are formed by crossing over their strategy parameters (s) and search variables (x) using the recombination coefficient a as

$$\begin{aligned} S_{child1} &= aS_{parent1} + (1-a)S_{parent2} \\ S_{child2} &= aS_{parent2} + (1-a)S_{parent1} \\ X_{child1} &= aX_{parent1} + (1-a)X_{parent2} \\ X_{child2} &= aX_{parent2} + (1-a)X_{parent1} \end{aligned} \tag{3.3}$$

This type of crossover is called arithmetic crossover. The recombination coefficient, a is in the range [0, 1]. The two offspring would be identical and have averaged variable values when $a = 0.5$. However, averaging may not be logical since it damages the diversity of the population. In [5], it was observed that using a between $0.7-0.9$ is a better choice for the cross-over operations. In addition to that, an upper-lower limit

is applied during the cross-over operation to prevent any violation on search variables limits given by the user.

3.1.4. Mutation

In the mutation procedure, each individual I_i has its own standard deviation for each search variable set $x_{i,j}$ and recombination coefficient a_i. During mutation, if an individual I_i, is selected for mutation, these standard deviations are initially updated according to:

$$\begin{aligned} \sigma^{'}_{x_{i,j}} &= \sigma_{x_{i,j}} e^{(\tau_0 N(0,1) + \tau N_i(0,1))} \\ \sigma^{'}_{a_i} &= \sigma_{a_i} e^{(\tau_0 N(0,1) + \tau N_i(0,1))} \end{aligned} \tag{3.4}$$

where $N(0,1)$ is a normally distributed random variable with expectation zero and standard deviation one, and $N_i(0,1)$ is a normally distributed variable that is sampled for each search variable. The recommended values for the parameters τ_0 and τ are

$$\tau_0 = \frac{1}{\sqrt{2n}},\ \tau = \frac{1}{\sqrt{2\sqrt{n}}} \tag{3.5}$$

where n is the dimension of the search space. After updating the standard deviations, search variables $x_{i,j}$ and recombination coefficients a_i are updated according to

$$\begin{aligned} x_{i,j} &= x_{i,j} + \sigma^{'}_{x_{i,j}} N_i(0,1) \\ a_i &= \sigma_{a_i} + \sigma^{'}_{a_i} N_i(0,1) \end{aligned} \tag{3.6}$$

3.1.5. Cost Calculation

The cost function combines circuit performances, evaluates them, and transforms them into a single minimization function. There are two different components of the cost function, where the first one is a performance related cost(C_{perf}), while the other

is a biasing related cost(C_{pen}). The performance related cost is the weighted sum of squared normalized distances from the target point and calculated as

$$C_{perf} = \sum_{i=1}^{n} w_i \hat{f}_i^{\,2}$$
$$\hat{f}_i = \frac{U_i - f_i}{f_i - L_i} \qquad \hat{f_{i,min}} = 0 \tag{3.7}$$

where n is the number of performance specifications and the normalized values $\hat{f}_i$ are calculated by using upper limits U_i, and lower limits L_i given by the user. The minimum value of these normalized cost values is kept as 0 to allow over-satisfying of performance constraints. In addition to the performance specifications, biasing constraints should be included in the cost. In analog circuits, MOSFETs are usually biased in the saturation region except the ones that are used as resistors. Therefore, a penalty term is included to the cost function to keep all transistors in the saturation region, which is calculated as

$$C_{pen} = W_{pen} \left(\sum_{j=1}^{m} p_{cut-off_j} + \sum_{i=1}^{n} p_{triode_i} \right) \tag{3.8}$$

Finally, the cost of an individual is calculated as

$$C = C_{pen} + C_{perf} \tag{3.9}$$

3.1.6. Selection

A selection process takes place after the cost calculation, where μ individuals, which will be parents of the next generation, are selected among $\mu+\lambda$ individuals. The major drawback of ES-based search algorithms is that they are highly prone to getting stuck at local minima. Therefore, selection mechanism is very critical to overcome this problem. A Metropolis criterion and simulated annealing based selection process was proposed in [79]. Some other versions can be found in [80, 81]. Metropolis criterion is based on a competition between the current solution I_i and a challenger solution I_j,

where the win probability of I_i is given as

$$p(I_i) = \frac{1}{e^{(C_i - C_j)/T}} \tag{3.10}$$

where C_i and C_j are the cost values and T is the temperature, which will be explained in the next section. Rather than such a competition between two candidates, in [5], a different type of Metropolis criterion was used. Namely, a randomly selected individual of I_i competes with a pseudo-individual having the average cost C_{av} and wins with the probability of

$$p(I_i) = \frac{1}{e^{(C_i - C_{av})/T}} \tag{3.11}$$

This process is repeated until μ individuals win against the average cost. The presence of very low performance (high cost) individuals increases the average cost and increases the probability to close to unity, which lead to random selection of individuals even at low temperatures. Therefore, an elitist nature should be included to prevent this random selection and provide a deep focus when the population was matured. In [5], an individual I_i is neglected if $C_i > kC_{min}$, where C_{min} is the minimum cost in the current population and k is a constant determining the neglecting threshold. It was reported that lower values of k tend to increase the elitist nature of selection and cause premature convergence while higher values of k are ineffective. However, this approach is quite problematic due to the high dependence on the value of k. Therefore, in this study, the elitist part of the selection process was modified, by directly selecting best individuals with a ratio of 10% of the whole population. Thus, the average cost value can be kept at a reasonable value; thus, the probability of I_i is sufficiently far from the unity.

The other important property of the utilized Metropolis criterion is the population temperature, which provides an adaptive probability adjustment through evolution. At higher temperatures at the beginning of the evolution, the probability of

selecting a low performing (high cost) individual is high and this provides population diversity. Furthermore, this behavior gives a chance to the offspring that may survive despite having low performing parents, especially considering the non-linear behavior of analog circuits. On the other hand, as the temperature is lowered, the probability of the selection of the low performing individuals also decreases; thus, the population focuses on a certain region of the search space and fine-tunes the variables, providing a a local search around the supposed global optimum.

3.1.7. Simulated Annealing: Population Temperature

Simulated annealing process is controlled by the population temperature, which has a number of parameters, such as initial (T_0) and final (T_{final}) temperatures, population cooling rate (α), and Markov chain length (T_{repeat}). Actually, the determination of the initial and final temperatures is somehow heuristic, which were discussed in detail in [5]. In the utilized tool, the final and initial temperature values were selected 1 and 1000, respectively.

The proposed cooling process is the exponential cooling schemes in [82,83], which are commonly preferred to obtain a finite time to finish cooling. The utilized synthesis tool uses a similar approach with a limited Markov. The temperature of the next generation (T_{k+1}) is determined according to:

$$T_{k+1} = \alpha T_k \tag{3.12}$$

Ultimately, the total number of generations can be calculated using

$$N_g = \left[\frac{\left(log\left(\frac{T_0}{T_f}\right)\right)\left(log\left(\frac{T_0}{T_f}\right)+1\right)}{2} \right] \left[\frac{\left(log\left(\frac{T_f}{T_0}\right)\right)}{log(\alpha)} \right] \tag{3.13}$$

where the value in left brackets is the average number of generations before temperature is updated, while the right one is the number of temperature updates.

Cooling rate (α) can be calculated by defining the number of generations (N_g). Actually, the selection of the simulated annealing coefficient varies with respect to the problem to be optimized. After the determination of the T_0, T_f, and N_g, the cooling rate of the population is calculated using Equation 3.13. Furthermore, the calculated T_f is not used as a strict stopping criterion and evolution is continued until either the convergence or maximum number of generations is reached. The default values for T_0, T_f, α, and N_g are 1000, 1, 0.98, and 200, respectively.

3.2. Implementation of the Analog Circuit Synthesis Tool

The optimizer tool was developed on the MATLAB® platform, where HSPICE was utilized for performance estimation. MATLAB® was preferred due to its ease of use, flexibility, and presence of many useful functions and libraries. These available functions and libraries make easy to integrate yield and lifetime analyses with the developed tool. On the other hand, MATLAB® exhibits a slower computational performance than the other languages (Python, C, etc.). However, this performance loss is negligible compared to the expensive SPICE simulations included.

A simplified flow chart of the tool is given in Figure 3.3. Design variables, design constraints, and search algorithm variables are determined by the user. Then, initialization, recombination, and mutation take place, respectively. To evaluate the performance of each individual, design variables are written to the parameter list and HSPICE is called. After performance evaluation, performance values are read and a particular cost value is calculated and assigned to each individual. Selection is applied to the current population to determine the surviving individuals. This loop is continued until either the convergence or maximum iteration number is reached.

3.3. Synthesis Example and Results

To evaluate the developed tool, a two stage operational transconductance amplifier depicted in Figure 3.4 was synthesized using the tool. Open loop gain, 3dB bandwidth, output resistance, power consumption, and chip area were determined

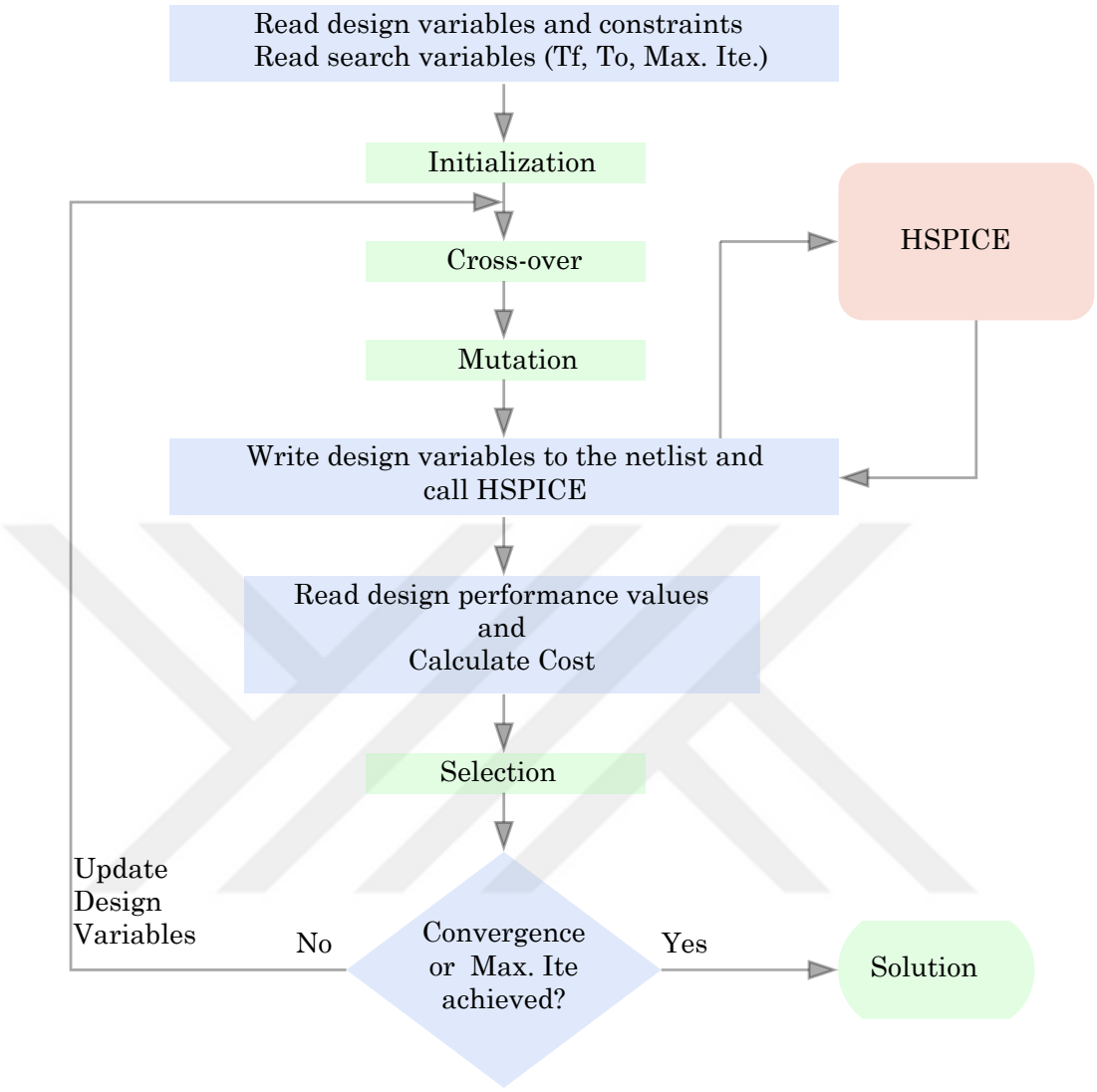

Figure 3.3. A simplified flow chart for the optimizer.

as design constraints. The values for T_0, T_f, α, and N_g are 1000, 1, 0.98, and 100, respectively.

The behavior of the average cost function through the generations is given in Figure 3.5. As expected, the average cost decreases as the population evolves. In addition to the cost value, average values of 3dB bandwidth, gain, and area are given in Figure 3.6. As seen from the results, gain and bandwidth are being maximized whereas area are being minimized during optimization process.

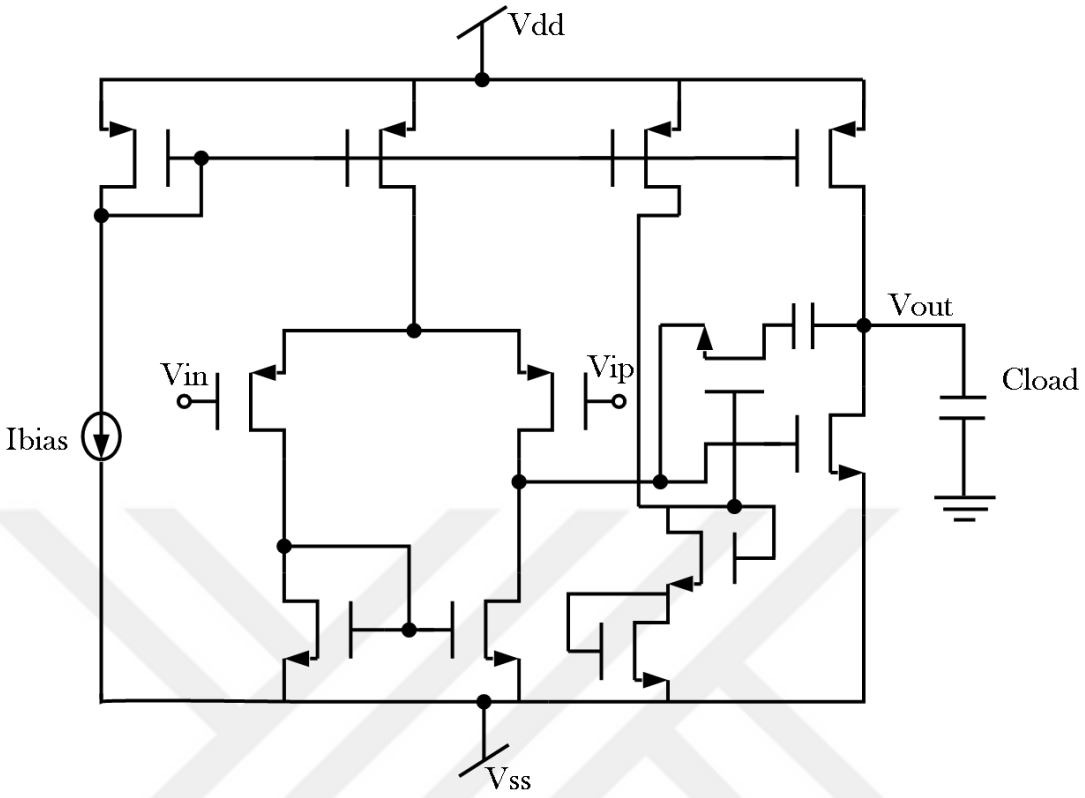

Figure 3.4. Schematic of the two stage OTA.

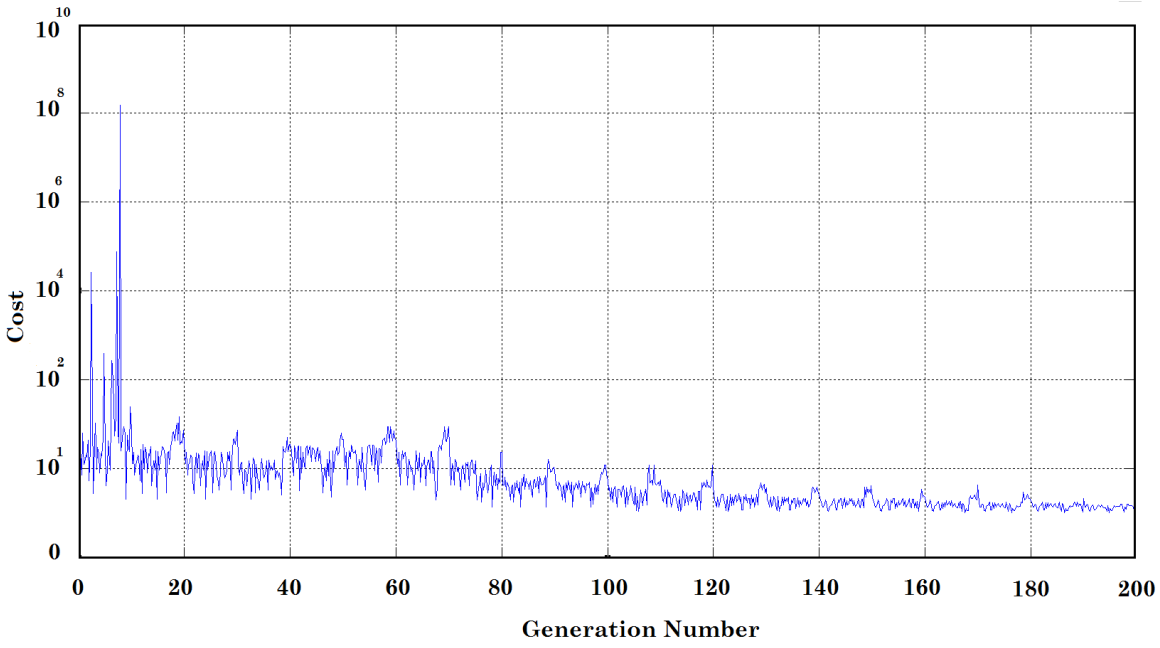

Figure 3.5. Cost behavior through generations.

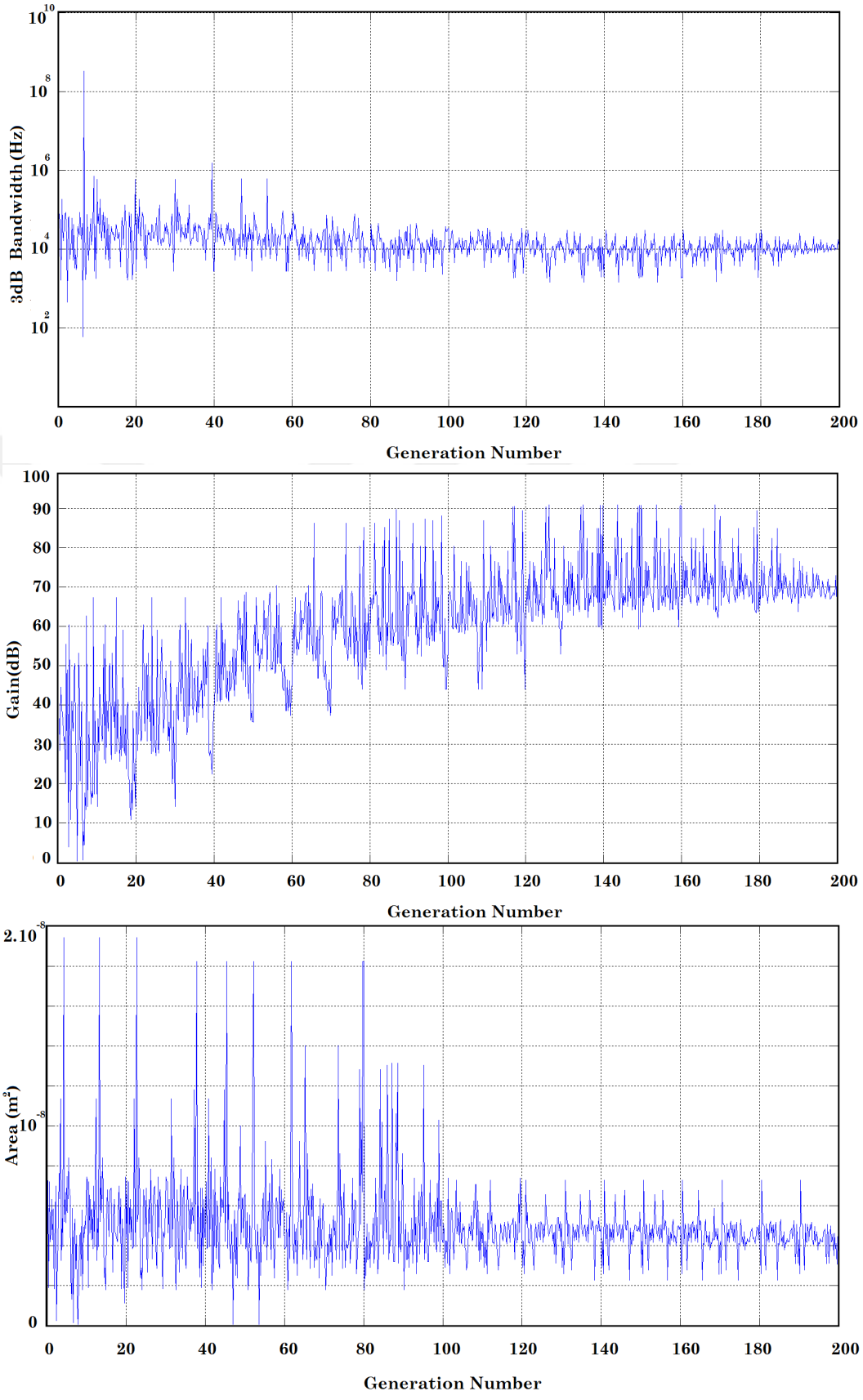

Figure 3.6. Design constraint evolutions through generations.

Table 3.1. Synthesis Results of 5 independent runs for Two Stage OTA.

	Bandwidth $[> 10kHz]$	Gain $[> 70dB]$	Phase Margin $[> 60^o]$	Power $[< 0.5mW]$	Area $[< 2000\mu m^2]$	Synthesis Time $[min]$
1	10.4	74.5	64	0.48	1780	21.2
2	10.3	70.7	63	0.36	1840	21.1
3	11.9	70.1	68	0.40	1280	21.3
4	12.3	71.5	66	0.38	1720	20.8
5	13.4	70.1	61	0.46	1360	21.1

Synthesis results of 5 independent runs for the OTA circuit are provided in Table 3.1. The average synthesis time was found to be around 21 minutes, where an Intel i7 chipset with 2.80GHz processor was utilized during the synthesis. All design constraints were satisfied for all runs. To validate synthesis results, ac and transient simulation results for the first solution are also provided in Figure 3.7 and Figure 3.8.

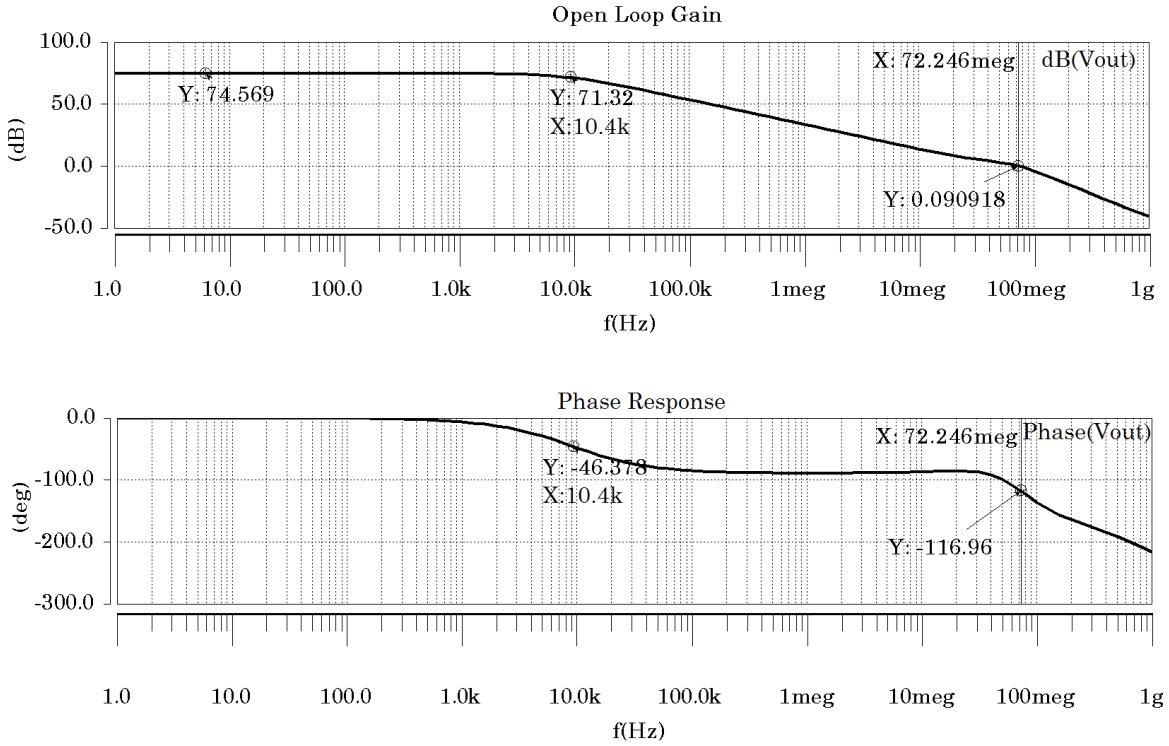

Figure 3.7. Frequency domain simulation results.

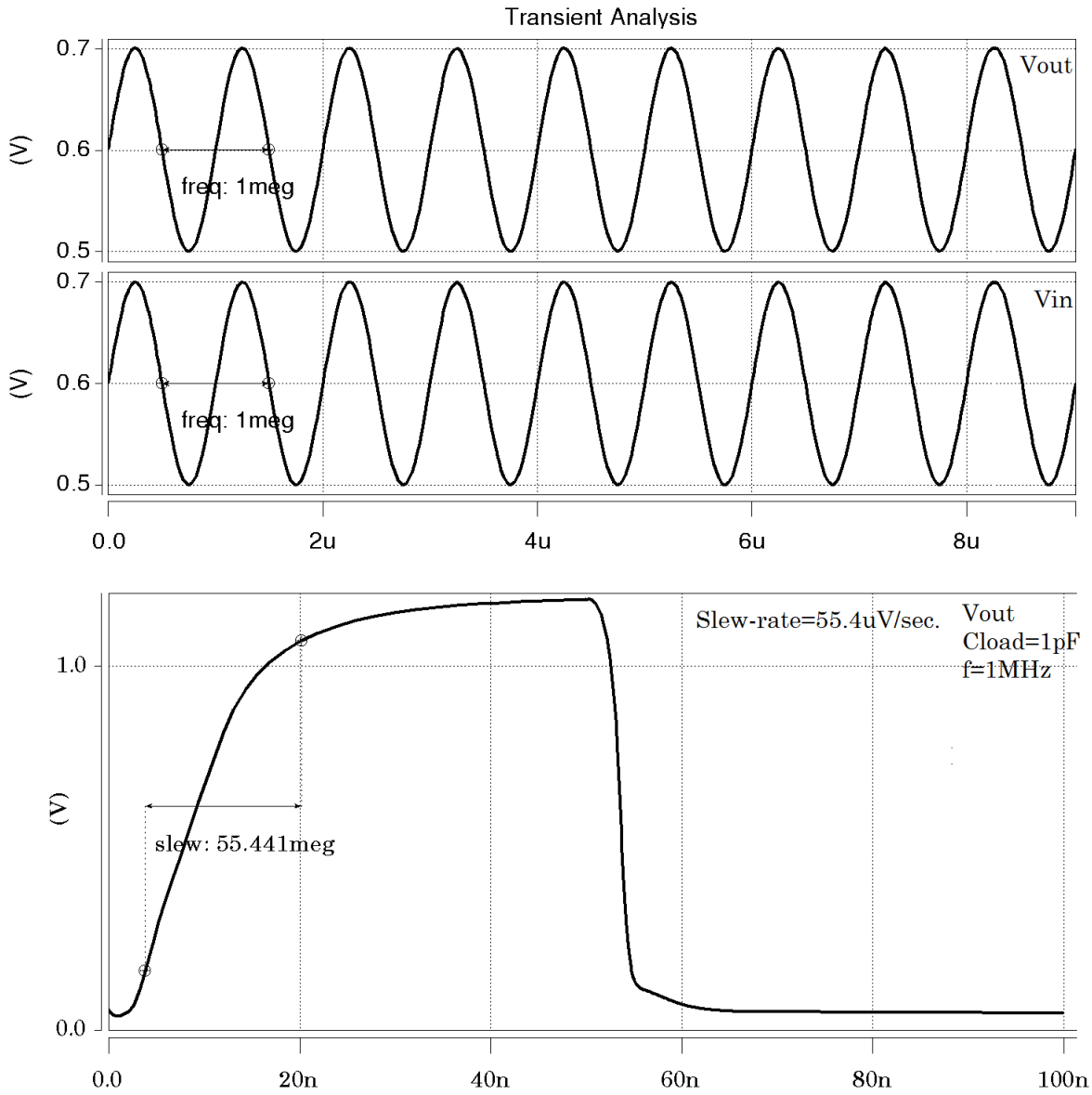

Figure 3.8. Time domain simulation results.

3.4. Mixed-domain Analog Circuit Synthesis

RF circuit synthesis is relatively difficult compared to the analog synthesis process since severe layout-induced parasitics of passive devices lead to a discrepancy between the synthesis results and post-layout results when only electrical parameters are considered as design parameters. In this section, a mixed-domain synthesis approach is introduced, where physical, rather than electrical, parameters of passive devices

are searched. Thus, more reliable synthesis results can be achieved and the iteration count between the synthesis and layout processes can be substantially decreased. The section starts with a brief background on RF circuit synthesis. Then, the proposed tool is presented in the second sub-section. To demonstrate the mixed-domain RF circuit synthesis, results of two different RF circuits are provided and discussed and the section is concluded in the last sub-section.

3.4.1. Background

Radio frequency (RF) circuit design has become a very challenging process due to increased non-idealities and secondary effects through rapidly developing CMOS technology. Several automatic sizing tools [84,85] for RF analog circuit synthesis have been proposed to keep the design time within acceptable limits and reduce the time to market. However, automatic sizing of RF CMOS circuits is not sufficient to guarantee a certain performance, where the behavior of analog RF circuits is extremely sensitive to the layout design due to relatively larger layout-induced parasitics [86]. Therefore, layout-generation has also been automated to take into account the effect of layout-induced parasitics efficiently. Thus, the design loop has been completely automated with the integration of sizing and layout tools as illustrated in Figure 3.9. In [87], it has been shown that a few additional layout iterations can be sufficient to achieve a solution that still satisfies the performance constraints after layout process. However, the case for RF circuits is quite different since the inclusion of layout-induced parasitics of passive devices (inductor and capacitor) causes severe performance degradation, necessitating a large number of iterations between circuit sizing and layout generation.

Another way to synthesize RF circuits is embedding the layout generation tool into the circuit sizing engine, where the design space exploration is carried out considering layout-induced effects. Optimization based layout generation yields impractically long synthesis times when it is in the circuit optimization loop, whereas template-based instantiation limits the design flexibility, affecting circuit performance severely in many cases. One possible solution is to use equivalent parasitic models for passive devices at the sizing level, which may provide a considerable speed and quality enhancement.

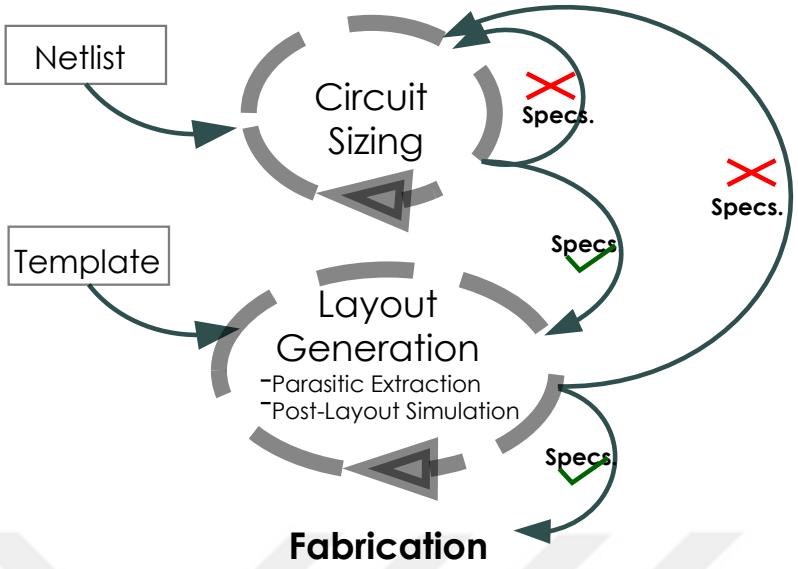

Figure 3.9. Analog circuit design loop.

In the literature, "$1-\pi$" model given in [88] has been commonly used for inductors on insulating substrates; the case for conductive substrates is quite problematic [89]. To palliate this problem, "$2-\pi$" models have developed [90], which is utilized by numerous commercial design tools. These models utilize a higher order equivalent sub-circuit in order to make the analysis more realistic. Furthermore, there are also capacitor equivalent models provided in such commercial tools.

3.4.2. Physical-based Equivalent Models

Most RF circuit sizing tools utilize ideal devices or simplified compact models during RF circuit synthesis, where electrical values of such devices (inductance and capacitance) are chosen as design parameters, and used for estimation of layout-induced parasitics. However, such estimations mostly generate optimistic results since passive device parasitics, which are the dominant source of layout-induced parasitics, are under-estimated. In order to obtain more realistic results at the sizing level, physical-based parasitic models that successfully cover layout parasitics were used in the developed tool. In Figure 3.10, the layout and the equivalent circuit of a the metal-insulator-metal capacitor are given. Geometry parameters of the capacitor are

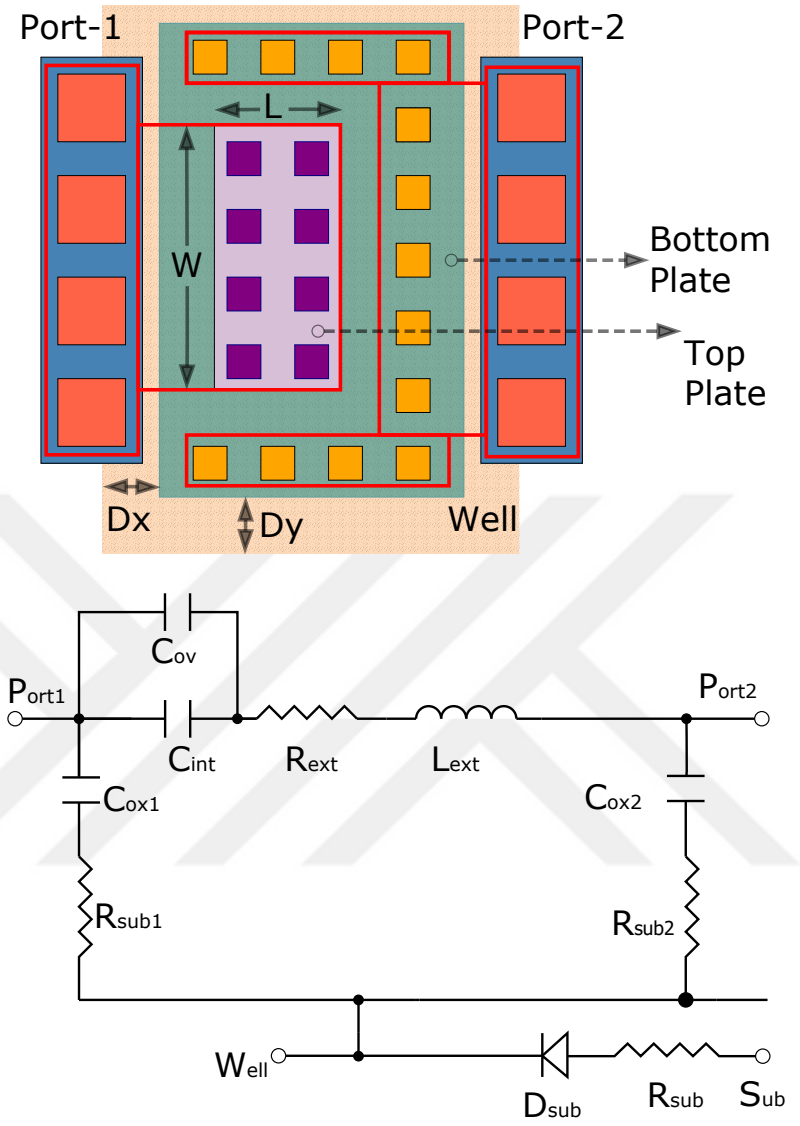

Figure 3.10. Layout and equivalent model for metal-insulator-metal capacitor.

metal width (W), length (L), and well spacings (D_x and D_y). Values of the equivalent sub-circuit are calculated according to these variables, where C_{ov}, C_{int}, C_{ox} are the overlap, intrinsic, and oxide capacitances, respectively. R_{ext} and L_{ext}, R_{sub}, and D_{sub} are parasitic resistors and inductors residing in the metal, the substrate resistances, and the diode between the well and the substrate. Most of the layout-induced parasitics are covered via this model, where values are automatically calculated utilizing user defined variables such as metal type, width, and length.

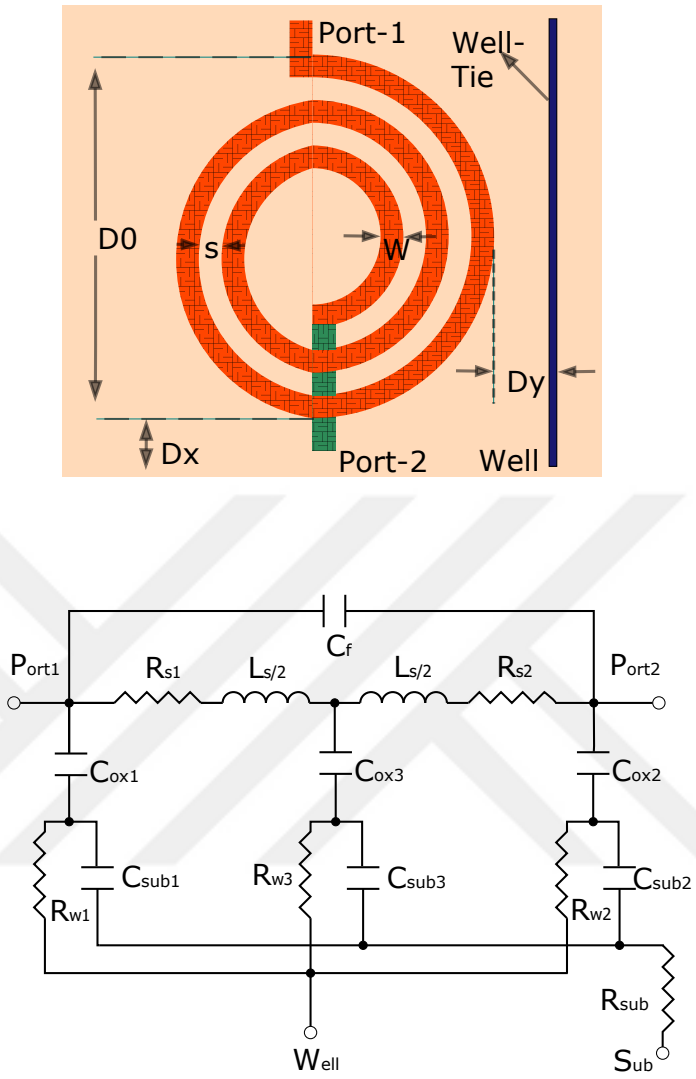

Figure 3.11. Layout and equivalent model ("$2-\pi$") for planar inductor.

On the other hand, layout of the utilized planar RF inductor and its circuit model are given in Figure 3.11. Due to the inductor geometry, a complicated model ("$2-\pi$") is used to estimate the behavior of the inductor after the layout process. W, D_O, s, and $D_{x,y}$ denote metal width, metal spacing, outer diameter, and well spacing respectively. There are 12 elements in the sub-circuit model consisting of parasitic capacitors and resistors, where the major design parameters are number of turns (N_t), outer diameter (D_O), and metal width (W_{ind}).

3.4.3. Mixed-domain RF Circuit Synthesis Tool

A flow chart of the developed RF tool is given in Figure 3.12. The main algorithm was developed on MATLAB®, which runs HSPICE-RF for performance evaluation. Passive device parasitic models are defined as sub-circuits at the top level, and automatically included into the circuit; thus, physical parameters can be directly converted to electrical equivalents for electrical domain simulations.

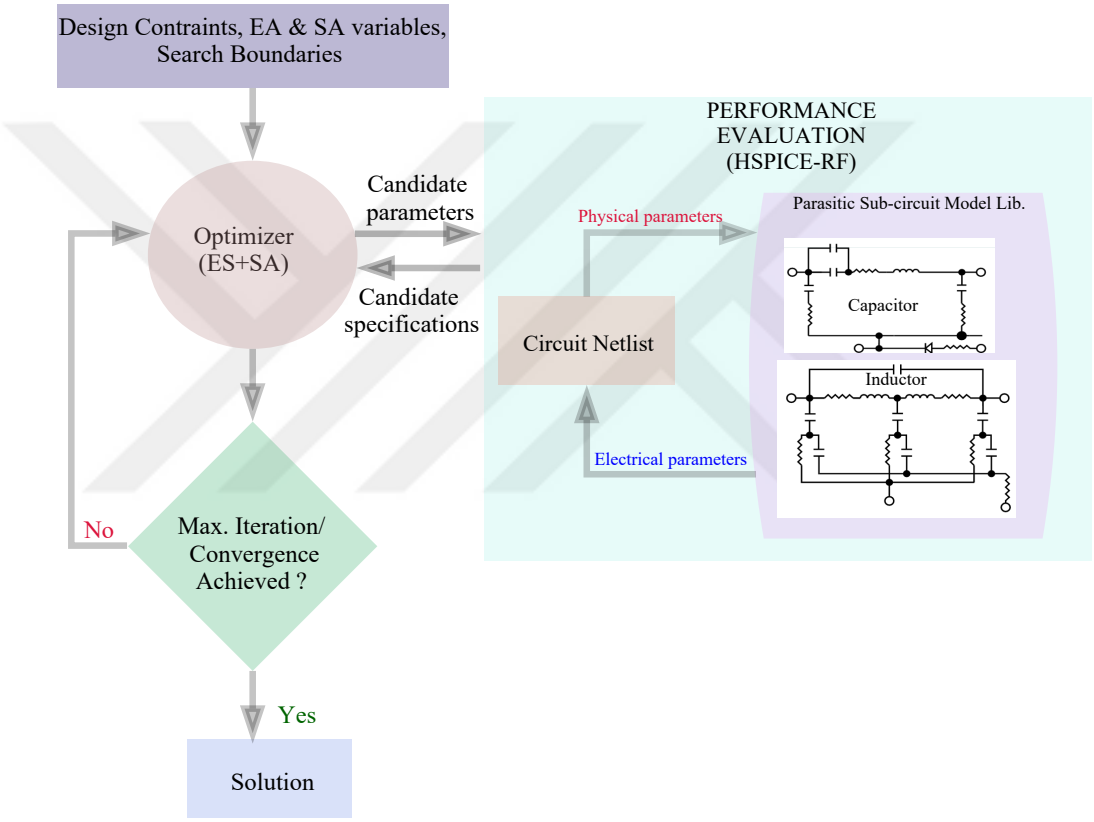

Figure 3.12. RF circuit synthesis flow.

3.4.4. Synthesis Examples

To demonstrate the proposed approach, two RF circuits, a single ended low noise amplifier (SLNA) and a CMOS differential cross-coupled oscillator were chosen as synthesis examples. An Intel $i7$ 4th generation chipset with 3.20 GHz processor was utilized during the synthesis process. $130nm$ CMOS technology models are utilized during the synthesis of both circuits. Numbers of parents, offspring, and maximum

number of iterations were chosen as 50, 50, and 200, respectively. Simulated annealing variables were kept at the default values ($T_f = 1$ and $T_0 = 1000$).

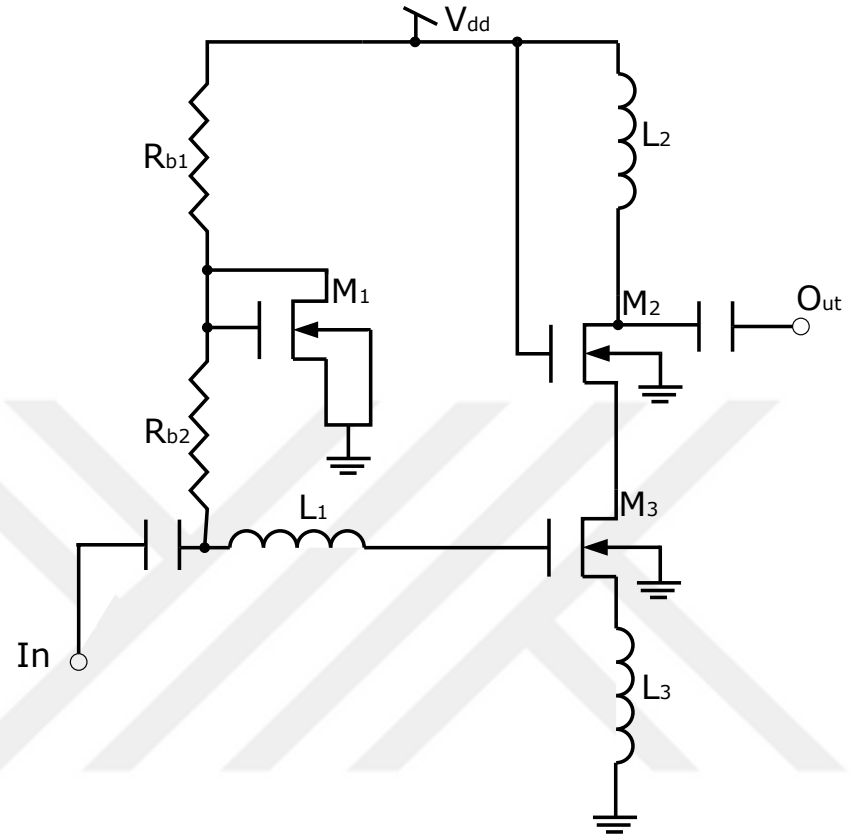

Figure 3.13. Schematic of the single ended low noise amplifier.

The schematic for the SLNA circuit is given in Figure 3.13. The operating frequency of the circuit was determined to be 2.4 GHz, where all circuit variables were chosen as design exploration parameters as given in Table 3.2. During the evaluation process, the sub-circuit given in Figure 3.11 was used for all inductors. Therefore, in addition to the electrical parameters (transistor dimensions, resistors, etc.), major design parameters of the planar inductor; namely, number of turns, metal width, and outer diameter are also optimized. Upper and lower limits for these physical properties are determined according to the data provided by the foundry.

Design constraints (S-parameters, noise figure (NF), and third order intercept point (IIP3) and synthesis results for 3 independent SLNA runs are given in Table 3.3. According to the results, all constraints have been satisfied and the average synthesis

Table 3.2. Design boundaries and variables for the SLNA.

	W $[\mu m]$	L $[\mu m]$	R_{bias} $[\Omega]$	N_t [ ]	W_{ind} $[\mu m]$	D_o $[\mu m]$	s $[\mu m]$
Minimum	24	0.12	1000	2.5	2	75	1.5
Maximum	480	1	10000	7.5	10	150	—

time is around 1.3 hours for SLNA example. This is because of the expensive harmonic balance analysis that is performed to measure IIP3. Furthermore, simulation results of a nominal synthesis, where ideal values of passive components were used as search parameters, are given in the fourth column in Table 3.3.

Table 3.3. Synthesis results for the SLNA.

Constraint	Run 1	Run 2	Run 3	Nominal Run	Implementation
$S_{11} < -15$(dB)	-14.9	-15.3	-15.7	-18	-13
$S_{12} < -30$(dB)	-36.2	-37.8	-37.6	-42	-37
$S_{21} > 10$(dB)	11.7	12.4	10.9	14.1	10.3
NF < 3	1.1	1.3	1.2	0.9	1.3
IIP3(dBm)	3.6	4.2	5.4	6.4	6.3
Synthesis Time(h)	1.36	1.28	1.34	0.6	—

To illustrate the superiority of the proposed approach, this ideal solution was implemented by using real components and the best results are given in the fifth column. As seen from the results, nominal synthesis achieved relatively better specifications compared to the parasitic-aware synthesis within a shorter synthesis time, since electrical domain synthesis has fewer search parameters. However, these specifications are not reliable and cannot be maintained after the implementation, where including parasitic effects has degraded the circuit performance. Simulation results for one obtained solution are provided in Figure 3.14.

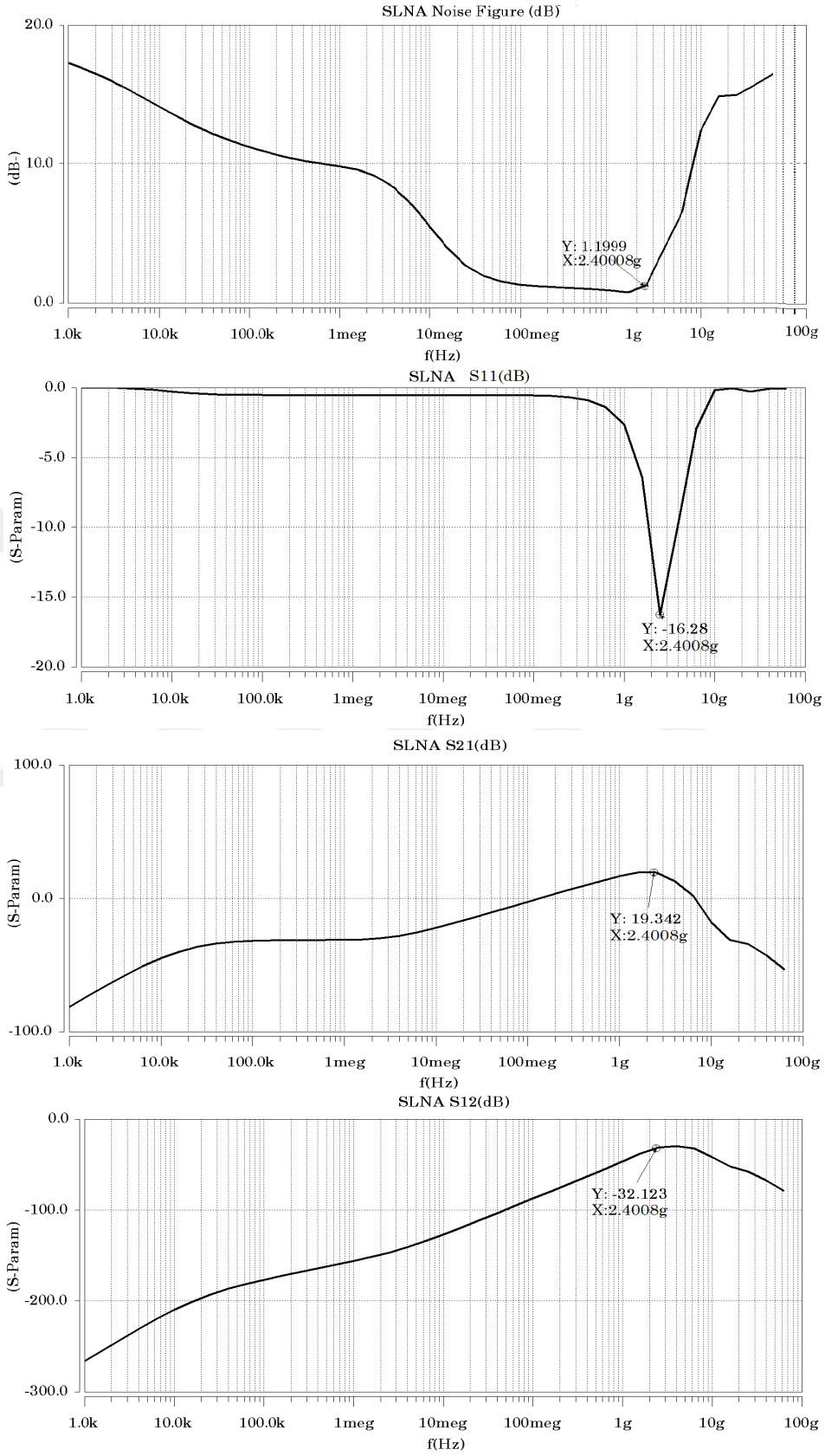

Figure 3.14. SLNA simulation results.

The other synthesis example is a differential LC cross-coupled oscillator, whose schematic is given in Figure 3.15. The oscillation frequency was selected as 5 GHz,

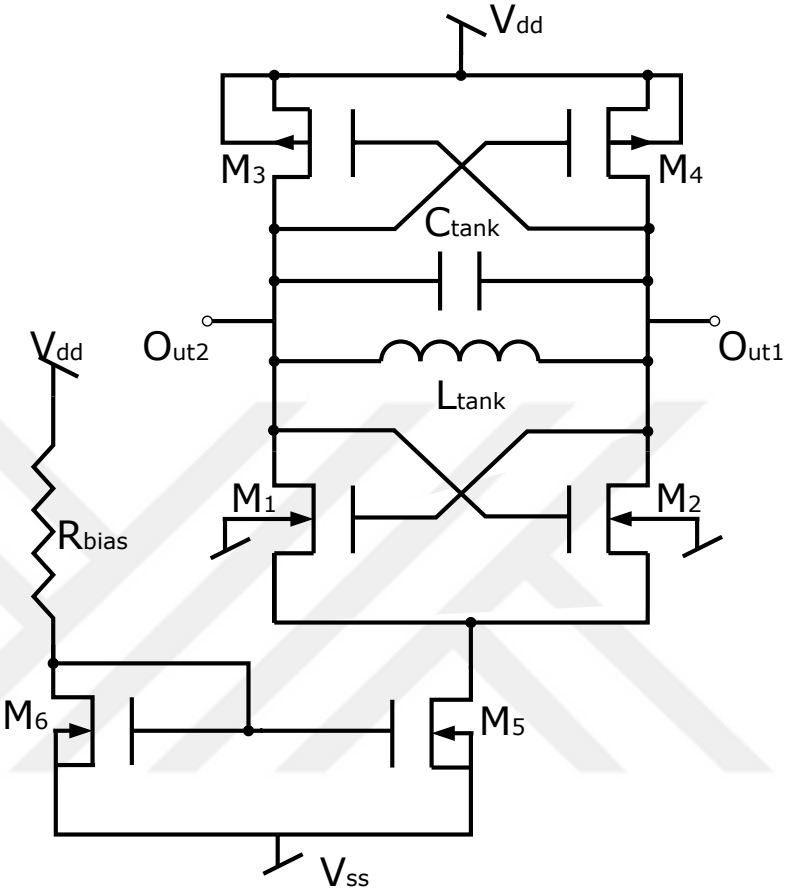

Figure 3.15. CMOS differential cross-coupled oscillator.

where all circuit parameters were selected as design parameters similar to the SLNA example. The list of design variables and boundaries are provided in Table 3.4.

Table 3.4. Design boundaries and variables for the oscillator.

	W $[\mu m]$	L $[\mu m]$	R_{bias} $[\Omega]$	N_t [ ]	W_{ind} $[\mu m]$	D_o $[\mu m]$	s $[\mu m]$	W_{cap} $[\mu m]$	L_{cap} $[\mu m]$
Minimum	0.24	0.12	100	2.5	2	75	1.5	10	10
Maximum	100	1	10000	4.5	10	150	—	50	50

Parasitic sub-circuit models given in Figure 3.10 and Figure 3.11 are called during the evaluation. Oscillation frequency, phase noise , power consumption, and oscillation amplitude were chosen as design constraints. There are two reasons to choose the oscillation amplitude as a design constraint. The first reason is to ensure that there is a certain oscillation, where a number of measurements are performed during the transient simulation in order to guarantee a permanent oscillation. The second one is to find a solution around the voltage limited mode of the oscillator, where the oscillator achieves the most effective point in terms of power consumption and phase noise [91].

Synthesis results for oscillator circuits are given in Table 3.5. A nominal synthesis was also run and the solution was implemented by using real RF components. Results of nominal synthesis and implementation are provided in the fourth and fifth columns, respectively. All targeted constraints are satisfied within an average synthesis time of 1 hour for parasitic-aware synthesis, where the targeted oscillation frequency 5 GHz was found with a standard deviation of 9.5 MHz for these three runs. On the other hand, nominal synthesis achieved a higher performance within a considerably shorter time, since the number of search parameters decreased from 12 to 9. After the implementation, whose results are given in the fifth column, the center frequency shift was substantially increased, where the phase noise performance also degraded due to inclusion of passive device parasitics. Furthermore, transient and frequency simulation results for one obtained solution are provided in Figure 3.16

Table 3.5. Synthesis results for the oscillator.

Constraint	Run 1	Run 2	Run 3	Nominal Run	Implementation
$\Delta f_{osc} < 10$(MHz)	9.2	10.5	9.5	0.4	20
PN < -115(dBc/Hz)	-116.12	-115.1	-115.23	-121.1	-116.9
Power < 13(mW)	12	11.4	10.9	11.2	11.3
$Osc_{Amp} > 1$(V)	1.14	1.16	1.12	1.2	1.09
Synthesis Time(h)	1.04	1.1	1.01	0.7	—

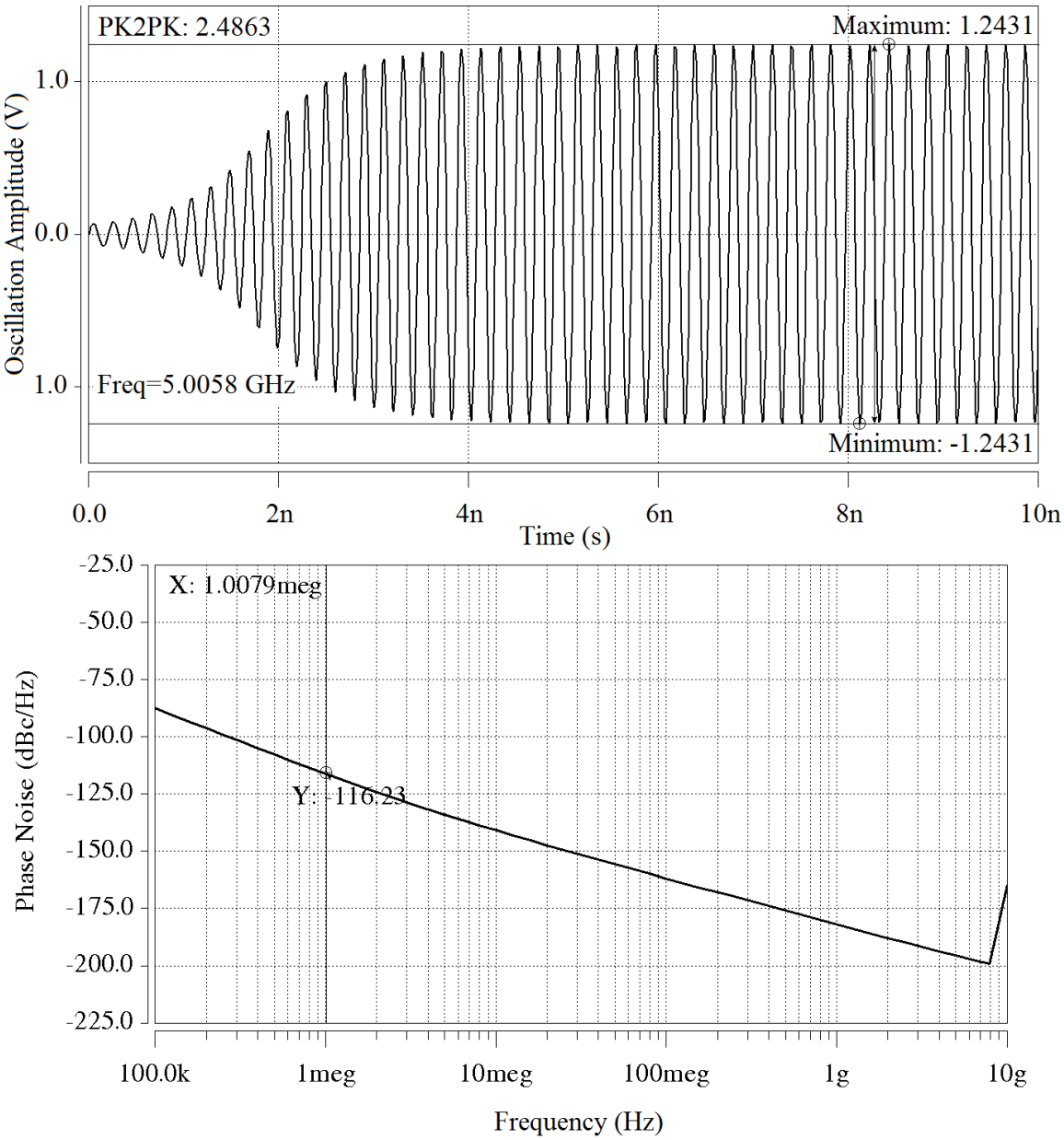

Figure 3.16. CMOS differental cross-coupled oscillator simulation results.

3.5. Conclusion

Simulation-based optimization engines promise more accurate results compared to knowledge-based and equation-based approaches, in which a SPICE level simulator is utilized during evaluation of circuits. Therefore, a SPICE-based analog circuit

synthesis tool is used in this thesis, which was implemented on MATLAB in order to exploit available functions and libraries. Synthesis results indicate that the synthesis tool can solve a moderate sizing problem in less than half hours. In addition to analog circuit sizing tool, a mixed-domain RF circuit synthesis approach was developed, where high level physical-based equivalent circuits are called during the evaluation of passive components, where the design space exploration is carried out by optimizing the physical parameters of these passive devices as well as other design parameters. Even though optimization surface becomes more complicated for mixed-domain circuits analysis compared to the conventional sizing approach (electrical domain sizing), it provides more reliable results; hence, the number of iterations between circuit sizing and layout processes can be substantially decreased.

4. VARIATION-AWARE ANALOG CIRCUIT DESIGN AUTOMATION

Even though automation of analog sizing considerably enhances the time to market, the ever-worsening variability problem lead to a large number of re-iterations, where the design for variability loop is still open-ended and additional evaluations are performed manually to achieve a reliable solution. Therefore, the scope of analog design automation tools have been expanded to meet the robustness requirement by including variability problem into the conventional objective minimization problem [92]. Hence, variability is considered as another design constraint as well as electrical specifications, and tried to be minimized during the synthesis process. However, a further problem arises with the integration of the variation analysis with the optimization process, where numerous iterations are performed during optimization [93]. Thus, the cost of making the tool variation-aware results in an excessively increased synthesis time due to expensive variability simulations. As a consequence, augmentation of synthesis tool with variability analysis should be well-designed to overcome this problem. Moreover, efficient variability analysis and yield estimation techniques can be utilized for yield-aware circuit sizing tools to move the time performance one step further.

Conventionally, sensitivity analysis (SA) [94, 95], worst case analysis (WCA) or corner analysis [96–98], Response surface models (RSM) [99–101], and Monte Carlo (MC) [102–104] analysis have been commonly utilized for variability simulations. SA-based approaches are based on minimizing the dependency to process variations by examining the circuit performance under small changes in uncertain parameters. The accuracy of sensitivity-based analysis is related to the order of the sensitivity matrix, where a higher order sensitivity analysis requires cross correlation factors between uncertain parameters. In WCA-based approaches, worst cases in terms of process variations for a given technology are taken into account, and the design is evaluated with respect to these corners. The efficiency is quite good since the number of simulations are limited thanks to being dimension independent. However, the accuracy

of the worst case analysis is argumentative, in which the yield is estimated for the cases corresponding to only the tails of the probability distribution space [105]. As a consequence, estimated pessimistic yield values may lead to unnecessary overdesign. On the other hand, RSM-based approaches utilize macro-models that are constructed considering design variables and process variations [100]. However, RSM methods suffer from the trade-off between the accuracy and the complexity of the model, where linearly approximated models are not valid for considerably larger variations in submicron technologies, so complicated models have emerged for more accurate estimations [100]. Among all these methodologies, MC-based approaches are prominently the most accurate to estimate the yield, where a stochastic analysis of uncertain parameters is performed via random sampling [106, 107]. However, the primitive MC approach requires a large number of simulations to provide a certain accuracy, which increases the computational effort.

To overcome the efficiency problem, several speed-up techniques have been developed in the literature such as Latin Hypercube Sampling (LHS) and Quasi Monte Carlo (QMC). The idea behind these techniques is to sample the design space in a more uniform way to make accurate estimations with lower sample sizes. Both techniques have been discussed and used for many different problems in the literature. LHS exhibits an excellent uniformity for only lower dimensional projections, whereas QMC provides a superior uniformity for multidimensional projections [102, 108]. One more important advantage of QMC exhibits itself for applications that require iterative analysis, such as yield-aware optimization. Since QMC is a deterministic approach, the sample size can be increased iteratively by pre-determined sample steps. This feature is highly crucial during the optimization process to determine the optimal number of samples and to enhance the efficiency. Two different types of variability analyses are studied in this thesis: sensitivity-based approach and QMC-based approach. Sensitivity analysis is preferred due to ease of use, flexibility, and faster computational performance. However, accuracy problems and lack of cross correlation factors of uncertain parameters limits the use of this analysis. Therefore, sensitivity analysis is then replaced by a MC-based approach, where QMC-based variability analysis is utilized to overcome

computational inefficiency of its conventional MC. Even though QMC analysis exhibits a better time performance, the deterministic nature does not allow probabilistic analysis. To defeat this problem, scrambled QMC-based approach has been proposed in the literature, where an artificial variance can be created by scrambling the sample set. A hybrid QMC-based approach is proposed in this thesis, where the conventional and scrambled QMC approaches are conducted together. In addition to the discussion on variability analysis techniques, the integration of variability analysis with analog circuit synthesis is also thoroughly discussed in this chapter.

This chapter is organized as follows. In Section 4.1, the characterization results of the first test chip are provided and model development process for variation is explained in detail. The developed sensitivity analysis based variation-aware circuit optimization tool is presented in Section 4.2. In Section 4.3, the proposed QMC-based yield-aware optimization tools (QMC and hybrid QMC) are introduced. Finally, the chapter is concluded in Section 4.8 by providing a discussion on the proposed approaches.

4.1. Process Variation Model Development

One aim of the first test chip, whose design is explained in Section A.1, is to observe both inter- and intra-die variation effects and obtain technology dependent variation model parameters for 130 nm technology. In this section, test chip measurements for process variation model development are explained in detail.

Process variation causes changes in some electrical parameters of transistors such as threshold voltage (V_{th}),oxide thickness (t_{ox}), transistor width (W), and length (L). These changes lead to a certain change in the saturation current of the transistors that causes functionality failures resulting in low yield of manufactured ICs. Simply, the saturation current and current factor can be expressed as

$$\begin{aligned} I_d &= \beta(V_{gs} - V_{th})^2 \\ \beta &= \frac{1}{2}\frac{W}{L}\mu_n C_{ox} \end{aligned} \tag{4.1}$$

Using these equations, small changes in the saturation current can be expressed as

$$\Delta I_d = \Delta\beta \frac{\delta I_d}{\delta \beta} + \Delta V_{th} \frac{\delta I_d}{\delta V_{th}} \tag{4.2}$$

The proportional change in the current is obtained as

$$\frac{\Delta I_d}{I_d} = \frac{\Delta \beta}{\beta} - \frac{2\Delta V_{th}}{V_{gs} - V_{th}} \tag{4.3}$$

By using Equation 4.3, the variance of the saturation current can be expressed as,

$$\sigma^2 \left(\frac{\Delta I_d}{I_d} \right) = \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + \frac{4\sigma^2(\Delta V_{th})}{(V_{gs} - V_{th})^2} \tag{4.4}$$

where variances of the threshold voltage and current gain factor for intra-die variations are given as

$$\begin{aligned} \sigma^2(\Delta V_{th}) &= \frac{A_{V_{th}}^2}{W.L} \\ \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) &= \frac{A_{\beta}^2}{W.L} \end{aligned} \tag{4.5}$$

As can be seen from Equation 4.4 and Equation 4.5, variation induced change in the saturation current can be calculated by incorporating variations in the threshold voltage and the current gain factor, which are inversely proportional to drawn area for intra-die variations. Furthermore, variation in current factor can be decomposed into three major components: t_{ox}, W, and L and given as

$$\begin{aligned} \sigma^2 \left(\frac{\Delta t_{ox}}{t_{ox}} \right) &= \frac{A_{t_{ox}}^2}{WL} \\ \sigma^2 \left(\frac{\Delta W}{W} \right) &= \frac{A_W^2}{\sqrt{WL^2}} \\ \sigma^2 \left(\frac{\Delta L}{L} \right) &= \frac{A_L^2}{\sqrt{W^2 L}} \end{aligned} \tag{4.6}$$

On the other hand, inter-die variations are independent from the device area [41], where inter-die variation is commonly accepted constant for all devices located in the same die.

Characterization of the process variation phenomenon was based on the saturation current measurements of single transistors in the test chip, which consists of a number of transistor arrays including transistors having different dimensions. As explained in Section A.1, there are four identical test blocks in a single chip, which are controlled by two control blocks (one for left hand side blocks; *Block1* and *Block2* and the other for right hand side blocks; *Block3* and *Block4*). A schematic view of the designed printed circuit board (PCB) set-up is shown in Figure 4.1.

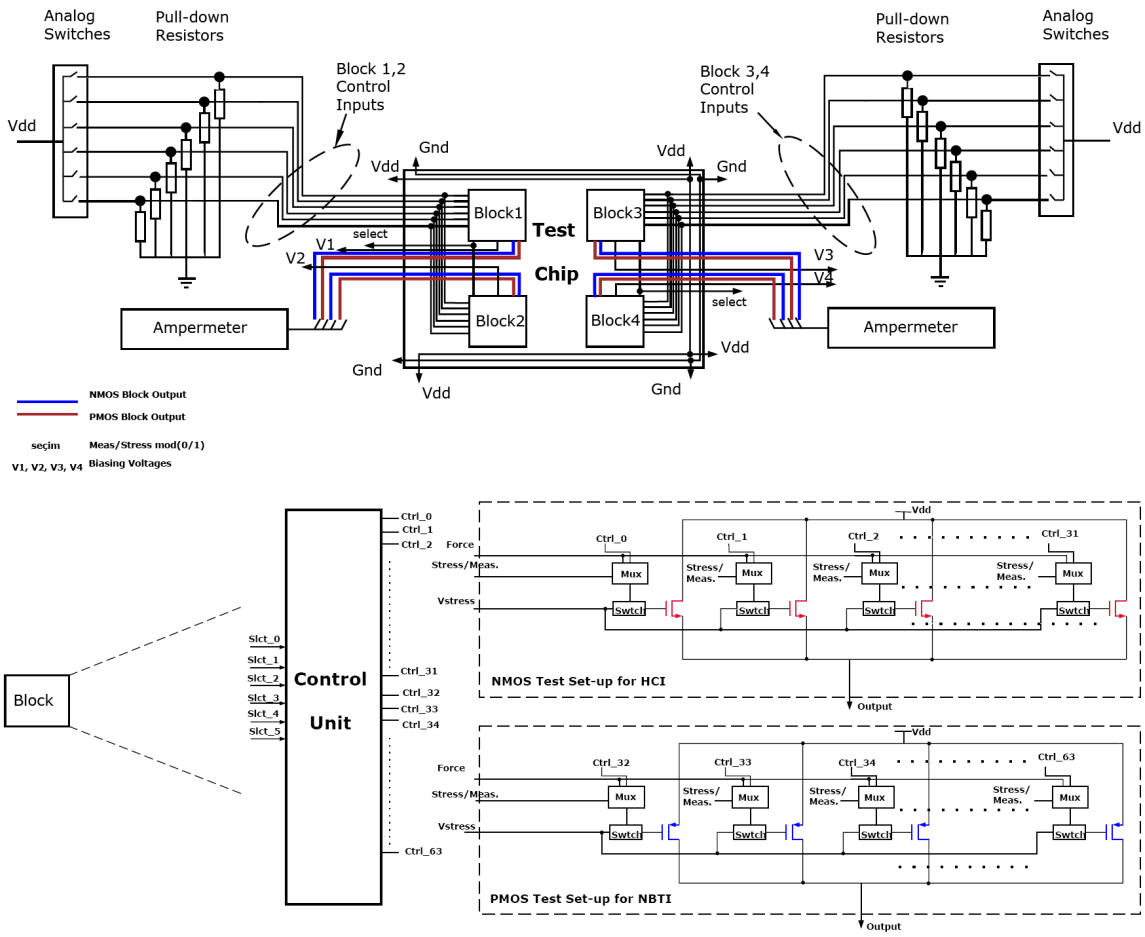

Figure 4.1. The schema of the printed circuit board.

As seen from the schematic, two analog switch arrays were located to generate the control signals. In order to avoid the high impedance case, pull down resistors were connected to switches. Thus, when any switch is opened, the related control input is pulled down to the minimum voltage level (ground). During measurements, "Thandar multimeter 1906 high resolution" was utilized to measure the transistor current. To eliminate leakage current induced measurement errors, the leakage current of each block was measured when all switches are deactivated and the measurement was calibrated by subtracting this leakage current from each measured data. The circuit was supplied by "Hameg HM 7042-5 Power Supply". A photograph depicting the packaged chip and the measurement set-up is given in Figure 4.2.

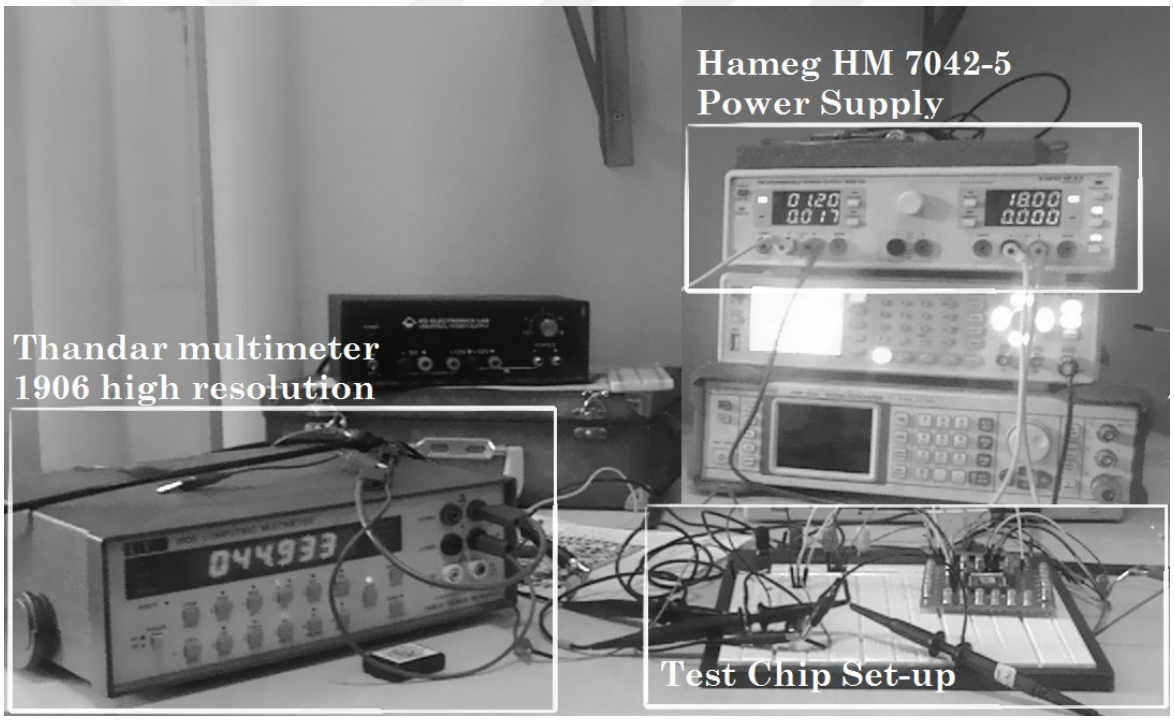

Figure 4.2. Measurement set-up of the test chip.

Measurements were carried out for 4 different chips. Saturation currents were measured for two different cases ($V_{gs1} = 0.5$ and $V_{gs2} = 0.6$) to extract threshold voltage and current gain factor of each transistor, where the threshold voltage of an NMOS device can be extracted as

$$
\begin{aligned}
I_{d1_{i,j}} &= \beta_{i,j}\left(V_{gs1} - V_{th_{(i,j)}}\right)^2 \\
I_{d2_{i,j}} &= \beta_{i,j}\left(V_{gs2} - V_{th_{(i,j)}}\right)^2 \\
\frac{I_{d1_{i,j}}}{I_{d2_{i,j}}} &= \frac{\left(V_{gs1} - V_{th_{(i,j)}}\right)^2}{\left(V_{gs2} - V_{th_{(i,j)}}\right)^2} \qquad \sqrt{\frac{I_{d1_{i,j}}}{I_{d2_{i,j}}}} = a \\
V_{th_{(i,j)}} &= \frac{a.V_{gs2} - V_{gs1}}{a-1}
\end{aligned}
\tag{4.7}
$$

where $i = 1, 2, 3, 4$ denotes the block number and $j = 1, 2, 3, ..32$ denotes the transistor number in each block. Similarly, the current gain factor of an NMOS device is extracted as

$$
\begin{aligned}
I_{d1_{i,j}} &= \beta_{i,j}\left(V_{gs1} - V_{th_{(i,j)}}\right)^2 \\
I_{d2_{i,j}} &= \beta_{i,j}\left(V_{gs2} - V_{th_{(i,j)}}\right)^2 \\
I_{d1_{i,j}} - I_{d2_{i,j}} &= \beta_{i,j}\left(V_{gs1} - V_{th_{(i,j)}}\right)^2 - \beta_{i,j}\left(V_{gs2} - V_{th_{(i,j)}}\right)^2 \\
\sqrt{I_{d1_{i,j}} - I_{d2_{i,j}}} &= \sqrt{\beta_{i,j}}\sqrt{\left(\left(V_{gs1} - V_{th_{(i,j)}}\right)^2 - \left(V_{gs2} - V_{th_{(i,j)}}\right)^2\right)} \\
\sqrt{I_{d1_{i,j}} - I_{d2_{i,j}}} &= b \\
\beta_{i,j} &= \frac{b}{\sqrt{\left(V_{gs1} - V_{gs2}\right)\left(V_{gs1} - V_{gs2} - 2\right)}}
\end{aligned}
\tag{4.8}
$$

These two steps were applied to PMOS transistors and threshold voltages and current gain factors were obtained, as well as NMOS transistors. In Figure 4.3, measurement results of 96 PMOS transistor currents (24x4) for a single chip is given. Transistor current values were normalized by transistor areas and the histogram was fitted to a normal distribution function. Similarly, normalized PMOS transistor current distribution for 4 different chips (4x24) is given in Figure 4.4.

In order to obtain variances of transistor parameters, threshold voltage and current gain factor values were extracted by using Equation 4.7 and Equation 4.8. These steps were repeated for both inter and intra chip variations.

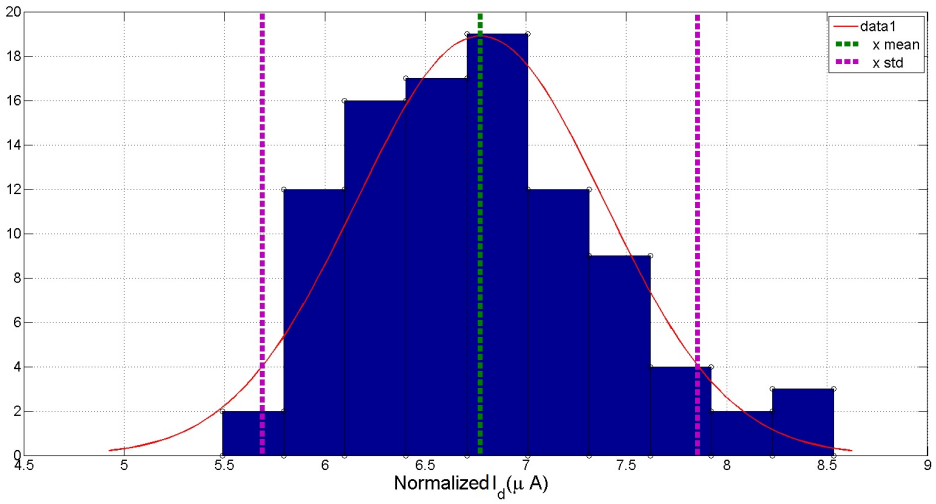

Figure 4.3. The distribution of PMOS transistor currents over a single chip.

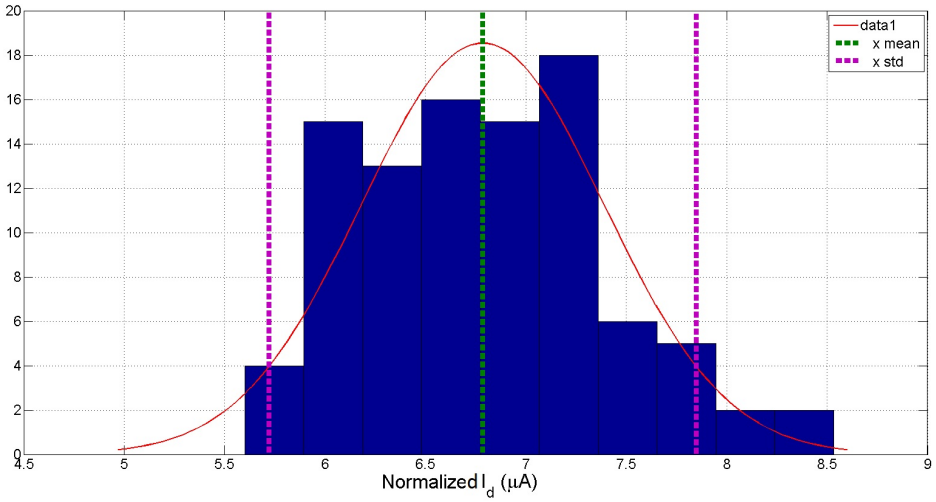

Figure 4.4. The distribution of PMOS transistor currents for four different chips.

The threshold voltage variation distributions of NMOS and PMOS transistors over a single chip are given in Figure 4.5 and Figure 4.6, where mean values were found as $0.35V$ and $-0.437V$, respectively.

In Figure 4.7 and Figure 4.8, obtained inter-die threshold voltage variation distributions are given for NMOS and PMOS transistors.

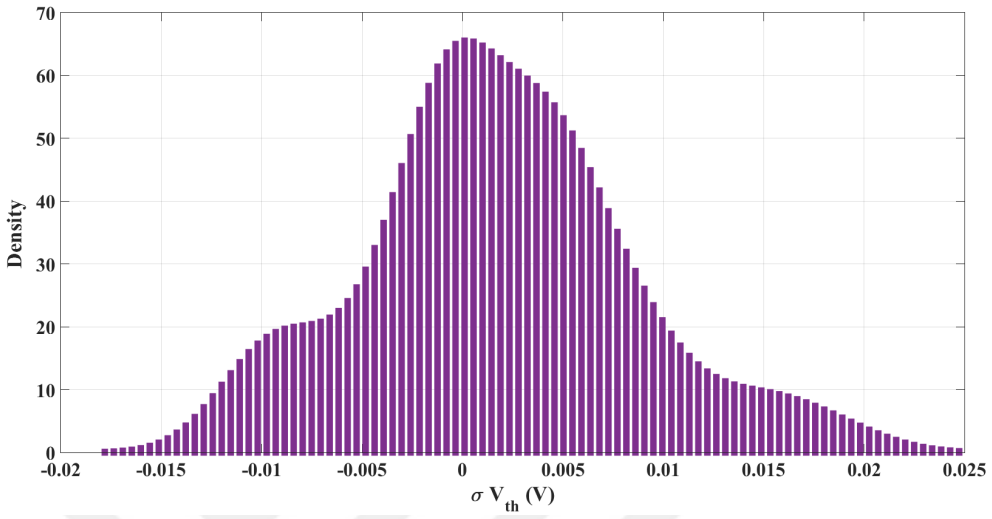

Figure 4.5. The threshold voltage distribution of NMOS devices over a sinle chip.

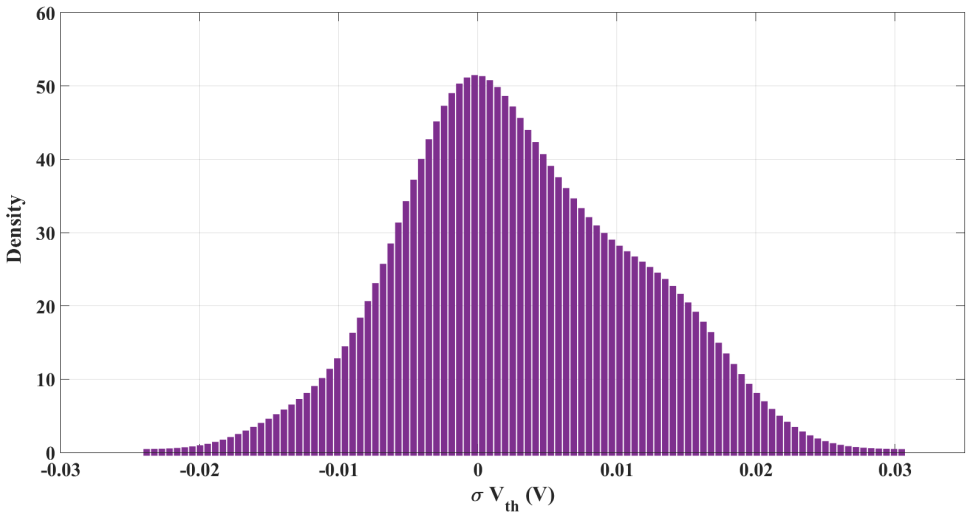

Figure 4.6. The threshold voltage distribution of PMOS devices over a sinle chip.

Distributions were obtained using the measurement results of 4 different chips and 48 transistors (24NMOS+ 24PMOS) in each block, where mean values were found 0.351 and -0.434, respectively.

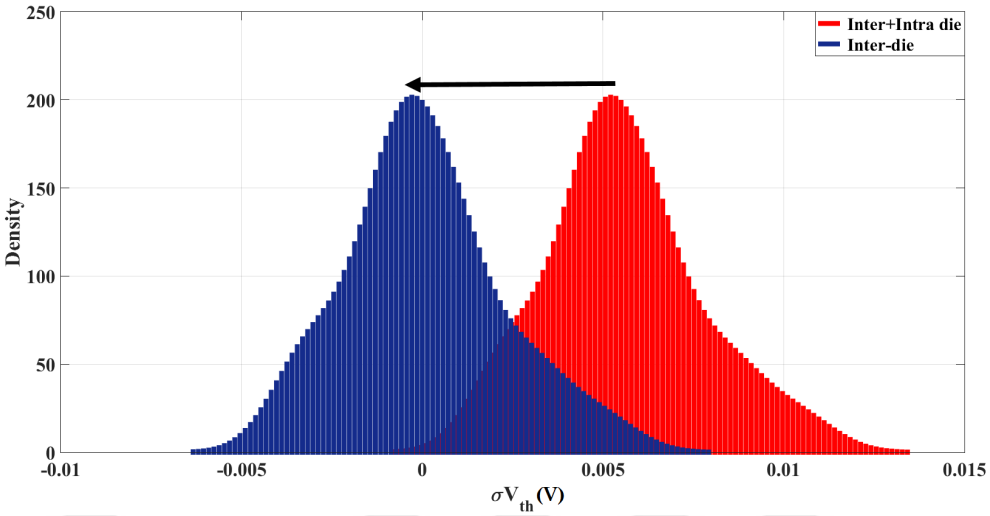

Figure 4.7. Inter-die threshold voltage distribution of NMOS devices.

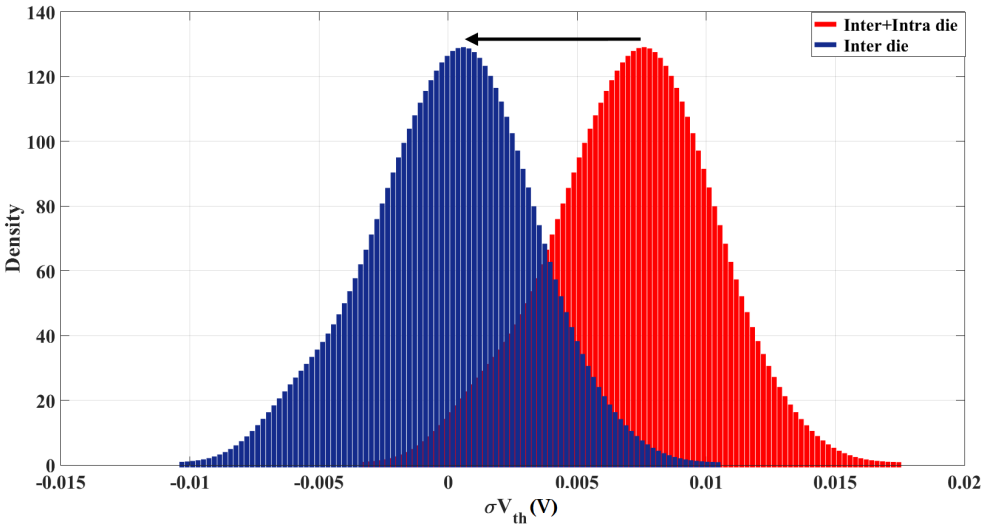

Figure 4.8. Inter-die threshold voltage distribution of PMOS devices.

According to the Pelgrom model [38], the current gain factor (β) is another uncertain parameter that may shift as a result of process variation phenomenon and cause changes in the saturation current.

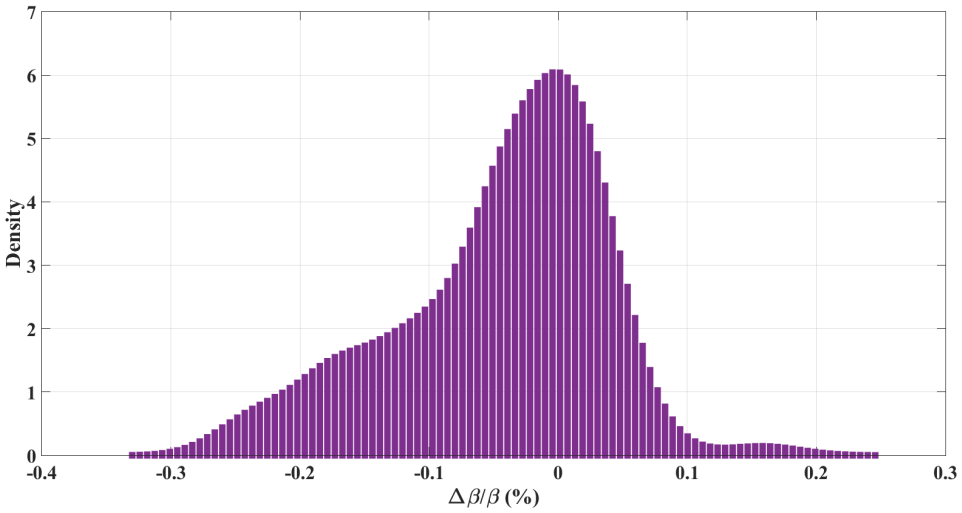

Figure 4.9. Intra-die β distribution of NMOS devices for a single chip.

As can be seen from Equation 4.9, the current gain factor includes three uncertain parameters, transistor width, length, and oxide thickness. As modeled in Equation 4.5, variations of these parameters were combined within a single term $\Delta\beta$.

$$\Delta\beta = \frac{1}{2}\frac{\Delta W}{\Delta L}\mu_n\frac{\epsilon_{ox}}{\Delta t_{ox}} \tag{4.9}$$

The same steps with the threshold voltage extraction approach were repeated for the extraction of current gain factors of NMOS and PMOS devices via Equation 4.8. In Figure 4.9 and Figure 4.10, intra-die distributions of current gain factor of NMOS and PMOS transistors, where a normalization is performed with respect to the (W/L) ratios, are given for a single chip, respectively. Mean values of $\mu_n C_{ox}$ and $\mu_p C_{ox}$ were found $932\mu A/V$ and $310\mu A/V$ for NMOS and PMOS transistors, respectively. In Figure 4.11 and Figure 4.12, obtained intra- and inter-die β distributions are given for NMOS and PMOS transistors. Distributions were obtained using the measurement results of 4 different chips and 48 transistors (24NMOS+ 24PMOS) in each block, where mean values were found $933\mu A/V$ and $310\mu A/V$, respectively.

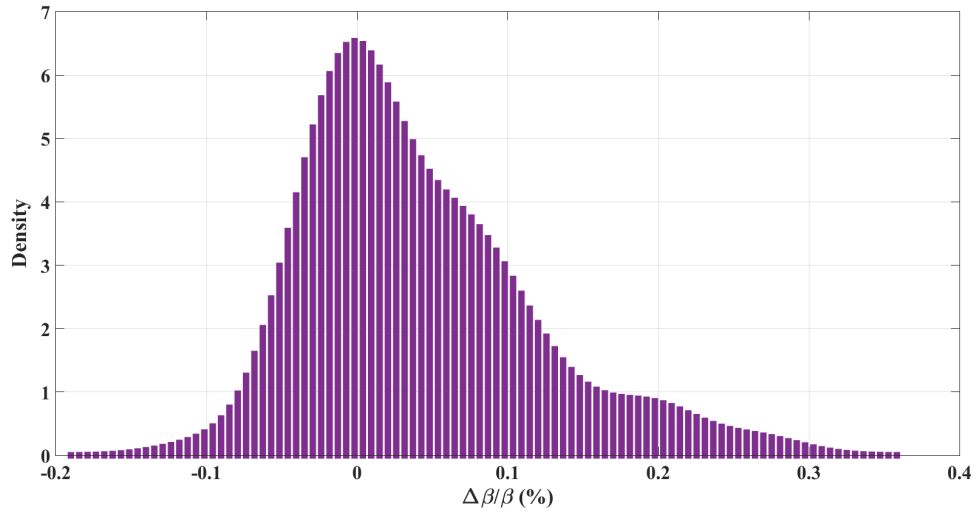

Figure 4.10. Intra-die β distribution of PMOS devices for a single chip.

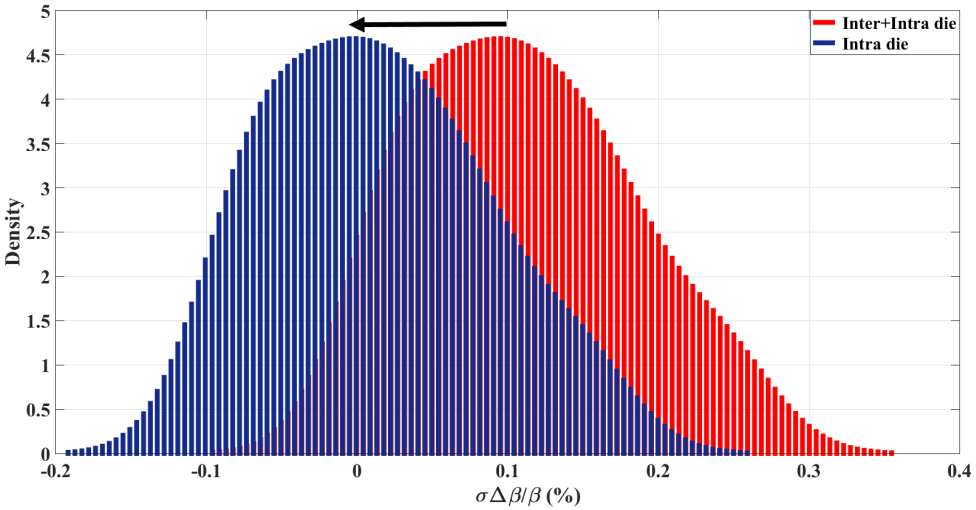

Figure 4.11. Inter-die β distribution of NMOS devices for a single chip.

Furthermore, both variations in current factor results were decomposed into variations in t_{ox}, W, and L. By using these distributions, both intra and inter die variation parameters were obtained. On the one hand, considering intra-die variation phenomenon, technology dependent constants ($A_{V_{th}}$, $A_{t_{ox}}$, A_W, and A_L) were extracted for 48 (24NMOS and 24PMOS) transistors in NMOS and PMOS blocks.

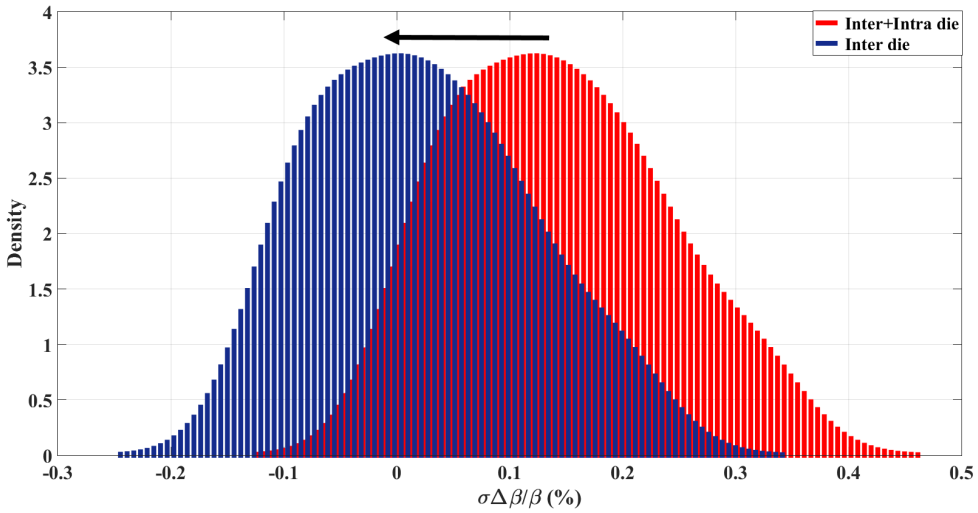

Figure 4.12. Inter-die β distribution of PMOS devices for a single chip.

Table 4.1. Extracted variables and parameters for 130nm technology.

Inter-die results			Intra-die results		
Variable	NMOS	PMOS	Variable	NMOS	PMOS
$V_{th}(V)$	0.351	-0.434	$V_{th}(V)$	0.35	-0.437
$\mu_n C_{ox}(\mu A/V^2)$	932	310	$\mu_n C_{ox}(\mu A/V^2)$	933	310
$\sigma_{V_{th}}(mV)$	7.29	9.01	$A_{V_{th}}(mV)$	5.14e-6	8.24e-6
$\sigma_{t_{ox}}(\%)$	3.1	4.3	$A_{t_{ox}}(\%)$	2.1e-6	4.2e-6
$\sigma_W(\%)$	5.2	6.1	$A_W(\%)$	1.5e-6	2.6e-6
$\sigma_L(\%)$	2.1	3.2	$A_L(\%)$	5.8e-6	7.3e-6

On the other hand, considering inter-die variation, which is independent of the transistor area, variance values were extracted. All measurement and extraction results are given in Table 4.1. According to the technology file provided by the vendor, threshold voltage values $0.32 - 0.36V$ and $0.41 - 0.45V$ for NMOS and PMOS devices for 130 nm technology. In addition to that, the technology file gives $\mu_n C_{ox}$ and $\mu_p C_{ox}$ values $940\mu A/V$ and $320\mu A/V$, respectively. As can be seen from the measurement results, extracted parameter values are in consistent with the fabrication data.

4.2. Sensitivity Analysis-based Variation-aware Analog Circuit Synthesis

Sensitivity analysis is based on the individual examination of the effect of uncertain parameters on circuit specifications. Basically, transistor parameters, such as threshold voltage, oxide thickness, transistor width, and length are deviated one by one and simulations are performed to obtain the effect of each parameter on circuit specifications. Finally, a sensitivity matrix is constructed and change in performance metrics are calculated using a linear approximation. A general form of a sensitivity equation is given as

$$\underbrace{\begin{pmatrix}\Delta y_1\\ \Delta y_2\\ \Delta y_3\\ \vdots\\ \Delta y_n\end{pmatrix}}_{\text{Y=Circuit Specification}} = \underbrace{\begin{pmatrix}\frac{\delta y_1}{\delta x_1} & \frac{\delta y_1}{\delta x_2} & \frac{\delta y_1}{\delta x_3} & \cdots & \frac{\delta y_1}{\delta x_m}\\ \frac{\delta y_2}{\delta x_1} & \frac{\delta y_2}{\delta x_2} & \frac{\delta y_2}{\delta x_3} & \cdots & \frac{\delta y_2}{\delta x_m}\\ \frac{\delta y_3}{\delta x_1} & \frac{\delta y_3}{\delta x_2} & \frac{\delta y_3}{\delta x_3} & \cdots & \frac{\delta y_3}{\delta x_m}\\ \vdots & \vdots & \ddots & \vdots & \\ \frac{\delta y_n}{\delta x_1} & \frac{\delta y_n}{\delta x_2} & \frac{\delta y_n}{\delta x_3} & \cdots & \frac{\delta y_n}{\delta x_m}\end{pmatrix}}_{\text{S=Sensitivity Matrix}} \times \underbrace{\begin{pmatrix}\Delta x_1\\ \Delta x_2\\ \Delta x_1\\ \vdots\\ \Delta x_m\end{pmatrix}}_{\text{X=Uncertain device parameters}} \tag{4.10}$$

where x and y denote uncertain device parameter and circuit specification, respectively. Change in a circuit specification is calculated as

$$\Delta y_i = y_{i0} - y_i = g_i \times \begin{pmatrix}\Delta x_1\\ \Delta x_2\\ \Delta x_1\\ \vdots\\ \Delta x_m\end{pmatrix} \tag{4.11}$$

where g_i denotes i^{th} row of the sensitivity matrix S and y_{i0} denotes the nominal value of the corresponding performance metric. Using this expression, variance of a performance metric is calculated as

$$\sigma_{y_i}^2 = g_i {g_i}^T C, \qquad C = \begin{pmatrix} \sigma_{x_1}^2 & 0 & 0 & \dots & 0 \\ 0 & \sigma_{x_2}^2 & 0 & \dots & 0 \\ 0 & 0 & \sigma_{x_3}^2 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots & \\ 0 & 0 & 0 & \dots & \sigma_{x_m}^2 \end{pmatrix} \tag{4.12}$$

The most important point in this analysis is constructing of correlation (C) matrix, where variance values of uncertain device parameters is required for a first order sensitivity-based variability analysis. As seen from C matrix, cross correlation values are taken as "0", but in practice this assumption is highly optimistic since uncertain parameters have a strong correlation to each other. Furthermore, including correlation of dependent parameters improves the estimation accuracy. Considering the correlation between parameters, the variance of the output takes the form;

$$\sigma_y^2 = \sum_i \left(\frac{\delta y}{\delta x_i}\right)^2 \sigma_{x_i}^2 + \sum_i \sum_j \left(\frac{\delta y}{\delta x_i}\right) \sigma_{x_i} \rho_{ij} \left(\frac{\delta y}{\delta x_j}\right) \sigma_{x_j} \tag{4.13}$$

where ρ_{ij} is the correlation of two uncertain parameters. Since extracting these correlation parameters are quite difficult, first order sensitivity analysis is conventionally utilized. However, this analysis loses the validity in advanced technology nodes, where variations in device parameters become considerably larger and can not be linearly approximated.

To integrate the sensitivity-based variability analysis to the analog circuit optimization tool, two different approaches are proposed in this thesis: over-design approach and robust-design approach. The flow diagram of the over-design approach is given in Figure 4.13. In this approach, nominal synthesis starts and continues until the search algorithm narrows the search space down to a certain region. When the decision mechanism determines that the solution is sufficiently close to the optimal point, variability analysis is included into the optimizer and sensitivity analysis is performed for each individual. Then, each design objective is modified depending on the average

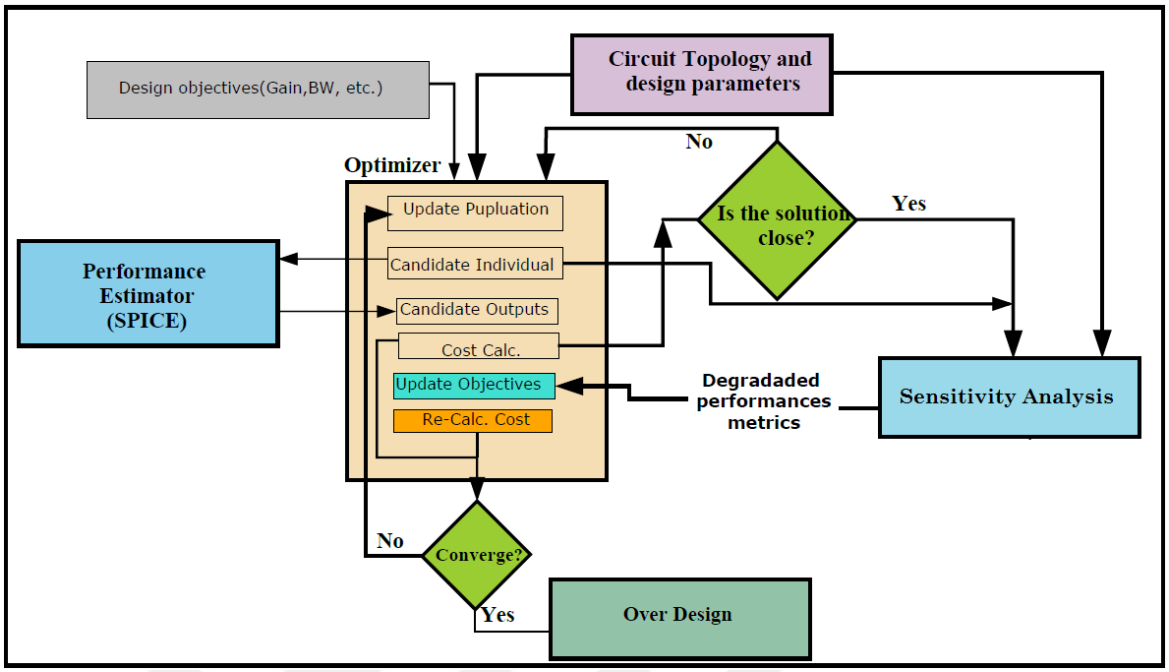

Figure 4.13. Flow diagram of over-design approach.

of the variation data coming from the sensitivity analysis for the current population. As a result, cost values for the next generation individuals are calculated with these new objectives. Thus, the optimizer is enforced to find a better solution to satisfy the former objectives despite the variation effects. In the decision mechanism, the optimizer compares the average cost of the current population with a pre-determined threshold value, and includes variability analysis into the optimization loop when the average value becomes less than this threshold value. Once variability analysis is included, the decision mechanism is disabled to prevent possible errors. As previously explained, sensitivity analysis is based on calculating the deviation of each performance metric by summing of all individual contributions of each uncertain parameter to the corresponding specifications. During the variability analysis, variations in threshold voltage, thickness oxide, transistor width, and transistor length are considered, where each parameter was deviated by 5% to mimic process variation effect.

A two stage OTA circuit shown in Figure 4.14 was utilized as the synthesis example. An Intel $i7$ 4th generation chipset with 3.20 GHz processor was utilized during

the synthesis process. $130nm$ CMOS technology was utilized during the synthesis. Numbers of parents, offspring, and maximum number of iterations were chosen as 50, 50, and 100, respectively. Simulated annealing variables were kept at the default values ($T_f = 1$ and $T_0 = 1000$). Open-loop gain, 3dB bandwidth, output resistance, power consumption, and chip area were determined as design constraints. Design parameter boundaries are provided in Table 4.2, where the circuit has 22 design parameters including transistor dimensions, bias current, and the compensation capacitor.

Table 4.2. Design boundaries and variables for two stage OTA.

Transistor Width $[\mu m]$	Transistor Length $[\mu m]$	I_{bias} $[\mu.A]$	C_{com} $[pF]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
1-100	0.13-10	100-500	0.1-50	1.2	0	1

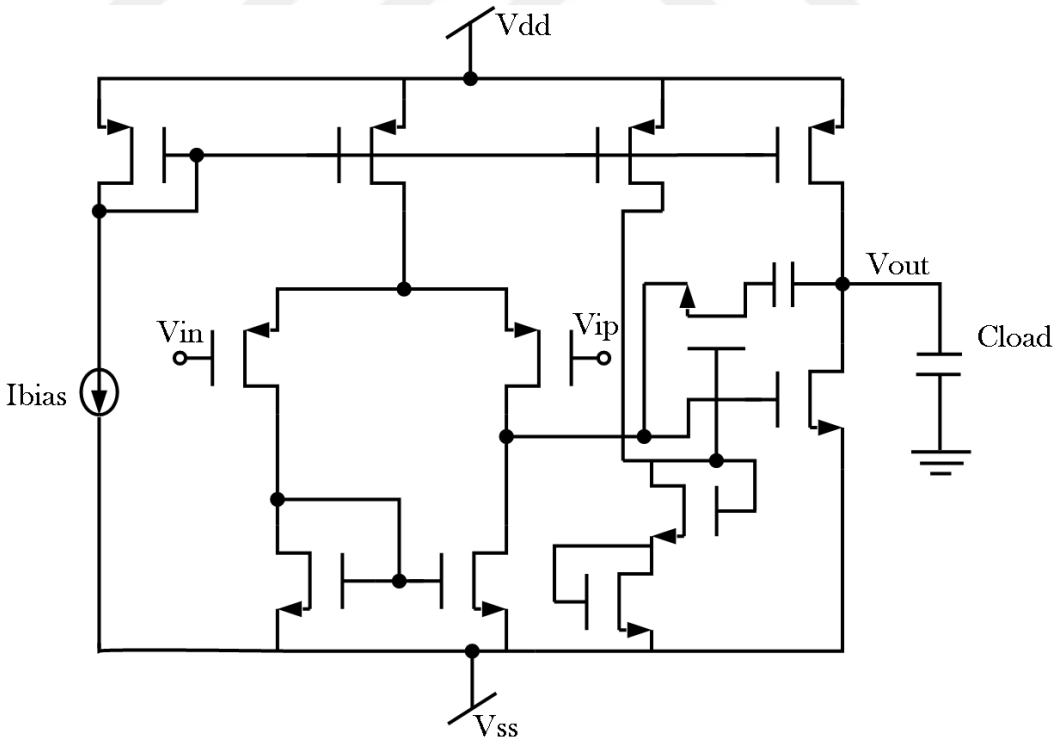

Figure 4.14. Two stage operational amplifier schematic.

Synthesis results of a run are visually illustrated on a pentagonal plane as shown in Figure 4.15, where edges of the planes represent design objectives. The blue circles

represent the best individual specifications that is found at the end of the whole synthesis process, while the red ones are the specifications of the best solution just before the inclusion of the variability analysis. As seen from the results, design boundaries

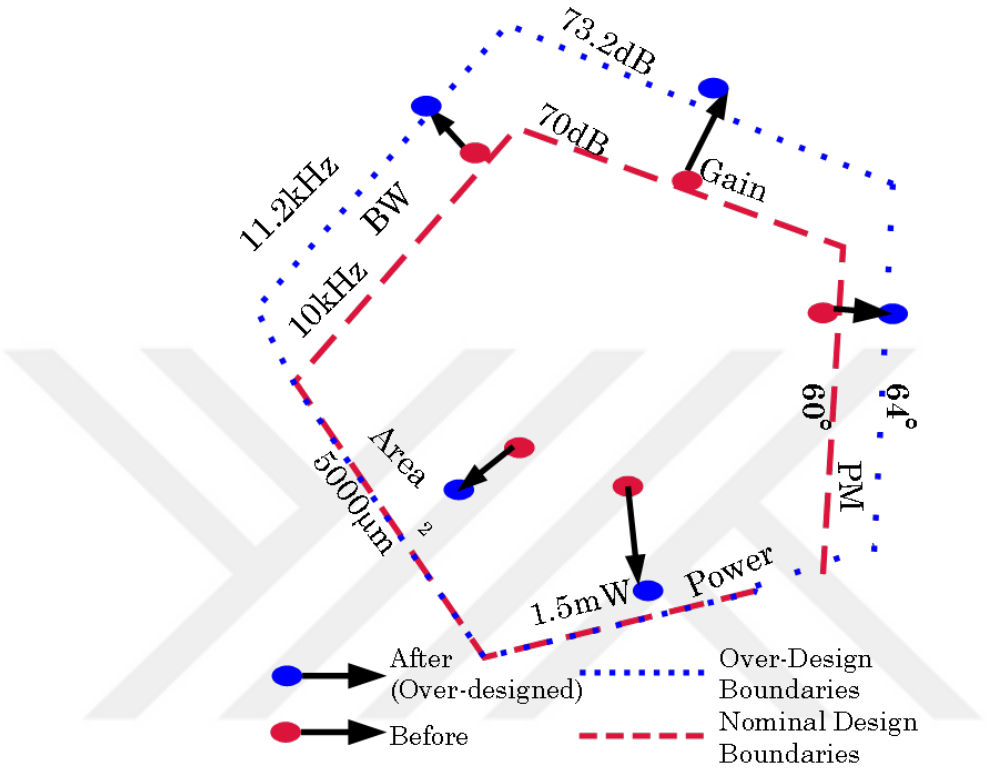

Figure 4.15. An illustration of the overdesigned OTA specifications.

were expanded, where gain, bandwidth, and phase margin specifications were increased during the optimization loop. Thus, the final solution was overly designed with respect to the initial design limits. Furthermore, as expected, chip area and power consumption increases after the variability included as a result of overdesign. Furthermore, design constraints, variation-aware synthesis results for 5 independent runs and nominal synthesis results are given in Table 4.3. As can be seen from the table, power and chip area constraints have been relaxed to make overdesign possible. All final solutions satisfy the former design objectives thanks to the overly designed specifications, which guard-band the design against variation effects. Since overdesign takes place, the final solutions consume more power and occupy large chip area compared to the nominal synthesis result given in the last row.

Table 4.3. Synthesis results of over-design approach.

Run	Synthesis Results	BW (kHz) $> 10kHz$	Gain (dB) $> 70dB$	PM (^{o}) $> 60^o$	Power (mW) $< 1.5mW$	Area (μm^2) $Area < 5000\mu m^2$	Synthesis Time ($min.$)
1	New Boundary	>11.5	>70.2	<63.2	<1.5	<5000	—
	Result	13	72.7	62.8	1.47	4690	82
2	New Boundary	>10.2	>75.6	<61.8	<1.5	<5000	—
	Result	11.2	75.2	64	1.38	4210	74
3	New Boundary	>11.7	>70.8	<66.4	<1.5	<5000	—
	Result	11.8	70.4	63	1.46	4490	58
4	New Boundary	>12.2	>70.4	<62.8	<1.5	<5000	—
	Result	15	71.4	65	1.15	4820	76
5	New Boundary	>11.2	>73.2	<64.1	<1.5	<5000	—
	Result	12.4	74.7	64	1.17	4330	69
6	Nominal Synthesis	11.6	71.8	65	0.45	1848	21.7

The second approach for variation-aware analog synthesis is *Robust-Design* approach, whose flow diagram is shown in Figure 4.16. Contrary to the overdesign approach, variability is defined as a new objective as well as electrical objectives in this method; thus forcing the optimizer to minimize the variability objective during the synthesis. Similar to the previous approach, nominal synthesis starts and con-

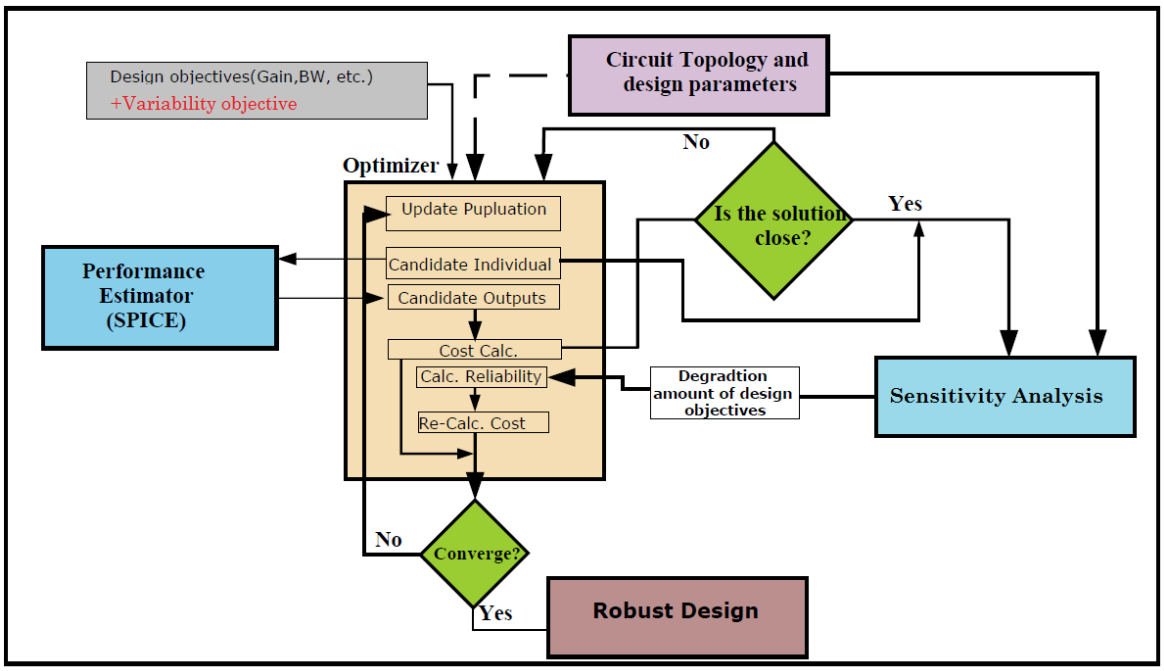

Figure 4.16. Flow diagram of robust design approach.

tinues until the population gets mature enough. The same determination mechanism was used in this approach, where a certain cost value was determined as the decision criterion. Variability objective is not taken into account until the average cost of the population becomes smaller than the decision criterion. When the optimizer focuses on a region around the optimum point, the cost value becomes smaller than the threshold value. Meanwhile, variability simulations started to be performed via sensitivity analysis.

Then, the degradation amount of each design objective is transmitted to the optimizer, where a particular variability cost is calculated by using this variability data. Afterwards, the cost value of the candidate individual is re-calculated by taking

into account the variability cost. As a result, after inclusion of variability analysis, the optimizer tries to minimize variation in design specifications and chooses more robust solutions in the selection part. Variations in threshold voltage, thickness oxide, transistor width, and length are considered during sensitivity analysis, where each parameter was changed by 5%. To illustrate the developed approach, the same OTA circuit was utilized as synthesis example. An Intel $i7$ 4th generation chipset with 3.20 GHz processor was utilized during the synthesis process and a $130nm$ CMOS technology was utilized during the synthesis. Numbers of parents and offspring were chosen as 50 and 50. In contrast to over-design approach, maximum iteration number was determined as 200, since optimizer could not find any robust solution in 100 generations.

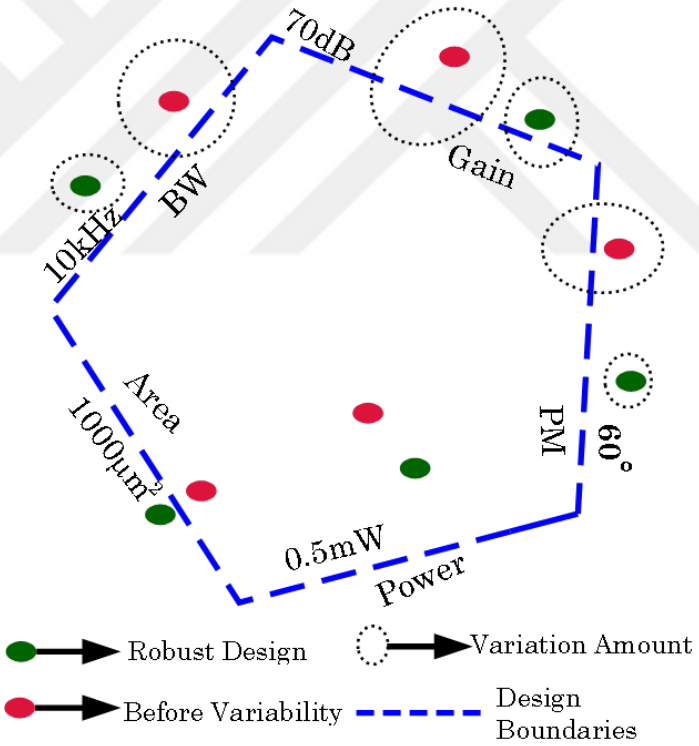

Figure 4.17. An illustration of the robust-design approach solution specifications.

To illustrate the main idea behind approach, synthesis results of a solution is visually shown on a pentagonal plane in Figure 4.17. Variation amounts of the individuals of the final population are represented as a halo around the best solution, which was successfully reduced via evolution of reliability performance over generation.

Table 4.4. Synthesis results of robust-design approach.

Run	Synthesis Results	BW (kHz) $> 10kHz$	Gain (dB) $> 70dB$	PM (^{o}) $> 60^o$	Power (mW) $< 0.5mW$	Area (μm^2) $Area < 1000\mu m^2$	Synthesis Time ($min.$)
1	Before Variability-Variation	12-2.8	69.5-3.5	63.1-3.4	0.36-0	1780-0	—
	After Variability-Variation	11.8-0.69	70.1-1.5	60.4-0.7	0.42-0	1960-0	148
2	Before Variability-Variation	11-2.2	74.6-2.6	6.9-0.6	0.4-0	1060-0	—
	After Variability-Variation	10.7-0.42	70.2-1.6	65-3.8	0.5-0	1120-0	166
3	Before Variability-Variation	11.3-2.9	72.2-3.8	64-2.7	0.41-0	1060-0	—
	After Variability-Variation	11.6-0.6	69.6-0.8	7.6-0.1	0.54-0	1890-0	142
4	Before Variability-Variation	12.4-3	70.2-2.7	62-3.8	0.18-0	1840-0	—
	After Variability-Variation	10.1-0.3	69.4-1.4	61-1.1	0.38-0	2010-0	192
5	Before Variability-Variation	13.1-3.8	70.8-3.1	62-2.4	0.52-0	1020-0	—
	After Variability-Variation	11.7-0.4	71.2-0.3	63-1.2	0.32-0	1280-0	184
6	Nominal Synthesis	11.6	71.8	65	0.45	1848	21.7

Design constraints and synthesis results for 5 independent runs are given in Table 4.2. As seen from the results, variation in design specifications become smaller than the former values just before the inclusion of the variability analysis. Almost all final solutions satisfy all electrical design objectives while minimizing the variability effect. However, it should be noted that the success rate of this approach is rather low (around 10%), where most of runs could not meet either variability objective or one or more electrical design objective even when the iteration number was increased to 200. Consequently, robust design approach promises higher quality results, but there is no convergence guarantee. The convergence is directly related to the design constraints and it would be improved by relaxing design constraints.

4.3. Monte Carlo Analysis-based Variation-aware Analog Circuit Synthesis

Due to the random nature of the variation phenomenon, MC-based approaches have been commonly utilized to simulate this stochastic process. MC approach is based on sampling of the uncertain design space in a random manner, thus, mirroring the stochastic behavior of physical variables for circuit level evaluation. Despite the simple construction and high-accuracy, conventional MC has slow convergence rate, which means a large number of simulations are required to make an accurate estimation, thus limiting the efficiency. This property becomes a bottleneck especially for design automation tools, where numerous variability simulations are performed. To deal with this bottleneck, several speed-up techniques for MC analysis have been developed in the literature. The idea behind these techniques is to minimize the number of samples by using either variance reduction techniques such as (LHS) or using QMC, that utilizes Low Discrepancy Sequences (LDS). There has been an ongoing discussion on superiorities of these approaches to each other. In this thesis, QMC-based sampling is utilized and two different QMC-based yield-aware circuit sizing tools are proposed. This part of the thesis is conducted with Gönenç Berkol, who also reported his contributions in [109].

4.3.1. Yield Estimation via MC-based Analysis

In order to capture the variation effects on circuit performances, the design space is sampled via several sampling approaches, and simulations are performed. Considering the design parameters, $\boldsymbol{X} = (x_1, x_2, ..., x_s)$, and performance values, $\boldsymbol{Y} = (y_1, y_2, ..., y_m)$, output samples of the variability analysis can be expressed as

$$[y_j]^k = \left[f_{sim_j}\left(\{\boldsymbol{X}\}\right)\right]^k, \quad k = 1, 2, ..., n \tag{4.14}$$

where n denotes the number of variability simulations. Deviations in the circuit performances are observed based on these variation simulations. Yield is estimated for each y_j with respect to pre-determined performance metrics for an acceptable design, where the acceptance region for a given design is defined as

$$\begin{aligned} A_j &= \{\boldsymbol{X} : y_j \geq K_j.O_j |\ x \in \mathbb{R}^s\} \\ I_{A_j}(\boldsymbol{X}) &= \begin{cases} 1, & \boldsymbol{X} \in A_j \\ 0, & \boldsymbol{X} \notin A_j \end{cases} \end{aligned} \tag{4.15}$$

where m is the number of design constraints, $K_1, K_2, ..., K_m$ are trade-off coefficients defined by the designer, and O_j denotes the design constraints. I_A is the characteristic function of the acceptance region, also known as the indicator function [110]. Yield can be calculated as the probability of a circuit instance to be in the acceptance region, which can also be obtained as the expected value of the indicator function given as

$$Y = P(\boldsymbol{X} \in A) = E\left[I_A(\boldsymbol{X})\right] = \int_{\mathbb{R}^s} I_A(\boldsymbol{X})\pi(\boldsymbol{X})dx \tag{4.16}$$

where $\pi(\boldsymbol{X})$ is marginal distribution of parameter vector $\boldsymbol{X}$. This s-dimensional integration has a canonical form and can be written as

$$Y = \int_{C^s} f(\boldsymbol{X})dx \tag{4.17}$$

where C is the unit cube in s dimensions [111]. Numerical approximation of this integral is expressed as

$$Y_N = \frac{1}{N}\sum_{i=1}^{N} f(\boldsymbol{X}_i) \tag{4.18}$$

where $\boldsymbol{X}_i$ are sampled points on the space.

4.3.2. Low Discrepancy Sequence and Quasi-Monte Carlo

The idea behind the enhanced MC techniques is based on Koksma-Hlawka theorem [112], where the estimation error can be decomposed into the factor related to the function itself and the factor related to the generated set of random points [112], and is given as

$$\mid \widehat{Y} - Y \mid \leq D_n^{\star}(x_1, x_2, x_3, ...x_n) V_{HK}(f) \tag{4.19}$$

In Equation 4.19, $\widehat{Y}$ and Y are the estimated and real values of the yield, respectively, and $D^{\star}$ is Star Discrepancy; measuring the uniformity of the generated points, where uniform distributions provide a smaller $D^{\star}$. $V_{HK}(f)$ is the total variance of the underlying integrand in the yield expression given in Equation 4.17. As a result of the Koksma-Hlawka inequality, the estimation error can be reduced via two methods: increasing the uniformity of samples or decreasing the variance of the function f [110]. The well-known variance reduction technique is LHS, based on stratification of design space by slices and equal sampling of each slice. It was reported that LHS provides better convergence rate for largely one dimensional problems, otherwise the behavior becomes closer to the primitive MC [104]. On the other hand, the QMC approach is based on decreasing the star discrepancy by using low discrepancy sample sets rather than a random set, thus, samples are homogeneously distributed over the design space. In contrast to LHS, QMC does not suffer from performance loss at higher dimensions [104]. However, the superiority of these approaches to each other has been an ongoing discussion and there is no agreement on this. One further supe-

riority of QMC exhibit itself thanks to its deterministic nature. Thus, sample size can be determined adaptively by using a certain adaptive sizing algorithm. This property becomes highly critical for problems demanding iterative variability analyses. In summary, QMC seems to be more advantageous than LHS for variation analyses handling during yield-aware optimization.

In mathematics, a low-discrepancy sequence is a sequence with the property that for all values of N, its sub-sequence $x_1, x_2, ..., x_N$ has a low discrepancy. Low-discrepancy sequences are also called quasi-random or sub-random sequences, due to their common use as a replacement of uniformly distributed random numbers. The "quasi" modifier is used to denote more clearly that the values of a low-discrepancy sequence are neither random nor pseudo-random, but such sequences share some properties of random variables and in certain applications such as the quasi-Monte Carlo method, their lower discrepancy is an important advantage. Several LDS construction techniques (Halton [113], Sobol [114], Faure [115], Niederreiter [116]) were proposed in the literature.

The main idea behind QMC is to lower the $D^{\star}$, which is a measure of the lack of uniformity and a low-discrepancy sequence is generally generated in the unit s-dimensional hypercube $I^s = [0,1]^s$, [117]. The star discrepancy of the conventional MC for n samples is given in [111] as

$$D^{\star}_{n|MC} = O\left(\frac{1}{\sqrt{n}} log(log(n))^{-0.5}\right) \tag{4.20}$$

where the estimation error of the conventional MC is $O(n^{-0.5})$. On the other hand, considering the QMC, the estimation error is $O(n^{-1})$ and the discrepancy becomes

$$D^{\star}_{n|QMC} = O\left(\frac{1}{n}(log^s(n))\right) \tag{4.21}$$

As a consequence, the convergence error of QMC is asymptotically better than the primitive MC; thus, the required sample size for similar accuracy would be smaller for

the QMC approach. In Figure 4.18, the distributions of 1000 points of pseudo-random numbers and quasi-random numbers on the 2D space are visually illustrated, where it is clearly seen that quasi-random numbers have a highly uniform distribution while psedo-random numbers are more prone to clusters or vacancies.

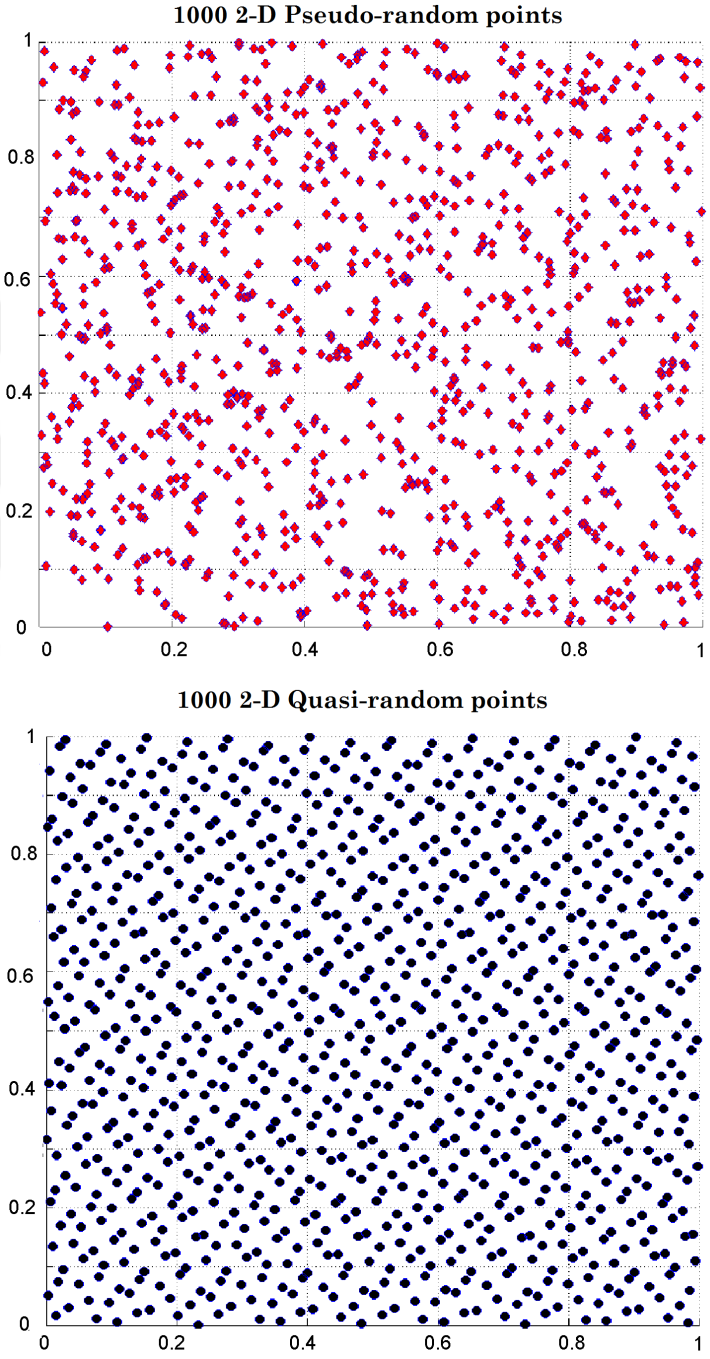

Figure 4.18. 2-D projections for Pseudo-random and Quasi-random numbers.

4.3.3. Integration of Yield Estimation into Analog Circuit Synthesis

Over-design and robust-design approaches were proposed for sensitivity-based analog circuit synthesis. In the sensitivity-based approach, overdesigning is applied by changing the design constraint limits depending on the variation in the corresponding specifications. Thus, the optimizer tries to choose the design point relatively far from the nominal design constraints that provides guarbanding of design constraints. However, power consumption and chip area are sacrificed for the sake of reliability. On the other hand, in the robust design, a variability constraint is defined and included to the optimization loop by defining a variability cost calculated depending on the variation amount of design specifications. Thus, the optimizer tries to minimize the variation amount to generate a robust solution against variation phenomenon. The success rate of the robust approach is considerably low, which highly degrades the time performance of the robust synthesis due to the requirement of re-synthesis iterations. Therefore, another strategy was developed that exploits superiorities of both approaches. In this new approach, power consumption and chip area are somehow relaxed at the beginning, which makes overdesign possible. In addition to that, a yield constraint is also defined at the beginning, which is tried to be maximized through the generations. Therefore, the optimizer determines which approach is utilized. Theoretically, the first choice is of course robust approach since the solution would have a minimum cost among other candidate circuits. However, considering the success rate of the robust approach, overly-designed solutions would be mostly obtained in the majority of runs.

The optimizer evaluates candidate individuals according to their cost values, which are calculated with respect to distances of outputs to the design objectives. When the cost is almost equal to zero, convergence is reached and optimal point is obtained. In this manner, yield term can be given as a new design constraint that the optimizer tries to satisfy. However, performing variability simulations for all individuals is not an efficient way because of waste of time. To include variability into the optimization flow in the sensitivity-based synthesis, a decision criterion was proposed to avoid redundant simulations for individuals of the immature population,

where the average cost value is used as a metric to determine whether the population is mature or not. However, this approach requires a large number of experiments to be performed to determine the threshold cost value. Moreover, there would be a decision problem when a solution partially satisfying the design constraints having high yield values is found. Therefore, the starting point of variability simulations through the evaluation is highly critical. In [118], yield analysis is performed in two different manners. At the initial region of evolution (10-20 generations), yield analysis is performed only for the solutions having less cost than the average cost of the current population. Then, for mature individuals, the variability analysis is only performed for the best individual. However, this approach also requires a number of pre-determined threshold values for the decision. The threshold values highly depend on the problem type so they should be updated for each new problem.

4.3.4. Infeasible Solution Elimination

The optimizer generally needs a few hundred generations of 100 individuals or a fraction of that for generations of 200 individuals. The total population count remains more or less constant and reaches several thousands. Considering that at least a few hundred variability simulations are needed for yield estimation even for one candidate, the synthesis takes excessively long times. In order to decrease the synthesis time, the most common method is Infeasible Solution Elimination (ISE). According to this approach, variability analysis is only performed for the candidates that satisfy the performance metrics given by the user. The acceptance region determines the feasibility space for a certain circuit according to the design constraints. In our case, additional coefficients are defined to take into account the trade-off between the yield and electrical performance. The mechanism of ISE is visually illustrated for two parameters space in Figure 4.19. Considering the uncertain design parameters, $[x_i]_{i=1}^{s}$, and one performance metric, $[y_j]_{j=1}^{m}$, the output can be written as

$$[y_m]^n = [f_{sim_m}([x_i]_{i=1}^{s})]^n \tag{4.22}$$

where n denotes the number of variability simulation (sample size).

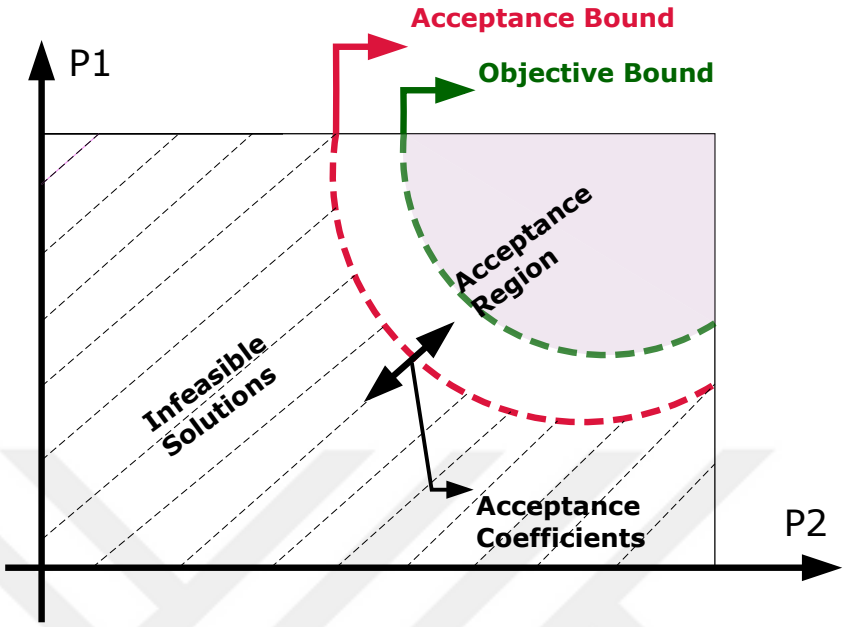

Figure 4.19. Acceptance region and boundaries for two parameters space.

There are some pre-defined specifications that the performance metrics must meet for an acceptable design. This region is called Acceptance Region, which is defined by the user via trade-off coefficients, $K_1, K_2, ..K_m$, in our tool. The acceptance region for a given design is defined as

$$A = \{x : y_m \geq K_m.O_m|,\ x \in \mathbb{R}^s\}$$
$$I_A = \begin{cases} 1, & x \in A \\ 0, & x \notin A \end{cases} \tag{4.23}$$

where m is the number of design constraints, K and O denote design constraint coefficients and the design constraints, respectively. I_A is the characteristic function of the acceptance region, also known as indicator function [111]. As a result, the optimizer does not perform redundant simulations for infeasible solutions.

4.3.5. Adaptive Sizing Methodology for QMC-based Variability Analysis

Although infeasible solution elimination proposed in [105] provides partial enhancement in the synthesis time by avoiding redundant variation simulations for unsatisfied candidates, variability analysis is still expensive for automation tools, where a large number of variability analyses is held during the optimization process. QMC approach improves the time performance of the yield estimation part, thereby reducing the total synthesis time. However, using static sample sizes during yield estimation creates a severe conflict. Namely, keeping the sample size small may lead to an increase in the convergence error, thus unreliable estimations, whereas over-sampling may cause inefficiency in terms of CPU time. To overcome this bottleneck, a dynamic technique can be used to determine the sample size by exploiting the deterministic nature of QMC. Since all points in the low discrepancy sequence can be foreseen at the beginning, the sample size can be increased iteratively without any repetitive simulations. In this sense, the optimum number of sampled points can be determined. In order to determine the optimum sample size, the algorithm given in Figure 4.20 is proposed.

The algorithm starts with an initial variation analysis by using a certain, and relatively small sample size. Then, the sample size is increased by one step, simulations are run for only these additional samples, and a second output space is obtained. Then, histograms of the outputs of these two consecutive sample sets are extracted. The error rate between two sample sets can be measured by using the Kullback-Leibler (K-L) distance between histograms.

The K-L [119] divergence or KL distance is a non-symmetric measure of difference between two probability distributions. It is related to mutual information and can be used to measure the association between two random variables. Given two discrete probability distributions $P(X)$ and $Q(Y)$ with discrete random variates, X and Y, having realizations $X = x_j$ and $Y = y_j$, over n singletons $j = 1, \ldots, n$. KL divergence or distance D_{KL} in between P and Q is defined as

$$D_{KL} = D_{KL}(P(X)||Q(Y)) = \sum_{j=1}^{n} P(X = x_j) log(\frac{P(X = x_j)}{Q(Y = y_j)}) \tag{4.24}$$

where log is in base e.

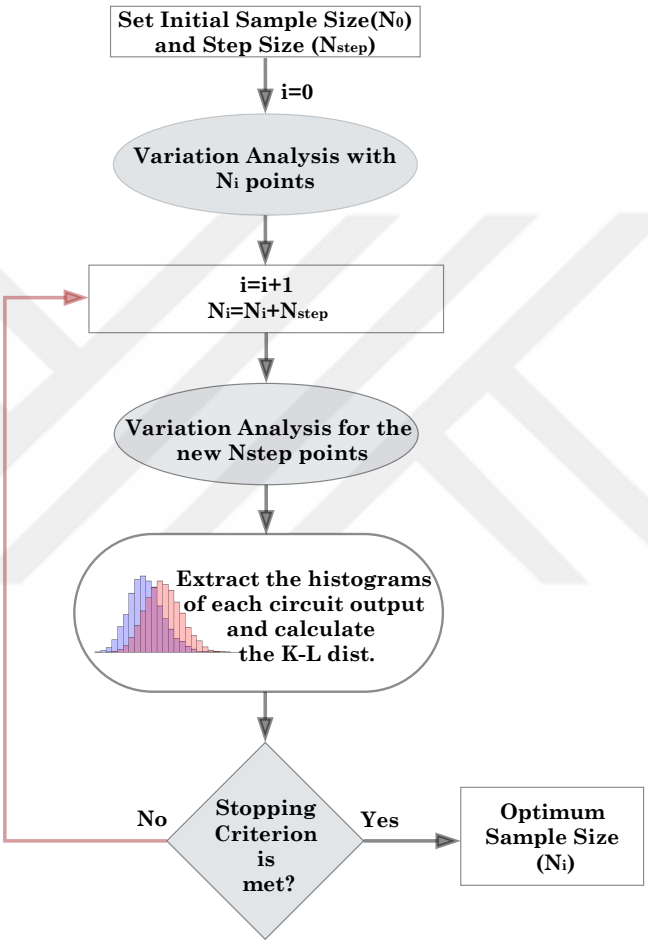

Figure 4.20. Adaptive sample size algorithm.

Two discrete random variables are X and Y, having realizations $X = x_k$ and $Y = y_l$, over m and n singletons $k = 1, \ldots, n$ and $l = 1, \ldots, m$ respectively. Mutual information, $I(X;Y)$ is defined as

$$I(X;Y) = \sum_{k=1}^{n} \sum_{l=1}^{m} R(X = x_k, Y = y_l) log \left(\frac{R(X = x_k, Y = y_l)}{R(X = x_k) R(Y = y_l)} \right) \tag{4.25}$$

log is in base e, and R denotes probabilities. Using these two discrete random variables X and Y, the mutual information $I(X;Y)$ is defined with D_{KL} as

$$I(X;Y) = D_{KL}(R(X,Y)||R(X)R(Y)) \tag{4.26}$$

By using D_{KL} distance, two consecutive sample sets can be compared and an error is calculated. When the error rate considerably diminishes, or in other words, the stopping criterion is met, the sample sequence expansion is stopped. Otherwise, the sample size is increased by one more step size, and the loop proceeds until the stopping criterion is satisfied. The behavior of the error rate over the expanding sample size is given in Figure 4.21. As can be seen from the figure, the error rate rapidly decreases down to a certain point that is called threshold value for the stopping criterion.

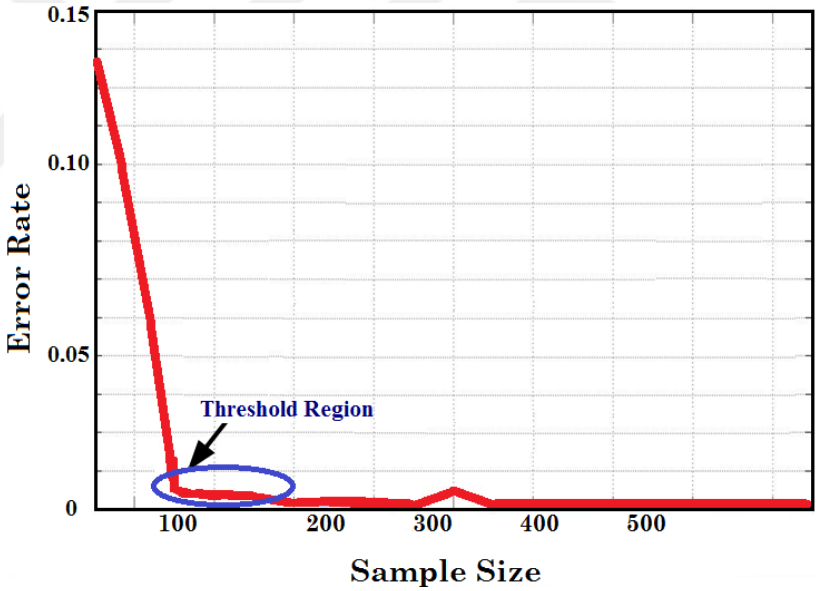

Figure 4.21. The behavior of the error rate between two consecutive sample sets.

4.4. QMC-based Yield-aware Analog Circuit Synthesis Tool

The idea behind the yield aware optimization is to find a dedicated solution region, where not only the electrical specifications, but also the yield requirement is satisfied. The general flow diagram of the proposed optimization tool is shown in Figure 4.22.

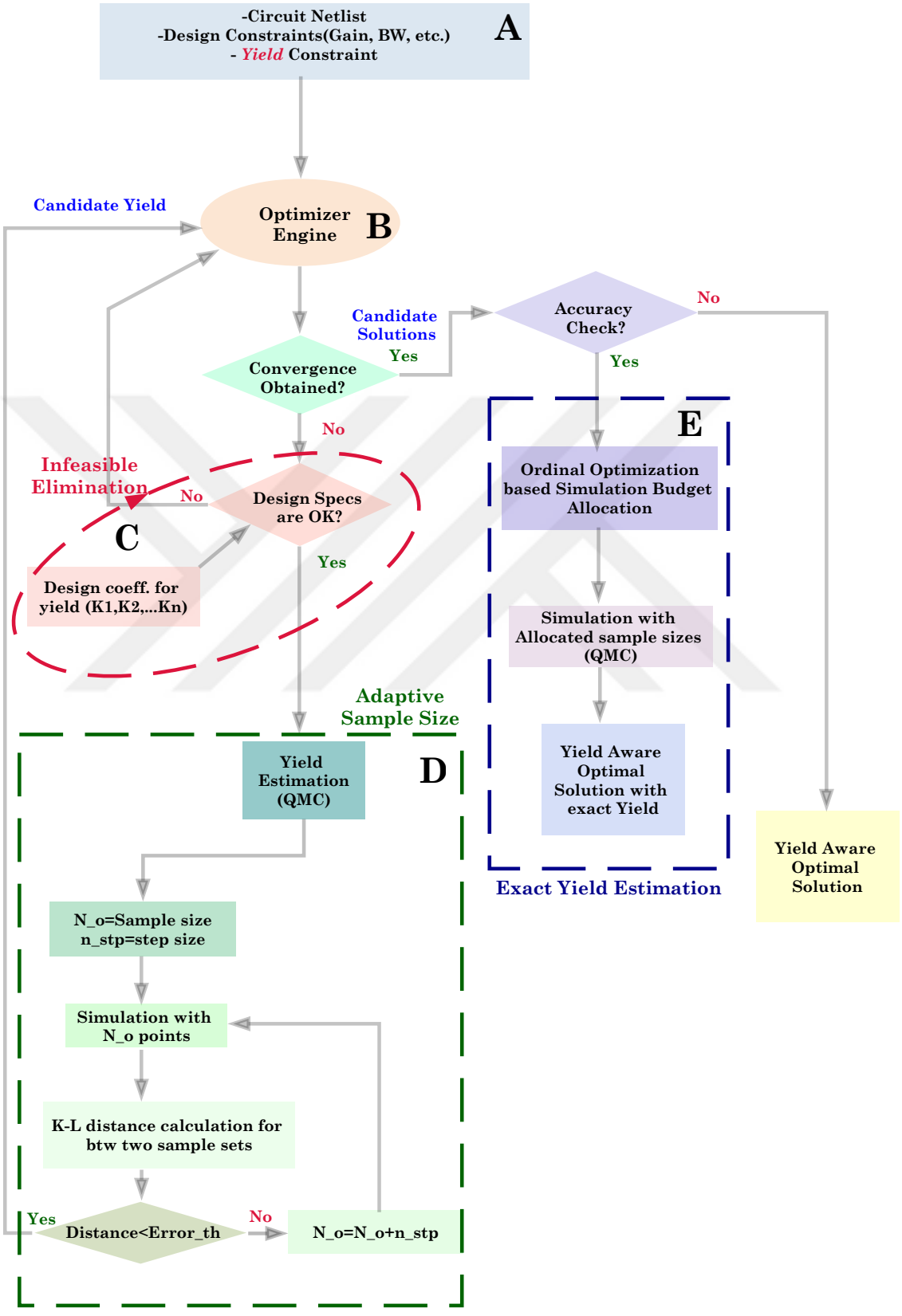

Figure 4.22. Flow diagram of QMC-based yield-aware analog circuit sizing tool.

4.4.1. Block Descriptions

According to this figure, the tool can be analyzed in five main modules, Optimizer, Infeasible Solution Elimination, Yield Estimation, and Exact Yield Estimation blocks. The tool was developed on the MATLAB® platform, where HSPICE was utilized for performance estimation. In the user interface module, circuit netlist, electrical specifications, yield requirement, and trade-off coefficients for yield estimation are defined by the user.

4.4.1.1. Optimization Engine. The single objective analog circuit optimization tool introduced in Section 3 is utilized as optimization engine.

4.4.1.2. Infeasible Solution Elimination. Low performing (infeasible) solutions are eliminated depending on the design coefficients defined by the user as visually illustrated in Figure 4.19.

4.4.1.3. Yield Estimation. Solutions satisfying the feasibility analysis are selected as candidates and sent to the yield estimation part. A QMC-based variability analysis is performed for each candidate. A Sobol sequence is chosen to generate sample sets during uncertain design space sampling. The deviations in V_{th}, t_{ox}, W, and L are considered to evaluate the variation effects. Inter- and intra-die variations are considered by using the technology variables given in Table 4.1.

4.4.1.4. Exact Yield Estimation. This module is an optional part. The aim of this part is to allocate a pre-defined simulation budget, T_{budget}, which is determined as given in Equation 4.27, to each candidate solution based on its yield value to observe a more accurate yield estimation. To determine the simulation amount for each candidate, an asymptotic approach proposed in [120, 121] is assigned. According to the approach, the simulation budget for each candidate is calculated as

$$
\begin{aligned}
n_b &= \sigma_b \left(\sum_{i=1,\ i\neq b}^{M_1} \left(\frac{n_i^2}{\sigma_i^2} \right) \right)^{0.5} \\
\frac{n_i}{n_j} &= \left(\frac{\sigma_i/\delta_{b,i}}{\sigma_j/\delta_{b,j}} \right)^2 \\
i, j &\in 1, 2, 3, ...N_{cand}\ i \neq j \neq b \\
T_{budget} &= sim_{ave}.N_{cand}
\end{aligned}
\tag{4.27}
$$

where b is the best candidate according to the yield specifications among N_{cand} candidates. σ_1^2,σ_2^2,σ_3^2, ...,$\sigma_{N_{cand}}^2$ denote the variance values of N_{cand} solutions. $\delta_{b,i}$ denotes the deviation of the estimated yield with respect to the yield of the best design and sim_{ave} is a user-defined variable arranging the average value of the number of simulations per candidate. The algorithm optimizes the trade-off between deviations of estimated yield and accuracy to obtain reliable yield estimation.

4.4.2. Synthesis Examples and Results

A two stage OTA and a folded cascode OTA were chosen as design examples. Simulations were performed with HSPICE using 130nm UMC technology. ΔV_{th}, Δt_{ox}, ΔW, and ΔL were considered during the yield estimation. An Intel i7 chipset with 2.80GHz processor was utilized during the synthesis process. Numbers of parents and offspring, and maximum number of iterations were chosen as 50, 50, and 200, respectively. For variability analysis, the initial value for sample size (N_0) and the step size (n_{stp}) were chosen as 48 and 10, respectively. To determine the total simulation budget for exact yield estimation, sim_{ave} was selected to be 100.

4.4.2.1. Two Stage OTA. The schematic of the two stage example is given in Figure 4.14. All circuit elements (transistor dimensions, bias voltages-currents, etc.) were given to the optimizer as design parameters, where the number of circuit design variables is 22.

Table 4.5. Design boundaries and variables for two stage OTA.

Transistor Width $[\mu m]$	Transistor Length $[\mu m]$	I_{bias} $[\mu.A]$	C_{com} $[pF]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
0.65-135	0.13-13	50-1000	0.1-50	1.2	0	1

Table 4.6. Synthesis results of 5 independent runs for yield aware and standard optimization.

	BW (kHz) $> 10kHz$	Gain $> 70dB$	PM $> 60^o$	Power $< 1.5mW$	Area $< 5000\mu m^2$	$Yield_{est.}$ $> 80\%$	N_{sample} —	$Yield_{exact}$ $> 70\%$	N_{exact} —	Error (%)	Synthesis Time (min.)
1	10.2	68.5	58	1.2	4900	98.96	108	99.02	5081	0.06	133
2	9.8	75.6	66	1.3	4700	99.83	128	99.22	5552	0.61	96
3	10	73.5	60	1.3	4300	99.02	168	99.84	4034	0.82	116
4	10.7	69.5	58	1.5	4800	99.45	138	99.84	4034	0.29	114
5	11.2	68.5	61	1.1	4030	98.7	128	98.84	4534	0.14	122
N	12.6	74.8	62	0.53	1880	—	—	62.74	1000	—	—

Design variable boundaries and synthesis are presented in Table 4.5 and Table4.6, where the results of 5 independent yield-aware optimizations and the average results of 3 independent nominal synthesis were provided, respectively. Constraint coefficients, $K_1, K_2, ...K_5$, for infeasible solution elimination were selected as 0.95. According to the sample size results, 108-168 samples seem to be sufficient to estimate the yield during the synthesis. After the synthesis process, simulation budget allocation for exact yield estimation was enabled, the maximum number of additional samples were devoted to the candidate with maximum yield, which is an order of magnitude larger than the sample sizes used during the optimization process. The maximum error rate in the yield is found to be 0.82%, which indicates that the stopping criterion is quite successful in determining the minimum sample size required for accurate yield estimation. As expected, the chip area and power consumption increase to satisfy the yield constraint.

According to the nominal optimization results, since yield was not taken into account as a design constraint, optimizer has focused on the electrical specifications and found better electrical specifications. The average synthesis time is around 110 minutes without exact simulations, which is quite acceptable. Furthermore, one should consider that the yield estimation depends on the acceptance region definition, where giving somehow relaxed coefficients may result with higher yields and vice versa. Namely, provided yield values were calculated for 0.95 acceptance region coefficients and the average yield increases to 100 by decreasing coefficients to 0.9. On the other hand, increasing acceptance region coefficients to 0.99 results with an average yield of 85.4%.

4.4.2.2. Folded Cascode OTA. The schematic of the folded cascode OTA is given in Figure 4.23, which has 16 design variables including transistor dimensions, bias current, and voltages. Design variable boundaries and synthesis results for the folded cascode circuit are given in Table 4.7 and Table 4.8, respectively. Similar to the previous example, the results of 5 independent yield-aware optimizations and the average results of 3 independent nominal optimizations are presented in the table.

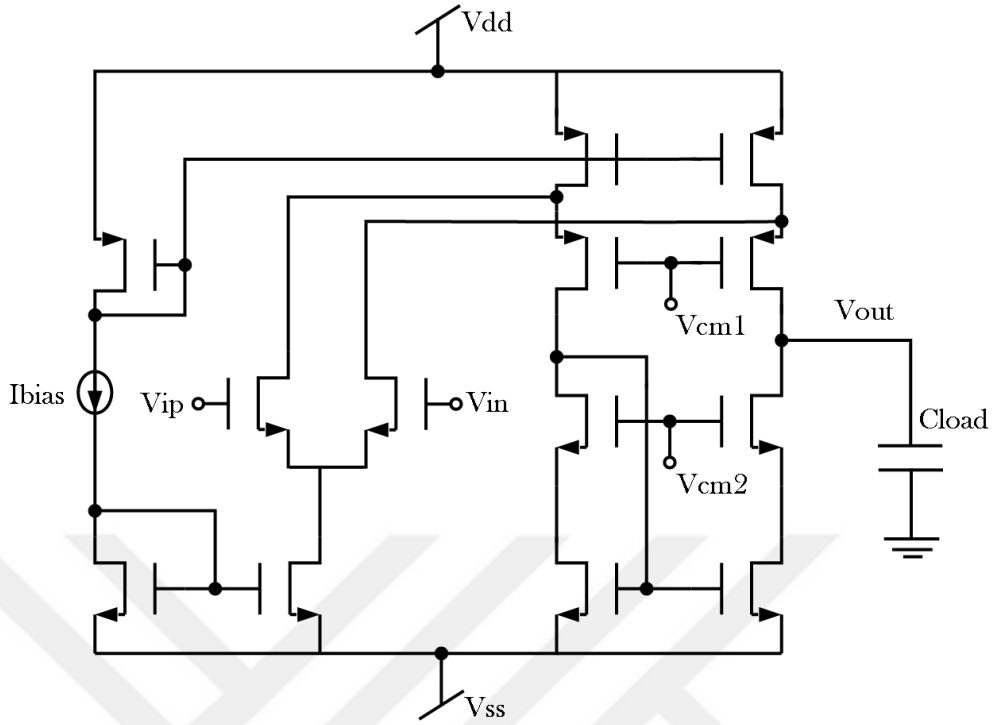

Figure 4.23. Folded cascode amplifier.

Constraint and acceptance region coefficients were selected as 0.95. The number of QMC samples varies between 108 and 188 for this circuit. The maximum error rate in the yield was found to be 0.5%, so the stopping criterion determines the efficient sample size with a high accuracy. As a result of overdesigning, the chip area and power consumption increase to satisfy the yield constraint. According to the nominal optimization results, the average yield was found to be %75, since yield is not taken into account during the synthesis. However, the optimizer has found better electrical specifications compared to the yield-aware synthesis. The average synthesis time is again around 110 minutes without exact yield simulations. Furthermore, the same comment is also valid for this case; the yield estimation depends on the acceptance region coefficients. In this circuit, the average yield increases to 100 by decreasing coefficients to 0.9 while increasing acceptance region coefficients to 0.99 results with an average yield of 90.4%.

Table 4.7. Design boundaries and variables for folded cascode OTA.

Transistor Width $[\mu m]$	Transistor Length $[\mu m]$	I_{bias} $[\mu A]$	V_{cm1} $[V]$	V_{cm2} $[V]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
0.65-135	0.13-13	50-1000	0.4-0.8	0.4-0.8	1.2	0	1

Table 4.8. Synthesis results of 5 independent runs for yield aware and standard optimization.

	BW (kHz) $> 10kHz$	Gain $> 70dB$	PM $> 60^o$	Power $< 1mW$	Area $< 5000e^{-9}m^2$	$Yield_{est.}$ $> 80\%$	N_{sample} —	$Yield_{exact}$ $> 70\%$	N_{exact} —	Error (%)	Synthesis Time (min.)
1	10.5	74.2	70	0.82	4860	98.7	128	98.24	1617	0.46	140.4
2	9.5	76	67	0.70	4750	98.8	168	98.46	1985	0.34	137.4
3	11.5	69.8	69	0.65	4960	99.24	188	99.4	5049	0.16	134.5
4	12.5	69	59	0.94	4420	98.0	148	98.50	8049	0.5	94.8
5	9.9	72	55	0.68	3960	99.15	108	99.41	6550	0.26	122.3
N	12.4	72	68	0.23	2050	—	—	75.4	1000	—	22.2

4.5. Statistical Error Estimation for QMC: Scrambled QMC

Efficient variability analysis and accurate yield estimation can be realized with the adaptively sized QMC approach. However, estimation of the yield is not sufficient for statistical analysis. Considering the mass production of ICs, a confidence interval should also be provided at the end of the variability analysis, where error bounds determine the probabilistic variation of the yield. Namely, a yield of 99.9 % can be worthless with a 5% confidence band, which means the yield value may potentially be unacceptable. Therefore, a confidence interval is required to be able to give the estimation reliability.

In practice, the exact value of the integral given in Equation 4.17 is unknown, so the error in the estimate Y_n is problematic. In MC and LHS, a probabilistic measure of the estimation error can be provided by running a number of variation analyses with varied sample sets. However, the case for QMC is quite different, where generated sample sets result in the same estimations due to their deterministic nature, so it is not possible to talk about a probabilistic error between estimations. Moreover, it is impossible to calculate both the total variation $V(f)$ and $D^\star$ in Koksma-Hlawka inequality. Even if error bounds can be obtained from Equation 4.19, these bounds can be different from the real error bounds [110].

In summary, the confidence interval of the estimation can not be obtained for QMC approach. To overcome this issue, randomizing QMC (scrambling) has been proposed [122–124]. The core idea behind randomizing QMC (RQMC) is to apply an effective and a fast randomization algorithm to existing quasi-random sequences. Thus, it provides a practical method to obtain error estimates for QMC, which is based on treating each scrambled sequence as a different and independent random sample from a family of randomly scrambled quasi-random numbers. Thus, scrambled-QMC overcomes the main disadvantage of QMC while possibly maintaining the superior convergence rate of QMC. Owen [122] proposed a general scrambling scheme for randomizing.

Assuming any quasi-random sequence number and its scrambled version in $[0,1]^s$ are

$$\begin{aligned} x_n &= \left[x_n^{(1)}, x_n^{(2)}, x_n^{(3)}, ..., x_n^{(s)}\right] \\ y_n &= \left[y_n^{(1)}, y_n^{(2)}, y_n^{(3)}, ..., y_n^{(s)}\right] \end{aligned} \tag{4.28}$$

respectively. The binary representation of the jth coordinate of x_n can be expressed as

$$x_n^j = \left[0 x_{n,1}^{(j)} x_{n,2}^{(j)} .... x_{n,k}^{(j)}\right] \tag{4.29}$$

where k is the number of digits to be scrambled and i^{th} digit of this coordinate is $x_{(n,j)}^{(i)}$. Then, the scrambled $x_{(n,i)}^j$ is expressed as

$$y_{(n,i)}^j = \pi^j_{\left(x_{n,1}{}^{(i)}, x_{n,2}{}^{(i)} .... x_{n,i-1}{}^{(i)}\right)} \left(x_{(n,i)}^j\right) \tag{4.30}$$

where $\pi^j_{x_{n,i}}$' s are random permutations of the digits $(0, 1, ..., k-1)$ in base k ($k = 2$ for Sobol points), chosen uniformly and independently. In Figure 4.24, quasi-random number distributions for non-scrambled and scrambled cases are illustrated, where scrambled numbers have still good uniformity over the space as well as non-randomized ones.

As consequence, a few differently scrambled QMC runs provide a standard deviation that can be used as a probabilistic measure of the estimation error. Let's $\left\{x_i^{(j)}\right\}_i^N, \quad j = 1, 2.., M$ be scrambled sample sets. The yield is estimated for each sample set and the mean of the yield is calculated as

$$Y^{(j)} = \frac{1}{N} \sum_{i=1}^{N} f(x_i^{(j)}), \quad j = 1, 2..., M \tag{4.31}$$

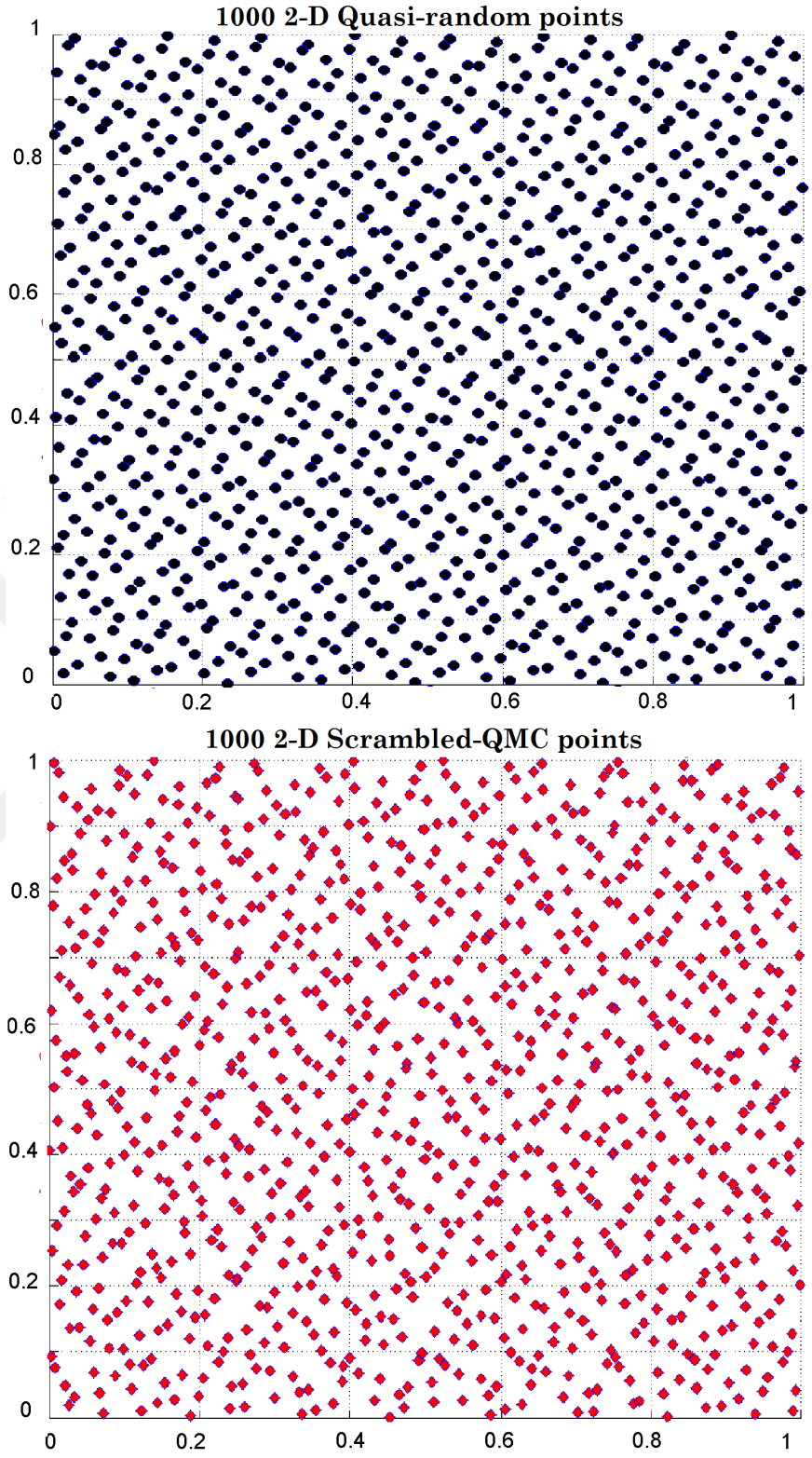

Figure 4.24. 2-D projections for Quasi-random numbers and Scrambled Quasi-random numbers.

$$\widehat{Y} = \frac{1}{M}\sum_{j=1}^{M} Y^{(j)} \tag{4.32}$$

The error of numerical integration is estimated using the variance of the evaluated yield values, which is calculated as

$$\widehat{\sigma}^2 = \frac{1}{M(M-1)}\sum_{j=1}^{M}(Y^{(j)} - \widehat{Y})^2 \tag{4.33}$$

Finally, the magnitude of the QMC error is

$$|E_{QMC}| = \widehat{\sigma}.\Phi^{-1}(\frac{1+p}{2}) \tag{4.34}$$

with user defined probability p, where Φ is the standard normal cumulative function.

4.6. Adaptive Sized Scrambled Quasi Monte Carlo-based Yield-aware Analog Circuit Synthesis

In this section, a novel yield-aware analog circuit tool is introduced and explained in detail, where both adaptive sample sizing mechanism and randomizing QMC approaches are combined to maintain the efficiency with providing reliability of the yield estimation. The flow chart of the developed tool is given in Figure 4.25, where the flow is enumerated for better understanding.

4.6.1. Description of the Developed Tool

Actually, most of blocks are the same with the QMC-based tool, so they are not discussed in detail in this section for the sake of conciseness. Initially, optimization variables such as design parameters (circuit netlist), upper and lower bounds of design parameters, and electrical constraints are defined and given to the optimizer.

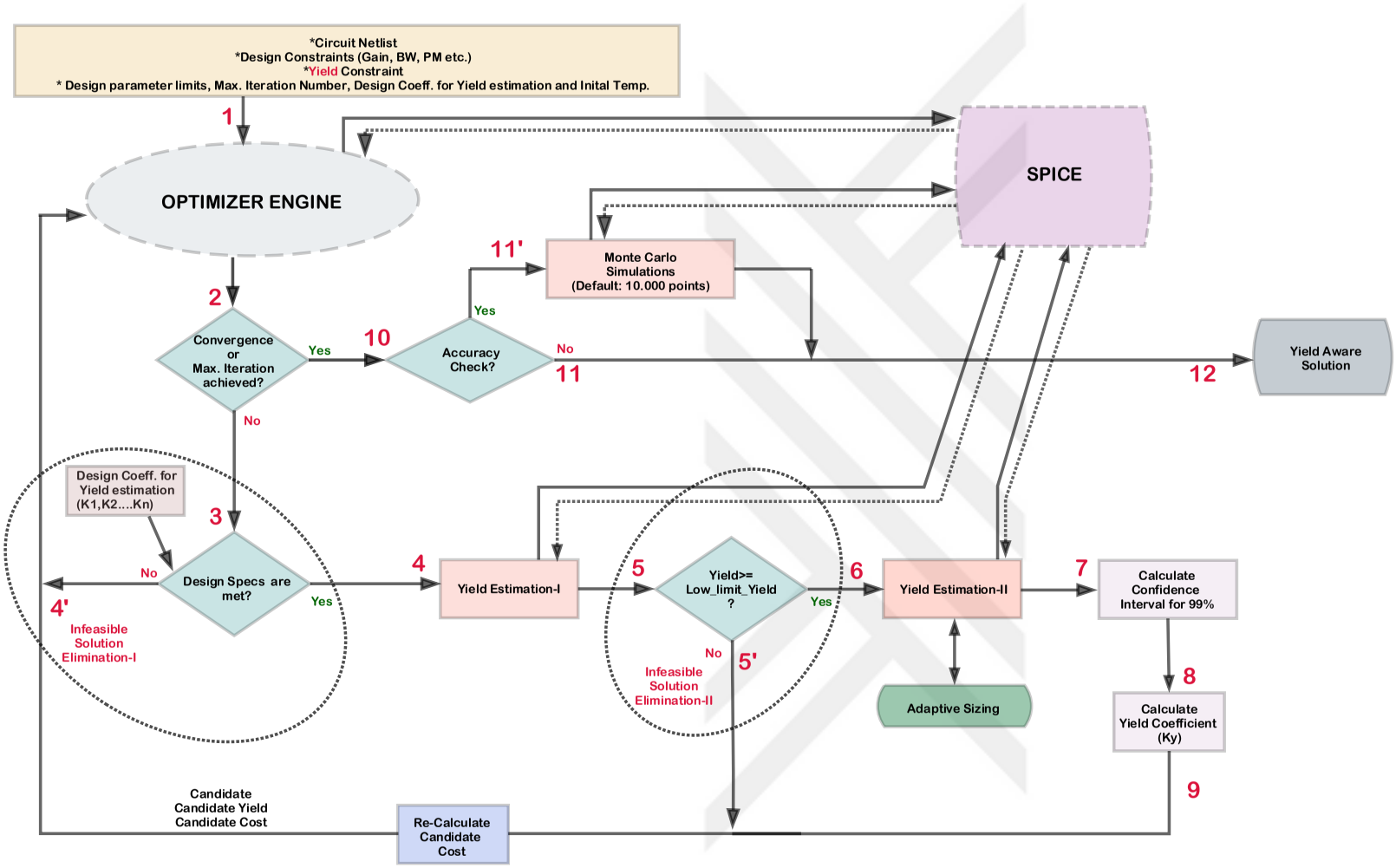

Figure 4.25. Flow chart of the proposed tool.

In addition to these variables, yield constraint, design coefficients for infeasible solution elimination, step size for adaptive sizing, and maximum dimension for the variability analysis are also defined by the user. Then, the optimization starts and operates as explained in Section 3 until a solution exists in the acceptance region. The acceptance region determines the feasibility space for a certain circuit according to the design constraints.

The first phase of the yield analysis is carried out on solutions satisfying the acceptance region criteria, which are applied as illustrated in Figure 4.19. At the end of the first yield analysis part, a rough idea about the yield of the candidate is obtained. Therefore, the sample size of the variability simulation is kept relatively small for this part to save the computation time. Scrambled-QMC is utilized during the variability simulations. Then, a second ISE is carried out depending on these rough estimations. Thus, redundant simulations for solutions having low yield values are avoided, which also compensates time loss due to multiple yield estimations. A further yield analysis is performed for each candidates that satisfies also the second ISE. In the second yield analysis part, scrambled-QMC approach is again used to sample the uncertain design space. Moreover, the adaptive sizing mechanism that was explained in Section 4.3.5 is employed to enhance the synthesis time without loss of accuracy. Variability analysis that was held in the first phase is just expanded and simulations are not renewed for the initial samples. Since scrambled-QMC includes a stochastic behavior in itself, a randomness occurs for each step during the adaptive sizing; thus, a number of different yield estimations is obtained, which are then used to calculate the error bounds. At the end of this part, a particular ranking is applied to the candidate and a new defined yield coefficient is calculated as

$$K_y = \frac{|Y_{best} - Y_{lower}| + \epsilon}{Y_{upper} - Y_{lower}} \tag{4.35}$$

where Y_{lower},Y_{upper} and, Y_{best} denote user defined yield constraints and the maximum bound of the current yield. The term ϵ is added to avoid zero cost value. The solution having a high yield value is assigned to minimum coefficient. Then, the cost of the

candidate solution is multiplied by the yield coefficient to reduce the cost of the solution with respect to its yield. This approach increases the probability of the selection of better individuals in terms of yield, thereby, orienting the population to find more robust solutions throughout evolution. During the cost calculation of yield, the lower limit is used rather than the estimated one; thus, guaranteeing that the yield of the solution is in the confidence interval. At the end of the synthesis, the user has the choice of an accurate yield estimation for the solution, where a large size of QMC is employed.

4.6.2. Synthesis Examples and Results

In this section, synthesis results of two different analog circuits (folded cascode OTA and basic two stage OTA) are provided and discussed. An Intel i7 4th generation chipset with 3.20 GHz processor was exploited during the synthesis process. The main algorithm is implemented on MATLAB®, and HSPICE is utilized for the performance evaluation. 130nm CMOS technology models are utilized during the synthesis of both circuits. Numbers of parents, offspring, and maximum number of iterations were chosen as 50, 50, and 200, respectively. The sample size for the first yield estimation part and the step size were selected as 100 and 20, respectively. Design coefficients for infeasible solution elimination were chosen as 0.95 for all electrical constraints and the yield. LDS sample sets for QMC are generated by using Sobol approach, where Owen's scrambling method proposed in [122] is employed for randomizing. The sample size for accuracy check analysis was determined 1000, where scrambled-QMC is utilized in this part. Both inter-die and intra-die variations are considered during the variability analysis, where variations in V_{th}, t_{ox}, W_{eff}, and L_{eff} are taken into account.

4.6.2.1. Two Stage Amplifier with Current Source. A basic two stage OTA given in Figure 4.26 was chosen as the first design example. The number of design parameters is determined as 24 (transistor dimensions, compensation capacitor, and the bias resistance) in this example, after the matching conditions are considered. The boundaries of design parameters and circuit variables are provided in Table 4.9.

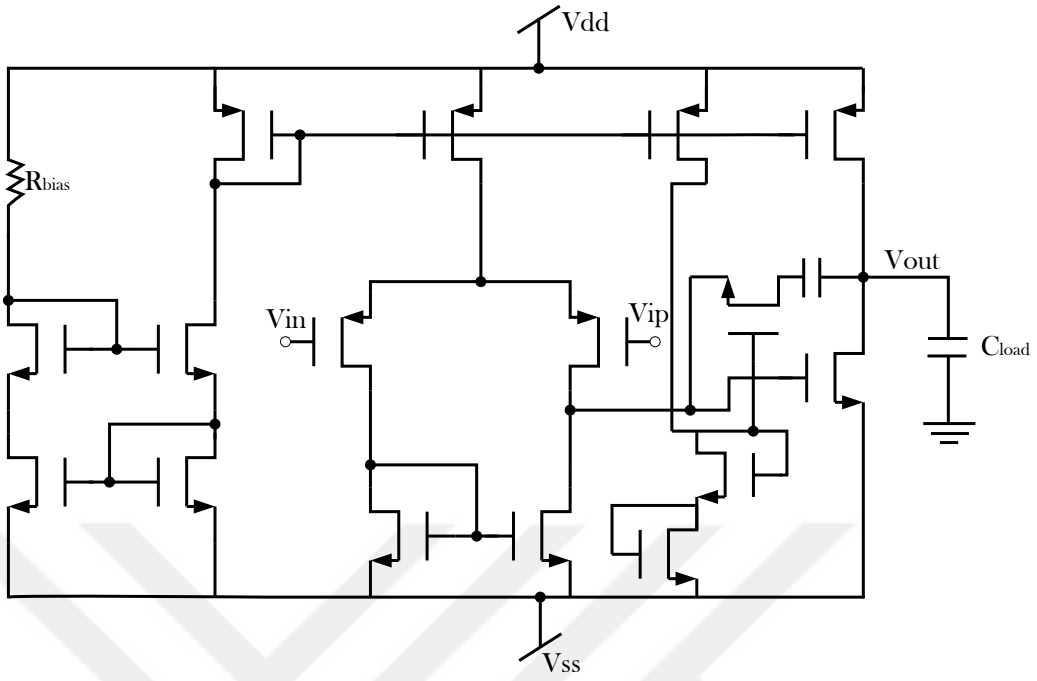

Figure 4.26. Schematic of two stage OTA circuit.

Table 4.10 represents synthesis results of the basic two stage OTA circuit for 5 independent runs. All electrical constraints and the yield are successfully met for every run. However, some violations occurred in the the power consumption and area occupation constraints, where the optimizer increases the power to satisfy the required phase margin. Thereby, the optimizer again applies the over-design approach, where power and area are generally sacrificed for the sake of the required yield. Sample size variates between 220-240. Confidence interval was calculated according to a probability of 99%. Since the optimizer takes the lower limit of the confidence interval into account, all yield values exist in the confidence interval. The maximum estimation error is found as 0.68% after an accurate yield estimation performed with 1000 samples. Synthesis time values are given in the last column, where the average time is found 97.5 minutes. The synthesis time is directly proportional to the number of individuals found in the acceptance region, where variability analysis is called for each individual. As a result, the overall synthesis time differs for each run. If the acceptance region coefficients are chosen as 0.9, yield of solutions increase to 100 %, whereas choosing the coefficients as to be 0.99, the average yield dramatically decreases to 88.2%.

Table 4.9. Design boundaries and variables for two stage OTA.

Transistor Width $[\mu m]$	Transistor Length $[\mu m]$	R_{bias} $[\Omega]$	C_{com} $[pF]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
0.65-135	0.13-13	50-1000	0.1-50	1.2	0	1

Table 4.10. Synthesis results of 5 independent runs for yield aware and nominal optimization.

	BW (kHz) $> 10kHz$	Gain $> 70dB$	PM $> 60^o$	Power $< 1.5mW$	Area $< 6000\mu m^2$	$Yield_{est.}$ $> 80\%$	N_{sample} —	$Yield_{exact}$ $> 80\%$	Confidence Interval	Error (%)	Synthesis Time (min.)
1	9.8	67.5	57	1.6	6390	97.46	220	98.01	$96.4 \leq x \leq 99.1$	0.55	133
2	9.5	72.6	56	1.3	5680	98.53	240	98.72	$97.1 \leq x \leq 99.2$	0.19	86
3	10.4	69.2	58	1.7	5840	99.02	240	99.51	$96.1 \leq x \leq 98.9$	0.49	87
4	9.7	71.5	58	1.5	5870	98.04	240	98.72	$97.4 \leq x \leq 99.8$	0.68	107
5	11.1	68.7	67	1.4	6030	98.7	220	98.2	$98.4 \leq x \leq 99.2$	0.5	122
N	11.6	70.8	61	0.43	2240	—	—	73.74	—	—	22.6

4.6.2.2. Folded Cascode OTA with Current Source. The second implementation example is a folded cascode OTA circuit whose schematic is given in Figure 4.27. Circuit variables and search space boundaries for design parameters are given in Table 4.11. Synthesis results of folded cascode OTA circuit for 5 independent runs are summarized

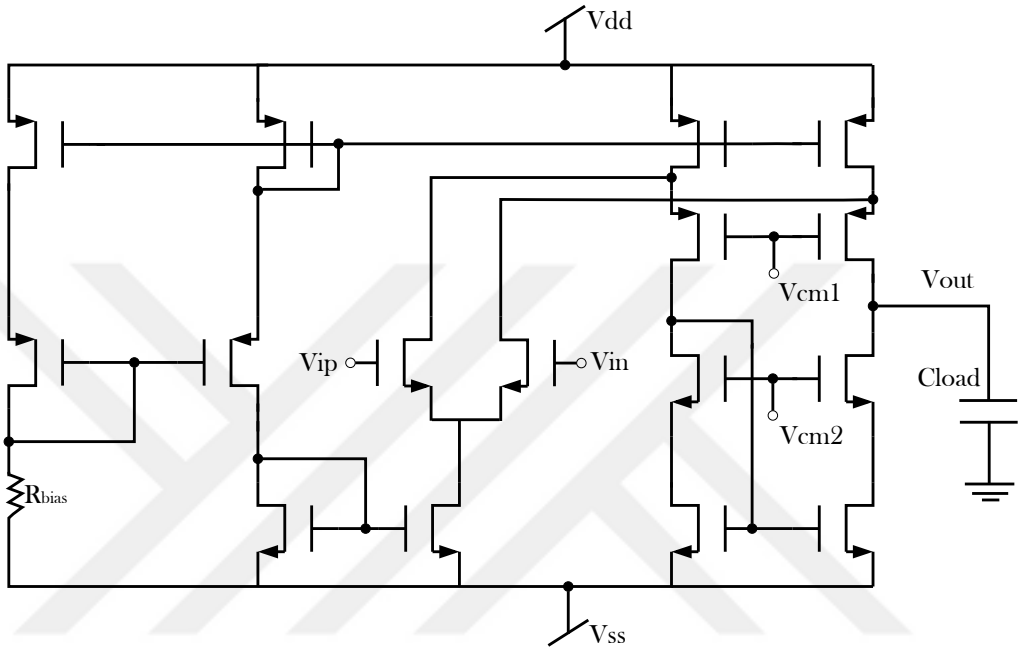

Figure 4.27. Schematic of folded cascode OTA circuit.

in Table 4.12. As seen from the table, all electrical constraints and the yield are satisfied for each run, except violations in the the power consumption and area occupation. The possible reason of these violations can be overdesign, where the particular yield ranking becomes dominant among the other constraints and the optimizer is more focused on the yield to satisfy the yield objective. The confidence interval ($\pm$) values are obtained assuming the yield of the solution would exist in the interval with the probability of 99%. Sample size variates between 220-240 and the maximum estimation error is found 0.36% for 5 different runs. In the last column, synthesis times values are given, which has an average value of 99.4 minutes, where the reason of the time difference between different runs is the number of candidate solutions during synthesis process.

Table 4.11. Design boundaries and variables for folded cascode OTA.

Transistor Width $[\mu m]$	Transistor Length $[\mu m]$	R_{bias} $[\Omega]$	V_{cm1} $[V]$	V_{cm2} $[V]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
0.65-135	0.13-13	500-10000	0.4-0.8	0.4-0.8	1.2	0	1

Table 4.12. Synthesis results of 5 independent runs for yield aware and standard optimization.

	BW (kHz) $> 10kHz$	Gain $> 70dB$	PM $> 60^o$	Power $< 1mW$	Area $< 6000\mu m^2$	$Yield_{est.}$ $> 80\%$	N_{sample} —	$Yield_{exact}$ $> 80\%$	Confidence Interval	Error (%)	Synthesis Time (min.)
1	9.5	69.2	68	0.77	5960	98.9	220	98.84	$96.2 \leq x \leq 99.8$	0.06	120.4
2	10.5	72	67	1.05	5750	97.8	240	98.16	$97.2 \leq x \leq 99.4$	0.36	77.4
3	10.1	69.8	68	0.69	6940	99.1	200	99.2	$98.2 \leq x \leq 100$	0.1	84.5
4	9.8	67.8	69	1.1	5316	98.9	220	99.10	$98.2 \leq x \leq 99.2$	0.2	92.8
5	9.95	70	70	0.88	5998	98.25	220	98.41	$98.1 \leq x \leq 99.6$	0.16	122.3
N	12	73	72	0.29	2390	—	—	75.4	—	—	22.2

4.7. VLSI Implementation

To verify the results of adaptively sized scrambled QMC-based yield aware analog circuit synthesis tool on silicon, a test chip was designed as explained in Section A.2. There are five major blocks in the chip; control unit, two stage OTA, folded cascode OTA, comparator, and RF blocks which are shown in Figure 4.28. Actually, two stage and folded cascode OTA, and comparator circuits were synthesized via the developed tool and synthesis results are provided in Section A.2. In these blocks, four different solutions were implemented for each block, where each of those includes four identical circuits. Consequently, each design is represented by 16 circuits in total. For OTA circuits, gain, bandwidth, and phase margin were determined as constraints. On the other hand, input sensitivity was determined as the constraint for the comparator circuit. Therefore, test chip measurements were designed to observe these specifications.

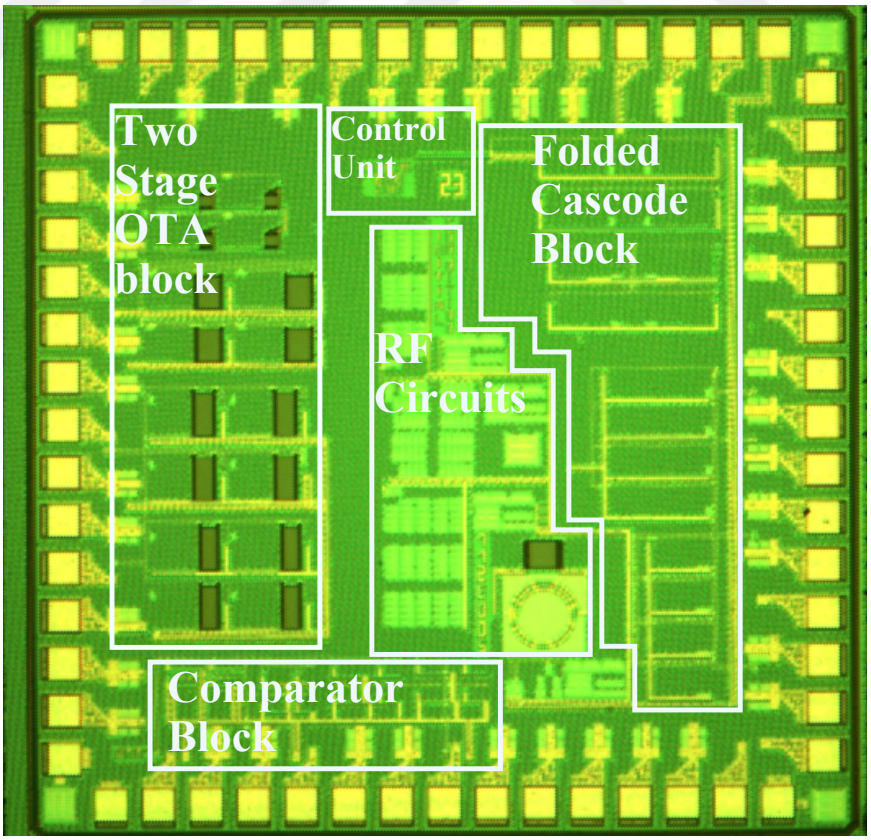

Figure 4.28. A microscopic photograph of the second schip.

Typically, measuring the open-loop gain is highly difficult in open-loop configuration due to stability problems. In addition to that, even very small offset voltage between the inputs nodes lead to either pulling-down or pushing-up of the output node. Therefore, the measurements were carried out in closed-loop configuration with unity feedback. The measurement strategy is based on measuring the difference between input and output nodes, and calculating the open loop gain according to

$$A_0 = \frac{V_{out}/V_{in}}{1 - V_{out}/V_{in}} \tag{4.36}$$

Since the open loop gain is not infinite, there is always a difference between the input and output nodes. By precisely measuring this difference at low frequencies, the open-loop gain can be extracted. On the other hand, to observe the 3 dB frequencies these obtained open loop gain values can be used. Namely, considering the gain-bandwidth graph of an amplifier, every factor-of-ten increase in frequency, the gain decreases by 20 dB after the 3 dB point. By considering this, the output voltage for the -23 dB point can be calculated by using the obtained open loop gain, and this point is practically obtained by sweeping the frequency. At last, by dividing this frequency by 10, the 3 dB frequency can be extracted. A photograph of the measurement setup is given in Figure 4.29. To measure the signal amplitudes precisely, a 5.5 digit multimeter was utilized, meanwhile amplifier output was observed by using a oscilloscope. A power board proposed in [125] was used and supplied by batteries rather than a power supply, to avoid any power supply induced distortion.

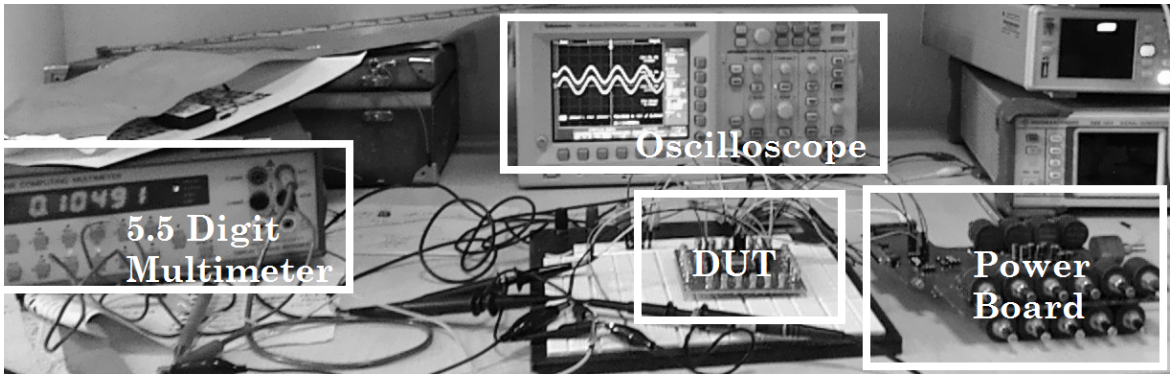

Figure 4.29. Test chip setup.

During measurements, 10 different chips were characterized for each circuit topology. Considering OTA circuits, design constraints were determined according to the post simulation results given in Table A.1 and Table A.2, respectively. According to post-simulation results of two stage OTA circuit, the average values for gain and 3dB bandwidth were approximately found 9.2 kHz and 71 dB and corresponding acceptance region values were determined as 8.75 and 67.5 by keeping the corresponding acceptance region coefficient to be 0.95, respectively. In addition to gain and bandwidth, phase margin was the other design constraint, but it is quite difficult to measure the phase margin. Therefore, amplifier output offset voltages were measured and taken into account during the yield estimation, where phase margin was just observed to be sure stability of the amplifier during measurements. Measurement results of two stage amplifiers are given in Table 4.7.

Table 4.13. Two stage OTA measurement results.

	Gain (dB)		BW (kHz)		Offset (V)		Yield (%)			Sample Size
Block	μ	σ	μ	σ	μ	σ	%90	%95	%99	—
1	70.1	1.8	10.7	1.4	1.6	0.25	100	97.5	87.5	40
2	71.4	2.5	10.4	1.3	0.7	0.1	100	100	90	40
3	73.5	2.3	8.9	1.1	0.95	0.15	100	97.5	87.5	40
4	72.5	1.6	9.2	1.6	0.7	0.15	100	97.5	85	40
Total	71.8	2.25	9.8	1.25	0.97	0.16	100	98.1	87.5	160

According to measurement results, the average yield was found to be 98.1%, where the average yield was approximately 98.6% according to the simulation results. Furthermore, the yield value was found to 100% when the acceptance region is determined as 90% of the actual values. On the other hand, if acceptance region coefficients are chosen as 99%, the yield value decreases to 87.5%.

Measurement results of folded cascode circuits are given in Table 4.7, where yield values were calculated for three different acceptance regions (90%, 95%, and 99%). The average yield was found to be 97.5% for this circuit, where it was almost 98.2% in simulation. The yield value increases to be 100% when the acceptance region is relaxed as 90% of the actual values. On the other hand, if acceptance region coefficients are chosen as 99%, the yield value decreases to 87.5%.

Table 4.14. Folded Cascode OTA Measurement Results.

	Gain (dB)		BW (kHz)		Offset (V)		Yield (%)			Sample Size
Block	μ	σ	μ	σ	μ	σ	%90	%95	%99	—
1	69.8	1.4	10.3	0.7	0.65	0.1	100	95	82.5	40
2	71.7	1.1	16.4	0.8	0.55	0.1	100	100	92.5	40
3	75.6	2.1	10.1	0.6	0.7	0.08	100	97.5	90	40
4	71.8	1	15.6	0.8	0.65	0.15	100	97.5	85	40
Total	72.2	1.4	13.1	0.75	0.65	0.1	100	97.5	87.5	160

Actually, measurement for comparators were also carried out, but the desired input sensitivity was not achieved for any chip. Therefore, results are not reported in this section. One possible reason of that dynamic input offset, where it is always challenging to analytically predict the input-referred random offset voltages since the operating points of transistors are time varying. During synthesis, input sensitivities were measured within a static manner, which may result in wrong prediction and evaluation during the synthesis. RF circuit block were not measured and reported in this thesis.

4.8. Conclusion

To incorporate the variability analysis into the conventional optimization problem and synthesize robust solutions against the variation phenomenon, a number of

different variation-aware analog circuit synthesis tools are introduced in this chapter, where mainly two different variability analyses were utilized: sensitivity-based and MC-based.

In sensitivity-based variation-aware circuit synthesis, two different approaches are proposed, which are over-design and robust-design approaches. Over-design approach promises reliable solutions by choosing the design point beyond the design objective limits; thus, a solution can still satisfy the design constraints despite variability. However, power consumption and chip area are sacrificed for the sake of reliability. On the other hand, robust-design approach based on minimizing variation in design constraints and promises solutions consuming less power and occupying smaller area compared to the over-design approach. However, there is no guarantee of finding a reliable solution for all circuits, which is a quite difficult problem in comparison to the over-design approach. The success rate of the approach is considerably lower than the over-design approach. The synthesis time is apparently longer compared to over-design since more iterations are proceeded for the robust solution.

In MC-based variation-aware circuit synthesis, two different enhanced sampling techniques are utilized for variability analysis: QMC and scrambled QMC, where utilized variation model parameters were extracted via characterization of a test chip. At first, a QMC-based variability analysis with adaptive sample sizing and automated stopping criterion for yield aware analog circuit optimization is proposed. Thanks to the deterministic property of the QMC, sampling can be performed iteratively without repeating the previous sample calculations. Moreover, an ISE method is also utilized to increase the efficiency of the optimizer, in which redundant simulations for infeasible solutions are not carried out. The developed tool also includes an optional module, in which a pre-determined simulation budget is shared among the candidate solutions with respect to their yield in order to obtain more accurate yield estimation. On the other hand, the major disadvantage of the conventional QMC is that the error of the estimated yield cannot be determined in any practical way. To palliate this problem, scrambled-QMC is utilized, where QMC samples are randomized by reordering of the samples (scrambling). To keep the efficiency, the developed tool uses

a two-step yield estimation and two different types of ISE during the optimization loop. The first ISE is assigned to eliminate the low performing solutions. Then, a rough yield estimation is performed via a relatively small sized scrambled QMC. The second ISE is assigned to avoid redundant simulations for candidate solutions with low yield values. In the second step of yield estimation, an expanded yield analysis is carried out for promising solutions, where the adaptive sizing algorithm is combined with scrambled QMC in order to determine a suitable sample size. Thanks to two-step yield estimation and ISE, the efficiency of the whole system is substantially increased while maintaining estimation reliability. Synthesis results indicate that the common trend for the developed tools is overdesign, where area and power are sacrificed to achieve high yields. Furthermore, to verify the synthesis results on silicon, measurement results of a test chip are provided.

5. AGING-AWARE ANALOG CIRCUIT DESIGN AUTOMATION

The idea behind aging-aware circuit synthesis is similar to yield-aware synthesis, where the yield constraint is replaced by a lifetime constraint and aging simulations are utilized in order to estimate the lifetime. In contrast to variability, aging is a time-dependent process and aging analysis (modeling, simulating, and observing the aging effects) is relatively difficult to perform. The most relevant effect of aging is an increase in the threshold voltage; hence, a typical aging evaluation is based on simulating circuits while increasing the threshold voltage as a function of operation time. However, an accuracy problem manifests itself during aging simulations due to the model inaccuracy and time-dependency of the aging phenomenon. Therefore, accurate models are required for reliable aging analysis. Furthermore, considering a large number of iterations during the synthesis process, efficient simulation methodologies are also needed in order to reduce the synthesis time. A lifetime-aware analog circuit synthesis tool is introduced in this chapter, where the discussion starts with aging modeling and simulations and concludes by describing the developed tool. This developed tool is the first application of lifetime-aware analog circuit synthesis in the literature. This chapter is organized as follows. In Section 5.1, modeling of aging phenomena is discussed. Semi-empirical model development process is explained in Section 5.2. The developed aging simulator is introduced in Section 5.3. In Section 5.4 the proposed lifetime-aware analog circuit synthesis tool is introduced. Synthesis results are provided and the chapter is concluded in Section 5.5.

5.1. Aging Modeling

Although underlying mechanisms are quite different from each other, both HCI and NBTI manifest themselves as an increase in the threshold voltage V_{th} over time. Therefore, aging models are based on the estimation of the shift in the threshold voltage. Conventionally, analytical models and semi-empirical models have been utilized

to estimate the aging effects. Typically, an analytical model is developed by performing experiments on silicon for a certain technology and scaled for different technologies, so they are flexible to use for any technology. Since no measurement data are not used during the scaling process, these models are called "Predictive Models". However, these predictive models may cause accuracy problems, where scaling is a challenging process and such models suffer from severe prediction errors. On the other hand, semi-empirical models are developed based on aging experiments on silicon data, thus providing more reliable estimations for a given technology, where aging experiments should be re-performed and semi-empirical model parameters should be modified for each technology node. The scaling of devices down to the nm range results in deterministic models to be changed into stochastic models in order to include the aging effects in evaluation of the IC performances [126, 127]. Recently, stochastic modeling has become popular since the effect of aging becomes stochastic for technologies below $32nm$, where aging effects are modeled and simulated via stochastic analysis [128, 129]. A further discussion on aging models can be found in [127].

5.1.1. Analytical Aging Models

Analytical models have been developed for a certain technology and scaled for different technology nodes. Predictive Technology Modeling (PTM) models provided in [61] have been commonly utilized for HCI and NBTI in the literature. According to [46], HCI induced threshold voltage degradation is modeled as

$$\begin{aligned} \Delta V_{th} &= \frac{q}{C_{ox}} N_{it} \\ N_{it} &= K \sqrt{C_{ox}\left(V_{gs}-V_{th}\right)} exp\left(\frac{E_{ox}}{E_0}\right) exp\left(-\frac{\phi_{it}}{q\lambda \text{ш} E_m}\right) t^n \\ E_m &= \frac{V_{ds}-V_{dsat}}{l}, \quad V_{dsat} = \frac{\left(V_{gs}-V_{th}+2V_t\right) L_{eff} E_{sat}}{V_{gs}-V_{th}+2V_t+A_{bulk} L_{eff} E_{sat}} \end{aligned} \tag{5.1}$$

Here, t is time, N_{it} is the number of interface traps, φ is the barrier energy, and K, E_0, λ, α, m, and n are technology independent parameters, which are provided in Table 5.1.

Table 5.1. Technology independent model coefficients for HCI.

$K\ (nm/C^{0.5})$	$E_0\ (V/nm)$	A_{bulk}	$\phi_{it}\ (eV)$	$\lambda\ (nm)$	n	$L\ (nm)$	$E_{sat}\ (V/nm)$
$1.7e+8$	0.8	0.005	3.7	7.8	0.5	17	0.011

On the other hand, NBTI occurs in PMOS transistors and causes an increase in V_{th} as well as HCI. However, the major difference of NBTI compared to HCI is that NBTI has a partial recovery mechanism when the stress is removed. As as result, NBTI modeling is quite difficult, in which both dynamic and static operations should be taken into account as shown in Figure 5.1. The NBTI model proposed in [61] is

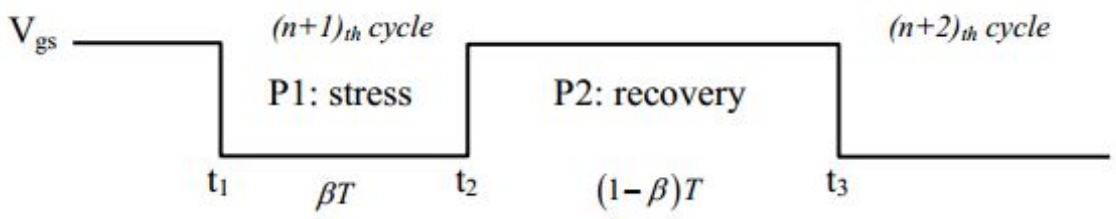

Figure 5.1. Stress and Recovery phases for NBTI.

given below:

$$\begin{aligned} &Stress\ Phase : t = (t_1, t_2) \\ &\qquad \Delta V_{th} = \sqrt{K_v^2.(t_2 - t_1)^{0.5} + \Delta V_{th1}} + \delta_v, \\ &Recovery\ Phase : t = (t_2, t_3) \\ &\qquad \Delta V_{th} = (\Delta V_{th2} - \delta_v)\left[1 - \sqrt{\eta.(t_3 - t_2)/t}\right] \end{aligned} \tag{5.2}$$

where,

$$K_v = A.t_{ox}.\sqrt{C_{ox}.(V_{gs} - V_{th})}.exp\left(\frac{E_{ox}}{E_0}\right)\left[1 - \frac{V_{ds}}{\alpha.(V_{gs} - V_{th})}\right].exp\left(-\frac{E_a}{k.T}\right) \tag{5.3}$$

$$E_{ox} = \frac{(V_{gs} - V_{th})}{t_{ox}} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

The NBTI model covers both recovery and stress phases for long term operation, where $\alpha,\ \eta,\ E_c, A, E_0$, and δ_v are technology independent parameters, which are listed in Table 5.2.

Table 5.2. Technology Independent model coefficients for BTI.

$A\ [mV/nm/C^{0.5}]$	1.8	α	1.3
$E_0\ [MV/cm]$	2.0	η	0.35
$E_a\ [eV]$	0.13	$\delta_v\ [mV]$	5.0

5.1.2. Semi Empirical Aging Models

During semi-empirical model development, it is not practical to perform aging experiments under nominal conditions, where tens of months (even years) are needed to observe the aging effects. Instead, the state of the art procedure is performing measurements under elevated temperature and voltages, which is called Accelerated Aging Test (AAT). It is a well-known fact that aging phenomena can be accelerated by increasing thermal and electrical stresses. Conventionally, AAT approaches utilize Arrhenius law based semi-empirical models [130–132], which consider temperature as a major acceleration factor during the measurements. According to the semi-empirical models, HCI and BTI degradations are typically modeled by a power law dependence on the stress time t as,

$$\begin{aligned} \Delta V_{th} &= f(V_{GS}, T, W, L)t^n e^{\frac{-E_a}{kT}} \\ \frac{\Delta I_d}{I_d} &= f(V_{DS}, T, W, L)t^n e^{\frac{-E_a}{kT}} \end{aligned} \tag{5.4}$$

The dominant source of the degradation is of course electrical stress on devices, but it also depends on absolute temperature (T), transistor dimensions (W, L), and time (t). Traditionally, AATs are carried out on some particular circuits, including differential amplifiers, comparators, and ring oscillators [133–135]. However, it is highly difficult to track the effect of aging on a circuit performance, where parameters of many devices can be changed due to aging. As a result, a comprehensive partitioning process is required in order to map individual contributions of devices on the total circuit performance degradation. This complicated partitioning process also limits the characterization accuracy due to imperfect correlation between circuit performances and device parameters.

5.2. Semi Empirical Model Development via Accelerated Aging Test

The other aim of the first chip, whose design process is explained in Section A.1, is developing semi-empirical aging models via AAT for 130nm technology. Semi-empirical equations for the threshold voltage degradation of PMOS due to NBTI and the drive current degradation for NMOS due to HCI are given in Equation 5.5.

$$\begin{aligned} \Delta V_{th} &= B.\left(V_{gs}\right)^{m_1}.e^{\frac{-E_a}{kT}}.L^{m_2}.W^{m_3}.t^{m_4} \\ \Delta I_d &= I_d.A.{V_{ds}}^{p_1}.e^{\frac{-E_a}{kT}}.L^{p_2}.t^{p_3} \end{aligned} \tag{5.5}$$

Here, time exponents m_4 and p_3 depend on the process and reported to be $0.19 - 0.25$ and 0.45 in [126, 136], respectively. Considering the NBTI model, t_{nom}, T_{nom}, t_{acc}, and T_{acc} are defined as the nominal and the accelerated variables for time (t) and temperature (T), thus, V_{th} degradation expressions for each case take the form,

$$\begin{aligned} \Delta V_{th(nom)} &= B.\left(V_{gs}\right)^{m_1}.e^{\frac{-E_a}{kT_{nom}}}.L^{m_2}.W^{m_3}.t_{nom}^{m_4} \\ \Delta V_{th(acc)} &= B.\left(V_{gs}\right)^{m_1}.e^{\frac{-E_a}{kT_{acc}}}.L^{m_2}.W^{m_3}.t_{acc}^{m_4} \end{aligned} \tag{5.6}$$

and the corresponding ratio is obtained as

$$\left(\frac{\Delta V_{th(nom)}}{\Delta V_{th(acc)}}\right) = e^{\frac{-E_a}{k}\left(\frac{1}{T_{nom}} - \frac{1}{T_{acc}}\right)}\left(\frac{t_{nom}}{t_{acc}}\right)^n \tag{5.7}$$

where E_a and k are equal to $0.15eV$ and $8.61x10^{-5}eVK^{-1}$, respectively. Using Equation 5.7, acceleration factor of AAT under high temperature (T_{factor}) can be calculated as,

$$T_{factor} = \frac{t_{nom}}{t_{acc}} = \sqrt[m4]{\frac{1}{e^{\frac{E_a}{k}(\frac{1}{T_{nom}} - \frac{1}{T_{acc}})}}} \tag{5.8}$$

To project 1 year of NBTI ($t_{nom} = 1y$) aging, the temperature for accelerated aging setup was chosen as $T_2 = 400K$. In this case, T_{factor} is found to be 1422, which corresponds to an accelerated aging duration of $7.03x10^{-4}$ years or 6.16 hours to emulate a 1 year nominal operation result.

Similarly, considering HCI effect on NMOS devices, the drive current degradation expressions become,

$$\begin{aligned} \frac{\Delta I_d}{I_d}_{nom} &= A.{V_{ds}}^{p_1}.e^{\frac{\Delta E}{kT_1}}.L^{p_2}.t_{nom}^{p_3} \\ \frac{\Delta I_d}{I_d}_{acc} &= A.{V_{ds}}^{p_1}.e^{\frac{\Delta E}{kT_2}}.L^{p_2}.t_{acc}^{p_3} \end{aligned} \tag{5.9}$$

where E_a, k, and t are equal to $0.15eV$, $8.61x10^{-5}eV/K^{-1}$, and 0.45, respectively. Assuming changes in I_d values are equal to each other , T_{factor} is found to be 25.25 for $t_{nom} = 1y$, $T_1 = 300K$, and $T_2 = 400K$, which corresponds an accelerated (t_{acc}) time of $12.2x10^{-3}y$ or $4.454d$ for HCI.

The measurement setup of the accelerated aging experiments is illustrated in Figure 5.2. A custom MTI EQ-DZF-6050 thermal furnace was utilized to expose the chip to thermal stress. Meanwhile, electrical stress was also applied to the chip using custom designed feedthrough pins of the oven. Selection inputs are controlled by switches, where pull-down resistors were located in order to avoid any high impedance nodes at the inputs. During experiments, saturation currents were measured by a high resolution ampermeter, where the measurement setup is given in Figure 5.3.

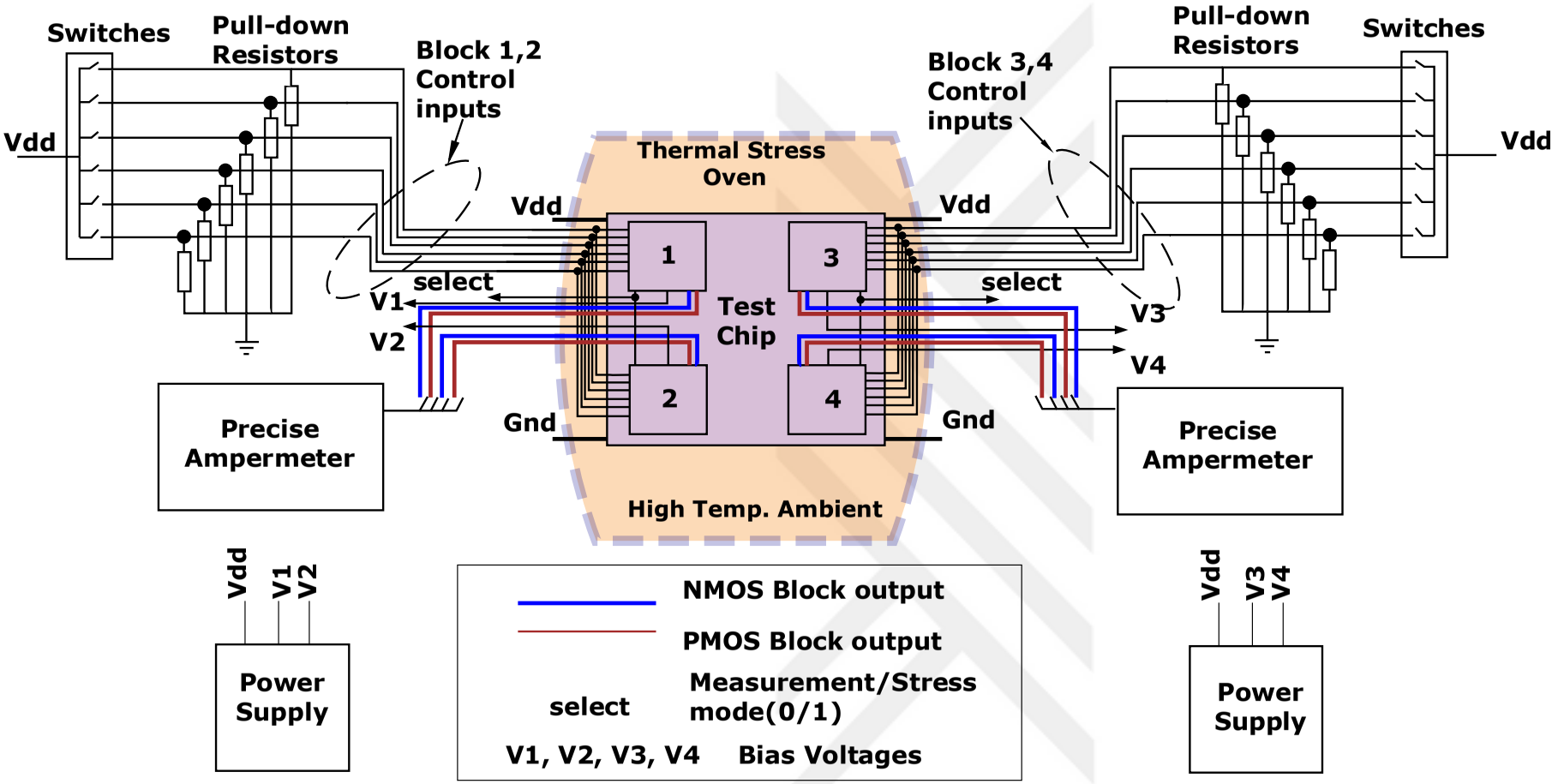

Figure 5.2. Accelerated aging measurement set-up.

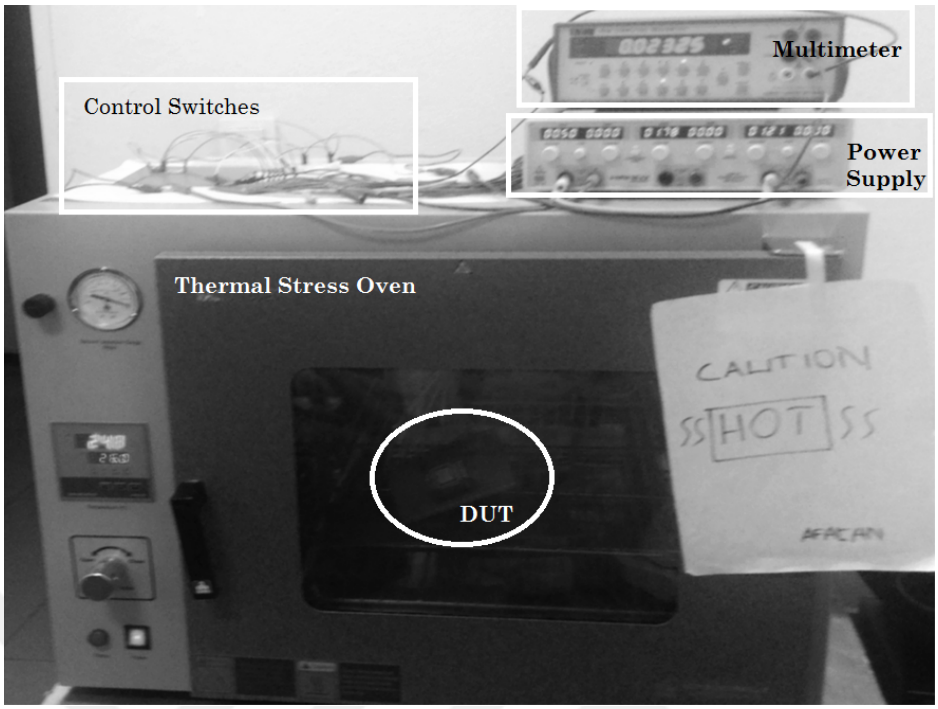

Figure 5.3. A photo of AAT measurement setup.

All transistors were individually characterized before the accelerated aging experiments in order to obtain parameters of the fresh transistors (threshold voltage and drain current). As previously calculated, PMOS devices were exposed to thermal ($400K$) and electrical stress ($V_{gs} < 0$), and current measurements were carried out when the ambient temperature reached the nominal value to ensure a permanent degradation. The average saturation current measurement results of the first 24 PMOS transistors for three different test chips are given in Figure 5.4. As expected, saturation current of an aged transistor reduces due to the increase in V_{th}. Corresponding threshold voltage results are given in Figure 5.5. According to the measurement results, the first 8 transistors having the shortest channels age more. On the other hand, considering devices having the same length with different width values, it can be concluded that device width does not play a consistent role during BTI degradation. Another observation is that aging shows a saturated power-law behavior, where degradation amount becomes smaller over time. This is because of the decreased number of dangling bonds, which are capable of trapping charges at the channel.

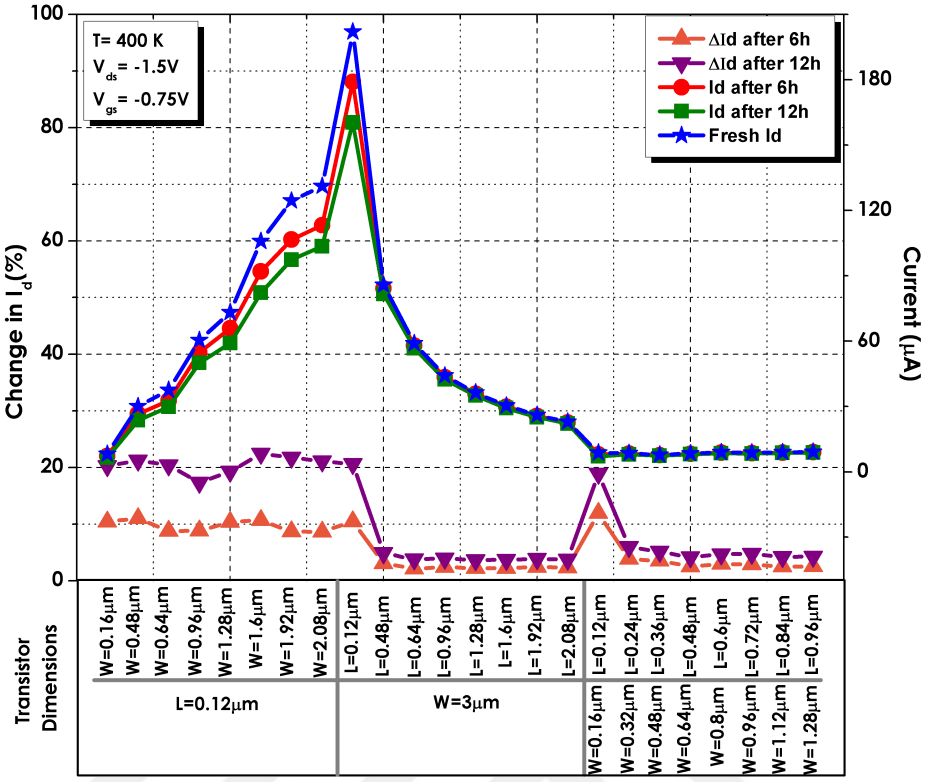

Figure 5.4. Measurement results of transistor I_d's.

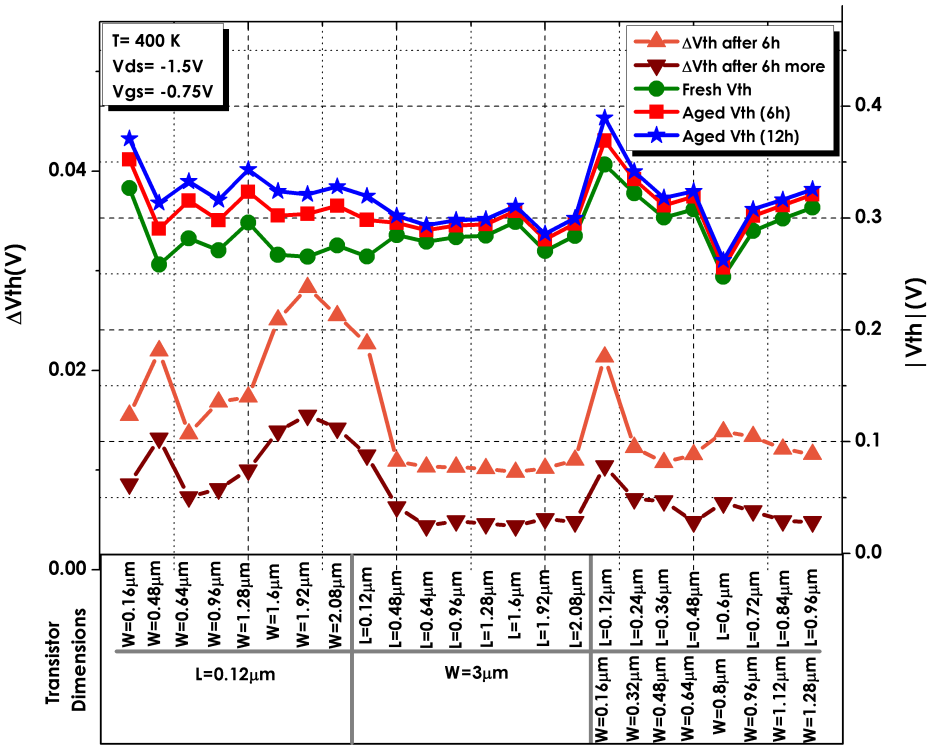

Figure 5.5. Measurement results of transistor V_{th}'s.

To extract the technology dependent parameters in the semi-empirical model, a curve fitting program was utilized. After fitting, NBTI model takes the form

$$\Delta V_{th} = B.(\mid V_{gs} \mid)^{m_1} .e^{\frac{-E_a}{kT}}.(m_2 L^{m_3} + m_4).W^{m_5}.t^{m_6} \tag{5.10}$$

Contrary to the other parameters, a second order model was used for the channel length to obtain a better fitting, where the fitting result is given in the Figure 5.6. Extracted technology dependent parameters for a $130nm$ technology are given in Table 5.3.

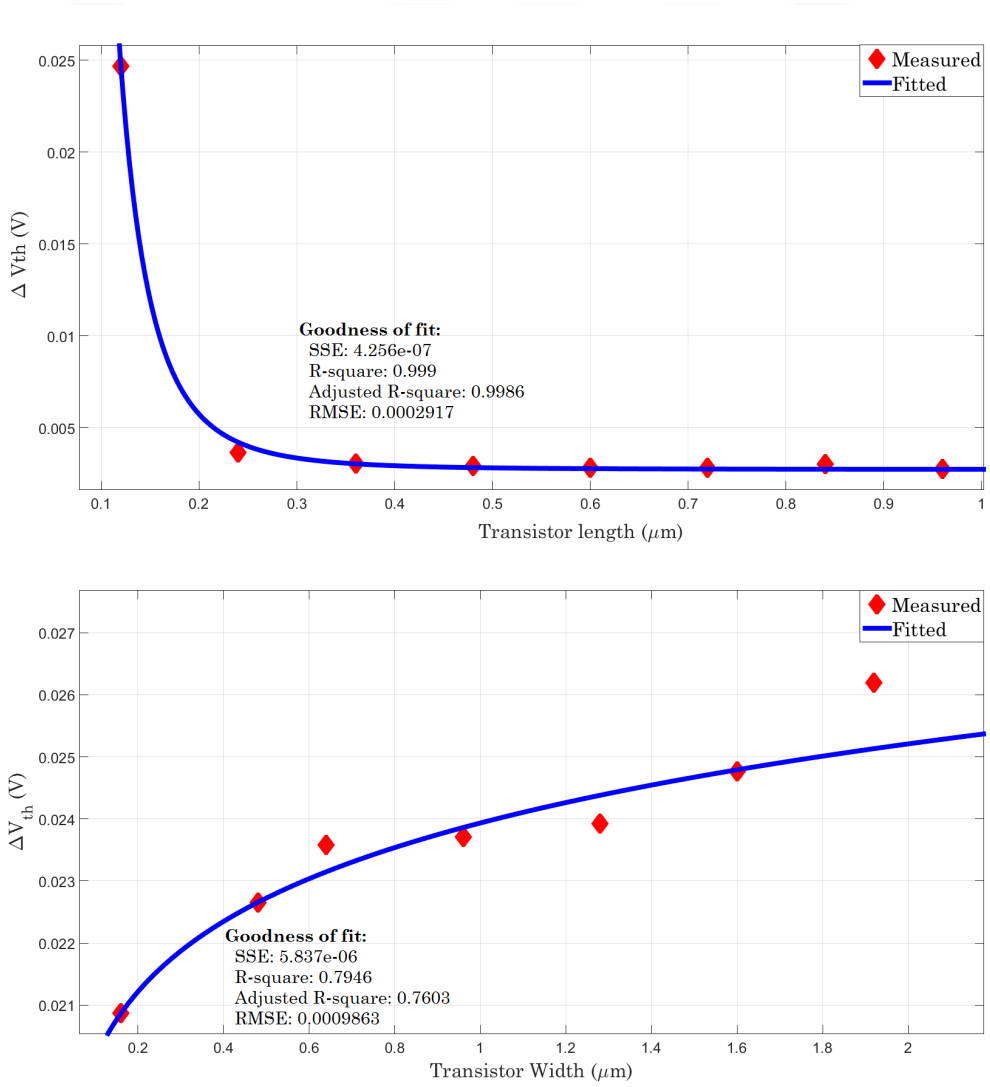

Figure 5.6. Fitting results of the transitor dimesions.

Table 5.3. Extracted technology dependent coefficents of NBTI model.

B	$m1$	$m2$	$m3$	$m4$	$m5$	$m6$
3.6457	2.175	$6.964e-7$	-4.872	0.0026	0.04318	0.25

All coefficients were extracted from the fitted data, except for the time exponent (m_6), which is kept constant at 0.25. As expected, increasing the electrical stress causes more degradation in V_{th}. Furthermore, increasing the channel length substantially reduces the threshold voltage degradation. Experiments demonstrate that transistor width does not affect aging, as confirmed by the value of m_5 in Equation 5.10. Therefore, the model can be modified by removing the channel width term. To validate the developed models, aging estimations were carried out for 2 years operation period under nominal temperature, where electrical stress is kept constant, and results are given in Figure 5.7.

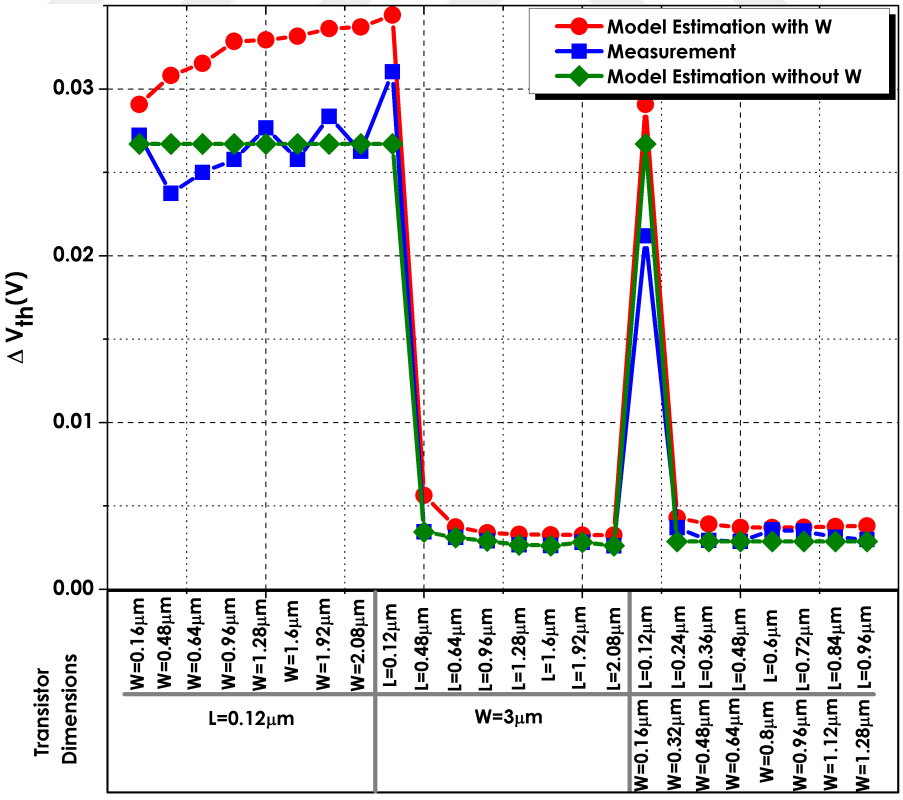

Figure 5.7. Comparison of model estimation and measurement results.

As seen from the results, both models are quite accurate to be used for NBTI estimations. The only difference stems from the channel width term, where the former model assumes that the wider devices degrade more, which creates a pessimistic trend in the estimation. On the other hand, estimates provided by the modified model are better correlated with measurements, since it does not take channel width into account. Similarly, NMOS devices were exposed to both electrical and thermal stress as desired by HCI stress conditions (high V_{ds} at elevated temperature). However, no considerable aging effect has been observed after AAT experiments. The possible reason may be that impact ionization, which is the major contributor of HCI, has a negligible effect 130nm technology, where the channel is still too long for HCI.

5.3. A Deterministic Aging Simulator Tool with Adjustable Step Size

Both mechanisms (HCI and NBTI) cause an increase in V_{th} of MOS devices, which leads to a change in operating conditions of a circuit over time. Therefore, aging simulations depend on including this time dependent change into the circuit evaluation. One should consider that as circuit ages, operating points also change over time due to the change of electrical stress on transistors. Therefore, performing long-term reliability simulations within a single and long step may cause prediction errors. To overcome this problem, some commercial tools such as MOSRA (Synopsys), UDRM (Mentor), and RelXpert (Cadence) divide the total simulation time into sub-periods by a certain number of steps, and partial simulations are carried out. Hence, substantial changes in the stress amount on devices can be captured, and are taken into account during the calculation of parameter shifts for the next step, as depicted in Figure 5.8.

Nevertheless, these tools also have some disadvantages. Firstly, such tools generally utilize low level aging models, which may lead to accuracy problems. In addition to that, using a static step size during long-term simulations can cause either inaccuracy or inefficiency. Namely, keeping the step size relatively small results in expensive simulation workload, whereas the use of larger steps may cause estimation errors.

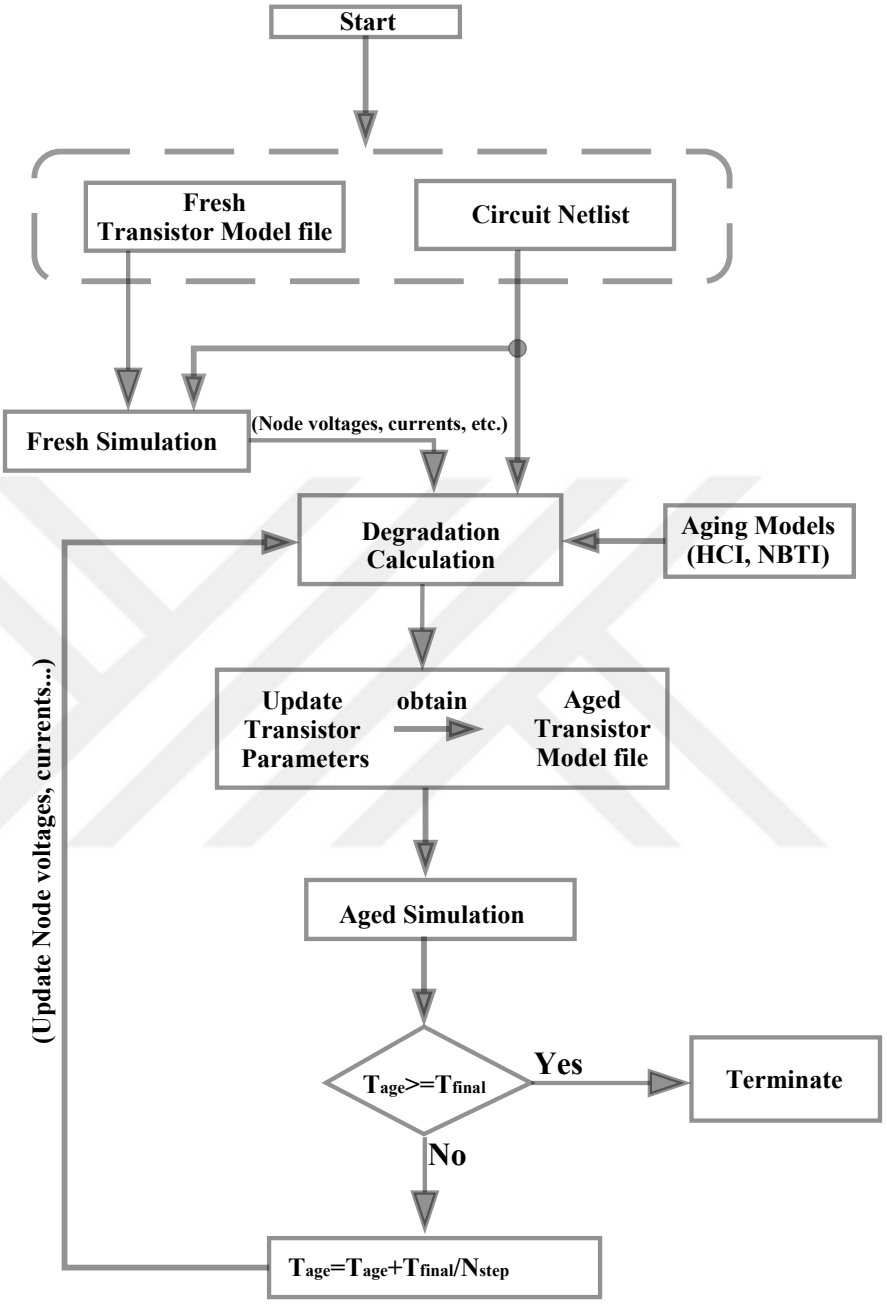

Figure 5.8. A general flow for aging simulation.

Especially, considering numerous evaluations of candidate circuits during optimization, efficient reliability simulations become vital to reduce the total synthesis time. Consequently, a dynamic step size (rather than a static one) would be better.

To deal with the bottleneck of available aging simulators, a novel spice-based simulator with adjustable step size is developed, where adjustable step size procedure is visually illustrated in Figure 5.9.

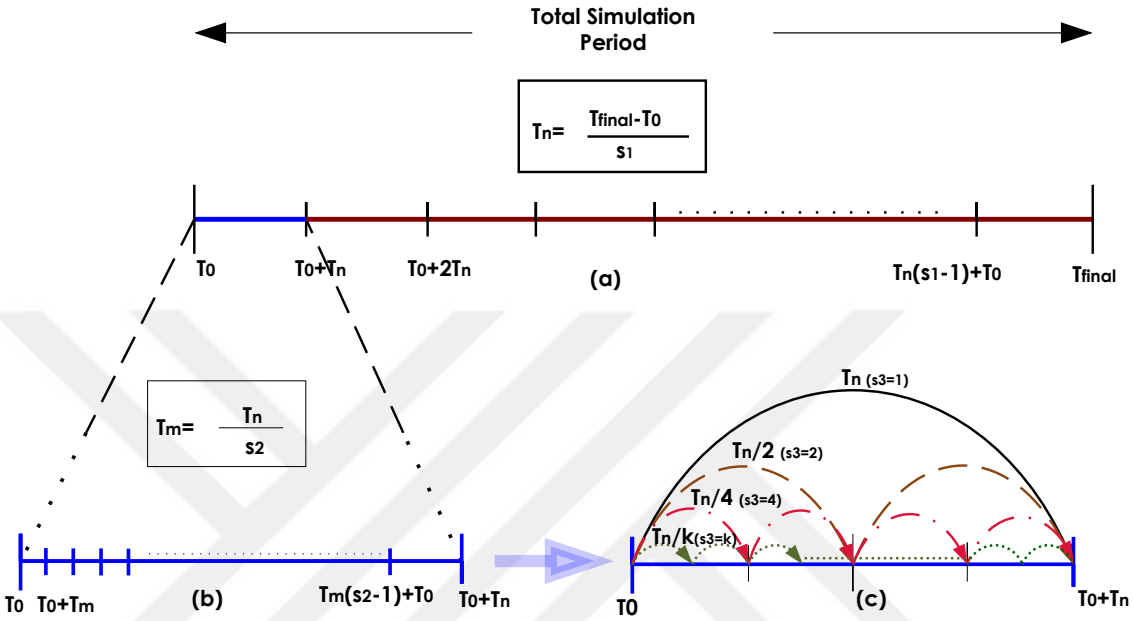

Figure 5.9. Determination of the step count for aging simulation.

The main idea behind the approach is based on the saturated power-law behavior of aging mechanisms, where a large portion of the degradation occurs during the initial phase of aging due to decreasing number of generation of interface states over time. In this context, the total simulation time $(T_{final} - T_0)$ is first split into equal time intervals by using a certain number of steps (s_1) as shown in Figure 5.9(a). Then, an aging simulation is carried out for the first period $(T_0 - T_0 + T_n)$, using a relatively large number of steps (s_2), as depicted in Figure 5.9(b). Meanwhile, the same simulation is performed by using a considerably fewer step count (i.e. $s_3 = 2$) as shown in Figure 5.9(c). Then, an absolute error is calculated using

$$E = \sum_{i=1}^{j} |\Delta V_{th(j,accurate)} - \Delta V_{th(j,adaptive)}| \tag{5.11}$$

where j, $\Delta V_{th(j,accurate)}$, and $\Delta V_{th(j,adaptive)}$ denote the number of transistors and degradation amounts of the first and the second simulations, respectively. If this error value is greater than the pre-determined tolerance value, the second simulation is re-run by increasing the step count. This procedure is repeated until the absolute error becomes either equal to or lower than the tolerance value. When the target error level is reached, the present value of the step count (s_3) is used to determine the simulation step count for the remaining part of the analysis, which is calculated as

$$s_{final} = s_3 \left(\frac{T_{final}}{T_n} \right) \tag{5.12}$$

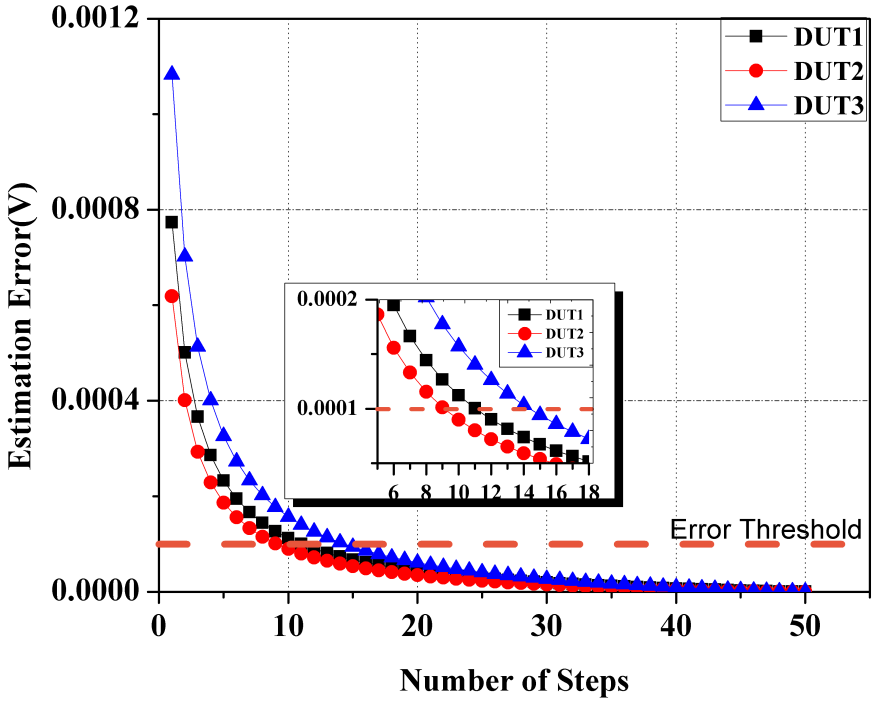

Figure 5.10. Estimation error vs simulation step count.

To demonstrate the advantage of the step count concept, three different solutions for an amplifier circuit were simulated by using different numbers of steps and results are given in Figure 5.10. The total simulation time, the accurate step count, and the error threshold values were determined as 1 $year$, 100 steps, and $0.1mV$, respectively. As can be seen from the results, the estimation error diminishes at the beginning and settles after a certain number of steps for each solution, where efficient step-counts were determined as 10, 12, and 15, respectively. Moreover, a lifetime simulation (10

years) was also run for each solution by using the determined step counts (100, 120, and 150) and results are given in Figure 5.11. Simulations took 34, 41, and 50 seconds, respectively. Again, an accurate simulation was performed by using a large value for step count (1000), which took almost 350 seconds. Estimation errors in the $3dB$ bandwidth were calculated for each solution. The maximum estimation error was found as $0.7Hz$, which corresponds a 0.08% error in the bandwidth. Furthermore, these circuits were also simulated by using a considerably lower step count (s=2). Even though the simulation took 0.7 seconds, estimation errors of these simulations were found to be 950 Hz, 730 Hz, and 510 Hz, respectively.

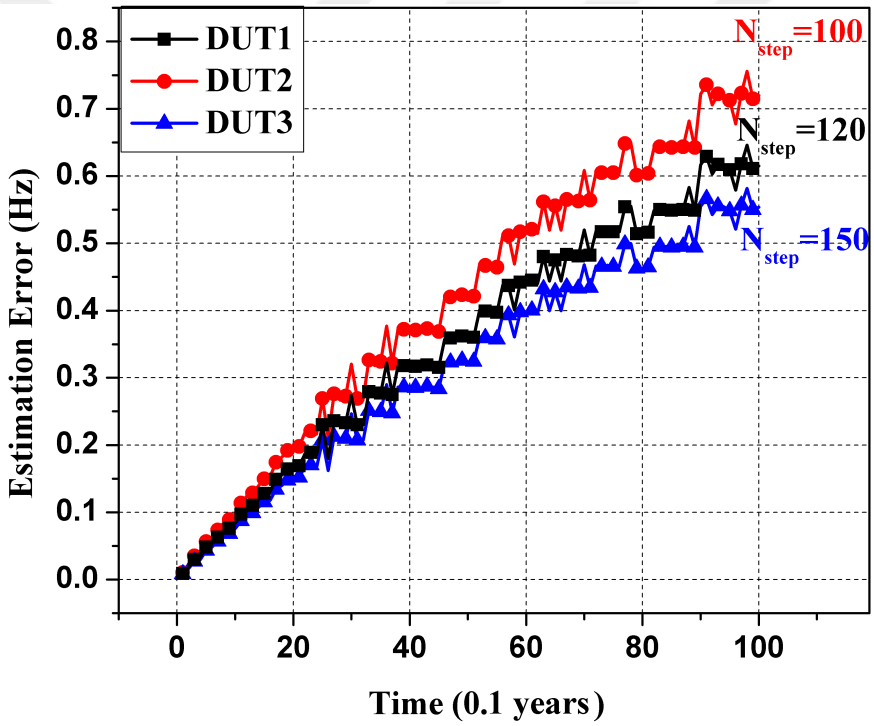

Figure 5.11. Estimation errors in the bandwidth for different solutions.

5.4. Lifetime-aware Analog Circuit Synthesis Tool

To develop a lifetime-aware analog circuit synthesis tool, the developed aging simulator was combined with the single objective analog circuit optimization tool as well as yield-aware circuit synthesis. Contrary to yield-aware tool, a lifetime constraint is defined as a new constraint and included in the objective minimization problem. The general flow of the developed tool is presented in Figure 5.12.

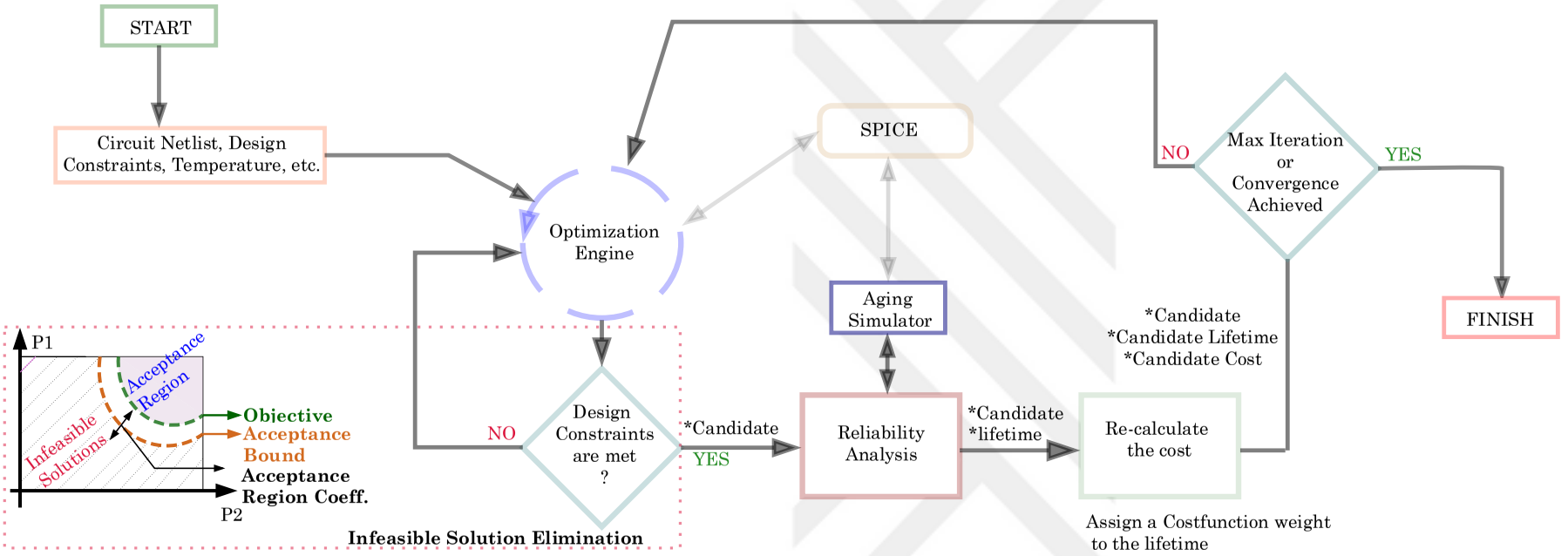

Figure 5.12. Flow diagram of the proposed tool.

Infeasible solution elimination, which is based on pruning of unsatisfied solutions, is used as an intermediate block between the optimization and the reliability analysis. Here, reliability analysis is not performed for solutions that do not meet the acceptance region criteria; thus, redundant simulations can be avoided. Similar to the yield-aware tool, the acceptance region boundaries are determined via coefficients determined by the user. Solutions satisfying the acceptance region are selected as candidates for the reliability analysis. Here, the developed aging simulator is used to predict the lifetime of each candidate. Lifetime of a candidate solution is determined as

$$\begin{aligned} A_j &= \{\boldsymbol{X} : y_j \geq K_j.O_j |\ x \in \mathbb{R}^s\} \\ I_{A_j}(\boldsymbol{X}) &= \begin{cases} 1, & \boldsymbol{X} \in A_j \\ 0, & \boldsymbol{X} \notin A_j \end{cases} \\ (\forall I_{A_j}(x) = 0) &\rightarrow (t_{life} = t_c) \end{aligned} \tag{5.13}$$

where A_j, K_j, and O_j denote acceptance value, acceptance coefficient, and the current value of outputs, respectively. I_{A_j} is the indicator function that indicates whether an output is in the acceptance region or not. Aging analysis is performed for a large number of candidate solutions through the iterations, which substantially increases the synthesis time.

To avoid redundant aging simulations and reduce the computational workload, the developed tool utilizes a stopping rule during the aging analysis. Namely, the acceptance region is continuously evaluated at the beginning of each time step during the aging analysis and if any acceptance region violation occurs, the simulation is stopped and the current time of simulation (t_c) is determined as the lifetime (t_{life}) of the candidate solution. Hence, unnecessary simulations are not carried out for solutions that have completed their lifetimes. As the final step, a particular cost is assigned to the candidate with respect to lifetime constraint given by the user. Then, the total cost given is then re-calculated by adding the reliability cost and included into the optimization loop. The loop ends either when the convergence or the maximum iteration number is reached.

5.5. Synthesis Examples and Results

Similar to the other tools proposed in this thesis, the lifetime aware synthesis tool was also implemented on MATLAB®, and HSPICE was utilized for performance evaluation. An Intel i7 4th generation chipset with 3.20 GHz processor was used during the synthesis process. In the optimization part, numbers of parents, offspring, and the maximum number of iterations were chosen as 50, 50, and 200, respectively. The developed NBTI model and the analytical HCI model given in Equation 5.1 were embedded in the aging simulator, in which s_1, s_2, and s_3 were selected as 10, 40, and 2, respectively. The error value for determining of the efficient step size was selected as $0.1mV$ per transistor.

The first synthesis example is a two stage OTA, whose schematic is given in Figure 4.26. There are 24 independent design parameters, including transistor dimensions, bias resistor, and compensation capacitor, whose limits are listed in Table 5.4. There are five different electrical design constraints including gain, $3dB$ bandwidth, phase margin, power consumption, and chip area. In addition to these electrical constraints, a lifetime constraint was also defined, which is dynamically added to the cost value if any candidate solution is found. The acceptance region coefficients for infeasible solution elimination were determined as 0.95 for all design constraints, where each candidate should have at least $9.5kHz$ bandwidth, $66.5dB$ gain, and 57° phase margin to be selected for the reliability analysis. In the reliability analysis part, the lower limits of design constraints were determined as being equal to values in ISE and lifetime calculation is performed considering these values.

Synthesis results for 5 independent runs are given in Table 5.5 for both lifetime-aware and nominal optimization. As listed in the table, the number of steps varies between 160 and 180 for different runs. All constraints except power and area were satisfied in all runs for a given lifetime. It can be concluded that the population evolved regarding the targeted lifetime; thus, solutions with larger devices and higher currents were preferred to increase the design safety margin and guarantee a certain lifetime.

Table 5.4. Design boundaries and variables for two stage OTA.

W $[\mu m]$	L $[\mu m]$	R_{bias} $[\Omega]$	C_{com} $[pF]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
0.65-130	0.12-10	100-10000	0.1-50	1.2	0	0.5

Table 5.5. Synthesis results of 5 independent runs for two stage OTA.

Run	Bandwidth $[> 10kHz]$	Gain $[> 70dB]$	Phase Margin $[> 60^o]$	Power $[< 1.5mW]$	Area $[< 6000\mu m^2]$	Step Count	Lifetime $[> 5years]$	Lifetime(exact) $[s = 1000]$	Synthesis Time $[min]$
1	11.5	71.34	67.14	1.6	6370	160	6.25	6.25	84.6
2	9.9	70.16	58.3	1.55	6230	180	5.75	5.75	66.8
3	13.4	72.10	70.42	1.5	5620	180	7.5	7.5	89.5
4	12.2	70	59	1.4	6400	150	6.25	6.25	97.8
5	9.5	68.4	60.23	1.3	5577	160	7.75	7.75	108.2
N	10.5	72.46	62.3	0.47	2350	—	—	3.11	21.8

Considering nominal synthesis results, power and area objectives are also satisfied. Lifetime-aware circuit synthesis power and area values are considerably larger. However, lifetimes of nominal synthesis results are relatively short, since the optimizer does not care about aging. $3dB$ bandwidth is the critical constraint for all runs, which decreased to the pre-determined limit (7 kHz) and determine the lifetime. To verify the efficiency and accuracy of the aging analysis part, an expanded aging simulation was run for each solution with larger step counts ($s = 1000$), and results indicate that the dynamic sizing algorithm in the aging analysis is highly reliable. To compare the efficiency of the developed tool, a single run was performed by using a fixed step count of 1000. The total synthesis time took almost 7 hours for this expanded synthesis, whereas the developed tool can complete the assignment in around 90 minutes. On the other hand, as expected, the developed tool is slower than the nominal synthesis due to the expensive aging simulations performed during the reliability analysis. Furthermore, it should be noted that the step count values given in the table denote the step counts of the final solutions, which results in an inconsistency between the provided step count and synthesis time values. However, in practice, the step count value may be different for each candidate solution due to adjustable step size approach, where the number of candidate solutions may also be different for each run. Namely, a run having a small number of average step count may have a long synthesis time due to having a large number of candidate solutions and vice versa. Consequently, the total synthesis time is affected by the combination of the average step-count and the number of candidate solutions during the synthesis process.

A folded cascode OTA shown in Figure 4.27 was chosen as the second synthesis example. This circuit has 15 design parameters, including transistor dimensions, bias voltages, and bias resistor, where limits of these parameters are listed in Table 5.6. There are also five different electrical design constraints, including gain, $3dB$ bandwidth, phase margin, power consumption, and chip area. Similarly, minimum targeted lifetime was selected as 5 years, and the optimizer tries to maximize this value during evolution. The acceptance region coefficients for infeasible solution elimination was also determined as 0.95 for all design constraints.

Table 5.6. Design boundaries and variables for folded cascode OTA.

W $[\mu m]$	L $[\mu m]$	R_{bias} $[\Omega]$	V_{cm1} $[V]$	V_{cm2} $[V]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
0.65-130	0.12-10	100-10000	0.4-0.8	0.4-0.8	1.2	0	0.5

Table 5.7. Synthesis results of 5 independent runs for Folded Cascode OTA.

	Bandwidth $[> 10kHz]$	Gain $[> 70dB]$	Phase Margin $[> 60^o]$	Power $[< 1mW]$	Area $[< 6000\mu m^2]$	Step Count	Lifetime $[> 5years]$	Lifetime (exact) $[s = 1000]$	Synthesis Time $[min]$
1	14.4	70.82	65	0.84	5500	160	9.38	9.38	101.1
2	13.6	72.81	62.66	0.92	3700	140	8.7	8.7	91.9
3	9.4	70.70	66.5	1.2	5800	140	7.65	7.65	80.12
4	9.36	75.9	64	1.05	5200	180	7.25	7.25	82.2
5	11.5	70.1	60.3	0.9	5120	150	8.25	8.25	114.2
N	12.8	71.8	66.2	0.3	2400	—	—	3.85	22.6

In the reliability analysis part, low limits of $3dB$ bandwidth, gain, and phase margin were determined as $9.5kHz$, $66.5dB$, and 57°, respectively. Results of lifetime-aware and nominal optimization are given in Table 5.7 for 3 independent runs. Constraint values are kept the same with the two stage example except for power consumption, where folded cascode topology requires a smaller current to achieve the same performance. For this example, the step count for aging simulations was to be found between 140 and 160. As expected, the optimizer again follows an overdesign approach during the lifetime-aware circuit synthesis by keeping device dimensions somewhat larger and increasing the bias current to satisfy the lifetime constraint. Considering lifetime-aware synthesis results, all electrical constraints and the targeted lifetime were achieved for all runs except for power consumption and area, which were sacrificed for the sake of lifetime. Similar to the two-stage circuit, $3dB$ frequency degraded over time and is the dominant constraint for the determination of the lifetime. Similar to the two stage example, another lifetime aware synthesis was also performed by setting the step count to 1000 in order to illustrate the efficiency of the developed tool. The total synthesis time for this fixed sized run was found to be 6 hours, which is almost 4 times slower than the proposed tool, in which the average synthesis time is around 90 minutes.

5.6. Conclusion

Increased aging effects on circuit performance result in lifetime reduction of CMOS ICs. As a result, aging-aware circuit design has become a major concern to guarantee a certain lifetime. To design robust analog circuits, an aging analysis is performed, effects on circuit performances are observed, and the design is revised, if necessary. As a result, the overall design time inevitably increases to satisfy both electrical and robustness constraints. One possible solution to reduce the synthesis time is automatic synthesis of analog circuits with a modified circuit optimizer, in which lifetime is taken into account as another design constraint in addition to the electrical constraints. However, one further challenge arises during augmentation of the optimizer with aging analysis, where present aging simulators examine the total

simulation time within sub-periods using a static step size. However, considering the numerous iterative evaluations during the optimization process, using a static step size leads to either unnecessarily increased synthesis times or inaccurate estimations. In this paper, a lifetime-aware circuit synthesis tool that uses an efficient aging simulation approach is described. Furthermore, a silicon verified semi-empirical NBTI model is proposed through AAT to improve the estimation accuracy. Since the HCI effect has not been observed in the AAT, an analytical model was utilized in the aging analysis part. Nevertheless, according to the simulation results, no HCI effect has been observed for the 130 nm technology, either. Another possible reason is that OTA circuits require a certain amount of channel length to provide a definite voltage gain, which also reduces the HCI effect. Therefore, average lifetime of folded cascode OTA topology was found to be higher than that of the two stage OTA, since folded cascode has an n-type differential pair and has not been degraded.

6. RECONFIGURABLE ANALOG CIRCUIT DESIGN

The idea behind lifetime-aware optimization is to find a design point that is relatively far from the minimum acceptance region (performance boundary); thus, the circuit can maintain its regular function for a certain time even if the circuit ages over time. Furthermore, defining lifetime as a design constraint provides insight to the optimizer to find more robust solutions through the evolution. However, in both cases, the optimizer converges to a solution that occupies a larger chip area and consumes much more power than the solution found with nominal optimization. As a result, lifetime-aware optimization has two major disadvantages.

At first, some design constraints (power and area) should be relaxed to find an overdesigned solution. The second problem arises during the synthesis of analog circuits for some particular applications such as low power and high frequency. Namely, transistors with shorter channel lengths are used to satisfy the high frequency requirement. However, the lifetime-aware synthesis tool generates solutions employing larger devices to increase the lifetime. In addition to that, increased power consumption also limits the use of lifetime-aware analog circuit synthesis. To overcome this bottleneck, reconfigurable circuit design approaches are commonly utilized. The most popular reconfigurable approach is called "Sense and React (S & R)" approach, which is based on sensing the degradation on circuit performances and activating the recovery operation, respectively. In this chapter, S&R approach is thoroughly discussed focusing on the aging phenomena.

The chapter is organized as follows. In Section 6.1, all components of S&R system are individually discussed and the developed methodologies are explained in detail, respectively. In Section 6.2, implementation of S&R systems is discussed for two different circuits, where two different design approaches are proposed. Finally, Section 6.3 concludes this chapter.

6.1. Sense and React Approach

S&R is the well-known reconfigurable design approach, where a general block diagram of a S&R loop is shown in Figure 6.1.



Figure 6.1. Sense and React loop.

The first block is called "Design Under Test (DUT)", which represents the circuit under examination. The second operation is called "Sense", in which any change in DUT output is measured via a sensor circuit. Typically, the type of sensor circuit depends on the application and varies depending on the function of the circuit. Typically, node voltages, branch currents, and phase/frequency are the measurable quantities for an electrical system. The third operation is called "Evaluation", where the data generated by the sensor is evaluated and enable signals are generated. The last operation is called "React", in which pre-determined recovery scenarios are applied to the circuit when an enable signal is received from the evaluation block.

6.1.1. Sense Operation

Aging leads to degradation in the threshold voltage of transistors causing a decrease in saturation current, which finally results in circuit performance deterioration. Obviously, direct measurement of degradation in any circuit performance is very difficult. Therefore, indirect measurements are commonly preferred, where some electrical quantities, such as node voltages, currents, and phase/frequency of a signal are measured and changes in these quantities are detected.

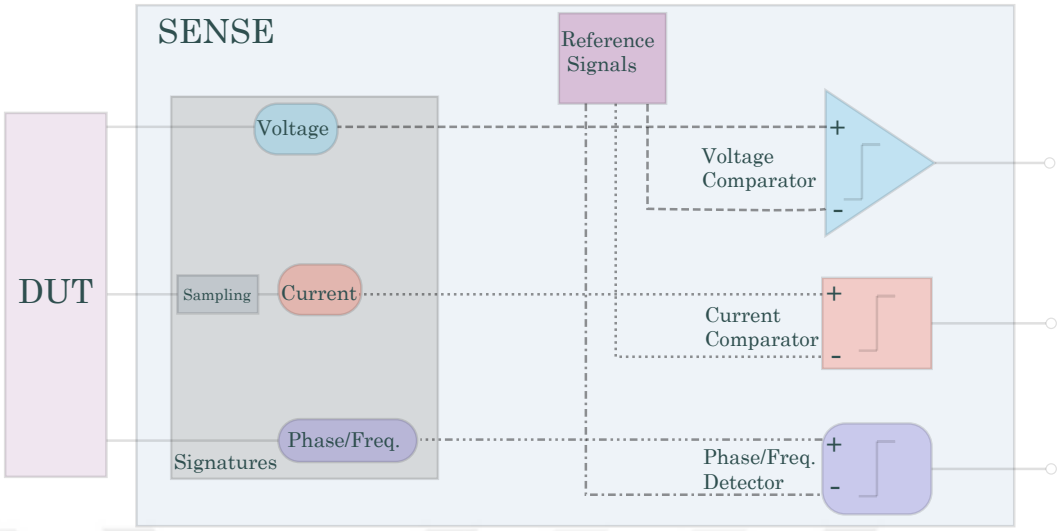

Figure 6.2. Sense operation scenarios.

As seen from Figure 6.2, a sampling circuit is required to sense the change in the current while voltage and phase/frequency quantities can be directly detected. Typically, current mirrors are utilized to sample the current. However, the design of current sampling circuit is highly critical since aging of mirroring transistor causes inaccurate sampling, which disrupts the whole recovery mechanism. Since indirect measurements are carried out during the sense operation, one or more signatures are required in order to detect degradation. However, signature selection is a complicated problem, where an efficient signature should have certain attributes, such as Relevance ($\mathcal{R}$), Measurability ($\mathcal{M}$), and Applicability ($\mathcal{A}$). First of all, the signature behavior

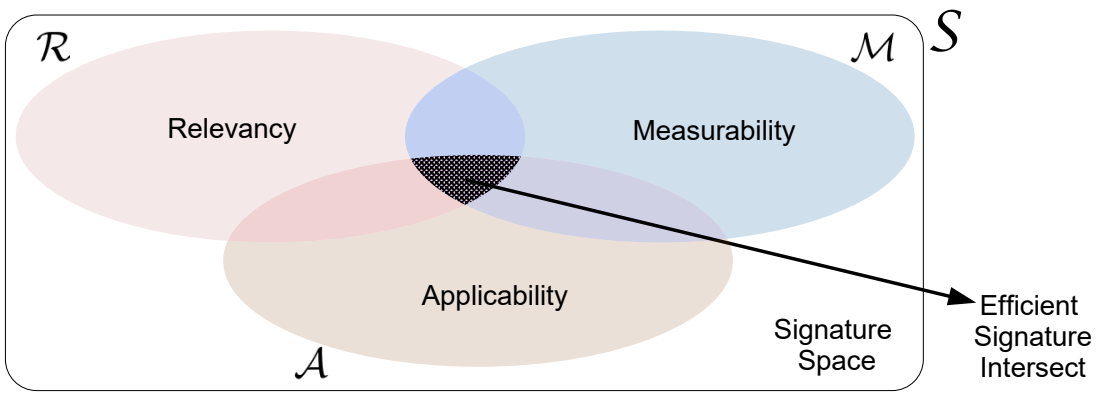

Figure 6.3. Efficient signature properties.

should be relevant with the behavior of the degraded performance feature to be able to map the signature changes into the performance degradation. Furthermore, aging-induced changes in the relevant signatures should also be within the limits of the input sensitivity of the sensor circuit; otherwise, the sensor circuit can not detect them, which results in sense operation malfunction. Finally, loading effects should also be considered in order to avoid any possible performance loss during the sense operation. Therefore, signatures without any data signal are preferred. To sum up, the efficient signature space can be defined as the intersection set of the Relevance, Measurability, and Applicability sets as illustrated in Figure 6.3.

Alternate test is a popular method in testing area, in which an indirect testing approach is utilized to mitigate the complexity and cost of production tests. Conventional specification-based tests are replaced at the production line by a set of low-cost indirect observations, and test results are then processed and interpreted to observe specification results. The process is developed in two stages: a learning stage and a testing stage. During the learning stage both performance features and signatures are measured by using a training set. Then, a machine learning algorithm is assigned to build a mapping model. In the testing stage, signatures are measured for each DUT, and test results are interpreted by using the mapping model obtained in the previous stage. A block diagram for a conventional signature based alternate test is given in Figure 6.4.

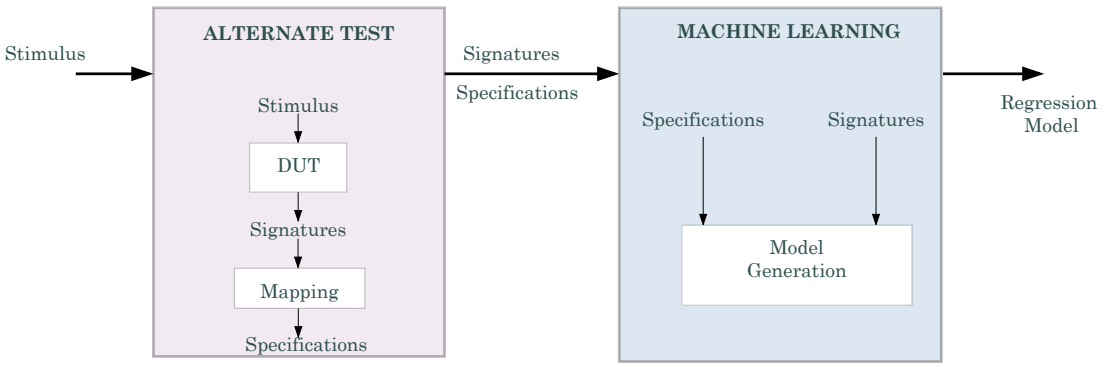

Figure 6.4. Signature-based test schema for analog circuit testing.

At the first phase, an appropriate stimulus is applied to the DUT. Then, signatures and specifications are measured and a correlation mapping is carried out to determine the relevant signatures. At the second phase, selected circuit signatures and related specifications are evaluated together and a model is constituted. Finally, the developed model is used during the testing of a large number DUTs.

This alternate test approach can be adopted in order to overcome signature selection problem in a S&R system. Since there is no mass testing requirement in this case, the machine learning part can be discarded. The next problem is the selection of the input stimulus. This problem was solved in [137], where a Monte Carlo-based training set was utilized to generates samples. The proposed approach is given in Figure 6.5.

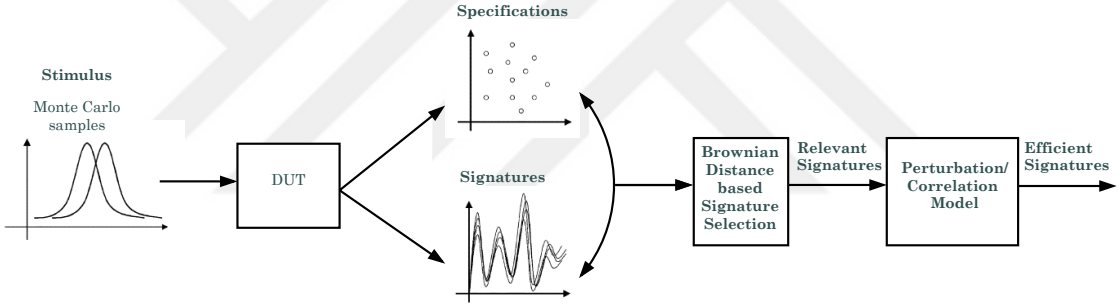

Figure 6.5. MC-based signature selection.

In this proposed approach, a large number of instances of DUT are generated by Monte Carlo simulations rather than a particular stimulus signal. Then electrical simulations are performed to obtain both signatures and specifications. Finally, a signature selection algorithm is applied to the signatures and the specifications to determine the relevant signature. A Brownian distance [138] based signature selection and ranking is used to capture the relevant signatures. Finally, a perturbation/correlation model is assigned to explore efficient signatures to select appropriate test signatures. Actually, this is an example of sensitivity analysis to determine signatures around the design boundary. This part of the analysis is related to testing problems, where a large number of devices are easily tested and evaluated.

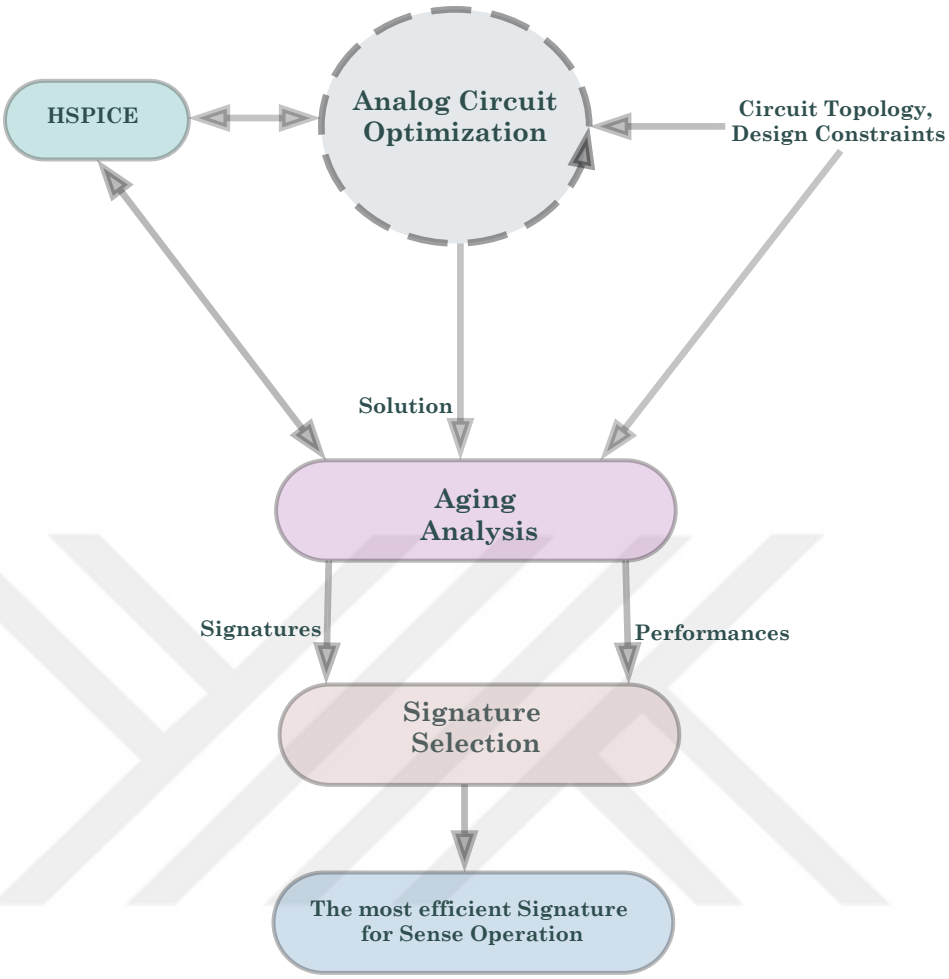

Figure 6.6. Flow chart of signatures selection for sense operation.

Brownian distance correlation-based signature selection seems to be convenient to be performed for relevancy analysis. Furthermore, no extra Monte Carlo analysis is required for S&R systems, because the developed aging simulator divides the life-time analysis into sub-periods by a variable step-size, so instances for training set for signature selection process are automatically generated. The only modification should be applied to the simulation part of the simulator in order to measure the candidate signatures during aging simulations. In Figure 6.6, a flow of the proposed approach is given. The flow starts with an optimization loop that generates a satisfied solution for a given circuit topology. Then, an modified aging analysis is performed to obtain the signatures and specifications.

A conventional approach to measure the dependence between two random variables is based on the Pearson's product-moment correlation (ρ) and co-variance. Pearson's correlation uses a first-order distance formula to calculate dependency of two random variables, so it is valid only for linear or monotone conditions. As a result, Pearson's correlation does not provide a reliable solution for a wide range of applications. To overcome this problem, the use of Brownian distance correlation ($\mathcal{R}$) in order to correlate signatures and specifications was proposed in [137]. Hence; non-linear behaviors can be captured with finite second order moments, where the detail can be found in [138].

For a signature and specification set $(S, F) = \{(S_i, F_i) : i = 1, 2, ...n\}$, the Euclidian distance matrices for vectors $S \in \Re^p$ and $F \in \Re^q$ can be computed as

$$\begin{aligned} (x_{ij}) &= (|S_i - S_j|_p) \\ (y_{ij}) &= (|F_i - F_j|_p) \end{aligned} \tag{6.1}$$

Defining $X_{ij} = x_{ij} - \bar{x_{i.}} - \bar{(}x_{.j}) + \bar{x..} \qquad i, j = 1, 2, ..., n$, where

$$\bar{x_{i.}} = \frac{1}{n}\sum_{j=1}^{n} x_{ij}, \quad \bar{x_{.j}} = \frac{1}{n}\sum_{i=1}^{n} x_{ij}, \quad \bar{x_{..}} = \frac{1}{n^2}\sum_{i,j=1}^{n} x_{ij} \tag{6.2}$$

Similarly, defining $Y_{ij} = y_{ij} - \bar{y_{i.}} - (\bar{y_{.j}}) + \bar{y..} \qquad i, j = 1, 2, ..., n$, the distance covariance $\mathcal{V}_n(S, F)$ and the sample correlation $\mathcal{R}(S, F)$ are calculated as

$$\mathcal{V}_n^2(S, F) = \frac{1}{n^2}\sum_{i,j=1}^{n} X_{ij}Y_{ij} \tag{6.3}$$

and

$$\mathcal{R}(S, F) = \begin{cases} \frac{\mathcal{V}_n^2(S,F)}{\mathcal{V}_n^2(S)\mathcal{V}_n^2(F)}, & \mathcal{V}_n^2(S)\mathcal{V}_n^2(F) > 0 \\ \\ 0, & \mathcal{V}_n^2(S)\mathcal{V}_n^2(F) = 0 \end{cases} \tag{6.4}$$

respectively. Consequently, the distance correlation $\mathcal{R}(S, F)$ between candidate signatures S_i and circuit specifications F_i can be used as a figure of merit for the relevant signature selection.

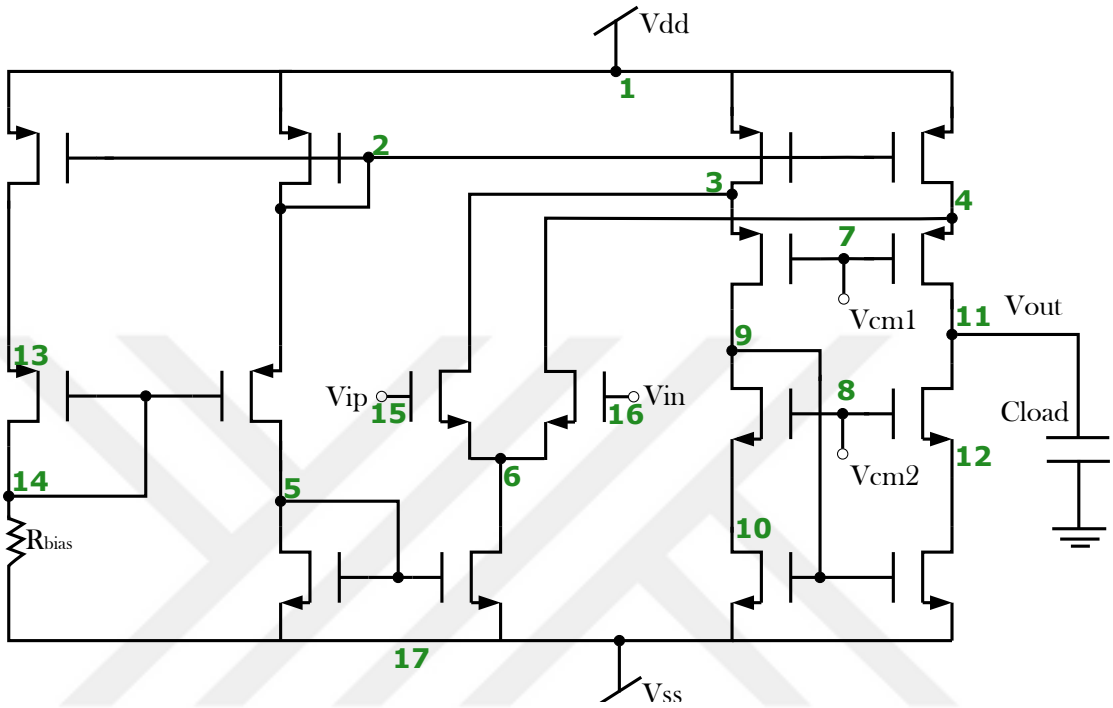

Figure 6.7. A preliminary flow for determination of efficient signatures for sense operation.

To illustrate the concept of correlation between signatures and circuit specifications, the folded cascode circuit given in Figure 6.7 was synthesized via the analog circuit optimizer and an aging analysis was performed with 500 steps. Node voltages were determined as the signatures while closed-loop gain, bandwidth, and phase margin were determined as the circuit specifications. Pearson's and Brownian distance correlations were computed for each specification. The results of three different signatures are given in Figure 6.8. As can be seen from the first signature (V14) specification correlation results, Brownian and Pearson's distance correlations are similar to each other for bandwidth and phase margin specifications, where the dependency is quite linear.

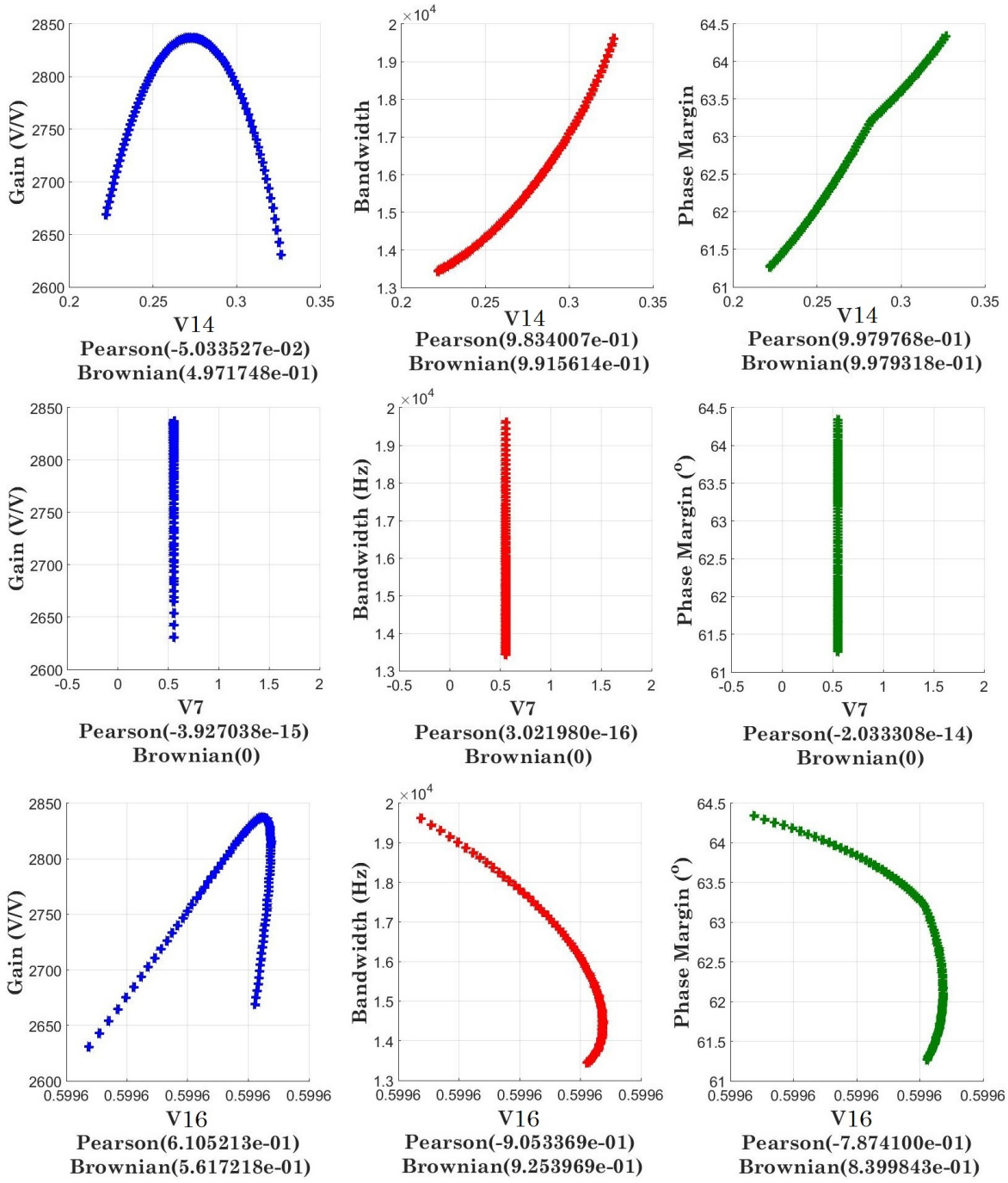

Figure 6.8. Pearson and Brownian distance correlations.

However, the correlation between the gain and the signature is non-linear, so Pearson's correlation is incapable of capturing the relation, whereas Brownian distance correlation still generates a valuable result. Results of an irrelevant signature (V7) are

given for the same specifications, where Pearson's and Brownian approaches generates similar results. A more interesting result is obtained for the last signature (V16), where the behavior is highly non-linear. However, the critical point is that the amount of change in the signature is negligible, so this signature is not correlated with circuit specifications. However, Brownian and Pearson's approaches correlate the signature and circuit specifications. This case reveals a further problem considering the sensor design. Comparator circuits are commonly used as sensors for the sense and react approaches and they have a certain input sensitivity. This sensitivity property of the sensor should be taken into account during the selection of the efficient signature. Therefore, an additional analysis is required to determine measurable signatures among all candidate signatures. In addition to measurability and relevancy, applicability is also important to avoid any distortion during the sense operation.

Considering all these properties, a comprehensive signature selection approach is proposed as shown in Figure 6.9. The flow again starts with an aging analysis, where changes in signatures and specifications (features) are obtained. Then, the flow continues in two parallel steps. On the one side, relevant signatures are determined by using the Brownian distance correlation. Thanks to the signature elimination part, irrelevant signatures are directly filtered out according to

$$I_{R_i} = \begin{cases} 1, & \mathcal{R}(S_i, F_i) \geq \overline{\mathcal{R}(S_i, F_i)} \\ \\ 0, & \mathcal{R}(S_i, F_i) < \overline{\mathcal{R}(S_i, F_i)} \end{cases} \tag{6.5}$$

where $i = 1, 2..., n$. I_{R_i} denotes the indicator function that indicates the signature is relevant ($I_{R_i} = 1$) or irrelevant ($I_{R_i} = 0$). The threshold value for the signature elimination is the average value ($\overline{\mathcal{R}(S_i, F_i)}$) of the signature set. On the other hand, a measurability analysis is performed in order to determine the measurable signatures, where other ones are directly eliminated. Defining the change in the signature ΔS_i and minimum sensitivity of the sensor P_{sensor}, the measurability of a signature is

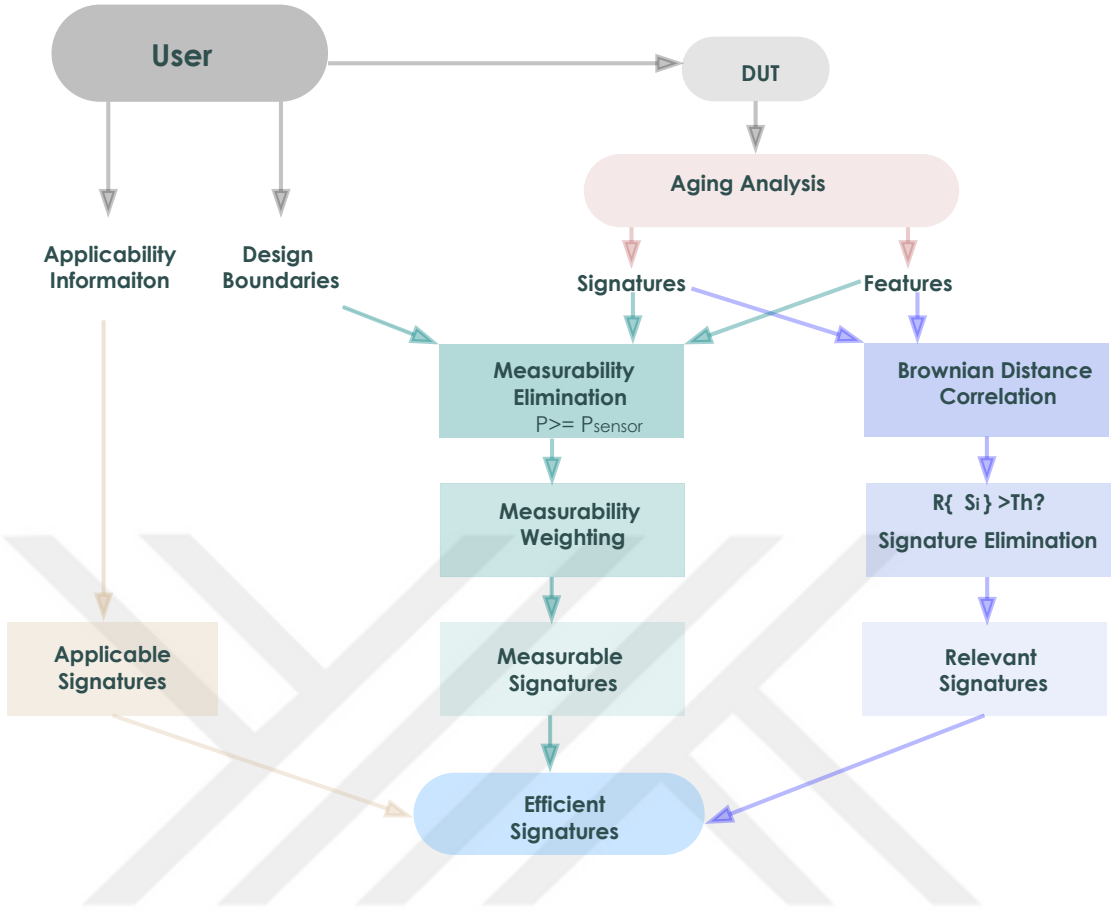

Figure 6.9. Flow chart of the proposed methodology.

determined as

$$I_{P_i} = \begin{cases} 1, & \Delta S_i \geq P_{sensor} \\ \\ 0, & \Delta S_i < P_{sensor} \end{cases} \tag{6.6}$$

where $i = 1, 2..., n$. I_{P_i} denotes the indicator function that indicates the change in the signature is measurable ($I_{P_i} = 1$) or not ($I_{P_i} = 0$). After the elimination, a total weight budget of W_{total} are allocated among the measurable signatures ($i = 1, 2..., k$) according to

$$W_i = \frac{\Delta S_i}{\sum_{i=1}^{k} \Delta S_i} W_{total} \tag{6.7}$$

This weighting process provides ordering of the candidate signatures depending on the change amounts, where signatures having larger changes are preferable to keep the comparison error at minimum. Contrary to measurability and relevancy, applicability information requires an expert knowledge on the circuit topology. Therefore, the applicability information is initially required by the user and taken into account at the final determination step in the developed tool. There are three different score defined for the applicability information of signatures: *low* (0.1), *moderate* (0.5), and *high* (1). Ultimately, the tool generates a list of efficient signatures, where all individual scores, signature-feature graphs, and the time for recovery are also provided.

The OTA circuit was synthesized using 130nm technology, where gain, 3dB bandwidth, and phase margin were selected as design features. Node voltages not including power (1,17), input (15,16), and bias (7,8) nodes were taken as 11 aging signatures. According to the fresh simulation results, the circuit has 68.3 dB gain, 19.7 kHz bandwidth, and 64.3^o phase margin. The lifetime was decided to be 10 years for aging simulations, where the step count was selected as 500. Design boundaries for sense operation were selected as $65dB$, $17kHz$, and 60°, respectively. In the case of violation in any circuit specification, changes in the signatures are calculated for measurability analysis. The input sensitivity of the sensor, which is typically a voltage comparator, was fixed to $1mV$. The total weight for the measurability was selected as 100. In Figure 6.10, aging simulation results are given for the folded cascode circuit.

As can be seen from the simulation results, the bandwidth of the amplifier substantially decreases over time, while there is no considerable degradation in the gain and the phase margin of the amplifier. Therefore, the sense strategy was designed to detect the degradation in the bandwidth.

Signature selection results are given in Table 6.1. Correlation results indicate that almost all candidate signatures have a strong correlation with the bandwidth behavior. However, more than half of these candidates were eliminated by the measurability elimination, since the variation amounts for these candidates at the critical point are

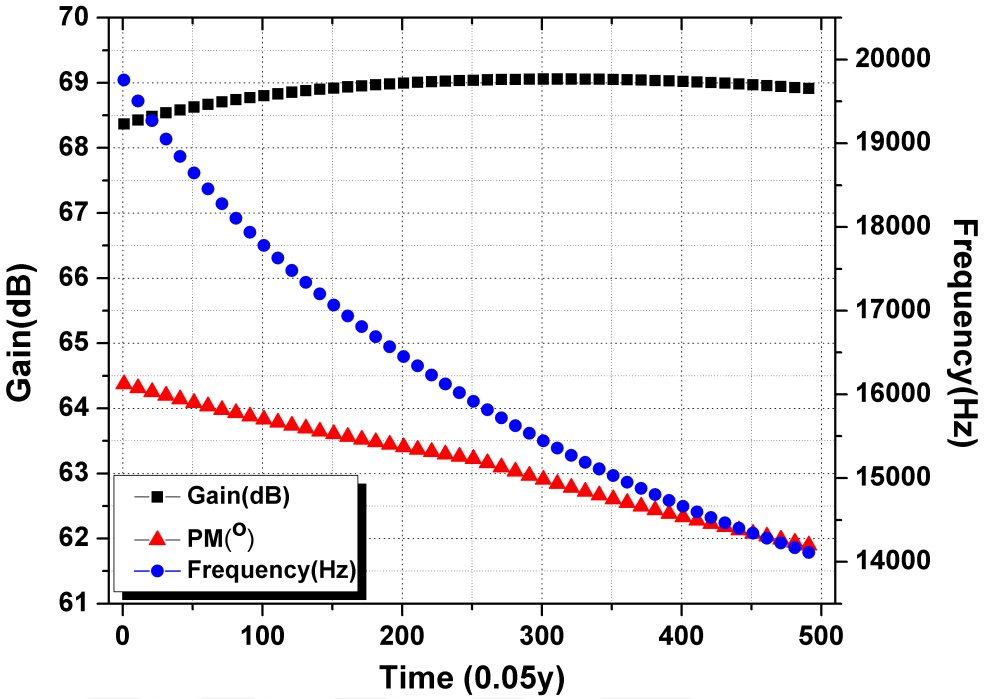

Figure 6.10. Aging simulation results.

Table 6.1. Signature selection results for the folded cascode amplifier.

Signatures (Nodes)	**2**	**3**	**4**	**5**	**6**	**9**	**10**	**11**	**12**	**13**	**14**
Correlation Score	99.5	99.9	99.8	99.2	99.3	99.2	77.3	97.5	99.2	99.4	99.5
Measurability Score	9.58	33.1	31.18	0	0	0	0	0	0	9.59	16.53
Applicability Score	1	0.1	0.1	1	0.5	0.1	0.5	0.1	0.5	1	1
Efficiency Score	953	330	311	0	0	0	0	0	0	953	***1644

lower than the input sensitivity of the sensor. After the measurability weighting, signatures 3, 4, and 14 are the prominent candidates out of the standing 5 signatures. At the third row, user-defined applicability scores are provided. Since the signal on nodes 3, 4, 9, and 11 may be affected during the sense operation, low applicability scores were assigned to these signatures. Finally, the total efficiency scores were presented at the last row, where the efficient signature for sense operation was found to be node 14. According to the aging simulation results, the sense operation would be activated after a two year operation, where the bandwidth violates the design boundary. Furthermore, the tool also provides a signature-feature graph as given in Figure 6.11 for the proposed signature.

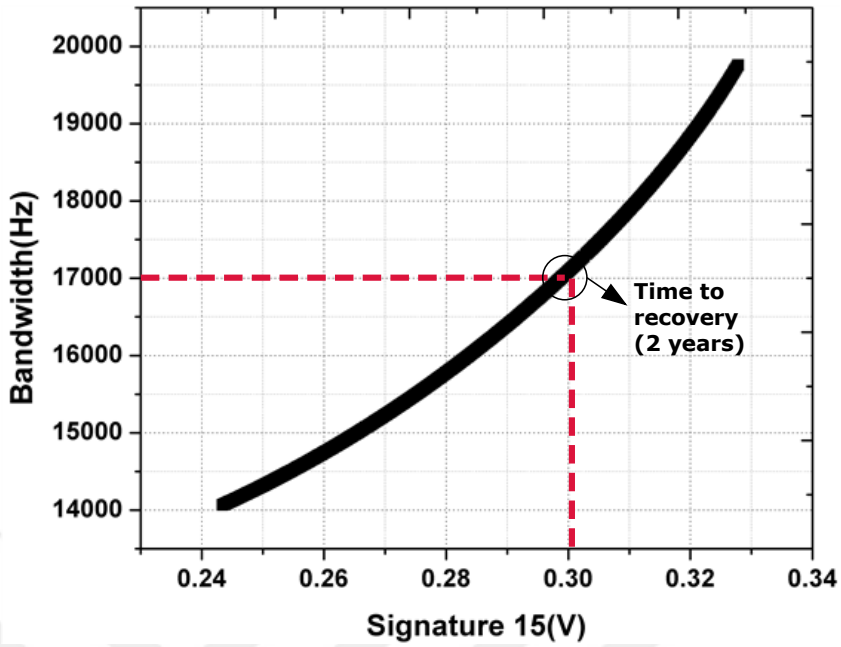

Figure 6.11. Signature vs feature graph.

6.1.2. Evaluation Operation

The next operation in a S&R system is the "Evaluation" step, in which signals transmitted by the sense block are evaluated and enable signals for recovery operation are generated. Actually, evaluation operation is an interface step between the sense and the react operations. Evaluation provides mapping of the circuit changes to recovery operations as illustrated in Figure 6.12. Typically, digital circuits are used in this step, such as flip-flops, counters, encoders, and multiplexers.

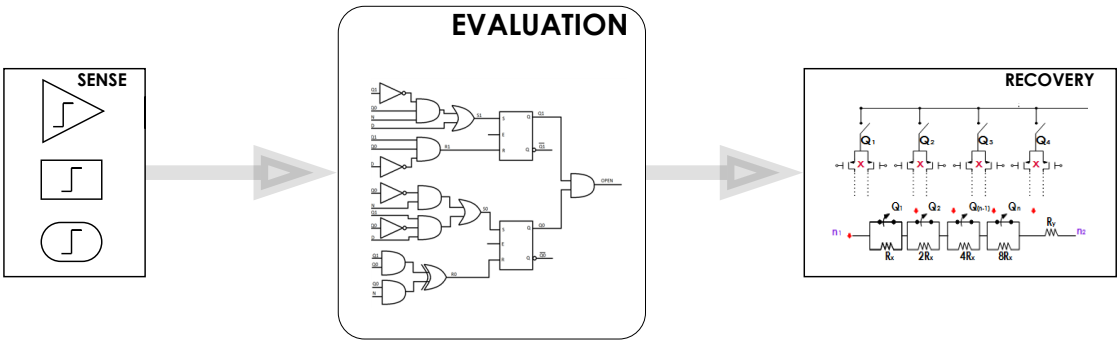

Figure 6.12. Evaluation block acts an interface block between sense and react.

In addition to these standard logic cells/blocks, some recovery operations require unique solutions at this part. Therefore, the design of the evaluation block depends on the type of recovery operation. As a result, the design of the evaluation block is not a standard process and different recovery applications require various types of evaluation block. Therefore, one should consider the react block operations during the design of the evaluation block.

6.1.3. React Operation

At the end of the evaluation operation, enable signals are generated and transmitted to the react operation block. Typically, there are three different recovery operations for react part, these are; adaptive biasing, adding supplementary transistors/blocks, and exchange of aged transistors/blocks by fresh ones.

In the "Adaptive Biasing" approach, the activation data generated by the evaluation is converted to some pre-determined voltages and applied to the critical nodes to compensate the increase in the threshold voltage. Thus, the currents provided by the aged transistors are recovered. However, this approach is quite difficult and expensive since both evaluation and conversion of change in the circuit output to bias voltages are highly challenging problems. In addition to this, a further problem arises due to the nature of aging for adaptive biasing approach, where the stress on the device is increased when recovery of the degradation in the current, which may accelerate the aging process for long term operations.

In the second approach, some supplementary devices in the chip, which are deactivated at the beginning, are activated to compensate the degradation effects. This approach is highly advantageous for circuits that age rapidly; thus, even small degradations can be detected and recovered within short time periods by circuits designed considering high resolution in terms of the change of the output parameters. However, adding extra devices may cause some performance deterioration in some particular applications such as increase in the device noise for RF applications.

In the last approach, rather than adding supplementary devices, aged transistors/blocks are completely replaced by fresh ones; thus, a full recovery is achieved. This approach does not suffer from any performance degradation. However, in general, the exchange operation can only be performed for one time due to the area occupation of fresh devices on the chip. Obviously, the type of recovery operation varies for different applications. Furthermore, aging analysis has a critical role for the recovery operation, where it provides the amount of degradation information for individual transistors. Hence, the designer has the information of the most critical devices for a given circuit. On the other hand, the designer takes over from the CAD tool for the recovery decision, because, an expert designer can find the efficient solution within a few number of iterations rather than a blind iterative recovery search.

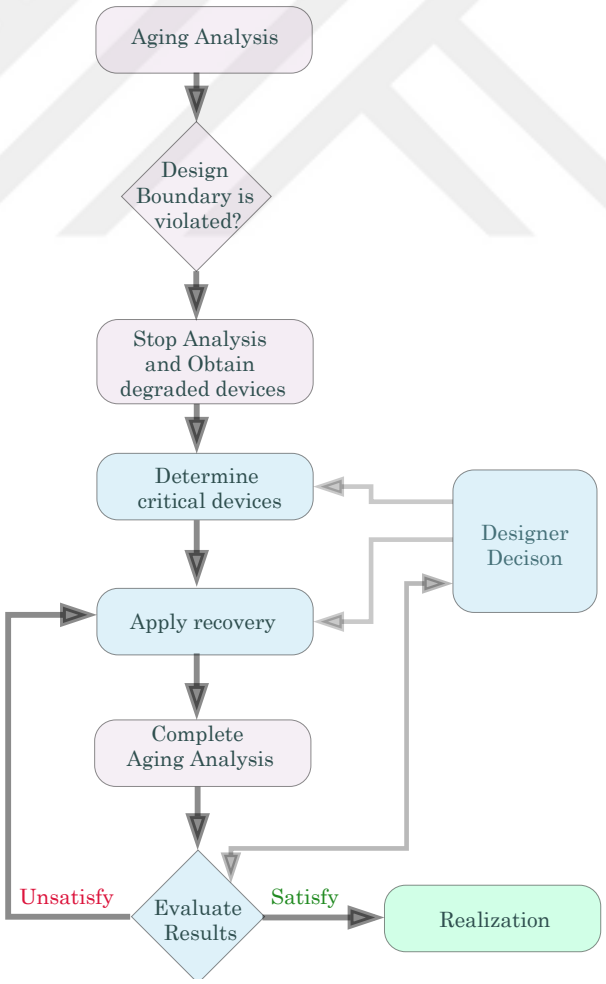

Figure 6.13. A semi-automatic system for determination of the react operation.

In this context, a semi-automatic recovery operation system was designed to find an efficient recovery solution for a given circuit topology, where the system requires designer decision at different steps. The flow chart of the recovery system is given in Figure 6.13.

At first, an aging analysis is performed for the DUT. During aging analysis, circuit features are continuously monitored, where the analysis is stopped when any boundary violation occurs. All circuit specifications, signatures, and degraded device information are obtained when the analysis is stopped. Here, the designer interferes in the flow in order to determine the critical devices among degraded ones. Then, a recovery operation that was also designed by the designer is implemented to the circuit. Finally, a verification simulation is carried out to test the recovery operation. The designer evaluates the final results and the flow ends with the realization if the recovery operation is satisfied. In the case of any unsatisfactory case, the recovery operation is replaced by a new one by the designer and the same procedure is repeated.

The folded cascode OTA circuit given in Figure 6.7 was chosen as the first example. Node voltages were determined as signatures while gain, bandwidth, and phase margin were determined as circuit specifications. Design boundaries were determined as the 0.9 times of the nominal values. Three different types of recovery operation were applied to the circuit: renewing degraded transistors, increasing the bias current, and adapting the common mode voltage, V_{cm1}. All of these recovery operations were determined considering the NBTI effect, since observations have indicated that HCI does not take place for $130nm$ technology.

The renewing method is based on replacing the degraded devices with fresh ones. There are a number of different renewing operations, in which different combinations of renewing transistor pairs were examined. The list of renewing operations and results are given in Figure 6.14. Simulation results indicate that only the $3dB$ bandwidth of the OTA worsens over time, where gain increases and there is no considerable degradation in the phase margin.

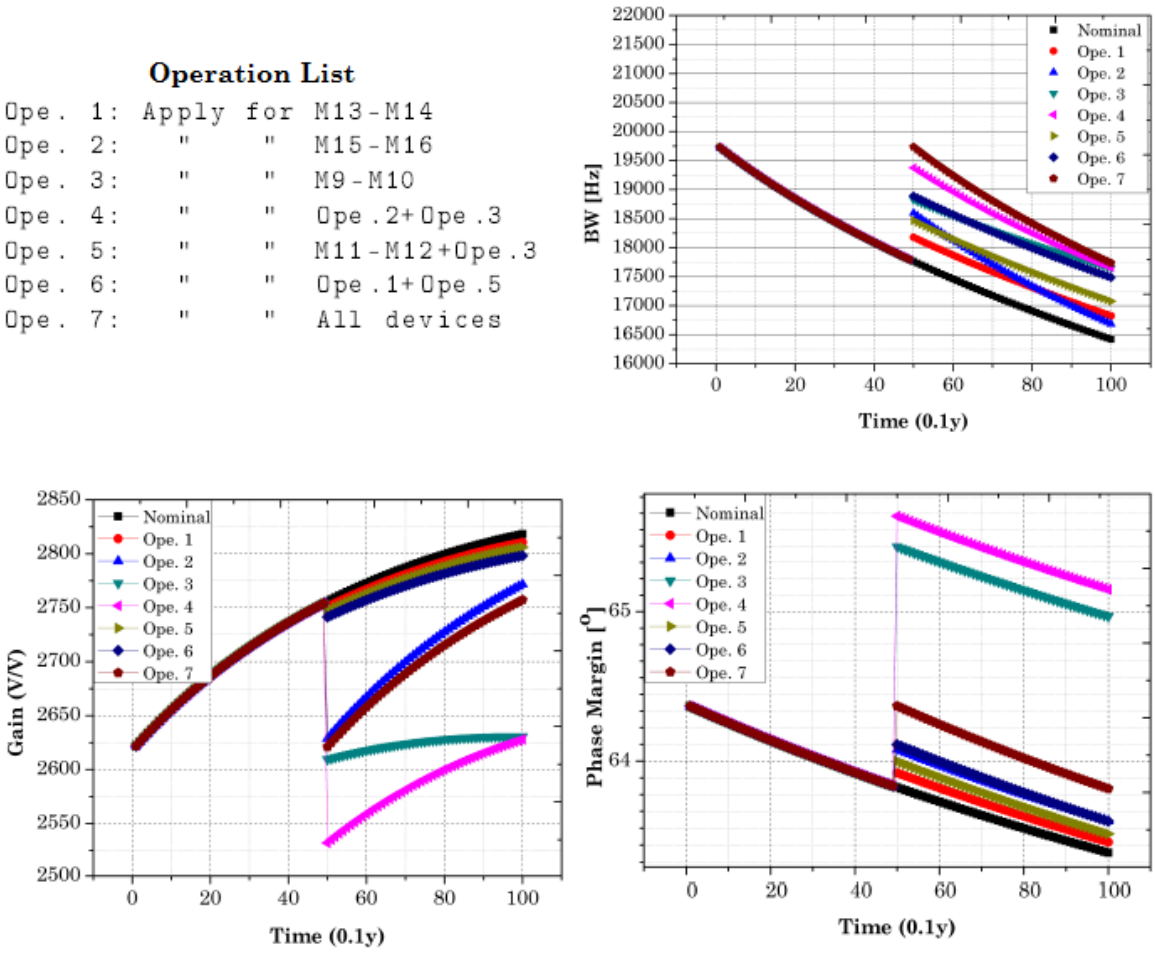

Figure 6.14. List of renewing operations and simulation results.

Furthermore, the most efficient recovery operation that recovers the degradation in the bandwidth seems to be operation 4, where M9-M10 and M15-16 transistor pairs are replaced by fresh ones. However, gain of the amplifier reduces in that case. Another disadvantage of this approach is that additional substitute transistor sets complicate the layout design, where a control switch will also be included to each device to manage the recovery operation.

Another recovery approach is to recover the bias current by an adaptive recovery operation. It is clear that saturation currents of transistors decreases over time due to increase in the threshold voltages. Therefore, increasing the bias current of the

system may provide a certain recovery. To illustrate this approach, the bias resistor (R_{bias}) was reduced by a number of scaling factors and simulation results are provided in Figure 6.15.

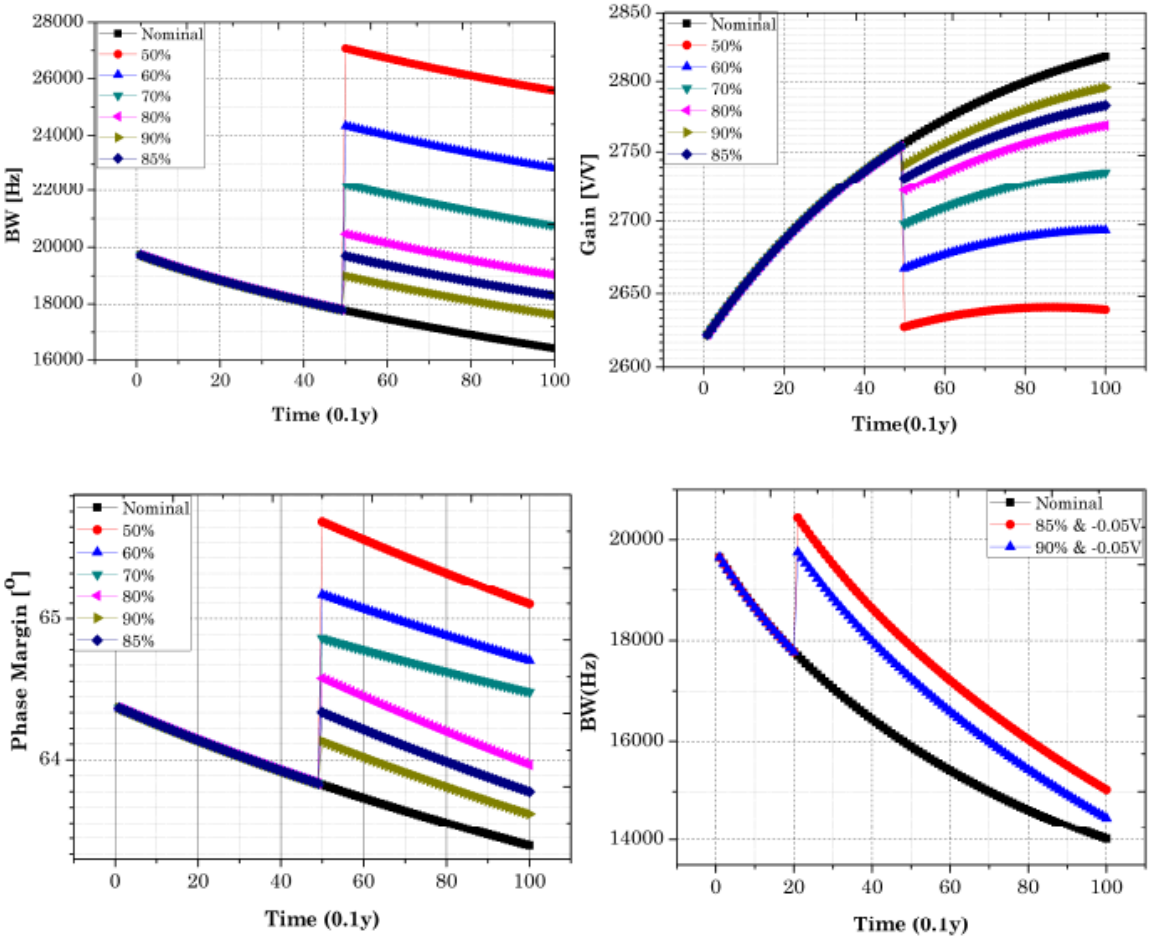

Figure 6.15. Simulation results of adaptive biasing approach.

As seen from the results, decreasing bias resistor by a factor of 15% provides a considerable recovery on the bandwidth response while keeping the gain and phase margin performance. This approach is quite simple and easy to be performed compared to the renewing approach. Furthermore, as can seen from the results, a fine tuning of the common-mode voltage (V_{cm1}) enhances the recovery operation.

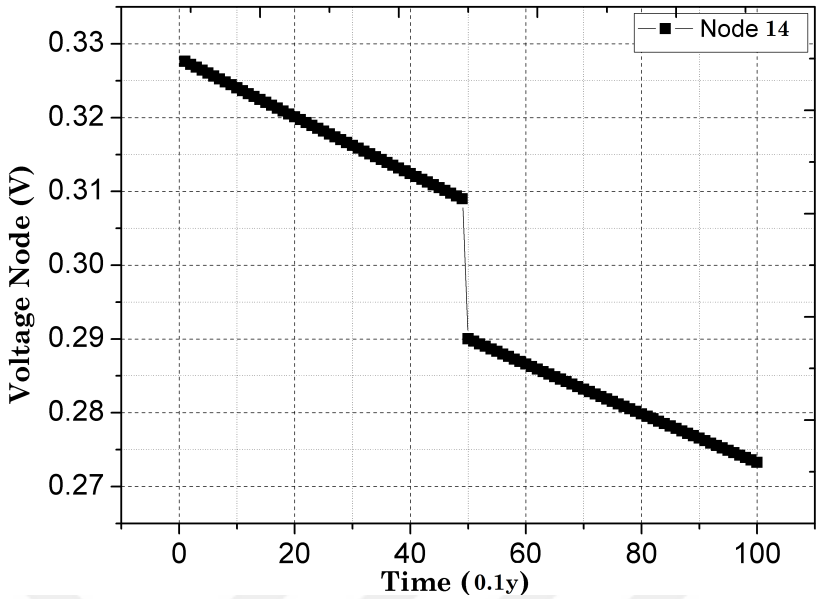

Figure 6.16. Behavior of the signature after recovery operation.

A further problem arises when the signature correlation is considered during the recovery. Namely, the recovery system is enabled, when a degradation occurs in any circuit specification. Signature selection algorithm gives the most efficient signature to notice the degradation in the circuit specifications. However, the recovery operation cannot guarantee recovery of the signature as given in the Figure 6.16, which is the most efficient signature for the folded cascode example. If the signature is not recovered to the initial value, the sense and evaluation operations will always generate an aging signal once the circuit ages. Therefore, this approach is only valid for a one-stage recovery, where only one recovery operation can be performed for a given circuit over its lifetime.

To palliate this bottleneck, the flow given in Figure 6.13 is modified as given in Figure 6.17. In the modified flow, another signature selection algorithm is applied after the recovery operation; thus, a relevant signature can be obtained to determine whether the circuit has been recovered, which is called reversibility. The new signature selection results are given in Figure 6.2.

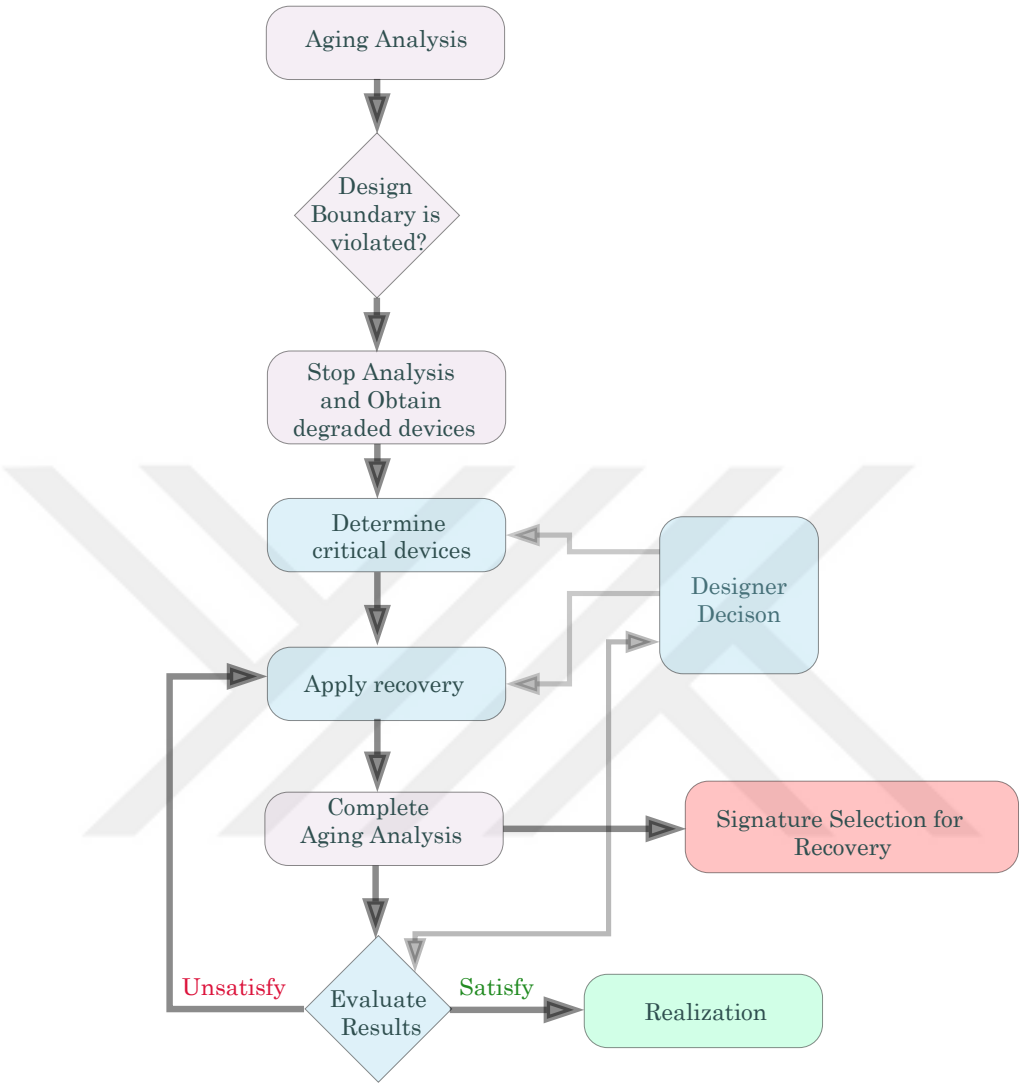

Figure 6.17. The modified react approach flow.

Table 6.2. Recovery-aware signature selection results.

Signatures (Nodes)	**2**	**3**	**4**	**5**	**6**	**9**	**10**	**11**	**12**	**13**	**14**
Correlation Score	0	94.3	94.3	97.6	79.3	97.2	77.3	98.1	98.2	0	0
Measurability Score	7.38	28.1	28.02	6.8	5.6	3.3	0	3.1	0	7.39	10.31
Applicability Score	1	0.1	0.1	1	0.5	0.1	0.5	0.1	0.5	1	1
Efficiency Score	0	208	208	***660	222	32	0	32	0	0	0

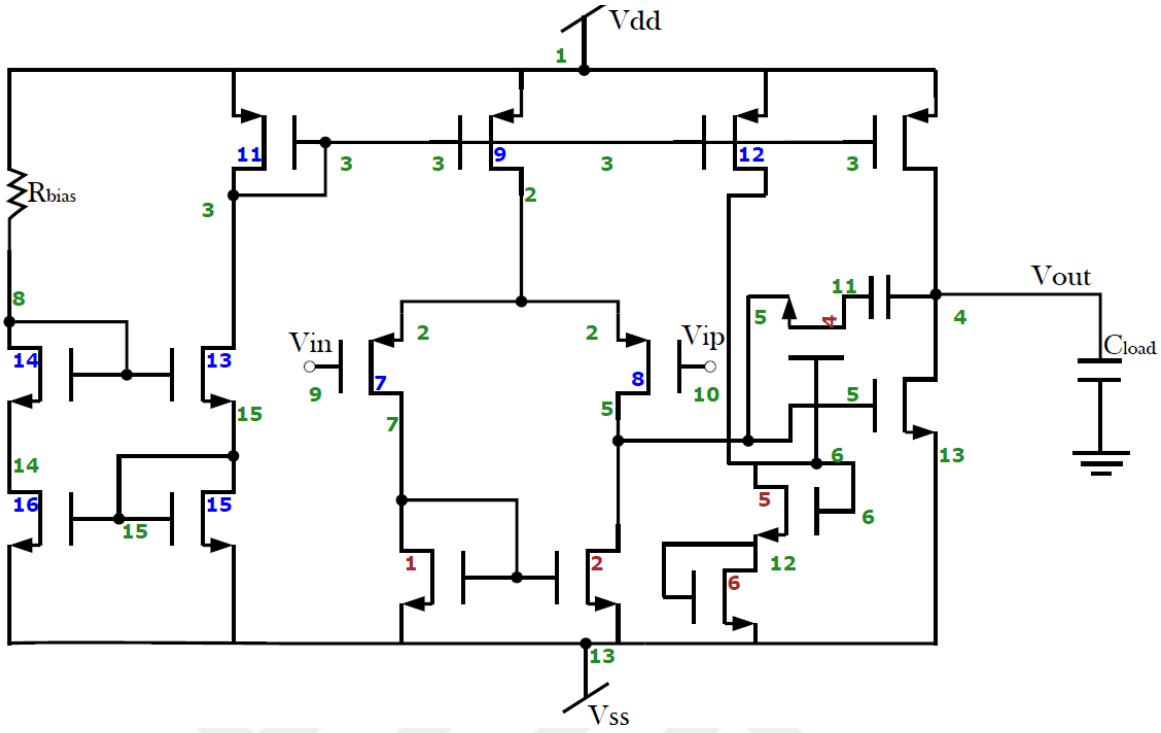

Figure 6.18. Circuit schematic of two stage OTA.

The two stage amplifier given in Figure 6.18 was utilized as another design under test example for the react operation search. This circuit has a p-type input differential pair, which is effected by NBTI. Considering circuit topology, the closed-loop gain and $3dB$ bandwidth of the amplifier depend on the transconductance of the input pair. Therefore, the react strategy was designed to recover the transconductance of the differential pair. There are two different approaches for this operation: renewing the differential pair and reinforcing the differential pair by adding supplementary devices.

The first approach was applied to this circuit by using the flow given in Figure 6.17 and simulation results are given in Figure 6.19. As can be seen from the results, all circuit specifications were successfully recovered by renewing only the differential pair transistors. Furthermore, an efficient signature (node 2) was obtained to determine whether the recovery operation is satisfied or not as proposed in Figure 6.17.

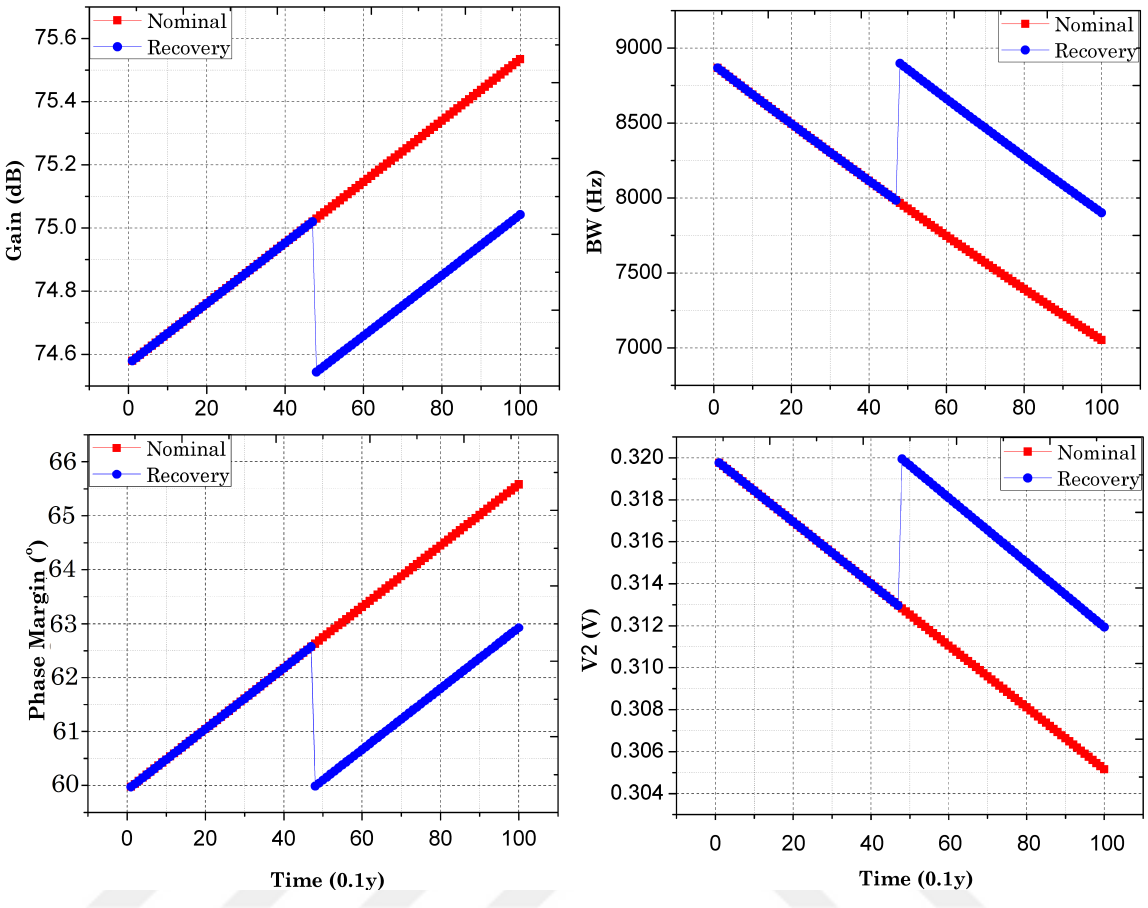

Figure 6.19. Simulation results of renewing approach for two stage OTA.

Another possible react operation for the two stage example is to reinforce the differential pair devices by adding supplementary devices. To illustrate this approach, additional transistor were connected to the related nodes on the circuit after a certain amount of aging occurs and simulation results are given in Figure 6.20. In this case, bandwidth and gain were also recovered, but the phase margin reduces negligibly. Again, node 2 can be recovered as well as the previous approach, which is then used to notice the success of the recovery operation.

6.2. Realization of Sense and React Approaches

To verify the proposed approaches in the previous section, two different sense and react systems were designed and simulated for each design under test examples (folded cascode and two stage OTA circuits).

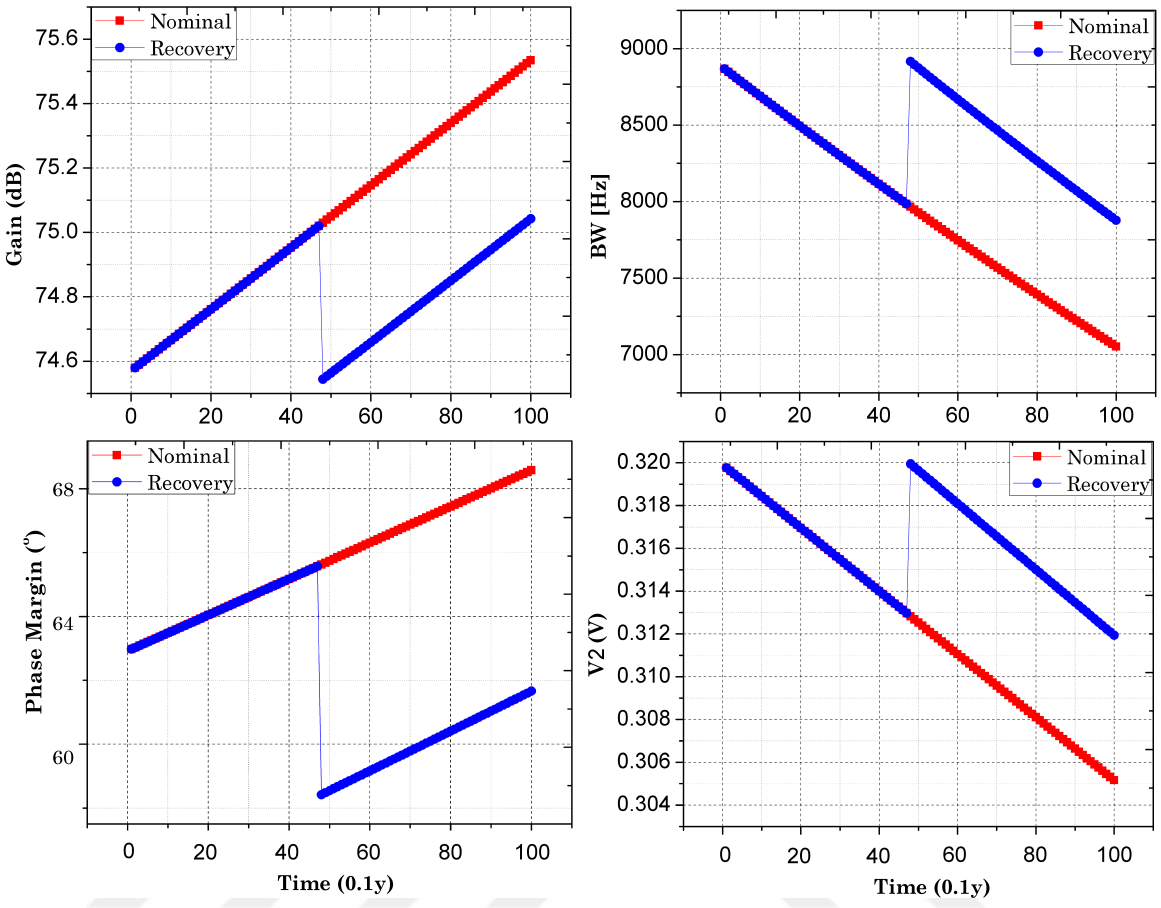

Figure 6.20. Simulation results of reinforcing approach for two stage OTA.

Node voltages were preferred as signatures to observe the aging and recovery information from the DUT devices for all developed systems. Therefore, a voltage comparator whose schematic given in Figure A.11 was utilized during sense operations. Specific evaluation blocks were designed for each sense and react system, since the type of react operations for the developed systems are unique for each approach. Two major S&R approaches are proposed in this thesis: *Discrete* and *Continuous*. In the discrete approach, S&R system is controlled by an external enable signal, thus, there is no additional power consumption for this approach since the peripheral devices are only active for a short duration. On the other hand, in the continuous approach, S&R system devices always operate as well as the actual circuit,; thus, it can sense and recover degradations at any time. Although this approach increases the power consumption, some critical applications may require such a system to protect the

circuit performance. Furthermore, both approaches can be applicable for several times by utilizing another signature that is still relevant with the circuit specifications even after the recovery operation.

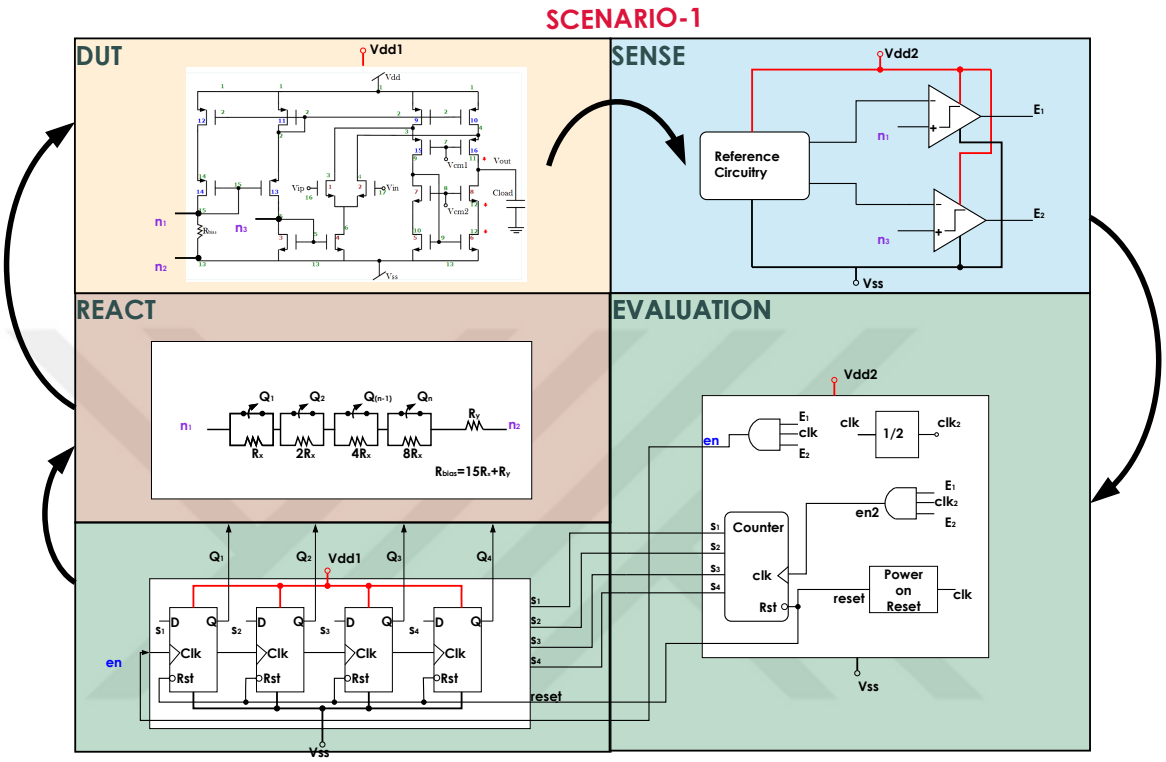

Figure 6.21. Schmeatic of the discrete approach for folded cascode example.

A comprehensive schematic of the first approach for the folded cascode OTA is given in Figure 6.21. The idea behind the approach is based on the deactivation of the required number of resistors in the bias resistor block, where the total resistor value is divided into small and different valued resistances that are controlled by switches. Thus, more current is provided to the circuit to compensate the aging effects. In the sense block, there are two comparators, which are named aging and recovery comparators, respectively. The first comparator senses the aging while the other is assigned to sense the recovery operation. In the evaluation block, a decimal counter, a clock divider, a power on reset circuit, and an AND gate are presented. The power on reset circuit generates a master reset signal for all flip-flops, when the recovery

operation is enabled. To guarantee the success of the recovery operation, the evaluation block should operate slower than the react block. Therefore, a clock divider is utilized to generate a slower clock signal for the counter. The counter is triggered by a master enable signal ("$en2$") that is generated by an AND gate, whose inputs are the slower clock signal ("$clk2$") and comparator outputs. The counter drives a flip-flop set, which is triggered by another enable signal ("en"). In the react part, a resistor set with different values is placed, which is controlled by normally on state switches that are driven by the flip-flop outputs ($Q_{1..4}$).

The system starts to work when the user activates the system and once the aging signature ($n1$) becomes lower than the reference signal. The aging comparator output becomes logic 1 and the evaluation block generates enable signals for the react operation. Meanwhile, the counter starts to count and the first resistor is deactivated. This cycle continues until the recovery comparator generates a logic '0', where all enable signals are pushed down to logic '0'. The counter stops to count and the flip-flop set saves the last states at the output until a new aging signal is generated from the aging comparator. Here, comparators and logic circuits in the evaluation block are supplied by a different power signal, which is controlled by the user, whereas the flip-flop set is supplied by the main power signal to maintain the last state.

A simulation output for the scenario-1 is provided in Figure 6.22. To simulate the total system, degraded model files are included into the simulator, where the bandwidth of the OTA decreased from $9.8kHz$ to $7.8kHz$. Change in the gain ($+3dB$) and phase margin (-3^0) values are negligible compared to the bandwidth. The nominal values of the aging signature and recovery signature are $320mV$ and $315mV$. When the system is activated, a master reset signal is generated for a while to initialize the all flip-flops, then the system starts to work. The counter counts up to 5, so resistor of $5R_x$ are deactivated. The recovery signature becomes closer to the initial value ($315mV$), so the recovery signal becomes logic 0 to stop the recovery system, where bandwidth of the amplifier becomes $9.6kHz$ after the recovery operation.

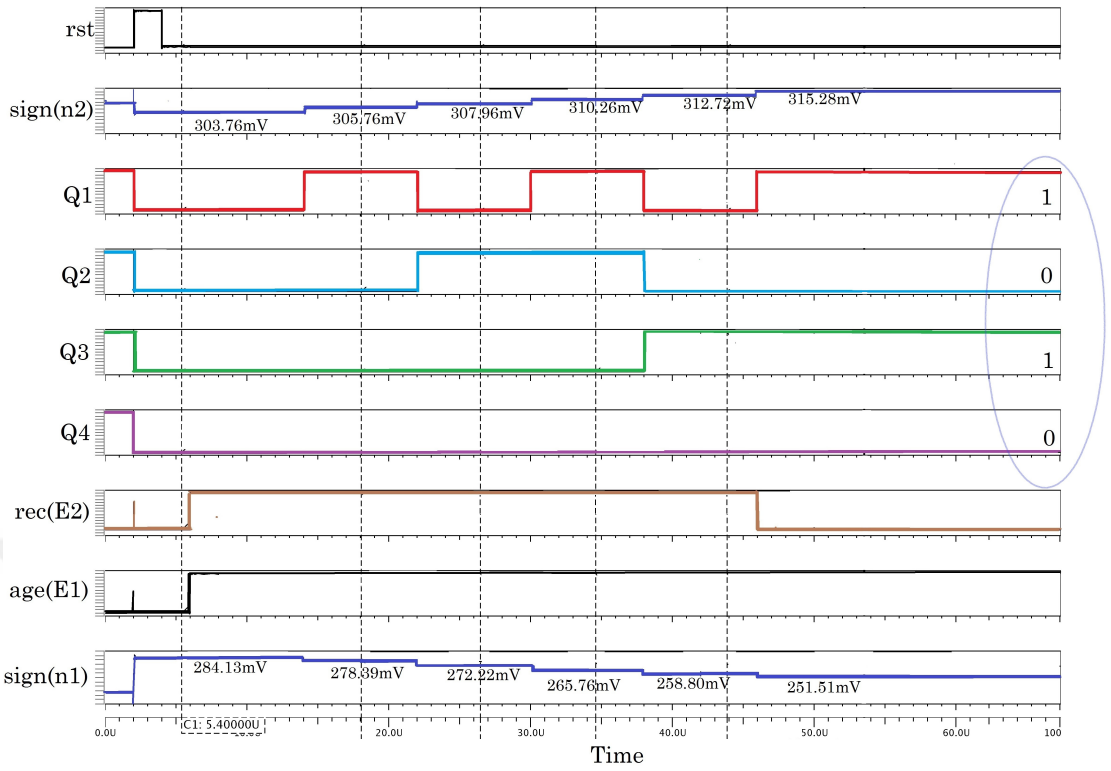

Figure 6.22. Simualtion results of the first approach for folded cascode circuit.

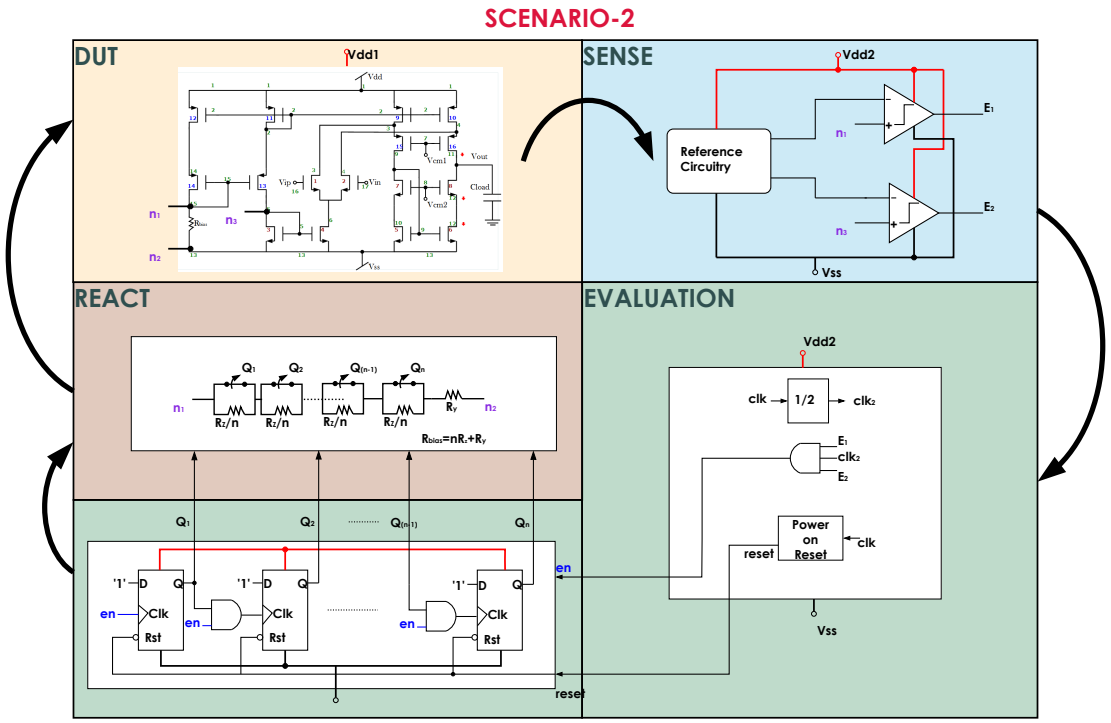

Figure 6.23. Schmeatic of the continous appraoch for the folded cascode OTA.

The schematic of the continuous approach for the folded cascode circuit is given in Figure 6.23. In this approach, S&R circuit starts to operate when the actual circuit is supplied. Therefore, a continuous recovery can be obtained. In the evaluation part, there are an AND gate, power on reset, and clock divider. Contrary to the former approach, the flip-flop block was designed considering the continuous approach. Therefore, inputs of the flip-flops were connected to logic '1', where flip-flop circuits behave as fuses for this case. In each cycle, one resistor is deactivated until the recovery signal becomes logic 0. To illustrate the system, a simulation result for the same circuit is provided in Figure 6.24.

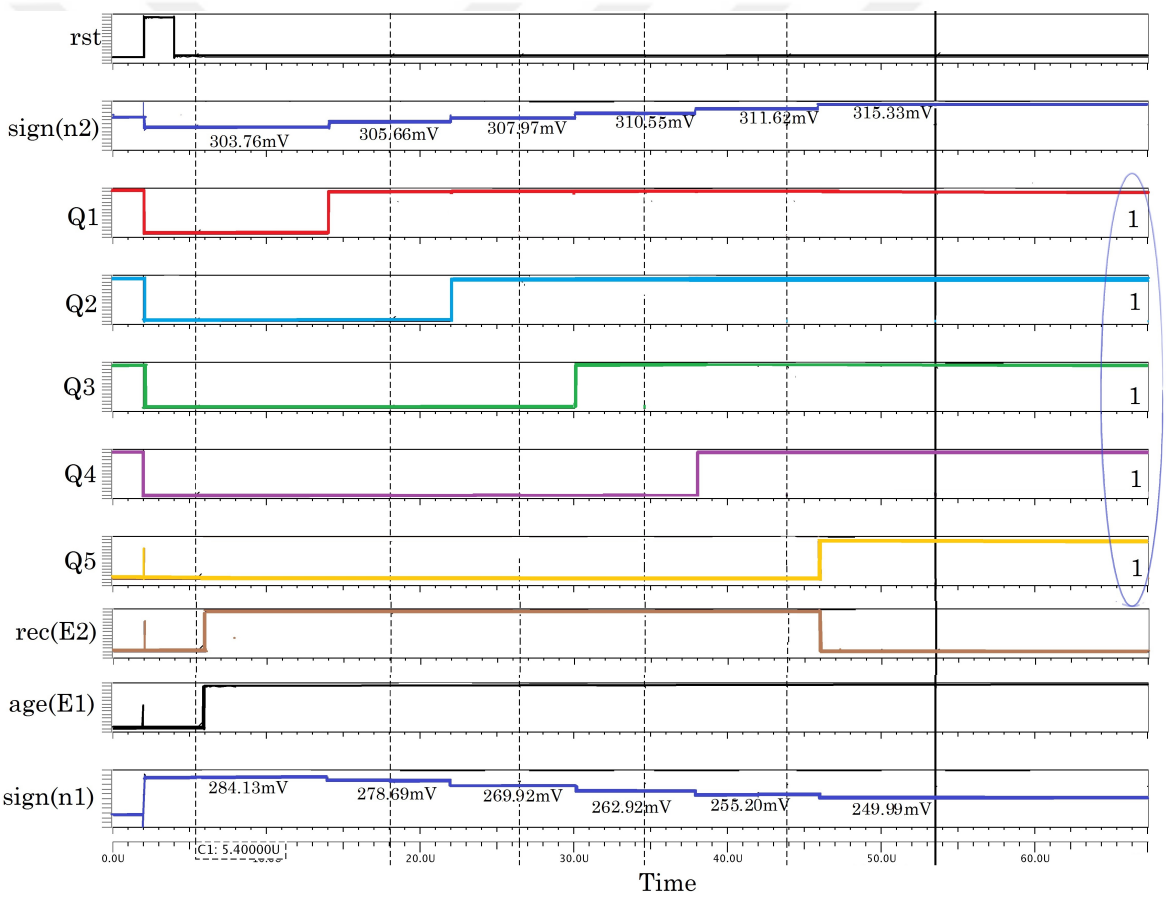

Figure 6.24. Simualtion results of the continous apparoch for the folded cascode OTA circuit.

As seen from the results, again $5R_x$ resistors were deactivated to recover the circuit. The value bandwidth of the bandwidth increased from $7.6kHz$ to $9.7kHz$,

where the nominal value is $9.8kHz$. The recovery signal ($n3$) becomes closer to its initial value ($315mV$) after the recovery operation. As seen from the simulation results, switches were permanently opened for this continuous approach.

The proposed schematic of the first approach for the two stage OTA is given in Figure 6.25.

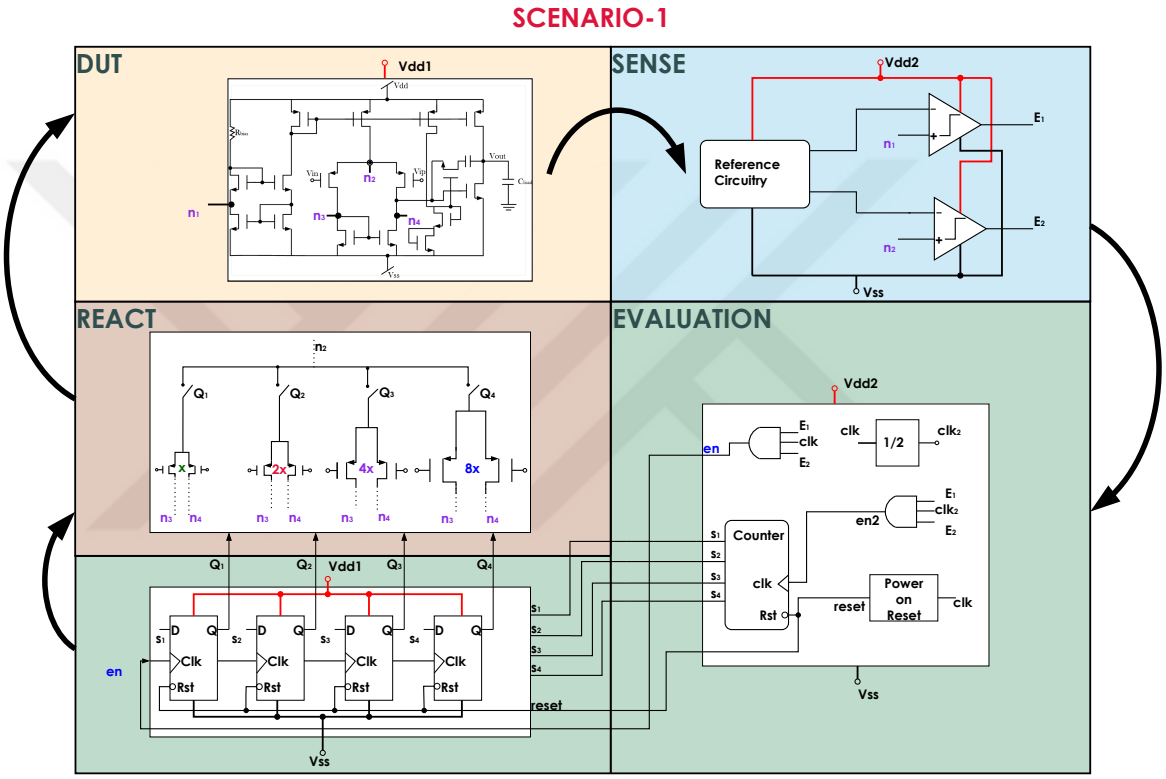

Figure 6.25. Schmeatic of the first sense and react appraoch for the two stage OTA.

The idea behind the approach is based on the activation of the required number of substitute transistors, where the differential pair transistors are reinforced to compensate the aging effects. Sense and evaluation block are the same with the folded cascode example. In contrast to the folded cascode example, a transistor set with different sizes are placed in the react part, which are controlled by switches that are driven by the flip-flop outputs ($Q_{1..4}$). The system starts to work when the user activates the system and once the aging signature ($n1$) becomes lower than the reference

signal. The aging comparator output becomes logic 1 and the evaluation block generates enable signals for the react operation. Meanwhile, the counter starts to count and the first transistor is activated. This cycle continues until the recovery comparator generates a logic '0', where all enable signals are pushed down to logic '0'. The counter stops to count and the flip-flop set saves the last states at the output until a new aging signal is generated from the aging comparator. Here, comparators and logic circuits in the evaluation block are supplied by a different power signal, which is controlled by the user, whereas the flip-flop set is powered by the main power signal to maintain the last state.

To demonstrate the proposed sense and react system, a simulation result for the two stage OTA is given in Figure 6.26. A degraded transistor model file was included to the design during the simulation, where the nominal and the aged values of bandwidth are $9.9kHz$ and $6.8kHz$. Changes in the gain ($+2dB$) and the phase margin($+3^0$) are both negligible.

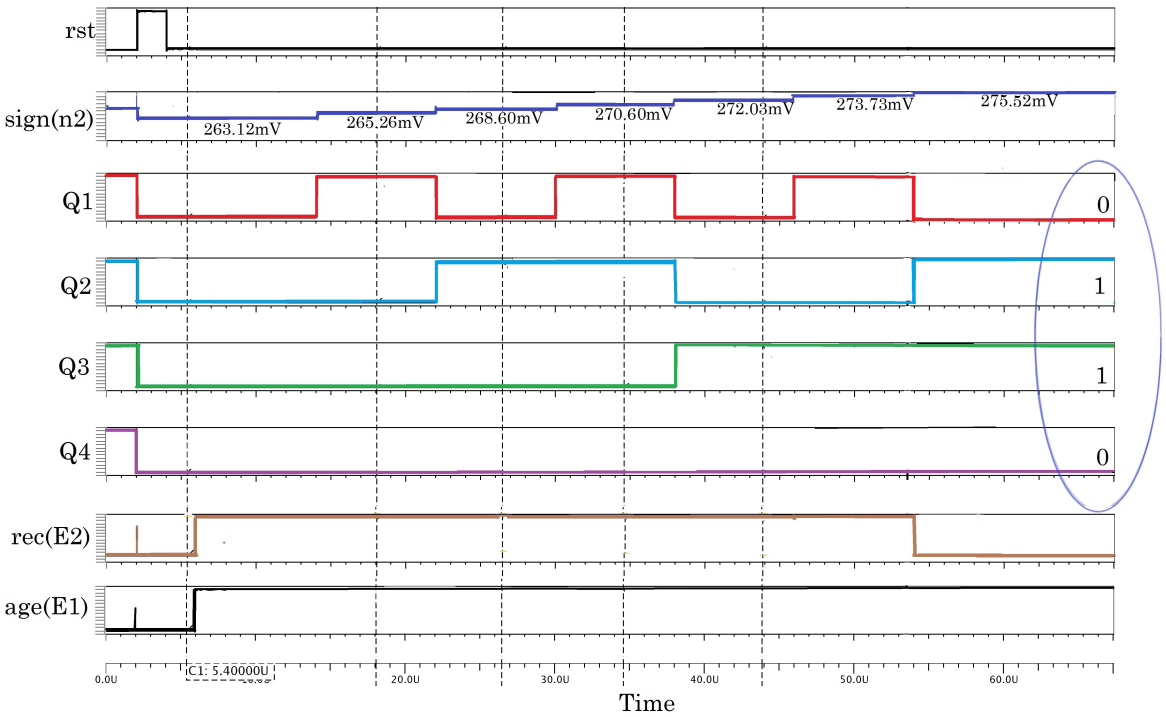

Figure 6.26. Simualtion results of the first apparoch for the two stage OTA circuit.

According to the simulation results, the counter counted up to 6 to recover the circuit, where the last substitute transistor was only activated while the others were still deactivated. The recovery signature ($n2$) increased from $263mV$ to $275mV$, whose fresh value is around $275mV$. After recovery, the bandwidth of the OTA increased to 10kHz, where gain and phase margin backed to their nominal values.

The schematic of the continuous approach for the two stage OTA is given in Figure 6.27. In this approach, S&R circuitry operates when the circuit is supplied as well as the folded cascode example. As a result, a continuous recovery can be performed for critical applications. In the evaluation part, there are an AND gate for the generation of the enable signal, power on reset, and clock divider. Contrary to the former approach, the flip-flop blocks are designed to provide permanent enable signals for the substitute transistors. Therefore, inputs of the flip-flops were connected to logic '1', where flip-flop circuits behave as fuse for this case. In each cycle, one transistor pair is included into the circuit until the recovery signal becomes logic 0.

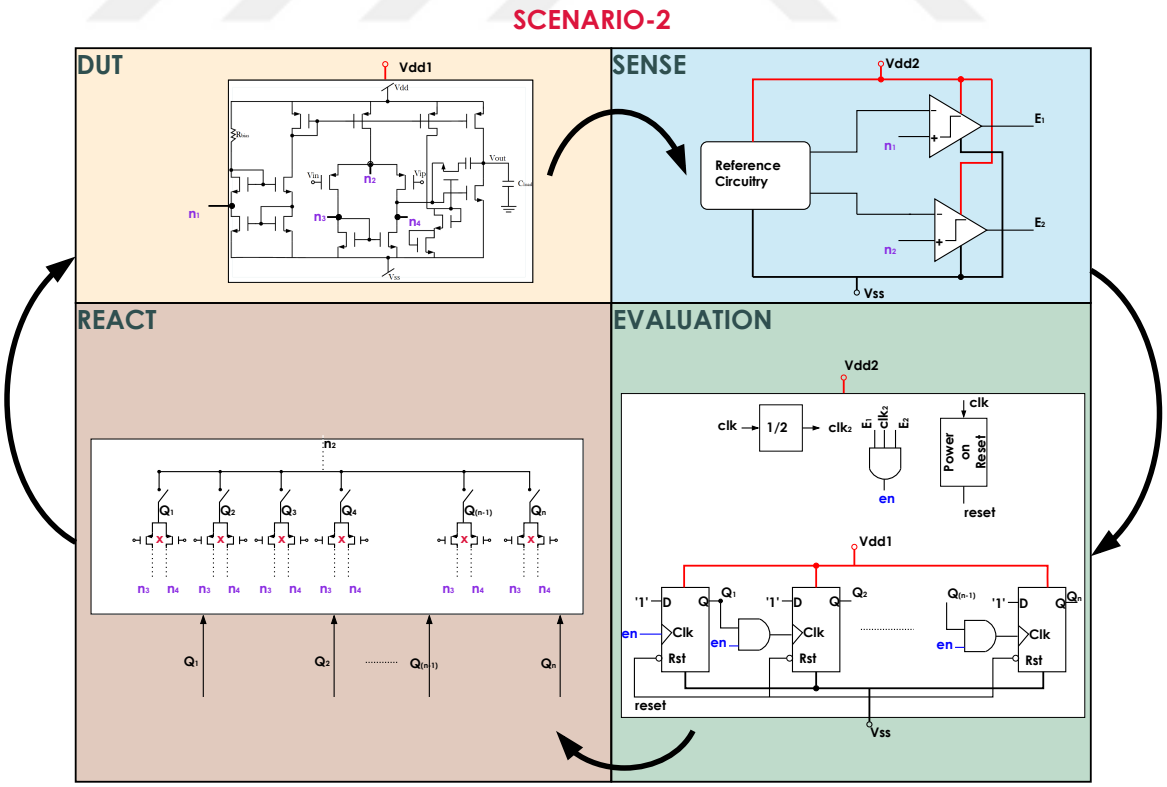

Figure 6.27. Schmeatic of the continuous appraoch for two stage OTA.

Simulation results of the continuous S&R approach for the two stage OTA are provided in Figure 6.28. Similar to the discrete approach, 6 substitute transistors were activated to recover the degradation in 3 dB bandwidth, where the nominal and the aged values of bandwidth are $9.9kHz$ and $7.5kHz$, respectively. Changes in the gain ($+1dB$) and the phase margin($+2^0$) are both ignorable.

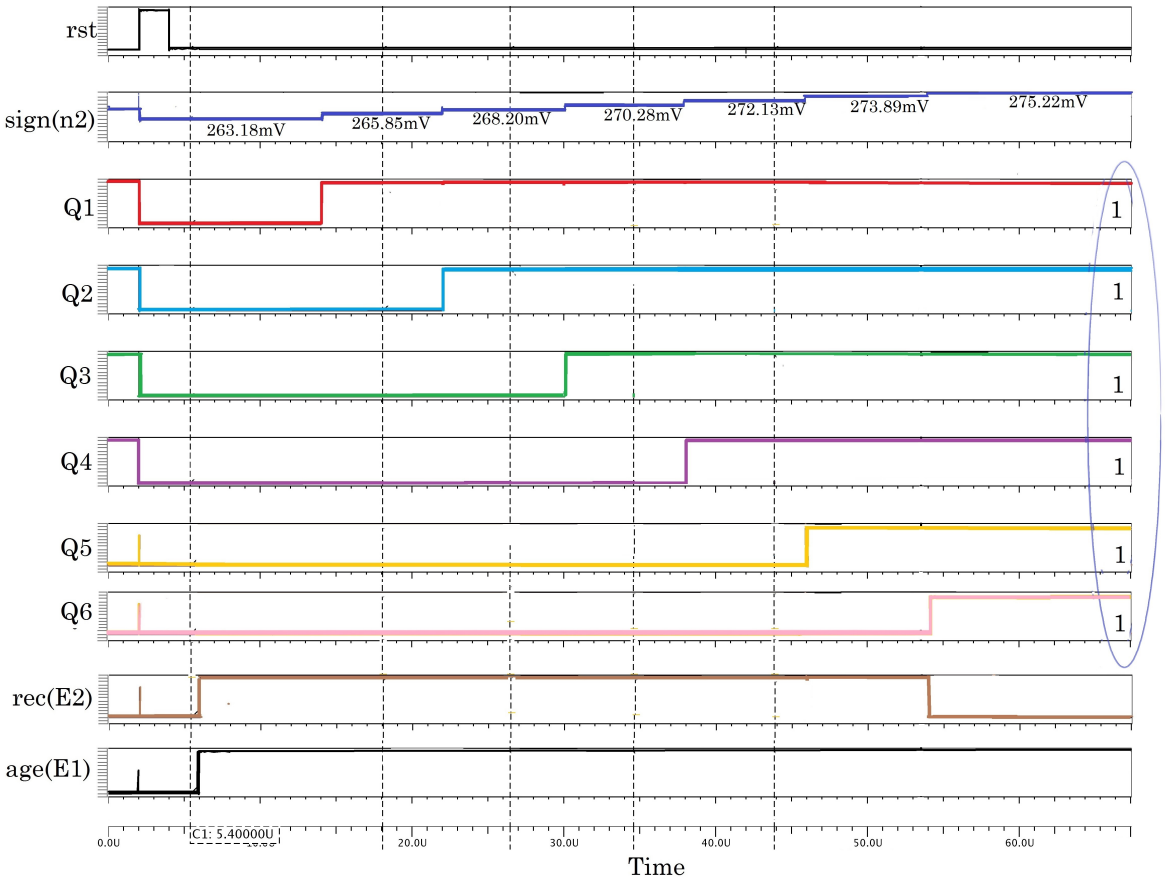

Figure 6.28. Simualtion results of the second apparoch for the two stage OTA.

Simulation results indicate that the evaluation block generated enable signals during 6 clock cycles, where the react block activated each of 6 transistors for each cycle. The system stopped working when the recovery comparator generates a logic 0, which means the DUT has recovered. After recovery, the bandwidth increased to $9.8kHz$, while the gain and the phase margin reached almost their initial (fresh) values.

6.3. Conclusion

Reconfigurable circuit design has become very important in the last decade for increasing the lifetime of CMOS circuits in deep sub-micron technologies. S&R approach is a popular reconfigurable design approach, which is based on sensing the degradation and activating the recovery to compensate the effects of aging effects. Indirect measurements are preferred to sense degradation, where electrical quantities of a signal are measured and mapped to the circuit performance changes. However, one should consider that an efficient signature should have certain properties such as applicability, measurability, relevancy, and reversibility. Traditionally, signature selection is performed by the designer in an iterative manner, which is highly inefficient, time consuming, and no procedure has been proposed for this process. To palliate this problem, a signature selection procedure and a novel tool for determining efficient signatures are proposed in this thesis. Evaluation and react approaches are also discussed in detail. Furthermore, different types of react operations are proposed and demonstrated on two different circuits. To perform react operations, a semi-automatic tool is presented, where the designer knowledge on the design under test provides insight during the determination of critical devices and evaluation of react operation results. By using all of these sub-blocks, two different S&R systems are designed for two different circuits. In the first approach, the S&R system is activated a master enable signal given by the user, so there is no extra power consumption for this approach. The chip area of course increases as a result of peripheral circuits around DUT. However, most of these peripheral circuits occupy considerably smaller areas, thus, this increase may be smaller than the chip area of overly-designed circuits, whose areas may be 2-3 times larger than a nominal circuit. In the second approach, the S&R system is always active when the actual circuit is supplied, which provides a continuous evaluation and instant sense and recovery capability to degraded devices. In this approach, power consumption increases due to continuous evaluation, but, some specific applications may require this approach, where degradation in the circuit specification is intolerable. The same comments for the area occupation is also valid for this approach.

7. CONCLUSION AND FUTURE WORK

CAD tools have been utilized for many years in order to assist to designer, where circuit design, simulation, analysis and verification, and manufacturing pre-processes have been performed via CAD tools. Afterwards, EDA tools have been developed and served to the market, which aimed to come with solutions providing automatic design (synthesis) and layout process, thus, the designer effort have began to reduce. Especially considering the market share of EDA industry for last ten years, it can be concluded that design automation systems have been emerged in order to reduce the time to market and cost.

Design automation systems for analog circuit design can be examined in two major categories: circuit sizing and layout generation. In circuit sizing, circuits are optimized at the schematic level, whereas layout generation deal with different problems at the layout level including floor-planning, placement, and routing. Design automation systems can be also divided into two categories, which are digital and analog automation systems. The design of the digital section of IC has been fully automated with a number of powerful tools such as digital circuit synthesis, layout generation, and verification tools etc. and a number of commercial tools have been utilized by the digital designers. However, analog circuit design automation is quite challenging problem due to non-linear behavior, compelling trade-offs between different design constraints, especially for advanced technology nodes.

Analog circuit sizing tools aim to automatically size circuits without designer effort. The earlier approaches needed a designer expertise during synthesis, then this need has been reduced and finally fully automated tools have been developed thanks to very high speed computers and advanced simulator tools. A simulation-based analog circuit sizing tool is proposed in this thesis, which is a modified version of a previous study. The developed tool utilizes HSPICE as performance evaluator, thus proving high accuracy. In addition to that a novel RF circuit synthesis tool is also introduced in this thesis, where a mixed-domain sizing is performed. Mixed domain sizing refers

to sizing at both electrical and physical levels, where electrical sizing is carried out for active circuit components, whereas passive elements are sized depending on their physical properties. Hence; layout-induced parasitics are taken into account during the circuit synthesis, which provides a substantial reduction in discrepancy between schematic level and post-layout simulations. Sophisticated physical models and equivalent electrical models provided by the foundry is utilized, and results are verified with two different examples.

However, increased reliability problems especially for sub-micron devices have created a new research area: reliability-aware analog circuit design automation, where reliability problems are considered during the synthesis process and the ultimate goal is expanded to meet the reliability requirement. Reliability problems in CMOS can be examined under two different subjects: variability and aging.

Variation-aware analog circuit design automation refers to sizing of circuits considering the variability problem. However, including variability into the conventional optimization problem is highly challenging due to the trade-off between efficiency and accuracy. Namely, fast variability analysis approaches suffer from accuracy problems, whereas accurate variability analysis leads to inefficiency in terms of synthesis time. Several approaches have been proposed in the literature, where both accuracy of the variability analysis and efficiency of the synthesis tools have been considered and solutions have been developed. This thesis examines variation-aware circuit synthesis utilizing two different variability analyses: sensitivity-based and QMC-based.

In sensitivity-based variation-aware analog circuit synthesis, the effect of changes in uncertain design parameters on circuit performances are individually evaluated and the total effect is estimated with linear approximation. Two different strategies are proposed for augmentation of variability analysis with sizing tool. In the first approach, design constraints are relaxed after the variation analysis results, thus, synthesis tool is obliged to overdesign, where the success rate of the tool (90%) is highly satisfying. However, power consumption and chip area are sacrificed for the sake of reliability in this case. In the second approach, variability is defined as a design constraint to be

satisfied, thus, the synthesis tool looks for the robust solutions without any increase in power consumption and chip area. However, the success rate of this approach is substantially worse (10%) than the over-design approach.

In QMC-based variation-aware circuit synthesis, two different QMC-based yield-aware analog circuit synthesis tools are proposed. Utilized process variation model parameters during MC simulations were extracted via experiments performed on a test chip. In this first tool, QMC is utilized during variability simulations to keep the sample size required for an accurate analysis at minimum. In additon to that, an ISE approach is presented to include yield estimation into the synthesis process in an efficient way, where variability analysis is applied for the solutions that satisfy the acceptance region determined by the user. This imprecise selection provides survived of reliable candidates satisfying the design constraints partially along with quite efficiency. Furthermore, an adaptive sample sizing algorithm for QMC samples is also developed to determine the efficient sample size in order to avoid unnecessary simulations. To demonstrate the developed tool, two different OTA circuits were synthesized. An expanded variability analysis is also performed for the candidate solutions where a simulation budget allocation algorithm is employed to share a pre-determined budget among all candidates. Synthesis results indicate that the synthesis tool prefers overdesign approach to generate reliable solutions, where power consumption and area constraints are somehow relaxed. The achieved yield values depend on the boundaries of the acceptance region, where a little bit relaxed constraints result with a yield of 100%, where hard design constraints result with yield values around 85-90%.

The second proposed tool promises a confidence interval of estimated yield. Since QMC is deterministic, the estimated yield values of a number of different runs will be the same, so there is no practical way to estimate the confidence interval. This second tool uses a scrambled-QMC used during sampling of uncertain, where generated QMC numbers are randomized by scrambling. However, at least three different runs are required to estimate the confidence interval, which would degrade the efficiency of the tool. To overcome this problem, the adaptive sample sizing approach is combined with scrambled QMC, where the step size is chosen somehow larger to create a variance

between two consecutive steps and estimate the confidence interval. Furthermore, existing of the solution yield within the confidence interval is guaranteed by evaluation of the lower limit of the interval as the yield of candidate. The same circuits were utilized during demonstration of the proposed tool, where a 1000 QMC is assigned to compare the results. Even though the average sample size increases, the average synthesis time is shorter than the previous tool thanks to a two step ISE, in which the second ISE is performed in order to eliminate low performing solutions in terms of yield. To verify the developed tool, a test chip including synthesized circuits was designed and measured. Measurement results are in consistent with estimations of the tool.

Aging is the other major reliability problem occurring in CMOS devices. In contrast to the variability problem, aging is a time dependent phenomena and have become a major reliability concern for technologies below 180 nm. HCI and NBTI are the most pronounced aging problems in CMOS devices, where both cause an increase in threshold voltage of devices. However, aging analysis (modelling and simulation) is quite problematic due to the time dependency. There are actually three different aging models in the literature: analytical models, semi-empirical models, and stochastic models. Analytical models are based on estimation of degradation using approximated analytical equations derived from physical background of these problems. Even though analytical models are widely used, the accuracy of such models change through different technology nodes. Therefore, semi-empirical models have been proposed, which are based on aging experiments performed on silicon for a given technology. The accuracy of such models is much better, but one should modify these types of models for each technology node. The last model has become popular in the last five years, where stochastic behavior of aging dominance the total effect especially devices with channel lengths less than 45 nm. A semi-empirical model development process is deeply discussed in this thesis from AAT to model fitting. Consequently, a semi-empirical model is proposed for NBTI for 130 nm technology, where no HCI effect was obtained during measurements. On the other hand, a deterministic aging simulator is also proposed to deal with the aging simulation problem. The proposed tool promises an adjustable

step size during simulations, thus avoiding redundant simulations during lifetime-aware analog circuit synthesis. To develop an aging-aware analog circuit synthesis tool, the developed aging simulator was integrated with the proposed analog circuit sizing tool. Similar to yield-aware synthesis, an ISE is utilized to manage the trade off between the lifetime and circuit specifications. In this tool, lifetime is considered as the reliability design constraint, which is estimated for candidates satisfying ISE boundaries. To avoid unnecessary simulations, the lifetime analysis is stopped for solutions that just start to violate any design constraint and complete the lifetime. To demonstrate the developed tool, the same circuits are utilized. Synthesis results indicate that the folded cascode circuit promises a longer lifetime compared to the two stage circuit. The possible reason is that the two stage circuit has an P-type input pair, which are exposed to NBTI, whereas the folded cascode has an N-type input transistor, thus, not suffering from NBTI. Moreover, to verify synthesis results, an expanded lifetime analysis with larger sample sizes were carried out for generated solutions.

The last subject of this thesis is reconfigurable analog circuit design, which is another way of increasing lifetime of analog circuits. S&R is a common approach to make circuits reconfigurable, which is based on sensing the degradation and enabling recovery operations to deal with aging phenomena. Sense operations are conventionally performed via indirect measurements since on chip direct measurement of a circuit feature is highly difficult. Indirect measurement is based on monitoring changes in measurable circuit quantities, which are called signatures. To reduce the cost of sense operation, one or more efficient signatures should be determined. However, this determination process is highly expensive to be performed manually since individual evaluation of each signature takes excessively longer time and no procedure has been proposed for this determination process. At first, the efficient signature concept is discussed in detail and properties of an efficient signature are determined, which are relevancy, measurability, applicability, and reversibility. By considering these properties, a signature selection tool is proposed in this thesis. The developed tool can be applied for any circuit with minimal modifications. Furthermore, a semi-automatic recovery determination procedure is also developed, which exploits an expert designer

insight to keep the design time at minimum. These signature selection and recovery determination tools substantially enhances the total design time of a S&R system. To illustrate the concept of a S&R system, two different approaches (continuous and discrete) are proposed and implemented for two different circuits. In continuous approaches, the system is enabled when the actual circuit is powered, thus, even small degradations can be recovered. Besides this fast response capability, this approach suffers from increase in power consumption, where the chip area is comparable with the solution that is generated via the lifetime-aware circuit sizing tool. On the other hand, the S&R system is only enabled when an external enable signal is applied in the discrete approach. Hence; there is no additional power consumption in this approach, where the chip area is the same with continuous approach. The only disadvantage of this approach is that an external enable signal is required to activate the S&R systems, thus, this type of system is incapable of recover instantaneous degradation.

Since there are a number of different subjects discussed in this thesis, future work of these different subjects are also separated to provide better understanding. On the side of analog circuit sizing, flat synthesis of complicated system is highly inefficient since enlarged optimization surface exponentially increase the synthesis time. Therefore, hierarchical synthesis of complicated ICs can be improved by developing new approaches by using the proposed single objective tool. Hierarchical analog circuit synthesis problem is addressed in Section 2.1.2 and two different model-based approaches are already proposed in [19], where they exploit macro-models for the system level description. However, the model dependency of this tool limits the use of tool for new circuits. Therefore, a model-free hierarchical synthesis approach may provide a wide range of use and get rid of time consuming model development process. With this regard, a model-free hierarchical synthesis tool is under construction as a future work. Moreover, another promising subject considering analog synthesis is the integration of the sizing tool with a layout generation, where a novel approach is proposed in [31]. Although the proposed tool promises a highly efficient integration, better results can be achieved by considering addressed problems. One future work can be analog intellectual properties (IPs). This subject has become very popular in

recent years. The main idea behind an analog IP is that rather than synthesizing a circuit scratch, an analog library including different types of analog circuits (amplifiers, filters, etc.) can be constructed and can be re-used when it is required. However, keeping all properties of an analog circuit in the library is highly expensive. Rather, Pareto fronts and front solutions can be obtained via a many objective optimization tool, saved in the library, and re-called when it is used. Meanwhile, the proposed single objective tool can be utilized to make a smooth search around the desired point on the Pareto front to achieve the best performing solution. Considering reliability-aware analog circuit sizing tool, the integration of yield-aware and lifetime-aware synthesis can be a novel future work that has not been studied yet. Of course, this integration would be very challenging due to the accuracy and efficiency balance, but, stochastic aging models are utilized for very deep sub-micron devices and evaluation requires a stochastic analysis rather than a deterministic approach as well as variation problem. Therefore, this integration process may become less problematic by utilizing stochastic aging models. Furthermore, aforementioned hierarchical and layout in the loop synthesis approaches can be made reliability-aware by including reliability analysis. Ultimately, the analog circuit synthesis can be completely closed by incorporating all of these into a single tool. A third test chip was designed by using the proposed approaches by Mohammed Ahmadlou and is being manufactured at the time of writing of this thesis. Measurement and silicon validation of the test chip is the immediate future work in this subject to verify the proposed approaches on silicon.

REFERENCES

1. Phelps, R., M. Krasnicki, R. A. Rutenbar, L. R. Carley and J. R. Hellums, "Anaconda: Simulation-based Synthesis of Analog Circuits via Stochastic Pattern Search", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 19, No. 6, pp. 703–717, 2000.

2. Asenov, A., S. Kaya and A. Brown, "Intrinsic Parameter Fluctuations in Decananometer MOSFETs Introduced by Gate Line Edge Roughness", *Electron Devices, IEEE Transactions on*, Vol. 50, No. 5, pp. 1254–1260, 2003.

3. Goodnick, S., D. Ferry, C. Wilmsen, Z. Liliental, D. Fathy and O. Krivanek, "Surface Roughness at the Si-SiO2 Interface", *Physical Review B, APS Journal of*, Vol. 32, No. 12, p. 8171, 1985.

4. Dumin, D., *Oxide Reliability: A Summary of Silicon Oxide Wearout, Breakdown, and Reliability*, Vol. 23, World Scientific, 2002.

5. Sönmez, Ö. S. and G. Dündar, "Simulation-based Analog and RF Circuit Synthesis Using a Modified Evolutionary Strategies Algorithm", *Integration, the VLSI journal*, Vol. 44, No. 2, pp. 144–154, 2011.

6. Harjani, R., R. A. Rutenbar and L. R. Carley, "OASYS: A Framework for Analog Circuit Synthesis", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 8, No. 12, pp. 1247–1266, 1989.

7. El-Turky, F. and E. E. Perry, "BLADES: An Artificial Intelligence Approach to Analog Circuit Design", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 8, No. 6, pp. 680–692, 1989.

8. Degrauwe, M. G., O. Nys, E. Dijkstra, J. Rijmenants, S. Bitz, B. L. Goffart, E. Vittoz, S. Cserveny, C. Meixenberger, G. Van Der Stappen *et al.*, "IDAC: An

Interactive Design Tool for Analog CMOS Circuits", *Solid-State Circuits, IEEE Journal of*, Vol. 22, No. 6, pp. 1106–1116, 1987.

9. Koh, H. Y., C. H. Sequin and P. R. Gray, "OPASYN: A Compiler for CMOS Operational Amplifiers", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 9, No. 2, pp. 113–125, 1990.

10. Gielen, G. G., H. C. Walscharts and W. M. Sansen, "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing", *Solid-State Circuits, IEEE Journal of*, Vol. 25, No. 3, pp. 707–713, 1990.

11. Van der Plas, G., G. Debyser, F. Leyn, K. Lampaert, J. Vandenbussche, G. G. Gielen, W. Sansen, P. Veselinovic and D. Leenarts, "AMGIE-A Synthesis Environment for CMOS Analog Integrated Circuits", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 20, No. 9, pp. 1037–1058, 2001.

12. Papadopoulos, S., R. Mack and R. Massara, "A Hybrid Genetic Algorithm Method for Optimizing Analog Circuits", *Circuits and Systems, Proceedings of the 43rd IEEE Midwest Symposium on*, Vol. 1, pp. 140–143, 2000.

13. Yuan, J., N. Farhat and J. VanderSpiegel, "GBOPCAD: A Synthesis Tool for High Performance Gain boosted OPAMP design", *Circuits and Systems I: Regular Papers, IEEE Transactions on*, Vol. 52, No. 8, pp. 1535–1544, 2005.

14. López, R. C., F. V. Fernández, Ó. Guerra-Vinuesa and Á. Rodríguez-Vázquez, *Reuse-based Methodologies and Tools in the Design of Analog and Mixed-signal Integrated Circuits*, Springer Science & Business Media, 2007.

15. Chang, H., *A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits*, Springer Science & Business Media, 1997.

16. Castro-López, R., A. Morgado, O. Guerra, R. del Río, J. de la Rosa, B. Pérez-

Verdú and F. V. Fernández, "Systematic Top-Down Design of Reconfigurable ΣΔ Modulators for Multi-Standard Transceivers", *Analog Integrated Circuits and Signal Processing*, Vol. 58, No. 3, pp. 227–241, 2009.

17. De Bernardinis, F., M. I. Jordan and A. SangiovanniVincentelli, "Support Vector Machines for Analog Circuit Performance Representation", *Proceedings of Design Automation Conference, IEEE Conference on*, pp. 964–969, 2003.

18. Martens, E. and G. Gielen, "Top-Down Heterogeneous Synthesis of Analog and Mixed Signal Systems", *Proceedings of Design, Automation and Test in Europe, IEEE Conference on*, pp. 275–280, 2006.

19. Afacan, E., S. Ay, F. V. Fernandez, G. Dundar and F. Başkaya, "Model Based Hierarchical Optimization Strategies for Analog Design Automation", *Proceedings of Design, Automation and Test in Europe Conference and Exhibition (DATE), IEEE Conference on*, pp. 1–4, 2014.

20. Castro-Lopez, R., O. Guerra, E. Roca and F. V. Fernández, "An Integrated Layout Synthesis Approach for Analog ICs", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 27, No. 7, pp. 1179–1189, 2008.

21. Vancorenland, P., G. Van der Plas, M. Steyaert, G. Gielen and W. Sansen, "A Layout-Aware Synthesis Methodology for RF Circuits", *Computer Aided Design, IEEE/ACM International Conference on*, pp. 358–362, 2001.

22. Dessouky, M. and M. Louerat, "A Layout Approach for Electrical and Physical Design Integration of High Performance Analog Circuits", *Proceedings of First International Quality Electronic Design, IEEE Symposium on*, pp. 291–298, 2000.

23. Agarwal, A., H. Sampath, V. Yelamanchili and R. Vemuri, "Fast and Accurate Parasitic Capacitance Models for Layout-Aware", *Proceedings of the 41st annual Design Automation, IEEE Conference on*, pp. 145–150, 2004.

24. Ranjan, M., W. Verhaegen, A. Agarwal, H. Sampath, R. Vemuri and G. Gielen, "Fast, Layout Inclusive Analog Circuit Synthesis Using Pre Compiled Parasitic Aware Symbolic Performance Models", *Proceedings of Design, Automation and Test in Europe, IEEE Conference on*, p. 10604, 2004.

25. Liao, Y.-C., Y.-L. Chen, X.-T. Cai, C.-N. Liu and T.-C. Chen, "LASER: Layout Aware Analog Synthesis Environment on Laker", *Proceedings of the 23rd International Conference on Great Lakes, ACM Symposium on VLSI*, pp. 107–112, 2013.

26. Zhang, L. and Z. Liu, "Directly Performance Constrained Template-based Layout Retargeting and Optimization for Analog Integrated Circuits", *Integration, the VLSI journal*, Vol. 44, No. 1, pp. 1–11, 2011.

27. Chen, Y.-L., Y.-C. Ding, Y.-C. Liao, H.-J. Chang and C.-N. Liu, "A Layout-Aware Automatic Sizing Approach for Retargeting Analog Integrated Circuits", *VLSI Design, Automation, and Test (VLSI-DAT), International Symposium on*, pp. 1–4, 2013.

28. Youssef, S., F. Javid, D. Dupuis, R. Iskander and M.-M. Louerat, "A Python-based Layout Aware Analog Design Methodology for Nanometric Technologies", *Design and Test Workshop (IDT), IEEE 6th International Conference on*, pp. 62–67, 2011.

29. Lourenço, N., A. Canelas, R. Póvoa, R. Martins and N. Horta, "Floorplan Aware Analog IC Sizing and Optimization based on Topological Constraints", *Integration, the VLSI Journal*, Vol. 48, pp. 183–197, 2015.

30. Habal, H. and H. Graeb, "Constraint-based Layout Driven Sizing of Analog Circuits", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 30, No. 8, pp. 1089–1102, 2011.

31. Berkol, G., A. Unutulmaz, E. Afacan, G. Dundar, F. V. Fernandez, A. E. Pusane

and F. Baskaya, "A Two-Step Layout in the Loop Design Automation Tool", *Proceedings of New Circuits and Systems Conference (NEWCAS), IEEE International Conference on*, pp. 1–4, 2015.

32. Conti, M., P. Crippa, S. Orcioni and C. Turchetti, "Parametric Yield Formulation of MOS IC's Affected by Mismatch Effect", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 18, No. 5, pp. 582–596, 1999.

33. Ye, Y., S. Gummalla, C.-C. Wang, C. Chakrabarti and Y. Cao, "Random Variability Modeling and Its Impact on Scaled CMOS Circuits", *Computational Electronics, IEEE Journal of*, Vol. 9, No. 3-4, pp. 108–113, 2010.

34. Tulunay, G., G. Dundar and A. Ataman, "A New Approach to Modeling Statistical Variations in MOS Transistors", *Circuits and Systems, ISCAS, IEEE International Symposium on*, Vol. 1, pp. I–757, 2002.

35. Cijan, G., T. Tuma and A. Burmen, "Modeling and Simulation of MOS Transistor Mismatch", *Proceedings of 6th Eurosim, IEEE International Symposium on*, pp. 1–8, 2007.

36. Lovett, S. J., M. Welten, A. Mathewson and B. Mason, "Optimizing MOS Transistor Mismatch", *Solid-State Circuits, IEEE Journal of*, Vol. 33, No. 1, pp. 147–150, 1998.

37. Lan, M.-F., A. Tammineedi and R. Geiger, "Current Mirror Layout Strategies for Enhancing Matching Performance", *Analog Integrated Circuits and Signal Processing, IEEE Journal of*, Vol. 28, No. 1, pp. 9–26, 2001.

38. Pelgrom, M. J., A. C. Duinmaijer and A. P. Welbers, "Matching Properties of MOS Transistors", *Solid-State Circuits, IEEE Journal of*, Vol. 24, No. 5, pp. 1433–1439, 1989.

39. Kinget, P. R., "Device Mismatch and Tradeoffs in the Design of Analog Circuits",

Solid-State Circuits, IEEE Journal of, Vol. 40, No. 6, pp. 1212–1224, 2005.

40. Serrano-Gotarredona, T. and B. Linares-Barranco, "A New Five Parameter MOS Transistor Mismatch Model", *Electron Device Letters, IEEE journal of*, Vol. 21, No. 1, pp. 37–39, 2000.

41. Drennan, P. G. and C. McAndrew, "A Comprehensive MOSFET Mismatch Model", *Proceedings of Electron Devices Meeting, International Symposium on*, pp. 167–170, 1999.

42. McAndrew, C. C., J. Bates, R. T. Ida and P. Drennan, "Efficient Statistical BJT Modeling, Why β is More Than Ic/Ib", *Proceedings of Bipolar/BiCMOS Circuits and Technology Meeting, IEEE conference on*, pp. 28–31, 1997.

43. Drennan, P. G., C. C. McAndrew and J. Bates, "A Comprehensive Vertical BJT Mismatch Model", *Proceedings of Bipolar/BiCMOS Circuits and Technology Meeting, IEEE conference on*, pp. 83–86, 1998.

44. Afacan, E., *Aging in CMOS Circuits and Analog Circuit Design Robust Aging Phenomena*, Master's Thesis, Bogazici University, 2011.

45. Groeseneken, G., R. Degraeve, B. Kaczer and P. Roussel, "Recent Trends in Reliability Assessment of Advanced CMOS Technologies", *Proceedings of Microelectronic Test Structures, IEEE International Conference on*, pp. 81–88, 2005.

46. Alam, M. A. and S. Mahapatra, "A Comprehensive Model of PMOS NBTI Degradation", *Microelectronics Reliability, Journal of*, Vol. 45, No. 1, pp. 71–81, 2005.

47. Mourrain, C., C. Tourniol and M. J. Bouzid, *Electrical Parameters Degradation Law of MOSFET During Aging*, Elsevier, 1998.

48. Radojcic, R., "Hot-Electron Aging in P-Channel MOSFETs for VLSI CMOS", *Electron Devices, IEEE Transactions on*, Vol. 31, No. 12, pp. 12–14, 1984.

49. Choi, J. Y., P. K. Ko and C. Hu, "Hot-Carrier-Induced MOSFET Degradation Under AC Stress", *Electron Devices, IEEE Transactions on*, Vol. 8, No. 8, pp. 333–335, 1987.

50. Koike, N. and K. Tatsuuma, "A Drain Avalanche Hot Carrier Lifetime Model for N- and P-Channel MOSFETs", *Device and Materials Reliability, IEEE Transactions on*, Vol. 4, No. 3, pp. 457–466, 2004.

51. Takeda, E., A. Shimizu and T. Hagiwara, "Role of Hot-Hole Injection in Hot-Carrier Effects and the Small Degraded Channel Region in MOSFETs", *Electron Devices, IEEE Transactions on*, Vol. 4, No. 9, pp. 329–331, 1983.

52. Tsuchiya, T., Y. Okazaki, M. Miyake and T. Kobayashi, "New Hot-Carrier Degradation Mode and Lifetime Prediction Method in Quarter-Micrometer PMOSFET", *Electron Devices, IEEE Transactions on*, Vol. 39, No. 2, pp. 404–408, 1992.

53. Choi, J. Y., P. K. Ko and C. Hu, "Hot-Carrier-Induced Degradation of Metal-Oxide-Semiconductor Field-Effect Transistors: Oxide Charge Versus Interface Traps", *Applied Physics, IEEE Journal of*, Vol. 65, No. 2, pp. 354–360, 1989.

54. Takeda, E., A. Shimizu and T. Hagiwara, "Device Performance Degradation to Hot-Carrier Injection at Energies Below the $Si - SiO_2$ Energy Barrier", *Proceedings of Electron Devices Meeting, International Conference on*, Vol. 29, pp. 396–399, 1983.

55. Cretu, B., F. Balestra and G. Ghibaudo, "Hot Carrier Stress in Deep Submicrometer MOSFETs", *Proceedings of Semiconductor, International Conference ON*, Vol. 2, pp. 507–510, 2001.

56. Cottrell, P. E., R. R. Troutman and T. H. Ning, "Hot-Electron Emission in N-Channel IGFETs", *Solid-State Circuits, IEEE Journal of*, Vol. 14, No. 2, pp. 442–455, 1979.

57. Tam, S., P. K. Ko and C. Hu, "Lucky-Electron Model of Channel Hot-Electron Injection in MOSFET's", *Electron Devices, IEEE Transactions on*, Vol. 31, No. 9, pp. 1116–1125, 1984.

58. Entner, R., *Modeling and Simulation of Negative Bias Temperature Instability*, Ph.D. Thesis, Wien Technical University, 2007.

59. Zafar, S., A. Kumar, E. Gusev and E. Cartier, "Threshold Voltage Instabilities in High-κ Gate Dielectric Stacks", *Device and Materials Reliability, IEEE Transactions on*, Vol. 5, No. 1, pp. 45–64, 2005.

60. Zafar, S., Y. Kim, V. Narayanan, C. Cabral, V. Paruchuri, B. Doris, J. Stathis, A. Callegari and M. Chudzik, "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO2/HfO2 Stacks with FUSI, TiN, Re Gates", *Proceedings of VLSI Technology, IEEE Symposium on*, pp. 23–25, 2006.

61. Vattikonda, R., W. Wang and Y. Cao, "Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design", *Proceedings of the 43rd annual Design Automation, ACM International Conference on*, pp. 1047–1052, 2006.

62. Chakravarthi, S., A. Krishnan, V. Reddy, C. Machala and S. Krishnan, "A Comprehensive Framework for Predictive Modeling of Negative Bias Temperature Instability", *Proceedings of Reliability Physics, IEEE International Symposium on*, pp. 273–282, 2004.

63. Dumin, D., *Oxide Reliability: A summary of Silicon Oxide Wearout, Breakdown, and Reliability*, Vol. 23, World Scientific, 2002.

64. Degraeve, R., G. Groeseneken, R. Bellens, M. Depas and H. E. Maes, "A Consistent Model for the Thickness Dependence of Intrinsic Breakdown in Ultra-Thin Oxides", *Proceedings of Electron Devices Meeting, IEEE International Symposium on*, pp. 863–866, 1995.

65. Lin, H., D. Lee, C. Lee, T. Chao, T. Huang and T. Wang, "New Insights Into Breakdown Modes and Their Evolution in Ultra-Thin Gate Oxide", *Proceedings ofVLSI Technology, Systems, and Applications, IEEE International Symposium on*, pp. 37–40, 2001.

66. Depas, M., T. Nigam and M. M. Heyns, "Soft Breakdown of Ultra-Thin Gate Oxide Layers", *Electron Devices, IEEE Transactions on*, Vol. 43, No. 9, pp. 1499–1504, 1996.

67. Azizi, N. and P. Yiannacouras, "Gate Oxide Breakdown", *Reliability of Integrated Circuits*, Vol. 4, No. 1, pp. 149–150, 2003.

68. Black, J. R., "Electromigration—A Brief Survey and Some Recent Results", *Electron Devices, IEEE Transactions on*, Vol. 16, No. 4, pp. 338–347, 1969.

69. Kraft, O., J. Sanchez, M. Bauer and E. Arzt, "Quantitative Analysis of Electromigration Damage in Al-based Conductor Lines", *Materials Research, Cambridge Journal of*, Vol. 12, No. 08, pp. 2027–2037, 1997.

70. Loh, W. B., M. S. Tse, L. Chan and K. F. Eo, "Wafer Level Electromigration Reliability Test for Deep-Submicron Interconnect Metallization", *Proceedings of Electron Devices Meeting, IEEE Journal of*, pp. 157–160, 1998.

71. Maulik, P. C., L. R. Carley and R. A. Rutenbar, "Integer Programming based Topology Selection of Cell-Level Analog Circuits", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 14, No. 4, pp. 401–412, 1995.

72. Harvey, J. P., M. I. Elmasry and B. Leung, "STAIC: An Interactive Framework for Synthesizing CMOS and BiCMOS Analog Circuits", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 11, No. 11, pp. 1402–1417, 1992.

73. Gielen, G. G., E. Maricau and P. De Wit, "Designing Reliable Analog Circuits in An Unreliable World", *Proceedings of Custom Integrated Circuits, IEEE Conference on*, pp. 1–4, 2012.

74. Keane, J., T. Kim and C. H. Kim, "An On-Chip NBTI Sensor for Measuring PMOS Threshold Voltage Degradation", *Semiconductor Manifacturing, IEEE Transactions on*, Vol. 18, No. 6, pp. 947–956, 2010.

75. Kang, K., S. P. Park, K. Kim and K. Roy, "On-chip Variability Sensor Using Phase-Locked Loop for Detecting and Correcting Parametric Timing Failures", *Very Large Scale Integration (VLSI) Systems, IEEE transactions on*, Vol. 18, No. 2, pp. 270–280, 2010.

76. Mostafa, H., M. Anis and M. Elmasry, "NBTI and Process Variations Compensation Circuits Using Adaptive Body Bias", *Semiconductor Manufacturing, IEEE Transactions on*, Vol. 25, No. 3, pp. 460–467, 2012.

77. Afacan, E., G. Dundar and F. Baskaya, "Reliability Assessment of CMOS Differential Cross-Coupled LC Oscillators and A Novel on Chip Self-Healing Approach Against Aging Phenomena", *Microelectronics Reliability, Elsevier Journal of*, Vol. 54, No. 2, pp. 397–403, 2014.

78. Maaranen, H., K. Miettinen and M. M. Mäkelä, "Quasi-Random Initial Population for Genetic Algorithms", *Computers & Mathematics with Applications*, Vol. 47, No. 12, pp. 1885–1895, 2004.

79. Alpaydin, G., S. Balkir and G. Dündar, "An Evolutionary Approach to Automatic Synthesis of High Performance Analog Integrated Circuits", *Evolutionary Computation, IEEE Transactions on*, Vol. 7, No. 3, pp. 240–252, 2003.

80. Eiben, A. E. and J. E. Smith, *Introduction to Evolutionary Computing*, Springer, 2003.

81. Mahfoud, S. W. and D. E. Goldberg, "Parallel Recombinative Simulated Annealing: A Genetic Algorithm", *Parallel computing*, Vol. 21, No. 1, pp. 1–28, 1995.

82. Kirkpatrick, S., "Optimization by Simulated Annealing: Quantitative Studies", *Journal of statistical physics*, Vol. 34, No. 5-6, pp. 975–986, 1984.

83. Ingber, L., "Very Fast Simulated Re-annealing", *Mathematical and computer modelling*, Vol. 12, No. 8, pp. 967–973, 1989.

84. Leenaerts, D., G. Gielen and R. A. Rutenbar, "CAD Solutions and Outstanding Challenges for Mixed-Signal and RF-IC Design", *Proceedings of Computer-aided design, IEEE/ACM International Conference on*, pp. 270–277, 2001.

85. Park, J., K. Choi and D. J. Allstot, "Parasitic-Aware RF Circuit Design and Optimization", *Circuits and Systems I: Regular Papers, IEEE Transactions on*, Vol. 51, No. 10, pp. 1953–1966, 2004.

86. Agarwal, A. and R. Vemuri, "Layout-Aware RF Circuit Synthesis Driven by Worst Case Parasitic Corners", *Proceedings of Computer Design: VLSI in Computers and Processors, IEEE International Conference on*, pp. 444–449, 2005.

87. Berkol, G., A. Unutulmaz, E. Afacan, G. Dundar, F. V. Fernandez, A. E. Pusane and F. Baskaya, "A Two-Step Layout in the Loop Design Automation Tool", *Proceedings of New Circuits and Systems Conference (NEWCAS), IEEE International Conference on*, pp. 1–4, 2015.

88. Yue, C. P. and S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon", *Electron Devices, IEEE Transactions on*, Vol. 47, No. 3, pp. 560–568, 2000.

89. Gao, W. and Z. Yu, "Scalable Compact Circuit Model and Synthesis for RF CMOS Spiral Inductors", *Microwave Theory and Techniques, IEEE Transactions on*, Vol. 54, No. 3, pp. 1055–1064, 2006.

90. Cao, Y., R. A. Groves, X. Huang, N. D. Zamdmer, J.-O. Plouchart, R. A. Wachnik, T.-J. King and C. Hu, "Frequency Independent Equivalent Circuit Model for On Chip Spiral Inductors", *Solid-State Circuits, IEEE Journal of*, Vol. 38, No. 3, pp. 419–426, 2003.

91. Hong, J.-P. and S.-G. Lee, "Low Phase Noise Gm Boosted Differential Gate-to-Source Feedback Colpitts CMOS VCO", *Solid-State Circuits, IEEE Journal of*, Vol. 44, No. 11, pp. 3079–3091, 2009.

92. Tiwary, S. K., P. K. Tiwary and R. A. Rutenbar, "Generation of Yield-Aware Pareto Surfaces for Hierarchical Circuit Design Space Exploration", *Proceedings of the 43rd Annual Design Automation, ACM International Conference on*, pp. 31–36, 2006.

93. Afacan, E., G. Berkol, A. E. Pusane, G. Dündar and F. Başkaya, "Adaptive Sized Quasi-Monte Carlo based Yield Aware Analog Circuit Optimization Tool", *Proceedings of the 5th European Workshop on CMOS Variability (VARI), IEEE Conference on*, pp. 1–6, 2014.

94. Afacan, E., G. Berkol, F. Başkaya and G. Dündar, "Sensitivity Based Methodologies for Process Variation Aware Analog IC Optimization", *Ph. D. Research in Microelectronics and Electronics (PRIME), IEEE Conference on*, pp. 1–4, 2014.

95. Tulunay, G., G. Dundar and A. Ataman, "A new approach to modeling statistical variations in MOS transistors", *Proceedings of Circuits and Systems, IEEE International Symposium on*, Vol. 1, pp. 754–757, 2002.

96. Schwencker, R., F. Schenkel, M. Pronath and H. E. Graeb, "Analog Circuit Sizing Using Adaptive Worst-Case Parameter Sets", *Proceedings of Design, Automation & Test in Europe, IEEE Conference on*, pp. 0581–0581, 2002.

97. Barros, M., J. Guilherme and N. Horta, "Analog Circuits Optimization based on Evolutionary Computation Techniques", *Integration, the VLSI journal*, Vol. 43,

No. 1, pp. 136–155, 2010.

98. Dharchoudhury, A. and S.-M. Kang, "Worst-Case Analysis and Optimization of VLSI Circuit Performances", *Computer-Aided Design Integration Circuits Systems, IEEE Transactions on*, Vol. 14, No. 4, pp. 481–492, 1995.

99. Okobiah, O., S. P. Mohanty and E. Kougianos, "Ordinary Kriging Metamodel-Assisted Ant Colony Algorithm for Fast Analog Design Optimization", *Proceedings of Quality Electronic Design (ISQED), International Symposium on*, pp. 458–463, 2012.

100. Li, X., Y. Zhan and L. T. Pileggi, "Quadratic Statistical Approximation for Parametric Yield Estimation of Analog/RF Integrated Circuits", *Computer-Aided Design Integration Circuits Systems, IEEE Transactions on*, Vol. 27, No. 5, pp. 831–843, 2008.

101. Li, X., P. Gopalakrishnan, Y. Xu and L. T. Pileggi, "Robust analog/RF circuit design with projection-based performance modeling", *Computer-Aided Design Integration Circuits Systems,IEEE Transactions on*, Vol. 26, No. 1, pp. 2–15, 2007.

102. Seaholm, S. K., E. Ackerman and S.-C. Wu, "Latin Hypercube Sampling and the Sensitivity Analysis of a Monte Carlo Epidemic Model", *Bio-Medical Computing, International Journal of*, Vol. 23, No. 1, pp. 97–112, 1988.

103. Singhee, A., S. Singhal and R. A. Rutenbar, "Practical, Fast Monte Carlo Statistical Static Timing Analysis: Why and How", *Proceedings of Computer-Aided Design, IEEE/ACM International Conference on*, pp. 190–195, 2008.

104. Singhee, A. and R. A. Rutenbar, "Why Quasi-Monte Carlo is Better Than Monte Carlo or Latin Hypercube Sampling for Statistical Circuit Analysis", *Computer-Aided Design Integration Circuits Systems, IEEE Transactions on*, Vol. 29, No. 11, pp. 1763–1776, 2010.

105. Liu, B., F. V. Fernández and G. G. Gielen, "Efficient and Accurate Statistical Analog Yield Optimization and Variation-Aware Circuit Sizing based on Computational Intelligence Techniques", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 30, No. 6, pp. 793–805, 2011.

106. Mutlu, A. A., N. G. Gunther and M. Rahman, "Concurrent Optimization of Process Dependent Variations in Different Circuit Performance Measures", *Proceedings of Circuits and Systems, IEEE International Symposium on*, Vol. 4, pp. IV–692, 2003.

107. Lemieux, C., *Monte Carlo and Quasi-Monte Carlo Sampling*, Springer, 2009.

108. Niederreiter, H. and C. Xing, *Monte Carlo and Quasi-Monte Carlo Methods*, Springer, 1998.

109. Berkol, G., *Novel Design Methods for Analog Design Atutomation Tools*, Master's Thesis, Bogazici Univesity, 2015.

110. Singhee, A., S. Singhal and R. A. Rutenbar, "Practical, Fast Monte Carlo Statistical Static Timing Analysis: Why and How", *Proceedings of Computer-Aided Design, IEEE/ACM International Conference on*, pp. 190–195, 2008.

111. Singhee, A., *Novel Algorithms for Fast Statistical Analysis of Scaled Circuits*, Ph.D. Thesis, Carnegie Mellon University, 2007.

112. Hlawka, E., "Funktionen von beschränkter variation in der theorie der gleichverteilung", *Annali di Matematica Pura ed Applicata*, Vol. 54, No. 1, pp. 325–333, 1961.

113. Halton, J. H., "On the Efficiency of Certain Quasi-Random Sequences of Points in Evaluating Multi-Dimensional Integrals", *Numerische Mathematik*, Vol. 2, No. 1, pp. 84–90, 1960.

114. Sobol, I. M., "Uniformly Distributed Sequences with An Additional Uniform Property", *Computational Mathematics and Mathematical Physics, Elsevier Journal of*, Vol. 16, No. 5, pp. 236–242, 1976.

115. Faure, H., "Discrepancy of Sequences Associated with A Number System (in Dimension s)", *Acta Arithmetica*, Vol. 41, No. 4, pp. 337–351, 1982.

116. Niederreiter, H., "Low-Discrepancy and Low-Dispersion Sequences", *Number Theory, Elsevier Journal of*, Vol. 30, No. 1, pp. 51–70, 1988.

117. Chi, H., *Scrambled Quasirandom Sequences and Their Applications*, Ph.D. Thesis, Florida State University, 2004.

118. McConaghy, T., P. Palmers, M. Steyaert and G. G. Gielen, "Variation-Aware Structural Synthesis of Analog Circuits via Hierarchical Building Blocks and Structural Homotopy", *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Vol. 28, No. 9, pp. 1281–1294, 2009.

119. Kullback, S. and R. A. Leibler, "On Information and Sufficiency", *The Annals of Mathematical Statistics, JSTOR Journal of*, pp. 79–86, 1951.

120. Chen, C.-H., J. Lin, E. Yücesan and S. E. Chick, "Simulation Budget Allocation for Further Enhancing the Efficiency of Ordinal Optimization", *Discrete Event Dynamic Systems, Elsevier Journal of*, Vol. 10, No. 3, pp. 251–270, 2000.

121. Chen, H.-C., C.-H. Chen and E. Yucesan, "Computing Efforts Allocation for Ordinal Optimization and Discrete Event Simulation", *Automatic Control, IEEE Transactions on*, Vol. 45, No. 5, pp. 960–964, 2000.

122. Owen, A. B., *Randomly Permuted (t, m, s)-Nets and (t, s)-Sequences*, Springer, 1995.

123. Chi, H., *Scrambled Quasirandom Sequences and Their Applications*, Ph.D. The-

sis, Florida State University, 2004.

124. L'Ecuyer, P. and C. Lemieux, Springer, 2005.

125. Batur, O. Z., *Robust Ultra-WİdeBand TransceİVer Integrated Circuit Design*, Ph.D. Thesis, Bogazici University, 2015.

126. Gielen, G. and E. Maricau, "Stochastic Degradation Modeling and Simulation for Analog Integrated Circuits in Nanometer CMOS", *Proceedings of Design, Automation & Test in Europe, IEEE Conference on*, pp. 326–331, 2013.

127. Toro-Frías, A., P. Martín-Lloret, J. Martin-Martinez, R. Castro-López, E. Roca, R. Rodriguez, M. Nafria and F. Fernández, "Reliability Simulation for Analog ICs: Goals, Solutions, and Challenges", *Integration, the VLSI Journal*, 2016.

128. Tyaginov, S., *Hot Carrier Degradation in Semiconductor Devices*, Springer, 2015.

129. Rzepa, G., W. Goes, B. Kaczer and T. Grasser, "Characterization and Modeling of Reliability Issues in Nanoscale Devices", *Proceedings of Circuits and Systems (ISCAS), IEEE International Symposium on*, pp. 2445–2448, 2015.

130. Bravaix, A., C. Guerin, V. Huard, D. Roy, J. Roux and E. Vincent, "Hot-Carrier Acceleration Factors for Low Power Management in DC-AC Stressed 40nm NMOS Node at High Temperature", *Proceedings of Reliability Physics, IEEE International Symposium on*, pp. 531–548, 2009.

131. Bernstein, J. B. *et al.*, "Electronic Circuit Reliability Modeling", *Microelectronics Reliability, Elsevier Journal of*, Vol. 46, No. 12, pp. 1957–1979, 2006.

132. Shiyanovskii, Y. *et al.*, "Process Reliability based Trojans Through NBTI and HCI Effects", *Proceedings of Adaptive Hardware and Systems (AHS), International NASA/ESA Conference on*, pp. 215–222, 2010.

133. More, S., M. Fulde, F. Chouard and D. Schmitt-Landsiedel, "Reducing Impact

of Degradation on Analog Circuits by Chopper Stabilization and Autozeroing", *Proceedings of Quality Electronic Design (ISQED), IEEE International Symposium on*, pp. 1–6, 2011.

134. Chouard, F. R., M. Fulde and D. Schmitt-Landsiedel, "Reliability assessment of voltage controlled oscillators in 32nm high-κ metal gate technology", *Proceedings of Electronic Solid State Circuits, IEEE International Conference on*, pp. 410–413, 2010.

135. Chouard, F. R., C. Werner, D. Schmitt-Landsiede and M. Fulde, "A Test Concept for Circuit Level Aging Demonstrated by A Differential Amplifier", *Proceedings of Reliability Physics, IEEE International Symposium on*, pp. 826–829, 2010.

136. Shen, C.-N. *et al.*, "The Study of Activation Energy (Ea) by Aging and High Temperature Storage for Quartz Resonator's Life Evaluation", *Proceedings of Piezoelectricity, Acoustic Waves, and Device Applications (SPAWDA), International Symposium on*, pp. 118–122, 2010.

137. Barragan, M. J. and G. Leger, "Efficient Selection of Signatures for Analog/RF Alternate Test", *Proceedings of Electronic Test Symposium (ETS), IEEE European Conference on*, pp. 1–6, 2013.

138. Székely, G. J. and M. L. Rizzo, "Brownian Distance Covariance", *The annals of Applied Statistics, Journal of Institute of Mathematical Statistics*, Vol. 3, No. 4, pp. 1236–1265, 2009.

139. Habal, H. and H. Graeb, "Evaluating Analog Circuit Performance in Light of MOSFET Aging at Different Time Scales", *Proceedings of IC Design & Technology (ICICDT), IEEE International Conference on*, pp. 41–44, 2013.

140. Chouard, F. R., S. More, M. Fulde and D. Schmitt-Landsiedel, "An Aging Suppression and Calibration Approach for Differential Amplifiers in Advanced CMOS Technologies", *Proceedings of Electronic Solid State Circuits, IEEE International*

Conference on, pp. 251–254, 2011.

141. Martin-Martinez, J., R. Rodríguez, M. Nafria and X. Aymerich, "Time-Dependent Variability Related to BTI Effects in MOSFETs: Impact on CMOS Differential Amplifiers", *Device and Materials Reliability, IEEE Transactions on*, Vol. 9, No. 2, pp. 305–310, 2009.

142. Agarwal, M., B. C. Paul, M. Zhang and S. Mitra, "Circuit Failure Prediction and Its Application to Transistor Aging", *Proceddings of VLSI Test, IEEE Symposium on*, pp. 277–286, 2007.

143. Bhushan, M., A. Gattiker, M. B. Ketchen and K. K. Das, "Ring Oscillators for CMOS Process Tuning and Variability Control", *Semiconductor Manufacturing, IEEE Transactions on*, Vol. 19, No. 1, pp. 10–18, 2006.

144. Yilmaz, C., L. Heiß, C. Werner and D. Schmitt-Landsiedel, "Modeling of NBTI-Recovery Effects in Analog CMOS Circuits", *Proceedings of Reliability Physics, IEEE International Symposium on*, pp. 2A–4, 2013.

145. Pelgrom, M. J., A. C. Duinmaijer and A. P. Welbers, "Matching Properties of MOS Transistors", *Solid-State Circuits, IEEE Journal of*, Vol. 24, No. 5, pp. 1433–1439, 1989.

146. Kinget, P. R., "Device Mismatch and Tradeoffs in the Design of Analog Circuits", *Solid-State Circuits, IEEE Journal of*, Vol. 40, No. 6, pp. 1212–1224, 2005.

147. Wu, X., Z. Chen and P. Madhani, "Physics and Modeling of Transistor Matching Degradation Under Matched External Stress", *Proceedings of Microelectronic Test Structures, IEEE International Conference on*, pp. 233–237, 2008.

APPENDIX A: TEST CHIPS

Two different test chips were designed for the silicon validation of proposed methodologies. The aim of the first test chip is to develop semi-empirical models for both process variations and aging phenomena. The second chip includes a number of different circuits, which were generated by using the developed variation-aware circuit synthesis. In this chapter, design process of test chips are explained in detail.

A.1. Test Chip Design for Aging and Variation Model Development

The aim of this chip is to obtain the process variation and aging effects on analog circuits for the 130nm UMC technology and fit the semi-empirical models provided in the literature [133–135, 139–141].

To observe degradation/variation effects on circuits, different circuit architectures such as ring oscillators for digital circuits and comparators for their analog counterparts have been used in the literature. The main idea behind using these circuits is to map the changes at the output to the degraded device parameters as a result of either aging or process variations.

To map the degradation effects, a perfect decomposition of the contributing parts of the circuit is required for an accurate model fitting. The case for digital circuits is quite simple and conventionally ring oscillators are commonly used as test circuits to obtain the degradation/variation effects. Using the simple inverter delay model expression, the change in the oscillation frequency can easily be mapped to the device parameter variations [142,143]. On the other hand, considering analog circuits, partitioning process is highly difficult and several simulations should be performed for several operating point scenarios. This procedure is called "Sensitivity Analysis" and it can only be applied for linear circuits. There are several studies that use sensitivity analysis to determine the dominant source of degradation in complicated analog circuits [133, 134, 140]. Another problem arises during the accelerated aging

tests. Gate voltages in most analog circuits can be neglected compared to the supply voltages, therefore there would not be any considerable change at the output due to aging. In general, operational amplifiers in open loop configuration are used for such a test, where voltages are closer to the supply voltages at gate terminals [140, 144]. For example, in [133], a two stage operational transconductance amplifier was utilized to capture the changes in device parameters. An asymmetrical stress was applied to the input differential pair to create a divergence between the device parameters. Then, the OTA circuit was aged utilizing an accelerated aging set-up and the output off-set voltage were measured. At last, the offset voltage degradation is mapped to the V_{th}/I_d degradation, where I_d degradation is modelled for HCI as;

$$\Delta I_d = I_d.A.{V_{ds}}^{p_1}.e^{\frac{\Delta E}{kT}}.L^{p_2}.t^{p_3} \tag{A.1}$$

where t and L denote time and transistor length, respectively. A, p_1, p_2, and p_3 are fitting parameters. On the other hand, V_{th} degradation in BTI is modeled as;

$$\Delta V_{th} = B.\left(V_{gs}\right)^{m_1}.e^{\frac{\Delta E}{kT}}.L^{m_2}.W^{m_3}.t^{m_4} \tag{A.2}$$

where t, L, and W are time, transistor length, and transistor width, respectively. Similarly, B, m_1, m_2, m_3, and m_4 are technology dependent fitting parameters.

These models are called as "Semi-Empirical Models" in the literature and can be adopted to each technology node by fitting the model parameters according to the single device stress measurements [133]. The stress measurement depends on the well-known Arrhenius law behavior, where the temperature is used to accelerate the aging effect along with a certain amount of applied electrical stress on devices.

In addition to the aging effects, the process variation effects can also be observed by monitoring the changes at the output. Mapping of these changes into the saturation current can be handled by using well defined models in the literature [145–147].

$$\sigma^2_{V_{th}} = \frac{A^2_{\sigma_{V_{th}}}}{2.W.L.M.F} \tag{A.3}$$

Even if sensitivity analysis gives the information about the dominant sources of degradation that cause changes in the output, other transistor parameters may also have contributions to related output specifications. For example, considering OTA configuration, the offset voltage highly depends on the difference between differential pair transistors at the input side. However, this divergence is multiplied by the open-loop gain of the OTA creates an offset voltage at the output. In this case, degradation of open-loop gain, which is affected by degradation of many other transistor, should not be ignored to avoid any estimation error leading inaccurate modeling. Therefore, the most reliable way of evaluating the effects of aging and process variations on circuits is using P and N type test transistor arrays with different properties in the chip and measuring the saturation current changes. Thus, independent evaluation of each transistor provides more accurate information about variation/aging on the corresponding device, resulting in better models.

A further problem arises due to the limited number of pins on the chip that inhibits the number of device under test (DUT). Therefore, a pin multiplexing mechanism is required to take the opportunity of testing maximum number of devices. Considering all of these, a block diagram of the test chip is given in Figure A.1. The test block consists of three different parts: *Control Block*, *Selection Block*, and *Test Devices Block*. Two operation modes were planned for test devices: Stress and Measurement modes, which are controlled by an input in the *Selection Block*. In the stress mode, all test devices become active; hence, all of them are exposed to electrical stress simultaneously. However, in the recovery mode, only one device is activated and remaining devices are de-activated by control signals generated by the *Control Block*.

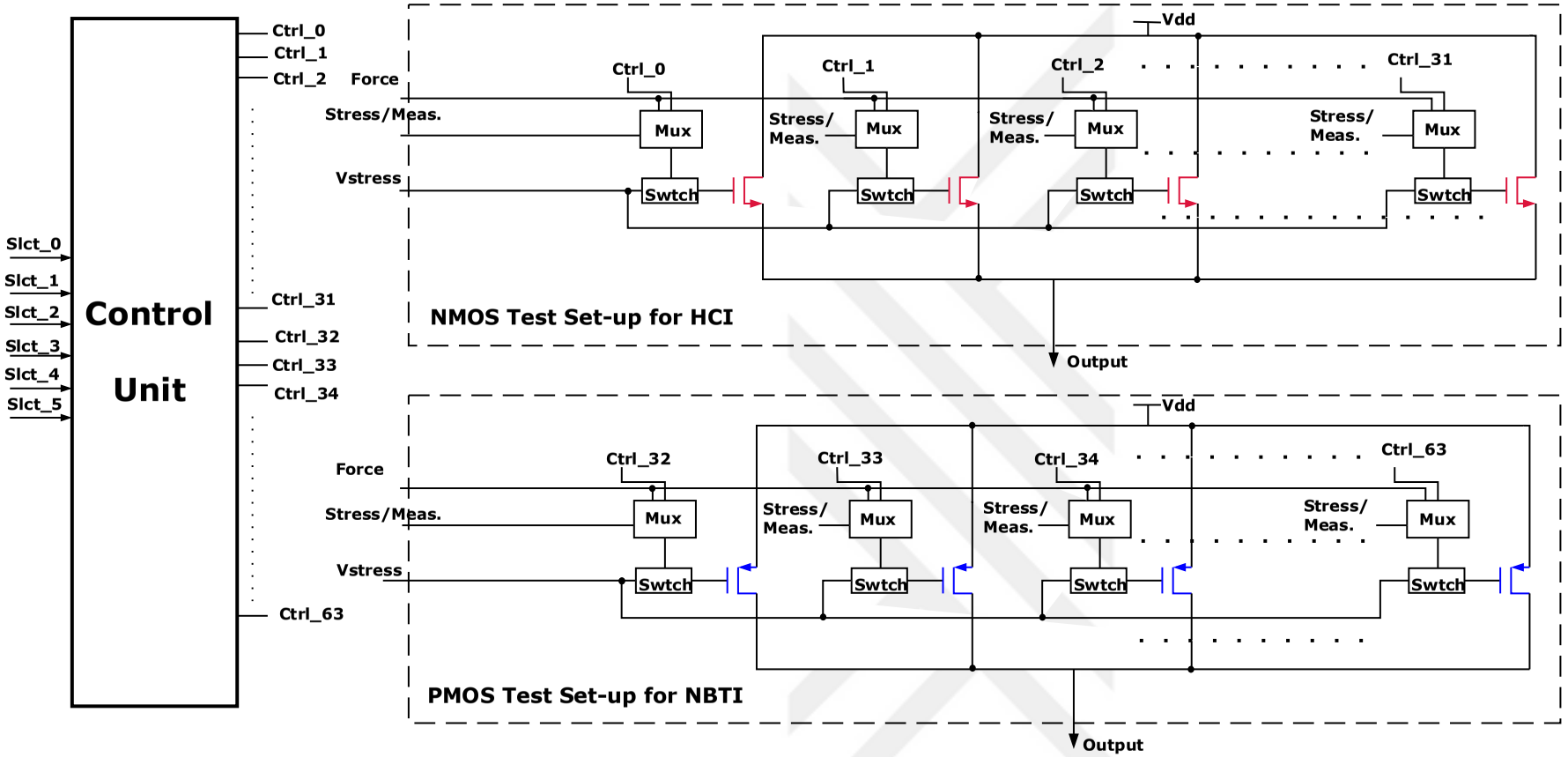

Figure A.1. A block diagram of the test chip.

A.1.1. Control Unit

In the *Control Module*, a 6x64 bit line decoder was utilized to produce independent enable signals to manage measurement operation. Thus, just one device can be activated at the measurement mode and this mechanism reduces the required number of pins to test all devices. The logic diagram and layout of the control block is provided in Figure A.2.

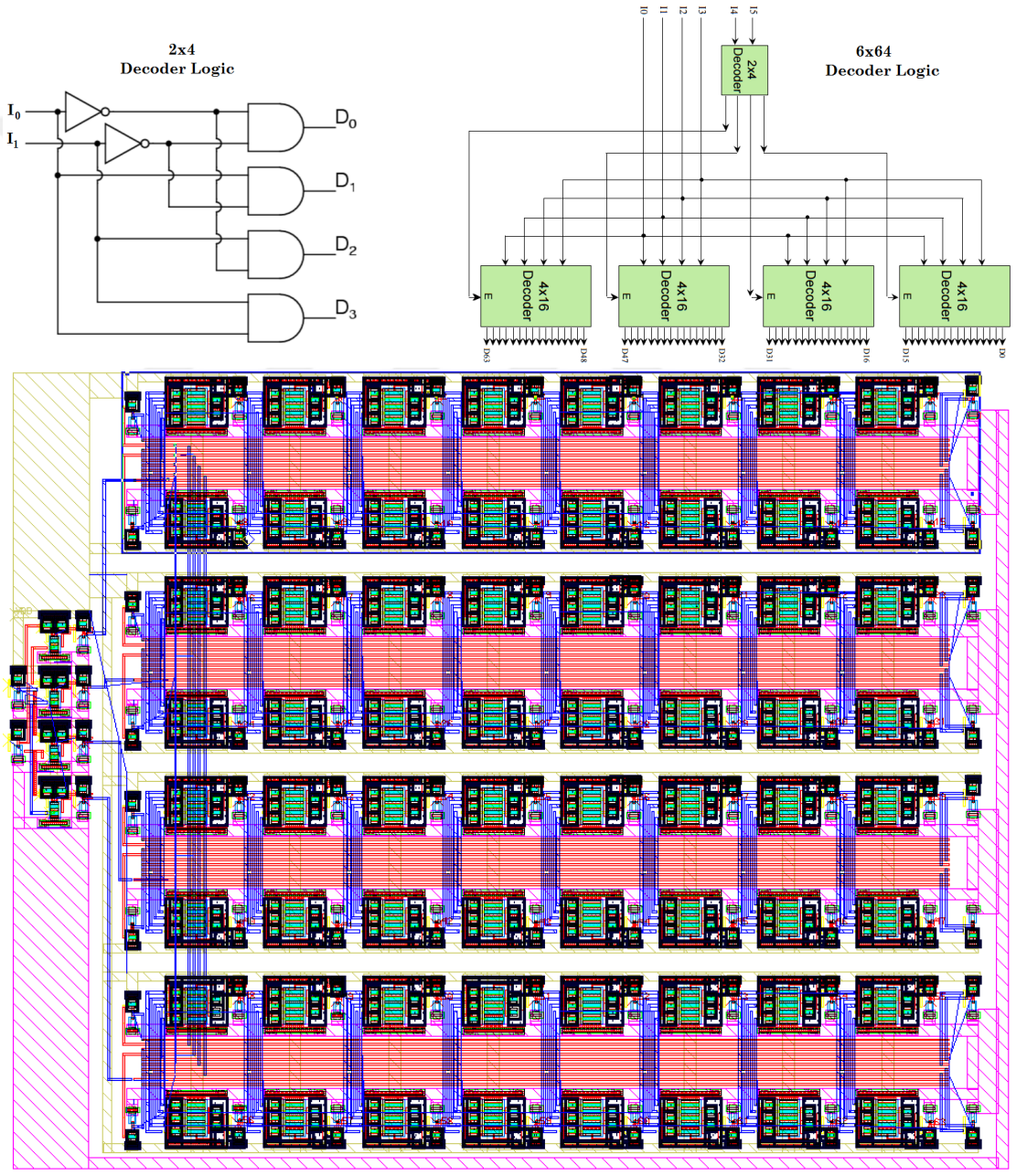

Figure A.2. Control module (6x64 line decoder) and the layout.

A.1.2. Selection Block

In the selection part, a multiplexer set whose logic diagram and layout given in Figure A.3 was designed to control design under test devices (DUTs.) When the multiplexer selection input is low, *Force* (Logic '1') inputs are selected and transmitted to the switch cells. When the multiplexer selection is high, control signals coming from

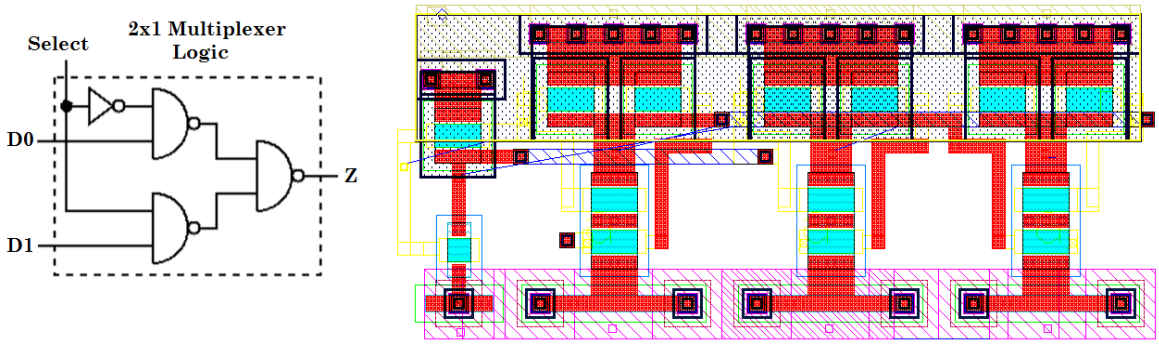

Figure A.3. Multiplexer layout (selection block).

the control block are sent to the switch. Thus, in stress mode, all devices become active. On the other hand, in the measurement mode, only the selected (via control block) device is activated, so all other devices are isolated during the measurement mode. To eliminate any leakage current induced measurement errors, the leakage current of each block can be measured when all switches are deactivated and the measurement is thus calibrated by subtracting this leakage current from each measured data.

A.1.3. Test Devices Block

Stress voltages are the inputs of switch cells, shown in Figure A.4, and applied to DUT's gate terminals depending on the enable signals that is sent from the multiplexer unit. Two different test blocks were implemented: P-type for NBTI and N-type for HCI. The source and drain terminals of these test transistors are connected to each other in each test block to reduce the necessary output pin. There are 32 devices in each test block with different dimensions to capture the effect of transistor dimensions on aging and mismatch phenomena.

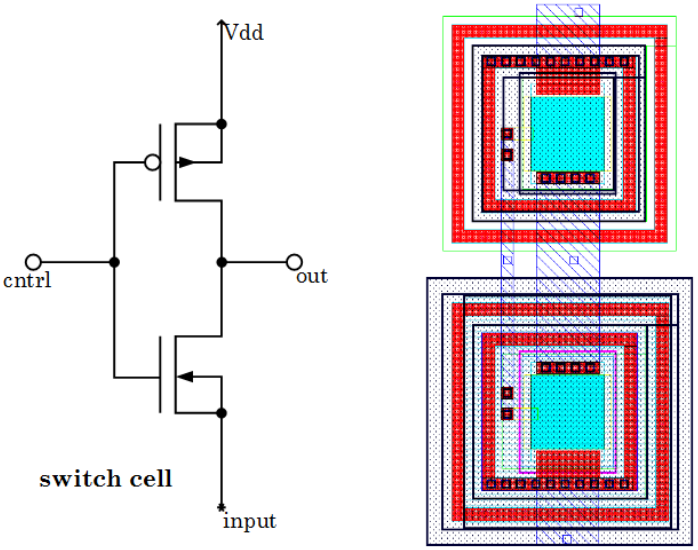

Figure A.4. Switch circuit that is used to enable/disable DUT devices.

A.1.4. Other Blocks

There should be some additional circuits to keep the chip in safe against voltage fluctuations at the power supply and electrostatic discharge induced burn out. A clamping circuit proposed in [125] was utilized to clamp the supply voltage at a certain level. The schematic and the layout of clamping circuit are given in Figure A.5.

Another problem arises when a pin is directly connected to the gate terminal of a device. In such case, electrostatic discharge lead to burn out of the device due to instantaneous high voltage occurring during the discharge. To avoid this problem, conventionally electrostatic discharge diodes are utilized. The schematic and the layout of the ESD diode is given in Figure A.6. The chip layout including pads, electrostatic protection diodes, and clamping circuits is given in Figure A.7 .

A.2. Test Chip Design for Aging and Variation Model Development

A scrambled-QMC-based yield-aware analog circuit optimization tool is introduced and explained in Section 4.6. According to the simulation results, the devel-

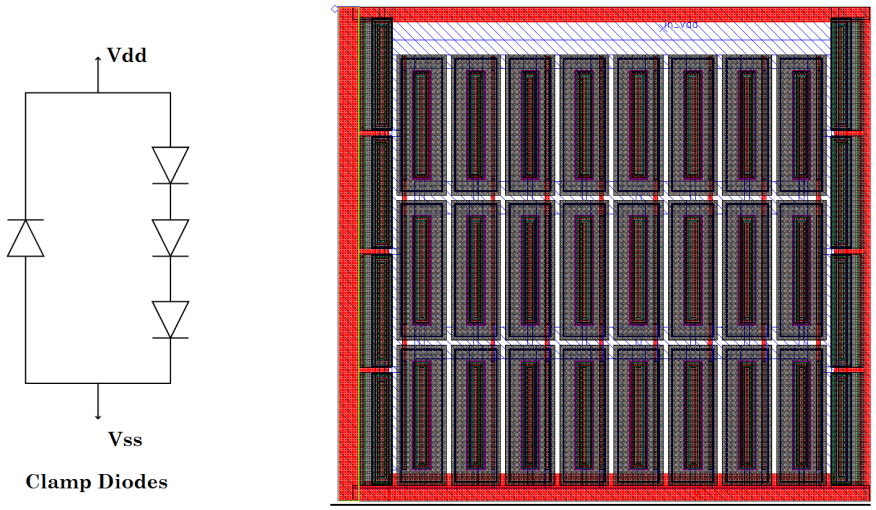

Figure A.5. Clamping circuit protects chip from power supply fluctuations.

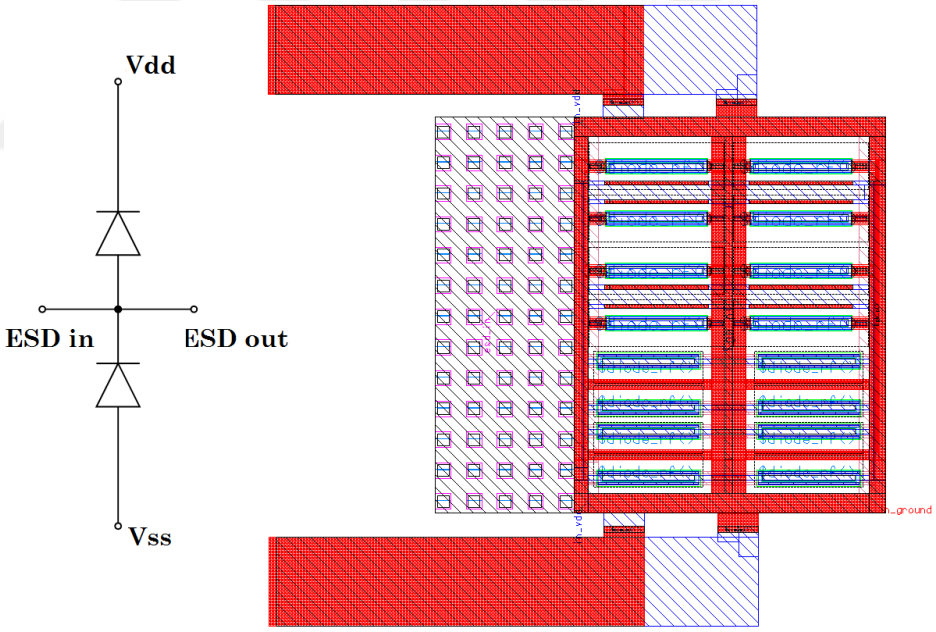

Figure A.6. ESD diode protects chip from electrostatic discharge.

oped tool guarantees a certain yield for a given analog circuit by using the over-design approach, where the optimizer tries to find a solution that overly satisfies the design constraints. Thus; a high yield can be achieved even if process variations take place. To verify the developed tool with the silicon data, a second test chip was designed and

taped-out using 130nm technology. Three different analog circuits; folded cascode OTA, two Stage OTA, and a latch comparator were included in the test chip.

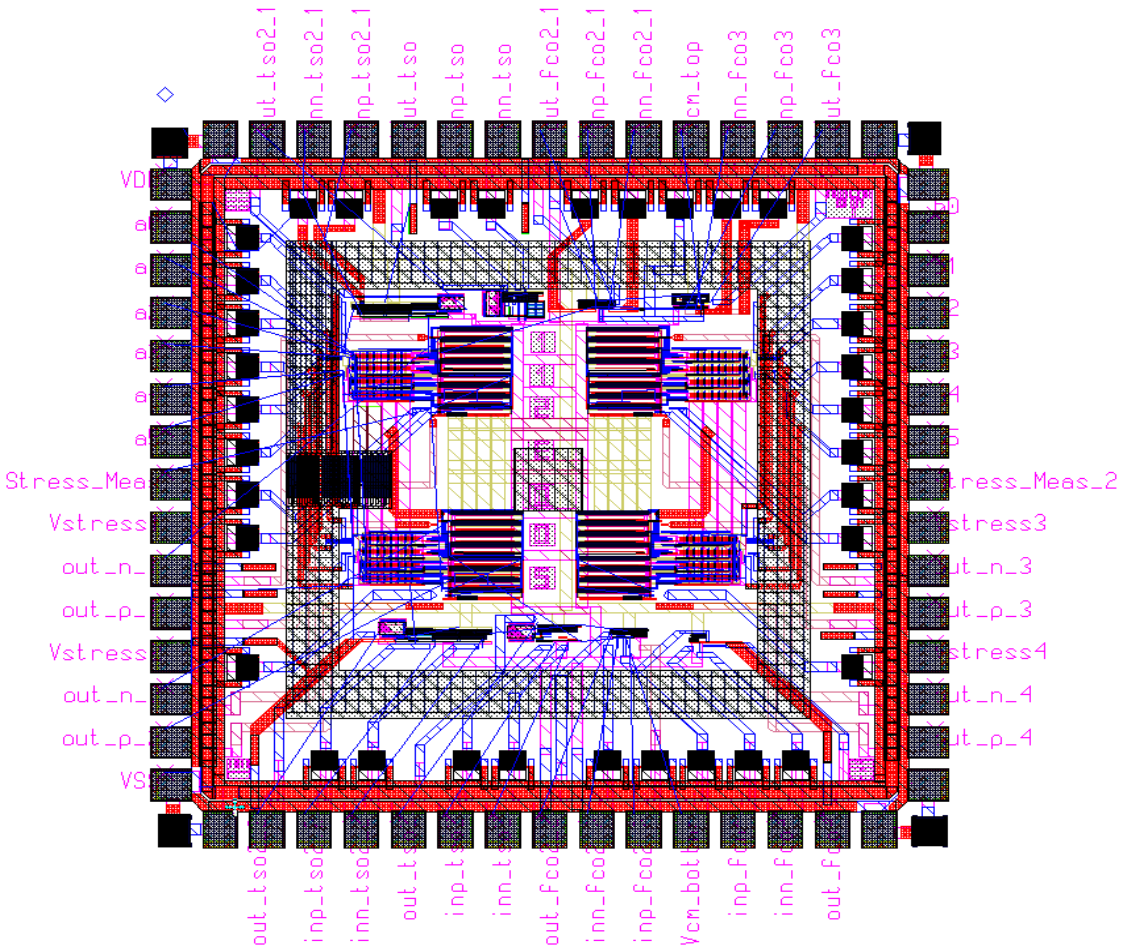

Figure A.7. The entire chip layout.

Typically, yield-aware optimization tool uses 200-300 points to sample the uncertain design space. Therefore, the number of test circuits was kept at 16 for each circuit topology, where 20 packaged dice have been received, thus, 320 samples can be measured for each test circuit, which is sufficient to make a fair comparison with the estimation results. The test chip consists of 5 major blocks: two stage and folded cascode OTA blocks, comparator block, control block, and RF circuitry block. Schematics of test circuits are given in Figure A.8, Figure A.9, Figure A.10, and Figure A.11.

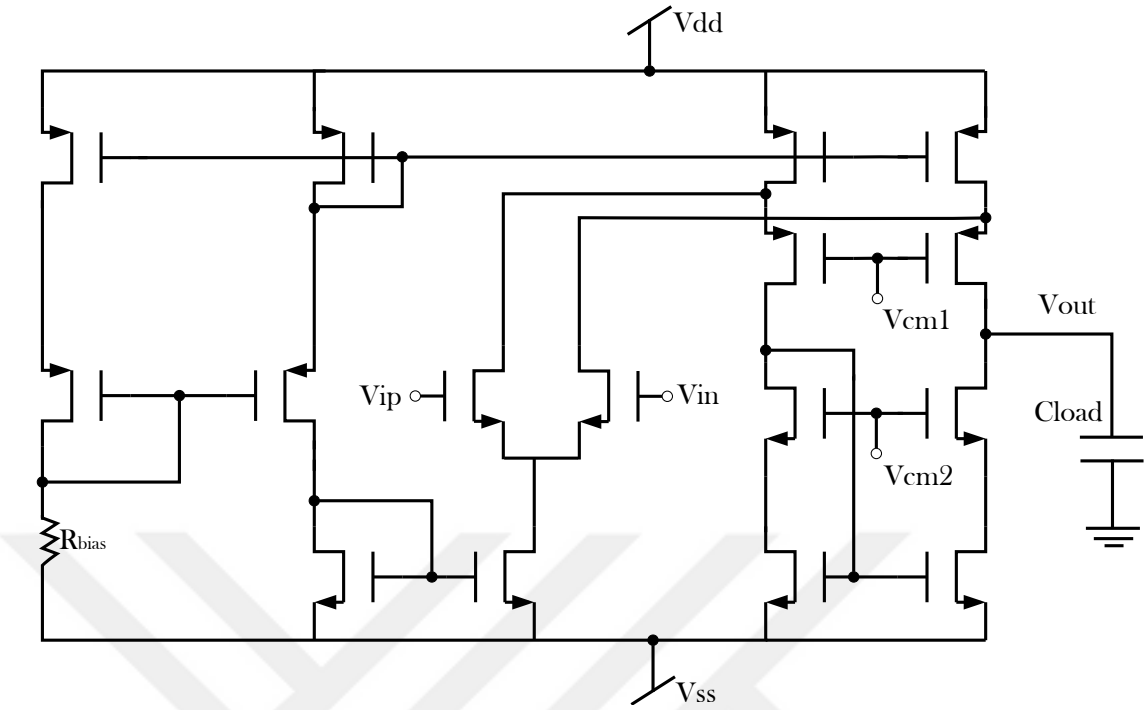

Figure A.8. Two stage OTA circuit schematic.

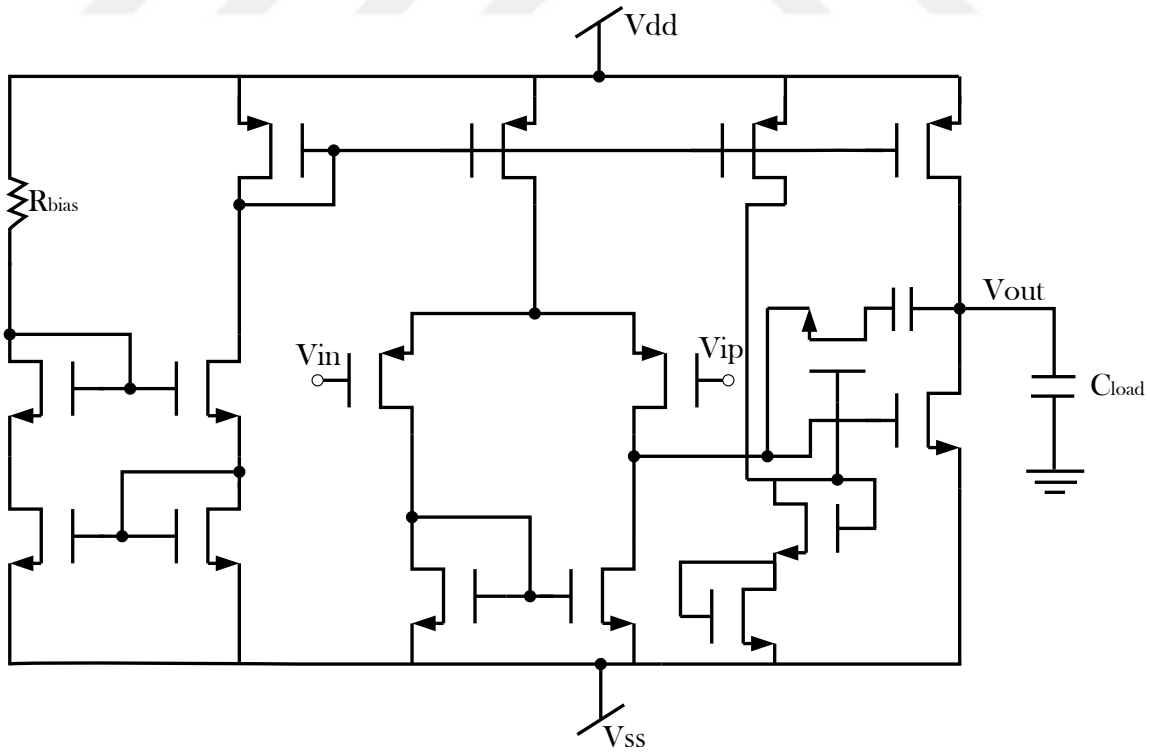

Figure A.9. Folded cascode and OTA circuit schematics.

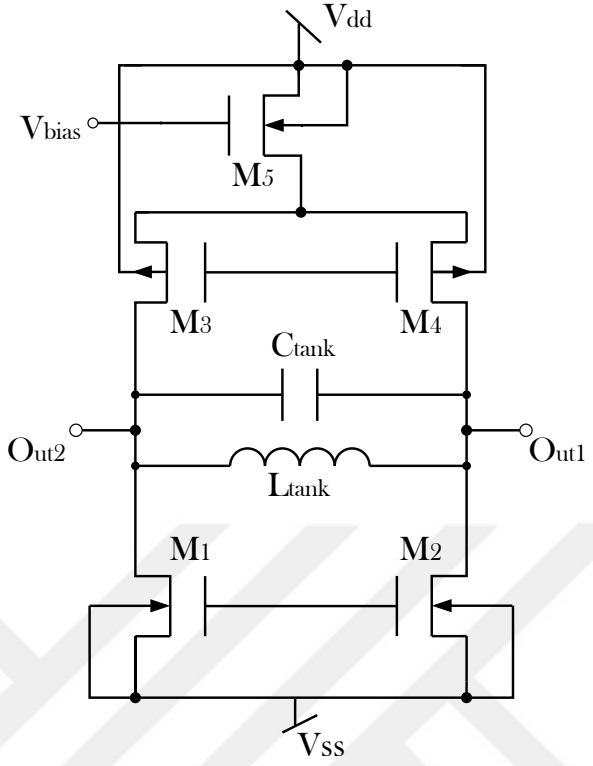

Figure A.10. LC oscillator circuit schematic.

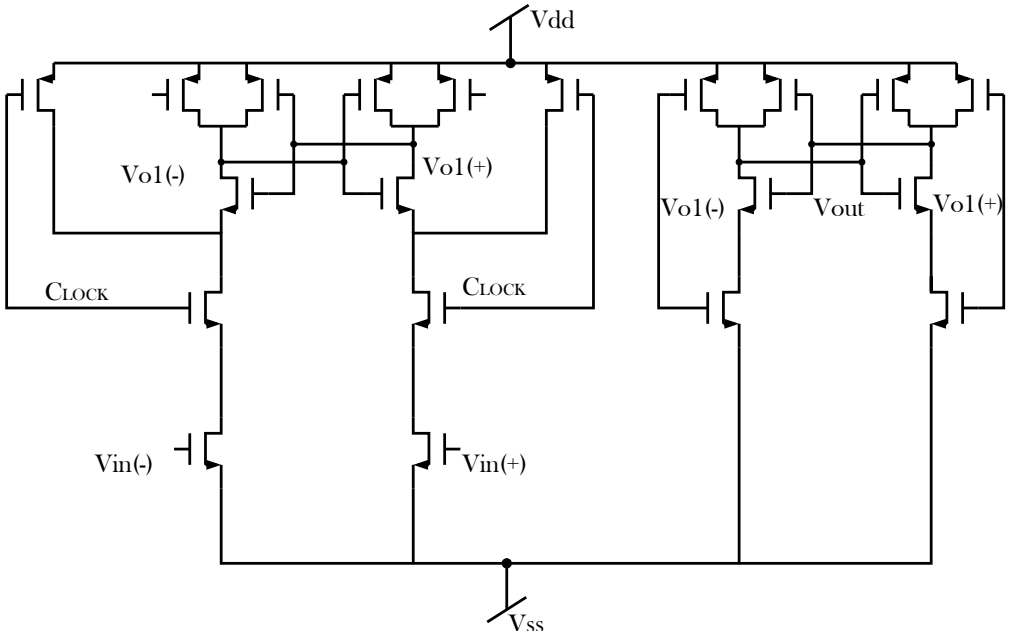

Figure A.11. Comparator circuit schematic.

RF circuit block was designed to utilize the free space in the chip. In this block, there are 3 ring oscillators with different oscillation frequencies and one p-type biased CMOS cross-coupled LC oscillator. To avoid interference during measurements, individual supply ports were allocated for the RF circuits. There are 16 test circuits in each analog block, where circuit outputs are connected to each other in each individual block via switches to multiplex the limited number of pins. These switches are controlled by a control block, where a 4x16 line decoder is assigned to generate individual enable signals for activation of the circuit to be measured. The schematic of the complete chip is illustrated in Figure A.12. There are 60 input/output ports, where 12 ports were assigned for the two stage block, 14 ports were assigned for the folded cascode block, and 13 ports were assigned for the comparator block. To provide perfect isolation, RF blocks have their own power supply ports ($V_{dd-ringo}$ and V_{dd-LC}). Furthermore, there are two other power supply ports allocated for the analog blocks ($V_{dd-right}$ and $V_{dd-left}$).

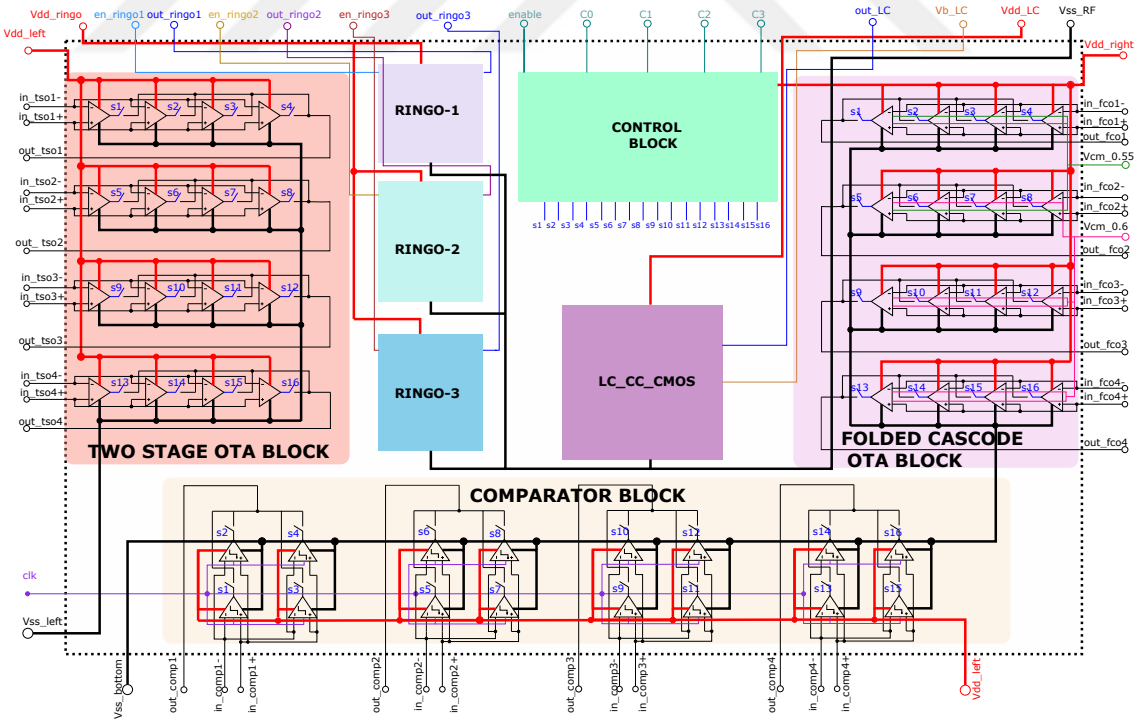

Figure A.12. Schematic of the second test chip.

In the RF block, 3 ring oscillators (45, 59, and 75 stages) with different oscillation frequencies ($598MHz$, $466MHz$, and $363MHz$) were designed. Moreover, an LC oscillator with $2.5GHz$ was also designed and resided to the chip. The major aim of this RF block is to observe the aging effects on RF circuits through the accelerated aging tests (AAT). Layouts of two stage OTA circuits are given in Figure A.13, where corresponding post-layout simulation results are also given in Table A.1.

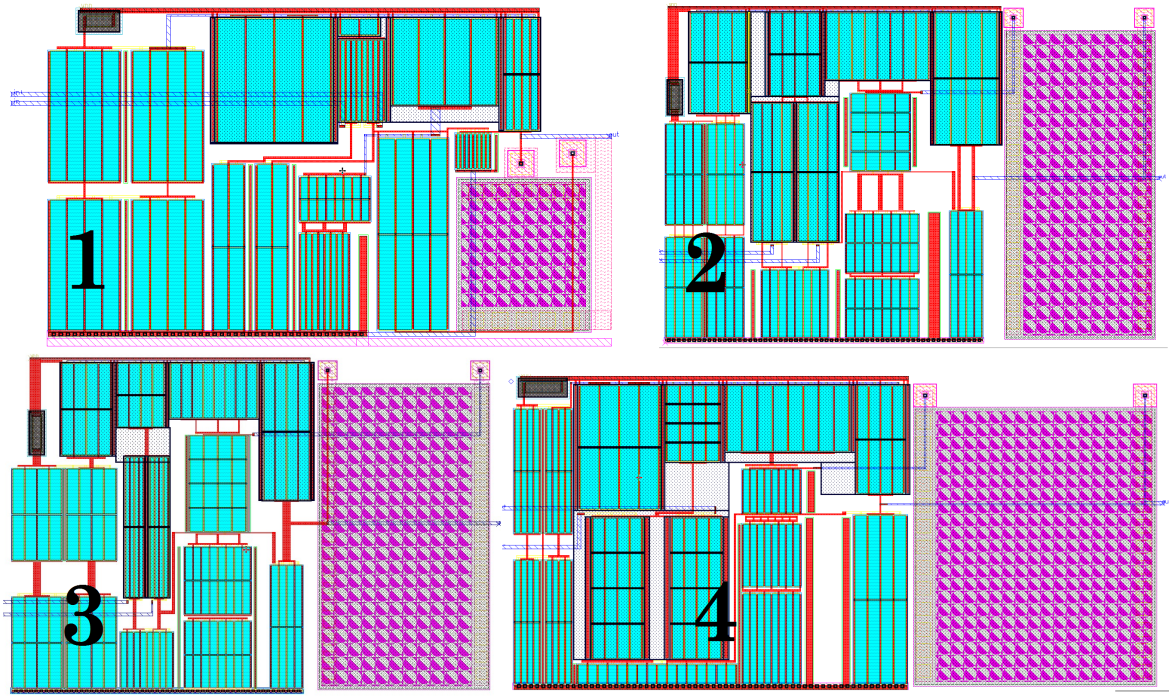

Figure A.13. Two stage OTA layouts.

Table A.1. Post-layout simulation results of two stage OTA circuits.

	3dB BW (kHz)	Gain (dB)	Phase Margin (^{o})	Offset (mV)	Power (mW)
1	9.24	70.83	82	1.53	1.80
2	9.4	71.65	81	0.48	1.32
3	8.92	70.1	58	0.89	1.44
4	9.2	72.1	66	0.56	1.2

Layouts of folded cascode OTA topology are given in Figure A.14. Post-layout simulation results of folded cascode circuits are provided in Table A.2.

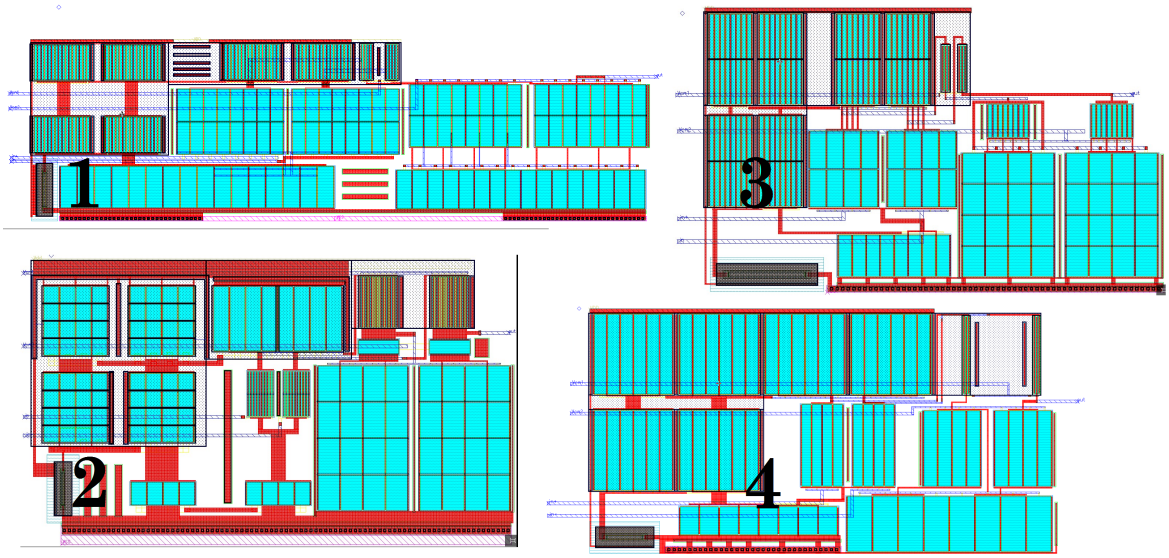

Figure A.14. Folded cascode OTA layouts.

Table A.2. Post-layout simulation results of folded cascode OTA circuits.

	3dB BW (kHz)	Gain (dB)	Phase Margin (^{o})	Offset (mV)	Power (mW)
1	10.39	70.07	69	0.37	0.71
2	14.69	71.58	74	0.02	0.152
3	10.14	71.27	71	0.31	0.201
4	15.21	70.21	67	0.26	0.119

Post-layout simulation results and layouts of comparator circuits are given in Table A.3 and Figure A.15. Gonenc Berkol, MSc., performed all the designs in this part including comparator synthesis, simulation, and layout.

Table A.3. Post-layout simulation results of comparator circuits.

	Offset Voltage (V)	Sensitivity (mV)	Clock Freq. (Hz)	Power (mW)
1	0.7	3.1	250	0.8
2	0.7	2.1	250	1.5
3	0.7	3.6	250	0.25
4	0.7	2.8	250	0.7

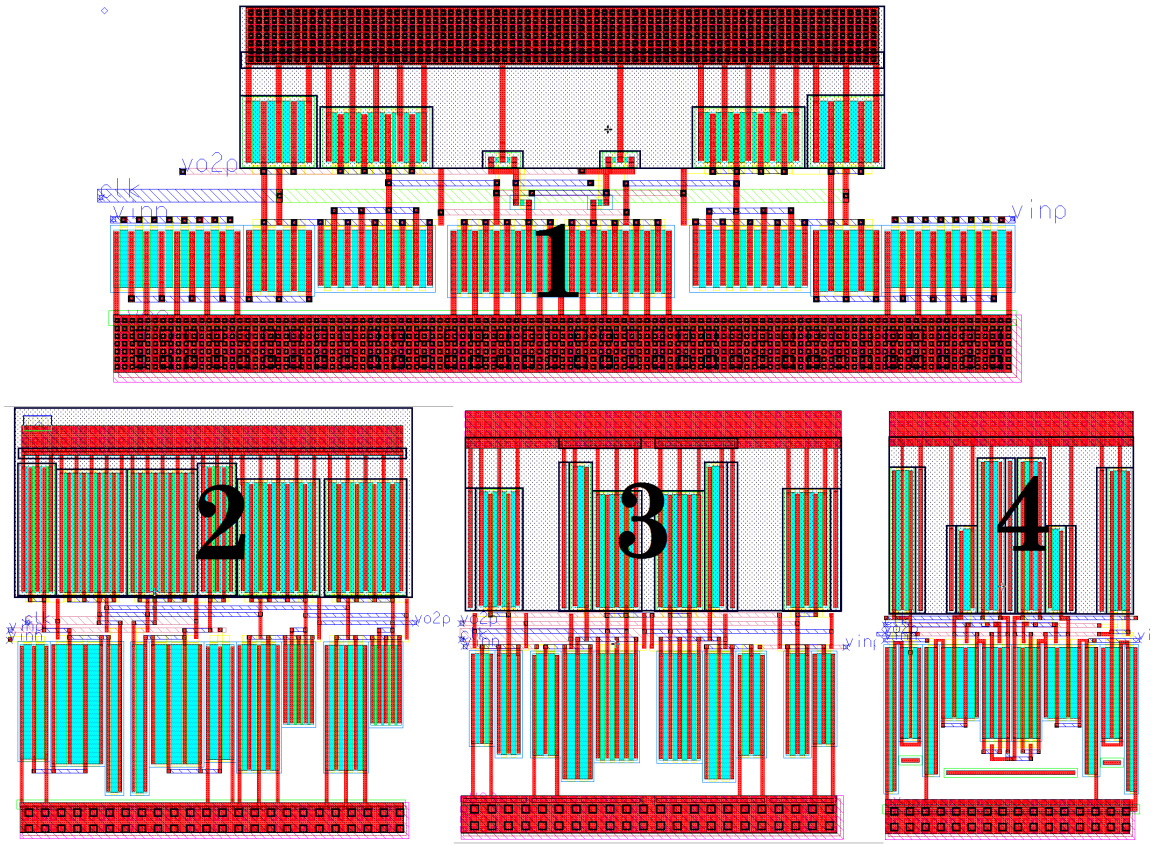

Figure A.15. Comparator layouts.

Ring oscillator and CMOS cross-coupled LC oscillator layouts are given in Figure A.16. It is opposed to the other analog circuits, RF transistors were used for all RF circuits. Ring oscillators have a nand-based first stage for starting-up the oscillation. In addition to these RF circuits, a buffer was designed to drive a 50 ohm

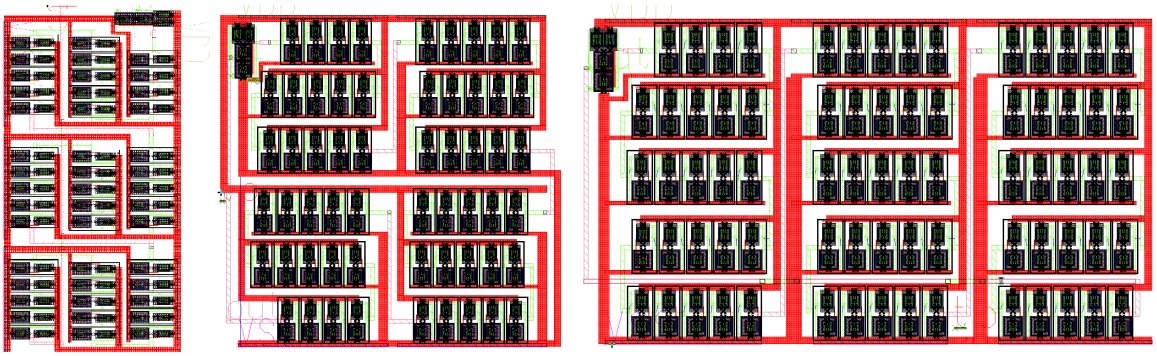

Figure A.16. Ring oscillator layouts.

load resistance. An optimally sized conventional inverter chain structure was used for the buffer. Furthermore, a back-end circuitry for CMOS LC cross-coupled oscillator was designed to probe the outputs from a single port, which then drives the buffer. The back-end circuit is a simple active loaded amplifier, which were designed so as to operate at $2.5GHz$. Layouts of the buffer stage and the back-end circuit are given in Figure A.17.

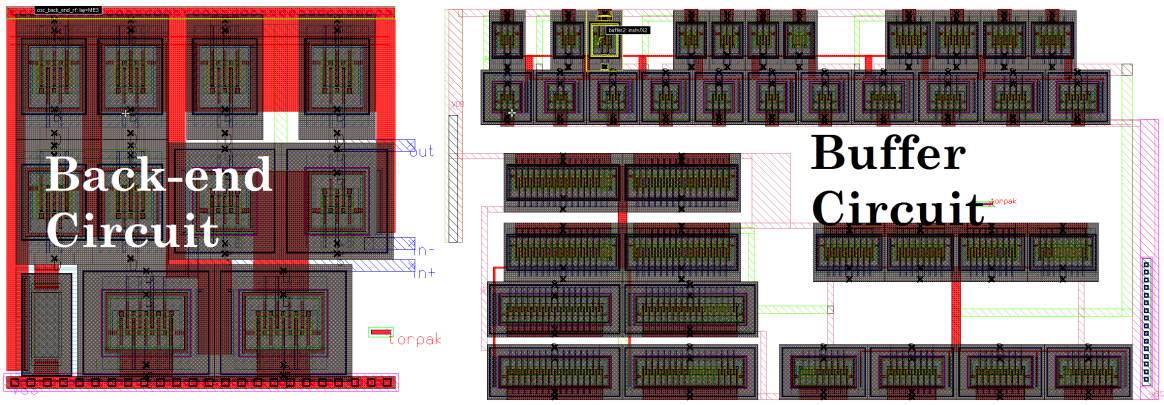

Figure A.17. Back-end and buffer layouts.

To control these analog blocks and multiplex the chip ports, a digital control block was designed. The control block includes a 4x16 line decoder, whose layout is given in Figure A.18. The complete layout of the test chip is given in Figure A.19.

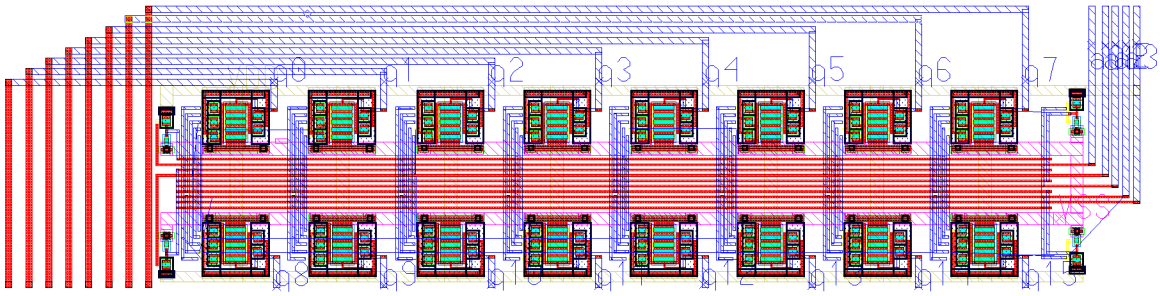

Figure A.18. Control block layout.

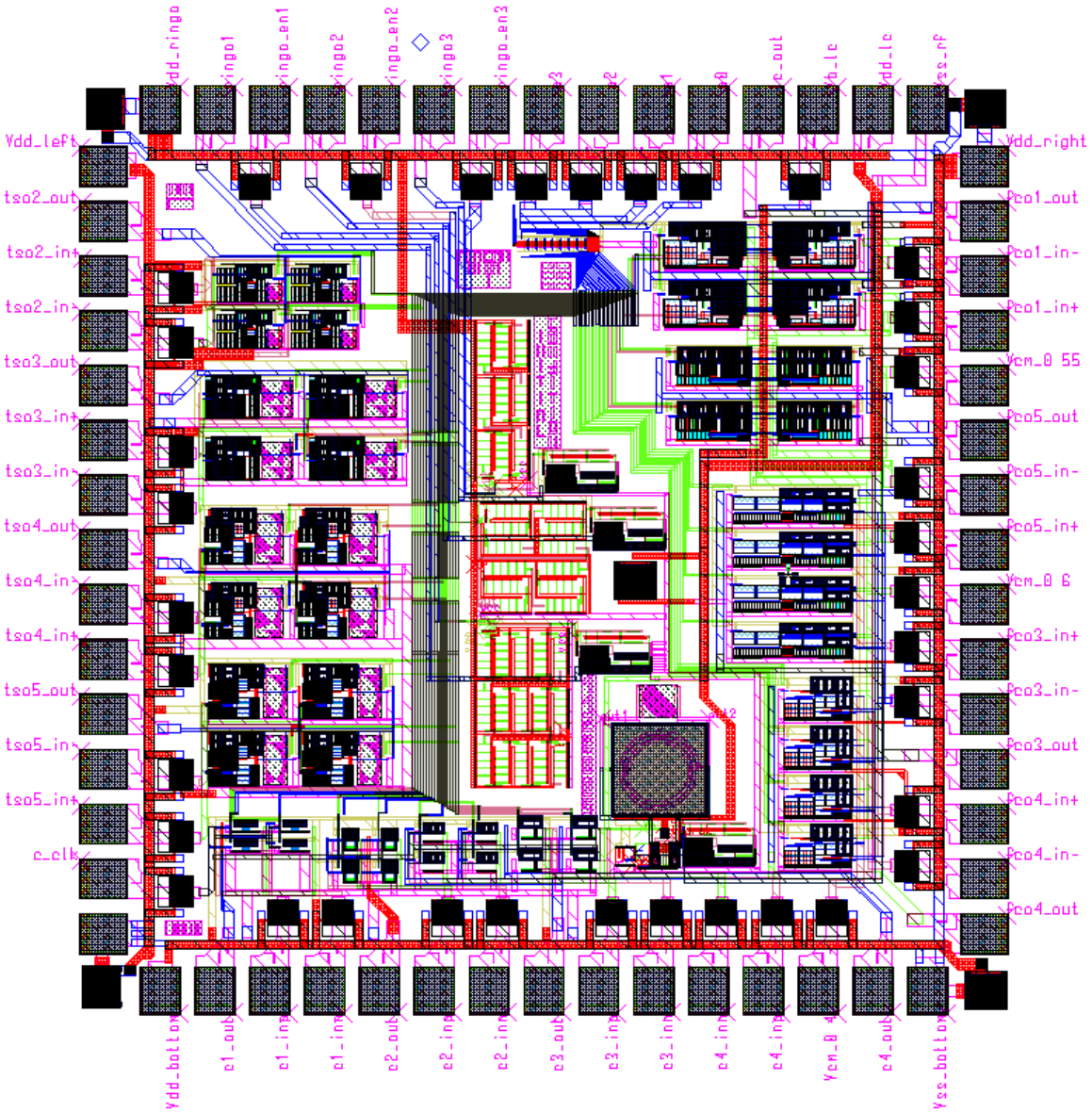

Figure A.19. The complete layout of the chip.