THE DESIGN OF AN OPTICALLY POWERED LOW VOLTAGE CMOS RECEIVER FOR MAGNETIC RESONANCE IMAGING

by

Ahmed Aksu

B.S., Electrical and Electronics Engineering, Marmara University, 2020

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Master of Science

Graduate Program in Electrical and Electronics Engineering

Boğaziçi University

2024

ACKNOWLEDGEMENTS

I would like to express my gratitude to my thesis advisor, Prof. Günhan Dündar, and co-advisor, Prof. Arda Deniz Yalçınkaya, for their invaluable guidance and extensive knowledge. Their remarkable foresight and insightful advice helped me overcome any challenges that arose during this research.

I would like to thank all the members of BETA Lab, including Uygar Yıldız, Atakan Türker, Dr. Kemal Ozanoğlu, Utku Arda Akıncı, Mehmet Gök, Macit Uluda, and many others, for their endless support and for helping me to manage my annoying anxiety. I would also like to thank Ümit Develer and İbrahim Kahraman for their support and encouragement throughout this journey.

ABSTRACT

THE DESIGN OF AN OPTICALLY POWERED LOW VOLTAGE CMOS RECEIVER FOR MAGNETIC RESONANCE IMAGING

This study proposes the design and layout of a fully differential, low-voltage CMOS low noise amplifier (LNA) and a mixer as a receiver for the radio frequency (RF) coils of magnetic resonance imaging (MRI) devices. The ultimate goal of the low-voltage design is to use an on-chip photodiode array as the power supply, which is expected to produce at least 0.9V supply voltage. The primary focus of the study is to achieve a sub-1 dB noise figure while maintaining sufficient gain and linearity, which are critical specifications due to the wide dynamic range of the MRI coils. The design constraints are interdependent, with gain, voltage swing, linearity, noise figure, and dynamic range being all related to each other. Consequently, achieving an optimal balance among these factors is a challenging but necessary task to ensure the system's effectiveness. The MRI coil is modeled as a voltage source with 50Ω impedance. The LNA is noise-matched with the coil. The post-layout simulation of the LNA achieved a 26 dB voltage gain and a 0.71 dB noise figure. The downconversion mixer is designed in a folded structure to efficiently utilize the supply voltage. The mixer demonstrated a conversion gain of 10.6 dB, a third-order input intercept point (IIP3) of around 1.8 dBm, and an input-referred 1 dB compression point at approximately -13.4 dBm. The designs were implemented using 65nm technology. The overall system consumes 2.7 mW and achieves a noise figure of less than 1 dB, a voltage gain of 36 dB, an input-referred 1 dB compression point of -45 dBm, and a third-order input intercept point of -30 dBm.

ÖZET

MANYETİK REZONANS GÖRÜNTÜLEME İÇİN OPTİK GÜÇLE ÇALIŞAN DÜŞÜK VOLTAJLI CMOS ALICI TASARIMI

Bu çalışma, manyetik rezonans görüntüleme (MRG) cihazlarının radyo frekansı (RF) bobinleri için alıcı devresi olarak tamamen diferansiyel, düşük voltajlı CMOS düşük gürültülü yükselteç (LNA) ve mikser tümdevre tasarımlarını ve serimlerini önermektedir. Güç kaynağı olarak en az 0,9V besleme gerilimi üretmesi beklenen yonga içi fotodiyot dizisi kullanımı hedeflendiği için devre düşük voltajlı olarak tasarlanmıştır. Tasarımın ana odak noktası, MRG bobinlerinin geniş dinamik aralığı nedeniyle kritik olan yeterli kazanç ve doğrusallığı korurken 1 dB'nin altında bir gürültü sayısı elde etmektir. Tasarım kısıtlamaları birbiriyle bağımlıdır; kazanç, voltaj salınımı, doğrusallık, gürültü faktörü ve dinamik aralık birbirleriyle ilişkilidir. Dolayısıyla, bu faktörler arasında optimal bir denge sağlamak, sistemin etkinliğini garanti etmek için zorlu ama gerekli bir görevdir. LNA, 50Ω empedansa sahip bir voltaj kaynağı olarak modellenen MRG bobini ile gürültü eşleşmesi yapmaktadır. LNA'nın serim sonrası simülasyonunda, 26 dB voltaj kazancı ve 0,71 dB gürültü sayısı elde edilmiştir. Mikser, besleme gerilimini verimli bir şekilde kullanmak için katlanmış bir yapıda tasarlanmıştır. Serim sonrası simülasyonlardan 10,6 dB dönüşüm kazancı, yaklaşık 1,8 dBm üçüncü dereceden giriş kesişim noktası (IIP3) ve yaklaşık -13,4 dBm'de girişe referanslı 1 dB sıkıştırma noktası sonuçları elde edilmiştir. Tasarım 65nm teknolojisi kullanılarak gerçekleştirilmiştir. Tüm sistem 2,7 mW güç tüketmektedir. Serim sonrası simülasyonlardan 1 dB'nin altında bir gürültü sayısı, 36 dB voltaj kazancı, -45 dBm girişe referanslı 1 dB sıkıştırma noktası ve -30 dBm üçüncü dereceden giriş kesişim noktası sonuçları elde edilmiştir.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS . . . iii
ABSTRACT . . . iv
ÖZET . . . v
LIST OF FIGURES . . . vii
LIST OF TABLES . . . xi
LIST OF SYMBOLS . . . xii
LIST OF ACRONYMS/ABBREVIATIONS . . . xiv
1. INTRODUCTION . . . 1
2. SYSTEM DESCRIPTION . . . 4
2.1. Receiver Architecture . . . 4
2.2. CMOS Technology . . . 6
3. NOISE . . . 12
3.1. Thermal Noise Model of Resistors . . . 12
3.2. Thermal Noise Model of MOSFETs . . . 13
3.3. Noise Analysis of Miller Resistance . . . 14
3.4. Impedance and Noise Matching . . . 15
4. FULLY DIFFERENTIAL LOW VOLTAGE LOW NOISE AMPLIFIER . . . 17
4.1. The First Approach: Two Stage LNA . . . 17
4.2. The Second Approach: Single Stage LNA . . . 20
5. LOW VOLTAGE MIXER CIRCUIT . . . 28
5.1. Gilbert Mixer Cell . . . 28
5.2. Folded Mixer . . . 30
6. SIMULATION RESULTS OF ENTIRE SYSTEM . . . 34
7. CONCLUSION . . . 36
REFERENCES . . . 37
APPENDIX A: COILCRAFT AIR CORE INDUCTOR DATASHEET . . . 42
APPENDIX B: ABOUT THE REFERENCES AND FIGURES . . . 45

LIST OF FIGURES

Figure 1.1. MRI scanner components [1]. 2

Figure 2.1. Block diagram of the overall system. 5

Figure 2.2. I_D-V_{DS} characteristics of a low threshold N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$. 6

Figure 2.3. I_D-V_{GS} characteristics of a low threshold N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$. 7

Figure 2.4. I_D-V_{DS} characteristics of a native N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 200nm$, (b) $L = 500nm$, (c) $L = 1\mu m$. 7

Figure 2.5. I_D-V_{GS} characteristics of a native N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 200nm$, (b) $L = 500nm$, (c) $L = 1\mu m$. 8

Figure 2.6. I_D-V_{DS} characteristics of a low threshold P-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$. 8

Figure 2.7. I_D-V_{GS} characteristics of a low threshold P-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$. 9

Figure 2.8. Layout of the native NMOS. 10

Figure 2.9. Layout of the PMOS. 10

Figure 2.10. Layout of a highly resistive polysilicon resistor. 11

Figure 3.1. Norton model of resistor noise. 12

Figure 3.2. Thevenin model of resistor noise. 13

Figure 3.3. Thermal noise model of MOSFET as current source. 13

Figure 3.4. Thermal noise model of MOSFET as voltage source. 14

Figure 3.5. Miller resistor model. 14

Figure 3.6. Single-Ended matching network. 15

Figure 3.7. Single-Ended matching network s-domain equivalent. 16

Figure 3.8. Matching network frequency response. 16

Figure 4.1. Two-stage fully differential low noise amplifier. 18

Figure 4.2. LNA drain current vs noise figure and gain. 19

Figure 4.3. LNA CMFB resistor vs noise figure and gain. 19

Figure 4.4. Single-stage fully differential low noise amplifier. 20

Figure 4.5. Small signal equivalent model of the low noise amplifier with matching network. 21

Figure 4.6. LNA noise model. 21

Figure 4.7. Noise figure calculation and simulation results. 24

Figure 4.8. Input pair finger width vs noise figure. 24

Figure 4.9. Simulated AC gain of the low noise amplifier. 25

Figure 4.10. Simulated input referred 1dB compression point of the low noise amplifier. 25

Figure 4.11. Low noise amplifier layout. 26

Figure 4.12. Low noise amplifier post-layout simulation results for (a)noise figure, (b)AC gain. 26

Figure 4.13. Comparison of schematic and post-layout simulation results for the LNA: (a) Noise figure, (b) AC gain. 27

Figure 5.1. Gilbert mixer cell. 29

Figure 5.2. Folded mixer schematic. 30

Figure 5.3. DC transfer characteristic of the folded mixer. 31

Figure 5.4. LO power vs conversion gain of the folded mixer. 31

Figure 5.5. Folded mixer layout. 32

Figure 5.6. Total harmonic distortion of the folded mixer. 32

Figure 6.1. Block diagram of the designed circuit. 34

Figure 6.2. Schematic and post-layout simulation results of the entire system for (a)conversion gain, (b)double-sideband (DSB) noise figure. . . 34

Figure A.1. Coilcraft air core inductors datasheet page 1. 42

Figure A.2. Coilcraft air core inductors datasheet page 2. 43

Figure A.3. Coilcraft air core inductors datasheet page 3. 44

LIST OF TABLES

Table 4.1. Table of schematic and post-layout simulation results for the low noise amplifier. 27

Table 5.1. Table of schematic and post-layout simulation results for the folded mixer. 33

Table 6.1. Table of schematic and post-layout simulation results for the entire system. 35

LIST OF SYMBOLS

A_{CG}	Conversion Gain
A_f	Closed-Loop Gain
A_v	Voltage Gain
B_0	Magnetic Field
C	Capacitance
C_c	Coupling Capacitor
f_{Larmor}	Larmor Frequency
g_m	Device Transconductance
I_D	Drain Current
$\overline{I_n^2}$	Thermal Current Noise
k'	Process Transconductance Parameter
L	Inductance
R	Resistance
R_s	Source Resistance
V_{A_N}	Early Voltage of NMOS transistor
V_{A_P}	Early Voltage of PMOS transistor
V_{DS}	Drain to Source Voltage
V_{GS}	Gate to Source Voltage
V_{ov}	Overdrive Voltage
V_s	Voltage Source
V_{th}	Threshold Voltage
$\overline{V_n^2}$	Thermal Voltage Noise
X	Reactance
Z_{in}	Input Impedance
α	Voltage Gain of the Matching Network
β	Feedback Factor
γ	Excess Noise Coefficient

γ_{gr}	Gyromagnetic Ratio

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital Converter
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
ENOB	Effective Number of Bits
IF	Intermediate Frequency
IIP3	Third Order Input Intercept Point
IV	Current-Voltage
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MRI	Magnetic Resonance Imaging
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NF	Noise Figure
NMOS	N-Channel MOSFET
PCB	Printed Circuit Board
PDK	Process Design Kit
PMOS	P-Channel MOSFET
RF	Radio Frequency
SINAD	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
UMC	United Microelectronics Corporation

1. INTRODUCTION

Magnetic Resonance Imaging (MRI) is a non-invasive medical imaging technique used to visualize the internal body structures. The MRI device utilizes a strong magnetic field and radio-frequency (RF) signals to first align and then excite the spins of atomic nuclei in body tissues [1]. The emitted signals from these excited spins are then received and processed to create detailed images. During this process, three main components work together: a giant magnet, gradient coils, and RF coils. The magnet produces the DC magnetic field B_0. Gradient coils enable three-dimensional image encoding. RF coils both excite the nuclei of the body tissues and receive the signals emitted from the excited body tissues. MRI is a broad field of study, with numerous research efforts focused on improving its performance [2–4]. In [2], compact NMR systems were developed, highlighting advancements in size reduction. A low-cost coil and on-chip NMR probe was designed in [4], making NMR systems more portable and cost-effective. The selection of an RF coil is critical for achieving optimal imaging in MRI systems. A comprehensive guide for choosing the appropriate MRI coil is provided in [3]. A low-noise CMOS receiver for 7T MRI applications was introduced in [5]. The work in [6] presents an MRI device featuring a fully integrated, digitally-assisted CMOS RF transceiver IC, delivering high-resolution imaging in a remarkably compact volume. In [7], a CMOS receiver designed for wearable coil arrays in 3T and 7T MRI measurements, with the ASIC mounted on a flexible PCB substrate. This thesis focuses on the design of a low voltage CMOS RF receiver circuit for the MRI system.

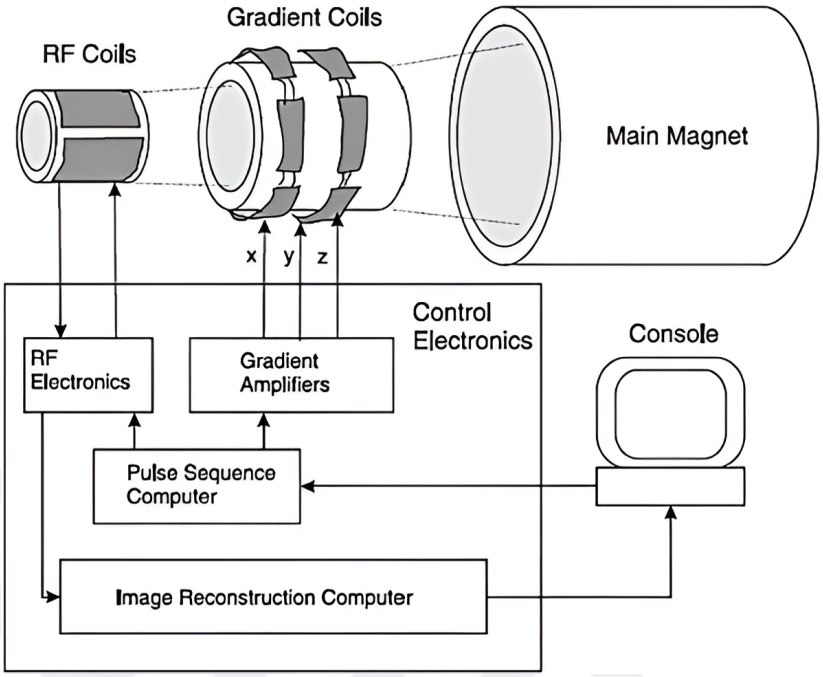

Figure 1.1. MRI scanner components [1].

The frequency of the signal emitted from the excited body tissues depends on the strength of the magnetic field B_0, as calculated by the Larmor equation [8]

$$f_{Larmor} = \gamma_{gr} B_0 \tag{1.1}$$

where f_{Larmor} is the Larmor or precessional frequency, and γ_{gr} is a constant known as the gyromagnetic ratio. Its value for hydrogen (H) atom is 42.6 MHz/Tesla. Thus, this constant, along with the magnetic field strength, determines the Larmor frequency, which is the frequency of the signal received by the electronic receiver circuit. Depending on the application, the magnetic field strength may vary from 1.5T up to 10.5T [9]. Fields of 1.5T and 3T are commonly used in medical applications [10]. This thesis focuses on a field strength of 1.5T. Consequently, the frequency of the received signal will be approximately 64 MHz.

The thesis is outlined as follows. Chapter 2 begins by explaining the receiver architecture in Section 2.1 introducing the blocks of the receiver. It then details the blocks that will be designed in this thesis and describes the system's power supply.

Finally, the operating frequency and noise figure requirements are discussed. In Section 2.2, the analysis of the transistors in 65nm technology is conducted to gain insight into the technology. chapter 3 first introduces the three main types of noise: shot noise, flicker noise, and thermal noise, with a particular focus on thermal noise. The noise equations for each circuit component in the design are derived. Finally, the concepts of impedance and noise matching are introduced, focusing more on noise matching due to the goal of achieving a low noise figure. Chapter 4 presents two designs of fully differential, low-voltage, low noise amplifiers. The first design and its equations are obtained from [11]. After analyzing the first design, a second, more compact design is proposed. The gain and noise equations for this design are derived in detail. The results from calculations, schematic simulations, and post-layout simulations are then compared. Chapter 5 discusses the mixer circuit design. It begins with an overview of the Gilbert Mixer Cell. Then the requirement of low voltage design is pointed out. Subsequently, a folded mixer structure is proposed to accommodate the low voltage design requirement. The schematic and post-layout simulation results of the folded mixer are then compared. The simulation results of the entire system are presented, and the circuit's performance is tabulated in chapter 6. Finally, in chapter 7, the overall work and obtained results are summarized. The strengths and weaknesses of the design, along with the trade-offs required to improve the circuit, are discussed.

2. SYSTEM DESCRIPTION

2.1. Receiver Architecture

Receiver designs are mostly based on two architectures: homodyne (also known as zero-IF or direct conversion) and heterodyne topologies [12]. The main difference between these two topologies lies in their signal conversion approach. While homodyne receivers convert the input signal frequency directly to baseband, heterodyne receivers use an intermediate frequency (IF) stage. Consequently, the latter has a more complex structure than the former. There are various receiver architectures available for MRI systems [5–7]. The overall receiver topology planned in this study is shown in Figure 2.1. This homodyne system is being developed by a project team, with each member focusing on a different block. This thesis specifically focuses on the Low Noise Amplifier (LNA) and the Mixer, essential components responsible for amplifying and downconverting the received signal, respectively.

The novel aim of the project is to generate a supply voltage through a monolithic CMOS photodiode powered by a laser via a fiber optic cable. The intention is to generate the supply voltage directly from the photodiode without the need for a DC/DC converter. This requires a unique photodiode design, currently under development by another participant in the project. An on-chip photodiode can typically generate a voltage of up to approximately 0.65V [13]. Through some design methods, this voltage can be increased to approximately 0.9V [14]. Given this information and objective, the project aims for a low-voltage design to ensure that the photodiode can adequately power the circuit. Consequently, the LNA and Mixer are designed to operate with a 0.9V supply voltage.

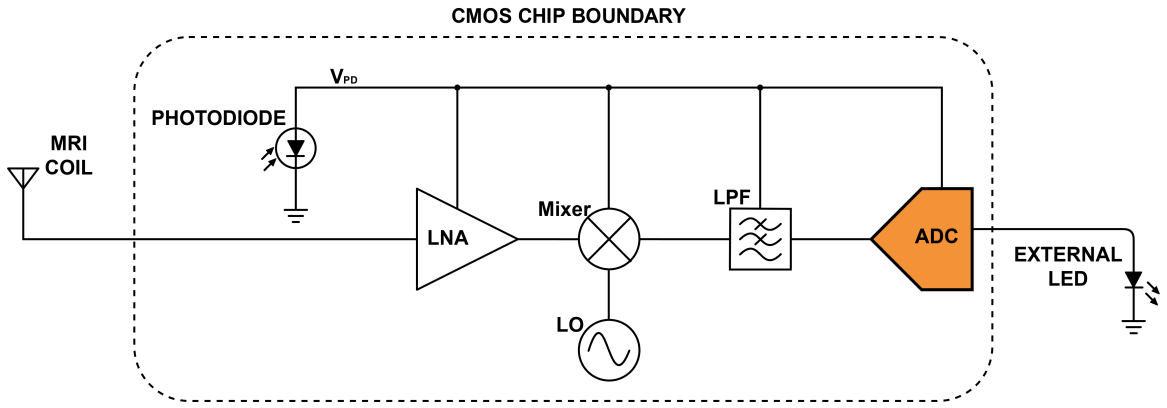

Figure 2.1. Block diagram of the overall system.

The 64 MHz MRI signal is received through the coil, amplified by the LNA, and downconverted with the mixer to 500 kHz. The downconversion requires the local oscillator (LO) frequency to be either 63.5 MHz or 64.5 MHz. Although the difference is minor, the LO frequency is selected as 64.5 MHz to maximize the spectral separation between the downconverted signal and the undesired upconverted image frequency.

The performance requirements of the Analog-to-Digital Converter (ADC) along with the bandwidth requirement of 500 kHz, will determine the properties of the Low-Pass Filter (LPF). The Effective Number of Bits (ENOB) of an Analog-to-Digital Converter is calculated as [15]

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{2.1}$$

where SINAD is the Signal-to-Noise and Distortion Ratio. According to the equation, to obtain an effective number of bits ranging from 12 to 16, a signal-to-noise and distortion ratio of 75 dB to 100 dB is required. To meet this requirement, the receiver must achieve a noise figure of less than 1 dB.

2.2. CMOS Technology

65nm technology from UMC is utilized in the designs. Due to the low supply voltage, the transistors operate within a restricted voltage range. The technology offers transistors with various threshold voltages (V_{th}). 65nm technology from UMC provides NMOS and PMOS transistors with low threshold voltages. Additionally, the PDK includes native NMOS transistors. A Native NMOS transistor, also called zero threshold transistor, is a type of MOSFET with a threshold voltage close to zero. It is commonly used in low-voltage applications [16].

The I-V characteristics of the transistors are analyzed in this section. The I_D-V_{DS} curves of low threshold NMOS, native, and low threshold PMOS transistors are shown in Figures 2.2, 2.4, 2.6, respectively. Similarly, I_D-V_{GS} curves are shown in Figures 2.3, 2.5, 2.7. These graphs help determine the optimal operating point and provide intuition about the technology. Although operating points can be generated by modern design tools, having an initial understanding of the technology is beneficial.

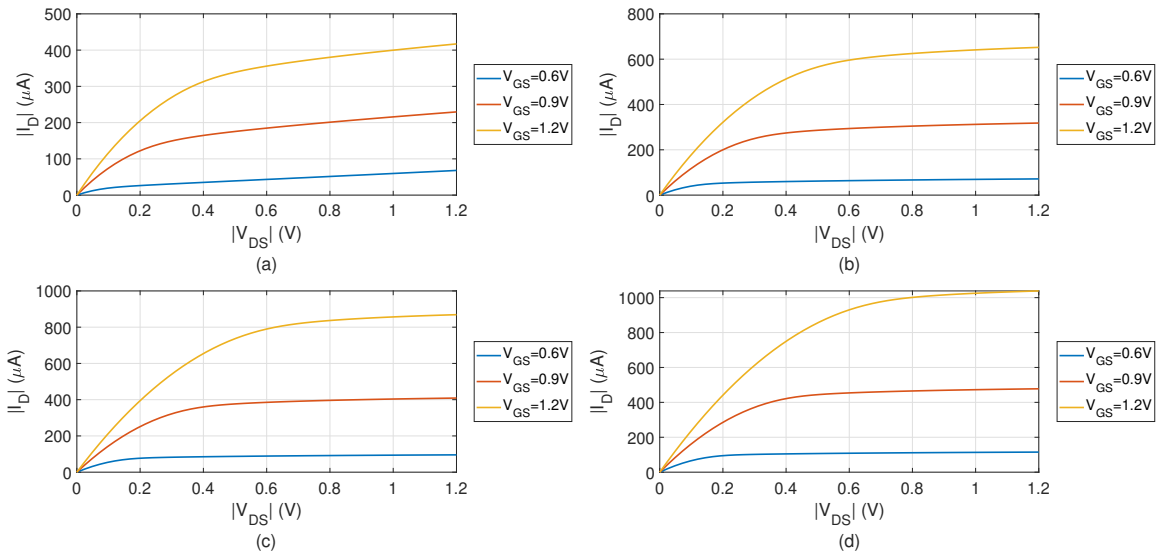

Figure 2.2. I_D-V_{DS} characteristics of a low threshold N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$.

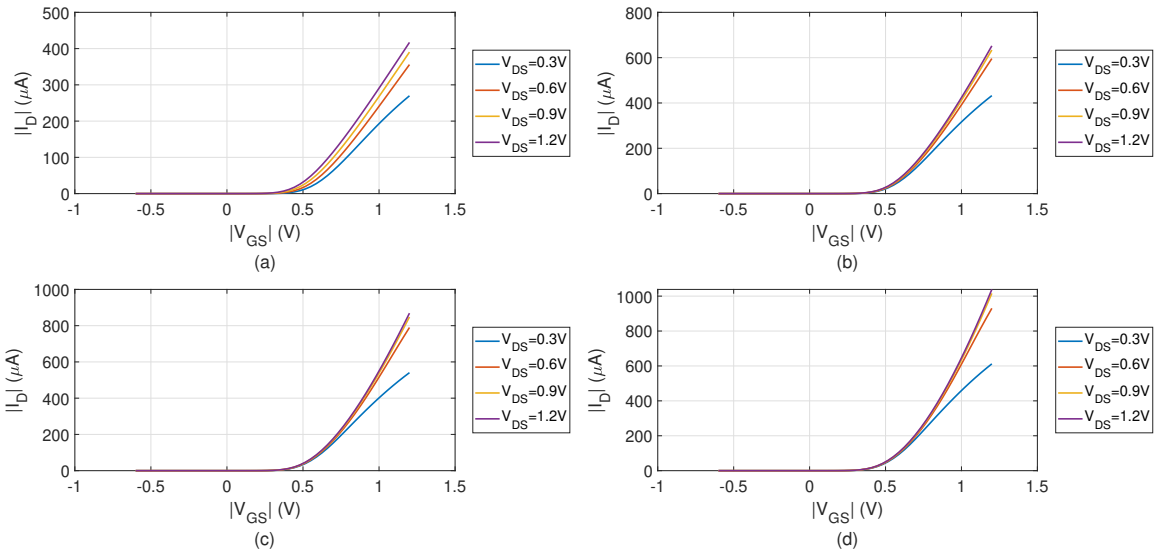

Figure 2.3. I_D-V_{GS} characteristics of a low threshold N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$.

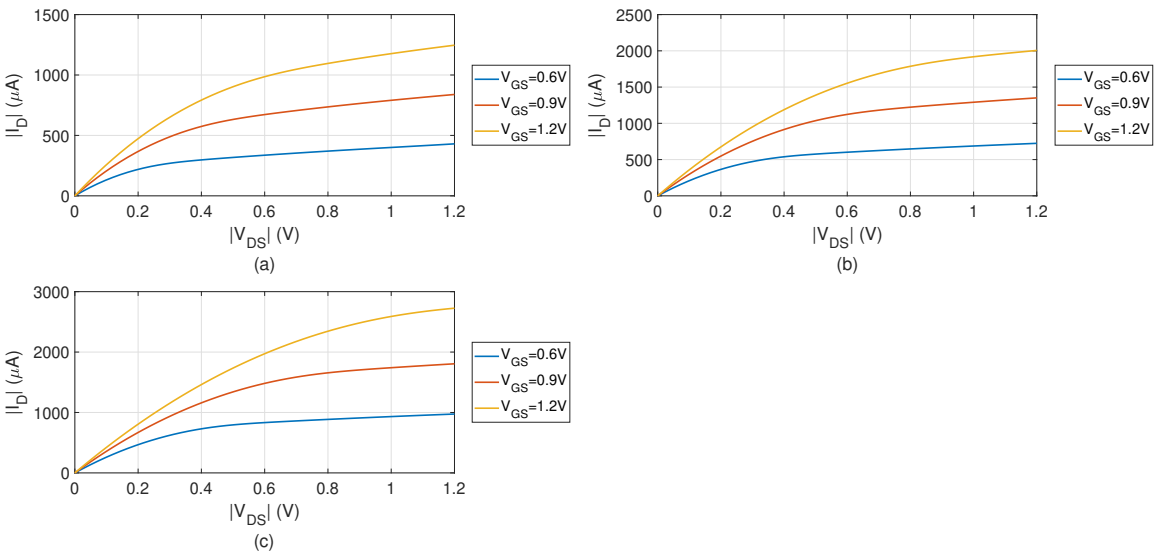

Figure 2.4. I_D-V_{DS} characteristics of a native N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 200nm$, (b) $L = 500nm$, (c) $L = 1\mu m$.

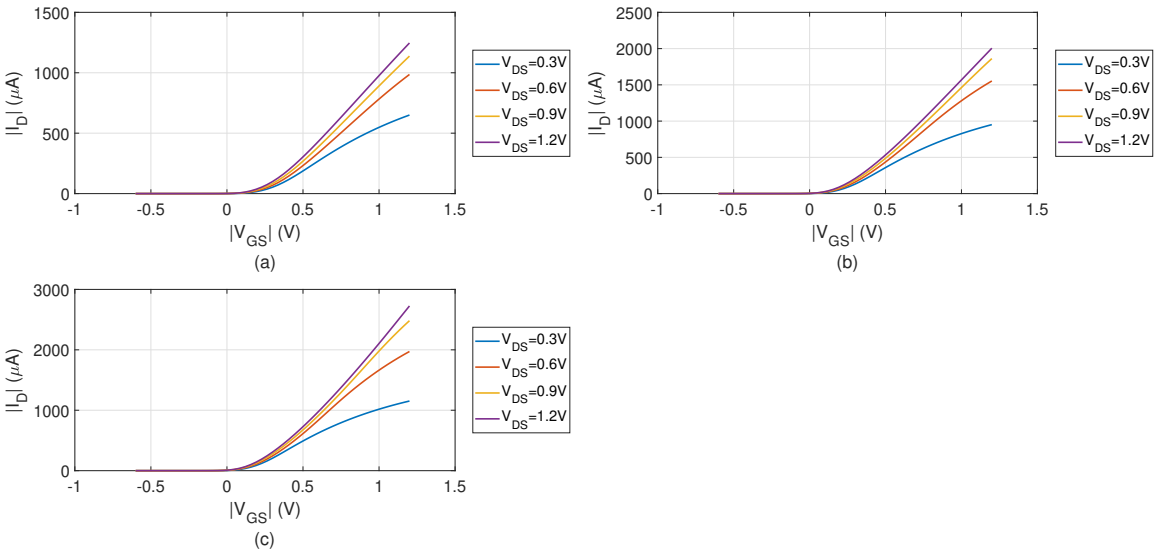

Figure 2.5. I_D-V_{GS} characteristics of a native N-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 200nm$, (b) $L = 500nm$, (c) $L = 1\mu m$.

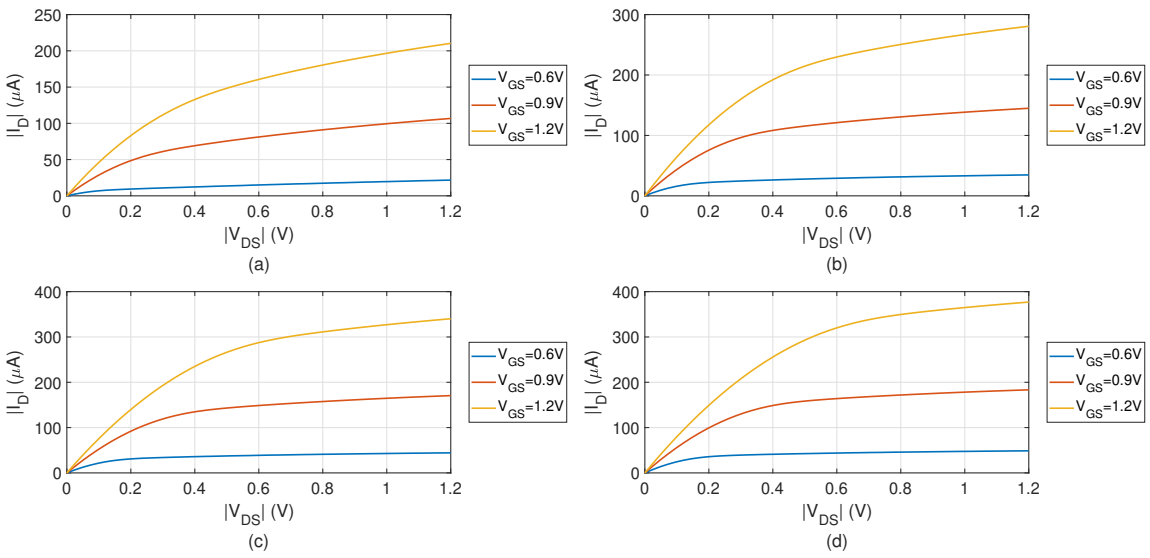

Figure 2.6. I_D-V_{DS} characteristics of a low threshold P-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$.

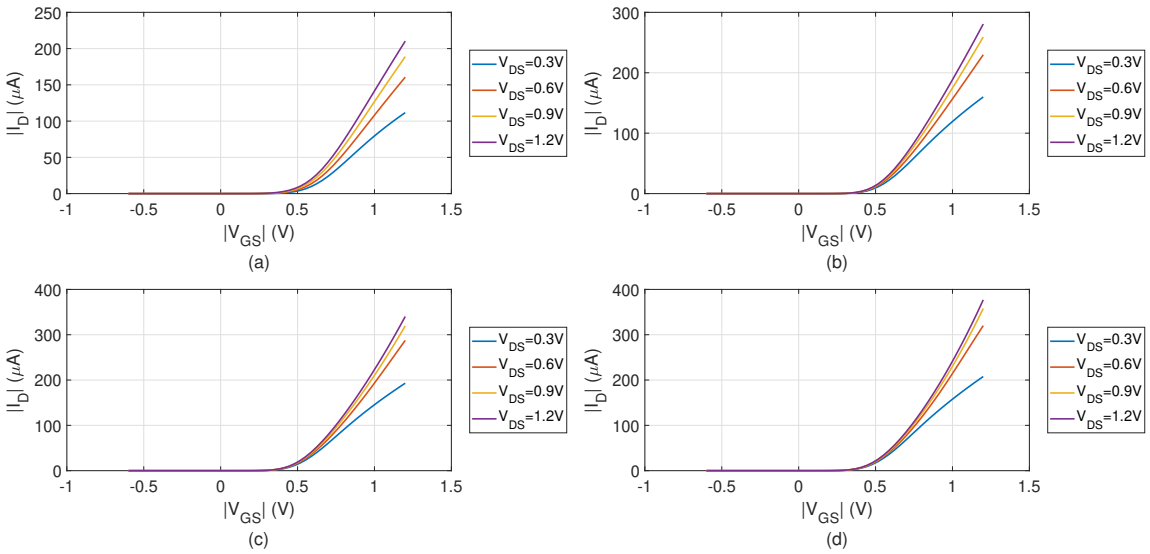

Figure 2.7. I_D-V_{GS} characteristics of a low threshold P-Channel MOSFET with a constant W/L ratio of 10 for (a) $L = 65nm$, (b) $L = 200nm$, (c) $L = 500nm$, (d) $L = 1\mu m$.

The analysis aims to fit the transistor models to the well-known saturation region equation for MOS transistors, given by

$$I_D = \frac{1}{2}k'\frac{W}{L}\left(|V_{GS}| - |V_{th}|\right)^2 \tag{2.2}$$

where k' is the process transconductance parameter, W/L is the width-to-length ratio, V_{GS} is the gate-to-source ratio and V_{th} is the threshold voltage. Please note that this equation was derived for earlier transistor models. Modern MOSFET models are significantly more complex [17]. Nevertheless, Eq. 2.2 is very straightforward and is still immensely useful for estimating the design's behavior.

Based on the analyses described in this section, the approximate operating parameters are as follows:

- For low-threshold NMOS: $V_{th} = 0.4V$, $k' = 144.87\frac{\mu A}{V^2}$.
- For native NMOS: $V_{th} = 0.15V$, $k' = 170.627\frac{\mu A}{V^2}$.
- For low-threshold PMOS: $V_{th} = -0.25V$, $k' = 62.15\frac{\mu A}{V^2}$.

In addition to transistors, resistors are essential in the design. The PDK provides resistors made from highly resistive polysilicon, enabling the use of resistances in the range of hundreds of kilo-ohms within the design.

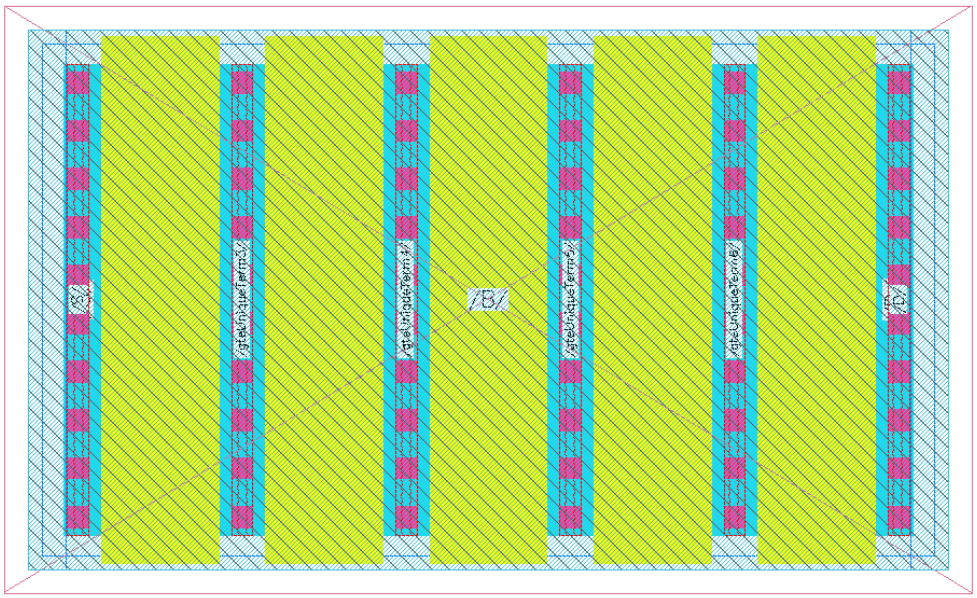

Figure 2.8. Layout of the native NMOS.

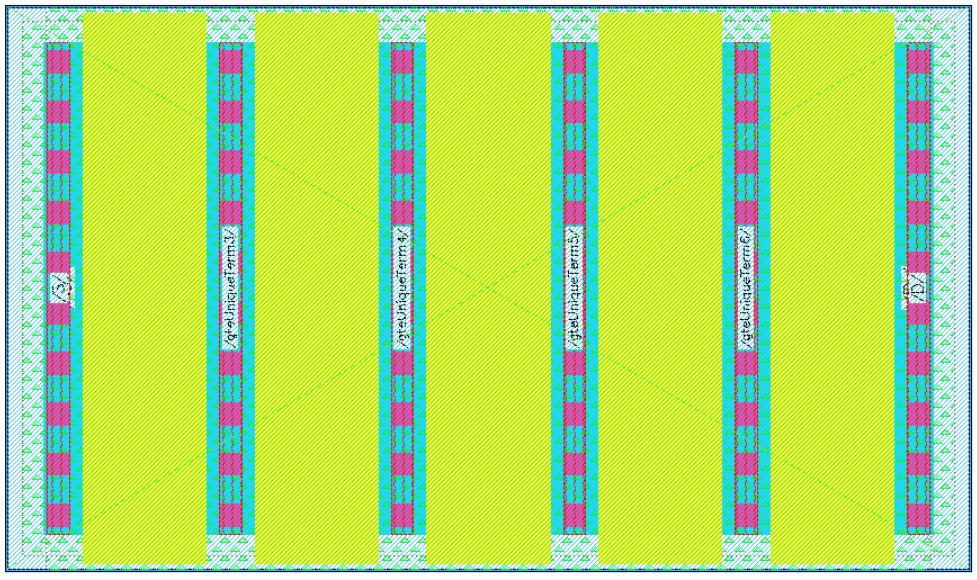

Figure 2.9. Layout of the PMOS.

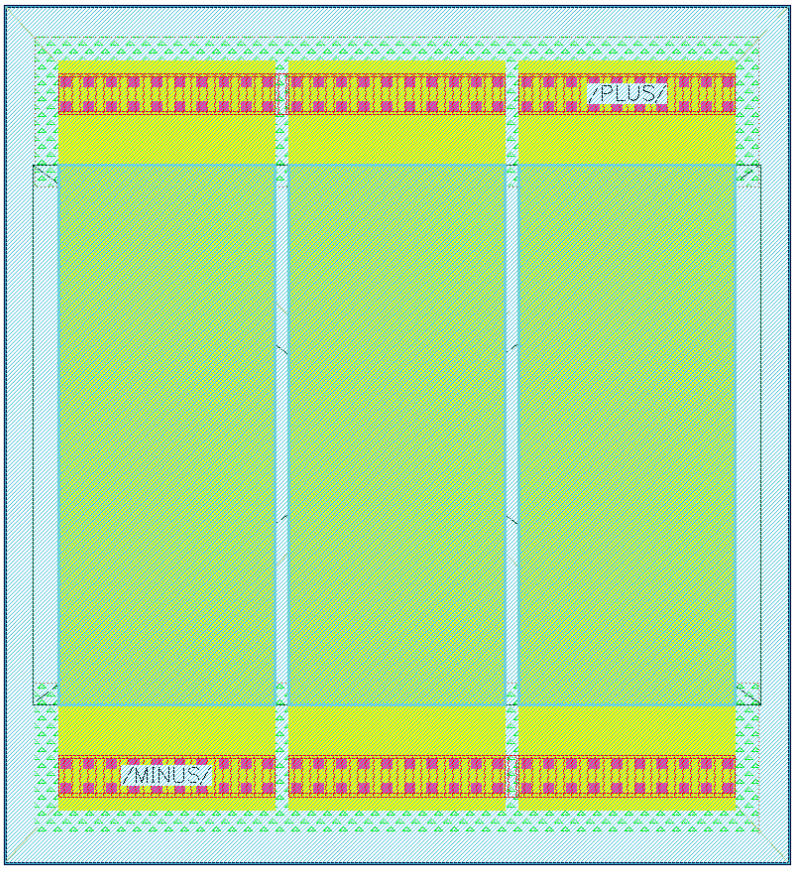

Figure 2.10. Layout of a highly resistive polysilicon resistor.

The native NMOS and low threshold PMOS transistors were selected for the designs. Layout examples of NMOS and PMOS transistors with fingers, and the highly resistive polysilicon resistor are shown in Figures 2.8, 2.9, 2.10, respectively.

3. NOISE

Noise is one of the main limitations in electronic circuits. It can be defined as small unwanted perturbations caused by several factors that interfere with the original signal. The instantaneous level of noise is completely random, making it impossible to measure. Therefore, noise is measured as average power. The three main sources of noise are shot noise, flicker noise, and thermal noise [18]. Shot noise occurs in active devices and is caused by the fluctuations and randomness in the number of carriers crossing through the junction [19].

Flicker noise, also known as 1/f noise, has an inverse relationship with frequency, making it dominant at lower frequencies. Although typically dominant up to a few kHz [20], flicker noise can extend to MHz levels in emerging CMOS technologies [21,22]. Thermal noise, also known as Johnson-Nyquist noise, is caused by the random thermal motion of electrons. It is proportional to the absolute temperature and the resistance of the device [20]. Due to the shot noise being smaller and operation at a relatively high frequency, shot noise and flicker noise are omitted, and only the thermal noise model is considered in the analysis.

3.1. Thermal Noise Model of Resistors

The thermal noise can be modeled either as a voltage or a current source [12,20], as shown in Figures 3.1 and 3.2. The choice depends on the ease of the analysis. The noise is calculated using Power Spectral Density.

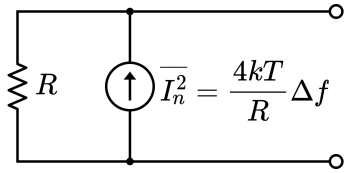

Figure 3.1. Norton model of resistor noise.

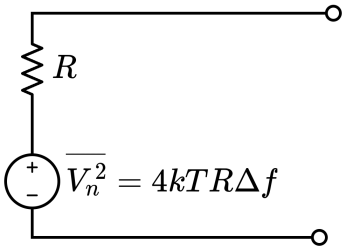

Figure 3.2. Thevenin model of resistor noise.

Thermal current noise and voltage noise of the resistor are calculated as

$$\begin{aligned} \overline{I_n^2} &= \frac{4kT}{R}\Delta f, \\ \overline{V_n^2} &= \overline{I_n^2}R^2 = 4kTR\Delta f, \end{aligned} \tag{3.1}$$

respectively. The Boltzmann constant, denoted by k, is defined as 1.380649×10^{-23} J/K [23], and T represents the temperature in Kelvin, which is typically taken as 300K for room temperature. The term Δf denotes the bandwidth. Since we are interested in the noise performance at 64 MHz, Δf can be taken as 1 Hz. Thus, the calculated noise is referred to as spot noise.

3.2. Thermal Noise Model of MOSFETs

The thermal noise of MOS devices in the saturation region is modeled as either a current source connected between the source and drain terminals or a voltage source connected in series with the gate terminal [12,20]. The models are illustrated in Figures 3.3 and 3.4.

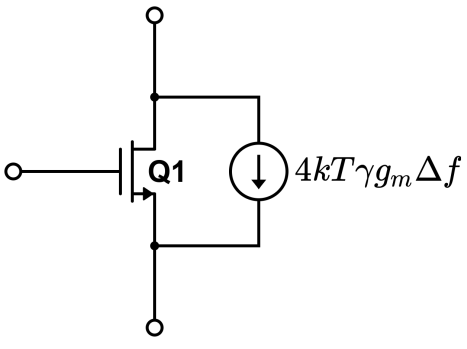

Figure 3.3. Thermal noise model of MOSFET as current source.

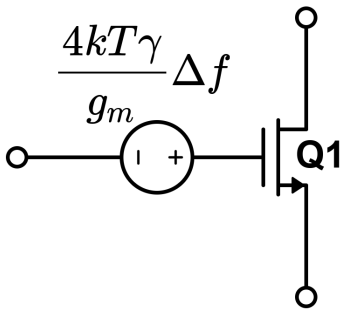

Figure 3.4. Thermal noise model of MOSFET as voltage source.

3.3. Noise Analysis of Miller Resistance

According to Miller's Theorem [24], the feedback resistor in an amplifier can be divided to the input and output nodes with respect to the gain of the amplifier, as shown in Figure 3.5. To find its noise contribution, the noise current generated by the feedback resistor is multiplied by the equivalent impedance seen at the node. The gain of the amplifier then amplifies the voltage noise to the output, formulated as

$$\overline{V_{n,R_f}^2} = \frac{4kT}{R_f}\left(R_{in} \parallel \frac{R_f}{1+|A|}\right)^2 A^2 \tag{3.2}$$

where A is the gain of the amplifier, R_f is the feedback resistor, R_{in} and R_{out} are the input and output impedances, respectively.

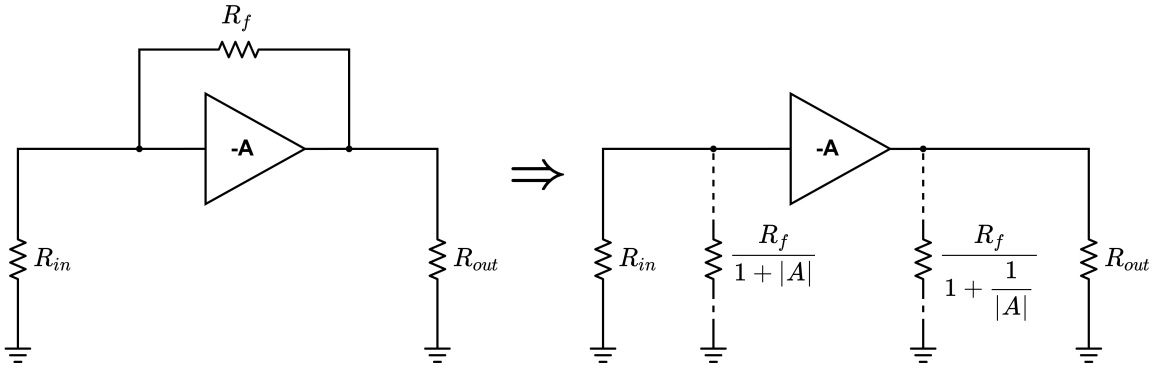

Figure 3.5. Miller resistor model.

3.4. Impedance and Noise Matching

Impedance matching is essential in RF circuits for maximizing power transfer and minimizing signal reflections. However, in low noise amplifier design, achieving the lowest possible noise figure often takes precedence over power transfer. This concept, known as noise matching, focuses on maximizing the voltage delivered to the LNA input [25], thereby achieving a low noise figure.

A single-ended matching network is illustrated in Figure 3.6. For perfect impedance matching, Z_{in} should be equal to R_s which is typically 50Ω. For noise matching, the impedance should be set to a level that minimizes the noise figure while maintaining a sufficient passive voltage gain. The load impedance $R-jX$ is measured from the input of the receiver's first stage; in other words, it is the input impedance of the Low Noise Amplifier. R and X denote the equivalent resistance and reactance, respectively.

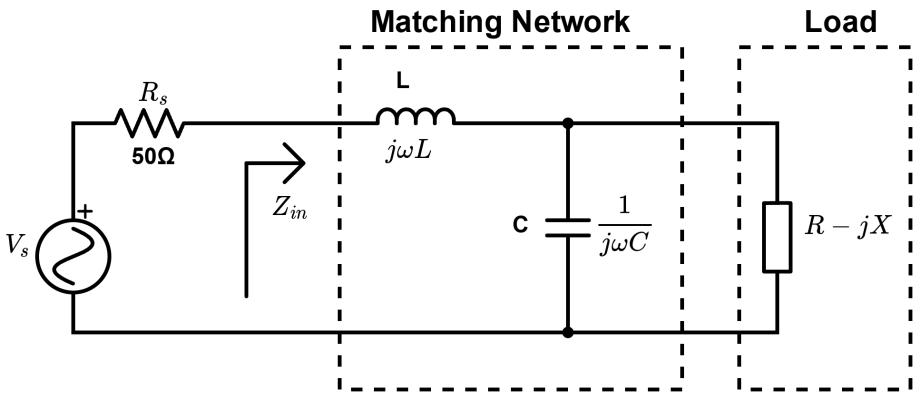

Figure 3.6. Single-Ended matching network.

The impedance seen by the source is derived as

$$Z_{in} = j\omega L + \frac{1}{j\omega C} \parallel (R - jX). \tag{3.3}$$

This value represents the impedance of the Low Noise Amplifier connected with the matching network. The s-domain equivalent is illustrated in Figure 3.7. The input impedance of the LNA, represented as $R - jX$ can be converted into a parallel R and C model.

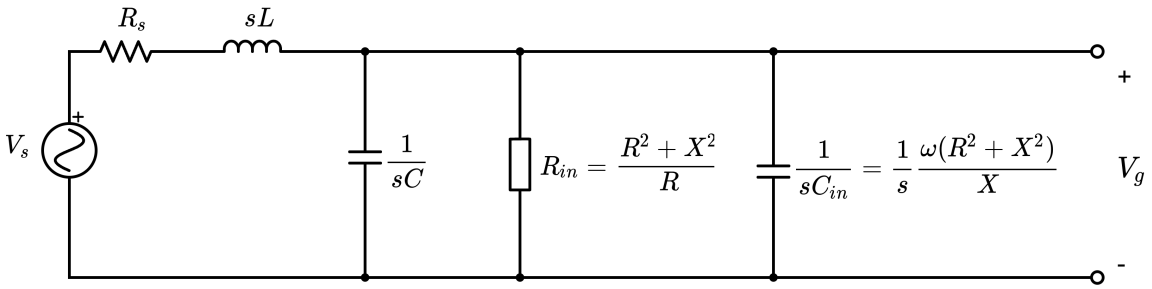

Figure 3.7. Single-Ended matching network s-domain equivalent.

The transfer function of the overall RLC network is calculated as

$$\alpha(s) = \frac{V_g}{V_s} = \frac{\frac{1}{sC} \parallel R_{in} \parallel \frac{1}{sC_{in}}}{\left(\frac{1}{sC} \parallel R_{in} \parallel \frac{1}{sC_{in}}\right) + R_s + sL}. \tag{3.4}$$

By adjusting L and C, an optimal point can be found where the output resonates at the desired frequency, a passive voltage gain is achieved, and noise figure is minimized. Figure 3.8 illustrates the output of the transfer function for $R_s = 50\Omega$, $L = 1\mu H$, $C = 5.1pF$, $R - jX = 106.9 - j2.342k\Omega$.

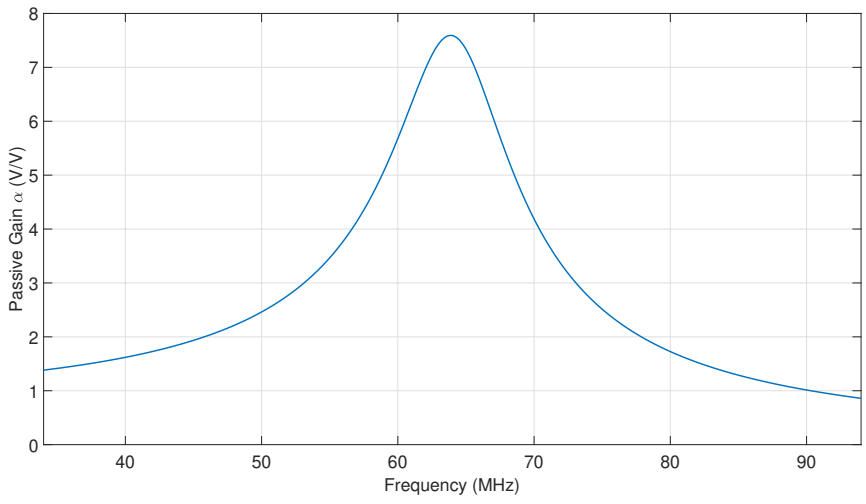

Figure 3.8. Matching network frequency response.

4. FULLY DIFFERENTIAL LOW VOLTAGE LOW NOISE AMPLIFIER

A fully differential system offers immunity to disturbances and external noise. The differential amplifier eliminates even harmonics, resulting in reduced harmonic distortion. Carrying halves of the signal at differential nodes allows for better voltage swing [26]. Furthermore, the mixer, to which the LNA output is connected, requires a differential input signal. For all these reasons, a fully differential topology was chosen.

4.1. The First Approach: Two Stage LNA

The two stage Low Noise Amplifier Circuit in Figure 4.1 was inspired by [11]. The first stage is the LNA, and the second stage is the gain stage. The resistors R_{cf_1} and R_{cf_2} are used as common-mode feedback resistors, which bias the load transistors. The resistors R_{f1} and R_{f2} are the DC feedback resistors, providing DC bias to the input pair. Choosing a high C_f creates an AC ground on it, so only DC voltage is fed back to the input. The noise figure equation of the circuit is derived as [11]

$$NF = 10log_{10}\left(1 + \frac{2}{\alpha^2 R}\left(\frac{1}{g_{m_1}^2 R_{cf_1}} + \frac{\gamma}{g_{m_1}} + \frac{\gamma g_{m_3}}{g_{m_1}^2}\right)\right) \tag{4.1}$$

where α is the voltage gain of the matching network. R is the resistance of the coil. γ is known as the "excess noise coefficient." It is a technology-dependent parameter, having a lower value in long-channel devices and a higher value in short-channel devices. Finding an accurate value for γ is a detailed work [27]. Therefore, its typical value of 2/3 for long-channel devices is used in this study.

The voltage gain of the first stage is calculated as

$$A_{v_1} = -g_{m_1}\left(r_{o_1} \parallel r_{o_3} \parallel R_{cf_1}\right). \tag{4.2}$$

Since both stages of the amplifier share the same topology, the same formula applies to the second stage. Using Eq. 4.1 and Eq. 4.2, an initial insight into the design can be obtained by finding an optimal point for the noise figure relative to current

consumption. For the analysis $R = 50\Omega$, $\alpha = 5$, $R_{cf_1} = 1k\Omega$, $\gamma = 0.7$, $V_{A_N} = 2.7V$, $V_{A_P} = 4.4V$ are chosen empirically. Derivation of α was given in Eq. 3.4. Due to its dependence on every component of matching network, a worst-case value is chosen. Finally, considering the low supply voltage, $|V_{ov}|$ is aimed to be around $0.15V$.

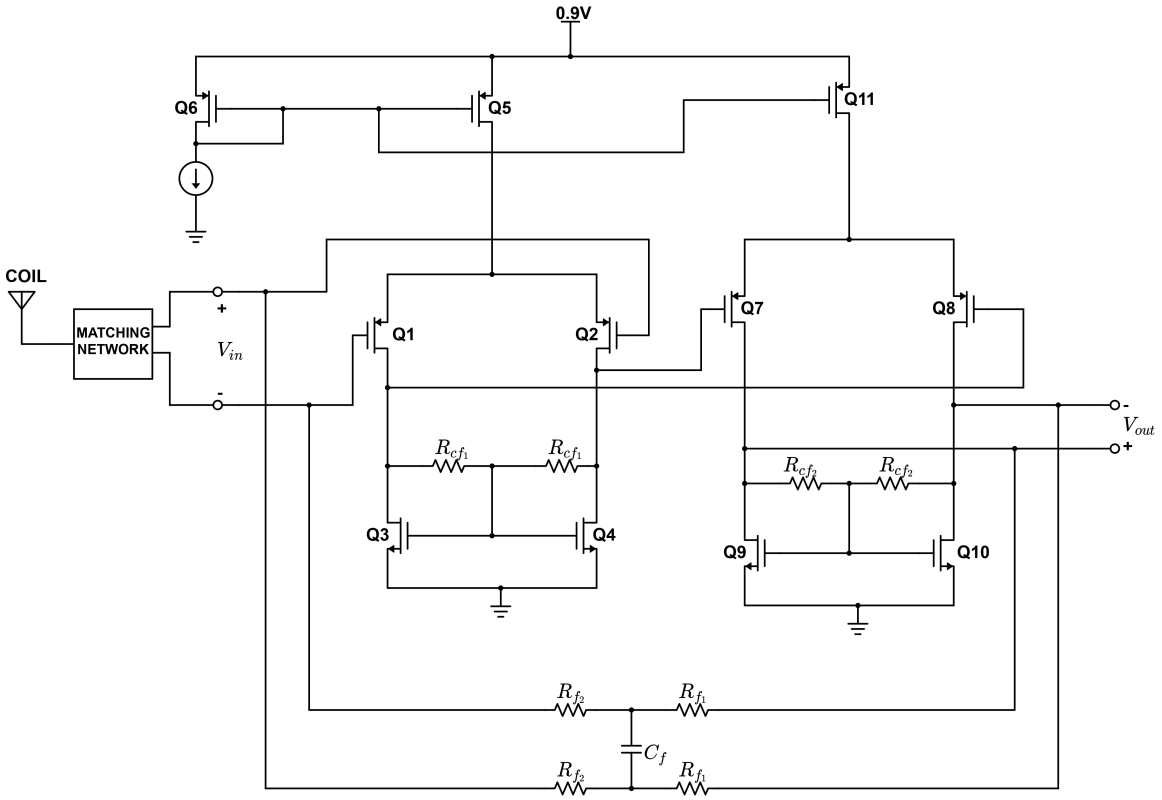

Figure 4.1. Two-stage fully differential low noise amplifier.

In Figure 4.2, the descent of noise figure saturates after a certain point. Therefore, increasing the current beyond this point will be futile. The optimum current for the design can be chosen as 1.5mA.

Figure 4.3 analyzes the effect of common-mode feedback resistor R_{cf_1} on noise figure and gain while maintaining a constant current consumption of 1.5 mA. The increase in voltage gain is more significant than the decrease in noise figure with increasing R_{cf}. Therefore, R_{cf} can be used for gain adjustment.

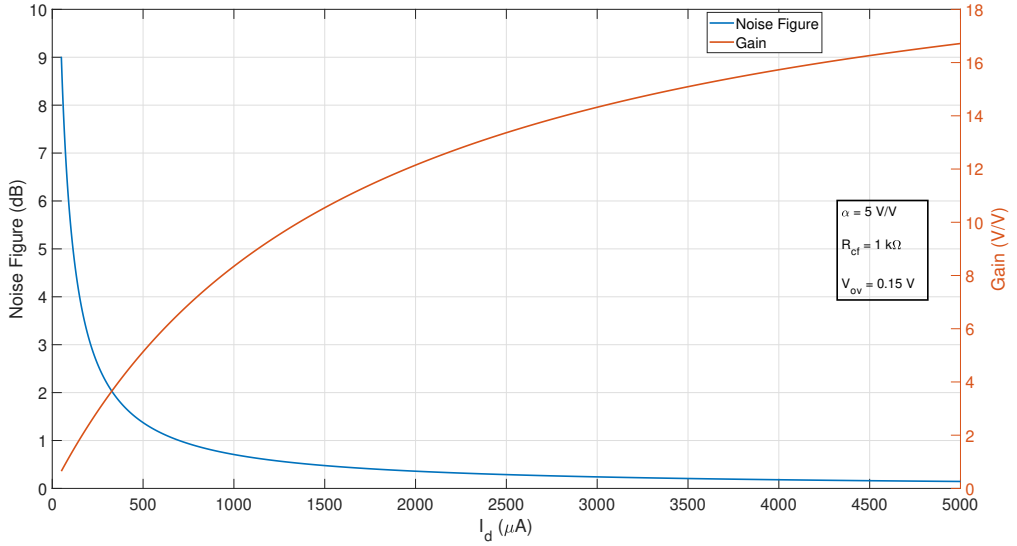

Figure 4.2. LNA drain current vs noise figure and gain.

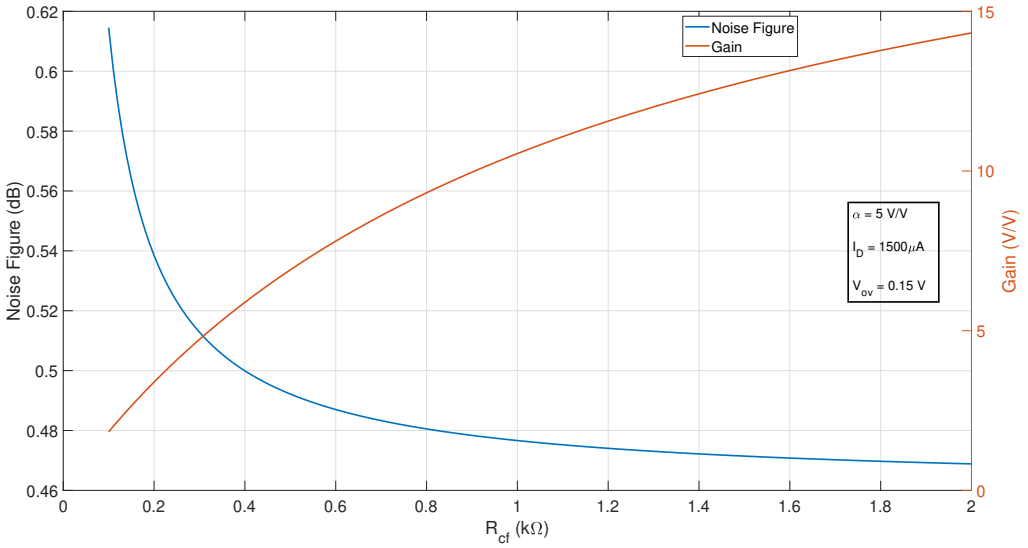

Figure 4.3. LNA CMFB resistor vs noise figure and gain.

This analysis is conducted only for the first stage of the amplifier. The second stage is utilized for controlling the gain. However, as observed from both analyses in Figures 4.2 and 4.3, only one stage can achieve sufficient amplification while maintaining acceptable noise performance. This result leads us to the Second Approach.

4.2. The Second Approach: Single Stage LNA

A more compact single-stage amplifier is shown in Figure 4.4. The coil input is modeled as an AC source in series with a source resistance R_s. L and C are the components of the matching network. Similar to the previous topology, R_{cf_1} resistors are used for common-mode feedback and setting the gain. C_c capacitors are coupling capacitors. R_{f1} resistors serve as feedback resistors that create current feedback, making this circuit a transimpedance amplifier. However, if a very high feedback resistor is chosen, the feedback factor β will decrease to near zero and the closed-loop gain A_f approximate the open-loop gain A. It is formulated as

$$0 < |\beta| = \left|\frac{-1}{R_{f_1}}\right| << 1 \Rightarrow A_f = \frac{A}{1 + A\beta} \approx A. \tag{4.3}$$

These feedback resistors maintain DC biasing with minimal AC feedback. This topology eliminates the need for an AC ground node on the feedback path, which was used in the previous design. The voltage gain of the circuit is formulated as

$$A_v = \frac{V_{out}}{V_{in}} = -g_{m_1}(r_{o1} \parallel r_{o3} \parallel R_{cf_1}). \tag{4.4}$$

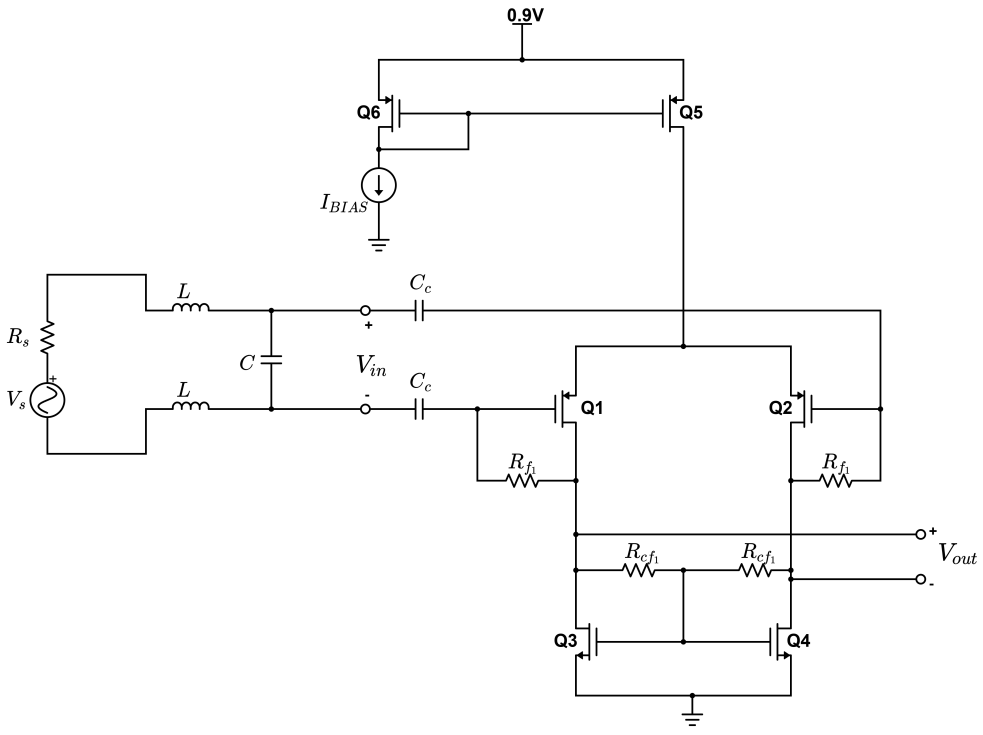

Figure 4.4. Single-stage fully differential low noise amplifier.

The effect of R_{f_1} on the gain is neglected due to its expected high value, which contributes very little.

An equivalent small signal model is shown in Figure 4.5. The values of R, X and R_{out} are obtained through simulation and used to calculate the equivalent impedance at the nodes. Please note that because it is a single-ended model, the value of L is doubled. In a differential model, L will be used for each input.

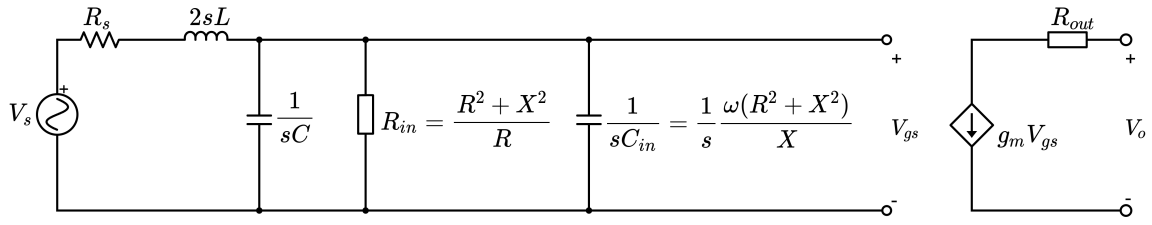

Figure 4.5. Small signal equivalent model of the low noise amplifier with matching network.

Figure 4.6 illustrates the equivalent noise circuit of the LNA. To calculate the noise contribution of the resistors R_s, R_{f_1}, R_{cf_1}, the equivalent impedance at the input and output nodes should be determined from the small signal model in Figure 4.5.

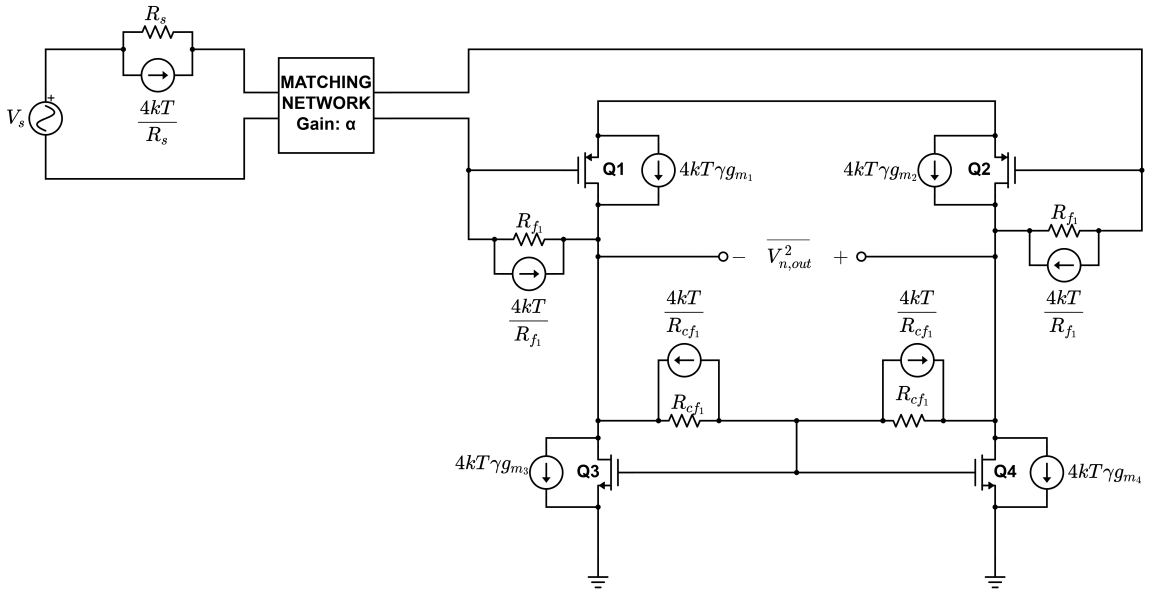

Figure 4.6. LNA noise model.

The thermal noise contributions of the PMOS input pair and the NMOS load are calculated in the same manner. The noise currents they generate are multiplied by the equivalent output impedance R_{out}. The noise of PMOS and NMOS are written as

$$\begin{aligned} \overline{V_{n,PMOS}^2} &= 4kT\gamma g_{m_1} R_{out}^2, \\ \overline{V_{n,NMOS}^2} &= 4kT\gamma g_{m_3} R_{out}^2, \end{aligned} \tag{4.5}$$

respectively.

The thermal noise current generated by the common-mode feedback resistor is multiplied by the R_{out}, written as

$$\overline{V_{n,R_{cf_1}}^2} = \frac{4kT}{R_{cf_1}} R_{out}^2. \tag{4.6}$$

Since R_{in} in Figure 4.5 includes the impedance caused by the Miller effect of the feedback resistor R_{f_1}, the thermal noise caused by the resistor R_{f_1} should be calculated at the input node and multiplied by the gain. Noise of the R_{f_1} at the output can be mathematically calculated as

$$\overline{V_{n,R_{f1}}^2} = \frac{4kT}{R_{f1}} \left| Z_{LNA_{in}} \right|^2 \left(\frac{A_v}{2} \right)^2. \tag{4.7}$$

The details of the calculation are explained in Section 3.3.

$Z_{LNA_{in}}$ in Eq. 4.7 denotes the equivalent impedance seen at the input node of the LNA, is formulated as

$$Z_{LNA_{in}} = \frac{1}{j\omega C_{in}} \parallel R_{in} \parallel \frac{1}{j\omega C} \parallel (2j\omega L + R_s). \tag{4.8}$$

Since R_s typically has a low impedance (mostly 50Ω in RF circuits), it largely determines the equivalent impedance by its value. Therefore, the thermal noise equation for the resistor R_s can be easily expressed as

$$\overline{V_{n,R_s}^2} = 4kTR_s. \tag{4.9}$$

With all the noise equations in hand, the total output noise of the differential circuit is calculated as

$$\overline{V_{n,out}^2} = 2 \times \left(\overline{V_{n,PMOS}^2} + \overline{V_{n,NMOS}^2} + \overline{V_{n,R_{cf_1}}^2} + \overline{V_{n,R_f}^2} \right) + \overline{V_{n,R_s}^2} \alpha^2 A_v^2. \tag{4.10}$$

To obtain the noise figure of the LNA, the input and output SNRs are required. The

SNR at the input of the LNA is calculated as

$$(SNR)_{in} = \frac{\alpha^2 V_{in}^2}{\alpha^2 \overline{V_{n,R_s}^2}}. \tag{4.11}$$

The output SNR Equation is formulated as

$$(SNR)_{out} = \frac{\alpha^2 A_v^2 V_{in}^2}{\alpha^2 A_v^2 \overline{V_{n,R_s}^2} + \overline{V_{n,LNA}^2}} = \frac{\alpha^2 A_v^2 V_{in}^2}{\overline{V_{n,out}^2}}. \tag{4.12}$$

Note that to obtain the output SNR, the input noise is amplified by the LNA gain and then added to the amplifier's noise. $\overline{V_{n,LNA}^2}$ in Eq. 4.12 is the output noise of the LNA. It is calculated as

$$\overline{V_{n,LNA}^2} = 2 \times \left(\overline{V_{n,PMOS}^2} + \overline{V_{n,NMOS}^2} + \overline{V_{n,R_{cf_1}}^2} + \overline{V_{n,R_f}^2} \right) = \overline{V_{n,out}^2} - \overline{V_{n,R_s}^2} \alpha^2 A_v^2. \tag{4.13}$$

By using the derived equations, the noise figure is calculated as

$$NF = \frac{(SNR)_{in}}{(SNR)_{out}} = \frac{\dfrac{\alpha^2 V_{in}^2}{\alpha^2 \overline{V_{n,R_s}^2}}}{\dfrac{\alpha^2 A_v^2 V_{in}^2}{\overline{V_{n,out}^2}}} = 1 + \frac{\overline{V_{n,LNA}^2}}{\alpha^2 A_v^2 \overline{V_{n,R_s}^2}}. \tag{4.14}$$

The noise figure equation can also be expressed in terms of the circuit parameters, mathematically derived as

$$NF = 1 + \frac{2 \left(\gamma (g_{m_1} + g_{m_3}) + \dfrac{1}{R_{cf_1}} + \dfrac{1}{4} \dfrac{g_{m_1}^2 \left| Z_{LNA_{in}} \right|^2}{R_{f1}} \right)}{R_s \alpha^2 g_{m_1}^2}. \tag{4.15}$$

Overall, the noise parameters in Eq. 4.14 are expanded in Eq. 4.15, reducing the equation to circuit parameters and therefore making it easier to analyze. The LNA is designed using UMC 65nm technology, operating at 2mA with a supply voltage of 0.9V. The transistor W/L ratios are as follows: $400\mu m/500nm$ for the input pair Q1 and Q2, $50\mu m/500nm$ for the active load Q3 and Q4, and $800\mu m/500nm$ for the tail transistor Q5. The differential input impedance $R_i - jX$ of the LNA is measured as $106.9 - j2342\Omega$. Optimal values for L and C, determined for a source resistance $R_s = 50\Omega$, are $500nH$ and $5.1pF$, respectively.

Circuit simulation is first conducted using ideal inductor models. Then, the Coilcraft 2929SQ-501 500nH air core inductor model [28] is used for a more realistic result. Figure 4.7 illustrates the noise figure results from both hand analysis and circuit simulations. The noise figure at 64 MHz is determined as 0.45 dB in theoretical

analysis, 0.41 dB in simulation using ideal inductors, and 0.61 dB in simulation using air core inductor models.

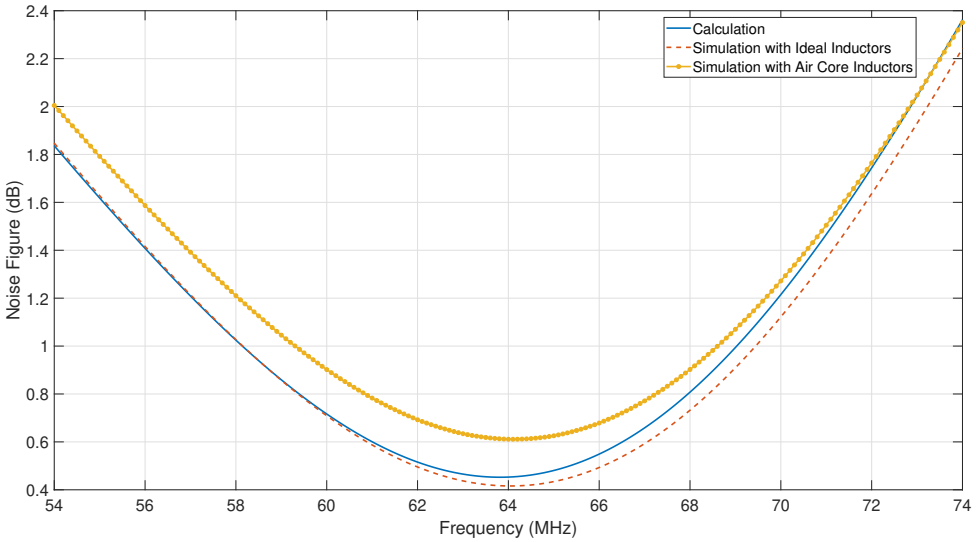

Figure 4.7. Noise figure calculation and simulation results.

The large widths of the transistors necessitate splitting them into multiples and fingers. Finger width is one of the factors affecting the noise figure. Figure 4.8 shows the increase in noise figure with increasing finger width. Although using transistors with smaller finger widths results in a lower noise figure, narrower finger widths cause excessively tall and narrow transistors, which are not effective for layout design. Therefore, finger widths are selected in a way that makes the layout more compact.

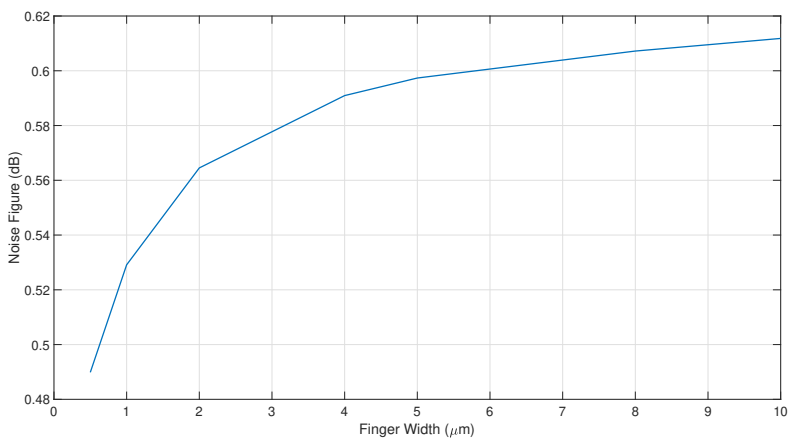

Figure 4.8. Input pair finger width vs noise figure.

The AC simulation result is shown in Figure 4.9. The output peaks at 64 MHz, achieving a gain of near 26 dB.

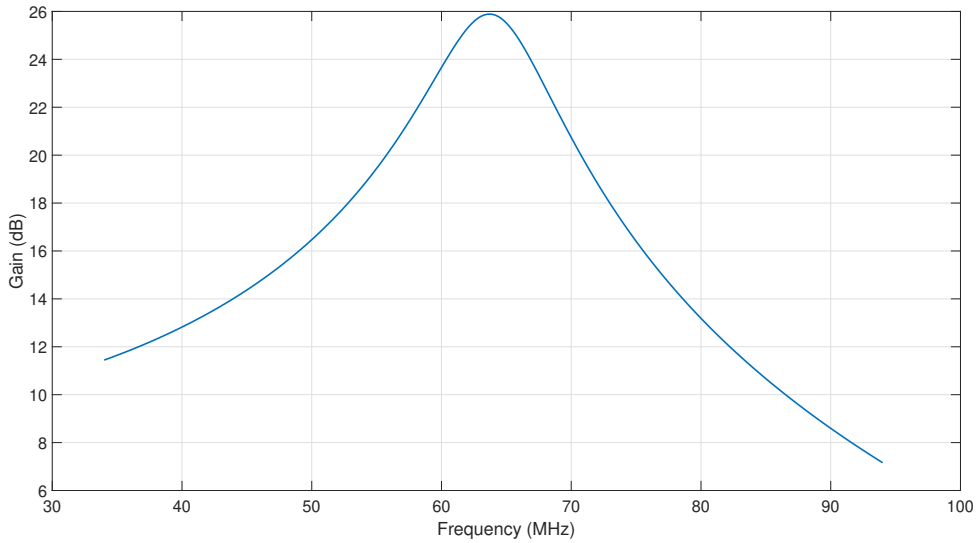

Figure 4.9. Simulated AC gain of the low noise amplifier.

Figure 4.10 illustrates the input referred 1dB compression point analysis. The 1dB compression point is reached at approximately -32 dBm.

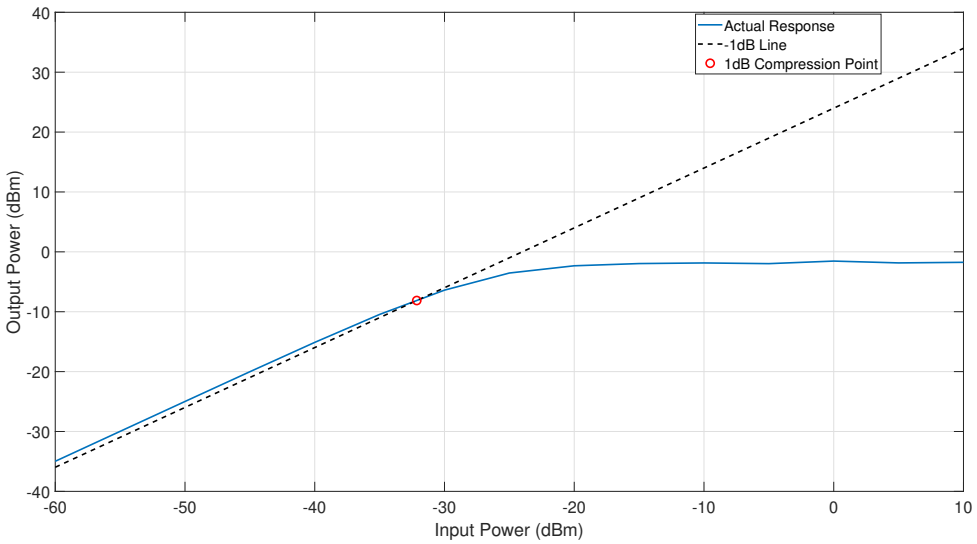

Figure 4.10. Simulated input referred 1dB compression point of the low noise amplifier.

The layout design of the LNA is illustrated in Figure 4.11. The layout employs a fully symmetric configuration, with the input pair transistors arranged in a common centroid configuration using an "ABBA-BAAB" structure. Thus, the effects of threshold mismatches are reduced [29–31].

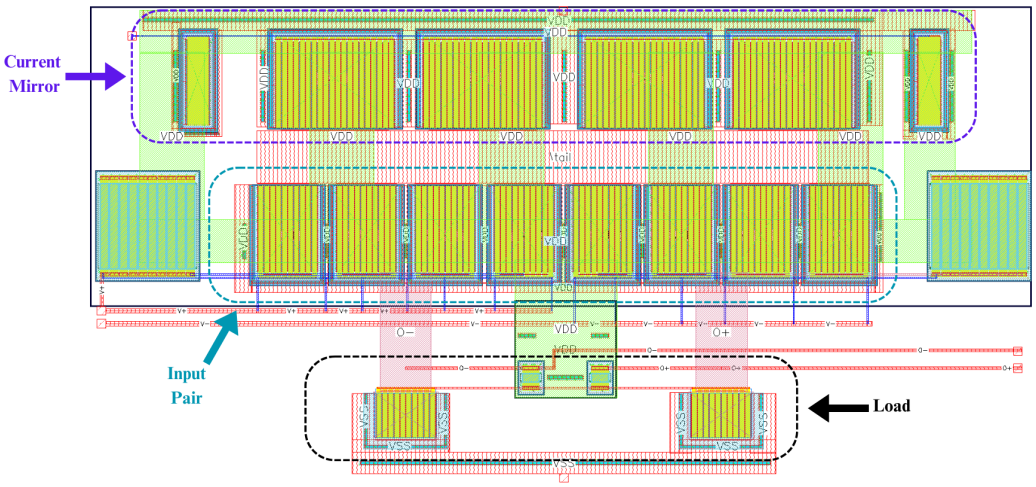

Figure 4.11. Low noise amplifier layout.

Figure 4.12 shows the noise figure and AC gain across the frequency range. A slight increase in the noise figure and a negligible shift in AC gain are observed. The noise figure is 0.71 dB, and the gain is around 25.8 dB at 64 MHz in the post-layout results.

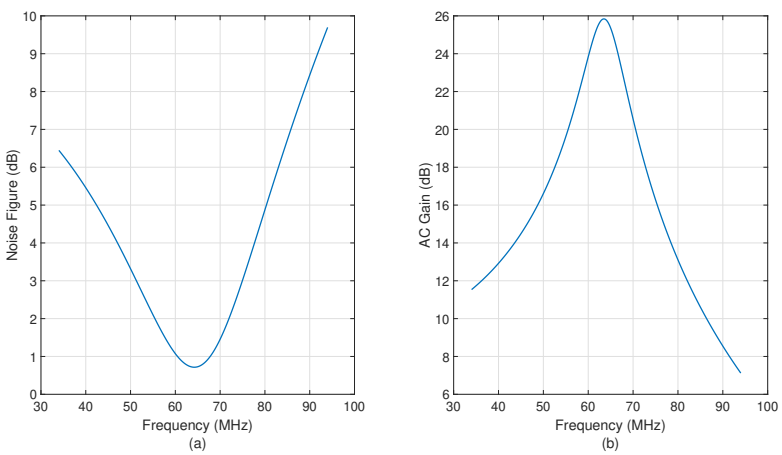

Figure 4.12. Low noise amplifier post-layout simulation results for (a)noise figure, (b)AC gain.

The comparison of pre-layout and post-layout simulation results is visualized in Figure 4.13 and tabulated in Table 4.1.

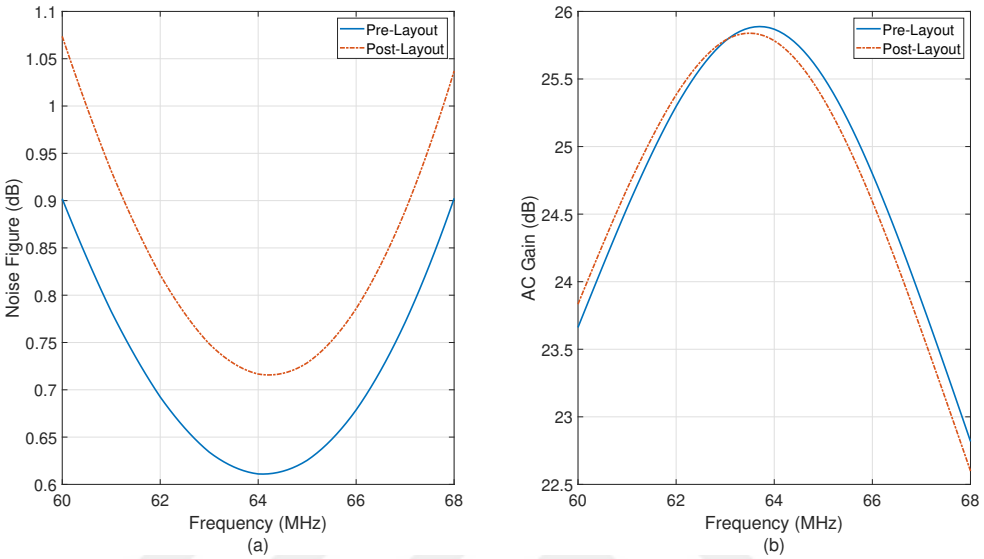

Figure 4.13. Comparison of schematic and post-layout simulation results for the LNA: (a) Noise figure, (b) AC gain.

Table 4.1. Table of schematic and post-layout simulation results for the low noise amplifier.

	Schematic Simulation	**Post-Layout Simulation**
Current Consumption	≈2mA at 0.9V	≈2mA at 0.9V
Noise Figure at 64 MHz	0.61 dB	0.71 dB
AC Gain at 64 MHz	25.8 dB	25.8 dB
Input Referred 1dB Compression Point	≈-32 dBm	≈-32 dBm

5. LOW VOLTAGE MIXER CIRCUIT

The mixer is a critical component in RF engineering. It is used in many applications such as communication engineering, microwave systems, and radar [32]. It is utilized in both transmitters and receivers. A mixer can also be referred to as an analog multiplier [19] because its primary function is to multiply two analog signals, typically producing output signals at the sum and difference of the input frequencies. To explain, two input cosine signals with different frequencies are represented as

$$\begin{aligned} v_1 &= A_1 \cos(2\pi f_1 t), \\ v_2 &= A_2 \cos(2\pi f_2 t). \end{aligned} \tag{5.1}$$

Multiplication of these signals results in two cosine signals, one with the sum of the frequencies and the other with the difference of the frequencies, expressed as

$$v_o = v_1 v_2 = \frac{A_1 A_2}{2} \left[\cos\left(2\pi\left(f_1 + f_2\right)t\right) + \cos\left(2\pi\left(f_1 - f_2\right)t\right)\right]. \tag{5.2}$$

This method effectively shifts the signal to a higher or lower band in the frequency domain. The cosine signal with the sum of the frequencies is called the upconverted signal, while the other signal with the difference of the frequencies is called the downconverted signal. Depending on the application, either the upconverted or downconverted signal can be utilized. This study focuses on downconverting the MRI signal from 64 MHz to 500 kHz, with noise suppression for efficient sampling by the ADC. To achieve this downconversion, the LO frequency is set to 64.5 MHz, as mentioned in Chapter 2. Please also note that, cubic and higher-order terms in the signal generate harmonics, specifically the odd harmonics in a fully differential topology. Suppressing the distortion caused by these harmonics is a critical design parameter.

5.1. Gilbert Mixer Cell

The Gilbert Mixer is one of the most common mixer topologies in RF circuits, first introduced in 1968 by Barrie Gilbert [33] as an improved version of the double-balanced four-quadrant analog multiplier invented by Howard Jones in the 1960s [34].

Figure 5.1 illustrates a generic topology of the Gilbert Mixer. The load resistor R_L may be replaced with an active load depending on the design.

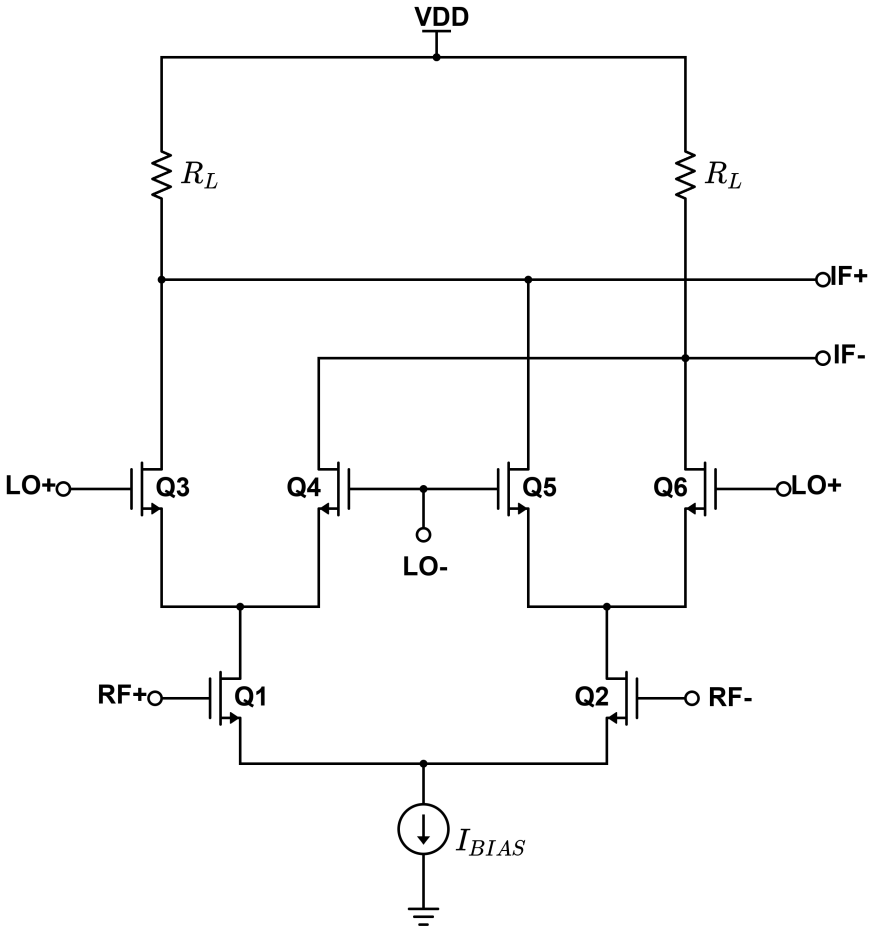

Figure 5.1. Gilbert mixer cell.

Transistors Q1 and Q2 form the transconductance stage, with the input signal applied to the RF+ and RF- pins of the stage. The Q3-Q6 transistors comprise the switching stage, driven by the Local Oscillator (LO) signal. The RF and LO signals are multiplied and the output is obtained through the Intermediate Frequency (IF+ and IF-) pins. Assuming the transistors are matched, the downconversion gain of the Gilbert mixer cell is roughly calculated as

$$A_{CG} = g_{m_1} R_o \tag{5.3}$$

where A_{CG} is the conversion gain, g_{m_1} is the transconductance of the Q1 and Q2. R_o is the equivalent output resistance. It can be approximated as R_L if the switching MOS-

FETs have high output impedance. Variations of the double-balanced mixer circuits are mostly based on this topology.

The challenge with the Gilbert Mixer is that to achieve sufficient performance, the supply voltage needs to be high. Since this thesis targets a 0.9V supply, an alternative design approach is necessary for the mixer. There are multiple approaches to designing a mixer at low voltage [35] such as folded design [36,37], current bleeding [38], operating the transistors at subthreshold region, [39], or bulk-injection [40].

5.2. Folded Mixer

A PMOS input folded mixer design is illustrated in Figure 5.2. Due to its folded structure, it provides wider voltage swing. Passive loads are used for achieving higher linearity. The transconductance stage, composed of PMOS transistors Q1 and Q2 with a size of $200\mu m/500nm$ is biased in saturation. NMOS transistors Q3-Q6 ($25\mu m/500nm$), are operated just below the threshold for rapid switching. The tail current transistor, Q7 ($400\mu m/500nm$) establishes the bias current. Resistors R_1 and R_2 are set to 754Ω and $2.55k\Omega$, respectively. The circuit consumes approximately 1 mA from a 0.9V supply.

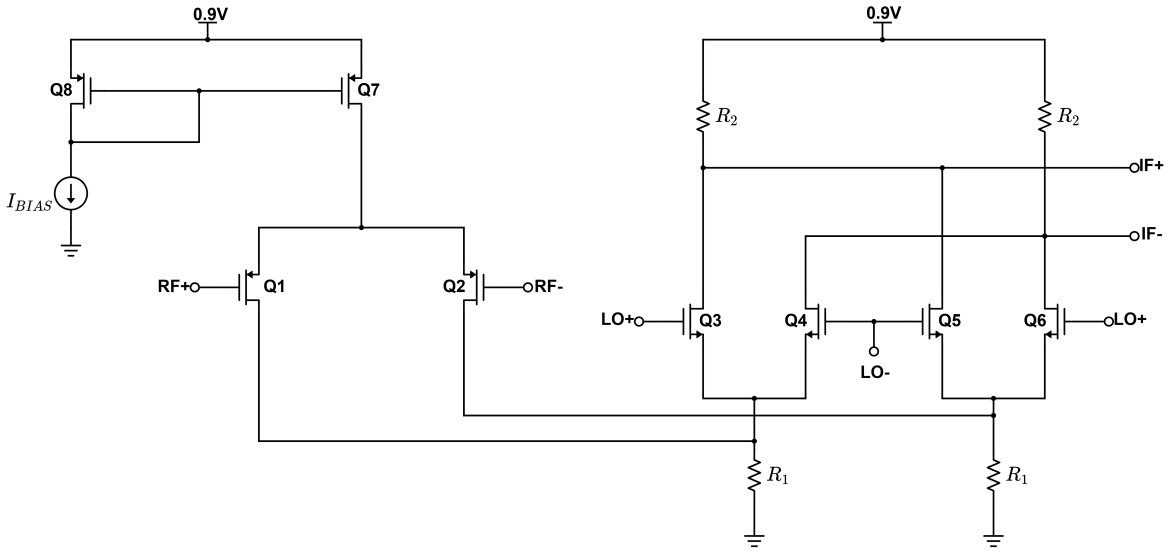

Figure 5.2. Folded mixer schematic.

Figure 5.3 illustrates the DC transfer characteristics of the folded mixer, showing symmetric operation in all four quadrants. The layout design of the mixer is shown in Figure 5.5. To avoid any mismatch, components and routes are placed symmetrically.

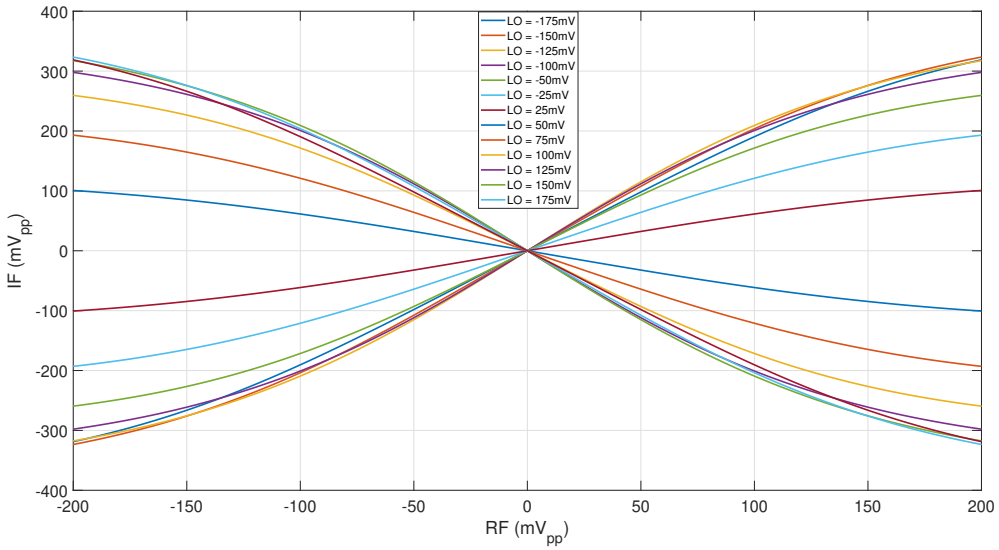

Figure 5.3. DC transfer characteristic of the folded mixer.

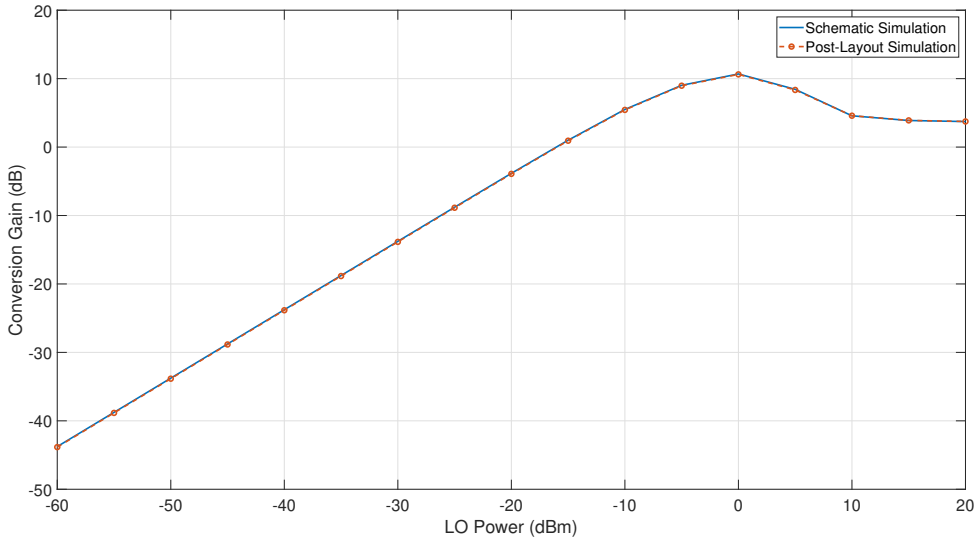

Figure 5.4. LO power vs conversion gain of the folded mixer.

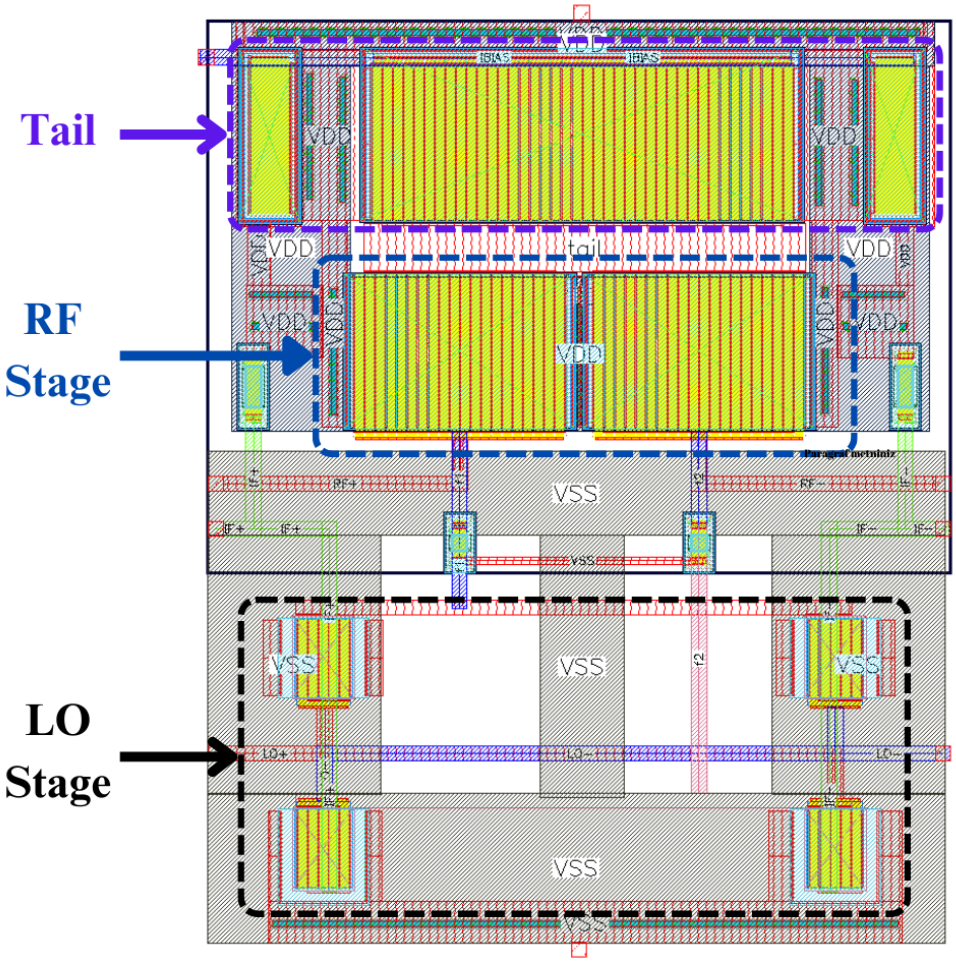

Figure 5.5. Folded mixer layout.

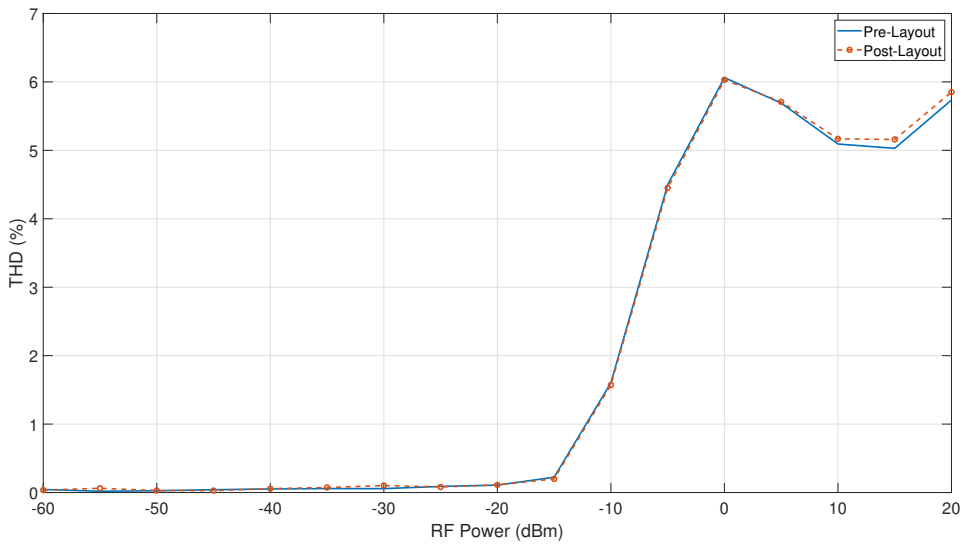

Figure 5.6. Total harmonic distortion of the folded mixer.

According to the LO Power versus Conversion Gain plot shown in Figure 5.4, a sinusoidal signal with an amplitude of $300mV_{peak}$ is applied to the LO ports differentially. The overall results are listed in Table 5.1.

Table 5.1. Table of schematic and post-layout simulation results for the folded mixer.

	Schematic Simulation	**Post-Layout Simulation**
Current Consumption	≈1mA @ 0.9V	≈1mA @ 0.9V
DSB Noise Figure	12.27 dB	13.31 dB
Conversion Gain	10.6 dB	10.6 dB
Input Referred 1dB Compression Point	-13.41 dBm	-13.38 dBm
Third Order Input Intercept Point (IIP3)	1.78 dBm	1.82 dBm

6. SIMULATION RESULTS OF ENTIRE SYSTEM

In the overall design, a 50Ω source is connected to the low noise amplifier through an LC matching network. The LNA amplifies the 64 MHz input signal. Subsequently, the folded mixer downconverts the amplified signal to a 500kHz IF using local oscillator. The process is illustrated in Figure 6.1. The overall system achieves a total gain of 36 dB and a noise figure below 1 dB, as shown in Figure 6.2.

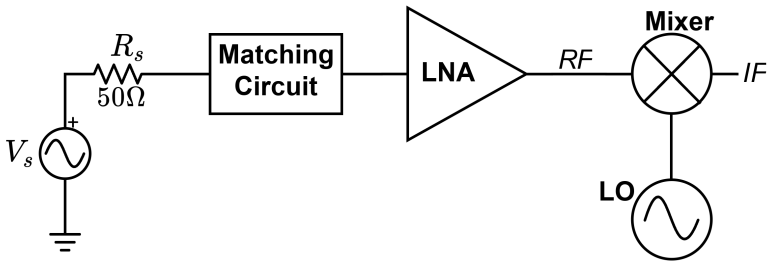

Figure 6.1. Block diagram of the designed circuit.

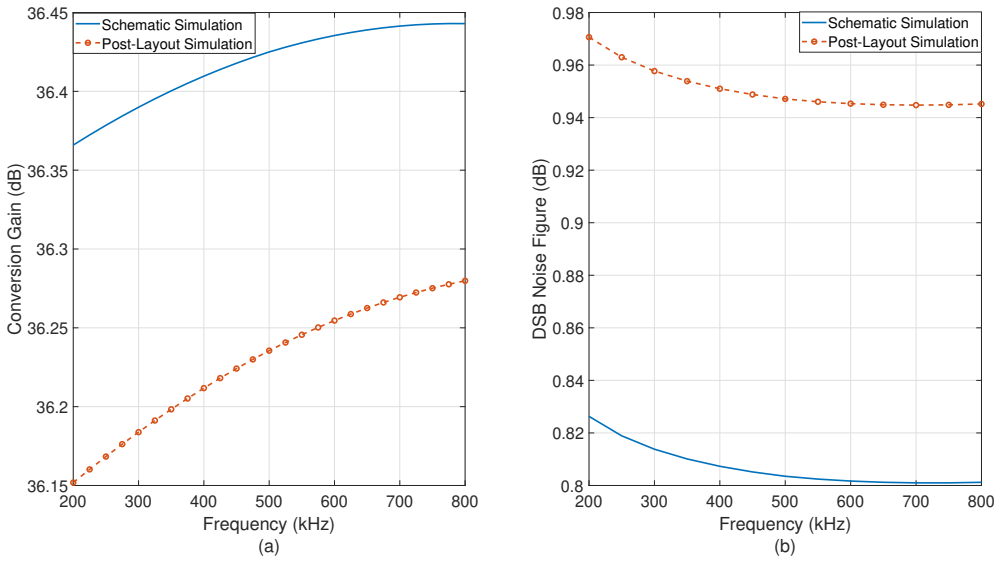

Figure 6.2. Schematic and post-layout simulation results of the entire system for (a)conversion gain, (b)double-sideband (DSB) noise figure.

Table 6.1. Table of schematic and post-layout simulation results for the entire system.

	Schematic Simulation	**Post-Layout Simulation**
Current Consumption	≈3mA @ 0.9V	≈3mA @ 0.9V
DSB Noise Figure	0.81 dB	0.95 dB
Conversion Gain	36.4 dB	36.2 dB
Input Referred 1dB Compression Point	-44.8 dBm	-44.7 dBm
Third Order Input Intercept Point (IIP3)	-30 dBm	-30 dBm

Simulation results are listed in Table 6.1. The overall system consumes around 2.7mW. A noise figure value below 1 dB is achieved. Input referred 1 dB compression point is around -45 dBm.

7. CONCLUSION

In summary, this thesis presents the schematic design and layout of a CMOS low noise amplifier and a folded mixer for an MRI receiver system operating at a supply voltage of 0.9 V, with the ultimate goal of powering the system through an on-chip CMOS photodiode. The noise equations for the LNA were derived, and the LNA was noise-matched with an MRI coil, which is assumed to have a 50Ω impedance. The LNA achieved a voltage gain of 26 dB with the matching network, and the post-layout simulation yielded a noise figure of approximately 0.7 dB. The folded mixer, connected to the LNA, exhibited a conversion gain of 10.6 dB. The overall system maintained a noise figure below 1 dB. However, achieving a lower noise figure may be possible with further optimization. Both the LNA and mixer designs involve a complex tradeoff between power consumption, gain, noise figure, and linearity. Given the limited power generated by the photodiode, power consumption was minimized. The lowest supply voltage achieved in the design was 0.9V, which provided sufficient headroom for biasing the transistors but limited the voltage swing due to the constrained voltage budget. Additionally, gain can positively or negatively impact the voltage swing, linearity, noise figure, and dynamic range. To operate within a wide dynamic range with a low noise figure, the gain must be set at an optimal level. Balancing these trade-offs poses significant design challenges. This thesis provides insights into the specifications for the low noise amplifier and folded mixer. The study also aims to demonstrate the effect of each design parameter on the overall system performance, with a particular focus on analyzing the noise performance of the low noise amplifier. The motivation behind this is to enable quick adjustments to design parameters for future designs and optimizations based on evolving requirements. By balancing these specifications, an optimal performance point can be achieved according to the specific needs of the application.

REFERENCES

1. Gruber, B., M. Froeling, T. Leiner and D. W. Klomp, "RF coils: A Practical Guide For Nonphysicists", *Journal of Magnetic Resonance Imaging*, Vol. 48, No. 3, pp. 590–604, 2018.

2. Sun, N., T.-J. Yoon, H. Lee, W. Andress, R. Weissleder and D. Ham, "Palm NMR and 1-Chip NMR", *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 1, pp. 342–352, 2011.

3. Kwok, W. E., "Basic Principles of and Practical Guide to Clinical MRI Radiofrequency Coils", *RadioGraphics*, Vol. 42, No. 3, pp. 898–918, 2022.

4. Gupta, M., C. P. Safvan, K. Singh, D. K. Lobiyal, P. Yadav and S. Singh, "Radio Frequency Planar Coil-Based On-Chip Probe for Portable Nuclear Magnetic Resonance", *IEEE Sensors Journal*, Vol. 19, No. 7, pp. 2500–2508, 2019.

5. Anders, J. and G. Boero, "A Low-Noise CMOS Receiver Frontend for MRI", *IEEE Biomedical Circuits and Systems Conference*, Baltimore, MD, pp. 165-168, 2008.

6. Kruger, D., A. Zhang, H. Hinton, V. M. Arnal, Y.-Q. Song, Y. Tang, K.-M. Lei, J. Anders and D. Ham, "A Portable CMOS-based MRI System with 67×67×83 μm^3 Image Resolution", *IEEE 48th European Solid State Circuits Conference*, Milan, Italy, pp. 225-228, 2022.

7. Sporrer, B., L. Bettini, C. Vogt, A. Mehmann, J. Reber, J. Marjanovic, D. O. Brunner, T. Burger, K. P. Pruessmann, G. Tröster and Q. Huang, "Integrated CMOS receiver for Wearable Coil Arrays in MRI Applications", *Design, Automation & Test in Europe Conference & Exhibition*, Dresden, Germany, pp. 1689-1694, 2015.

8. Sarıoğlu, Baykal, *CMOS Based Optoelectronic Catheter Localization System for*

Magnetic Resonance Imaging Environment, Ph.D. Thesis, Bogazici University, 2013.

9. Sporrer, B., L. Wu, L. Bettini, C. Vogt, J. Reber, J. Marjanovic, T. Burger, D. O. Brunner, K. P. Pruessmann, G. Tröster and Q. Huang, "A Fully Integrated Dual-Channel On-Coil CMOS Receiver for Array Coils in 1.5–10.5 T MRI", *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 11, No. 6, pp. 1245–1255, 2017.

10. Ridgway, J. P., "Cardiovascular Magnetic Resonance Physics for Clinicians: Part I", *Journal of Cardiovascular Magnetic Resonance*, Vol. 12, No. 1, p. 71, 2010.

11. Aktan, Ozan, *The design Aspects of an Optically Powered CMOS receiver Front-End for Electrically Isolated Applications*, Ph.D. Thesis, Bogazici University, 2011.

12. Razavi, B., *RF Microelectronics*, 2nd Edition, Prentice Hall Press, New Jersey, 2011.

13. Sarioglu, B., O. Aktan, A. Oncu, S. Mutlu, G. Dundar and A. D. Yalcinkaya, "An Optically Powered CMOS Receiver System for Intravascular Magnetic Resonance Applications", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2, No. 4, pp. 683–691, 2012.

14. Madrenas, J., J. M. Sánchez-Chiva, D. Fernández and J. Cosp, "Design Considerations for Analog LCMOS Harvest-Use Integrated Signal Processing", *IEEE International Symposium on Circuits and Systems*, Kuala Lumpur, Malaysia, pp. 1-5, 2019.

15. Maloberti, F., *Data Converters Specifications*, Springer, New York, 2007.

16. Blakiewicz, G., "Low-Voltage LDO Regulator Based on Native MOS Transistor with Improved PSR and Fast Response", *Energies*, Vol. 16, No. 12, 2023.

17. Liu, W. and C. Hu, *BSIM4 and MOSFET Modeling For IC Simulation*, World

Scientific, Singapore, 2011.

18. Der Ziel, A. V., "Thermal Noise in Field-Effect Transistors", *Proceedings of the IRE*, Vol. 50, No. 8, pp. 1808–1812, 1962.

19. Gray, P. R., P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition John Wiley, Chichester, 2010.

20. Razavi, B., *Design of Analog CMOS Integrated Circuits*, 1st Edition, McGraw-Hill, Inc., Boston, MA, 2001.

21. Fleetwood, D. M., "Total-Ionizing-Dose Effects, Border Traps, and 1/f Noise in Emerging MOS Technologies", *IEEE Transactions on Nuclear Science*, Vol. 67, No. 7, pp. 1216–1240, 2020.

22. Re, V., L. Gaioni, M. Manghisoni, L. Ratti and G. Traversi, "Comprehensive Study of Total Ionizing Dose Damage Mechanisms and Their Effects on Noise Sources in a 90 nm CMOS Technology", *IEEE Transactions on Nuclear Science*, Vol. 55, No. 6, pp. 3272–3279, 2008.

23. Newell, D. and E. Tiesinga, *"The International System of Units (SI)"*, 2019, `https://api.semanticscholar.org/CorpusID:242934226`, accessed on July 20, 2024.

24. Sedra, A. S. and K. C. Smith, *Microelectronic Circuits*, 7th Edition, Oxford University Press, Cary, NC, 2014.

25. Sun, N., Y. Liu, H. Lee, R. Weissleder and D. Ham, "CMOS RF Biosensor Utilizing Nuclear Magnetic Resonance", *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 5, pp. 1629–1643, 2009.

26. Figueiredo, M., R. Santos-Tavares, E. Santin, J. Ferreira, G. Evans and J. Goes, "A Two-Stage Fully Differential Inverter-Based Self-Biased CMOS Amplifier With

High Efficiency", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 58, No. 7, pp. 1591–1603, 2011.

27. Smit, G. D. J., A. J. Scholten, R. M. T. Pijper, L. F. Tiemeijer, R. van der Toorn and D. B. M. Klaassen, "RF-Noise Modeling in Advanced CMOS Technologies", *IEEE Transactions on Electron Devices*, Vol. 61, No. 2, pp. 245–254, 2014.

28. Coilcraft, *"Square Air Core Inductors"*, 2024, `https://www.coilcraft.com/en-us/products/rf/air-core-inductors`, accessed on June 25, 2024.

29. Gray, P. and R. Meyer, "MOS Operational Amplifier Design-A Tutorial Overview", *IEEE Journal of Solid-State Circuits*, Vol. 17, No. 6, pp. 969–982, 1982.

30. Sharma, A. K., M. Madhusudan, S. M. Burns, P. Mukherjee, S. Yaldiz, R. Harjani and S. S. Sapatnekar, "Common-Centroid Layouts for Analog Circuits: Advantages and Limitations", *Design, Automation & Test in Europe Conference & Exhibition*, Grenoble, France, pp. 1224-1229, 2021.

31. Hastings, R., *The Art of Analog Layout*, Prentice Hall, Upper Saddle River, NJ, 2001.

32. Zhang, H., S. Tang, M. Cai and Y. Jiang, "Optimal Design of CMOS Mixer: A Research Review", *International Journal of RF and Microwave Computer-Aided Engineering*, Vol. 32, No. 12, p. 23531, 2022.

33. Gilbert, B., "A New Wide-Band Amplifier Technique", *IEEE Journal of Solid-State Circuits*, Vol. 3, No. 4, pp. 353–365, 1968.

34. Hong, B. and A. Hajimiri, "Analysis of a Balanced Analog Multiplier for An Arbitrary Number of Signed Inputs", *International Journal of Circuit Theory and Applications*, Vol. 45, No. 4, pp. 483–501, 2017.

35. Sulivan, P., B. Xavier and W. Ku, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 7, pp. 1151–1155, 1997.

36. Hampel, S., O. Schmitz, M. Tiebout and I. Rolfes, "Low-voltage, Inductorless Folded Down-Conversion Mixer in 65nm CMOS for UWB Applications", *IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA, USA, pp. 119-122, 2009.

37. Dan, S. and Z. Xiaolin, "Low-voltage CMOS Folded-cascode Mixer", *Chinese Journal of Aeronautics*, Vol. 23, No. 2, pp. 198–203, 2010.

38. Sravanthi, P. and A. Chandra, "Current-bleeding Folded Gilbert RF Mixer Design For Wireless Applications", *IEEE Conference on Information & Communication Technologies*, Thuckalay, India, pp. 1044-1048, 2013.

39. Seo, J.-B., J.-H. Kim, H. Sun and T.-Y. Yun, "A Low-Power and High-Gain Mixer for UWB Systems", *IEEE Microwave and Wireless Components Letters*, Vol. 18, No. 12, pp. 803–805, 2008.

40. Liang, K.-H., H.-Y. Chang and Y.-J. Chan, "A 0.5–7.5 GHz Ultra Low-Voltage Low-Power Mixer Using Bulk-Injection Method by 0.18- μm CMOS Technology", *IEEE Microwave and Wireless Components Letters*, Vol. 17, No. 7, pp. 531–533, 2007.

41. Binkley, D., *Tradeoffs and Optimization in Analog CMOS Design*, Wiley, New York, NY, 2008.