DESIGN AND DEVELOPMENT OF HALL SENSORS FOR MAGNETIC MICROSYSTEMS

by

Nazanin Takbiri

B.S., Electrical Engineering, University of Tehran, 2012

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Master of Science

Graduate Program in Electrical and Electronics Engineering
Boğaziçi University

2015

DESIGN AND DEVELOPMENT OF HALL SENSORS FOR MAGNETIC MICROSYSTEMS

APPROVED BY:

Assist. Prof. Hamdi Torun (Thesis Supervisor)	.....
Prof. Günhan Dündar	.....
Assist. Prof. Onur Ferhanoğlu	.....

DATE OF APPROVAL: 20.08.2015

ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere gratitude to my advisor Prof. Hamdi Torun for the continuous support of my Ph.D study and related research, for his patience, motivation, and immense knowledge.

I would also like to thank Prof. Günhan Dündar for his illuminating guidance and his broad experience that helped me in all the time of research and writing of this thesis.

Besides my advisor, I would like to thank my family: my parents and to my husband, Ali, for supporting me spiritually throughout writing this thesis and my life in general.

ABSTRACT

DESIGN AND DEVELOPMENT OF HALL SENSORS FOR MAGNETIC MICROSYSTEMS

Nowadays, magnetic sensors are widely used in variety of applications. One of the most common classes of magnetic sensors is Hall effect based sensors. Improving characteristics of Hall effect based sensors, such as sensitivity, resolution, power consumption, and chip area has always been a center of attention for many researchers. In this work, a Hall sensor is designed in $0.13\,\mu m$ CMOS technology. Two cross-shaped Hall plates are used to increase sensitivity and to cancel the DC offset output of Hall plates. To provide input current for the Hall plates, a biasing circuit is designed. Using a common mode feedback network, consistency of the input current is ensured. To automatically ignore the process variations, which causes asymmetric output from different Hall plate ports, the current spinning method is used. 32 switches are connected to input-output ports of the Hall plates to rotate their connections functionality and compensate the probable defects after fabrication. A digital circuit is designed to generate 4 non-overlapping clock signals to control the switches. In order to increase signal to noise ratio, the signal is converted from current to voltage mode using a capacitor and then amplified using two fully differential amplifiers. The capacitor is discharged every complete cycle to ensure linear functionality. Layouts of different blocks used in the project are designed and pre-layout and post-layout simulation results are gathered and presented. Simulation results show sensitivity of 8383 $\frac{V}{A.mT}$ and power consumption of 36 μW, while using 3 μA as input bias current, 1.8 V as supply voltage, and consuming 6259 μm^2 of chip area.

ÖZET

MANYETİK MİKROSİSTEMLER İÇİN KORİDOR ALGILAYICI TASARIMI VE GELİŞTİRİLMESİ

Günümüzde manyetik algılayıcılar bir çok alanda kullanılmaktadır. Manyetik algılayıcıların en yaygın türlerinden biri koridor etkisi tabanlı algılayıcı. Koridor etkisi tabanlı algılayıcıların hassasiyet, çözünürlük, enerji tüketimi ve yonga alanı gibi karakteristik özelliklerinin geliştirilmesi her zaman araştırmacıların ilgi alanındadır. Bu çalışmada, $0.13\,\mu m$ CMOS teknolojinde koridor algılayıcı tasarlanmıştır. İki tane çapraz-şekilli koridor plaka hassasiyeti arttırmak ve koridor plakaların doğru akım ofset çıkışı iptal etmek için kullanılmıştır. Koridor plakalara girdi akımı sağlamak için, kutuplama devresi tasarlanmıştır. Ortak modlu geri dönüşüm ağı kullanılarak girdi akımının tutarlılığı sağlanmıştır. Farklı koridor plaka portlarından simetrik olmayan çıktılara sebep olan işlem değişimlerini otomatik olarak engellemek için akım dönme metodu kullanılmıştır. Koridor plakaların bağlantı işlevlerini çevirebilmek ve olası üretim sonrası hataları engellemek için 32 tane düğme koridor plakaların giriş ve çıkış portlarına bağlanmıştır. Düğmeleri kontrol etmek için 4 tane kesişmeyen saat işareti üretecek sayısal devre tasarlanmıştır. Sinyal, sinyal-gürültü oranını arttırmak için, kapasitör kullanılarak akımdan voltaj moduna dönüştürülür ve sonrasında iki tane farksal yükseltici kullanılarak yükseltilir. Kapasitör, doğrusal işlevselliği sağlamak için her tam tur sonunda boşaltılır. Projede kullanılan farklı blok şemaları tasarlanmıştır ve şema-öncesi ve şema-sonrası benzetim sonuçları elde edilip sunulmuşturr. $3\ \mu A$ sapma akımı, $1.8\ V$ besleme voltajı kullanan ve $6259\ \mu m^2$ yonga alanı kaplayan benzetim sonuçlarında $8383\ \frac{V}{A.mT}$ hassasiyeti ve $36\ \mu W$ güç tüketimi gözlenmiştir.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS . . . iii
ABSTRACT . . . iv
ÖZET . . . v
LIST OF FIGURES . . . viii
LIST OF TABLES . . . xiii
LIST OF SYMBOLS . . . xiv
LIST OF ACRONYMS/ABBREVIATIONS . . . xvi
1. INTRODUCTION . . . 1
1.1. Hall Effect Based Sensors . . . 2
1.1.1. Hall Effect . . . 3
1.1.2. Hall Plate . . . 5
1.1.2.1. Geometry of a Hall Plate . . . 5
1.1.2.2. Operation Mode . . . 7
1.2. Thesis Outline . . . 11
2. SYSTEM DESIGN . . . 12
2.1. Hall Plate . . . 12
2.1.1. Hall Plate Model . . . 14
2.2. Current Spinning Circuit . . . 15
2.2.1. Switching Clock Generator Circuit . . . 16
2.2.1.1. Frequency Divider . . . 16
2.2.1.2. Clock Generator . . . 20
2.2.1.3. Buffer . . . 20
2.3. Current Biasing Circuit . . . 22
2.3.1. Low Voltage Current Mirror . . . 22
2.3.2. Common Mode Feedback Circuit . . . 24
2.4. Current to Voltage Converter . . . 25
2.5. Differential Voltage Amplifier . . . 26
2.5.1. First Stage Amplifier . . . 26

2.5.2. Second Stage Amplifier 27
3. Simulation Results 29
3.1. Hall Plate 29
3.2. Current Spinning Circuit 33
3.3. Current Biasing Circuit 37
3.4. Current to Voltage Converter 38
3.5. Differential Voltage Amplifier 38
3.6. Noise Simulation 40
3.6.1. Noise of Hall Plates 40
3.6.2. Noise of Electronic Circuitry 41
3.6.3. Total System's Noise 41
4. CONCLUSION 44
APPENDIX A: LAYOUTS 46
A.1. Hall Plates 46
A.2. Current Spinning Circuit 47
A.2.1. Switches 47
A.2.2. Clock Generator Circuit 47
A.3. Current Biasing Circuit 48
A.4. Current to Voltage Converter 48
A.5. Differential Voltage Amplifier 49
A.5.1. First Stage Amplifier 49
A.5.2. Second Stage Amplifier 49
A.6. Whole Proposed Circuit Surrounding Hall Plates 50
REFERENCES 51

LIST OF FIGURES

Figure 1.1. General sensor based on Hall effect. 3

Figure 1.2. Hall effect principle, no magnetic field. 4

Figure 1.3. Hall effect principle, magnetic field is present. 5

Figure 1.4. Rectangular Hall plate. 6

Figure 1.5. Diamond Hall plate. 6

Figure 1.6. Cross Hall plate. 7

Figure 1.7. Voltage-mode Hall sensor. 8

Figure 1.8. Current-mode Hall sensor. 9

Figure 2.1. Schematic of the circuit blocks surrounding the Hall plates. 12

Figure 2.2. A pair of current-mode Hall sensors structure. 13

Figure 2.3. Simplified model for CMOS integrated cross-shaped Hall plate. . . 14

Figure 2.4. Hall plates with switches configuration for current spinning. 17

Figure 2.5. Clock signals' diagram for current spinning operation. 18

Figure 2.6. Schematic of transmission gate used as a switch. 18

Figure 2.7. Schematic of a divide-by-2 frequency divider. 19

Figure 2.8. Desired result of a divide-by-2 frequency divider. 19

Figure 2.9. Clock 1. 20

Figure 2.10. Clock 2. 20

Figure 2.11. Clock 3. 21

Figure 2.12. Clock 4. 21

Figure 2.13. Schematic of buffer circuit. 21

Figure 2.14. Effect of using buffers on switching. 22

Figure 2.15. Schematic of current biasing circuit. 25

Figure 2.16. Current to voltage converter circuit. 26

Figure 2.17. First stage differential voltage amplifier. 27

Figure 2.18. Second stage differential voltage amplifier. 28

Figure 3.1. FEM simulation of a current-mode Hall plate when bias current is equal to $3\,\mu A$. 30

Figure 3.2. FEM simulation result of a current-mode Hall plate when bias current is equal to $3\,\mu A$. 30

Figure 3.3. FEM simulation of two current-mode Hall plates structure when bias currents are equal to $3\,\mu A$ and $-3\,\mu A$. 31

Figure 3.4. FEMl simulation result of two current-mode Hall plates structure when bias currents are equal to $3\,\mu A$ and $-3\,\mu A$. 32

Figure 3.5. Result of Hall sensor's model when bias current is equal to $3\,\mu A$. . 32

Figure 3.6. Result of a pair of Hall sensors' model when two Hall plates are used and bias currents are equal to $3\,\mu A$ and $-3\,\mu A$. 33

Figure 3.7. Pre-layout simulation result of the divide-by-2 frequency divider. . 34

Figure 3.8. Post-layout simulation result of the divide-by-2 frequency divider. 34

Figure 3.9. Pre-layout simulation result of complete switching clock generator circuit. 35

Figure 3.10. Post-layout simulation result of complete switching clock generator circuit. 35

Figure 3.11. Pre-layout simulation result of Hall plates connected to current spinning block. 36

Figure 3.12. Post-layout simulation result of Hall plates connected to current spinning block. 36

Figure 3.13. Pre-layout simulation result of Hall plates biased using current biasing circuit and connected to current spinning block. 37

Figure 3.14. Post-layout simulation result of Hall plates biased using current biasing circuit and connected to current spinning block. 37

Figure 3.15. Pre-layout simulation result of current to voltage converter. 38

Figure 3.16. Post-layout simulation result of current to voltage converter. . . . 39

Figure 3.17. Pre-layout simulation result of whole proposed circuit. 39

Figure 3.18. Post-layout simulation result of whole proposed circuit. 40

Figure 3.19. Density spectrum of noise of whole electronic circuitry. 41

Figure 3.20. Density spectrum of total output noise. 42

Figure 3.21. Spectrum of square $V_{n(rms)}$. 42

Figure A.1. Layout of two Hall plates. 46

Figure A.2. Layout of 32 switches connected together. 47

Figure A.3. Layout of complete switching clock generator circuit. 47

Figure A.4. Layout of current biasing circuit. 48

Figure A.5. Layout of current to voltage converter circuit. 48

Figure A.6. Layout of first stage amplifier. 49

Figure A.7. Layout of second stage amplifier. 49

Figure A.8. Layout of circuit blocks surrounding Hall plates. 50

LIST OF TABLES

Table 2.1. Hall plates' connections on each phase. 16

Table 3.1. Model parameters. 29

Table 4.1. Performance summary and comparison table of this work with recently published CMOS Hall sensors. 44

LIST OF SYMBOLS

A	Cross sectional area
B	Magnetic field
B_{z}	Magnetic field along z-direction
C	Capacitor
C_{ox}	Gate oxide capacitance per unit area
dI	An infinitesimal change in current
dt	An infinitesimal change in time
E_{y}	Electrical field along z-direction
f_{in}	Input frequency
f_{out}	Output frequency
$f_{\mathrm{Reseting\ switch}}$	Capacitor reseting switch frequency
$f_{\mathrm{Switching\ clock}}$	Switching clock frequency
g_{m}	Transconductance of each transistor
G_{m}	Transconductance of input network
I_{Bias}	Bias current
I_{D}	Drain current of a transistor
$I_{\mathrm{H-}}$	Negative output current of a current-mode Hall plate
$I_{\mathrm{H+}}$	Positive output current of a current-mode Hall plate
I_{Hall}	Current Hall
I_{HN}	Negative output current of two current-mode Hall plates
I_{Hp}	Positive output current of two current-mode Hall plates
I_{x}	Current along x-direction
K	Boltzmann's constant
L	Length
m	An integer
n	Carrier density
q	Electrical charge
R	Resistance

r_{H}	Hall coefficient
r_{OUT}	Output Resistance of each transistor
R_{OUT}	Output Resistance of output network
S	Sensitivity
S_{I}	Current-mode sensitivity
$S_{\mathrm{V_I}}$	Current-related voltage-mode sensitivity
t	Thickness
T	Temperature
V_{A}	Early voltage
V_{Bias}	Bias voltage
V_{G}	Gate voltage of a transistor
$V_{\mathrm{H-}}$	Negative output voltage of a voltage-mode Hall plate
$V_{\mathrm{H+}}$	Positive output voltage of a voltage-mode Hall plate
V_{Hall}	Hall voltage
V_{IN}	Input voltage
V_{n}	Noise density
$V_{\mathrm{n_{1/f}}}$	Flicker noise
$V_{\mathrm{n_{Thermal}}}$	Thermal noise
V_{OUT}	Output voltage
V_{ov}	Over-drive voltage
W	Width
μ_{H}	Hall mobility
υ_{x}	Velocity of charge along x-direction
ΔB	Total change in magnetic field
ΔI	Total change in current
ΔV	Total change in voltage

LIST OF ACRONYMS/ABBREVIATIONS

2D	Two Dimensional
AMR	Anisotropic MagnetoResistance
BW	BandWidth
CMFB	Common Mode Feed-Back
CMOS	Complementary Metal–Oxide–Semiconductor (technology)
CMRR	Common Mode Rejection Ratio
DC	Direct Current
FEM	Finite-Element Method
GMR	Giant MagnetorResistance
HP	Hall Plate
IC	Integrated Circuit
LPF	Low-Pass Filter
MEMS	MicroElectroMechanical Systems
MOS	Metal-Oxide Semiconductor
NEMS	NanoElectroMechanical Systems
NMOS	N-channel Metal-Oxide Semiconductor
PMOS	P-channel Metal-Oxide Semiconductor
RMS	Real Mean Square
SNR	Signal to Noise Ratio
VCM	Voltage Common Mode

1. INTRODUCTION

Fabrication process and industrial machinery to fabricate integrated circuits (IC) have been developed to a level where electronic engineers are now able to design and fabricate miniaturized circuits and systems. The most important factor for this improvement is based on electronic and mechanical characteristics of silicon. Combining these two important features of silicon, scientists were able to fabricate microelectromechanical systems (MEMS). MEMS technology enables realization of electro-mechanical systems in micrometer, or even nanometer scale, which is also known as nanoelectromechanical Systems (NEMS).

Different types of MEMS devices have been demonstrated for applications ranging from magnetic micro systems [1], pressure sensing [2] to biomedical applications [3]. Microfabrication technology allows us to design the mechanical micro structures before, during, and after complementary metal–oxide–semiconductor (CMOS) production, pre-CMOS, intermediate-CMOS, and post-CMOS respectively. Using the fact that CMOS technology and MEMS are compatible and can be integrated on a single chip, several kinds of sensors and actuators can be designed and fabricated [4].

Microsensors detect and quantify certain physical, chemical, or biological quantities, such as temperature, pressure, force, humidity, light, nuclear radiation, magnetic flux, and chemical composition [5]. An important advantage of microsensors is that they sense very small changes in the quantity accurately [6]. One of the most important types of microsensors is magnetic sensors.

Magnetic sensors have been in use for well over 2000 years. They are devices that measure the magnetic field in a medium. Magnetic sensors can be designed based on different concepts such as Magnetostrictive effect, giant magnetoresistance (GMR), anisotropic magnetoresistive (AMR), and Hall effect.

- Magnetostrictive sensors [7,8]: Magnetostrictive sensors use the concept of mag-

netostrictive effect. According to this phenomenon, changing magnetization of a magnetostrictive material results in changing its strain which it is exhibit in length per unit length.

- AMR based sensors [9,10]: Anisotropic magnetoresistance effect can also be used to sense a magnetic field and the angle between magnetization direction and an electrical current. According to this effect, the resistance of a ferromagnetic material changes with regard to the magnetic field around it. Its resistance will be minimum when the magnetization direction is perpendicular to the direction of electrical current.
- GMR based sensors [11,12]: GMR based sensors use the concept of giant magnetoresistance. GMR is a quantum mechanical magnetoresistance effect that can be observed in metallic multilayer structures where magnetic layers are separated by non-magnetic layers. The magnetic layers can be rotated in the presence of an external magnetic field which changes the resistance of the structure. Resistance is minimum when the the current flows in parallel with the layers.
- Hall effect based sensors: Hall structure is fabricated using a thin conductive material with contacts on edges to act as input and output ports. The voltage induced across the Hall plate is proportional to intensity of magnetic field. Considering possible dimensions for Hall plate, the induced voltage cannot reach a usable level to be used in electronics devices and needs amplifications and together they make a Hall effect sensor [13]. Hall plates, that act as sensors for Hall sensing device, can be integrated with CMOS technologies [14].

The sensor system presented in this thesis is based on Hall effect. So it is necessary to know the working principle of this kind of sensors.

1.1. Hall Effect Based Sensors

Figure 1.1 shows a block diagram of a sensing device that uses the Hall effect. Magnetic system generates a magnetic field which in turn is sensed by the Hall plates. The field generated by the magnetic system is related with the quantity that we are trying to sense such as current, temperature, pressure, and position. Electronic cir-

cuitry is placed in output interface where signal is converted to an acceptable electrical signal [13].

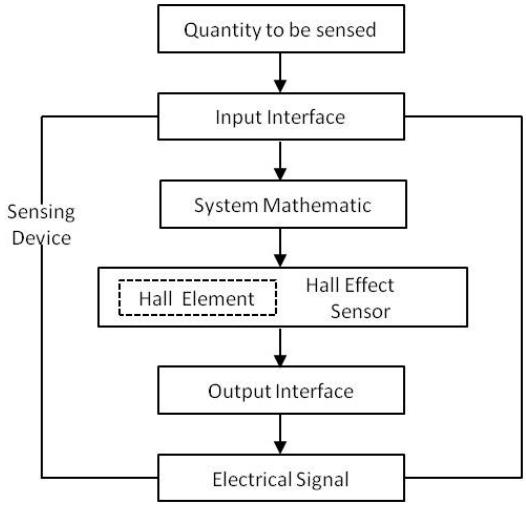


Figure 1.1. General sensor based on Hall effect [13].

1.1.1. Hall Effect

The Hall effect was discovered by Dr. Edwin Hall in 1879. He observed that when a magnet was placed so that its field was perpendicular to one face of a thin rectangle of gold through which current was flowing, a difference in potential appeared at the opposite edges. He found that this voltage was proportional to the current flowing through the conductor, and the flux density or magnetic induction perpendicular to the conductor [15].

Figure 1.2 illustrates the basic principle of the Hall effect. It shows a thin sheet of semiconducting material (Hall element) through which a current is passed along x-direction I_x. The output connections are perpendicular to the direction of current. When no magnetic field is present, current distribution is uniform and no potential difference is seen across the output.

When a perpendicular magnetic field is present along z-direction B_z, as shown in Figure 1.3, a Lorentz force is exerted on the current. This force disturbs the

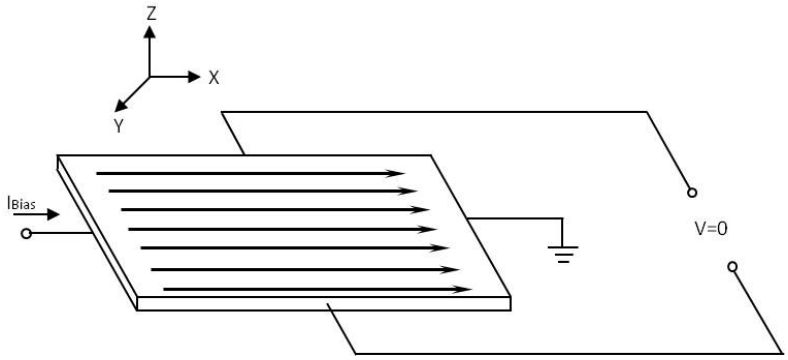


Figure 1.2. Hall effect principle, no magnetic field [13].

current distribution, resulting in a potential difference (voltage) across the output. This voltage is the Hall voltage (V_{Hall}) [16].

$$I_x = q \times n \times A \times \upsilon_x \tag{1.1}$$

$$q \times E_y = q \times \upsilon_x \times B_z \tag{1.2}$$

$$V_{Hall} = E_y \times W = \upsilon_x \times B_z \times d \tag{1.3}$$

$$V_{Hall} = \frac{I_x \times B_z}{q \times t \times n} \tag{1.4}$$

Hall sensitivity is equal to:

$$Sensitivity = \frac{\Delta V}{\Delta B} \tag{1.5}$$

From here, Hall coefficient (r_H) can be defined as:

$$r_H = \frac{1}{n \times q} \tag{1.6}$$

In the above equations, E_y is electrical field along y-direction, A is cross section area, υ_x is velocity of charge along x-direction, n is carrier density, q is electrical charge, t and W are thickness and width of Hall plate.

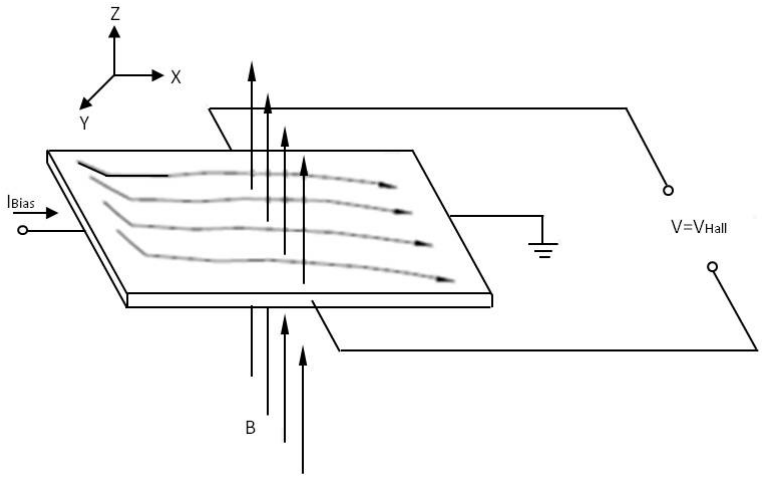


Figure 1.3. Hall effect principle, magnetic field is present [13].

1.1.2. Hall Plate

Hall plates are categorized in different groups according to their geometry and operation mode.

1.1.2.1. Geometry of a Hall Plate. Performance of a Hall plate heavily depends on its geometry. Modifying the geometry of a sensor can help adjusting the sensitivity, offset, and power consumption [16, 17]. The most common shapes for Hall plates are:

- Rectangular shape Hall plates [18]: Bias electrodes placed on width of a rectangular Hall plate and form a uniform current sheet. To determine the optimum dimension for the rectangle, output current can be considered for constant input voltage for different plate sizes. At first sight, it seems by increasing the length of the plate or making it narrower, more current can be obtained from induced voltage, thus we can increase the sensitivity. However, by making the plate long and short, its resistance will decrease to the point where the Hall voltage

is then short circuited and sensitivity is decreased. That is why using multiple Hall plates in parallel does not improve the sensitivity noticeably. The optimum length to width ratio for a Hall plate is reported as 1.35:1 [17]. A rectangular Hall plate is shown in Figure 1.4.

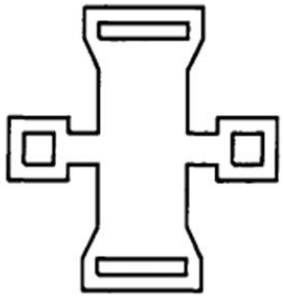


Figure 1.4. Rectangular Hall plate [17].

- Diamond shape Hall plates [19]: To avoid the terminal shorting, which is explained above, the plate can be designed in the shape of a diamond. Thus, current will spread thought the plate in a non-uniform manner. Because the current flow at the sense corners of the diamond is low, the voltage gradient in the corners also be low. So ohmic offset from contact misalignment effects is reduced [17]. A diamond Hall plate is shown in Figure 1.5 .

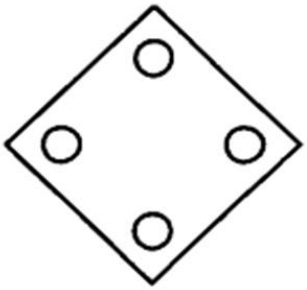


Figure 1.5. Diamond Hall plate [17].

- Cross shape Hall plates [20–23]: There are 4 contacts on each side of a cross shaped Hall plate. Two of the contacts are biased, either upper and lower ones or left and right ones. Magnetic field induces current inside the plate that is converted to an induced voltage, which can be sensed on two remaining contacts. Hall plates in a cross-shaped geometry are widely used, since they provide the best sensitivity while having least noise and residual effect. They are also immune

to alignment tolerance resulting from fabrication process. Direct current (DC) offset is a negative aspect of these sensors since it reduces the DC resolution of the sensor, however; taking benefit of the symmetrical shape of the cross-shaped Hall plate, current spinning method can be used. This method effectively reduces the DC offset as well as flicker noise [24–29]. A cross-shaped Hall plate is shown in Figure 1.6.

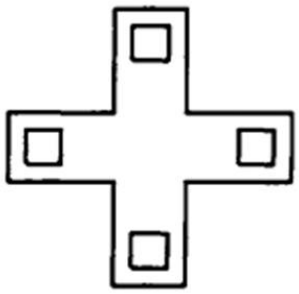


Figure 1.6. Cross Hall plate [17].

1.1.2.2. Operation Mode. Since Hall sensors convert magnetic field into an electrical signal, either voltage or current, the operation can be classified as voltage or current mode.

- Voltage-mode Hall plates: In voltage-mode Hall plates, the output is measured as induced voltage. The output voltage is typically in the order of micro- to millivolt and, therefore, it must be amplified before being transmitted to the outside world. In this mode, V_{Hall} is proportional to bias current applied to the sensor (I_{Bias}), the current-related voltage-mode sensitivity (S_{V_I}), and the applied perpendicular external magnetic field(B),

$$V_{Hall} = S_{V_I} \times I_{Bias} \times B \tag{1.7}$$

$$\begin{aligned} S_{V_I} &= \frac{V_{Hall}}{I_{Bias} \times B} \\ &= \frac{1}{n \times t \times q} \end{aligned} \tag{1.8}$$

$$V_{H+} = \frac{V_{Bias}}{2} + \frac{V_{Hall}}{2} \tag{1.9}$$

$$V_{H-} = \frac{V_{Bias}}{2} - \frac{V_{Hall}}{2} \tag{1.10}$$

V_{H+} and V_{H-} are positive and negative outputs voltage of a voltage-mode Hall plate, respectively.

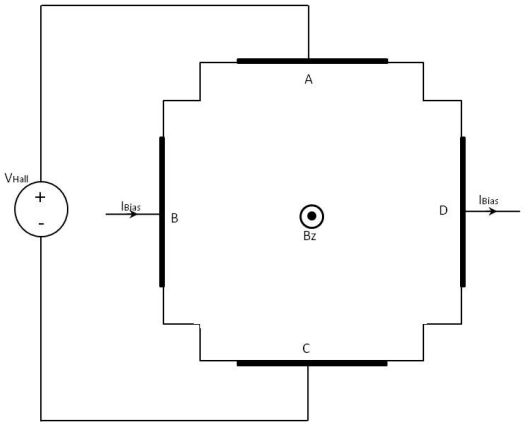


Figure 1.7. Voltage-mode Hall sensor.

- Current-mode Hall plates: The Hall plate is biased with current in this mode and the output is also obtained as current. The voltages at the 4 contacts will stay constant, theoretically, and as a result, there will be no influence of the parasitic capacitances. In addition, some of the terminals may share the current, which results in reducing the number of terminals, thus enabling further miniaturization of the design. In this mode of operation, the Hall current (I_{Hall}) is proportional to the bias current of the Hall plate (I_{Bias}), the current-mode sensitivity (S_I), and the applied perpendicular external magnetic field(B),

$$I_{Hall} = S_I \times I_{Bias} \times B \tag{1.11}$$

$$\begin{aligned} S_I &= \frac{I_{Hall}}{I_{Bias} \times B} \\ &= \mu_H \times (\frac{W}{L}) \end{aligned} \tag{1.12}$$

where μ_H is Hall mobility, W is width and L is length of Hall plate.

$$I_{H+} = \frac{I_{Bias}}{2} + \frac{I_{Hall}}{2} \tag{1.13}$$

$$I_{H-} = \frac{I_{Bias}}{2} - \frac{I_{Hall}}{2} \tag{1.14}$$

In the above equations, I_{H+} and I_{H-} are positive and negative outputs current of a current-mode Hall plate, respectively.

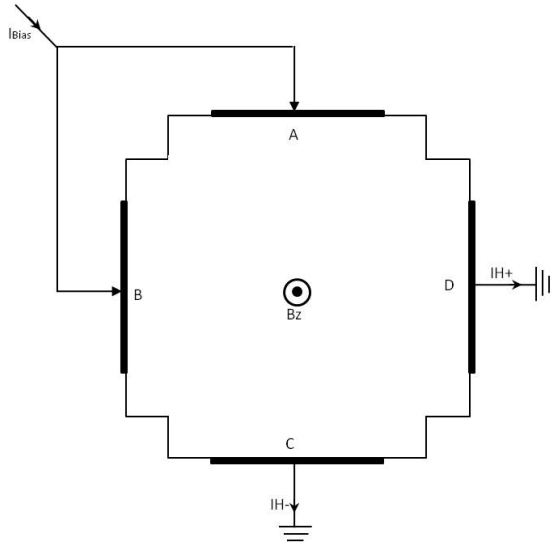


Figure 1.8. Current-mode Hall sensor.

A sensor designer should consider some characteristics of a Hall effect sensor. Some of these characteristics are listed below.

- Sensitivity: Sensitivity is the change in the output for a unit change in magnetic field (B). The effectiveness of Hall devices is measured by the sensitivity. For example, when sensitivity is higher, for a certain changes in input, the sensor provides greater output which reduces the need for supporting electronics circuitry.

$$Sensitivity = \frac{\Delta Output}{\Delta B} \tag{1.15}$$

- Input and output resistance: Input resistance of a Hall plate will determine the restrictions on biasing circuitry, however, output resistance can be used to design the follow-up amplifier stages. That is why knowing resistance of Hall plates is very important for designers.
- Noise: In addition to providing a signal, Hall effect sensors also present electrical noise at their outputs.The most fundamental and unavoidable of electrical noise sources is called Johnson noise, and it is the result of the thermally induced motion of electrons (or other charge carriers) in a conductive material. It is solely a function of the resistance of the device and the operating temperature. Johnson noise ($V_{n_{Thermal}}$)is generated by any resistance (including Hall plates), and is described by Equation 1.16. In this equation, T is temperature, BW is measurement bandwidth, R is series resistance and K is Boltzmann constant and is equal to $1.38 \times 10^{-23}\, K^{-1}$ [17].

$$V_{n_{Thermal}} = \sqrt{4 \times K \times T \times BW \times R} \tag{1.16}$$

  At lower frequencies, another source of noise begins to take dominance among others. Flicker ($1/f$) noise sometimes is more problematic than Johnson noise. Flicker noise ($V_{n_{1/f}}$)can be originated from many different sources and from various materials. However, the measurements show the inverse proportional relation between power of this noise with the frequency.

  The basic difference between Johnson noise and flicker noise is the fact that Johnson noise is intrinsic and exists in any resistance, however, the flicker noise depends on the materials and fabrication processes [17]. In this equation, $V_{n_{1/f}\,(rms)}$ is root-mean-squared of flicker noise.

$$V^2{}_{n_{1/f}\,(rms)} = \int_0^\infty V^2_{n_{1/f}}(f)df \tag{1.17}$$

- Resolution: Another important characteristics of Hall effect sensors is the resolution. Resolution defines the smallest changes in the quantity that the sensor can detect.

Resolution depends on noise voltage and sensitivity of the system and can be calculated according to Equation 1.18.

$$B_{Resolution} = \frac{V_{n(rms)}}{Sensitivity} \tag{1.18}$$

1.2. Thesis Outline

In this thesis, a CMOS compatible Hall effect sensor is designed and simulated. A Hall plate needs to be biased and its weak output signal needs to be amplified. These are the reasons why various electronics circuits are needed for efficient functionality of Hall sensor. Different designed parts of this system are listed below.

- Hall plates are main components of the Hall sensor. According to their size, they convert the magnetic field to electrical signals that can be easily manipulated and observed. Shape of the Hall plate and the mode in which it is working is determined according to our methodology.
- Current spinning method is used to decrease offset and flicker noise. Basically, the functionality of Hall plate ports is changed from input to output periodically so that the output is an average of outputs while ports of the Hall plates change their directions.
- To use the Hall plates efficiently, they need to be biased accurately. This is a responsibility of current biasing circuit to provide precise input current for the Hall plates.
- In order to utilize output currents of the Hall plates, they are converted to voltage before amplification step.
- Finally, two amplifiers are designed to increase signal to noise ratio (SNR) and signal amplitude.

Then, layouts of different circuit parts are designed, parasitics are extracted, post-layout results are compared with pre-layout results, and conclusion is presented.

2. SYSTEM DESIGN

The Hall element is the basic component of magnetic field sensors. It requires signal conditioning to make the output usable for most applications. Figure 2.1 shows a schematic of the circuit blocks surrounding the Hall plates. Each block will be discussed in upcoming sections.

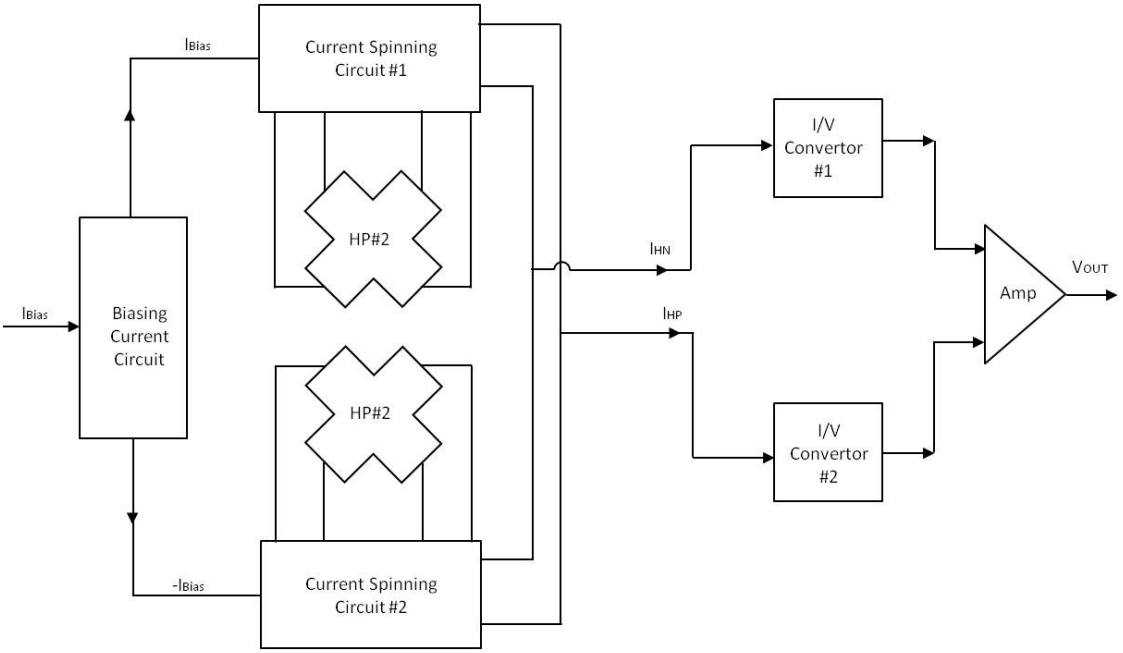


Figure 2.1. Schematic of the circuit blocks surrounding the Hall plates.

2.1. Hall Plate

As discussed in Section 1.1.2.2, current-mode Hall sensors have some advantages over voltage-mode Hall sensors. A cross-shaped Hall plate is used to utilize current spinning technique. According to Equation 2.1, the sensitivity of this mode can be calculated using Equations 1.13 and 1.14.

$$Sensitivity = \frac{\Delta I}{\Delta B} = \frac{I_{H+} - I_{H-}}{\Delta B} \tag{2.1}$$

In order to achieve differential currents at the output and increase sensitivity, a pair of Hall plates is used. Using two Hall plates results in zero output currents, I_{HN}

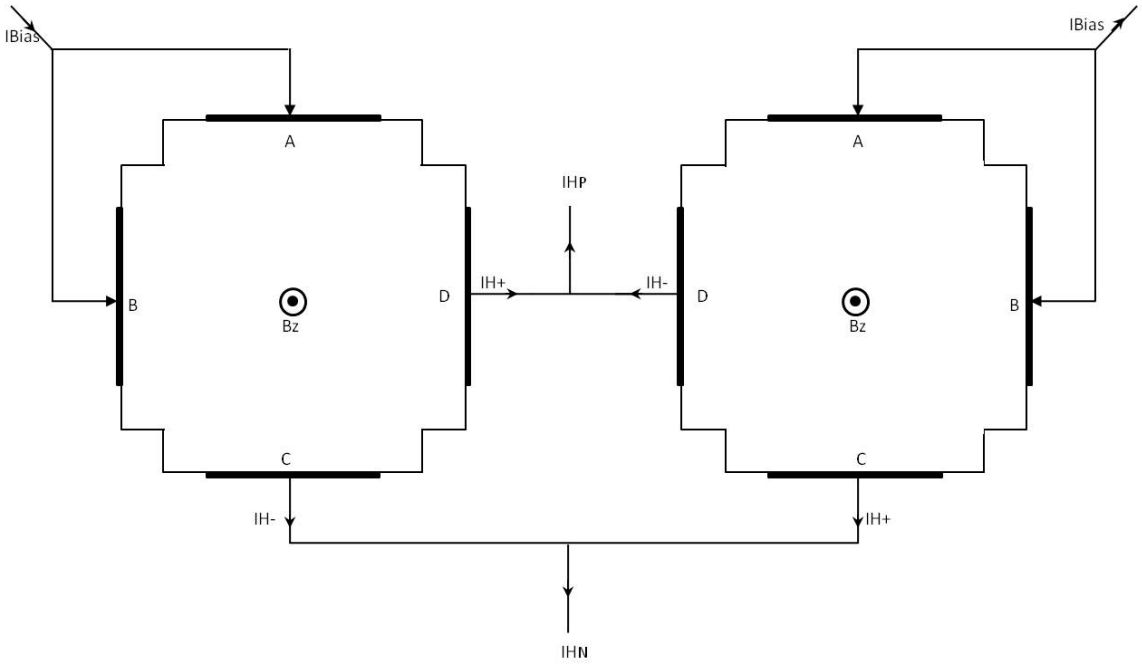


Figure 2.2. A pair of current-mode Hall sensors structure.

(negative output current of two current-mode Hall plate) and I_{HP} (positive output current of two current-mode Hall plate) when $B = 0$. Upon applying a magnetic field, the sensors generate Hall currents, I_{Hall}, at the output nodes. By using this method, the sensitivity of the sensor can be doubled.

$$I_{HP} = I_{H+} - I_{H-} \tag{2.2}$$

$$I_{HN} = I_{H-} - I_{H+} \tag{2.3}$$

$$Sensitivity = \frac{\Delta I}{\Delta B} = \frac{I_{HP} - I_{HN}}{\Delta B} \tag{2.4}$$

2.1.1. Hall Plate Model

In order to facilitate the simulation analysis of electrical circuit with integrated Hall devices, a simulation model of the Hall plate is needed considering the important physical effects and technological influences of the Hall plate. A simple yet effective extracted model of the Hall plate describes the behavior of the Hall plate in electrical circuits [30].

The model used for Hall plate with the configuration used in this thesis is shown in Figure 2.3.

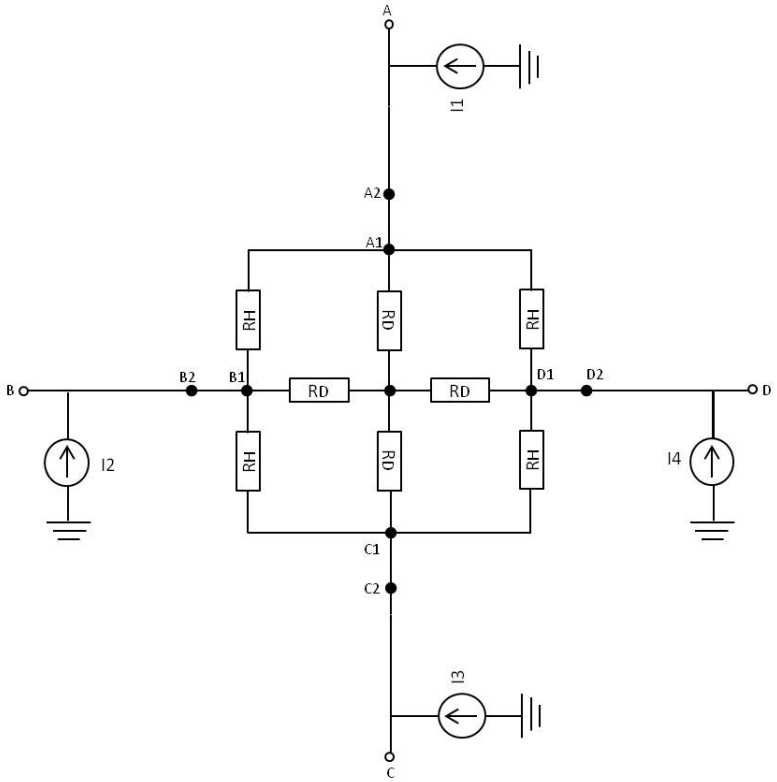


Figure 2.3. Simplified model for CMOS integrated cross-shaped Hall plate adopted from [30].

$$R_H = \frac{2R_S}{\pi}[(2\frac{L}{W} + \frac{2}{3})\pi - 2ln2] \tag{2.5}$$

$$\frac{R_H}{R_D} = 2 - \frac{8}{\pi}\frac{ln2}{2L/W + 2/3} \tag{2.6}$$

$$R_{eq} = \frac{R_H R_D}{R_D + \frac{R_H}{2}} \tag{2.7}$$

In the model, each Hall current is modeled by using the current-controlled current sources with the following equations:

$$I_{H/2_1} = \frac{1}{2}\frac{1}{R_{eq}} S_{V_I} I(D_1, D_2) B \tag{2.8}$$

$$I_{H/2_2} = \frac{1}{2}\frac{1}{R_{eq}} S_{V_I} I(A_1, A_2) B \tag{2.9}$$

$$I_{H/2_3} = \frac{1}{2}\frac{1}{R_{eq}} S_{V_I} I(B_1, B_2) B \tag{2.10}$$

$$I_{H/2_4} = \frac{1}{2}\frac{1}{R_{eq}} S_{V_I} I(C_1, C_2) B \tag{2.11}$$

2.2. Current Spinning Circuit

The performance of Hall plates may suffer from process variations and because of contact misalignment, they have a large and time dependent offset. Other disadvantages include thermal effects, surface charges, and stress [27]. This is where the spinning current method proves most useful. Using this method, the Hall plates will rotate relative to the input currents, and as a result, the offset will be compensated in time due to the averaging outputs.

The clock signals used to control the switches are 4 different non-overlapping

clock signals, CLK_1, CLK_2, CLK_3, and CLK_4. At the end of each rotation, the average of output offset is zero. The topology of the Hall plates as well as the switches connected to their terminals is shown in Figure 2.4. The switches are derived with clock signals shown in Figure 2.5. During each phase, switching part connects two of each Hall plate terminals to input bias current, I_{Bias}, while other two terminals form the outputs. According to this design, 32 switches are needed, each of them consisting of parallel NMOS and PMOS transistors forming a transmission gate (Figure 2.6).

Table 2.1. Hall plates' connections on each clock phase.

Hall plate number	Terminals name	CLK_1	CLK_2	CLK_3	CLK_4
Hall plate 1	A	I_{Bias}	I_{HP}	I_{HN}	I_{Bais}
	B	I_{Bias}	I_{Bias}	I_{HP}	I_{HN}
	C	I_{HN}	I_{Bias}	I_{Bias}	I_{HP}
	D	I_{HP}	I_{HN}	I_{Bias}	I_{Bias}
Hall plate 2	A	$-I_{Bias}$	I_{HN}	I_{HP}	$-I_{Bias}$
	B	$-I_{Bias}$	$-I_{Bias}$	$-I_{HN}$	I_{HP}
	C	I_{HP}	$-I_{Bias}$	$-I_{Bias}$	I_{HN}
	D	I_{HN}	I_{HP}	$-I_{Bias}$	$-I_{Bias}$

2.2.1. Switching Clock Generator Circuit

In order to generate the clock signals used in current spinning, a unique digital circuit is needed, which in turn needs a frequency divider.

2.2.1.1. Frequency Divider. A frequency divider, also called a clock divider, is a circuit that takes an input signal of a frequency, f_{in}, and generates an output signal of a frequency according to Equation 2.12. In this equation, m is an integer.

$$f_{out} = \frac{f_{in}}{m} \tag{2.12}$$

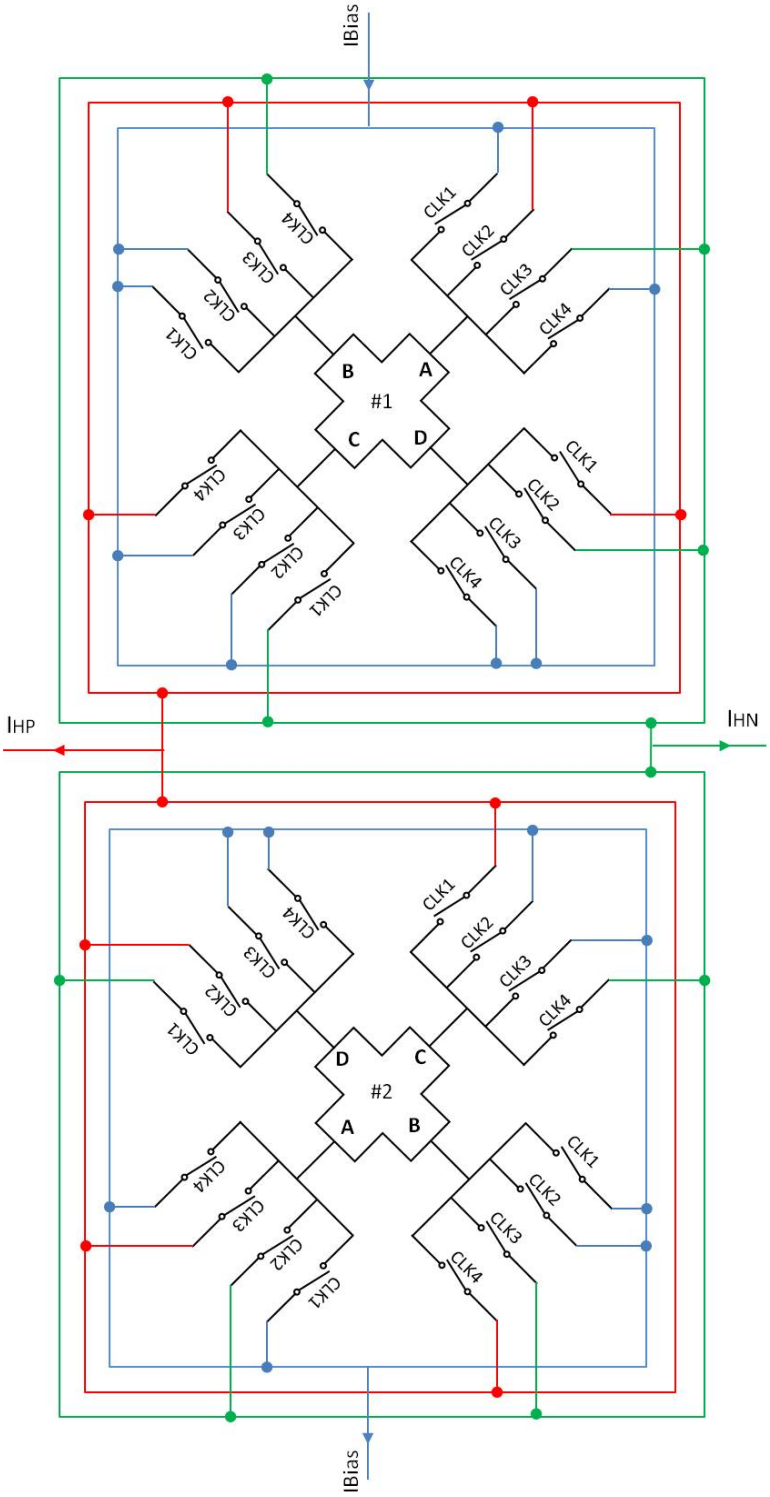


Figure 2.4. Hall plates with switches configuration for current spinning.

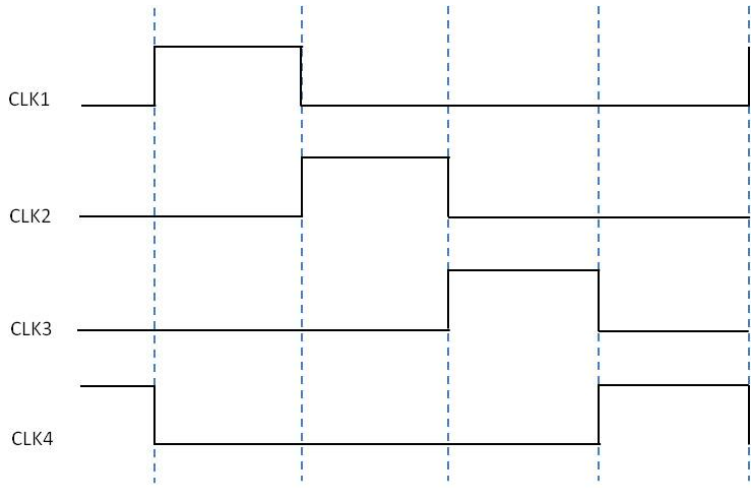


Figure 2.5. Clock signals' diagram for current spinning operation.

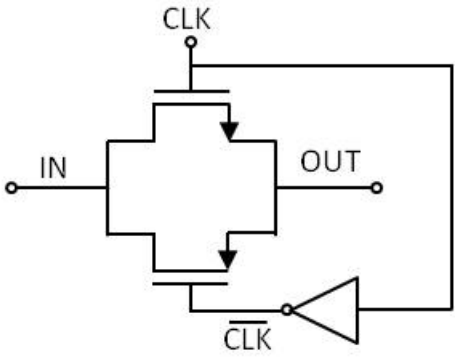
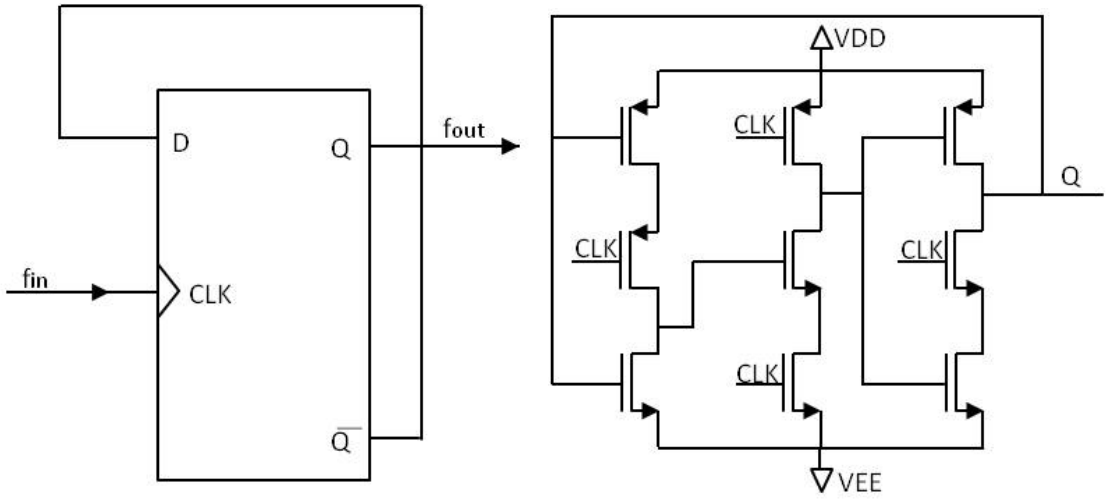


Figure 2.6. Schematic of transmission gate used as a switch.

A simple binary counter can perform the divide-by-2 operation (Figure 2.7). By connecting the output of the circuit $\overline{Q}$ to the input node, D, on each rising-edge of the input clock signal, the output changes its logic value, hence, having half the frequency compared to the input clock. Schematic of a divide-by-2 frequency divider which is implemented using D-type flip-flop is shown in Figure 2.7. The design is based on the parasitic capacitances of wires. Figure 2.8 shows the desired result for a divide-by-2 frequency divider.



(a) (b)

Figure 2.7. Schematic of a divide-by-2 frequency divider.

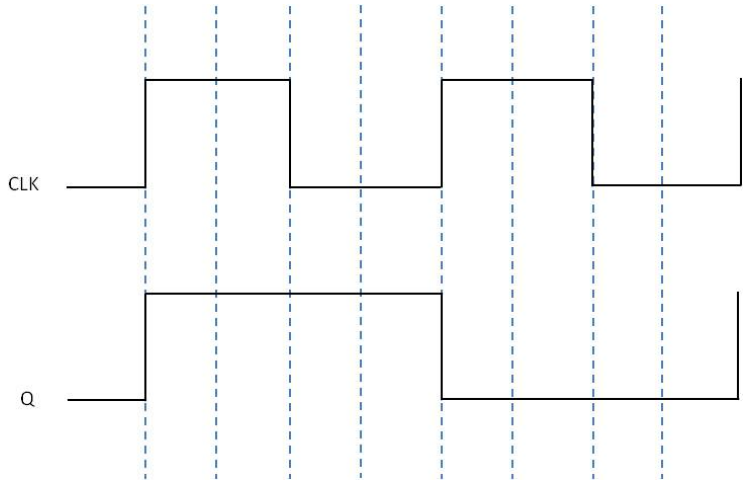


Figure 2.8. Desired result of a divide-by-2 frequency divider.

2.2.1.2. Clock Generator. Now, by using the frequency divider designed above, signal clocks are generated. A digital circuit is designed to generate 4 different clock signals based on input clock signal of the circuit and the output of frequency divider. These two signals can have 4 possible permutations, each turning one output clock signals to 1. The schematics are shown in Figures 2.9, 2.10, 2.11, and 2.12.

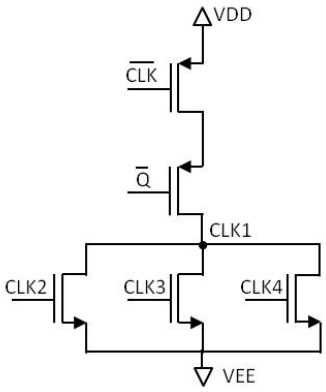


Figure 2.9. Clock 1.

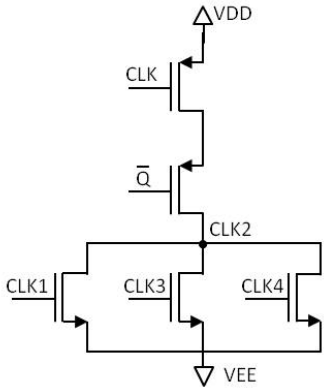


Figure 2.10. Clock 2.

2.2.1.3. Buffer. In order to make the clock signals stronger and synchronize their fall and rise times, a buffer is used at the outputs. The simplified block diagram of the buffer and its schematic are shown in Figure 2.13. The effects of using buffers on switching is shown in Figure 2.14.

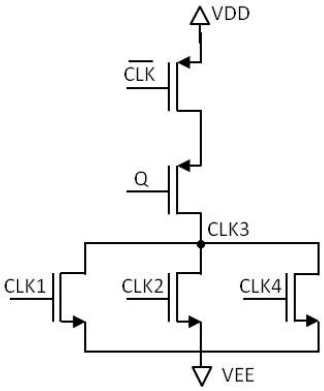


Figure 2.11. Clock 3.

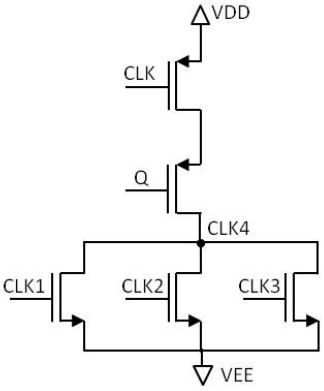
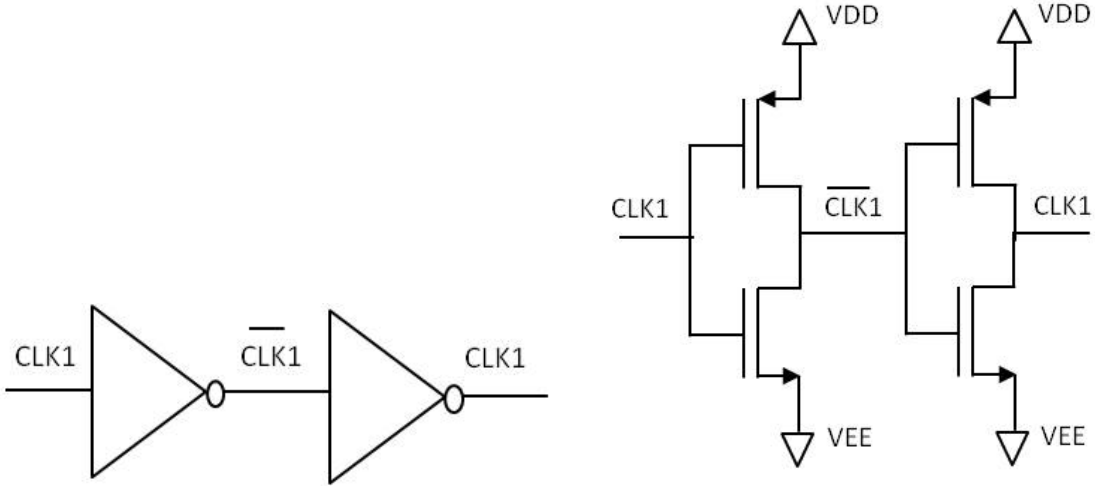


Figure 2.12. Clock 4.



(a) (b)

Figure 2.13. Schematic of buffer circuit.

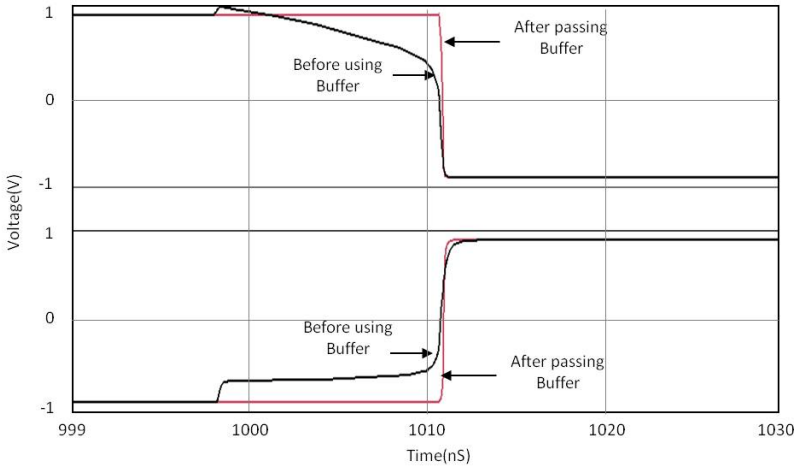


Figure 2.14. Effect of using buffers on switching.

2.3. Current Biasing Circuit

Biasing in electronics is the method of establishing predetermined voltages or currents at various points of an electronic circuit for the purpose of establishing proper operating conditions for different components in the circuit. Figure 2.15 shows the circuit that is used to bias the Hall plates. Hall plates need two identical bias currents which are determined by the input resistance of the Hall plates and supply voltage.

2.3.1. Low Voltage Current Mirror

Low voltage cascode current mirror is used to mirror the current in order to lower the supply voltage requirement while preserving the properties of a traditional cascode current amplifier. In order to determine the bias current, the supply voltage and input resistance of each Hall plate should be determined. According to Figure 1.8, the input resistance of the Hall plate $R_{Hall\ plate}$ can be calculated by Equation 2.13.

$$R_{Hall\ plate} = \frac{V_{A,B}}{I_{Bias}} \tag{2.13}$$

According to Figure 3.1, the input resistance of each Hall plate is approximately equal to $200\,K\Omega$, so I_{Bias} should be considered equal to $3\,\mu A$ according to supply

voltages which are $-0.9\,V$ and $+0.9\,V$. As a result, over-drive voltage (V_{ov}) for each transistor is considered approximately $0.15\,V$, so that transistors run in saturation region. According to the Figure 2.15:

$$I_{Bias} = I_{D_{M1}} = I_{D_{M2}} \tag{2.14}$$

$$I_D = \frac{1}{2} \times \mu \times C_{ox} \times (\frac{W}{L}) \times (V_{ov}^2) \tag{2.15}$$

where I_D is drain current of a transistor, μ is mobility, C_{ox} is gate oxide capacitance per unit, W is width of transistor, and L is length of transistor.

Because M_1, M_3, M_5, and M_{11} share the same gate source voltage and have same coefficients:

$$\frac{I_{D_{M3}}}{I_{D_{M1}}} = \frac{(\frac{W}{L})_{M3}}{(\frac{W}{L})_{M1}} \tag{2.16}$$

$$\frac{I_{D_{M5}}}{I_{D_{M1}}} = \frac{(\frac{W}{L})_{M5}}{(\frac{W}{L})_{M1}} \tag{2.17}$$

$$\frac{I_{D_{M11}}}{I_{D_{M1}}} = \frac{(\frac{W}{L})_{M11}}{(\frac{W}{L})_{M1}} \tag{2.18}$$

Also, M_8 and M_{10} share the same gate source voltage and have same coefficients and as a result:

$$\frac{I_{D_{M8}}}{I_{D_{M10}}} = \frac{(\frac{W}{L})_{M8}}{(\frac{W}{L})_{M10}} \tag{2.19}$$

2.3.2. Common Mode Feedback Circuit

The sensor structure of Figure 2.4 needs two identical input currents. A possible mismatch results in lower available over-drive voltage for the circuit with higher current, possibly brings its transistors to linear region. A common mode feedback (CMFB) network is implemented to solve this issue and tries to keep the currents identical. This circuit, senses the common mode voltages and compares them with a reference voltage. The result is an error signal that cancels the mismatch in bias current and fixes the output voltages to a desired level.

$$V_{CM} = \frac{V_{G_{M13}} + V_{G_{M14}}}{2} \tag{2.20}$$

where V_G is gate voltage of a transistor.

$$I_{D_{M11}} = I_{D_{M12}} + I_{D_{M13}} + I_{D_{M14}} \tag{2.21}$$

If $I_{D_{M13}} + I_{D_{M14}} = I_{Constant}$:

$$I_{D_{M11}} = I_{D_{M12}} + (\frac{I_{Constant}}{2} + \Delta I) + (\frac{I_{Constant}}{2} - \Delta I) \tag{2.22}$$

The equations show that $I_{D_{M11}}$ will not change even when large differential signal voltages are present. If VCM is used to control the bias voltages of the output stage, then the voltage in output nodes of the main circuit can vary without changing the bias current. CMFB has 3 important advantages:

- Sense the common-mode voltages level of the differential outputs
- Compare the common-mode voltages to a reference voltage
- Return the error to the amplifier's bias network to adjust the current and eventually the outputs voltage

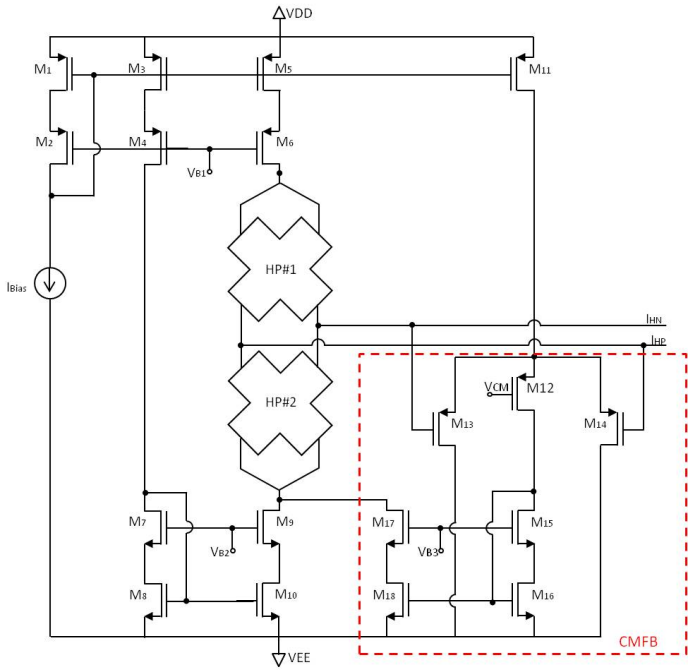


Figure 2.15. Schematic of current biasing circuit adopted from [14].

2.4. Current to Voltage Converter

Using a capacitance, the current output of Hall plates can be converted to voltage.

$$I_{OUT} = C \times \frac{dV}{dt} \tag{2.23}$$

A capacitor reseting switch is needed to reset capacitor voltage. This capacitor reseting switch helps discharging the capacitor. The relation between reseting switch frequency $f_{Reseting\ switch}$ and switching clock frequency $f_{Switching\ clock}$ is described in Equation 2.24.

$$f_{Reseting\ switch} = \frac{f_{Switching\ clock}}{2} \tag{2.24}$$

Schematic of the current to voltage converter circuit is show in Figure 2.16. A transmission gate which is shown in Figure 2.6 is used as a switch.

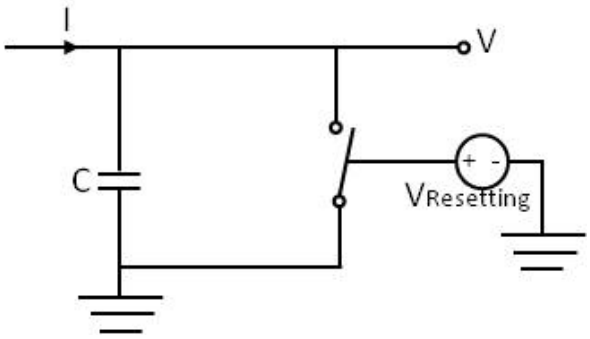


Figure 2.16. Current to voltage converter circuit.

2.5. Differential Voltage Amplifier

After converting the Hall current to voltage, the result is a small voltage ranging up to 70 μV at maximum magnetic field. Since this value is small considering the noise and non-ideal current biasing circuit, amplifying this signal and increasing SNR are essential. Consequently, two differential amplifiers are designed and added to output of the current to voltage blocks. Differential amplifiers are used since they have a high common mode rejection ratio (CMRR) and it has higher immunity to environmental noise in comparison with single ended amplifiers. The total gain of these two stage amplifiers can be calculated according to Equation 2.25.

$$Gain_{Total} = Gain_{First\ stage} \times Gain_{Second\ stage} \tag{2.25}$$

2.5.1. First Stage Amplifier

A fully differential cascode amplifier is used as the first stage because it has good noise performance and can provide larger gain by increasing the output resistance of a stage. Schematic of the amplifier is shown in Figure 2.17.

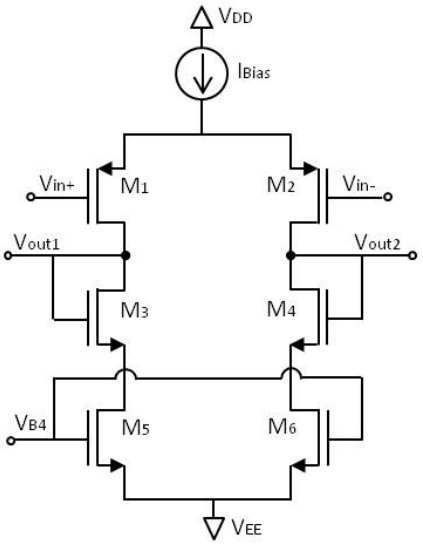


Figure 2.17. First stage differential voltage amplifier.

$$I_{D_{M1}} = I_{D_{M2}} = I_{D_{M3}} = I_{D_{M4}} = I_{D_{M5}} = I_{D_{M6}} = \frac{I_{Bias}}{2} \tag{2.26}$$

$$Gain = \frac{V_{OUT_1}}{V_{IN_1}} = G_{m_1} \times R_{OUT_1} \tag{2.27}$$

$$Gain \approx -g_{m_{1,2}} \times r_{out_{1,2}} \parallel r_{out_{5,6}} \tag{2.28}$$

$$g_m = \frac{2 \times I_D}{V_{ov}}, r_{out} = \frac{V_A}{I_D} \tag{2.29}$$

In the above equations, G_m transconductance of input network, R_{OUT} is output resistance of output network, g_m is transconductance of each transistor, r_{out} is output resistance of each transistor, and V_A is Early voltage.

2.5.2. Second Stage Amplifier

A fully differential pair amplifier is used loaded with a biased transistor working as a current source for the second stage. The schematic of the amplifier is shown in

Figure 2.18. In this amplifier, M_7 and M_8 are input NMOS devices and are relatively large and are derived with smaller over-drive voltage with higher output resistance to provide a gain boost for the system. In addition, choosing this configuration for these transistors, increase the CMRR of the amplifier. The PMOS devices M_9 and M_{10} are designed to have high resistance to increase the gain. Current passing through the tail transistor M_{11} is twice other transistors, so it should have roughly twice over-drive voltage compared with the input transistors.

$$I_{M_7} = I_{M_8} = I_{M_9} = I_{M_{10}} = \frac{1}{2} I_{M_{11}} \tag{2.30}$$

$$Gain = \frac{V_{OUT_2}}{V_{IN_2}} = G_{m_2} \times R_{OUT_2} \tag{2.31}$$

$$Gain = -g_{m_{7,8}} \times (r_{out_{7,8}} \parallel r_{out_{9,10}}) \tag{2.32}$$

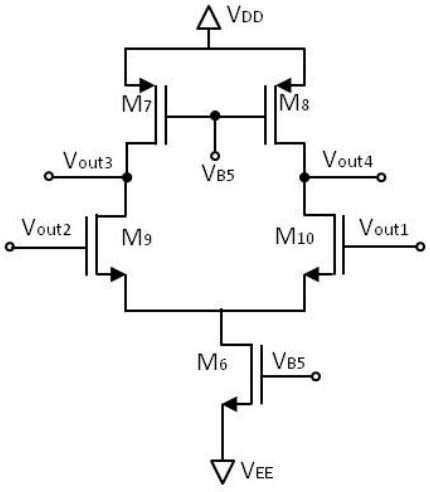


Figure 2.18. Second stage differential voltage amplifier.

3. Simulation Results

3.1. Hall Plate

The current-mode technique is applied to a two-dimensional (2D) model of the Hall plate simulated using commercial finite-element method (FEM) software, with parameters summarized in Table 3.1. The parameters are extracted from $0.13\,\mu m$ CMOS technology characteristics. As mentioned in previous chapters, the cross shaped Hall plate is used with dimensions shown in Figure 3.1. The maximum width and length are $8\,\mu m$ and the simulation uses the nominal bias current of $3\,\mu A$. Surface electrical distribution of the Hall plate when a magnetic field of $20\,mT$ is applied is shown in Figure 3.1.

Table 3.1. Model parameters.

Symbol	Value
q $[C]$	-1.602×10^{-19}
n $[cm^{-3}]$	1.7×10^{17}
μ $[cm^2/(V \times Sec)]$	416
t $[m]$	2.73×10^{-9}

FEM simulation result of a current-mode Hall plate is shown in Figure 3.2. Sensitivity can be calculated according to Equation 3.1.

$$Sensitivity = \frac{\Delta I}{\Delta B} = 52.2\, n \frac{A}{T} \tag{3.1}$$

In order to to achieve differential currents at the outputs and increase sensitivity, a pair of Hall plates is used. As a result, the current-mode technique is applied to a pair of 2D model of the Hall plates. Figure 3.3 also shows the surface electrical

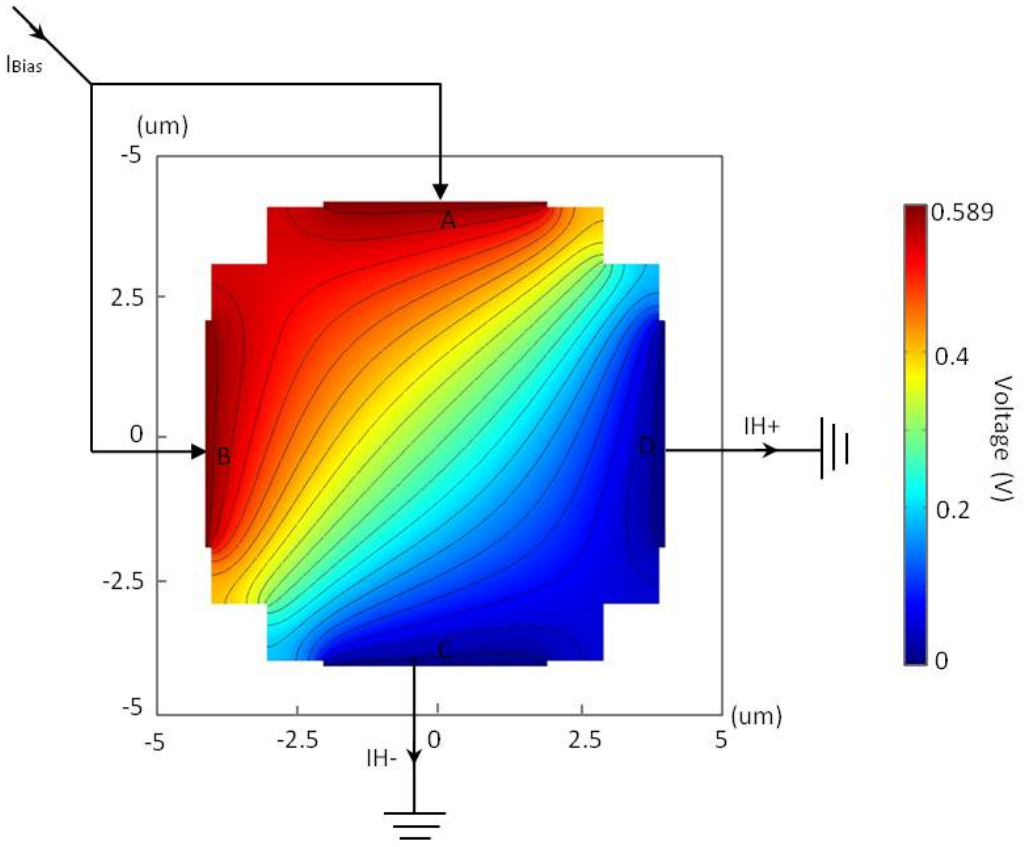


Figure 3.1. FEM simulation of a current-mode Hall plate when bias current is equal to $3\,\mu A$.

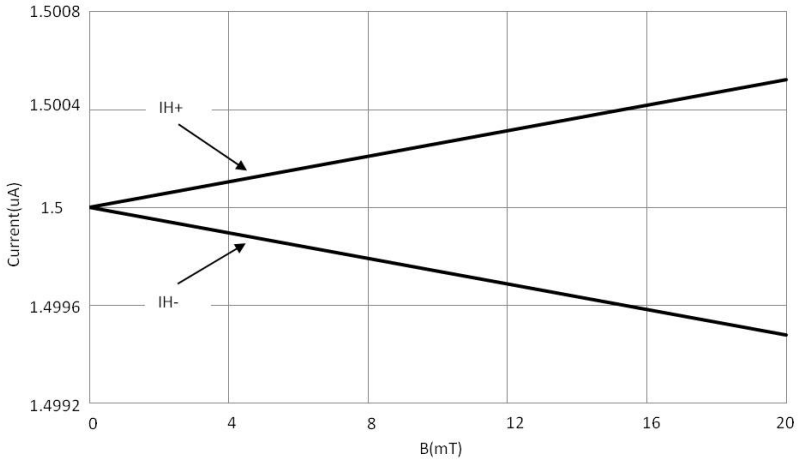


Figure 3.2. FEM simulation result of a current-mode Hall plate when bias current is equal to $3\,\mu A$.

distribution when a magnetic field of $20\,mT$ is applied and the simulation uses the nominal bias currents of $3\,\mu A$ and $-3\,\mu A$.

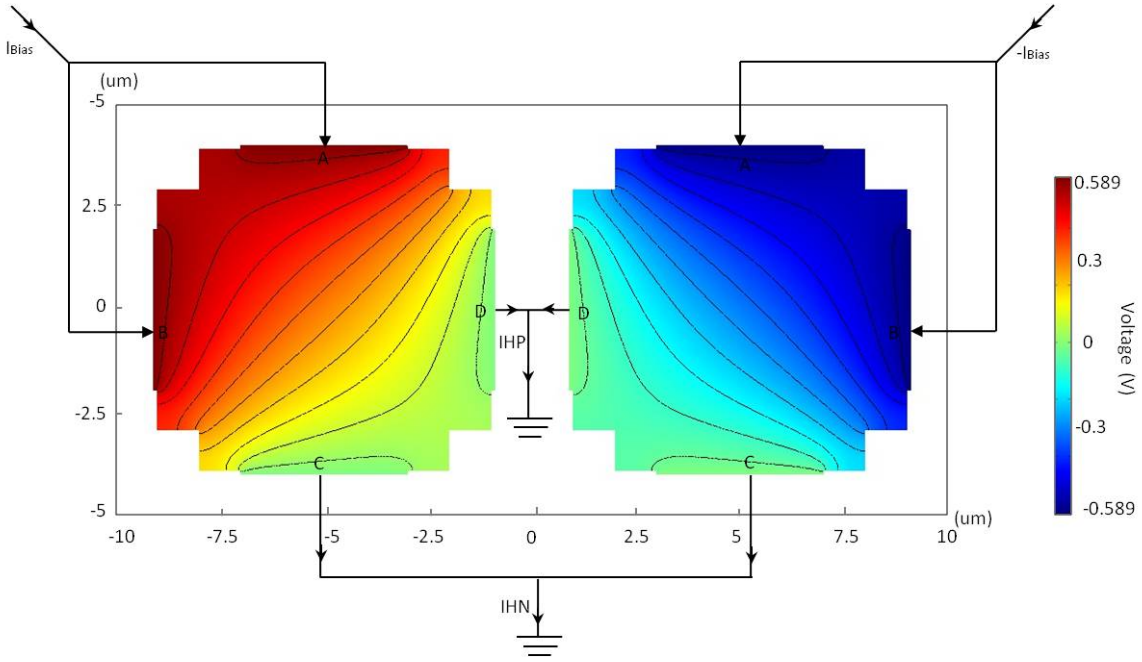


Figure 3.3. FEM simulation of two current-mode Hall plates structure when bias currents are equal to $3\,\mu A$ and $-3\,\mu A$.

FEM simulation result of a pair of current-mode Hall plates is shown in Figure 3.2.

$$Sensitivity = \frac{\Delta I}{\Delta B} = 104.2\,n\frac{A}{T} \tag{3.2}$$

According to Equation 3.2, sensor sensitivity is doubled by using a pair of Hall plates.

Spice model for a Hall plate is described in Section 2.1.1. According to Table 3.1, $R_D = 1.08\,M\Omega$, $R_H = 1.44\,M\Omega$, $R_{eq} = 863\,K\Omega$, $S_I = 1.35 \times 10^4$. The results of FEM simulations and spice simulations agree very well as shown in Figures 3.2, 3.4, 3.5 and 3.6. The values of sensitivity are shown in Equations 3.3 and 3.4.

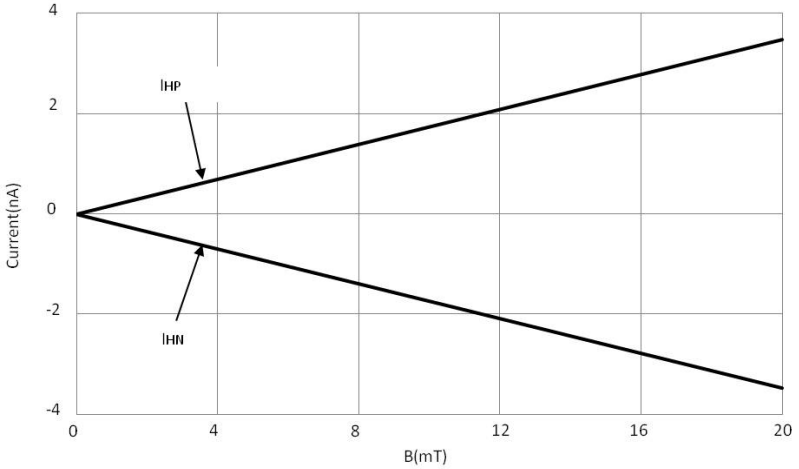


Figure 3.4. FEM simulation result of two current-mode Hall plates structure when when bias currents are equal to $3\,\mu A$ and $-3\,\mu A$.

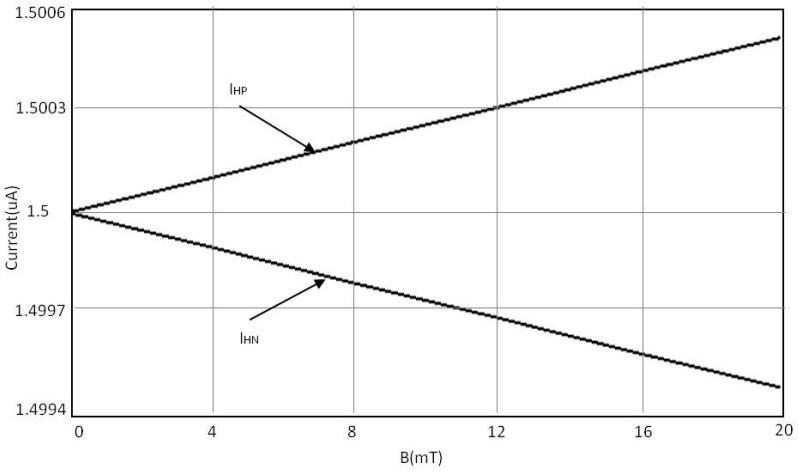


Figure 3.5. Result of Hall sensor's model when bias current is equal to $3\,\mu A$.

$$Sensitivity = 52.2\, n\frac{A}{T} \tag{3.3}$$

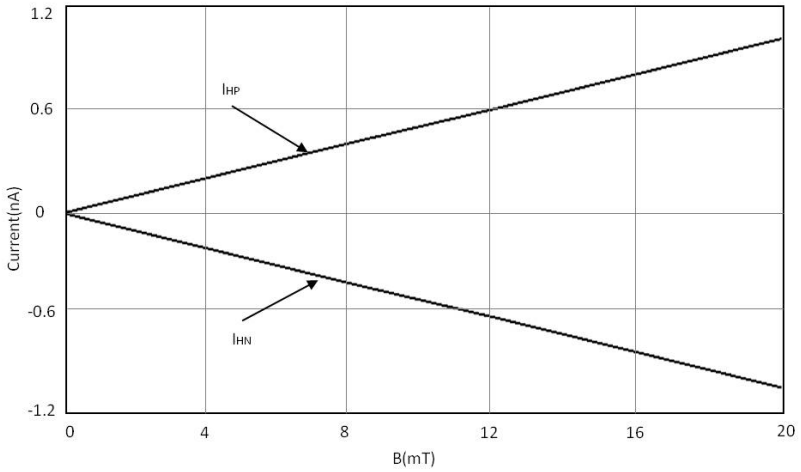


Figure 3.6. Result of a pair of Hall sensors' model when two Hall plates are used and bias currents are equal to $3\,\mu A$ and $-3\,\mu A$.

$$Sensitivity = 104.2\, n\frac{A}{T} \tag{3.4}$$

3.2. Current Spinning Circuit

As mentioned in Section 2.2, the proposed cross current-mode Hall plates enables us to apply the current spinning technique. Four clock signals CLK_1, CLK_2, CLK_3, and CLK_4 control the switches and consequently connections of Hall plates terminals. These four clock signals are generated by a switching clock generator circuit which is described in Section 2.2.1. This switching clock generator consists of a frequency divider, 4 clock generator circuits and buffers. Pre-layout and post-layout simulation results of frequency divider are shown in Figures 3.7 and 3.8.

In the next step, the frequency divider circuit is connected to a digital circuit, which generates clock signals, and buffer blocks. The layout of this part of the circuit

is shown in Figure A.3. Pre-layout and post layout simulation results of whole clock generator circuit are shown in Figures 3.9 and 3.10.

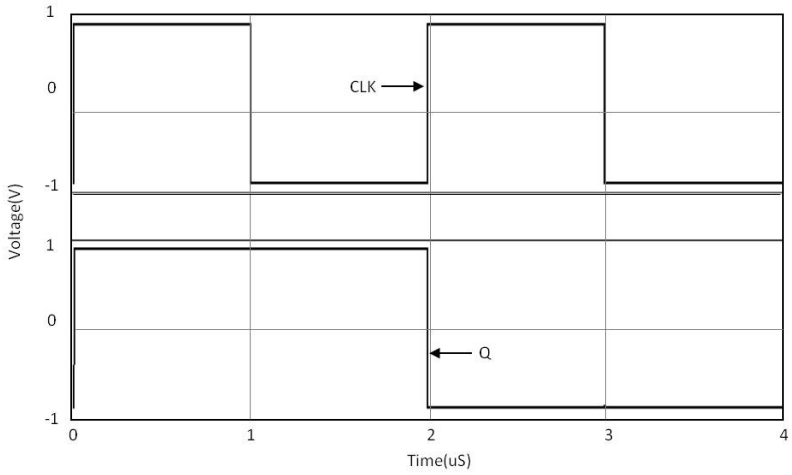


Figure 3.7. Pre-layout simulation result the divide-by-2 frequency divider.

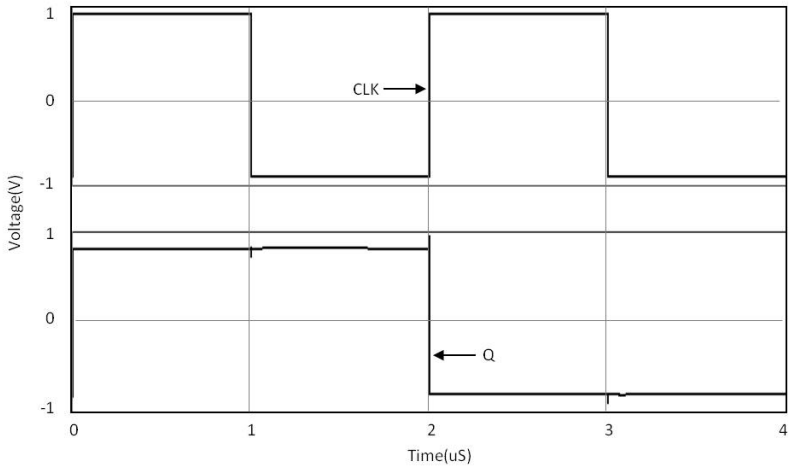


Figure 3.8. Post-layout simulation result of the divide-by-2 frequency divider.

Finally, the complete switching clock generator block (Figure A.3) is connected to 32 switches (Figure A.2) and pre-layout and post-layout simulation results are shown in Figures 3.11 and 3.12.

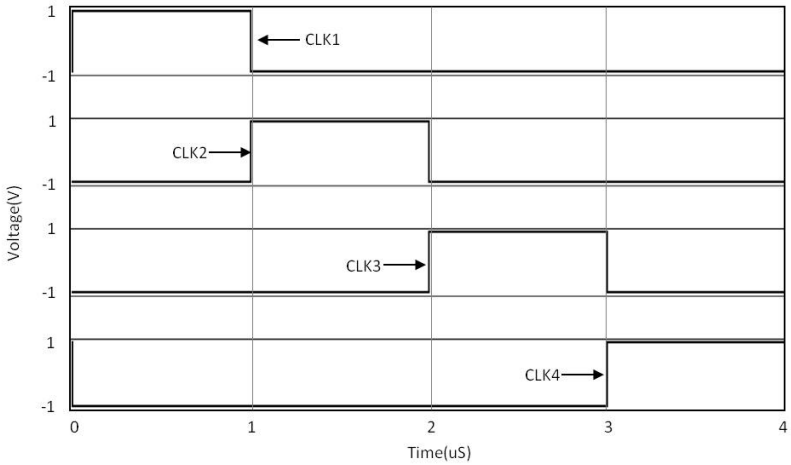


Figure 3.9. Pre-layout simulation result of complete switching clock generator circuit.

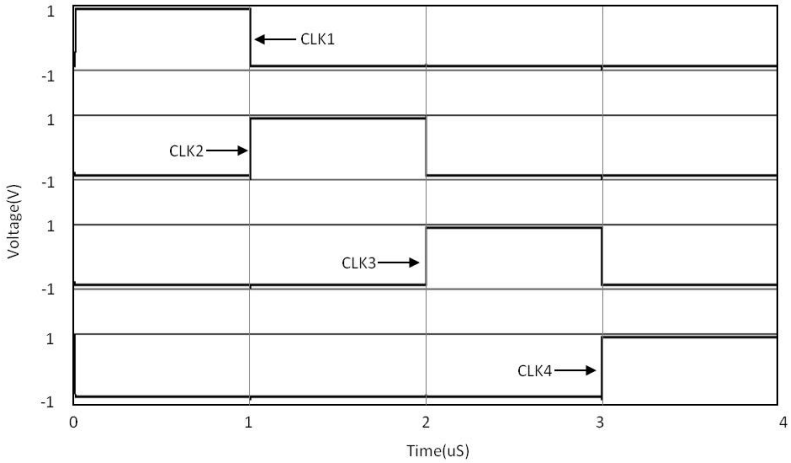


Figure 3.10. Post-layout simulation result of complete switching clock generator circuit.

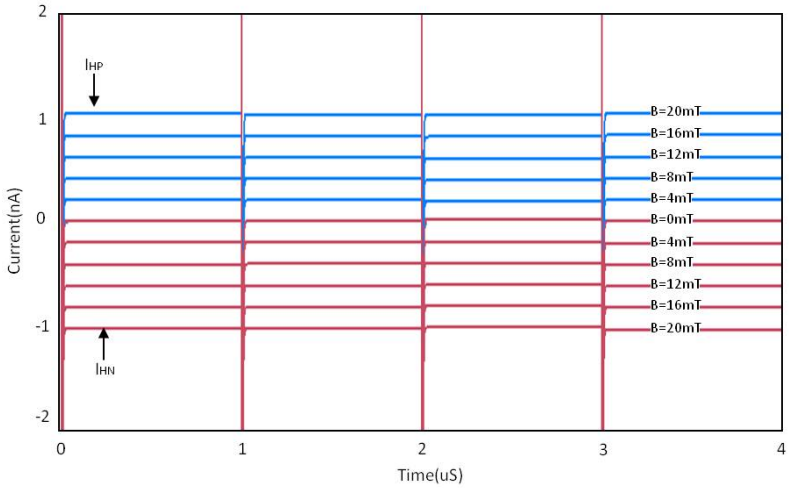


Figure 3.11. Pre-layout simulation result of Hall plates connected to current spinning block.

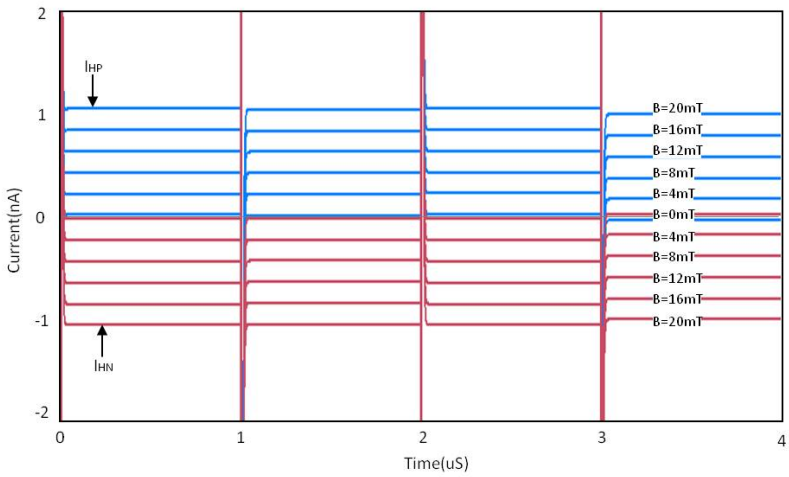


Figure 3.12. Post-layout simulation result of Hall plates connected to current spinning block.

3.3. Current Biasing Circuit

The proposed current biasing circuit in Figure 2.15 is designed and simulated in Mentor Graphics. Considering certain over-drive voltages for transistors in current biasing circuit and the resistance of Hall plates, $3\,\mu A$ is calculated as DC current passing through all plates. The layout of the current biasing circuit is drawn (Figure A.4) and connected to other parts of the circuit. Pre-layout and post-layout simulation results are shown in Figures 3.13 and 3.14 .

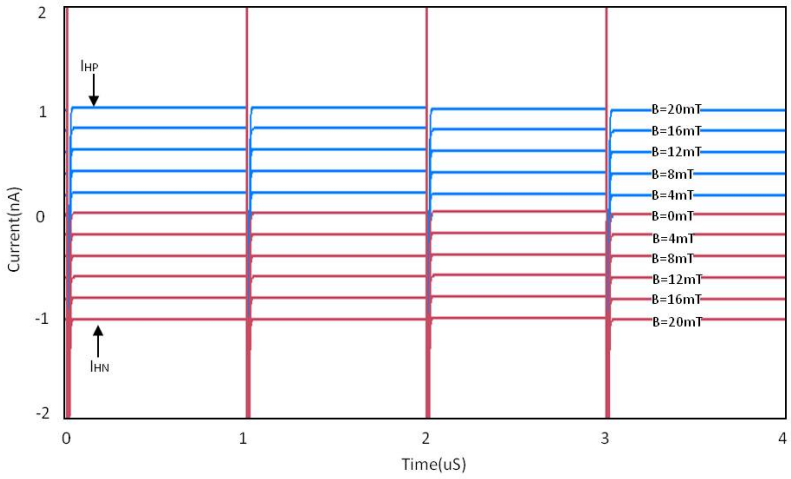


Figure 3.13. Pre-layout simulation result of Hall plates biased using current biasing circuit and connected to current spinning block.

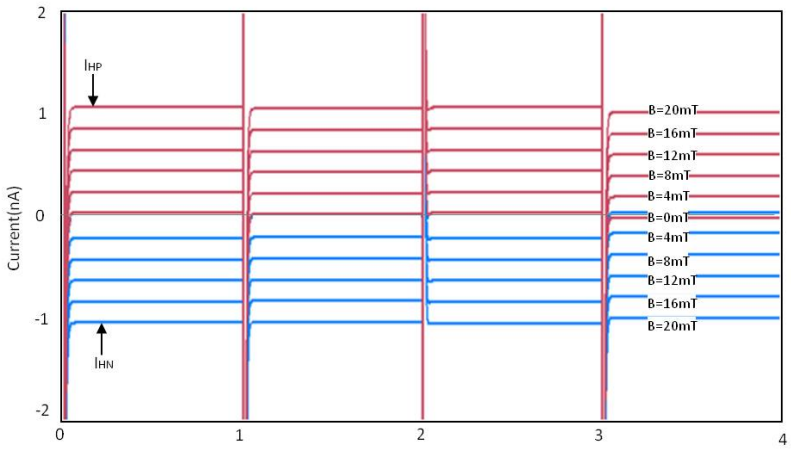


Figure 3.14. Post-layout simulation result of Hall plates biased using current biasing circuit and connected to current spinning block.

3.4. Current to Voltage Converter

By using the proposed circuit (see Figure 2.16) the current is converted to voltage. In the next step, the current to voltage converter circuit layout (Figure A.5) is connected to other parts of circuit and tries to convert current outputs come from Hall plates to voltage. Pre-layout and post-layout simulation results are shown in Figures 3.15 and 3.16. Parasitics add a small current offset to the outputs of current biasing circuit; this mismatch in currents is then converted to voltage and acts as an offset. This is the reason why in post-layout simulations, the converted voltage signal has an initial value, which changes in each phase according to the designed current spinning circuit and as a result, the output voltage will be free of the offset and will have additional high frequency noise. Frequency of this noise is same as frequency of the input signal of the clock divider circuit and can be filtered out easily with low-pass filter (LPF).

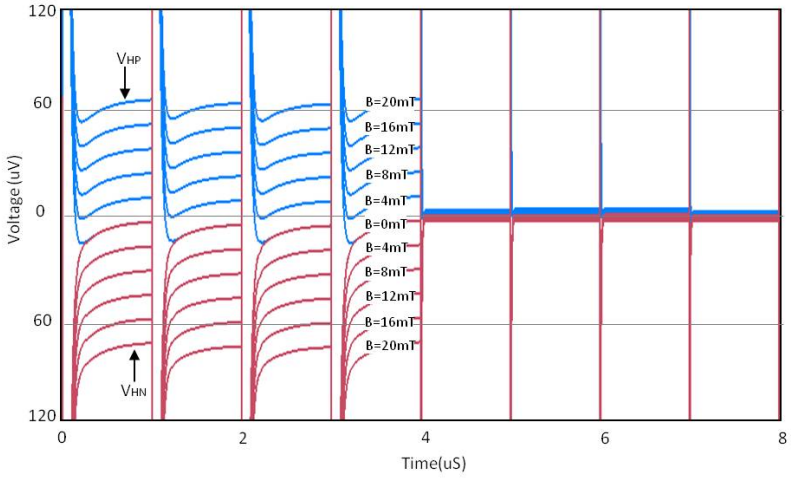


Figure 3.15. Pre-layout simulation result of current to voltage converter.

3.5. Differential Voltage Amplifier

As mentioned in Section 2.5, the output voltage comes from current to voltage converter, needs to be amplified in order to increase sensitivity. Two fully differential amplifiers are used. Total gain of these two amplifiers is approximately equal to 3570. Layout of these two differential amplifiers (Figures A.6 and A.7) are drawn

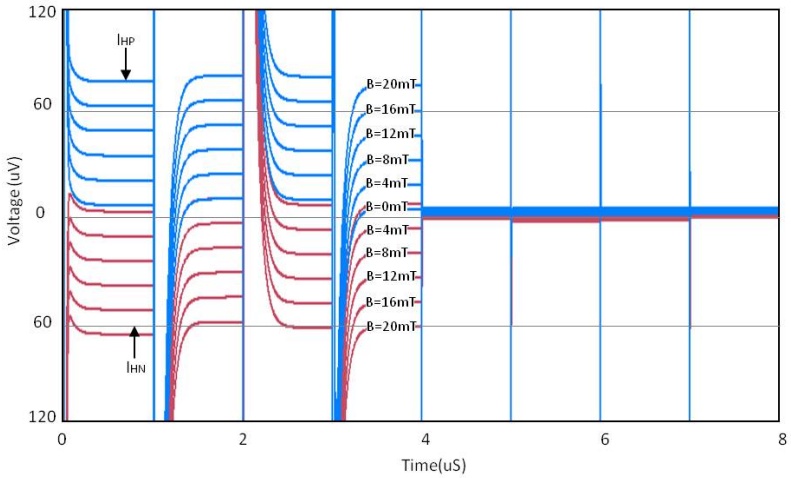


Figure 3.16. Post-layout simulation result of current to voltage converter.

and connected to other parts of the circuit (Figure A.8). Pre-layout and post-layout simulation results are shown in Figures 3.17 and 3.18.

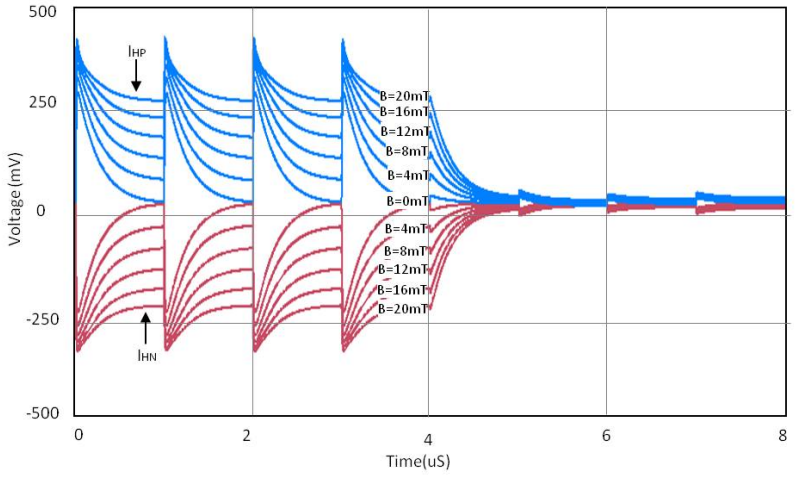


Figure 3.17. Pre-layout simulation result of whole proposed circuit.

The sensitivity of whole proposed system is calculated in Equation 3.5.

$$Sensitivity = \frac{\Delta V}{\Delta B} = \frac{503\,mV}{20\,mT} = 25.15\,\frac{V}{T} \tag{3.5}$$

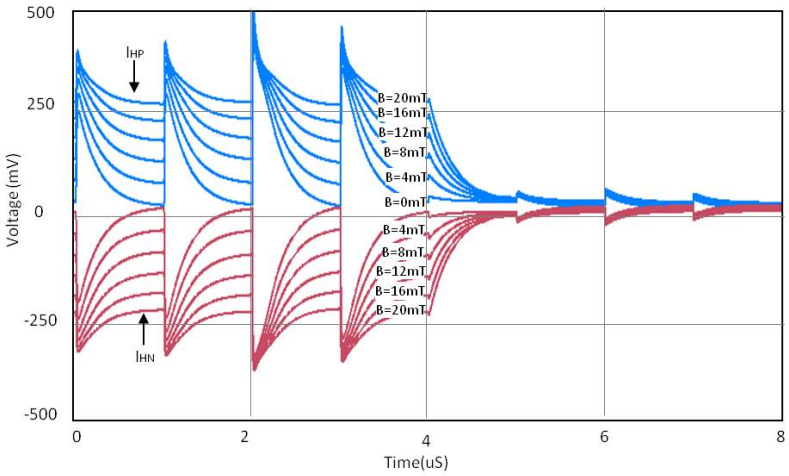


Figure 3.18. Post-layout simulation result of whole proposed circuit.

3.6. Noise Simulation

Noise is an inseparable part of every electronics circuitry. In addition, Hall plates can act as extra noise sources. As a result, it is essential to consider effects of noise.

3.6.1. Noise of Hall Plates

Noise of the Hall plates mostly consists of thermal and flicker noise. The thermal noise of each Hall plate can be calculated according to Equation 3.6.

$$Vn(Hall\,plate) = \sqrt{4 \times K \times T \times R_{Hall\,plate}} \tag{3.6}$$

According to Equation 2.13, $R_{Hall\,plate}$ is equal to $196\,K\Omega$. So:

$$Vn(Hall\,plate) = 5.7 \times 10^{-8}\,V/\sqrt{Hz} \tag{3.7}$$

In addition, flicker noise can be compensated using spinning current technique.

3.6.2. Noise of Electronic Circuitry

Since noise sources have amplitudes that vary randomly with time, they can only be specified by a probability density function. The density spectrum of whole circuitry parts is shown in Figure 3.19.

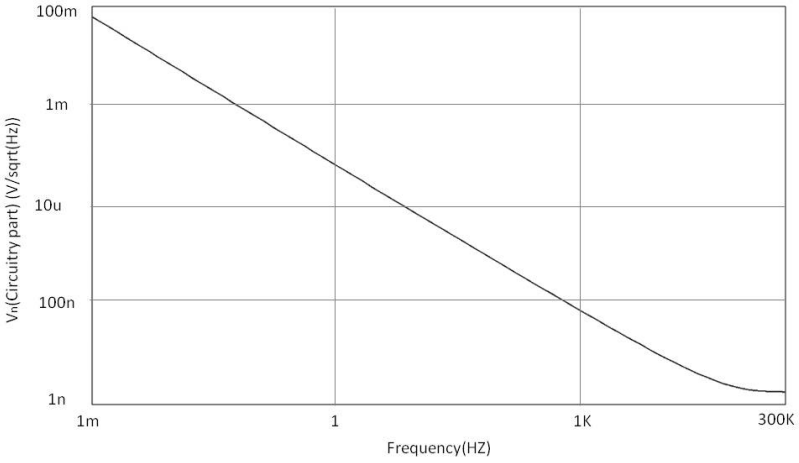


Figure 3.19. Density spectrum of noise of whole electronic circuitry.

3.6.3. Total System's Noise

The spectrum density of total noise (which is consists of total noise of whole electronic circuitry and thermal noise of Hall plates) is shown in Figure 3.20.

$$Vn(Total) = Vn(Circuitry\,part) + 2 \times Vn(Hall\,plate) \tag{3.8}$$

To calculate the real mean squared noise voltage ($V_{n(rms)}$), its power needs to be integrated over a frequency range. The beginning and ending frequency of the band is used as limits in the integration. Following equations illustrate the process.

$$V_{n(rms)}^2 = \int_{f1}^{f2} V_n^2 df \tag{3.9}$$

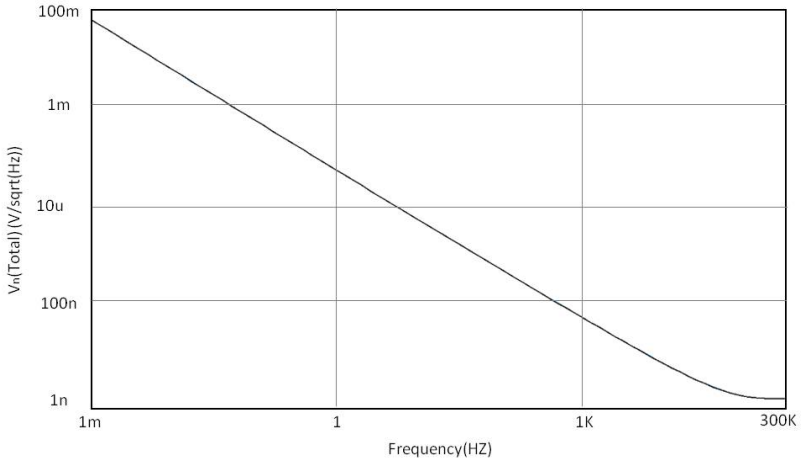


Figure 3.20. Density spectrum of total output noise.

If the noise voltage over $100\,mHz$ and $100\,Hz$ are wanted to be calculated according to the application. Figure 3.21 shows the $V^2_{n(rms)}$.

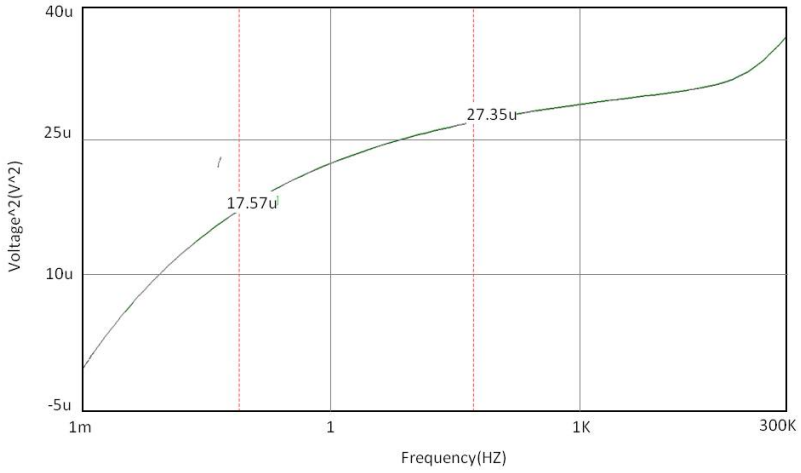


Figure 3.21. Spectrum of square $V^2_{n(rms)}$.

$$V^2_{n(rms)} = \int_{100m}^{100} V_n^2\, df = 27.35 \times 10^{-6} - 17.57 \times 10^{-6} = 9.78 \times 10^{-6} \tag{3.10}$$

$$V_{n(rms)} = 3.15 \times 10^{-3}\, V \tag{3.11}$$

Also, The magnetic field resolution can be calculated according to Equation 3.12 in a bandwidth of $100\,mHz - 100\,Hz$.

$$Resolution = \frac{V_{n(rms)}}{Sensitivity} = 124\,\mu T \tag{3.12}$$

4. CONCLUSION

The aim of this work is to improve performance of existing Hall sensors. In this work, design of Hall sensors together with electronic circuitry is presented. Two cross shaped Hall plates are used in current-mode. This choice gave us the ability to use current spinning method to overcome the asymmetric problem of Hall plates. 32 switches are used and a clock generator block is designed that is responsible for providing us with 4 non-overlapping clock signals to control the switches. Using a capacitor, the output currents are converted to voltage and then amplified using two differential amplifiers. Layout of the design is drawn and post-layout simulations are done and the results are gathered.

Even though the designed system consumes around 4 times smaller power and drains significantly lower current comparing to other works that have been published recently, the result can detect wider magnetic field range and has more than 4 times higher sensitivity that the best work available in literature. Characteristics of the design as well as post-layout simulation results and comparison with previous works in details are gathered in Table 4.1.

Table 4.1. Performance summary and comparison table of this work with recently published CMOS Hall sensors.

	This work	[31]	[32]	[33]
Year of publication	-	2015	2014	2014
CMOS technology	0.13 μm	0.18 μm	0.18 μm	0.6 μm
Supply voltage	1.8 V	1.8 V	5 V	5 V
Sensor bias current	3 μA	12 μA	350 μA	1 mA
HP shape	Cross	Cross	Cross	Cross
Sensor's number	2	2	4	1
Operation mode	Current	Current	Voltage	Voltage
Magnetic field range	20 mT	10 mT	N/A	N/A
Max sensitivity	8383 $V/(A \times mT)$	1660 $V/(A \times mT)$	0.143 $V/(A \times mT)$	0.129 $V/(A \times mT)$
Power consumption	36 μW	120 μW	N/A	120 mW

Simulation results show great promise for future works which include using this Hall sensor in pressure sensor and finally designing an array of Hall sensors to provide multi-point sensing ability for the system. Fabrication and testing the sensor remains to be done in near future.

APPENDIX A: LAYOUTS

Layout of each block of whole proposed system is shown in upcoming sections. Finally, the layout of whole proposed circuits surrounding Hall plates is shown in Section A.8.

A.1. Hall Plates

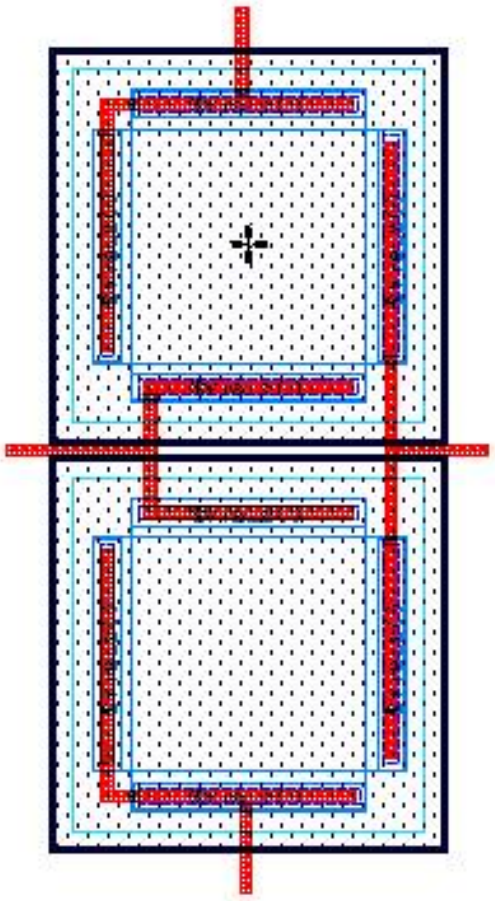


Figure A.1. Layout of two Hall plates.

A.2. Current Spinning Circuit

A.2.1. Switches

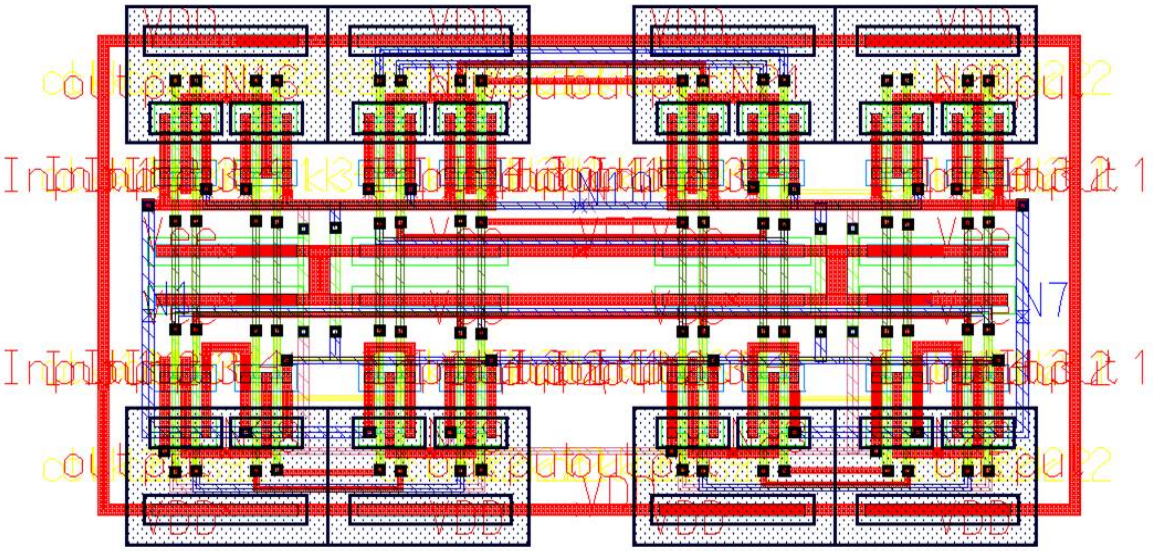


Figure A.2. Layout of 32 switches connected together.

A.2.2. Clock Generator Circuit

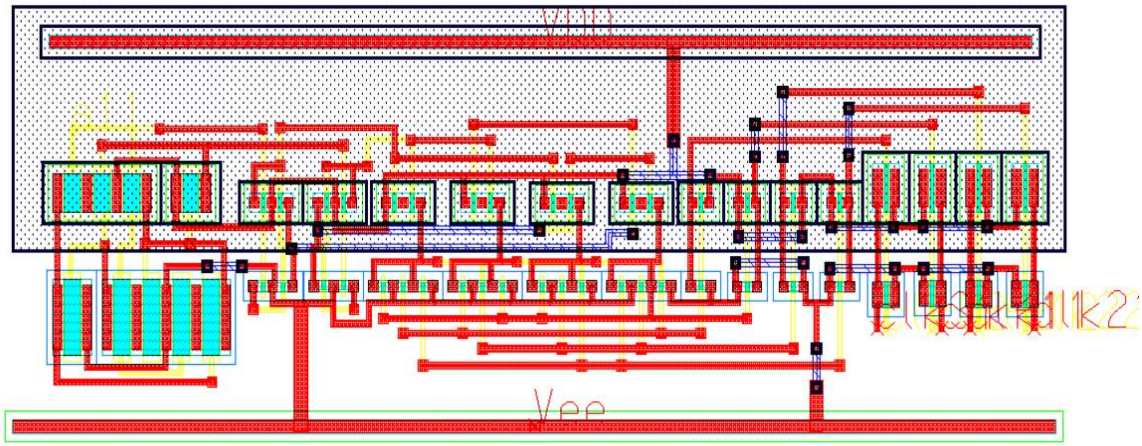


Figure A.3. Layout of complete switching clock generator circuit.

A.3. Current Biasing Circuit

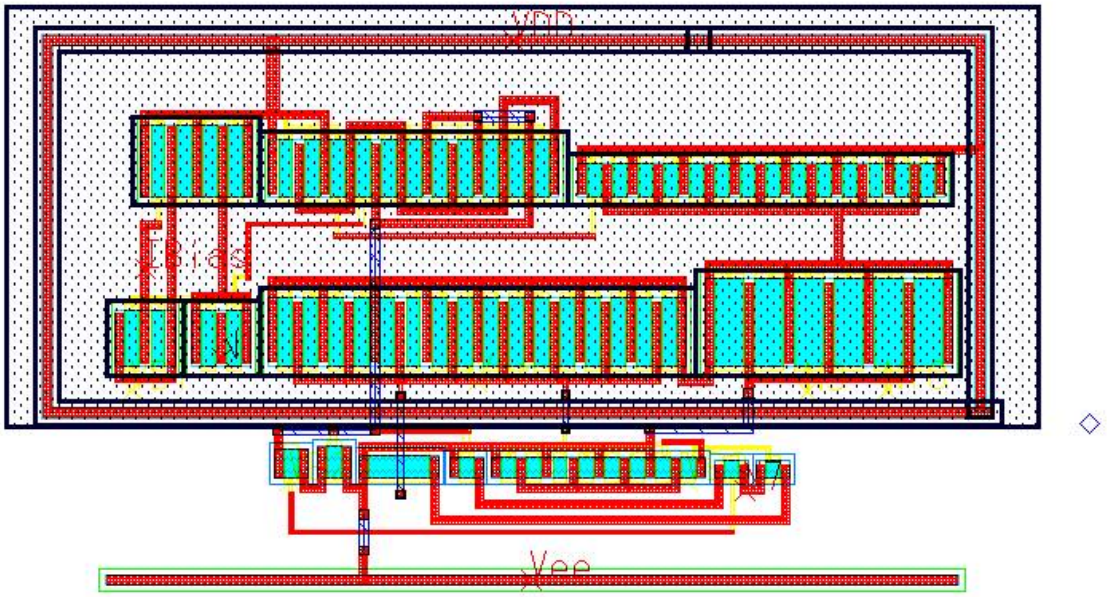


Figure A.4. Layout of current biasing circuit.

A.4. Current to Voltage Converter

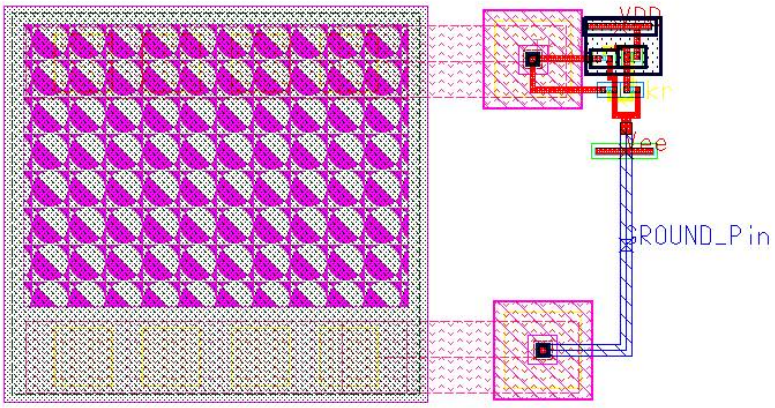


Figure A.5. Layout of current to voltage converter circuit.

A.5. Differential Voltage Amplifier

A.5.1. First Stage Amplifier

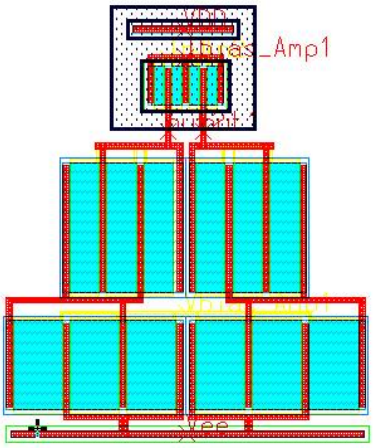


Figure A.6. Layout of first stage amplifier.

A.5.2. Second Stage Amplifier

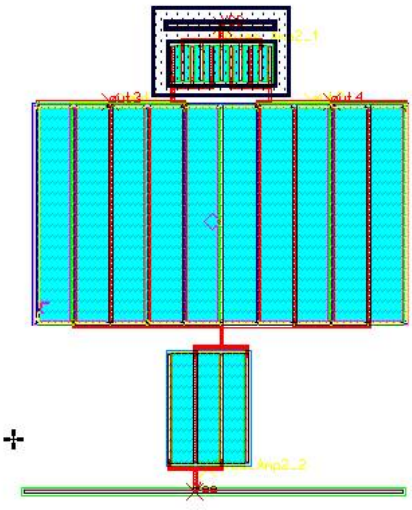


Figure A.7. Layout of second stage amplifier.

A.6. Whole Proposed Circuit Surrounding Hall Plates

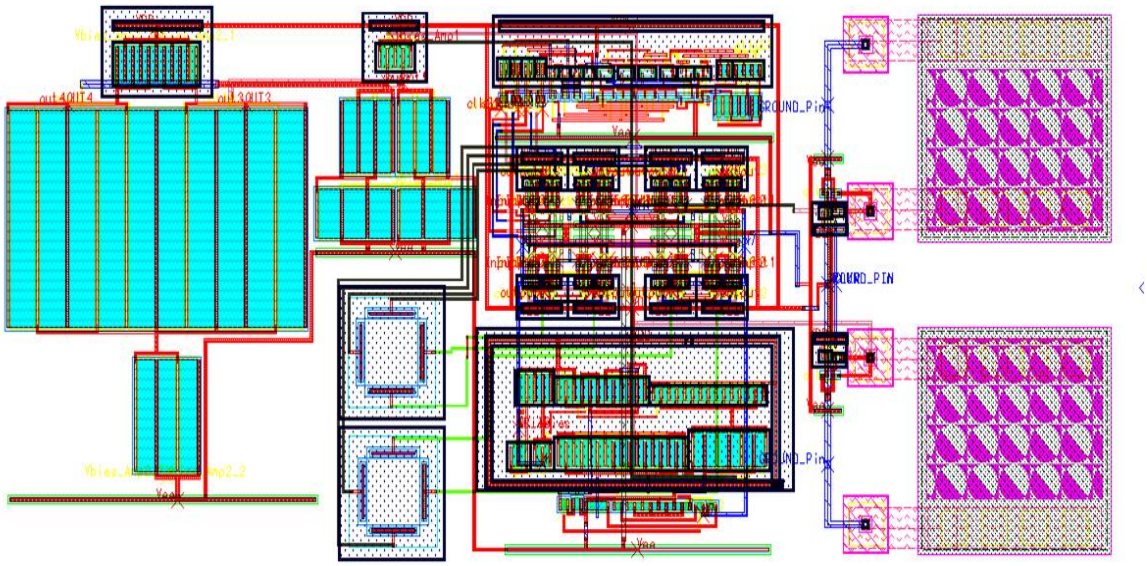


Figure A.8. Layout of circuit blocks surrounding Hall plates.

REFERENCES

1. Vanha, R. S., F. Kroener, T. Olbrich, R. Baresch and H. Baltes, "Trench-Hall Devices", *IEEE Journal of Microelectromechanical Systems*, Vol. 9, No. 1, pp. 82–87, 2000.

2. Hierold, C., "Intelligent CMOS Sensors", *The Thirteenth Annual International Conference on Micro Electro Mechanical Systems*, pp. 1–6, 2000.

3. Khoshnoud, F. and C. W. de Silva, "Recent Advances in MEMS Sensor Technology- Biomedical Applications", *IEEE Instrumentation and Measurement Magazine*, Vol. 15, No. 1, pp. 8–14, 2012.

4. Ibrahim, A., *Remotely Interrogated MEMS Pressure Sensor*, Ph.D. Thesis, University of Glasgow, 2011.

5. Hsur, T. R., *MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering*, McGraw-Hill, Inc., New York, NY, USA, 2008.

6. Madou, M. J., *Fundamentals of Microfabrication: The Science of Miniaturization*, CRC Press, Inc., CRC Press, FL, USA, 2002.

7. Mora, J., A. Diez, J. L. Cruz and M. V. Andres, "A Magnetostrictive Sensor Interrogated by Fiber Gratings for DC-Current and Temperature Discrimination", *IEEE Sensors Journal*, Vol. 12, No. 12, pp. 1680 – 1682, 2000.

8. Anwarza, B., A. Dubcek and Z. Figura, "Magnetostrictive Sensors in Mechatronics", *13th International Symposium MECHATRONIKA*, pp. 71–73, 2010.

9. Battini, F., M. Tonarelli and L. F. M. D. M. A.Giambastiani, "Experiencing With AMR Sensor Conditioning in Automotive Field", *Research in Microelectronics and Electronics Conference*, pp. 205–208, 2007.

10. Zheng, W., C. Xiaoming and H. Wakiwaka, "Study on Impulse Magnetic Field of Magnetostrictive Position Sensor", *2nd International Workshop on Intelligent Systems and Applications (ISA)*, pp. 1–4, 2010.

11. Edwards, D. M. and J. M. R. B. Muniz, "A Resistor Network Theory of the Giant Magnetoresistance in Magnetic Superlattices", *IEEE Transactions on Magnetics*, Vol. 27, No. 4, pp. 3548 – 3552, 2003.

12. Ono, H., M. Sakurai and K. Yoshida, "Read Response of a GMR Sensor Investigated With a Micromagnetic Model", *IEEE Transactions on Magnetics*, Vol. 41, No. 10, pp. 3088 – 3090, 2005.

13. MICRO SWITCH Sensing and Control, "Hall Effect Sensing and Application", 2004, `http://www.sensing.honeywell.com/hallbook.pdf`, [Accessed August 2015].

14. Heidari, H., E. Bonizzoni, U. Gatti and F. Maloberti, "A Current-Mode CMOS Integrated Microsystem forCurrent Spinning Magnetic Hall Sensors", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 678–681, 2014.

15. Wang, P. and Q. Liu, *Biomedical Sensors and Measurement*, Zhejiang University Press, Hangzhou, China, 2011.

16. Popovic, R., *Hall Effect Devices*, Academic Press, Inc., London, UK, 2003.

17. Ramsden, E., *Hall-Effect Sensors: Theory and Application*, Elsevier, Oxford, UK, 2006.

18. Dolgiy, L., I. Lovshenko, V. Nelayev, I. Shelibak, L. Dolgiy and I. Lovshenko, "Hall Sensor Based System for Detection of Adiponectin Protein", *5th International Conference on Bioinformatics and Biomedical Engineering, (iCBBE)*, pp. 1–4, 2011.

19. Crescentini, M., A. Romani and E. Sangiorgi, "Physical Simulations of Response Time in Hall Sensor Devices", *15th International Conference on Ultimate Integration on Silicon (ULIS)*, pp. 7–9, 2014.

20. Ajbl, A., M. Pastre and M. Kayal, "A Fully Integrated Hall Sensor Microsystem with Current-Mode Output", *18th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 464–467, 2011.

21. Heidari, H., U. Gatti, E. Bonizzoni and F. Maloberti, "Low-Noise Low-Offset Current-Mode Hall Sensors", *9th Conference on Ph.D. Research in Microelectronics and Electronics)*, pp. 325–328, 2013.

22. Dolgiy, L., I. Lovshenko, V. Nelayev, I. Shelibak, L. Dolgiy and I. Lovshenko, "Technology and Device Design and Optimization for the MOSFET Hall Sensor on SOI Structure", *Proceedings of the 19th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, pp. 398–400, 2012.

23. Janković, N., S. Aleksić and D. Pantić, "Simulation and Modeling of Integrated Hall Sensor Devices", *Proceedings of Small Systems Simulation Symposium*, 2012.

24. Bilotti, A., G. Monreal and R. Vig, "Monolithic Magnetic Hall Sensor Using Dynamic Quadrature Offset Cancellation", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 6, pp. 829–836, 2002.

25. Yin, S. B. S. and A. Bakker, "Spinning Current Hall Plate With Integrated Switches", *Proceedings of the ProRISC Workshop on Circuits, Systems and Signal Processing*, pp. 37–41, 1997.

26. Cesaretti, J. M., *Mechanical Stress and Stress Sompensation in Hall Sensors*, Master's Thesis, Georgia Institute of Technology, 2008.

27. Weiss, H., *Structure and Application of Galvanometric Devices*, Pergamon Press Ltd., Pergamon, Oxford, UK, 1969.

28. Steiner, R., A. Haberli, E.-P. Steiner and H. Baltes, "Offset Reduction in Hall Devices by Continuous Spinning Current Method", *International Conference on Solid State Sensors and Actuators*, pp. 381–384, 1997.

29. Udo, A., "Limits of Offset Cancellation by the Principle of Spinning Current Hall Probe", *Proceedings of IEEE Sensors*, pp. 1117–1120, 2004.

30. Xu, Y. and H. B. Pan, "An Improved Equivalent Simulation Model for CMOS Integrated Hall Plates", *Journal of Sensors (Basel)*, Vol. 11, No. 6, pp. 6284–6296, 2011.

31. Heidari, H., E. Bonizzoni, U. Gatt and F. Maloberti, "A CMOS Current-Mode Magnetic Hall Sensor With Integrated Front-End", *IEEE Transactions on Circuits and Systems I*, Vol. 62, No. 5, pp. 1270–1278, 2015.

32. J.Jiang, K.A.A.Makinwa and W.J.Kindti, "A Continuous-Time Ripple Reduction Technique for Spinning-Current Hall Sensors", *IEEE Journal of Solid-State Circuits*, Vol. 49, No. 7, pp. 1525 – 1534, 2014.

33. Ramirez, J. and F. Fruett, "Offset Reduction in a Multiple Terminal Hall Plate Ssing Current Spinning", *9th Ibero-American Congress on Sensors (IBERSENSOR)*, pp. 1–4, 2014.