TESTS OF THE FRONT-END ELECTRONICS FOR THE PHASE-I UPGRADE OF THE CMS-HB CALORIMETER

by

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ABSTRACT

TESTS OF THE FRONT-END ELECTRONICS FOR THE PHASE-I UPGRADE OF THE CMS-HB CALORIMETER

The Phase-I Upgrade of the CMS HB calorimeter is going to be implemented during the long shutdown 2 (LS2) for it to be ready for the second decade of LHC operations which aims to increase luminosity by an order of magnitude above its present value. The major component of this upgrade is the replacement of the current photo-detector HPDs, which have more noise due to electric discharges in the presence of a magnetic field, with SiPMs. SiPMs offer more data channels in the same physical space and are not sensitive to magnetic field preventing anomalous signals. This increase in data channels necessitates an upgrade for each component of the front end electronics of the HB. The work reported on this thesis focuses on the production testing and assembly of one of these front end components called new generation clock and control module.

ÖZET

CMS HB KALORİMETRESİNİN ÖN UÇ ELEKTRONİKLERİNİN 1. AŞAMA GÜNCELLEMELERİ KAPSAMINDAKİ ÜRETİM TESTLERİ

CMS HB kalorimetresinin 1. aşama güncellemesi Büyük Hadron Çarpıştırıcısının ışıklılık artışıyla uyumlu olması amacıyla 2. uzun ara süresinde gerçekleştirilecektir. Bu güncelleme kapsamında HB kalorimetresinin mevcut fotodetektörü olan hibrit fotodiyotlar silikon fotoçoğaltıcılar ile değiştirilecektir. Hibrit fotodiyotların manyetik alan varlığında elektriksel boşalım yapmasından kaynaklanan gürültüyü ortadan kaldırmak amacı ile mantetik alandan etkilenmeyen silikon fotoçoğaltıcılar seçilmiştir. Ayrıca hibrit fotodiyotların kapladığı fiziksel alana hibrit fotodiyotlardan çok daha fazla veri kanalı sığdırabilmektedirler. Silikon fotoçoğaltıcılarla birlikte artan veri kanalları, HB kalorimetresi üzerinde bulunan ön uç elektronik elemanlarının da güncelenmesini gerektirmektedir. Bu tezde, ön uç elektronik elemanlarından biri olan yeni nesil clock ve kontrol modülünün 1. aşama güncellemesi kapmasındaki üretim testleri anlatılmaktadır.

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LIST OF SYMBOLS

GeV	Giga electron-volt
Gbps	Gigabit per second
kpbs	Kilobit per second
MeV	Mega electron-volt
MHz	Megahertz
ns	Nanosecond
T	Tesla
TeV	Tera electron-volt
η	Pseudorapidity
θ	Polar angle
ϕ	Azimuthal angle
μm	Micrometer

LIST OF ACRONYMS/ABBREVIATIONS

ADC	Analog to Digital Converter
ALICE	A Large Ion Collider Experiment
AMC	Advanced Mezzanine Card
ATLAS	A Toroidal LHC ApparatuS
APD	Avalanche PhotoDiode
ASIC	Application Specific Integrated Circuit
BE	Backend
B2B	Board-to-Board
CMS	Compact Muon Solenoid
CU	Calibration Unit
DAQ	Data Acquisition
DCC	Data Concentration Cards
ECAL	Electromagnetic Calorimeter
FE	Frontend
FEC	Frontend Controller
FEE	Frontend Electronics
FPGA	Field Programmable Gate Array
GBT	Gigabit Transceiver
GLIB	Gigabit Link Interface Board
GOL	Gigabit Optical Link
HB	Hadron Barrel Calorimeter
HE	Hadron Endcap Calorimeter
HF	Hadron Forward Calorimeter
HO	Hadron Outer Calorimeter
HCAL	Hadron Calorimeter
HPD	Hybrid Photodiode
LEP	Large Electron-Positron Collider
LHC	Large Hadron Collider

LHCb	LHC Beauty
L1A	Level 1 Accept
MCLK	Master Clock
MM	Multimode
ngCCM	New Generation Clock and Control Module
ngFEC	New Generation Frontend Controller
ODU	Optical Decoder Unit
PCB	Printed Circuit Board
PMT	Photomultiplier Tube
PRBS	Pseudo-Random Binary Sequence
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster
QIE	Charge Integrator and Enumerator
RBX	Readout Box
REFCLK	Reference Clock
RF	Radio Frequency
RM	Readout Module
RS	Reed-Solomon Decode
SM	Single Mode
SFP	Single Form-factor Pluggable
SiPM	Silicon Photomultiplier
SPS	Super Proton Synchrotron
TTC	Timing, Trigger and Control System
TDC	Time to Digital Converter
WLS	Wavelength Shifting Fibers
WTE	Warning-Test-Enable
μHTR	Micro HCAL Trigger Readout
μTCA	Micro Telecommunications Computing Architecture
VTRx	Versatile Transceiver

1. INTRODUCTION

Operating at the center of mass energy of 13 TeV and luminosity of 10^{34} cm^{-2} s^{-1}, The Large Hadron Collider (LHC) is the world's largest and most powerful particle accelerator and the most complex scientific instrument ever built. Located at one of the four collision points around the accelerator ring, the Compact Muon Solenoid (CMS) is one of the two general-purpose particle detectors and built to investigate a broad range of physical phenomena, including the Higgs Boson, extra dimensions, and dark matter.

The Hadron Calorimeter (HCAL) is a sampling calorimeter dedicated to the detection of hadrons and is composed of layers of brass and plastic scintillators. The Hadron Barrel Calorimeter (HB) covers the pseudorapidity region $|\eta| < 1.3$ and consists of 36 azimuthal wedges, where each wedge contains one readout box (RBX). With the Phase-I Upgrade of photodetectors used in HB, from HPD to SiPM, a new version/generation for each of the current elements of the readout box was designed. The focus of this thesis is the assembly and testing of the new generation Clock and Control Modules (ngCCM) which are housed in readout boxes (RBXs) and are responsible for controlling the readout of all the channels from each wedge and the distribution of the LHC Clock signal.

The second chapter of this thesis contains brief information about the LHC, the chapter after that summarizes the CMS; the detector and its subsystems. The fourth chapter focuses on the HCAL and gives detailed information about the HB. The next chapter summarizes the Phase-I Upgrade of the HCAL and then moves into details for the Phase-I Upgrade of the HB. The last two chapters cover the statistics of the work done and the conclusion, respectively.

2. THE LARGE HADRON COLLIDER

The Large Hadron Collider is so far the world's most powerful particle accelerator and collider and lies in a tunnel beneath the Franco-Swiss border near Geneva (Figure 2.1). Having a circumference of 27 km, LHC re-uses the tunnel that was built for the previous machine, the Large Electron Positron Collider (LEP). Even before LEP started running, scientists started thinking about the LHC in the early 1980s and its construction was officially approved in 1994. [1]

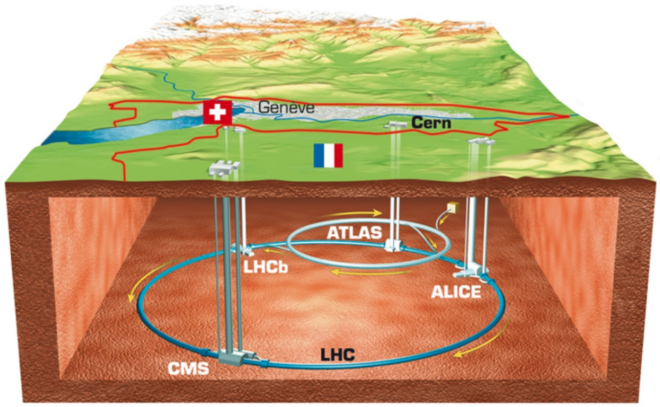

Figure 2.1. An illustration of the LHC ring located beneath Franco-Swiss Border.

LEP was limited because the energy loss of the electrons due to synchrotron radiation is large. Under this limitation, LEP could maximally reach an energy of 209 GeV. However the LHC currently reaches a center of mass collision energy of 13 TeV, since the energy loss of hadrons caused by synchrotron radiation is much lower than that of the lighter particles such as electrons and positrons.

Along with its prime motivation, i.e., search for the Higgs Boson, LHC was also designed to investigate the Charge-Parity Violation, Supersymmetry, Dark Matter and Dark Energy, Antimatter, and the state of matter that existed in the early Universe called Quark-Gluon Plasma.

2.1. Design

LHC is a two-ring superconducting hadron accelerator and collider re-using the existing 27 km long tunnel first used by the previous collider LEP. The tunnels are at a mean depth of 100 m and on a plane tilted with 1.4% slope towards Lake Geneva. The depth is around 175 m under the Jura mountains and 50 m towards Lake Geneva. Re-using the existing tunnels from the LEP was approved because not only it would cost less but also the earth's crust would be a good shielding for the radiation produced.

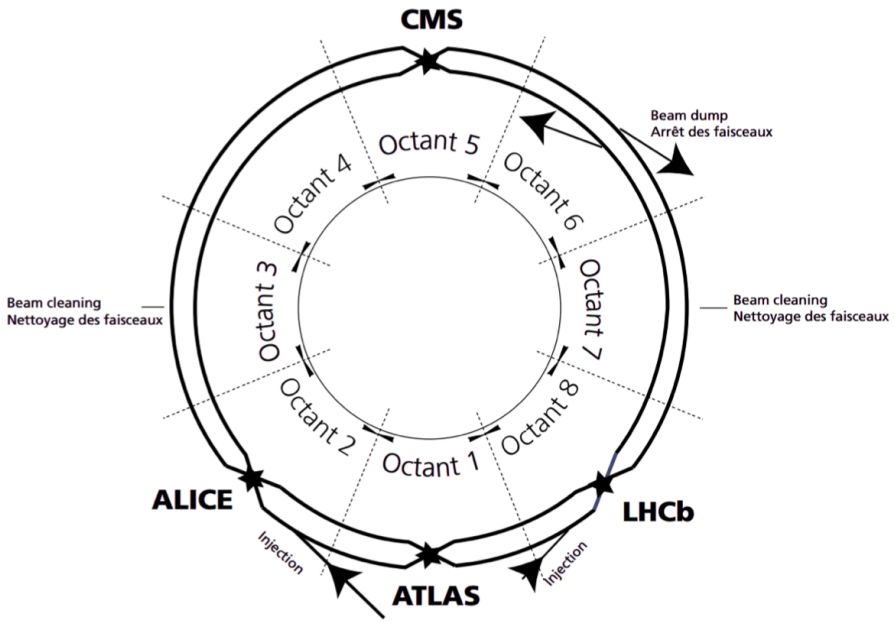

Figure 2.2. Schematics of the LHC layout.

The LHC is not a perfect circle with its arcs and straight sections and its basic layout follows the LEP tunnel geometry. It has eight arcs and eight insertions where insertion means a long straight section consisting of two transition regions. The octants shown in Figure 2.2 are regions that start from the middle of an arc and end in the middle of the following arc, hence spanning a full insertion. Each arc is 2.45 km long and each one contains 154 dipole bending magnets. Each insertion is 528 m long and the specific use of each insertion can be different, e.g. physics (beam collisions within an experiment), injection, beam dumping, beam cleaning. Of eight straight sections there are, only four are used and the remaining four are suppressed, i.e., the beams cross at only four of these sections. There are four experimental insertions for each of these

beam crossings which are the ATLAS experiment at Point 1, the CMS experiment, which is located diametrically opposite to the ATLAS experiment, at Point 5, the ALICE experiment at Point 2, and the LHCb experiment at Point 8. Point 2 and Point 8 also house the injection systems for Beam 1 and Beam 2, respectively. Point 3 and Point 7 include collimation systems; Point 6 contains the beam dump insertion, where the two beams are vertically extracted from the machine. [2]

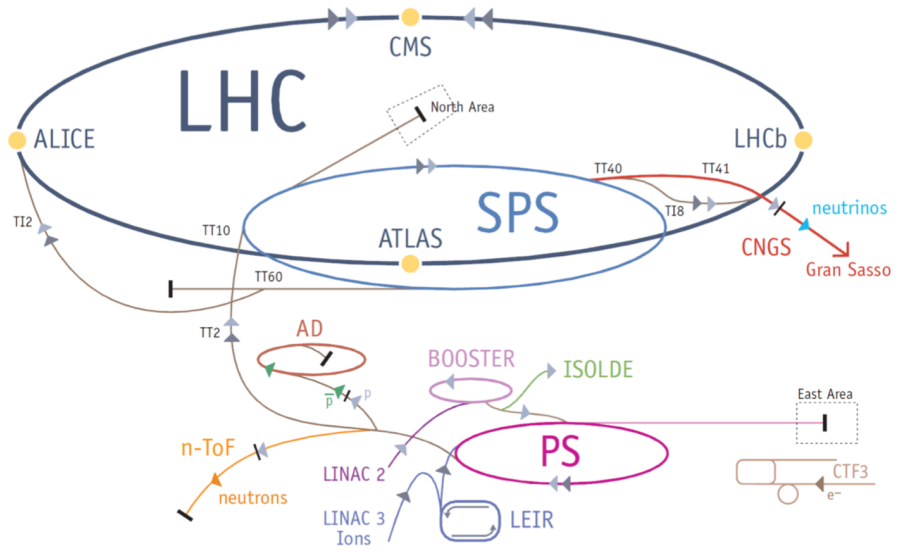

Figure 2.3. Schematics showing the accelerator complex.

The process of accelerating a proton to 0.999999991 times the speed of light is not done only by the LHC ring. The LHC itself is fed by a number of particle accelerators, working in sequence to achieve a final energy of 7 TeV (Figure 2.3). Starting with the extraction of protons from the gaseous hydrogen, these protons are first accelerated to 50 MeV in Linac 2 and then fed into the Booster, the first ring of the acceleration process. After the protons are accelerated to 1.4 GeV in the Booster, they are passed on to the Proton Synchrotron (PS) to be accelerated to 25 GeV. It is right here at the PS that the LHC bunch crossing frequency is set to 40 MHz (corresponding to 25 ns time spacing). The protons are then injected into the Super Proton Synchrotron (SPS) where they are accelerated to 450 GeV. The protons at 450 GeV are then injected into the LHC from the injection points at Octant 2 and Octant 8 and are then accelerated and kept at constant energy by the Radio Frequency cavities up to 6.5 TeV. While in the LHC, the beams are kept in circular orbits by the dipole magnets and are focused by

the quadrupole magnets. The two beams are then collided at the four interaction points corresponding to four experimental insertions, i.e., the four big experiments: ATLAS, CMS, ALICE, LHCb. There are three minor experiments installed at the LHC: the Large Hadron Collider forward (LHCf) experiment, the TOTal Elastic and diffractive cross section Measurement (TOTEM) experiment, and Monopole and Exotics Detector at the LHC (MoEDAL). [3]

2.2. The Detectors and Experiments of the LHC

There are a total of seven experiments installed at the LHC. ALICE, ATLAS, CMS and LHCb are major experiments installed in underground caverns built around the four collision points of the LHC beams. A Toroidal LHC ApparatuS (ATLAS) and the Compact Muon Solenoid (CMS) are general-purpose detectors designed to cover the widest possible range of physics at the LHC, from precision measurements of the Higgs boson to searches for new physics beyond the Standard Model. A Large Ion Collider Experiment (ALICE) is designed to investigate the state of matter that existed in the early Universe called Quark-Gluon Plasma. The Large Hadron Collider beauty (LHCb) experiment is designed to study the B-particles; events and interactions with b quark. The two minor experiments LHCf and TOTEM are forward detectors located near the collision points of ATLAS and CMS detectors, respectively. The third minor experiment MoEDAL is a detector located near the collision point of LHCb detector and is designed to investigate hypothetical particles.

3. THE COMPACT MUON SOLENOID

The Compact Muon Solenoid is a multi-purpose detector with physics motivations, including search for the Higgs Boson, which was discovered together with ATLAS, search for supersymmetric particles, search for new massive vector bosons, and search for extra dimensions. Weighing 12.5 tonnes and being 21.6 m long, 14.6 m high and 14.6 m wide, it is *compact*. With the intense bending power of the magnets which actually contain more iron than the Eiffel Tower, measuring the momentum of *muon*s with a higher precision was the driving force behind the detector design. This bending power, resulting from the 3.8 T magnetic field is provided by the superconducting *solenoid* magnet. [4]

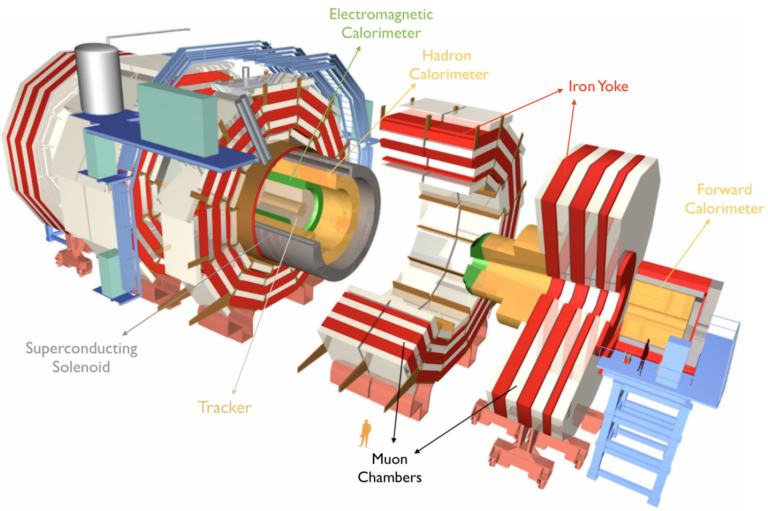

Figure 3.1. A three dimensional view of the CMS. [5]

Built around its central piece, the superconducting solenoid magnet, CMS has a cylindrical shape (Figure 3.1) with a symmetry in the azimuthal angle ϕ. The bore of the solenoid is large enough to accommodate the tracker and the calorimetry inside. Being the closest detector to the beam, trackers are surrounded by the Electromagnetic Calorimeter (ECAL), and ECAL is surrounded by the brass/scintillator sampling Hadron Calorimeter (HCAL). The iron return yoke interspersed with muon chambers are the outer layers positioned right after the solenoid. [6]

3.1. Coordinate conventions

Located at the north of the LHC center, CMS detector has the origin centered at the collision point (the small tilt of the LEP/LHC plane is neglected.) and uses a right-handed Cartesian coordinate system (Figure 3.2). The x-axis is horizontal, pointing radially inward toward the center of the LHC, the y-axis is vertical, pointing upward, and hence the z-axis points along the beam direction. Considering the cylindrical structure of the CMS, a polar coordinate system is used as well and it is defined such that the azimuthal angle ϕ is measured from the positive x-axis in the x-y plane (*the transverse plane*) and the radial coordinate in this plane is defined as r, the polar angle θ is measured from the z-axis in the r-z plane, and the pseudorapidity, which is a spatial coordinate calculated by using θ, is defined as $\eta = -\ln\tan(\theta/2)$.

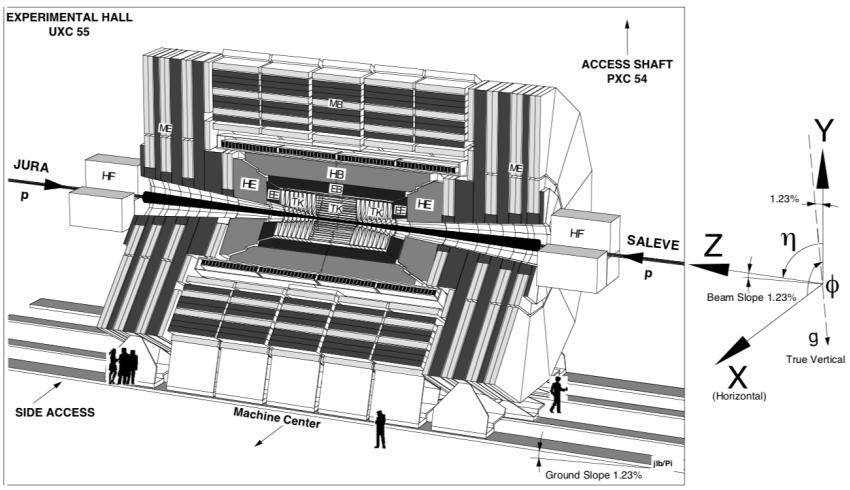

Figure 3.2. An overall view of the CMS.

3.2. Superconducting Solenoid Magnet

Yielding a magnetic field of 3.8 T over a length of 12.5 m and a free bore radius of 5.9 m, this large superconducting solenoid was the central feature of the CMS design, i.e., precise momentum measurement of charged particles while they escape from the interaction point by bending their track. It is made of superconducting Niobium Titanium *(NiTi)* wires, which are powered by an electrical current of 20,000 Amperes to reach the nominal magnetic field of 3.8 T. The 5.9 m radius is large enough to ac-

commodate the trackers (pixel tracker and silicon tracker), electromagnetic calorimeter and hadron calorimeter inside.

3.3. Tracker

The trajectory of a particle with a positive or negative charge is bent under the influence of magnetic field. (The bent tracks of the particles are then used in the calculation of the transverse momentum.) The tracker system was designed to provide a precise measurement of the bent trajectories of the particles (under the influence of the homogeneous magnetic field provided by the solenoid magnet) emerging from the LHC collisions as well as to reconstruct the secondary tracks of the charged particles produced in the decays of the primary particles inside the tracker volume. Surrounding the interaction point, it is the closest detector system to the collisions. It consists of two main parts, the vertex or pixel detector, and the Silicon Strip Tracker (SST).

Pixel Detector is the innermost detector sub-system, being the closest to the interaction region. It consists of three barrel layers and two endcap disks with 250 μm thin silicon pixel detectors with a pixel cell size of 100×150 μm^2 and it covers a pseudo-rapidity range of $-2.5< \eta <2.5$. The pixel detector is essential for the reconstruction of secondary vertices from b and tau decays.

Silicon Strip Tracker is made of silicon modules consisting of one or two silicon micro-strip sensors. The barrel region comprises ten layers; four layers of Tracker Inner Barrel (TIB) and six layers of Tracker Outer Barrel (TOB) with different thicknesses for the sensors, $320 \pm 20\mu$m for the TOB and 500 ± 20 μm for the TIB. The forward region consists of three Tracker Inner Disks (TID) on each side and is completed by the Tracker End Caps (TEC), comprising nine disks on each side. The thickness of the sensors is 320 ± 20 μm for the TID and the 3 innermost rings of the TEC and 500 ± 20 μm for the rest of the TEC. [7, 8]

3.4. Electromagnetic Calorimeter

As it is the case for most of the particle physics experiments, a distinction is made between electromagnetic calorimetry and hadron calorimetry (see Figure 3.3 for all the stages for the detections of particles). The electromagnetic calorimeter (ECAL) of the CMS, as the other electromagnetic calorimeters do, measures the energy of the particles that interact through the electromagnetic force, i.e., it is based on the production of electromagnetic showers. The ECAL is a hermetic homogeneous calorimeter made of lead tungstate ($PbWO_4$) and comes right after the trackers, consisting of two main parts; barrel and endcaps. The barrel part, comprising 61200 $PbWO_4$ crystals, covers the pseudorapidity range of $|\eta| < 1.479$. The endcaps, having 7324 $PbWO_4$ crystals mounted on each, cover the pseudorapidity range of $1.479 < |\eta| < 3$. The driving criteria in the design was the capability to measure the two-photon decay mode for $m_H \leq 150$ GeV and to measure the electrons and positrons from the decay of Ws and Zs originating from the $H \rightarrow ZZ^{(*)}$ and $H \rightarrow WW$ decay chain for 140 GeV $\leq m_H \leq$ 700 GeV. Since most of the energy from electrons or photons is deposited within

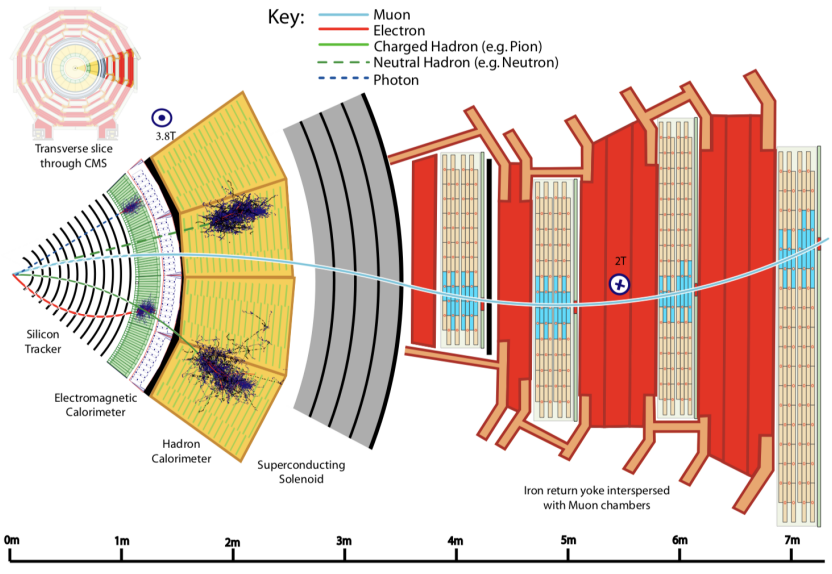

Figure 3.3. A sketch of the particle flow in a transverse slice of the CMS detector, from the beam interaction point to the muon detector.

the homogeneous crystal volume of the calorimeter, use of these homogeneous crystals helps achieve this capability. Not only achieve this capability, but also having short

radiation (0.89 cm) and Molière lengths (2.2 cm) and being fast (about 80% of the light is emitted from the crystals in 25 ns, which is the same as the LHC bunch crossing frequency) made it certain that the lead tungstate was the ideal choice for the design. The light pulses that are converted from electrons and photons are read out by the silicon photodiodes. Avalanche photodiodes (APDs) to collect the scintillation light are used in the barrel, and to survive a much higher radiation dose and neutron fluence vacuum phototriodes (VPTs) are used in the endcap regions. [9]

3.5. Hadron Calorimeter

Located right after the ECAL and surrounding it, HCAL is a sampling calorimeter and is responsible for the measurement of the energies of hadrons escaping from the LHC collisions. This calorimeter will be explained in detail in the next chapter.

3.6. Muon System

Muon detection is the most powerful tool to detect interesting events over the background since they are less affected than electrons by radiative losses in the tracker material, e.g., a "gold plated" signal of the Higgs boson is its decay into four leptons, of which the best resolution is achieved if the leptons are muons ($H \rightarrow ZZ^{(*)} \rightarrow 4\mu$). Positioned right after the solenoid magnet, muon system in the CMS is the outermost detector system and is expected to perform three major tasks; muon identification (the central theme and the middle name of the experiment), muon triggering, and momentum measurement via the three types of gaseous detectors; drift tubes (DT) in the barrel region, cathode strip chambers (CSC) in the endcap region, and resistive plate chambers (RPC) in both the barrel and endcap. The solenoid magnet and the return yokes help ensure the performance of these tasks. Interspersed with the iron return yokes, the muon detectors obey the cylindrical geometry of the solenoid magnet, hence comprising a barrel region and planar endcaps. The barrel region, covering the pseudorapidity region $|\eta| < 1.3$, consists of four muon stations, MB1 to MB4, of 250 chambers. The endcaps also have four stations, ME1 to ME4, and cover the pseudorapidity region $|\eta| < 2.4$. [10, 11]

4. HADRON CALORIMETER

4.1. Calorimetry as a Detection Principle

Originally invented for the cosmic-ray phenomena, calorimetry was developed and perfected for accelerator-based particle physics and it is now a very advantageous method for particle detection. This technique is very advantageous over others by being sensitive to both charged and neutral particles, having high granularity, having good and easy particle identification, and not needing a magnetic field (in contrast with magnetic spectrometers). Calorimeters are blocks of material in which the particles get absorbed and some fraction of their energy gets transformed into a measurable signal in the form of light or electric charge. They can be classified either by their construction method or by their purpose of use. The former classification is made by the medium used in calorimetry. If a single medium is used throughout the calorimeter, serving both as absorber and detector, they are called homogeneous calorimeters. On the other hand, having an alternating medium is classified as heterogeneous or *sampling* calorimeter and it has alternating layers of passive absorbers and active detectors. The latter classification, dividing the calorimeters into two as electromagnetic and hadron calorimeters, is made by the particles they detect. Electromagnetic calorimeters are used to measure the energy of the electrons and photons through their electromagnetic interactions and hadron calorimeters are used to measure the energy of hadrons through their strong and electromagnetic interactions. The detection principle used in calorimeters is mainly ionization and excitation of the calorimeter medium. The photodetectors or anodes/diodes detects the photons emitted by scintillation or electrons released by the ionization. The focus of this thesis, the hadron calorimeter, is of the second kind of the first classification, i.e. it is a sampling calorimeter and will be explained in the following section. [12, 13]

4.2. Design

Surrounding the electromagnetic calorimeter (ECAL), HCAL is a sampling hermetic calorimeter designed to measure the timing and energy of hadronic showers. In accordance with the CMS geometry, HCAL consists of a central barrel region and two endcap disks.

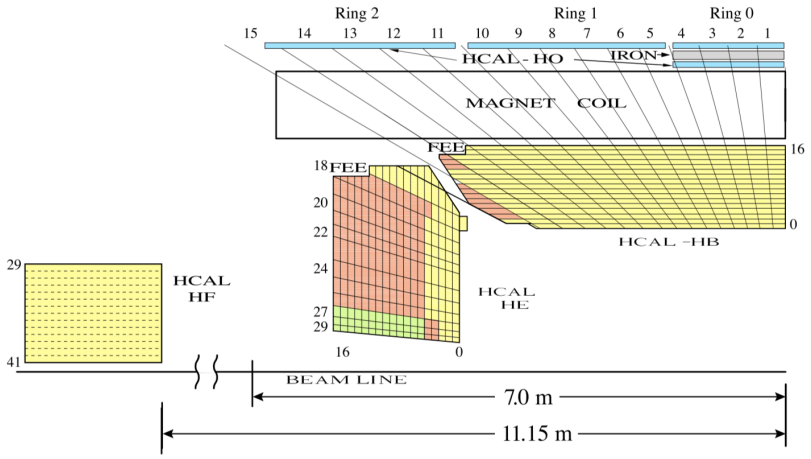

Figure 4.1. A quarter slice of the CMS HCAL detectors. The right end of the beam line is the interaction point. FEE denotes the location of the Front End Electronics for the barrel and the endcap. In the diagram, the numbers on the top and left refer to segments in η, and the numbers on the right and the bottom refer to scintillator layers. [14]

As shown in Figure 4.1, the HCAL is organised into a central barrel, comprising the Outer (HO) and Barrel (HB), endcap (HE), and forward (HF) sections. The barrel and endcaps are positioned such that they are the last layer of subsystems put inside the magnet, coming after the electromagnetic calorimeter and the tracker as seen from the collision point. The barrel is restricted by the inner extent of the magnet coil from above and by the outer extent of the electromagnetic calorimeter from below which in turn leaves the possibility of some particles escaping from HB, and hence HO is positioned right after the magnet coil, complementing the barrel and ensuring no energy leaks left undetected. The forward sections (HF) are positioned relatively farther from the interaction point and is designed to detect particles escaping from the collision point at low angles relative to the beam line [15, 16].

4.3. Subsystems

Hadron Outer is an additional layer of scintillators placed outside of the solenoid magnet, as the first layer of each of the five iron yoke rings to ensure that the perfect absorption/containment of the hadronic showers. The rings are numbered starting from the central ring, naming it ring 0. The remaining four are numbered $\pm$ 1 and $\pm$ 2 and the numbering increases with z. The central ring has two layers of HO scintillators and all other rings have only one layer of scintillator. Specifically designed to account for identifying late starting showers and measuring their energy, HO covers the pseudorapidity range of $|\eta| < 1.3$. Out of 9072 readout channels of HCAL, HO contributes 2160 channels where the readout signal is acquired from the collection of the scintillation light by wavelength shifting (WLS) fibers and then their transfer to hybrid photodiodes (HPD).

Hadron Endcap consists of two disks, endcap minus (HEM) and endcap plus (HEP), inserted into the ends of the solenoid magnet (attached to the muon endcap yoke), hence made of non-magnetic material, covering the pseudorapidity region 1.3 $|\eta| < 3$. HE approximately contains about 34% of the particles produced in the final state. As in HB, HE is made of 18 wedges on each side and is composed of brass absorber plates and active plastic scintillating tiles. Of 9072 readout channels of HCAL, 2592 channels (exactly the same number of channels that HB contributes) belongs to HE. Again identical to HB, the scintillation light from the tiles are collected by WLS and read out by hybrid photodiodes (HPD).

Hadron Forward calorimeters are cylindrical steel structures installed outside of the muon endcap yokes. They are azimuthally subdivided into 18 wedges on each side, and are embedded with radiation hard quartz fibers. HF differs from the rest of the HCAL with quartz fibers producing and collecting the Cherenkov light and photomultiplier tubes (PMT) forming the readout. Out of 9072 readout channels, HF contributes 1728 channels. The pseudorapidity region covered by HF is rather wide and is $3.0 < |\eta| < 5.0$.

5. HADRON BARREL CALORIMETER

Hadron Barrel Calorimeter is a heterogeneous sampling calorimeter, meaning it consists of alternating layers of absorbers and scintillators, and covers the pseudorapidity range of -1.3 $< \eta <$ 1.3. Surrounding the lead tungstate electromagnetic barrel (EB), it is formed by two half barrels and is cylindrically symmetric. Each half barrel holds 18 wedges having a segmentation $\Delta\phi = 20°$. The wedge consists of layers of copper alloy absorber plates and each plate accommodates 9 mm wide slots for the scintillator trays (See Figure 5.1 for the design (left) and a picture (right) of a wedge).

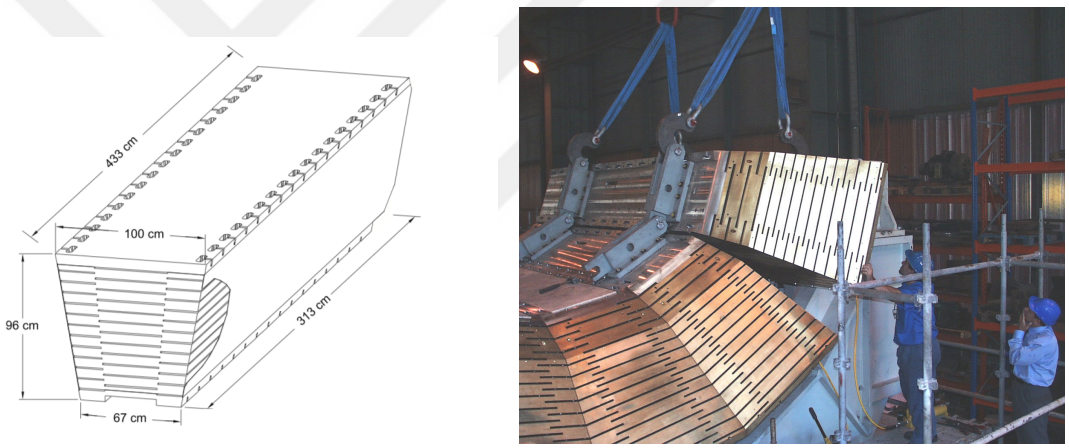

Figure 5.1. The design (left) and assembly (right) of a wedge.

Absorber plates are made of a copper alloy composing 70% Cu and 30% Zn known as C26000/cartridge brass with a density of 8.83 g/cm^3, radiation length of 1.49 cm, and nuclear interaction length of 16.42 cm. 31 of these brass plates are bolted together, forming the body of a wedge. Stainless steel plates are used for the bottom and top of these 31 plates to finalize one wedge and to ensure structural strength. Each wedge is further segmented into four azimuthal sectors, $\Delta\phi = 5°$, forming slots for scintillator trays. Each wedge weighs 27 tonnes and each have 16 layers of absorber plates. The first and last steel layers are 40 mm and 75 mm thick, respectively. The first layer is followed by eight brass plates, 50.5 mm thick each, which are then followed by six layers of 56.5 mm thick brass [6], [15].

Scintillators are transparent materials that exhibit scintillation, i.e. when struck by an incoming particle/radiation, they emit the absorbed energy as a flash of light. The scintillator type used in the HB is Kuraray SCSN81 plastic scintillator, chosen for its long-term stability and acceptable radiation hardness. To better organize the large number of tiles, 70.000 overall, they are grouped into trays. Each tray is installed on the azimuthal slots on the wedges, ϕ-index 2 and 3 being the central slots and ϕ-index 1 and 4 being the edge slots. There are a total of 17 layers of scintillators on the HB, each having 108 trays. The first layer is located in front of the front steel plate and is made of 9 mm thick Bicron BC408. The remaining 16 layers are made of Kuraray SCSN81 but have different thicknesses. Layers 1 to 15 have a thickness of 3.7 mm and the last layer has a thickness of 9 mm as well. The first and last layers are responsible for the early developing showers (between EB and HB) and late developing showers leaking out the back of the HB, respectively.

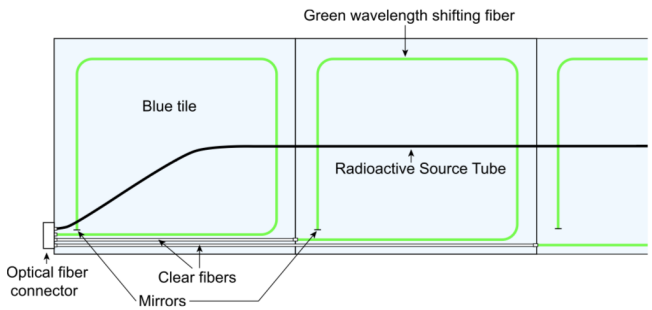

Figure 5.2. Schematics showing the components of a scintillator tray.

As shown in Figure 5.2, the components of a scintillator tray are the wavelength shifting fibers (WLS), radioactive source tube, clear fibers, and optical fiber connector. Each tray is made of individual scintillators with white painted edges wrapped in Tyvek 1073D sheets which are attached to a 5-mm thick plastic substrate with plastic rivets [15]. 0.94-mm-diameter green double-cladded WLS fibers are placed in machined grooves on tiles. 1 mm thick stainless steel radioactive source tubes are placed on each tray for calibration purposes. The WLS fibers are mirrored at one end and are attached with clear fibers at the other end so that the connection to the optical connector is made and the transfer of light to the optical units is ensured. As seen in Figure 4.1, there are 16 η divisions for the scintillator in the r-z plane, 16th overlapping HE endcap. This division then results in a segmentation of $(\Delta\eta, \Delta\phi) = (0.087, 0.087)$ for the scintillator

tiles (the tower segmentation for HB is given in Table 5.1). The wedges composing the absorber plates and the plastic scintillators are then bolted together in a hermetic way such that the gap between the wedges is smaller than 2 mm (See Figure 5.3). The numbering of the wedges is done counter clockwise, starting from the central left wedge (see Figure 5.4)

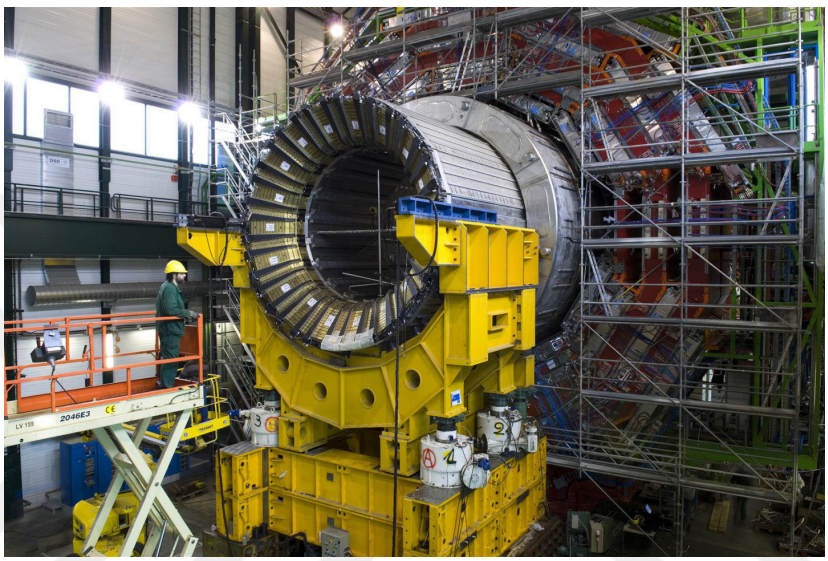

Figure 5.3. Picture showing the insertion of an assembled half-barrel into the superconducting solenoid magnet.

The barrel calorimeter is segmented into two radial compartments each consisting of 18 wedges. HB1 comprises 30 mm thick copper absorber plates and 10 sampling layers and HB2 comprises 59 mm thick copper absorber plates and 9 sampling layers, which add up to a total of 19 sampling layers for the barrel calorimeter.

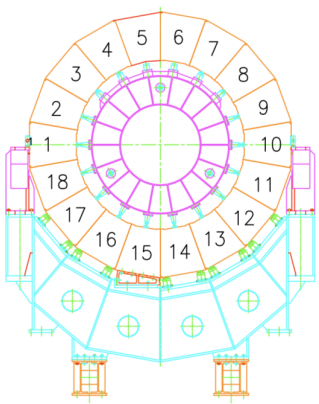

Figure 5.4. Schematics showing the numbering of the HB wedges.

5.1. Optics

To organize the large number of tiles, they are grouped into scintillator trays or megatiles, which are partially shown in Figure 5.2. The optical system is mainly driven by the WLS fibers (Kuraray Y-11, double-clad) and optical decoder units. Scintillating tiles are first read out by WLS fibers, which are attached to clear fibers by splicers (see Figure 5.5). The collected light is guided out by clear fibers to the optical fiber connector which is then connected to an optical decoder unit (ODU), and hence to the front-end electronics, by the optical fibers. (The details of the front-end electronics are given in the next section.)

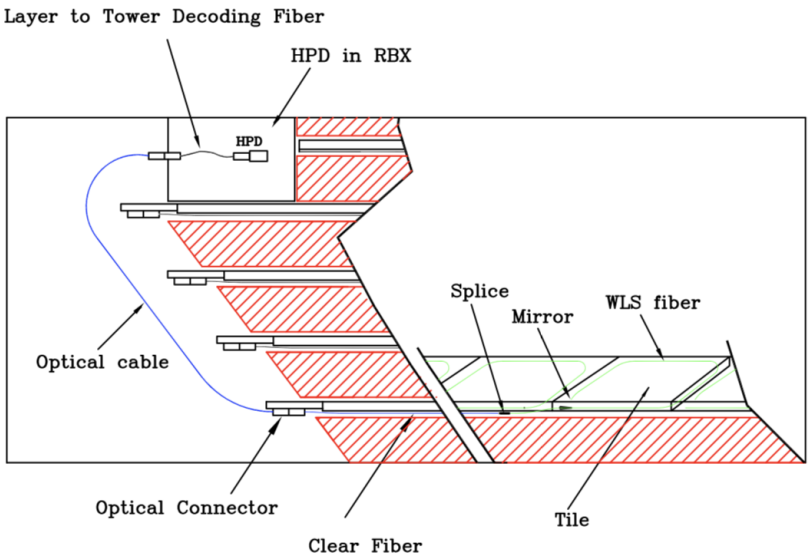

Figure 5.5. A schematic view of the HB optics.

The splicer used for the connection of WLS fibers to clear fibers was specifically designed for this task and the light transmission across the splice is 92.6% with an *rms* of 1.8%. The optical cables from each layer are organized into bundles and cables corresponding to a calorimeter tower are mapped via ODU to the individual pixels on hybrid photodiodes (HPD). The HPD is a vacuum device consisting of a photocathode which absorbs photons and emits photoelectrons and is held at a high voltage of 8 kV and a silicon photodiode standing $\sim$ 3 mm away from the photocathode. The accelerated photoelectrons ionizes the silicon which in turn results in a gain of the

device, of approximately 2000. A single HPD contains 19 hexagonal pixels which are 20 mm^2 wide and each HPD is fed an additional fiber for the injection and the distribution of LED (light emitting diode) or laser light for calibration and monitoring purposes.

5.2. Electronics and Data Acquisition

The Barrel Calorimeter (HB) is a scintillator sampling calorimeter composed of 36 wedges, each wedge containing 72 readout channels and hence comprising a total of 2592 readout channels. The layers of each wedge is embedded with WLS fibers which are optically bundled together to form towers (see Table 5.1). The overall readout circuitry

Table 5.1. Tower data for HB.

Tower Number	$\lvert\eta_{range}\rvert$	Thickness (λ_I)	ϕ
1	0.000 - 0.087	5.39	5°
2	0.087 - 0.174	5.43	5°
3	0.174 - 0.261	5.51	5°
4	0.261 - 0.348	5.63	5°
5	0.348 - 0.435	5.80	5°
6	0.435 - 0.522	6.01	5°
7	0.522 - 0.609	6.26	5°
8	0.609 - 0.696	6.57	5°
9	0.696 - 0.783	6.92	5°
10	0.783 - 0.870	7.32	5°
11	0.870 - 0.957	7.79	5°
12	0.957 - 1.044	8.30	5°
13	1.044 - 1.131	8.89	5°
14	1.131 - 1.218	9.54	5°
15	1.218 - 1.305	10.3	5°
16	1.305 - 1.392	overlaps HE	5°

of the barrel calorimeter is divided into two sets of Front-End Electronics, sitting on the detector and operating in a 3.8 T magnetic field environment, mounted on each wedge

near tower 14 and Back-End Electronics. The front-end circuits are held in an enclosure named readout box (RBX) which houses 4 readout modules (RMs), a calibration unit (CU), and a clock and control module (CCM). Each readout module contains an optical decoder unit (ODU), a 19-channel photodetector (HPD), and three custom readout cards operating at 40 MHz, which is the LHC bunch crossing frequency. The data flow starts from the collection of the scintillation light by WLS fibers which is then transferred to ODU where the optical fibers together with their signals are arranged into readout towers and the light signal from each individual $(\Delta\eta, \Delta\phi) = (0.087, 0.087)$ tower is registered to HPDs. After the transferred light is gone through the HPD and hence lead to a gain of about 2000, the HPD signals are further fed into the six-channel custom readout cards called charge integrator and encoder (QIE). QIE cards are custom flash ADCs (analogue to digital converter) that operate at the LHC frequency, with a wide dynamic range of 10^4, and generate a new 5-bit mantissa plus 2-bit range number every 25 ns (*hence the digitization of the data*). The digitized data are then sent off the detector via Gigabit Optical Link (GOL) driving optical fibers at 1.6 Gbps, each carrying three channels of data. From this point on, the data are taken into the back-end electronics.

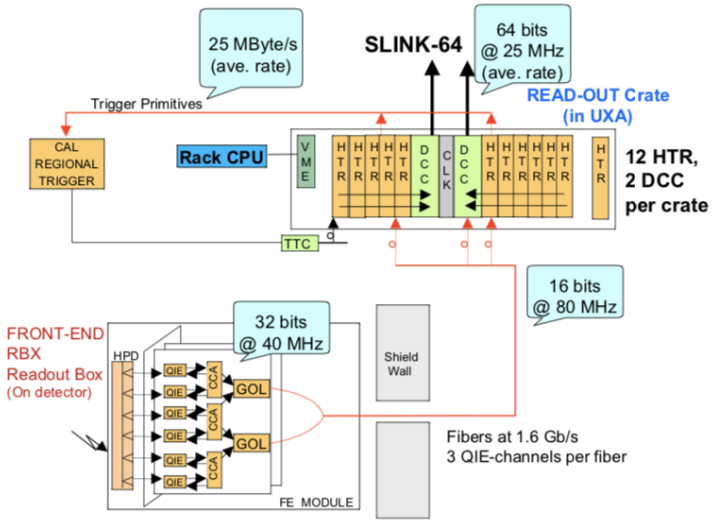

Figure 5.6. A schematic view of the HB on-detector front-end and off-detector back-end electronics.

The data sent off of the detector are taken to HCAL Trigger and Read-out (μHTR) where the trigger primitives are created. μHTR contains two data pipelines; one responsible for the transfer of the trigger primitives to the regional trigger and the other responsible for the transfer of the read-out values to Data Concentrator Cards (DCC) after Level 1 Accept (L1A) is received through the Timing, Trigger, and Control (TTC) system. The data are kept at DCC waiting for transmission to the Data Acquisition (DAQ) (Figure 5.6). [6, 17]

5.3. Clock and Control Module (CCM)

Clock and Control Modules, abbreviated as CCM, are modules consisting of four printed circuit boards (PCB). They initially shared the same design among HB, HE, and HO (Phase-0) and were initially named Clock, Control, and Monitor Module. The module works as an interface between front-end boards and the main control system and has three major tasks; receiving and distributing a low skew, low jitter 40 MHz LHC Clock along with a beam-crossing marker to RMs, monitoring the temperature at front-end boards and power supply voltages that are present on the backplane, provide a means for the Main Control system to communicate with the ASICs located on the FE cards and also provide a method to download parameters to those ASICs during a global reset. Each of these tasks which are listed above are performed individually by each board. [18]

Clock Board, performing the first task, receives and distributes 40 MHz clock signal through the TTC system via a custom receiver ASIC (TTCrx, see [19]), which was developed by CERN Microelectronics Group. The clock signal is then distributed to the RMs by a differential clock driver. A beam-crossing marker is also received by TTCrx and distributed onto the backplane by a differential translator. Finally, a copy of the clock signal is carried to the Control Board to be used as a master clock.

Control Board, along with controlling Clock and Monitor Boards, communicates with the Main Control System and decodes and distributes commands to RMs. An FPGA is used to provide the communication between the Main Control System and

RMs. The commands from the Main Control System is received by the FPGA and then distributed onto the backplane, i.e., onto the RBXbuses which are serial communication paths connected to RMs.

Monitor Board performs the monitoring of the temperature of the RMs and power supply voltages that are present on the backplane. A temperature transducer is used to produce a current representing the temperature of each RM. The produced current is then converted to voltage and is sent via the backplane to the Monitor Board. These temperatures along with the power supply voltages are converted to a digital word using an ADC and an Analog Multiplexer. The temperature and voltage readings can be accessed by the Main Control system through the Control Board of the CCM.

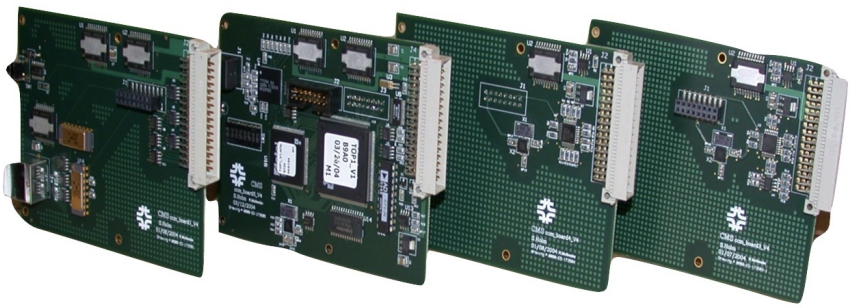

Figure 5.7. A picture of CCM boards in the following order; Board 1, Board 5, Board 3, Board 4.

The four board CCM module consists of one monitor, one control, and two clock boards. The numbering of the boards is made such that the monitor board is Board 1, the control board is Board 5, and the Board 3 and Board 4 are clock boards (see Figure 5.7). A fully assembled CCM module with and without the Aluminum housing is shown in Figure 5.8.

Figure 5.9 shows the links between the CCM and the control system in the Legacy (Phase-0) System. The CCM requirements given above are performed with what can be narrowed down to three types of signals: Clock and Fast Control (often the clock signal is considered part of the Fast Control), and Slow Control. In Legacy System, Fast Control and Clock Signals are sent to the CCM from the TTC via a unidirectional optical link operating at 80 Mbps. Fast control signals must be in sync with the clock

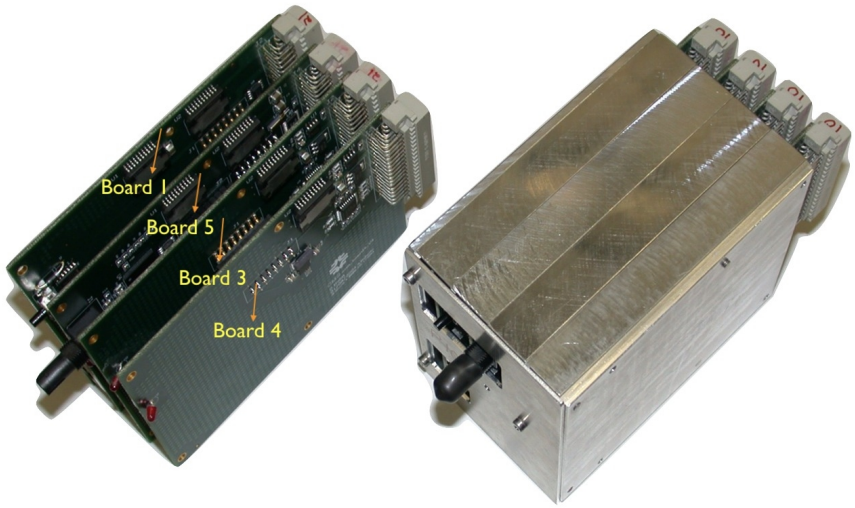

Figure 5.8. A picture of CCM modules without and with the Aluminum housing.

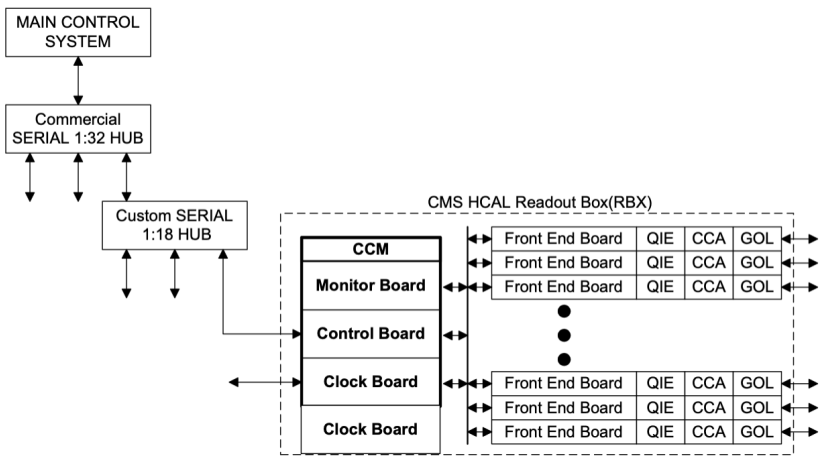

Figure 5.9. Schematics of the links between Front-End and the Main Control System.

signal used for processing of the detector data. On the contrary, the Slow Control signals are not required to be in sync with the detector data, and they are sent from the Custom HUB via a bidirectional copper link operating at about 100 kbps.

6. PHASE-I UPGRADE OF THE HADRON BARREL CALORIMETER

The Phase-I Upgrade is the first step of two-staged upgrade plan of the CMS experiment. For HCAL, it does not imply any changes in the absorber and active material but does imply changes in the Front End Electronics (FEE), Data Acquisition (DAQ), and Trigger. The focus of this thesis is the changes made on FEE of the HB.

As it is the case for the HE and HO, the main driver of the Phase-I Upgrade of the HB is the radiation damage to the scintillator tiles and the solution to how this radiation damage can be compensated by a change of photodetectors. HPDs were chosen as photodetectors for their gain (of about 2000) and their magnetic field tolerance. However, some anomalous signals (not coming from beam collisions) during Run 1 proved to be caused by electrical discharges from the HPDs. Silicon PhotoMultipliers (SiPMs), on the other hand, have about a gain of 10^5, and are operated at a much less voltage of about 100 V, compared to the 8 kV that is required for the HPDs, and are not sensitive to magnetic fields, hence they eliminate the sources of anomalous signals. SiPMs are also much smaller in size compared to HPDs and this implies that more channels can be fit in the same physical space (Figure 6.1). This makes the main component of the HB upgrade to be the replacement of HPDs with SiPMs which in turn makes it the first large scale use of SiPMs in a radiation environment. To be compatible with the new readout for the new photosensors, the associated front-end electronics is also upgraded. [20]

New Generation Readout Modules (ngRMs) are of the same physical size as Phase-0 RMs but have a different number of readout cards. ngRMs include an ODU that organizes the analog light pulses into calorimeter tower segments, one SiPM Mounting Board hosting eight SiPM arrays (64 SiPMs), one SiPM Control Board and four new 16-channel QIE11 Boards (see Figure 6.2). The readout chain remains conceptually the same as Phase-0. It starts with the collection of light from the scintillators and

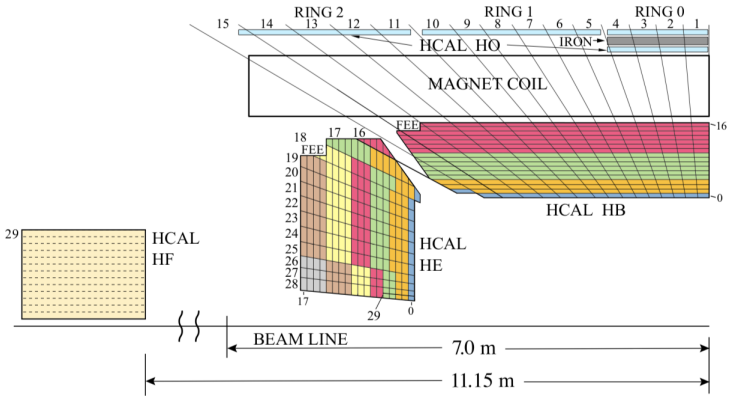

Figure 6.1. The upgraded depth segmentation of HCAL.

their transfer to the photosensors, SiPMs, via ODU. The charge output of SiPMs is then fed into the QIE to be digitized and sent off the detector via a new optical link with a greater bandwidth of 4.8 Gbps called The Versatile Link (will be explained later in this chapter). [21]

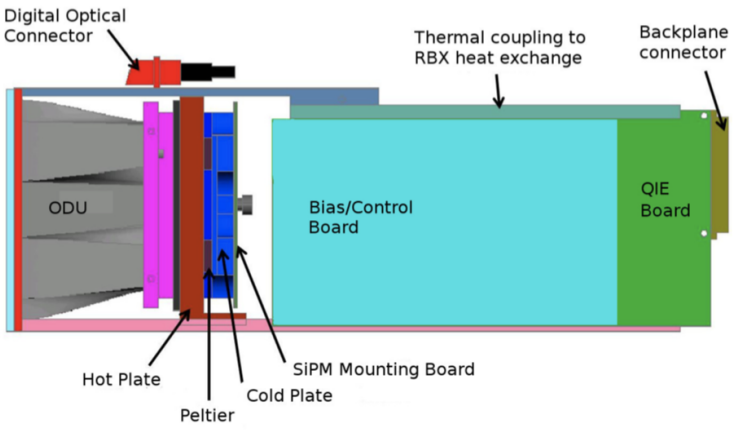

Figure 6.2. Illustration of the ngRM design.

Calibration Unit (CU) is housed in the RBX along with RMs and CCMs. It contains an LED pulser for the SiPMs as well as a laser light distribution system. Major changes in the design compared to Phase-0 CU is repositioning of QIE and Pulser Boards and repositioning of light mixer box and laser slitter. [21]

New Generation Clock and Control Modules (ngCCMs) are composed of three boards called clock, primary control, and secondary control. They do differ in design

compared to their Phase-0 version now that they have three boards and one of which supports a redundant link. They also differ in number because now each RBX houses two ngCCMs. ngCCMs will be explained later in detail as they are the focus of this thesis.

The rest of the main Control System is also going to be upgraded in order to meet the requirements of the new FEE. The New Generation FrontEnd Controller (ngFEC) is responsible for grouping the Fast Control signals (including the LHC clock) and Slow Control signals onto the optical control link used to communicate with the FEE. The upgrade includes the replacement of the existing VME standard with μTCA standard (see [22]) and it was designed to satisfy the following requirements:

- ability to receive fast control signals from the existing TTC system and to distribute these signals to FE,
- ability to combine fast and slow controls into one bidirectional optical link,
- ability to make use of the front-end redundancy scheme.

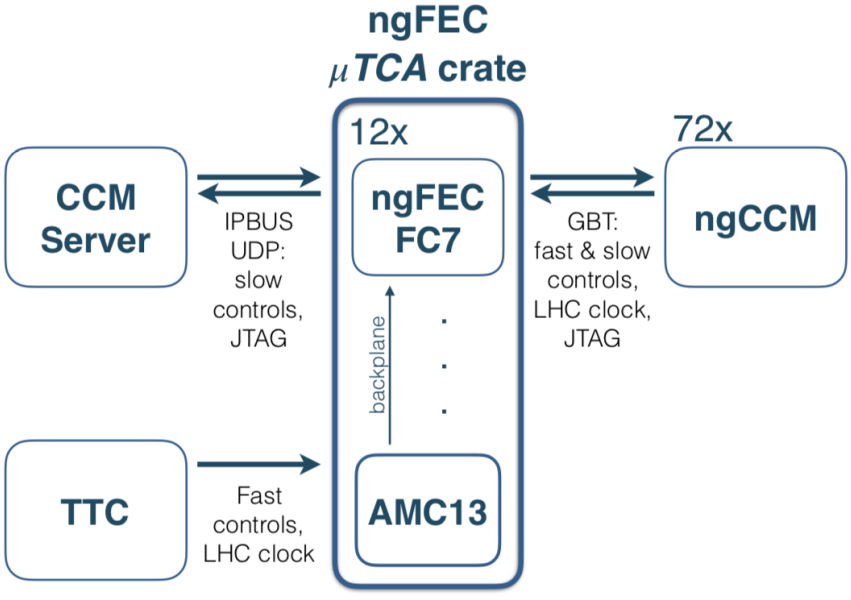

Figure 6.3. Diagram of the ngFEC system.

Figure 6.3 shows the components of a ngFEC μTCA crate and nearby systems. Each crate consists of a new generation clock, timing, and DAQ module called AMC13 [23], a μTCA carrier hub (MCH), two redundant power supplies, and up to twelve

FC7 which is a μTCA compatible Advanced Mezzanine Card (AMC) for generic data acquisition/control applications. [24]

As mentioned before at the end of Section 5.3, the three types of signals that are required for detector operation are now sent from ngFEC with a slightly different link map. The Clock and Fast Control Signals are formed and sent by the TTC system to AMC13. After receiving these signals, AMC13 distributes them onto the ngFEC boards through the backplane. The Slow Control Signals are formed by the CCM Server and sent to ngFEC boards via IPBUS Protocol. These signals are then sent to the ngCCM via GBT protocol through fiber connections. When compared to the Legacy System, Phase-I System uses a new optical link to drive data off the FE via a protocol called 8b10b which operates at 5.0 Gbps. The new bidirectional control link, merging slow and fast controls, is also quite faster than its older version by operating at 4.8 Gbps via GBT protocol. [25]

6.1. The GigaBit Transceiver (GBT) Project

The GigaBit Transceiver (GBT) Project is a common project developed at CERN and it is designed in the framework of Versatile Link Project to support high speed transmission of DAQ, TTC and detector control data over the same link. [26]

6.2. The Versatile Link Project

The Versatile Link Project is a common project developed at CERN. It is a radiation tolerant, high speed (4.8 Gbps), bidirectional optical link to be used in each system required by any high energy physics experiment: DAQ, TTC, and Detector Control. It is designed to operate in tandem with the Gigabit Transceiver (GBT) chips. [27]

The implementation of this high speed data transmission scheme for the upgrade of LHC implies relatively high rates of Single Event Upsets (SEUs). The solution to overcome this high rate of SEUs does not lie in the typical approach of using redundancy

techniques but in the transmission of the data with Forward Error Correction code generated at the input of the serializer and verified at the output of the de-serializer. Any transmission errors occurring on the serializer-deserializer (SERDES) circuit is corrected at the receiver during the decoding process. The error correcting code chosen for this task is Reed-Solomon (RS) and it is contained in the GBT protocol.

RS codes contained in the GBT frame generate a corrected frame which is compared with the actual received frame. If they differ in comparison, the RS Decode error counter gives the number of differing bits as error counts. In the raw frame of 120-bits, RS Decode requires 32 bits leaving 88 bits for the comparison of frames. The RS algorithm is complemented with a bit error rate (BER) detection module on both BE and FE to detect the communication errors that RS algorithm was not able to correct. This BER module consists of a Pseudo-Random Binary Sequence (PRBS) generator and a generic error detection module. The PRBS generator generates 20-bit sequence contained in the payload of the control link which is going to be compared with an expected sequence generated by assuming an error-free communication. Any difference in the comparison of the bits is then indicated as a communication error. [26, 28]

6.3. New Generation Clock and Control Module

As already discussed in this chapter, Phase-I Upgrade of CMS remains loyal to the existing design, but does necessitate some changes in parts of the detector, which is the case for FEE. New Generation Clock and Control Modules (ngCCMs) are expected to perform the same core functions as the existing CCMs but with a faster control link and redundant links, considering that the absence of redundant links in Phase-0 posed a danger of loss of data.

The core functions to be performed by ngCCMs;

- Provide a good quality clock in phase with the LHC clock and synchronize the FE with the BE
- Provide an orbit signal to the FE (RESET-QIE)

- Provide reset capabilities for the FE (RESET)
- Provide Warning-Test-Enable signal (WTE) for calibration
- Provide readout of Board Temperature, Voltages, and Currents
- Provide I^2C (an electronics protocol used for the communication between components of a PCB) communication over GBT (*for the configuration of the QIE11 and FE-FPGA chips*)
- Provide I^2C communication for the bias voltage setting of the SiPMs and for the Peltier control loop (Peltier Enable)
- Provide JTAG communication over GBT
- Power enable and status

Although it seems that Phase-0 and Phase-I CCMs look similar, there are few differences. One is the change of the optical link from GOL to Versatile Link which brings out a new bidirectional control link operating at 4.8 Gbps. In the existing FE, one CCM controls 72 data channels. However, each ngCCM now controls 128 data channels, which actually increases the need of a redundant link because losing one ngCCM means losing 128 data channels. The switch is done via the remote programming of the FPGAs over the GBT link which ensures that in case of the loss of a control board it is possible to reprogram the other as needed and hence the redundancy (this is done by the JTAG protocol and will be explained in the next chapter). The difference in design has twofolds because initially HB ngCCMs shared the same design as HE ngCCMs but then because of mechanical constraints, HB ngCCMs differed in design.

The first PCBs made by the University of Virginia were based on HF ngCCM layout as a starting point and were initially the same for HE and HB and they included a simpler design, which reduced the cost. They differed in simplicity from the existing PCBs by having two distinct boards instead of four, which combined control and monitor boards into two identical control boards and the other two clock and timing boards into similar clock boards and the proposed module was composed of four boards in the following order; clock, master control, slave control, and clock. They also differed in size compared to existing boards. The original PCBs have a size of 120 x 88.8 mm whereas the new ones (Figure 6.4) have 140 x 88 mm.

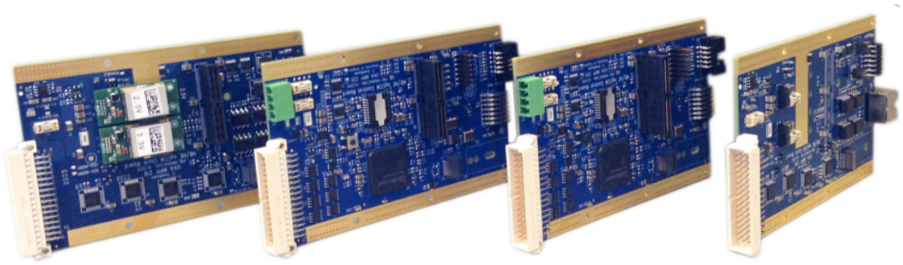

Figure 6.4. A picture of the pre-production clock and control boards for ngCCMs. The two central boards are identical control boards and the two outer boards are similar clock boards.

The initial four-board ngCCM was compatible with the HE but not with the HB because of mechanical constraints. The proposed solutions were either splitting the ngCCM or splitting the backplane itself. The former solution was not efficient enough because it meant two-board ngCCMs which did not include a redundant link. The latter, however, was an efficient solution, offering redundant clock and control links for each side of the RBX (see Figure 6.5). However, the four-board module could not be fit into the half backplane which in the end showed that the final design should be a three-board ngCCM, with the removal of one clock board.

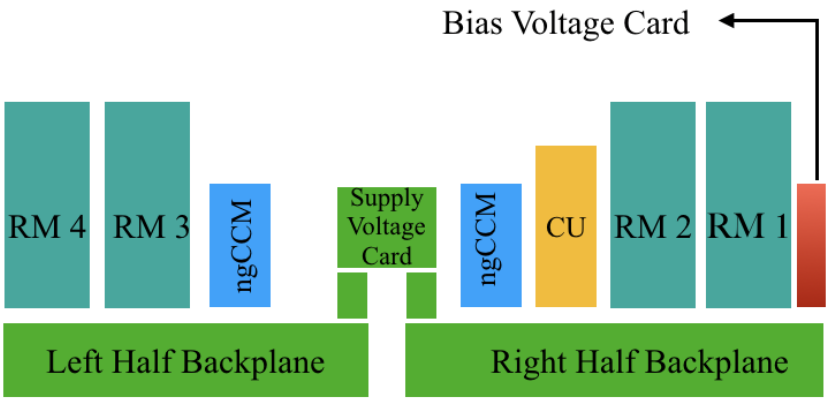

Figure 6.5. Illustration showing the upgraded backplane. Each ngCCM now supports two ngRMs. ngCCM on the right backplane also supports the CU.

The three board ngCCM is configured as clock, master control, and slave control boards and the production process of the boards is three-staged. Production 1 and Production 2 clock and control Boards are the same for HB and HE and they are blue and red respectively. Production 3 boards are designed for HB and are yellow for clock

boards and red for control boards.

6.4. Clock Board

The clock board requirements are the same as the existing Phase-0 clock boards. However, the increase in channel counts that comes with Phase-I upgrade is not on par with the increase in power use. The HB upgrade increases the data volume by a factor of five, however the increase in power is constrained to increase by a factor of three. To compensate for the gap in increased power use, DC/DC converters are used on clock boards. The DC/DC converters used on clock boards are designed at CERN and are called FEASTMPs. The PCBs are made of eight layers of laminate and have overall dimensions of 140.0 mm × 88.0 mm. [29] (See Figure 6.6 for pictures of Production 1, Production 2, and Production 3 Clock Boards.)

6.5. Control Board

As discussed in section 6.1, the control board design was made such that the requirements from control and monitor boards can be satisfied by combining them into one control board. Therefore, the control board performs the same tasks as old control and monitor boards combined. The two control boards in ngCCMs are identical PCBs but have different firmware. Compared to their Phase-0 versions, the control boards now accommodate multimode Versatile Transceivers (VTRx) and FPGAs programmed with GBT protocol. VTRxs are modules designed for use in Versatile Links and they contain one optical transmitter and one optical receiver. The control boards also have a set of DIP Switches each enabling a different feature when switched down (switching down is the ON direction.). The PCBs are made of twelve layers of laminate and have overall dimensions of 140.0 mm × 88.0 mm. [26, 27] (See Figure 6.6 for pictures of Production 1, Production 2, and Production 3 Control Boards.)

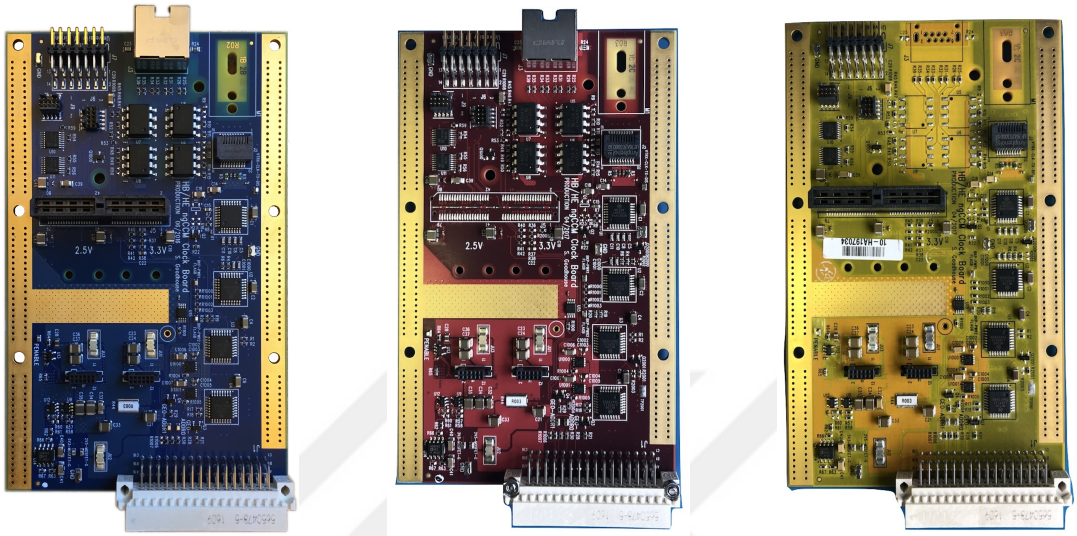

Figure 6.6. Pictures of Production 1, Production 2, and Production 3 Clock Boards from left to right.

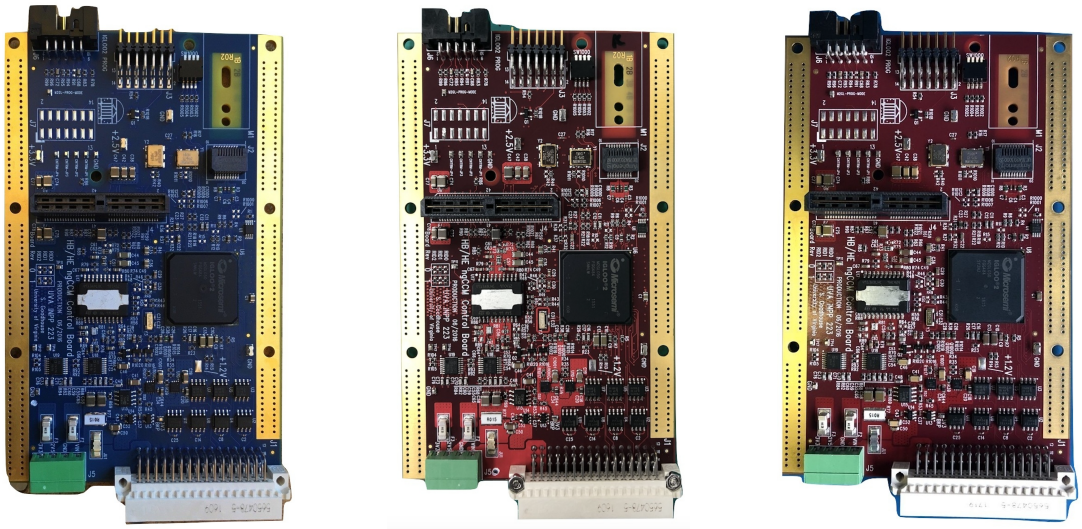

Figure 6.7. Pictures of Production 1, Production 2, and Production 3 Control Boards from left to right.

7. TESTS AND INSTALLATION OF THE ngCCMS

The three-board ngCCM modules are housed in aluminum shells of four layers, composing three slots which correspond to clock, primary control, and secondary control boards and each of these individual boards is tested before the module assembly. This chapter explains the assembly and test procedure of the modules starting with the tests of individual boards, followed by the assembly and tests of ngCCMs.

7.1. Tests and Assembly of Individual Boards

7.1.1. Test Setup

The setup used in single board tests differ for clock and control boards as they have different tasks to perform. They have two components in common; external power supplies to power up the boards and a multimeter to check the power supply rails if they have the specified impedance value. In control board testing however, there is more to test than only checking the power supply rails. The first is checking the reference clocks on the boards by using an oscilloscope and the second is the programming of the FPGAs on the boards. This is done by a hardware JTAG programmer called FlashPro with a computer installed with the FlashPro software. The control board testing also uses a GLIBv2 μTCA board as a mock FEC to communicate with the module and a FE emulator board complemented with an HB/HE to HF adapter board.

7.1.2. Clock Board

The individual tests of the clock boards start with the visual inspection of the PCB to make sure there are no abnormalities, e.g. solder shorts or misalignment of the connectors. After making sure the PCB is manufactured properly, the power supply rails are checked for shorts using a multimeter set to measure resistance. The rails are located among VIN pins, 2.5V, 3.3V, 3.3V-Backplane(BKP), and Ground (GND) pads on the PCB (see Figure 7.1 (right)) making up a total of 10 rails which are

- from VIN pins to GND (either GND pins or gold side rails can be used),
- from 3.3V-BKP pad to GND,
- from 3.3V pad to GND,
- from 2.5V pad to GND,
- from 3.3V-BKP pad to VIN pin,
- from 3.3V pad to VIN pin,
- from 2.5V pad to VIN pin,
- from 3.3V pad to 3.3V-BKP pad,
- from 2.5V pad to 3.3V-BKP pad,
- from 2.5V pad to 3.3V pad.

The impedance measured in each rail is expected to be greater than 50 ohms. As mentioned in the previous chapter, ngCCM clock boards now have DC/DC converters called FEASTMPs. If no abnormality is observed in the power supply rails, the test proceeds with the installation of FEASTMPs.

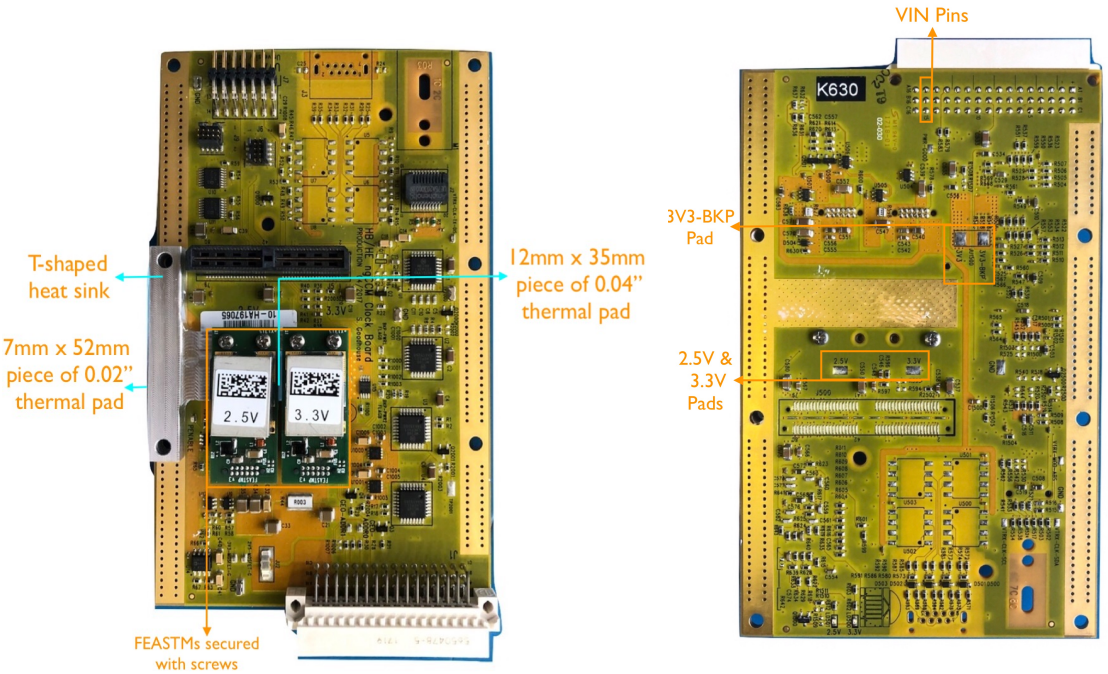

Figure 7.1. The picture of the top (left) and bottom (right) of the assembled clock board PCB.

Custom T-shaped metal heat sinks that are complemented with thermal pads and thermal paste are used under the FEASTMPs and on the edge of the heatsink that touches aluminum housing to prevent overheating. Figure 7.1 (left) shows the places and dimensions of the thermal pads used. The thermal paste is applied on the bottom of the heat sink where it touches the PCB and also on the top to the left of the FEASTMPs where it is in contact with the next layer of the aluminum housing. After the heat sink is screwed to the PCB, FEASTMPs are inserted into their connectors and are screwed to the heat sink. The last test before sending the board to the module assembly is checking the power consumption of the board. After setting the emulator board power supply to a voltage limit of 9.5 V and a current limit of 1.0 A, the clock board is installed on the J16 slot of the adapter board. The power supply is turned on and a current reading of about 0.5 A is expected. The voltage outputs of FEASTMPs is measured by a multimeter and expected to be between 3.2 V - 3.4 V for 3.3 V module, and between 2.4 V - 2.6 V for 2.5 V module. If no anomaly is observed, the clock board is put aside for module assembly and testing.

7.1.3. Control Board

The individual tests of the control boards also start with the visual inspection to make sure there are no manufacturing defects. After making sure the PCB is manufactured properly, the power supply rails are checked for shorts using a multimeter set to measure resistance. The rails are located among VIN pins, 1.2 V, 2.5 V, 3.3 V, 3.3 V-Backplane (BKP), and Ground (GND) pads on the PCB (see Figure 7.2 (left)) making up a total of 15 rails which are

- from VIN pins to GND (either GND pins or gold side rails can be used),
- from 3.3V-BKP pad to GND,
- from 3.3V pad to GND,
- from 2.5V pad to GND,
- from 1.2V pad to GND,
- from 3.3V-BKP pad to VIN pin,

- from 3.3V pad to VIN pin,
- from 2.5V pad to VIN pin,
- from 1.2V pad to VIN pin,
- from 3.3V pad to 3.3V-BKP pad,
- from 2.5V pad to 3.3V-BKP pad,
- from 1.2V pad to 3.3V-BKP pad,
- from 2.5V pad to 3.3V pad,
- from 1.2V pad to 3.3V pad,
- from 1.2V pad to 2.5V pad.

The impedance measured in each rail is expected to be greater than 50 ohms. After checking each rail and making sure of no shorts, the control board is powered through the green power connector (J5) with use of 9.5 V, 2.5 V, and 3.3 V power supplies with current limits of 1.0 A. The power supplies are turned on starting with 9.5 V, followed by 2.5 V and 3.3 V. The expected current readings are about 100 mA for each. The 1.2 V regulator output voltage is measured with a multimeter and expected to be between 1.19 V - 1.25 V.

There are two reference clocks installed in the control PCB. REFCLK1 which is the default reference clock and REFCLK0, a redundant reference clock. After checking the power consumption and making sure of no abnormalities, REFCLK voltages and frequencies are measured with an oscilloscope. The clock signal is expected to be monotonic with a high voltage falling between 1.8 V - 2.5 V and low voltage falling between -0.2 V - 0.6 V. The expected frequency for both clocks is about 120 MHz.

The control boards have Igloo2 FPGAs programmed with GBT protocol and are responsible for the communication of ngCCMs with ngFEC and also with the FE readout cards. The next step in the control board test is checking the access to the Igloo FPGA. This is done via a JTAG programmer and FlashPRO software. There are two control boards in the ngCCM and they only differ in the firmware. After choosing whether the board will be primary control or secondary control board, the JTAG programmer is attached to the J6 JTAG connector. Among the list of actions

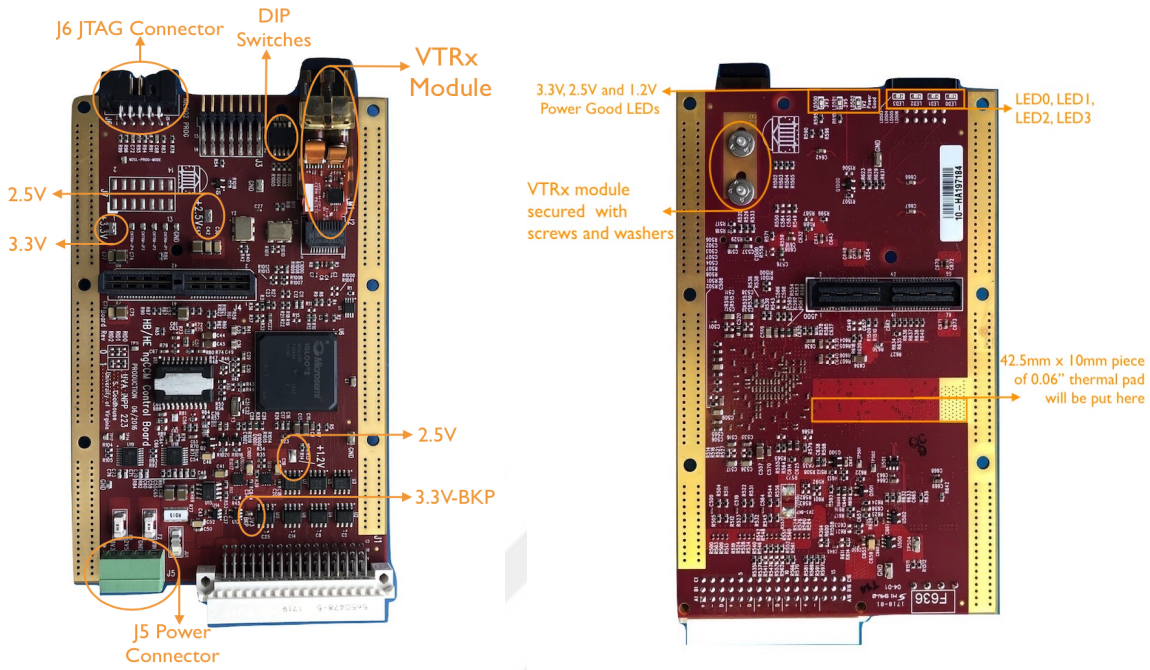

Figure 7.2. The picture of the top (left) and bottom (right) of the assembled control board PCB. The LEDs shown in the right picture are used to verify operation of the ngCCM.

in the software toolbar, DEVICE INFO is performed first and verified if the action is successful (DEVICE_INFO PASSED message is received in the console and RUN PASSED green indicator appears in the Programmer Status bar). The respective firmware is then chosen and the FPGA is programmed and Programmer Status is checked if the green indicator appeared. A VERIFY action is performed after the programming and checked if passed. DEVICE INFO action is repeated to record the device serial number and Checksum. After a successful programming, the currents drawn by each power supply is recorded. 1.2 V regulator output voltage is measured with a multimeter and recorded. The board is powered down to install the MM VTRx module. A torque driver, screws and washers are used to secure the module. After the module is installed (see Figure 7.2 (left and right)), power supply currents are recorded again.

The last step before setting the board aside for module assembly and testing is checking the GBT communications. A GLIBv2 board with MM SFP module along

with a MM fiber is used. GLIBv2 board power supply is set to a voltage limit of 12.0 V and a current limit of 2.5 V and it is turned on. The PRBS error counts are checked by using the ERR_STATUS command under the GBT:NGCCM menu in GLIBtool. An example of the output of the ERR_STATUS command is given in Figure 7.3. CLEAR_ERR command under the same menu as before is used and error status is checked several times and expected to remain 0. The TEMP command under the same menu is used to check if the temperature sensor IDs and temperature values can be read. The output of the TEMP command is recorded and the board is put aside for module assembly and testing.

```
GLIB RX <- ngCCM TX Error Count:              0 (w/o DV:  ----------)
GLIB TX -> ngCCM RX Error Count:              0 (pre-FEC:          0){RX PLL Delay: -30}
GLIB TX -> ngCCM RX Error Count last ms:      0 / PLL Unlock:      0
```

Figure 7.3. A sample output of ERR_STATUS command.

7.2. ngCCM Module Assembly and Tests

7.2.1. Assembly

After each of the three boards is ready for module assembly, the four-layered Aluminum enclosure (see Figure 7.4) is first visually inspected. The bottom layer of the housing, which is in contact with the clock board, needs to have a cutoff on the edge where it touches the MCLK pins below the J1 connector. (*If not cut off, it shorts the MCLK pins of clock boards and causes a loss of clock signals.*)

After a successful visual inspection, the bottom plate of the enclosure is Kapton taped for insulation. The threaded rods to hold the layers together are glued with Locktite and screwed into the holes in the bottom plate. After the glue dries, the clock board is carefully placed. Four brass stand-offs of are placed over the four threaded rods, leaving the two rods that pass through the metal heat sink without stand-offs. Then, the next layer of the enclosure is placed over the clock board. The long aluminum spacers are placed on both sides of this layer and the primary control board is placed on this while paying attention to the alignment of the thermal pad and the FEASTMPs.

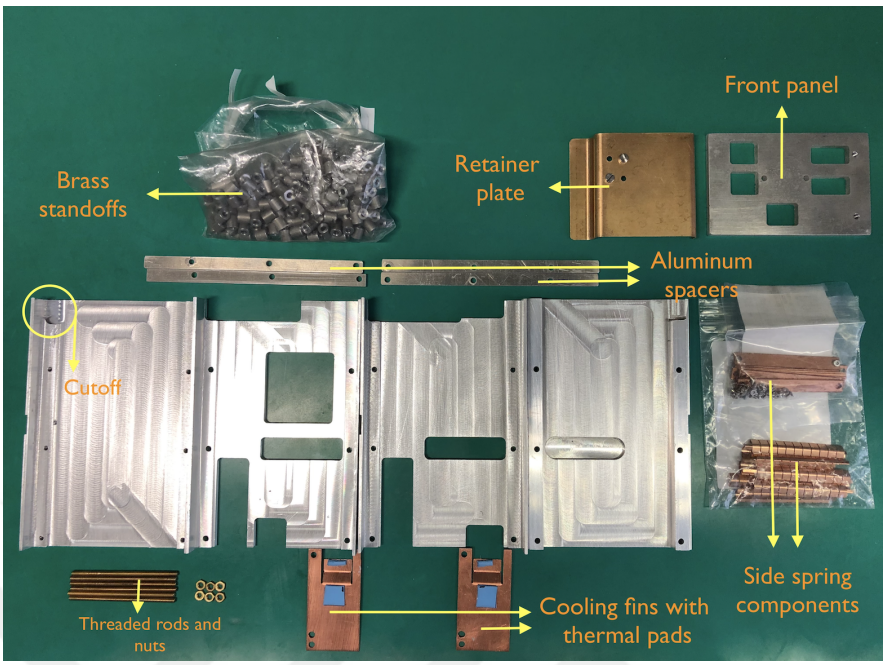

Figure 7.4. Picture showing all components of the mechanical enclosure used to assemble a ngCCM module.

Four longer brass standoffs are put on the four screws that do not have any contact with VTRxs and two shorter standoffs are put on the screws which are to the left of VTRx module. A cooling fin complemented with thermal pads of 3 mm $\times$ 7 mm, 0.1″ thick and 12 mm $\times$ 12 mm 0.06″ thick is placed over this two standoffs to prevent overheating of VTRx and prolong their lifetime. The next Aluminum layer and the secondary control board are put exactly in the same manner, with standoffs and cooling fin. Finally, the top layer of the housing is put and nuts are tightened on the ends of the threaded rods. (See Figure 7.5 for a step by step assembly.)

Module assembly is not fully completed before the module tests are performed and passed. The side spring and the front plate together with the retainer plate are put when the module is ready to be sent to installation. The last step before completing the module assembly and send it off to module tests is checking the DIP switches. As mentioned before in Chapter 6, control boards now have four DIP switches next to the VTRx module. Each of these switches has a feature that is enabled when switched down and these features are as following;

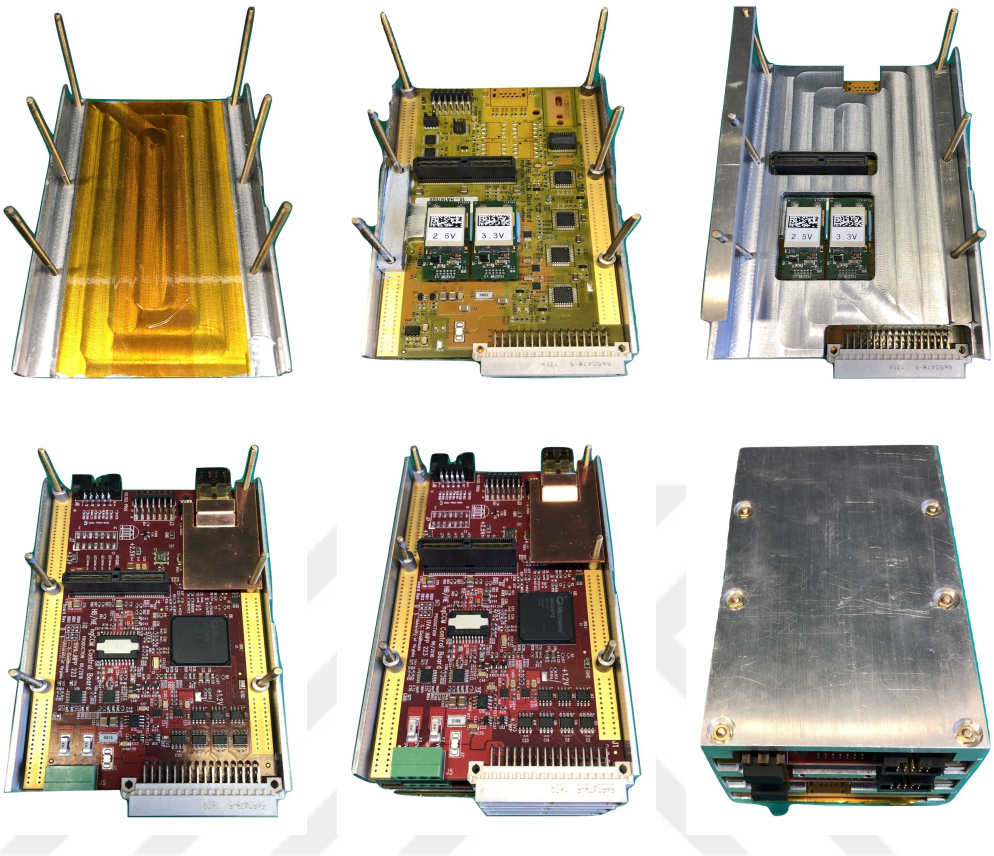

Figure 7.5. Pictures showing the step by step assembly process of the ngCCM module.

- DIP Switch 1: Enables JTAG DEBUG so that internal JTAG signals can be sent out of the FPGA and monitored
- DIP Switch 2: Enables UART so that the UART Debug Interface can be reached and several test modes can be enabled, i.e. changing REFCLK
- DIP Switch 3: Enabled when MM VTRx is used on J15 or SM VTRx is used on J14
- DIP Switch 4: Enables HB mode

In accordance with the above explanations, DIP switches 2 and 4 should be switched on to enable uART and HB mode respectively. Also, because MM VTRxs are used with both control boards, DIP switch 3 should also be switched on for primary control board J15 and all other switches must be off. J15 control board defaults to a SM VTRx and when a MM VTRx is used, it inverts the TX line. After making sure the switches are set correctly, the module is sent off to module testing.

7.2.2. Test Setup

The setup used in module testing should be able to mimic the entire electronics scheme of the HB to make sure each function of the module can be tested as it is installed in the detector. Therefore there needs to be a mock control system and a mock front-end. A GLIBv2 μTCA board is used as the mock FEC system and a front end emulator board with an HB/HE to HF adapter board (as in control board testing) is used as the mock FE. External power supplies are used to power up the GLIB board and the module as well as a computer to connect to the module via GLIBtool to be used on a Linux system. There is one more component to this setup which is to test the new redundancy scheme of ngCCMs called JTAG evaluation board.

Front-End Emulator Board is used as a mock front end and it has LEDs installed to check the output signals from ngCCMs and switches to check the input signals for ngCCMs. It is complemented with an HB/HE to HF adapter which has four slots called J16, J15, J14, and J13 corresponding to actual slots in RBX backplane (see Figure 7.6 and 7.7).

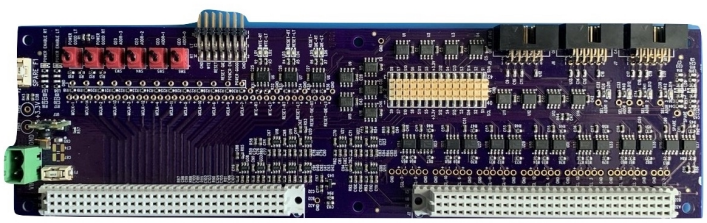

Figure 7.6. Picture of the emulator board.

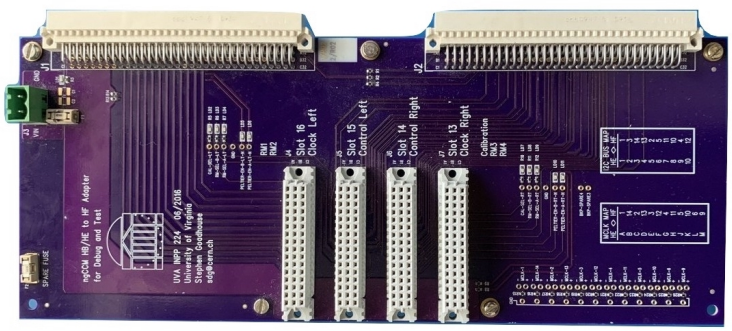

Figure 7.7. Picture of the emulator adapter board.

The adapter board is designed to be compatible for both HB and HE and because HB and HE ngCCMs initially shared the same design which proposed a four-board ngCCM, hence there are four slots.

GLIB, Gigabit Link Interface Board, is a mock FEC system used for production tests and firmware debugging of the ngCCMs. It has Small Form-factor Pluggable (SFP) transceivers which are connected to the VTRxs on the control boards with MM optical fibers. This interface is reached with GLIBtool which is a C++, text-based tool for controlling and monitoring the ngCCM through a GLIBv2 (Figure 7.8). [30]

JTAG is an industry standard used in the testing of PCBs. A JTAG evaluation board is used in this setup to test if the FPGAs on ngCCMs and on readout cards can be successfully programmed (Figure 7.8).

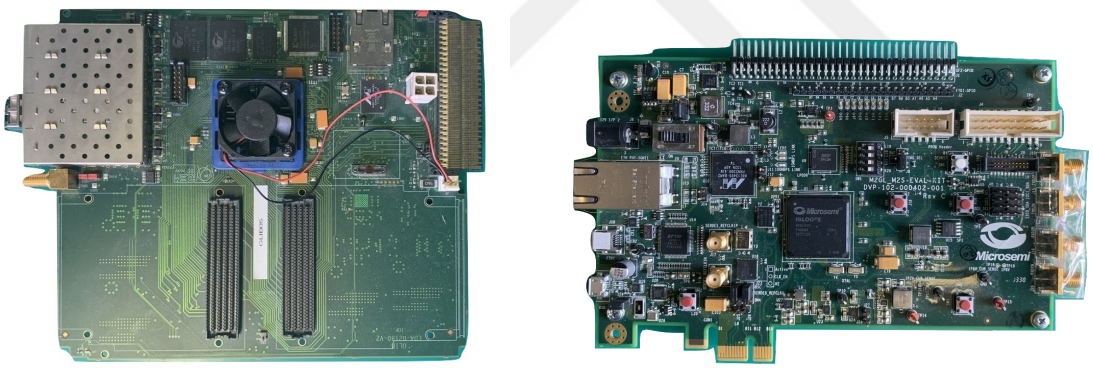

Figure 7.8. The pictures of GLIBv2 μTCA board (left) and JTAG evaluation board (right).

7.2.3. Module Testing

As it can be concluded from the ngCCM requirements that were given in Section 6.3, there are eight important tests to be conducted in module testing. Each of these tests is aiming to check the performance of the ngCCM under upgrade requirements. The tests to be conducted are;

- Check if the communication with GLIBv2 is recovered after repetitive interruptions (GBT Test)

- Check the power consumption of the ngCCM in a range of voltages is as expected (ADC Check)
- Check that good quality output clocks are received (MCLK Check)
- Check that the input and output signals are transmitted from the ngCCM when told by the GLIBv2 (IO Test)
- Check that the I^2C communication is stable (I2C Test)
- Check that the board-to-board communication is stable (B2B Test)
- Check if OneWire Temperature IDs and Temperatures can be read out
- Check remote programming of FPGAs between the control boards and from the ngCCM to the RMs via JTAG (JTAG Test)

The above tests are performed in the setup explained in Section 7.2.2. After it is properly assembled, the ngCCM module is plugged into the emulator adapter board and two USB serial cables are attached to the pins of J3 debug connector to enable uART Debug Interface. The VTRx modules used in ngCCMs are multi-mode (MM), hence a MM fiber is attached from GLIBv2 to the VTRx module on J15 primary control board. The power supplies for GLIBv2 and the emulator board are set to 12 V and 9.5 V, respectively, with the emulator board power supply set to a current limit of 2.5 A. After the power supplies are turned on and the operation of ngCCM is checked via LEDs, uART pyhton script is used to functionally verify the operation of the ngCCM. An example of the uART console output is given in Figure 7.9.

The console output includes same status information for two different links, from each control board, and each link has two lanes, between the two control boards. The output is checked to see if the boards are configured for REFCLK1 and NORMAL test mode and if RX Frame Clock frequencies are as expected, which is about 20 MHz. The first five GBT Status bits are also checked if they are all 1 and the RX_BITSLIP_NUMBER is checked for both links, expected to be 0:10 for the first link and 0:9 for the second link for both boards. Finally, the error counts are checked if they are working correctly by verifying that the error counter for both control boards is not increasing for link 2 and for the J15 control board, the error counter for link 1 is not increasing. To verify error counter operation, the fiber is disconnected from

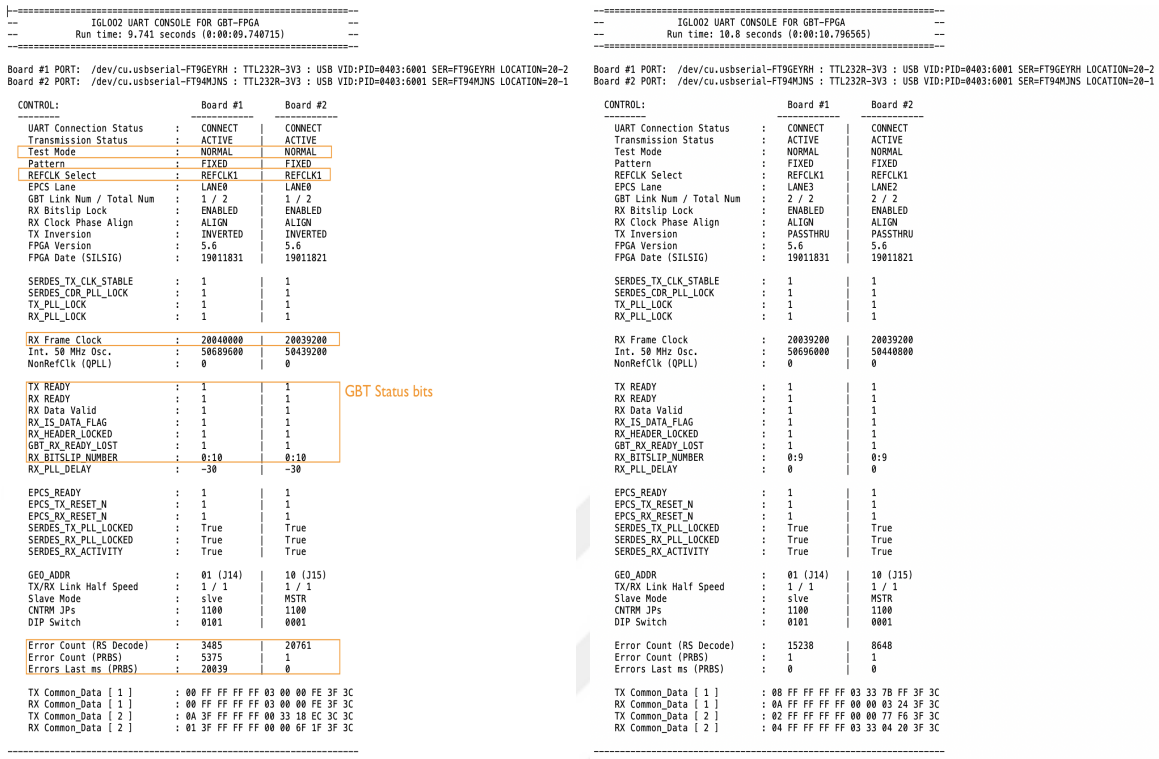

Figure 7.9. uART console output for both links.

GLIBv2 to see if the error counters change value for the first link of J15 control board. If the console output satisfies all these specifications, the module is set to be tested.

The following tests use the GLIBtool software on a Linux system. After starting the GLIBtool software, GBT menu is chosen by typing GBT which is followed by ngCCM for the ngCCM menu.

Among the commands in ngCCM menu (see Figure 7.10), PWR_ON command is used to power up the backplane. This is verified by the LEDs because they are expected to turn off when the backplane is powered. The expected current drawn by the module and the emulator board combined is between 1.2 A - 1.5 A. This is followed by ERR_STATUS command where the error counters are checked if they match the error counters in uART console output. As explained in Chapter 6, any transmission error occurring on SERDES is corrected at the receivers which implies that the error counts can only be checked at the receivers. There are five receivers in the ngCCM test setup; the two VTRxs on control boards (only one of them connected to GLIB and

```
HB> gbt
[
   PICK         Pick Which SFP Port to Use
   STATUS       Return Status bits
   CLOCKS       Return GBT-Related Clock Rates
   RESET        Issue a Top-Level GBT Reset
   LINK_RESET   Reset the high-speed links
   TXPLL_SHIFT  Issue command to phase shift TX PLL
   BIST         Toggle Built-In Self Test Enable
   HEARTBEAT    Toggle Heart Beat LED flashed used not in BIST
   HEARTBEAT    Toggle Heart Beat LED
   RX_PRBS      Toggle Check for PRBS Data   (RX)
   TX_PRBS      Toggle PRBS Data Generation  (TX)
   ERRCLR       Clear both error bits
   NGCCM        Accessing ngCCM via GBT
   QUIT         Back to top menu
HB> ngccm
[
   GBT_STATUS   Return GBT Status bits
   NGCCM_STATUS Return ngCCM Status & RX Status bits (from GLIB)
   ERR_STATUS   Return the RX & TX Error Counts
   CLEAR_ERR    Clear the RX & TX Error Counts
   CLEAR_ALL    Clear all of the RX & TX Error Counts
   IO           Reading and writing of ngCCM I/O via GBT
   TESTS        Semi-automated tests for ngCCM + FE Emulator
   PWR_ON       Enable Power on the Backplane
   PWR_OFF      Disable Power on the Backplane
   BKP_RESET    Issue a Reset over Backplane
   MASTER_SW    Switch which Control board is Master
   RX_SET       Set values for RX PLL & alignment
   I2C_WRITE    Write to a specified I2C device
   I2C_READ     Read from a specified I2C device
   I2C_DUMP     Dump from a specified I2C EEPROM-like device
   SLOT_WR      Write to Bridge FPGA on RM/QIE Card via I2C
   SLOT_RD      Read from Bridge FPGA on RM/QIE Card via I2C
   MEZZ_WR      Write to Registers inside Mezzanine FPGA via I2C
   MEZZ_RD      Read from Registers inside Mezzanine FPGA via I2C
   MEZZ_DUMP    Dump All Known Registers inside Mezzanine FPGA via I2C
   ADC          Read and Dump all values from ngCCM ADCs
   TEMP         Read and Dump all values from ngCCM Temp. sensors
   MORE         Menu of extra ngCCM commands
   QUIT         Back to previous menu
```

Figure 7.10. GBT and NGCCM Menus in the GLIBtool.

a fiber loopback is used for the other), the two board-to-board links and the GLIB. Therefore, when ERR_STATUS command is run, it goes through these five receivers and indicates the errors. This can be seen in Figure 7.11. Next is the verification of the stability of the communication links which is performed by the GBT Test.

- GBT Test is performed either by going to the TESTS menu in the ngCCM menu and by manually interrupting the link (with power cycles) or by using the gbtTest python script. This test basically checks the error counters for each link between the two control boards and between the GLIB and the ngCCM after the communication link is interrupted. The default user inputs for the test is 10 iterations, 2 seconds to wait before clearing errors (this is to get rid of errors caused by power cycle) , and 10 seconds to wait after clearing to check errors. As seen in Figure 7.11, the error counters are expected to show zero. (see Figure B.1 & Figure B.2 for a full sample output.)

```
Run GBT Test w/ num_iters=10, wait_clear=2, wait_check=10
Can stop GBT test and get summary by pressing Ctrl-C while test is waiting.

  NOTE: Control Link is to J15 with J15 as Master

  NOTE: Direct is using REFCLK1/1 and Neighbor is using REFCLK1/1

1/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   1 out of   1 PASSED with No Errors after GBT Interruption
```

Figure 7.11. An example of a GBT test performed with gbtTest.py script.

After a successful GBT test, the next step is to check the power consumption of the module. This is done by the ADC command; both for verifying the communication and for monitoring board status.

```
HB> adc
  LCLK VIN:  9.32V  IIN:  0.96A  PIN:  8.95W
  LCtl VIN:  9.37V  IIN:  0.03A  PIN:  0.26W
  RCtl VIN:  9.36V  IIN:  0.02A  PIN:  0.21W
  Total Power:  9.42W

        LCLKV  LCLKA   LCtlV  LCtlA   RCtlV  RCtlA   Tot.W
  3V3:  3.31V/ 1.51A   3.31V          3.30V          4.99W
  2V5:  2.51V/ 1.11A   2.50V          2.50V          2.79W
  1V2:                 1.23V/ 0.33A   1.23V/ 0.32A   0.79W
  BKP:  3.27V          3.29V          3.29V
  VTRx RSSI:  0.007mA        0.371mA        0.317mA

  LHC4913 Pwr Diss. 3.3Vin    0.68W          0.66W
  LHC4913 Pwr Diss. 2.5Vin    0.42W          0.40W

  LCLK Temp  U10:  26.25C  U11:  26.25C / LCtl  U18:  30.75C  U19:  29.00C
                                       / RCtl  U18:  30.00C  U19:  27.75C
```

Figure 7.12. A sample ADC readout.

The ADC output is then used to verify (see Figure 7.12);

- that the total input power is less than 13.0 W
- that the 3.3 V power is less than 6.5 W
- that the 2.5 V power is less than 4.5 W
- that the 1.2 V power is less than 1.3 W
- that the input voltage (VIN) on all three boards is $\geqq$ 9.2 V

- that the 3.3 V voltage is between 3.2 V - 3.4 V on all three boards
- that the 3.3V-BKP voltage is between 3.2 V - 3.4 V on all three boards
- that the 2.5 V voltage is between 2.4 V - 2.6 V on all three boards
- that the 1.2 V voltage is between 1.19 V - 1.24 V on all two control boards
- that the ngCCM temperature readings are all less than 50°C

The next test to be performed is checking the Master Clock (MCLK) outputs of the ngCCM, which is of great importance to the entire calorimeter HB itself. The MCLKs are the sample clocks to be distributed onto the FE boards. Loss of one of these clocks means losing the synchronization of that particular board and the FEC, resulting in the loss of data. There are a total of 12 MLCKs on a clock board and the number of clocks to be distributed to each RM is 5 because there 4 QIE cards and 1 SiPM control card in each RM. The remaining 2 clocks are for the CU. Because there is only 1 CU in each RBX, this is redundant. The MCLKs are checked by using an oscilloscope and are probed on the FE emulator board. They are located on the side of the clock board and can be seen in Figure 7.13. The clock signal is expected to be monotonic, with a nominal frequency of 40.0789 MHz (see Figure 7.14).

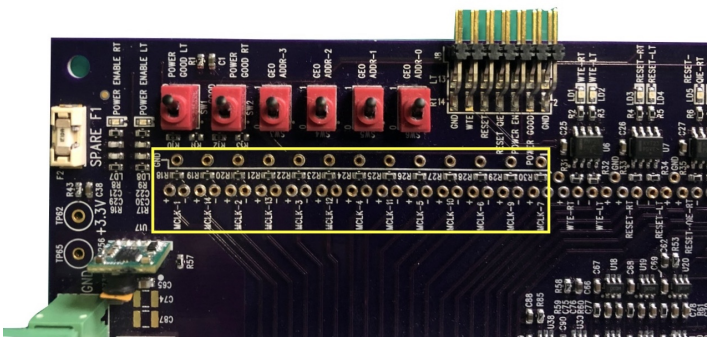

Figure 7.13. A picture of the emulator board showing the MCLK outputs in the yellow rectangle.

After probing 12 good quality MCLKs, the reference clocks on the control boards are switched to REFCLK0. This is done by running a jumper from pin 1 to pin 11 and pin 2 to pin 13 of J7 connector on the clock board. The REFCLK status is checked either by using uART interface or by using MEZZ_RD command in the NGCCM menu in GLIBtool. After verifying that both control boards are switched to



Figure 7.14. An example of an expected clock signal.

REFCLK0, the GBT test performed to check if the communication link is still stable now that the reference clock is changed. If the GBT test is successful, the jumper is released from J7 and the control boards are switched back to the default reference clock, REFCLK1 (This is also verified by either uART interface or MEZZ_RD command from the NGCCM menu.). Before moving to the next test, CLEAR_ERR command is used to clear all error counters and verified that they are all 0 by using ERR_STATUS command. As the previous MCLK test was of great importance, the following test is of the same importance as it is performed to check if the control signals are transmitted from the ngCCM when told by the GLIBv2.

- IO (input-output) test basically checks the backplane inputs and outputs via LEDs and switches on the emulator board. As there are only two kinds of input signals, Power Good and the data line of I2C busses which are tested in I2C test, switches are used only for Power Good signal. The test is performed by running the IO test in the NGCCM/TESTS menu. Steps 5 to 8 are performed with switches (as they include Power Good), remaining 23 steps are performed with LEDs. See Figure 7.15 for a sample output of IO test and Table 7.1 for the description of output signals.

  In each step of the test, the indicated LED is expected to light or the indicated switch needs to be set. The steps including SEL-ADDR and CAL-SEL/RM-SEL signals are performed with more attention as they include LEDs both on the emulator board and on the adapter board.

```
[ HB> io

[  What version of motherboard? (pre-production = 0, production = 1):  [1]
[  Test with both control boards (ENTER=yes, M=master only, Q=quit)

   NOTE: Control Link is to J15 with J15 as Master

[01/28 Test State: Power Enable (lt only)               (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[02/28 Test State: RESET JTAG LEDS                      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[03/28 Test State: ALL BKP LEDS Off                     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[04/28 Test State: Power Enable (lt only)               (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[05/28 Test State: Set Power Good LT - switch left      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[06/28 Test State: Set Power Good RT - switch left      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[07/28 Test State: Set Power Good LT - switch right     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[08/28 Test State: Set Power Good RT - switch right     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[09/28 Test State: Check GEO ADDR all=R                 (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[10/28 Test State: WTE (rt & lt)                        (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[11/28 Test State: RESET (rt & lt)                      (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[12/28 Test State: RESET-QIE (rt & lt)                  (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[13/28 Test State: PELTIER-EN-A-LT-N                    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[14/28 Test State: PELTIER-EN-B-LT-N                    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[15/28 Test State: ALL BKP LEDS ON (9 LEDs)             (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[16/28 Test State: SEL-ADDR 3/SPR12=000 / CAL-SEL-LT    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[17/28 Test State: SEL-ADDR 3/SPR12=100 / RM-SEL-A-LT   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[18/28 Test State: SEL-ADDR 3/SPR12=010 / RM-SEL-B-LT   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[19/28 Test State: SEL-ADDR 3/SPR12=110 / CAL-SEL-LT    (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[20/28 Test State: SEL-ADDR 3/SPR12=001 / RM-SEL-A-LT   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[21/28 Test State: SEL-ADDR 012=000 / RM-SEL-A-RT       (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[22/28 Test State: SEL-ADDR 012=100 / RM-SEL-B-RT       (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[23/28 Test State: SEL-ADDR 012=010 / CAL-SEL-RT        (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[24/28 Test State: SEL-ADDR 012=110 / RM-SEL-A-RT       (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[25/28 Test State: SEL-ADDR 012=001 / RM-SEL-B-RT       (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[26/28 Test State: ALL SA LEDS Off / CAL-RT / RM-B-LT   (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[27/28 Test State: ALL SEL-ADDR/SPARE LEDS ON (6 LEDs)  (ENTER=proceed, F=prev. fail, S=skip, Q=quit)
[28/28 Test State: Power Enable OFF                     (ENTER=proceed, F=prev. fail, S=skip, Q=quit)

All tested IO reads and writes completed successfully.
```

Figure 7.15. A sample IO test result.

Table 7.1. Backplane signal descriptions for the IO test.

Output Signal	Description
Power Enable:	Enables Backplane Power
Power Good:	Signals that FE cards have Good Power Level
GEO ADDR:	Selects Geographical Address
WTE:	Warning Test Enable for Calibration Purposes
RESET:	General Reset
RESET-QIE:	Beam Zero
PELTIER-EN:	Enables Peltier for SiPMs
SEL-ADDR:	Selects JTAG Address
CAL-SEL:	Selects Calibration Unit
RM-SEL:	Selects Readout Module

The IO test is followed by the I2C test. The aim of the test is checking the stability of the I^2C communication.

- The I^2C bus was designed by Philips to allow easy communication between the components of the PCB. It is implemented in the ngCCM design for the configuration of control board FPGAs and FE boards. The I2C test is performed

by going to the NGCCM/TESTS menu and typing the I2C command. The test goes through all 10 I2C busses and tests reads and writes of I2C. This is done via verifying each slot with 8 test patterns. See Figure 7.16 for a sample output of I2C test.

```
[ HB> i2c

[ Test all slots (all), half (half) or pick a slot (one) ?  [All]
[  I2C Frequency (Hz):  [80000]

    NOTE: Turning on the backplane power to power the I2C buffers.
    Enabling power on backplane ...

      Backplane PWR-GOOD = 1


  NOTE: Control Link is to J15 with J15 as Master


NOTE: Data verifies stop with the first data mismatch for each slot/eeprom.

Testing Pri. Slot: 1 while verifying all slots with each test pattern.

    1: Slot  1  Pri. I2C Addr: 0xA0  expData[0]: 0x00
0000  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0010  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0020  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0030  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0040  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0070  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0080  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
0090  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00a0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00b0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00c0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00d0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00e0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
00f0  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 : ................ :
```

Figure 7.16. A sample I2C test result showing the first test pattern used to verify bus 1.

After the I2C communication is checked and making sure all I2C reads and writes is completed successfully, the control signals between two control boards are tested with B2B test.

- B2B, board-to-board, test is performed by going to the NGCCM/TESTS menu and typing the B2B command. The main purpose of the test is checking all board-to-board signals by changing the Master/Slave designation of the two control boards J15 and J14. This function is of great importance as it enables Master/Slave switch from either control board in case of the optical link of one control board fails. See Figure 7.17 for a sample output of B2B test.

After the B2B test is completed successfully, the next step is reading out the OneWire Temperature IDs and ngCCM Temperatures, which are verified to be less

```
[ HB> b2b

 Test being run while GLIB connected to: J15 (mezz) with J14 (smezz)
 Master is currently J15 and will be restored at the end of the test
 FPGA Version: 05:06

01/18 Test: Normal Mode
02/18 Test: J14 Master mezz  -> smezz
03/18 Test: J14 Master mezz <-  smezz
04/18 Test: J14 Master mezz <-> smezz
05/18 Test: Clear MASTER_J14_ENABLE
06/18 Test: J14 Master mezz <-> smezz
07/18 Test: Reset Mezz  1
08/18 Test: Reset Smezz 1
09/18 Test: J14 Master mezz <-> smezz
10/18 Test: Reset Smezz 2
11/18 Test: Reset Mezz  2
12/18 Test: J14 Master mezz <-> smezz
13/18 Test: Reset Mezz & Smezz 1
14/18 Test: J14 Master mezz  -> smezz
15/18 Test: Reset Mezz & Smezz 2
16/18 Test: J14 Master mezz <-  smezz
17/18 Test: Reset Mezz & Smezz 3
18/18 Test: Return to Normal Mode

All 18 performed B2B tests completed successfully.
```

Figure 7.17. A sample B2B test result.

than 50°C. This is done by running the TEMP command in the NGCCM menu in GLIBtool. See Figure 7.18 for a sample output of the TEMP command.

```
 HB> temp

J14:
     ID #1:  0x289dc8610a00008c   Ur1:  75  Ur2:  70  TEMP:  39.81 C (103.66 F)
J15:
     ID #1:  0x28370f620a0000e4   Ur1:  75  Ur2:  70  TEMP:  40.94 C (105.69 F)
J16:
     ID #1:  0x283ddf610a0000fd   Ur1:  75  Ur2:  70  TEMP:  41.12 C (106.03 F)
```

Figure 7.18. An example of the TEMP command output.

Next is reading the mezzanine registers in both control boards. This is done by MEZZ_DUMP command in the NGCCM menu and the command dumps all known registers inside mezzanine FPGA via I2C. J15 mezzanine registers are read by using I2C bus 11 and device address 0× 12 and J14 registers are read by using I2C bus 12 and device address 0 ×12. The output gives information about the REFCLK selection, firmware version number, error counts and many other important details. A sample output can be seen in Figure B.3 & Figure B.4. The mezzanine registers are read for both control boards and recorded in the database.

The ngCCM power consumption is checked again but this time with a low voltage input to test the low end of the input voltage range. The power supply voltage is lowered to 6.0 V and the current limit is raised to 3.0 A. Then, backplane power is

enabled by typing PWR_ON command which is followed by ADC command. The ADC output is checked in the same manner as before except that the input voltage on all three boards is now expected to be ≥ 5.5 V. After this, there is only one step left for the power consumption check which is performed when the backplane power is disabled. PWR_OFF command in the NGCCM menu is used to disable backplane power and this is followed by ADC command. The output is checked in the same manner but with different specifications for 3.3 V power. 3.3 V power is verified to be less than 1.5 W which drops the total input power by 5 W. Hence, total input power when the backplane is disabled for a low voltage input is expected to be less than 8.0 W.

If the module meets all the specifications given above, the power supply voltage is returned back to 9.5 V and the current limit is set back to 2.5 A. The tests proceed with JTAG test, which is the last test to perform through the primary link of the ngCCM (through J15 primary control board). This is a test of great importance as well because it tests one of the most crucial arguments of Phase-I upgrade by testing the remote programming of the boards.

- JTAG test is performed by going to the NGCCM/TESTS menu and by typing JTAG. The test consists of six steps and there are two things that are tested. First is the remote programming of QIE cards in RMs and second is the remote programming of the ngCCM control boards. In both cases, the FPGAs are not programmed as there is a limit to how many times an FPGA can be programmed. Remote programming of QIEs is tested in the first four steps by using an evaluation board and by a VERIFY test instead of a full program. In each of these four steps, the evaluation board has a certain blink pattern to its LEDs installed on it which are ignited when a JTAG is successfully initiated. Remote programming of the control boards is tested in the last two steps by a BYPASS test to make sure overall JTAG protocol is working, instead of a full program (the BYPASS test exercises the same signals as programming). The last two steps are to guarantee that in case of a corruption of firmware on any of these control boards, the other can be used to reprogram the corrupted firmware and they are performed without

the JTAG evaluation board. These two steps are completed successfully if the returned DSN from the BYPASS test can be manually verified at the end of the test. See Figure B.5-B.10 for sample outputs of the JTAG test.

After all the tests above are performed and succeeded, the control link is switched to the secondary control board by moving the MM fiber to J14 MM VTRx and using the MASTER_SWITCH command in GLIBtool under NGCCM menu to make J14 master and each step is repeated for this secondary link.

8. CONCLUSION

The work reported on this thesis covers the assembly and production tests of the new generation Clock and Control Modules for the HB. ngCCMs are front end modules designed under the requirements of the Phase-I upgrade to replace their Phase-0 versions called Clock, Control and Monitor modules. CCMs are four-board modules with each board performing a particular task and they have no redundant control links. Lacking redundant links imposes a risk for the control link between the front end and the back end which could result in loss of data. ngCCMs are designed with the risks of old versions in mind hence they introduce a redundancy scheme by increasing the number of the modules per readout box to two and including two control boards in each module; one master and one slave. They are performing the same tasks as before; distributing the LHC clock and controlling and monitoring the front end electronics.

During this assembly and testing process, three major problems were encountered. First problem was the loss of MCLK signals. Out of the first ten assembled modules, only one seemed to have a proper set of MCLKs and the remaining nine were missing 2 of the 12 clocks. This has been investigated in various ways; replacing the front end emulator board, replacing the boards in the module, or replacing the probes used to monitor the signals. However, the problem was diagnosed when compared the housing used in the good module and the housings used in the bad ones. As mentioned in section 7.2.1, the bottom plate of the housing in the good module had a cutoff whereas the remaining nine housings were missing this cutoff causing the MCLK pins to short; i.e., loss of the clock signal. After this diagnosis, all the housings missing the cutoff were modified with proper cutoffs. The second and the third problems were the overheating of two components on the clock and control boards; DC/DC converters on the clock boards and VTRxs on the control boards. After taking temperature measurements on both components, they showed temperature levels close to 50°C degrees, which is the temperature threshold. This is solved by adding extra cooling components. A custom T-shaped heat sink to be used under the DC/DC modules and a cooling fin to be placed over the VTRx were designed and added to the ngCCM housing. Both components

were complemented with thermal pads for better thermal conduction and better heat removal.

Within the scope of this work, 111 clock boards and 244 control boards were tested and assembled. Out of this many boards, 4 clock and 4 control boards failed the tests. In all cases, there were manufacturing faults and the boards were sent back to the vendor for repairing.

100 modules built and tested from the properly tested and assembled boards and 92 modules passed all the production tests. Modules that passed these tests were passed on to a burn-in period of three weeks and after passing the burn-in, the modules will be installed in the detector starting from June 2019.

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APPENDIX A: PHASE-0 AND PHASE-I READOUT SCHEMES

The overall readout circuitry of the barrel calorimeter is divided into two as Front-End Electronics, sitting on the detector and operating in a 3.8 T magnetic field environment and Back-End Electronics located off detector. The following figures show the overall readout schemes for the Phase-0 or Legacy system and the Phase-I system, respectively.

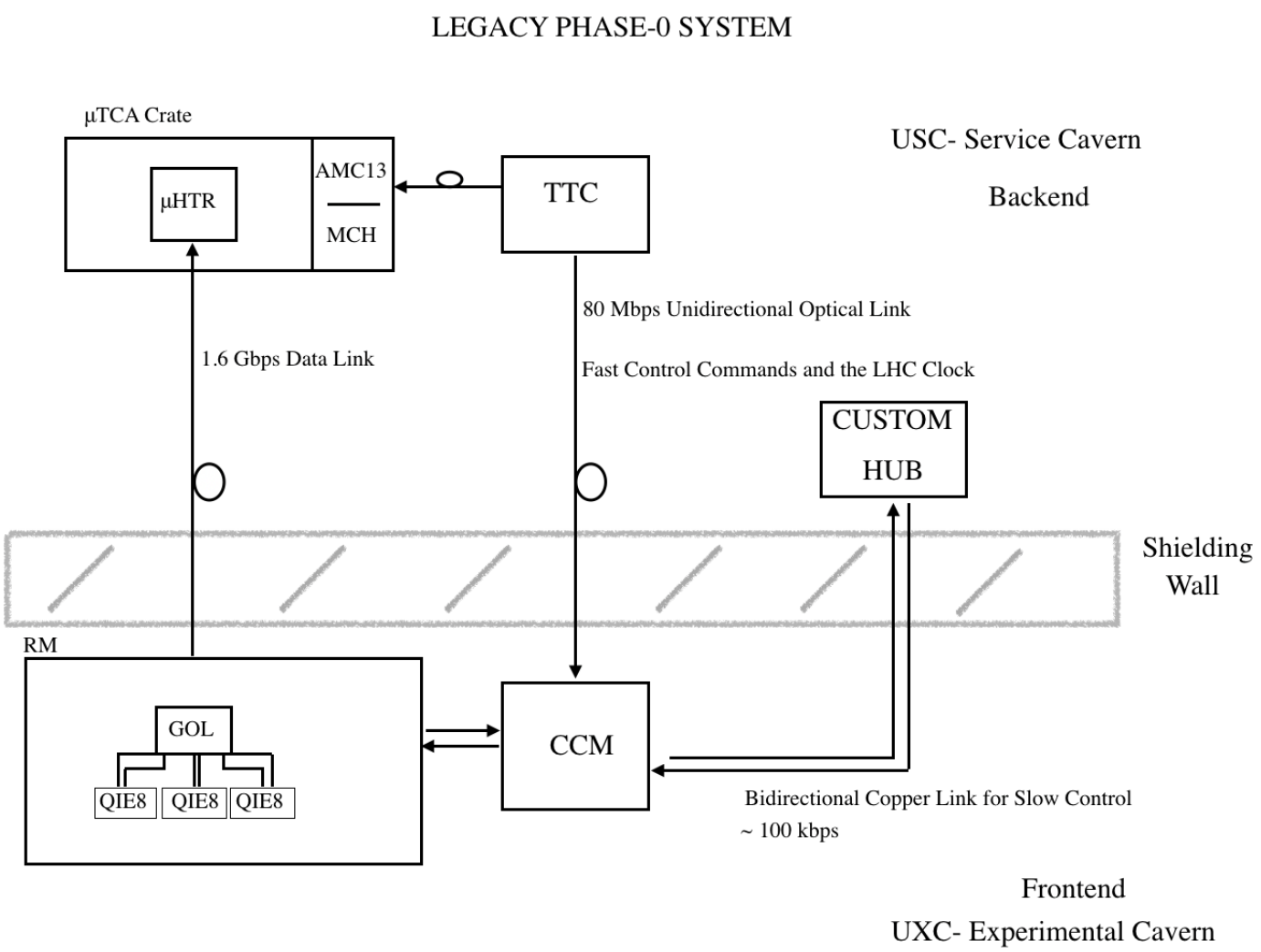

Figure A.1. The overall communication scheme of the HCAL in the old Phase-0/Legacy System.

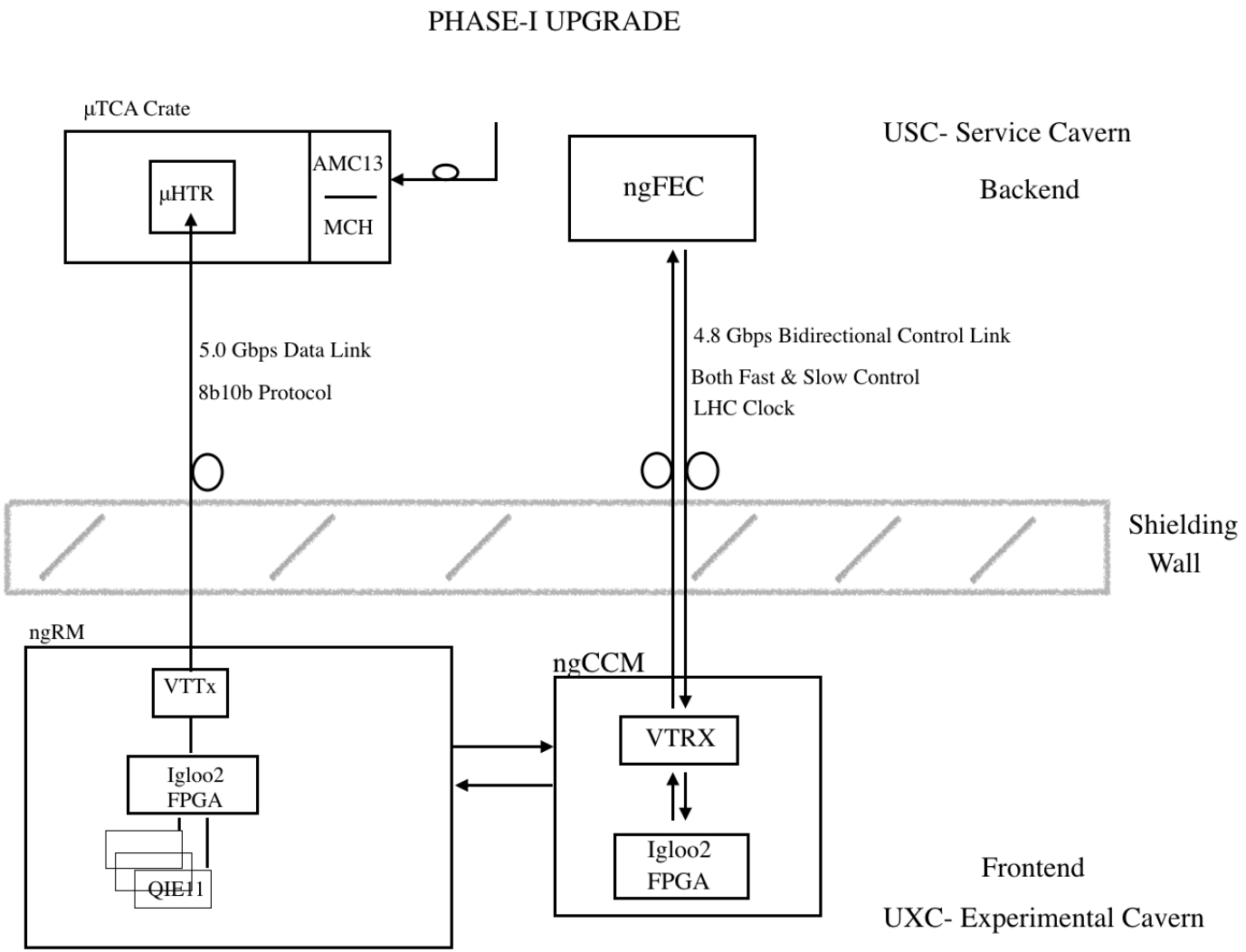

Figure A.2. The upgraded Phase-I version of the overall communication scheme of the HCAL.

APPENDIX B: SAMPLE TEST OUTPUTS

```
-bash-4.2$ ./gbtTest.py
PyChips v1.4.1
Executed with: ./gbtTest.py


ngCCM is ON: 9.4850 V 1.1289 A

--======================================--
  Opening GLIB with IP 192.168.0.111
--======================================--

->           SYSTEM         USER
->         ----------    ----------
-> brd  :     GLIB          USER
-> sys  :     LAB           VTS
-> ver  :    2.0.0         3.0.8
-> date :   5/1/2016     17/1/2019

GLIB GBT Rates: TX=Half (2.4Gbps) / RX=Half (2.4Gbps)

ngCCM Info:
Master J15 - FW v5.6 - 19012922 - DSN: 6BB67F7C-8B0D5583-B9B7B2F7-9431DCCF
Slave  J14 - FW v5.6 - 19012932 - DSN: 993173BD-E2501CFB-31769E4F-C58D2881


Run GBT Test w/ num_iters=10, wait_clear=2, wait_check=10
Can stop GBT test and get summary by pressing Ctrl-C while test is waiting.

  NOTE: Control Link is to J15 with J15 as Master

  NOTE: Direct is using REFCLK1/1 and Neighbor is using REFCLK1/1

1/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   1 out of   1 PASSED with No Errors after GBT Interruption

2/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   2 out of   2 PASSED with No Errors after GBT Interruption

3/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   3 out of   3 PASSED with No Errors after GBT Interruption

4/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   4 out of   4 PASSED with No Errors after GBT Interruption
```

Figure B.1. A sample output of the GBT test.

```
5/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   5 out of   5 PASSED with No Errors after GBT Interruption

6/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   6 out of   6 PASSED with No Errors after GBT Interruption

7/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   7 out of   7 PASSED with No Errors after GBT Interruption

8/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   8 out of   8 PASSED with No Errors after GBT Interruption

9/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

So Far:   9 out of   9 PASSED with No Errors after GBT Interruption

10/10 Power Cycling ngCCM with off time=1.50s  .P.W..C.........

 GLIB RX <- ngCCM TX Error Count:                0 (w/o DV:           0)
 GLIB TX -> ngCCM RX Error Count:                0 (pre-FEC:          0){RX PLL Delay: -30}
 GLIB TX -> ngCCM RX Error Count last ms:        0 / PLL Unlock:      0

 ngCCM J15 <- J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 <- J14 Error Count last ms:           0 / PLL Unlock:      0

 ngCCM J15 -> J14 Error Count:                   0 (pre-FEC:          0){RX PLL Delay:   0}
 ngCCM J15 -> J14 Error Count last ms:           0 / PLL Unlock:      0

 Neigh. TX -> J14 Error Count:              ------ (pre-FEC:          0){RX PLL Delay: -30}
 Neigh. TX -> J14 Error Count last ms:      ------ / PLL Unlock:      0

RESULT:  10 out of  10 PASSED with No Errors after GBT Interruption
```

Figure B.2. A sample output of the GBT test.

```
 HB> mezz_d
  I2C Bus Number [Backplane: 1-10, NGCCM Master: 11, Slave: 12]:  [11]
  I2C Frequency (Hz):  [80000]
  Mezzanine I2C Device Address (0x prefix for hex):  [0x12]

Mezz Reg 0:
SERDES REFCLK:         REFCLK1
GEO ADDR:              2 (J15)

Mezz Reg 1:
Bitslip Num:           10
Require Bitslip Lock:  YES
Comm Good TX:          YES
Comm Good RX:          YES


Mezz Reg 2:
RX Error Count Reset:  Run
FlashPro Mode Enabled: No
CTL LED OFF:           No
DEVRST:                No
JTAG - RM Select A:    No
JTAG - RM Select B:    No
JTAG - Cal Select:     No
JTAG - Igloo2 Select:  No

Mezz Reg 3:
TX PLL Lock Lost Count Clear: No
RX PLL Lock Lost Count Clear: No
Reset 1-Wire Controller:      No
FastCtrlCount Clear:          No
Orbit Status Clear:           No
WTE   Status Clear:           No
PWR Fault Count Clear:        No
Peltier Disable Count Clear:  No

Mezz Reg 4:
FPGA Version: 05:03

SERDES LANE:              0 / VTRx
SERDES NUM LINKS:         2
SERDES RX Align Clock En: YES
SERDES TX Invert (MM):    YES
TMR F/F Enabled:          YES
In Slave Mode:            No
Board Revision ID:        5
FPGA Design Version:      503 (0x01F7)

Board ID:     'HEHB ngCCM'

Mezz Reg 5:
BKP Pwr1 Enabled:      No
BKP Pwr1 Powered:      No
BKP Pwr1 Fault:        No
BKP Pwr1 Power Good:   No

BKP Pwr2 Enabled:      No
BKP Pwr2 Powered:      No
BKP Pwr2 Fault:        No
BKP Pwr2 Power Good:   No

BKP PwrK Enabled:      No
BKP PwrK Powered:      No
BKP PwrK Fault:        No
BKP PwrK Power Good:   No

BKP Power Fault Count: 0

CNTRM JP 1 DEPRESSED:  YES
CNTRM JP 2 DEPRESSED:  YES
CNTRM JP 3 DEPRESSED:  No
CNTRM JP 4 DEPRESSED:  No

TEST SW 1  ON:   No  (Disable Bitslip Lock)
TEST SW 2  ON:  YES  (Enable UART)
TEST SW 3  ON:  YES  (Invert VTRx TX)
TEST SW 4  ON:  YES  (HB Mode)
```

Figure B.3. A sample output of the MEZZ_DUMP command.

```
VTRx CTL MOD ABSENT:   No
VTRx CLK MOD ABSENT:   YES
SlowSig1 (HF):         0
SlowSig2 (HF):         0

RX Bitslip Num:        0:10
RX PLL Delay Num:      -30

F2F spare_p_in:        1
F2F spare_n_in:        0
F2K clk_mux_alt_in:    0

Peltier En IN (4-1):   0 0 0 0
Peltier Disable Count: 1


Mezz Reg 6:
Seconds since POR:             62
TMR Error Count:               0
TX PLL Lock Lost Count:        1
RX PLL Lock Lost Count:        1
FPGA Silicon Signature:        0x18082421

Mezz Reg 7:
FPGA Device Serial Number:     6BB67F7C-8B0D5583 B9B7B2F7-9431DCCF

Mezz Reg 8:
RX Data Error (RSDEC) Count:   16365
RX Data Error (RSDEC) last ms: 0
RX Data Error (PRBS) Count:    1
RX Data Error (PRBS) last ms:  0

Mezz Reg 9:
Clock Count:           1246951539
QIE Reset (BC0) Count:          0
WTE Count:                      0

Mezz Reg 10:
 Orbit / BC0 / QIE Reset Monitoring
   Missing:      *YES*
   Count:             0
   Min:               0
   Max:               0
   Shift:             0

Mezz Reg 11:
 WTE Monitoring
   Missing:      *YES*
   Count:             0
   Min:               0
   Max:               0
   Shift:             0

Mezz Reg 249:
MASTER J14 ENABLE:     No
CLK MUX SEL (unused):  A
MASK PWR GOOD:         No

Mezz Reg 250:
DEBUG Byte:            0x00

Mezz Reg 251:
RX PLL DELAY SET:      -30
RX PLL DELAY LOCKED:   No

Mezz Reg 252:
RX BITSLIP SET:        10
RX PHASE LAG SET:       0

Mezz Reg 253:
VTRx CTL TX CAN NO LONGER BE CHANGED
VTRx CLK TX DISABLE:   No
RX PLL REALIGN:        No
F2F SPARE N Out:       0
F2K CLK ALT MUX:       B/A

Mezz Reg 254:
VTRx MUX:              CTL

Mezz Reg 255:
Scratch Register:      0x00
```

Figure B.4. A sample output of the MEZZ_DUMP command.

```
 HB> jtag
  NOTE: Control Link is to J15 with J15 as Master

Select the JTAG Target (PROD1 or EVAL) ?  [EVAL]

01/06 Test PROGRAM   of QIE-RT (via J13/J16) slots 24-27 using J5:

       1. Power off the ngCCM
       2. Verify that the Igloo2 Eval Board (EVB) is powered from the emulator board and its switch is toward the power conn.
       3. Connect "J5" on FE emulator to JTAG conn. on EVB with a ribbon cable.
       4. Power ON the ngCCM and Igloo2 Eval Board (EVB) together.

     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
              message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


Jam STAPL Player Version 2.5 (20040526)
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file: "Igloo2_EVB_LEDS_incr1.stp", len: 962726
CRC matched: CRC value = 4D37
Export: key = "JAM_STATEMENT_BUFFER_SIZE", value = 2279
NOTE "CREATOR" = "FlashPro Version: v11.5"
NOTE "CAPTURE" = "11.5.0.26"
NOTE "DEVICE" = "M2GL010T"
NOTE "PACKAGE" = "M2GL010T-fg484"
NOTE "DATE" = "2015/02/12"
NOTE "TIME" = "14:33:41"
NOTE "STAPL_VERSION" = "JESD71"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8031CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "Igloo2_EVB_LEDS_incr1"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "2C4B"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "00000000"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Error: memory corruption detected for allocation #261... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 00827144
Export: key = "CRCERR: ", 1 bits, value = HEX 0
Export: key = "EDCERR: ", 1 bits, value = HEX 1
TEMPGRADE: ROOM
Export: key = "VPPRANGE: ", 3 bits, value = HEX 7
VPPRANGE: HIGH
Export: key = "TEMP: ", 8 bits, value = HEX 40
Export: key = "VPP: ", 8 bits, value = HEX 61
Programming FPGA Array and eNVM...
Export: key = "PERCENT_DONE", value = 4
Export: key = "PERCENT_DONE", value = 8
Export: key = "PERCENT_DONE", value = 12
Export: key = "PERCENT_DONE", value = 16
Export: key = "PERCENT_DONE", value = 21
Export: key = "PERCENT_DONE", value = 25
Export: key = "PERCENT_DONE", value = 29
Export: key = "PERCENT_DONE", value = 33
Export: key = "PERCENT_DONE", value = 37
Export: key = "PERCENT_DONE", value = 42
Export: key = "PERCENT_DONE", value = 46
Export: key = "PERCENT_DONE", value = 50
Export: key = "PERCENT_DONE", value = 54
Export: key = "PERCENT_DONE", value = 58
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 67
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 75
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 84
Export: key = "PERCENT_DONE", value = 88
Export: key = "PERCENT_DONE", value = 92
Export: key = "PERCENT_DONE", value = 96
Export: key = "Fabric component digest", 256 bits, value = HEX D769B81B432B95BAC6FD4D7B9082024850CFA00C9A9783B2EAF2DD729AA9342F
Export: key = "eNVM component digest", 256 bits, value = HEX C2433AFC67C5C5750DCF5D7ECC2CF2B0919AE45C6AEBDFA1F100993037122765
================================================================================
Export: key = "DSN", 128 bits, value = HEX 03E8AA010000CD5A0023000C001E0022
================================================================================
Error: memory corruption detected for allocation #353... bad end guard
Exit code = 0... Success
Elapsed time = 00:00:50
Memory Usage Info: peak memory usage = 2214193d (2163KB)
Memory Usage Info: peak allocations = 355


     JTAG action "PROGRAM" with "Igloo2_EVB_LEDS_incr1.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Verify that the EVB LEDs show this pattern: Single LED turned ON from right to left (Pass or Fail) pass
```

Figure B.5. A sample output of the JTAG test.

```
02/06 Test VERIFY    of QIE-RT (via J13/J16) slots 6-9 using J5:

     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
              message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


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file: "Igloo2_EVB_LEDS_incr1.stp", len: 962726
CRC matched: CRC value = 4D37
NOTE "CREATOR" = "FlashPro Version: v11.5"
NOTE "CAPTURE" = "11.5.0.26"
NOTE "DEVICE" = "M2GL010T"
NOTE "PACKAGE" = "M2GL010T-fg484"
NOTE "DATE" = "2015/02/12"
NOTE "TIME" = "14:33:41"
NOTE "STAPL_VERSION" = "JESD71"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8031CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "Igloo2_EVB_LEDS_incr1"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "2C4B"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "00000000"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Error: memory corruption detected for allocation #261... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 00826E44
Export: key = "CRCERR: ", 1 bits, value = HEX 0
Export: key = "EDCERR: ", 1 bits, value = HEX 0
TEMPGRADE: ROOM
Export: key = "VPPRANGE: ", 3 bits, value = HEX 7
VPPRANGE: HIGH
Export: key = "TEMP: ", 8 bits, value = HEX 40
Export: key = "VPP: ", 8 bits, value = HEX 61
Verifying FPGA Array and eNVM...
Export: key = "PERCENT_DONE", value = 4
Export: key = "PERCENT_DONE", value = 8
Export: key = "PERCENT_DONE", value = 12
Export: key = "PERCENT_DONE", value = 16
Export: key = "PERCENT_DONE", value = 21
Export: key = "PERCENT_DONE", value = 25
Export: key = "PERCENT_DONE", value = 29
Export: key = "PERCENT_DONE", value = 33
Export: key = "PERCENT_DONE", value = 37
Export: key = "PERCENT_DONE", value = 42
Export: key = "PERCENT_DONE", value = 46
Export: key = "PERCENT_DONE", value = 50
Export: key = "PERCENT_DONE", value = 54
Export: key = "PERCENT_DONE", value = 58
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 67
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 75
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 84
Export: key = "PERCENT_DONE", value = 88
Export: key = "PERCENT_DONE", value = 92
Export: key = "PERCENT_DONE", value = 96
================================================================================
Export: key = "DSN", 128 bits, value = HEX 03E8AA010000CD5A0023000C001E0022
================================================================================
Error: memory corruption detected for allocation #337... bad end guard
Exit code = 0... Success
Elapsed time = 00:00:40
Memory Usage Info: peak memory usage = 2214193d (2163KB)
Memory Usage Info: peak allocations = 355


     JTAG action "VERIFY" with "Igloo2_EVB_LEDS_incr1.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Verify that the EVB LEDs show this pattern: Single LED turned ON from right to left (Pass or Fail) pass
```

Figure B.6. A sample output of the JTAG test.

```
03/06 Test PROGRAM   of QIE-LT (via J12/J15) slots 1-4 using J6:

       1. Power off the ngCCM
       2. Verify that the Igloo2 Eval Board (EVB) is powered from the emulator board and
its switch is toward the power conn.
       3. Connect "J6" on FE emulator to JTAG conn. on EVB with a ribbon cable.
       4. Power ON the ngCCM and Igloo2 Eval Board (EVB) together.

     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
              message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


Jam STAPL Player Version 2.5 (20040526)
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file: "Igloo2_EVB_LEDS_live.stp", len: 962725
CRC matched: CRC value = 32BC
NOTE "CREATOR" = "FlashPro Version: v11.5"
NOTE "CAPTURE" = "11.5.0.26"
NOTE "DEVICE" = "M2GL010T"
NOTE "PACKAGE" = "M2GL010T-fg484"
NOTE "DATE" = "2015/02/12"
NOTE "TIME" = "14:22:38"
NOTE "STAPL_VERSION" = "JESD71"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8031CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "Igloo2_EVB_LEDS_live"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "829D"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "00000000"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Error: memory corruption detected for allocation #261... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 00826E44
Export: key = "CRCERR: ", 1 bits, value = HEX 0
Export: key = "EDCERR: ", 1 bits, value = HEX 0
TEMPGRADE: ROOM
Export: key = "VPPRANGE: ", 3 bits, value = HEX 7
VPPRANGE: HIGH
Export: key = "TEMP: ", 8 bits, value = HEX 40
Export: key = "VPP: ", 8 bits, value = HEX 61
Programming FPGA Array and eNVM...
Export: key = "PERCENT_DONE", value = 4
Export: key = "PERCENT_DONE", value = 8
Export: key = "PERCENT_DONE", value = 12
Export: key = "PERCENT_DONE", value = 16
Export: key = "PERCENT_DONE", value = 21
Export: key = "PERCENT_DONE", value = 25
Export: key = "PERCENT_DONE", value = 29
Export: key = "PERCENT_DONE", value = 33
Export: key = "PERCENT_DONE", value = 37
Export: key = "PERCENT_DONE", value = 42
Export: key = "PERCENT_DONE", value = 46
Export: key = "PERCENT_DONE", value = 50
Export: key = "PERCENT_DONE", value = 54
Export: key = "PERCENT_DONE", value = 58
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 67
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 75
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 84
Export: key = "PERCENT_DONE", value = 88
Export: key = "PERCENT_DONE", value = 92
Export: key = "PERCENT_DONE", value = 96
Export: key = "Fabric component digest", 256 bits, value = HEX
31499640A1BC2B600A2ED643D46FE65C3A6AD70B0DA36A66E72822D7176F125C
Export: key = "eNVM component digest", 256 bits, value = HEX
C2433AFC67C5C5750DCF5D7ECC2CF2B0919AE45C6AEBDFA1F100993037122765
================================================================================
Export: key = "DSN", 128 bits, value = HEX 03E8AA010000CD5A0023000C001E0022
================================================================================
Error: memory corruption detected for allocation #353... bad end guard
Exit code = 0... Success
Elapsed time = 00:00:51
Memory Usage Info: peak memory usage = 2214193d (2163KB)
Memory Usage Info: peak allocations = 355


     JTAG action "PROGRAM" with "Igloo2_EVB_LEDS_live.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Verify that the EVB LEDs show this pattern: LEDs "moving" from outside to inside and
back outside (Pass or Fail) pass
```

Figure B.7. A sample output of the JTAG test.

```
04/06 Test VERIFY    of QIE-LT (via J12/J15) slots 17-22 using J6:

     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
              message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


Jam STAPL Player Version 2.5 (20040526)
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file: "Igloo2_EVB_LEDS_live.stp", len: 962725
CRC matched: CRC value = 32BC
NOTE "CREATOR" = "FlashPro Version: v11.5"
NOTE "CAPTURE" = "11.5.0.26"
NOTE "DEVICE" = "M2GL010T"
NOTE "PACKAGE" = "M2GL010T-fg484"
NOTE "DATE" = "2015/02/12"
NOTE "TIME" = "14:22:38"
NOTE "STAPL_VERSION" = "JESD71"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8031CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "Igloo2_EVB_LEDS_live"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "829D"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "00000000"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Error: memory corruption detected for allocation #261... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 00826E44
Export: key = "CRCERR: ", 1 bits, value = HEX 0
Export: key = "EDCERR: ", 1 bits, value = HEX 0
TEMPGRADE: ROOM
Export: key = "VPPRANGE: ", 3 bits, value = HEX 7
VPPRANGE: HIGH
Export: key = "TEMP: ", 8 bits, value = HEX 40
Export: key = "VPP: ", 8 bits, value = HEX 61
Verifying FPGA Array and eNVM...
Export: key = "PERCENT_DONE", value = 4
Export: key = "PERCENT_DONE", value = 8
Export: key = "PERCENT_DONE", value = 12
Export: key = "PERCENT_DONE", value = 16
Export: key = "PERCENT_DONE", value = 21
Export: key = "PERCENT_DONE", value = 25
Export: key = "PERCENT_DONE", value = 29
Export: key = "PERCENT_DONE", value = 33
Export: key = "PERCENT_DONE", value = 37
Export: key = "PERCENT_DONE", value = 42
Export: key = "PERCENT_DONE", value = 46
Export: key = "PERCENT_DONE", value = 50
Export: key = "PERCENT_DONE", value = 54
Export: key = "PERCENT_DONE", value = 58
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 67
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 75
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 84
Export: key = "PERCENT_DONE", value = 88
Export: key = "PERCENT_DONE", value = 92
Export: key = "PERCENT_DONE", value = 96
================================================================================
Export: key = "DSN", 128 bits, value = HEX 03E8AA010000CD5A0023000C001E0022
================================================================================
Error: memory corruption detected for allocation #337... bad end guard
Exit code = 0... Success
Elapsed time = 00:00:40
Memory Usage Info: peak memory usage = 2214193d (2163KB)
Memory Usage Info: peak allocations = 355


     JTAG action "VERIFY" with "Igloo2_EVB_LEDS_live.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Verify that the EVB LEDs show this pattern: LEDs "moving" from outside to inside and
back outside (Pass or Fail) pass
```

Figure B.8. A sample output of the JTAG test.

```
05/06 Test BYPASS_TEST of ngCCM J13/J16 slave control board:

       1. Power off the ngCCM and the Igloo2 Eval Board (EVB) together
       2. Remove EVB ribbon cable from FE emulator.
       3. Be sure that NO JTAG/FlashPro programmers are connected to either Control board.
       4. If fiber is plugged into the secd. control (ie. J14), move it to the prim.
control (ie. J15).
       5. Power ON the ngCCM.
     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
              message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


Jam STAPL Player Version 2.5 (20040526)
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file: "HBHE_CCC_bypass_test.stp", len: 3869572
CRC matched: CRC value = 4867
NOTE "CREATOR" = "FlashPro Version: 11.8 SP3"
NOTE "CAPTURE" = "11.8.3.6"
NOTE "DEVICE" = "M2GL050T"
NOTE "PACKAGE" = "M2GL050T-fg484"
NOTE "DATE" = "2018/03/01"
NOTE "TIME" = "20:54:59"
NOTE "STAPL_VERSION" = "JESD71-FIXED"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8021CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "HBHE_CCC"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "54EC"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "18022803"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Export: key = "IDCODE", 32 bits, value = HEX 4F8021CF
Family: Igloo2
Product:      M2GL050
Error: memory corruption detected for allocation #312... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 007E6844
Export: key = "CRCERR", 1 bits, value = HEX 0
Export: key = "EDCERR", 1 bits, value = HEX 0
Testing BYPASS...
Export: key = "PERCENT_DONE", value = 7
Export: key = "PERCENT_DONE", value = 15
Export: key = "PERCENT_DONE", value = 23
Export: key = "PERCENT_DONE", value = 31
Export: key = "PERCENT_DONE", value = 39
Export: key = "PERCENT_DONE", value = 47
Export: key = "PERCENT_DONE", value = 55
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 87
Export: key = "PERCENT_DONE", value = 95
BYPASS Test Complete.
================================================================================
Export: key = "DSN", 128 bits, value = HEX 993173BDE2501CFB31769E4FC58D2881
================================================================================
Exit code = 0... Success
Elapsed time = 00:00:11
Memory Usage Info: peak memory usage = 9009805d (8799KB)
Memory Usage Info: peak allocations = 513


     JTAG action "BYPASS_TEST" with "HBHE_CCC_bypass_test.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Manually verify that the reported DSN from above DEVICE_INFO is: 993173BD-E2501CFB
31769E4F-C58D2881 (Pass or Fail) pass

     Verify that the LEDs show this pattern: ngCCM secd. control board LEDs are blinking
as expected (Pass or Fail) p
```

Figure B.9. A sample output of the JTAG test.

```
06/06 Test BYPASS_TEST of ngCCM J12/J15 slave control board:

     NOTE: HB Version of ngCCMJTAGSelect()

       1. Move GLIBv2 Fiber to Secondary Control Board.
       2. If need to switch b/w MM and SM SFP, power down the GLIBv2 while LEAVING THE
ngCCM POWERED.
       3. Power ON the GLIB if swapping SFPs.
     Once ready, make your selection (ENTER=proceed, S=skip, Q=quit)

     NOTE: May see some memory corruption errors reported and they can be ignored.
     NOTE: Each JTAG action can take several minutes but a periodic "PERCENT_DONE"
              message will indicate that the action is progressing.

     NOTE: HB Version of ngCCMJTAGSelect()


Jam STAPL Player Version 2.5 (20040526)
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file: "HBHE_CCC_bypass_test.stp", len: 3869572
CRC matched: CRC value = 4867
NOTE "CREATOR" = "FlashPro Version: 11.8 SP3"
NOTE "CAPTURE" = "11.8.3.6"
NOTE "DEVICE" = "M2GL050T"
NOTE "PACKAGE" = "M2GL050T-fg484"
NOTE "DATE" = "2018/03/01"
NOTE "TIME" = "20:54:59"
NOTE "STAPL_VERSION" = "JESD71-FIXED"
NOTE "VENDOR" = "Microsemi Corporation"
NOTE "IDCODE" = "0F8021CF"
NOTE "IDMASK" = "0FFFFFFF"
NOTE "DESIGN" = "HBHE_CCC"
NOTE "DESIGN_DIRECTORY" = ""
NOTE "CHECKSUM" = "54EC"
NOTE "SECURITY" = "Disable"
NOTE "ALG_VERSION" = "2"
NOTE "MAP_VERSION" = "0"
NOTE "TOOL_VERSION" = "1"
NOTE "MAX_FREQ" = "10000000"
NOTE "SILSIG" = "18022803"
NOTE "SPEED_GRAD" = "-1"
NOTE "TEMP_GRAD" = "COM"
NOTE "PLAYER_VERSION_VARIABLE" = "PLAYERVERSIONVARIABLE"
NOTE "PLAYER_VERSION_SW_VARIABLE" = "PLAYERVERSIONSWVARIABLE"
Frequency: 4000000 Hz
Export: key = "IDCODE", 32 bits, value = HEX 4F8021CF
Family: Igloo2
Product:      M2GL050
Error: memory corruption detected for allocation #312... bad end guard
Export: key = "ISC_ENABLE_RESULT", 32 bits, value = HEX 00796444
Export: key = "CRCERR", 1 bits, value = HEX 0
Export: key = "EDCERR", 1 bits, value = HEX 0
Testing BYPASS...
Export: key = "PERCENT_DONE", value = 7
Export: key = "PERCENT_DONE", value = 15
Export: key = "PERCENT_DONE", value = 23
Export: key = "PERCENT_DONE", value = 31
Export: key = "PERCENT_DONE", value = 39
Export: key = "PERCENT_DONE", value = 47
Export: key = "PERCENT_DONE", value = 55
Export: key = "PERCENT_DONE", value = 63
Export: key = "PERCENT_DONE", value = 71
Export: key = "PERCENT_DONE", value = 79
Export: key = "PERCENT_DONE", value = 87
Export: key = "PERCENT_DONE", value = 95
BYPASS Test Complete.
================================================================================
Export: key = "DSN", 128 bits, value = HEX 6BB67F7C8B0D5583B9B7B2F79431DCCF
================================================================================
Exit code = 0... Success
Elapsed time = 00:00:11
Memory Usage Info: peak memory usage = 9009805d (8799KB)
Memory Usage Info: peak allocations = 513


     JTAG action "BYPASS_TEST" with "HBHE_CCC_bypass_test.stp" returned with code: 0

     NOTE: HB Version of ngCCMJTAGSelect()

     Manually verify that the reported DSN from above DEVICE_INFO is: 6BB67F7C-8B0D5583
B9B7B2F7-9431DCCF (Pass or Fail) pass

     Verify that the LEDs show this pattern: ngCCM prim. control board LEDs are blinking
as expected (Pass or Fail) p

All 6 performed JTAG tests completed successfully with 0/6 tests skipped.
```

Figure B.10. A sample output of the JTAG test.