On Chip Reconfigurable CMOS Analog Circuit Design and Automation Against Aging Phenomena: Sense and React

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Performance of analog circuits degrades over time due to several time-dependent degradation mechanisms. Due to the increased aging problems in ever-shrinking dimensions, reliability of complementary metal-oxide-semiconductor analog circuits has become a major concern. Overdesign is a popular aging-aware circuit design approach, where circuit operation is guardbanded by choosing the design point beyond the optimal region. For the sake of reliability, power consumption and chip area are sacrificed in this approach, which is undesirable considering strict energy limitations in modern applications. Conversely, Sense and React (S&R) approach serves the same purpose without any additional power consumption, in which degradation of circuit features is detected by online monitoring and recovered immediately. Furthermore, such systems enable remote control and healing of circuits. However, design of an S&R system is quite complicated. In particular, determination of efficient aging signatures and design of recovery strategy are highly challenging problems. This study thoroughly discusses the design process of S&R systems and proposes computer-aided-design-based design strategies that reduce the designer effort considerably. A novel design automation tool for S&R systems was developed, in which signature selection and recovery determination were integrated. To demonstrate proposed design strategies, two different S&R systems are implemented, simulated, and discussed in detail.

CCS Concepts: • **Hardware → Electronic design automation**; **Software tools for EDA**; **Failure recovery, maintenance and self-repair**; **Aging of circuits and systems**;

Additional Key Words and Phrases: Reliability, aging, sense and react, reconfigurable, design automation, CMOS, CAD, analog, signature selection

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1 INTRODUCTION

Based on rapid advancements in complementary metal-oxide-semiconductor (CMOS) technology, low-power, high-performing, and smaller analog circuits can be achieved. However, the scaling

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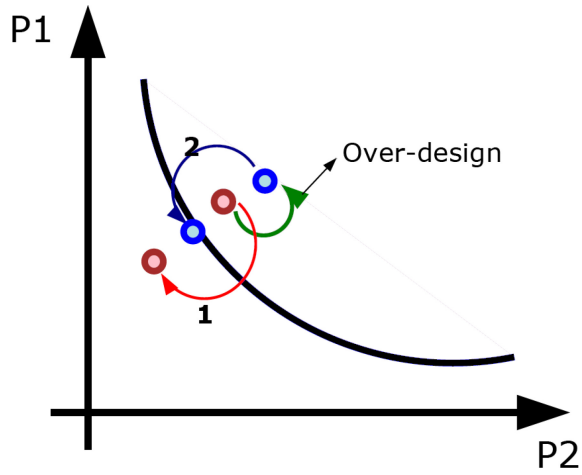

Fig. 1. In the Overdesign approach, the solution point is put beyond the optimal point by sacrificing power and area constraints; thus, the performance of the circuit can be kept within the acceptance region despite the time-dependent degradation.

of supply voltage and threshold voltage has slowed down due to the non-scalability of the subthreshold slope. However, the gate length (L) and the oxide thickness (t_{ox}) has continued to scale down; as a result, there has been an expanding scaling difference between supply voltages and device dimensions. This scaling difference results in a considerable increase in local electrical fields (lateral and vertical), which leads to a considerable increase in electrical stresses on devices. Ultimately, wear-out mechanisms have become more severe, where aging takes place earlier and results in lifetime reduction. Therefore, reliability has become another major design concern for integrated circuits, where circuit designers should consider aging problems during the design process and try to maximize the lifetime as well as circuit performance while minimizing the power consumption and chip area. This new challenge has changed the design problem, where the solution should be oriented on the center of electrical performance, power consumption, area overhead, and reliability objectives.

Analog circuit design robust to aging phenomena has been studied extensively and several precaution-based solutions have been proposed in the literature (Afacan et al. 2016a; Askari and Nourani 2010; Ferreira et al. 2015; Gielen et al. 2008). One of these precaution-based approaches is overdesign, in which the design is guardbanded by anticipating the worst-case performance degradation. In other words, design specifications are satisfied with a large margin; so that, even if transistor parameters change, circuit performance can still be maintained within the design specifications as depicted in Figure 1. Overdesign approach has two major drawbacks. First, power consumption and chip area are sacrificed for the sake of reliability. Second, larger devices are utilized during overdesign, which restricts the use of this approach in some particular applications such as low-power and high-frequency circuits.

Self-healing approach is another way to increase lifetime of analog circuits. This is achieved through healing circuits when they age by activating ad hoc recovery operations (De Wit and Gielen 2012; Gielen et al. 2008, 2012; Lu et al. 2015; Natarajan et al. 2010). Typically, recovery blocks are dormant until an external enable signal awakens them; thus, they do not consume any additional power. Furthermore, area occupation of a typical self-healing system would not be very large, since most of the circuits are digital, and device sizes are considerably smaller. Another

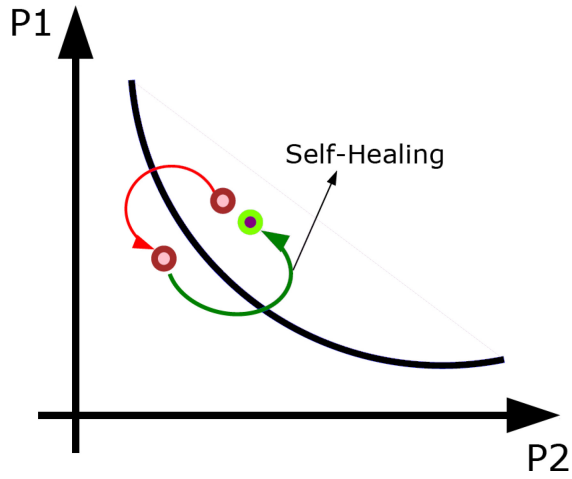

Fig. 2. In the Self-Healing approach, performance losses due to aging can be fully compensated by applying an ad hoc recovery operation; thus, the lifetime of circuit can be considerably increased.

important advantage is that the degraded circuit performance can be fully recovered by a proper recovery operation as illustrated in Figure 2.

Sense and React (S&R) approach is the well-known reconfigurable circuit design approach, in which the design is online monitored and degradation of circuit performance is sensed via a sensor circuit (Chang et al. 2014; Mishra et al. 2002; Qi and Stan 2008). If any degradation occurs, then the recovery is activated and performance loss is compensated. Considering low-power requirement in modern applications, self-healing approach seems to be more suitable compared to a conventional overdesign approach. Furthermore, the self-healing approach also provides remote access, evaluation, and immediate reaction capability during circuit operation; thus, aging-induced failures can be prevented without any operational deduction. There are several problems in the design of S&R systems. The first problem arises during the sense operation, in which it is not practically possible to measure the degradation on any of the circuit performance indicators. Rather, indirect measurements of various electrical quantities (voltage, current, frequency, etc.) are preferred. These quantities are called aging signatures. Considering the measurement cost, number of aging signatures should be minimized. However, if the number of candidate signatures is large, determination of the efficient signature manually could be tedious and computationally expensive. Efficient signature concept is discussed and a signature selection tool presented in Afacan et al. (2016b). However, recovery operation is not considered during the signature selection process in Afacan et al. (2016b), which may cause severe functional failures when operated the healing system. Furthermore, the design of the recovery operation is application-specific, so that only an expert designer can determine a proper recovery operation for a given circuit. A large number of iterations must be conducted to achieve this, which is very time consuming when performed manually.

Contributions of this article can be listed as follows.

- Challenges in the design of S&R systems as a whole from signature selection to recovery operation determination are discussed in detail.
- Efficient signature concept discussed in Afacan et al. (2016b) was revised considering the recovery operation and a modified signature selection approach was proposed.
- A recovery operation determination approach was developed to minimize the designer effort and reduces the total design time.

- The signature selection and recovery determination approaches were integrated; thus, design of an S&R system was made fully automated.
- To demonstrate the developed tool, and demonstrate S&R approach, two different scenarios were configured, designed, simulated, and discussed in detail. One of these scenarios is based on voltage sensing and adaptive biasing while the other utilizes current sensing and reinforcing the critical transistors.

This article is organized in the following main sections. Section 2 reviews the literature with a keen focus on time-based degradation of CMOS circuits as well as IC reliability simulations. S&R approach is explained in detail in Section 3, where signature selection and recovery determination approaches are introduced. The developed design automation tool for S&R system is introduced in Section 4. Circuit level realization of S&R systems is presented and discussed in Section 5. Finally, conclusion of this study is provided in Section 6.

2 BACKGROUND: AGING IN CMOS CIRCUITS

Various wear-out mechanisms can lead to device and circuit degradation over the defined operating lifetime. This results from non-constant aggressive scaling of device dimensions, increasing electric fields, and usage of new materials that enhances the reliability concerns at deep-submicrometer CMOS technology era. Among various degradation mechanisms, Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI) have been reported as the most dominant problems that cause aging in CMOS circuits.

2.1 Hot Carrier Injection

Due to very high lateral fields, carriers can acquire a high level of kinetic energies, yielding higher channel velocities. When the carrier energy level achieves a significantly high value, which is larger than that associated with the lattice in thermal equilibrium, these carriers are called "hot carriers," which can be holes (for p-type) or electrons (for n-type) (Groeseneken et al. 2005). Since the carriers reach this energy near the drain region, impact ionization occurs above the pinch-off region, where hot carriers get trapped into the oxide and create interface states. Traps cause an increase in the threshold voltage and reduce the channel mobility due to scattering along the channel (Groeseneken et al. 2005). The maximum hot carrier damage has traditionally been associated with the peak I_{sub} region, where $V_{gs} \simeq V_{ds}$ (Mourrain et al. 1998). Conventionally, it has been assumed that HCI is negligible in p-channel devices due to lower hole mobility (Radojcic 1984):

$$\Delta I_d = I_d.A.{V_{ds}}^{p_1}.e^{\frac{-E_a}{kT}}.L^{p_2}.t^{p_3}. \tag{1}$$

The degradation in I_d resulting from HCI is modeled by Equation (1). The device-related parameters are fitted by single device stress measurements as presented in Afacan et al. (2016b), where A, p_1, and p_2 are experimentally determined fitting parameters, k is the Boltzmann constant, T is temperature, t is time, and p_3 is the time exponent, which is greater than 0.2 (Wang et al. 2015).

2.2 Negative Bias Temperature Instability

High electrical field across the gate oxide in combination with an elevated temperature leads to an electrochemical reaction in the interface region between silicon and gate oxide (Vattikonda et al. 2006). Due to different lattice structures of monocrystaline silicon and the amorphous oxide, an interface region that consists of a few atomic layers and many dangling bonds, acting as interface states, occurs after gate oxide processing. They can catch carriers, trap them for a certain time, and later emit them back into the channel. Filled interface states shift the threshold voltage. Absence of stress can recover some of the interface traps resulting in partial relaxation (Vattikonda et al.

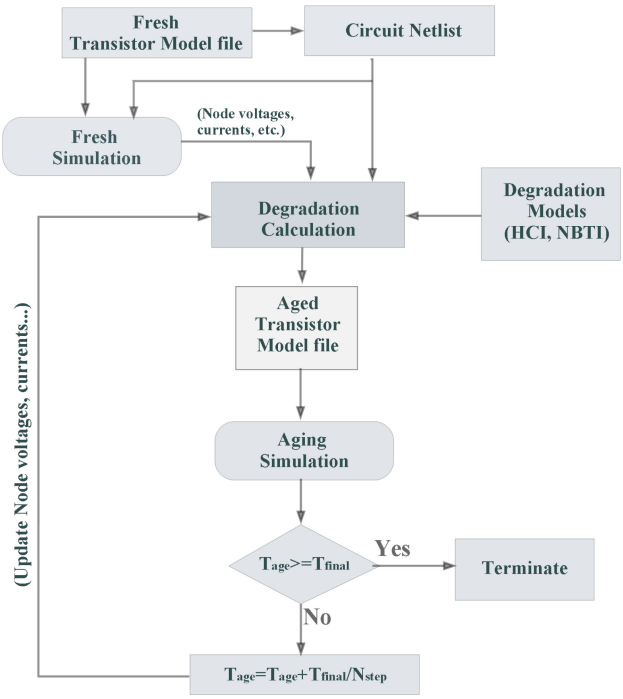

Fig. 3. Simulation flow of the deterministic aging simulator, which considers both HCI and BTI effects and estimates the values of signatures and features.

2006). The other mechanism lead to BTI are hole trapping in process-related SiO_2 bulk traps and generation of new SiO_2 bulk traps (Mahapatra 2016). The dominant consequence of NBTI on PMOS transistor is the increase in the threshold voltage, which is modeled as given in Equation (2):

$$\Delta V_{th} = B.(V_{gs})^{m_1}.e^{\frac{-E_a}{kT}}.L^{m_2}.W^{m_3}.t^{m_4}, \tag{2}$$

where, B, b_1, m_2, and m_3 are technology dependent fitting parameters, k is the Boltzmann constant, T is temperature, t is time, and m_4 is the range of 0.19–0.25 depending on the hydrogen passivation process during fabrication. In contrast to HCI, Negative Bias Temperature Instability (NBTI) occurs dominantly in p-type devices. However, due to increasing usage of high-κ devices, in which charge trapping is more severe compared to conventional SiO_2, PBTI may become significant in n-type devices especially for CMOS technologies beyond 45nm (Zafar et al. 2005, 2006).

2.3 Aging Simulation Tool

Aging analysis provides a projection of lifetime of circuits; thus, changes in circuit performance and aging signatures can be observed. The aging simulator proposed in Afacan et al. (2015) was implemented in this study. The simulator can processes both NBTI and HCI effects; however, only NBTI in p-type devices is considered during aging analysis, since it is reported that no appreciable HCI effect on n-type devices for 130nm technology was observed (Afacan et al. 2016b). The flow chart and the main algorithm of the utilized simulator are provided in Figure 3 and Algorithm 1, respectively. Initially, a fresh simulation is performed by using a fresh transistor model file and electrical specifications including node voltages and branch currents are measured. Degradation amount of each device is calculated by using the semi-empirical model and technology parameters given in Equation (3) and Table 1. The model is a modified version of Equation (2), whose

Table 1. Technology-dependent Coefficents of NBTI Model

B	$m1$	$m2$	$m3$	$m4$	$m5$	$m6$
3.6457	2.175	$6.964e-7$	-4.872	0.0026	0.04318	0.25

parameters were determined via measurements performed on silicon. More details can be found in Afacan et al. (2016c). As the next step, the transistor model file is successively updated by using the calculated degradation parameters:

$$\Delta V_{th} = B.(\mid V_{gs} \mid)^{m_1}.e^{\frac{-E_a}{kT}}.(m_2 L^{m_3} + m_4).W^{m_5}.t^{m_6}. \tag{3}$$

ALGORITHM 1: Aging Simulation

Input: t_{final}, N_{step};
$\Delta t = 0$, $\Delta V_{th_{1,2,\ldots m}} = 0$, $k = 1$;
$(S(1,:), F(1,:)) \Leftarrow simulation_{fresh}()$;
while $t_{step} < t_{final}$ **do**
  k++;
  $\Delta t = \Delta t + t_{final}/N_{step}$;
  $\Delta V_{th1,2,\ldots,m}$ = Degradation$(S_{k-1,p}, t_{step})$;
  (ModelCards) $\Leftarrow$ Update$(\Delta V_{th1,2,\ldots,m})$;
  $(S(k,:), F(k,:)) \Leftarrow$ simulation$_{\text{age}}()$;
end
return S, F

Then, an aging simulation is performed and circuit performance degradations are obtained. Since the stress on each device changes over time, the total simulation time is divided into sub-periods by a certain step number (N_{step}) and consecutive simulations are performed until the final simulation time is reached. Thus, changes in the stress amount on devices are captured periodically, and are taken into account during the calculation of parameter shifts for the next step. The value of step number affects the accuracy of the analysis; however, one should consider that a large step number would cause excessively long simulation time. Heuristically, 100–200 would be sufficient for a quite accurate estimation. At the end of the simulation, the aging simulator returns all signatures' (S) and features' (F) values.

3 RECONFIGURABLE ANALOG CIRCUIT DESIGN AUTOMATION: SENSE AND REACT

S&R is the well-known reconfigurable circuit design approach. In the "Sense" operation, any change in circuit output is detected by a sensor circuit. The type of sensor circuit depends on the application type and the function of the circuit. Conventionally, node voltages, branch currents, and phase/frequency are considered as major measurable quantities for an electrical system. The sense operation is followed by the "Evaluation" operation, where the degradation information is evaluated and enable signals for recovery operations are generated. The last operation is called "React," in which pre-determined recovery scenarios are applied considering the data received from the evaluation block. The whole S&R system (sense, evaluation, and recovery) is initially dormant and only activated when a master enable signal is received. Hence, recovery operation can be managed via the cloud network by a remote user or service.

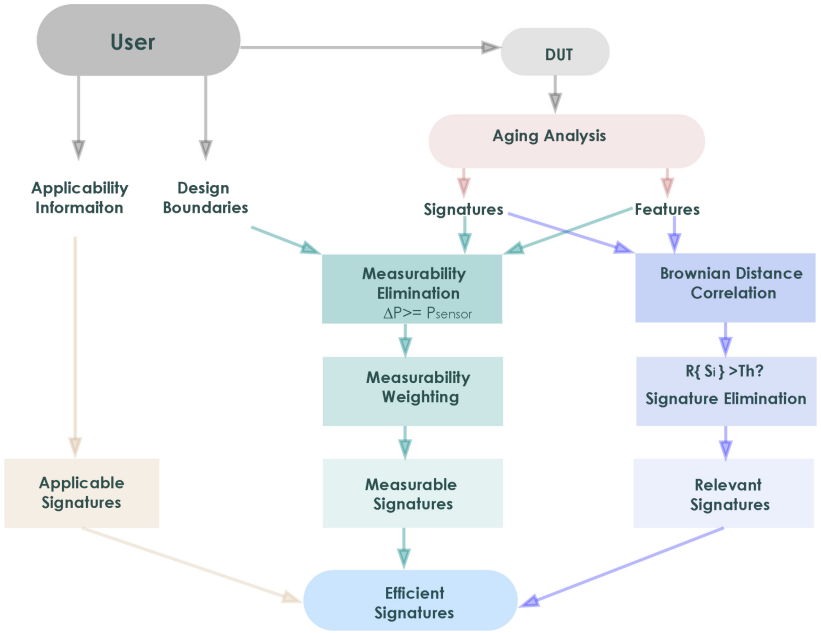

Fig. 4. Flow chart of the signature selection tool, where measurability, relevance, and applicability of candidate signatures are considered to determine the most efficient signature(s).

3.1 Sense Operation: Signature Selection

Aging leads to degradation (increase) in the threshold voltage of transistors causing a decrease in saturation current, which ultimately results in circuit performance deterioration. Since direct measurement of degradation on circuit performances is not practical, indirect measurements are carried out in the sense block, where electrical quantities, such as node voltages, currents, and phase/frequency of a signal are measured, and changes in these quantities are detected. It is important to note that a sampling circuit is required to sense the change in the current while voltage and phase/frequency quantities can be directly detected. In general, current mirrors are utilized to sample the current. However, design of current sampling circuits is highly critical, since aging of the mirroring transistor itself may cause inaccurate sampling, which may disrupt the whole recovery mechanism.

Since indirect measurements are carried out during the sense operation, one or more signatures are required to detect degradation. To minimize the measurement cost, the number of efficient signatures should be kept minimum. However, efficient signature selection is a complex problem. An efficient signature should have certain attributes, such as Relevance ($\mathcal{R}$), Measurability ($\mathcal{M}$), and Applicability ($\mathcal{A}$). Considering efficient signature properties, a signature selection procedure is introduced as provided in Figure 4.

- **Relevance Analysis:** The signature behavior should be relevant to the behavior of the degraded performance feature so that the signature changes can be mapped into the performance degradation. In the relevance analysis part, a modified alternate test-based approach proposed in Barragan and Leger (2015) is used, where a large number of instances of DUT are generated through Monte Carlo simulations to obtain changes in signatures and specifications. Then, a correlation algorithm is applied to determine the relevant signature set for the testing process. In contrast to Barragan and Leger (2015), no extra Monte Carlo analysis

is required for S&R systems, because the developed aging simulator divides the lifetime analysis into sub-periods by a certain step number, so instances of training set for signature selection process are automatically generated. The only modification is the simulation part of the simulator is the measurement of candidate signatures. A conventional approach to measure the dependence between two random variables is based on the Pearson's product-moment correlation (ρ) and co-variance. Pearson's correlation uses a first-order distance formula to calculate dependency of two random variables, so it is valid only for linear or monotonic conditions. As a result, Pearson's correlation does not provide a comprehensive solution for a wide range of applications. To overcome this problem, Brownian distance correlation ($\mathcal{R}$) proposed in Székely et al. (2009) is commonly used to correlate signatures and specifications in the testing area (Barragan and Leger 2015). Since this approach utilizes a second-order product-moment correlation, non-linear behavior on the signatures can be successfully captured through finite second-order moments (Barragan and Leger 2013).

Considering the signature set (S) (node1, node2, etc.) and the feature (gain, bw, etc.) set (F), $(S, F) = \{(S_i, F_i)_{i=1,2,\ldots n}\}$, the euclidian distance matrices for vectors $S \in \mathfrak{R}^p$ and $F \in \mathfrak{R}^q$ are computed as

$$\begin{aligned}(x_{ij}) &= (|S_i - S_j|_p),\\ (y_{ij}) &= (|F_i - F_j|_q).\end{aligned} \tag{4}$$

Defining $X_{ij} = \bar{x}_{ij} x_{i\cdot} - \bar{x}_{\cdot j} + \bar{x}_{\cdot\cdot} \quad i, j = 1, 2, \ldots, n$, where

$$\bar{x}_{i\cdot} = \frac{1}{n}\sum_{j=1}^{n} x_{ij}, \quad \bar{x}_{\cdot j} = \frac{1}{n}\sum_{i=1}^{n} x_{ij}, \quad \bar{x}_{\cdot\cdot} = \frac{1}{n^2}\sum_{i,j=1}^{n} x_{ij}. \tag{5}$$

Similarly, defining $Y_{ij} = y_{ij} - \bar{y}_{i\cdot} - (\bar{y}_{\cdot j}) + \bar{y}_{\cdot\cdot} \quad i, j = 1, 2, \ldots, n$. The distance covariance $\mathcal{V}_n(S, F)$ and the sample correlation $\mathcal{R}(S, F)$ are calculated as

$$\mathcal{V}_n^2(S, F) = \frac{1}{n^2}\sum_{i,j=1}^{n} X_{ij} Y_{ij} \tag{6}$$

and

$$\mathcal{R}(S, F) = \begin{cases} \frac{\mathcal{V}_n^2(S,F)}{\mathcal{V}_n^2(S)\mathcal{V}_n^2(F)}, & \mathcal{V}_n^2(S)\mathcal{V}_n^2(F) > 0,\\ 0, & \mathcal{V}_n^2(S)\mathcal{V}_n^2(F) = 0, \end{cases} \tag{7}$$

respectively. Consequently, the distance correlation $\mathcal{R}(S, F)$ between candidate signatures S_i and circuit features F_i can be used as a figure of merit for relevant signature selection.

To filter out irrelevant signatures, an elimination is performed after the relevance analysis according to

$$I_{R_i} = \begin{cases} 1, & \mathcal{R}(S_i, F_i) \geq \overline{\mathcal{R}(S_i, F_i)},\\ 0, & \mathcal{R}(S_i, F_i) < \overline{\mathcal{R}(S_i, F_i)}, \end{cases} \tag{8}$$

where $i = 1, 2 \ldots, n$. I_{R_i} denotes the indicator function that indicates the signature is relevant ($I_{R_i} = 1$) or irrelevant ($I_{R_i} = 0$). The threshold value for the signature elimination is the average value ($\overline{\mathcal{R}(S_i, F_i)}$) of the signature set.

- **Measurability Analysis:** Aging-induced changes in the relevant signatures should be within the limits of the input sensitivity of the sensor circuit (mostly a comparator); otherwise, the sensor circuit cannot detect them, resulting in sense operation malfunction. Defining the change in the signature ΔS_i and minimum sensitivity of the sensor P_{sensor},

which is determined by the user, the measurability of a signature can be defined as

$$I_{P_i} = \begin{cases} 1, & \Delta S_i \geq P_{sensor}, \\ 0, & \Delta S_i < P_{sensor}, \end{cases} \tag{9}$$

where $i = 1, 2 \ldots, n$. I_{P_i} denotes the indicator function that indicates the change in the signature is measurable ($I_{P_i} = 1$) or not ($I_{P_i} = 0$). After the elimination, a total weight budget of W_{total} are allocated among the measurable signatures ($i = 1, 2 \ldots, k$) according to

$$W_i = \frac{\Delta S_i}{\sum_{i=1}^{k} \Delta S_i} W_{total}. \tag{10}$$

This weighting process provides ranking of the candidate signatures with respect to the change amounts, where signatures having larger changes are preferable to minimize the sense operation error.

- **Applicability Analysis:** Loading effects of sensor circuit may deteriorate circuit performance during degradation monitoring, (i.e., input capacitance of the sensor may damage the frequency performance). Therefore, applicability should also be considered to maintain circuit operation during the measurement mode. Furthermore, accessibility of signatures may also be included within applicability, which may cause improper layout of the design. Contrary to measurability and relevance analyses, applicability information requires an expert knowledge on the circuit topology. Therefore, the applicability information is initially required by the user and taken into account at the final determination step in the developed tool. There are three different scores defined for the applicability information of signatures: *low* (0.1), *moderate* (0.5), and *high* (1). This procedure may be automated by modeling sensor-induced loading effects and performing simulations for each signatures including these loading effects.

Finally, accounting all these properties, the efficiency ($\mathcal{E}$) of a signature is calculated as

$$\mathcal{E}_i = \mathcal{R}_i \mathcal{M}_i \mathcal{A}_i \mathcal{R}\mathcal{R}_i, \quad i = 1, 2, \ldots, n. \tag{11}$$

To demonstrate the signature selection approach, a folded cascode OTA circuit given in Figure 5 was designed using 130nm technology, for which gain, 3dB bandwidth, and the phase margin were selected as design features. Node voltages not including power (1,17), input (15,16), and bias (7,8) nodes were taken as 11 aging signatures. According to the fresh simulation results, the circuit has 68.3dB gain, 19.7kHz bandwidth, and 64.3° phase margin. The time for aging simulation was decided to be 10 years, where the step count was selected as 500. Design boundaries for sense operation were selected as 65dB, 17kHz, and 60°, respectively. In the case of violation in any circuit specification, changes in the signatures are calculated for measurability analysis. The input sensitivity of the aging sensor, which is typically a voltage comparator, was fixed to 500μV. The total weight for the measurability was selected as 100. In Figure 6, aging simulation results are given for the folded cascode circuit. As can be seen from the simulation results, the bandwidth of the amplifier substantially decreases over time, while there is no considerable degradation in the gain and the phase margin of the amplifier. Therefore, the sense strategy was designed to detect the degradation in the bandwidth. It should be noted that in the case of degradation of more than one performance metrics, all of them are taken into account during the signature determination process and the average of the relevance scores evaluated. Signature selection results are given in Table 2.

Correlation results indicate that almost all candidate signatures have a strong correlation with the bandwidth behavior. However, more than half of these candidates were eliminated by the measurability elimination, since the variation amounts for these candidates at the critical point

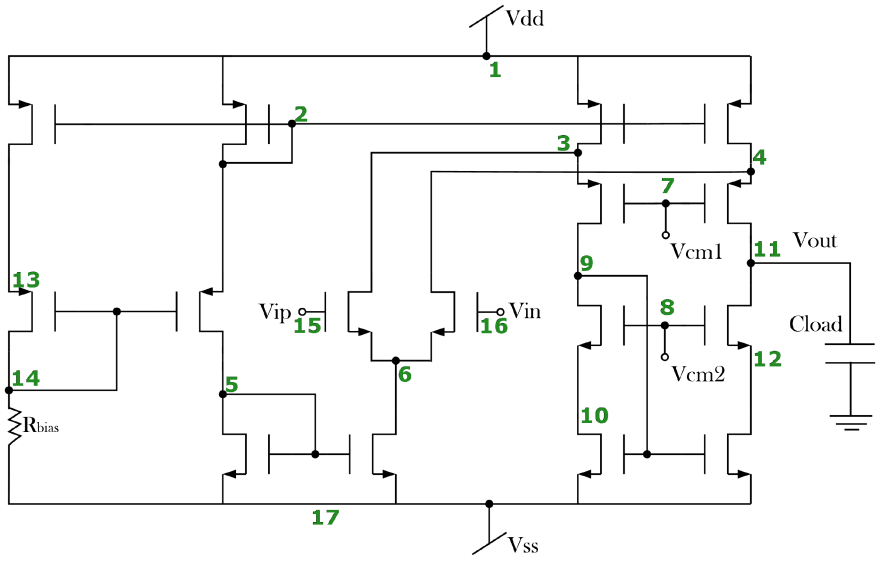

Fig. 5. Schematic of folded cascode OTA with cascode current source.

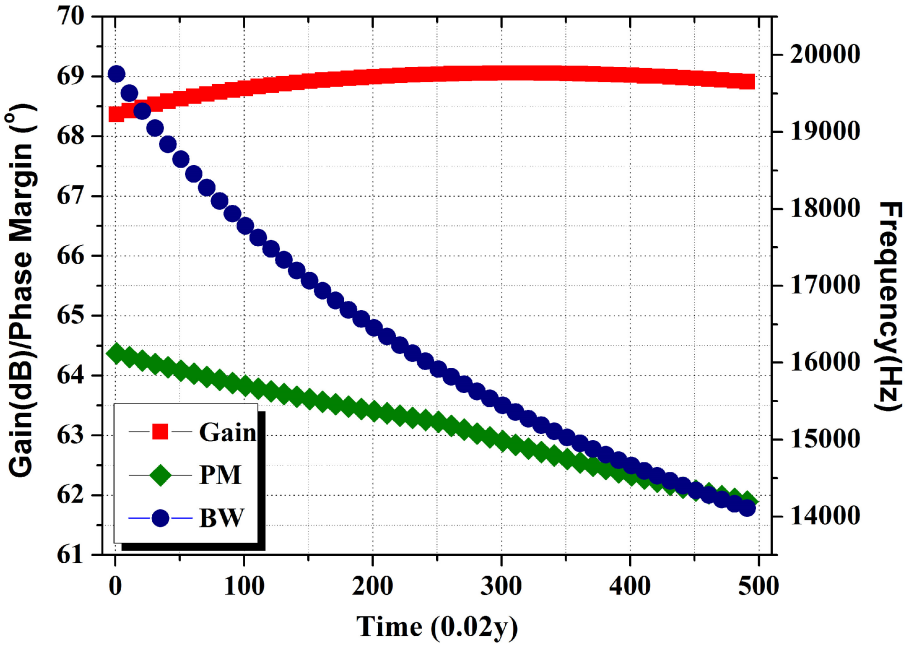

Fig. 6. Aging simulation results of the folded cascode OTA, whose 3dB bandwidth is the most sensitive specification and degrades drastically over time.

are lower than the input sensitivity of the sensor. After the measurability weighting, signatures 3, 4, and 14 are the prominent candidates out of the standing 5 signatures. At the third row, user-defined applicability scores are provided. Since the signal on nodes 3, 4, and 11 may be affected due to loading effects during the sense operation, low applicability scores were assigned to these signatures. Finally, the efficiency scores are presented at the fourth row, where the efficient signature

Table 2. Signature Selection Results for the Folded Cascode Amplifier

Candidate Signatures (Node Voltages)	**2**	**3**	**4**	**5**	**6**	**9**	**10**	**11**	**12**	**13**	**14**
Relevance Score	99.5	99.9	99.8	99.2	99.3	99.2	77.3	97.5	99.2	99.4	99.5
Measurability Score	9.58	33.1	31.18	0	0	0	0	0	0	9.59	16.53
Applicability Score	1	0.1	0.1	1	0.5	0.5	0.5	0.1	0.5	1	1
Efficiency	953	330	311	0	0	0	0	0	0	953	**1644**
Efficiency (after MC)	978	310	309	0	0	0	0	0	0	1033	**1713**

for sense operation was found to be node 14. A further problem may arise due to the process variations, where varying transistor parameters may change the signature attribute resulting in wrong selection of the efficient signature. To discover the effect of variability, a Quasi-Monte Carlo analysis with 500 samples was performed for the DUT and signature selection procedure was repeated for each solution set. According to the variability-aware efficiency results given in the last row, there is no considerable change in any signature feature; thus, the total efficiency that is calculated as given in Equation (11) would not be affected by variability problem.

3.2 Recovery Operation: Recovery Determination

Typically, there are three different recovery operations for the react part, which are; adaptive biasing, additional supplementary transistors/blocks, and exchange of aged transistors/blocks by fresh ones.

In the "Adaptive Biasing" approach, the activation data generated by the evaluation is converted to some pre-determined voltages and applied to the critical nodes to compensate for the increase in the threshold voltage (Tschanz et al. 2007). Thus, more current can be supplied by the aged transistors. However, this approach is quite difficult and expensive, since both evaluation and conversion of the circuit output changes to bias voltages are highly challenging problems. A further problem arises due to the nature of aging for adaptive biasing approach, where the stress on the device is increased during recovery of the degradation in the current, which may accelerate the aging process for long-term operations.

In the second approach, a limited number of supplementary devices in the chip, which are passive at the beginning, are activated to compensate the degradation effects. This approach is highly advantageous for rapidly aging circuits; thus, even small degradations can be detected and quickly recovered within short time periods by circuits designed with a high of sensitivity to the change of the output parameters (Maricau and Gielen 2011). However, adding extra devices may cause sizable performance deterioration certain applications such as increased device noise in RF circuits.

In the last approach, rather than adding supplementary devices, aged transistors/blocks are completely replaced by fresh ones; thus, a full recovery is achieve (Afacan et al. 2014). This approach does not suffer from any performance degradation. However, in general, the exchange operation can only be performed for one time due prohibitive area occupation of multiple fresh devices on the chip. The type of recovery operation varies for different applications, so each circuit/system requires a specific evaluation and recovery part. Aging analysis also has a critical role, which it generates the amount of degradation information for each individual transistor; thus, the designer has the knowledge of the most critical devices for a given circuit. Then, an expert designer decides an efficient recovery strategy within a number of iterations. However, this process may be very time consuming due to expensive aging simulations and repetitive recovery trials.

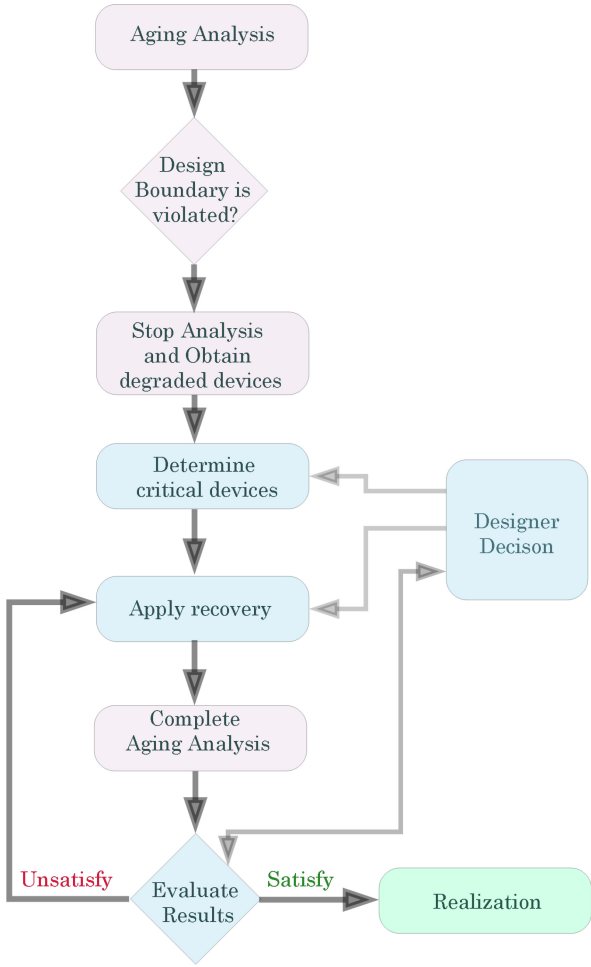

Fig. 7. The flow chart of the recovery operation determination approach, in which possible recovery operations are applied consecutively and the most efficient operation is determined.

To deal with this inefficiency problem, a recovery determination procedure, whose flowchart given in Figure 7, is developed. The proposed approach facilitates computer-aided design (CAD) during the evaluation of recovery operation, which is performed at the netlist domain according to the instructions given by an expert designer. Hence, the designer takes the role from the CAD tool for the recovery decision, because, an expert designer can find an efficient solution within a few number of iterations rather than a blind iterative search. At first, aging analysis is performed for the DUT. During aging analysis, circuit features are continuously monitored and the analysis is stopped when a boundary violation occurs. Meanwhile, all circuit features, signatures, and degraded device information are recorded. Here, the designer interferes in the flow to determine the critical devices among the degraded ones and the type of recovery operation. After the completion of recovery operation, a verification simulation is carried out to test the recovery operation. Then, the designer evaluates final results and the flow is ended if the recovery operation is satisfied. In the case of any unsatisfactory operation, the designer replaces the recovery operation by a new one and the procedure is repeated.

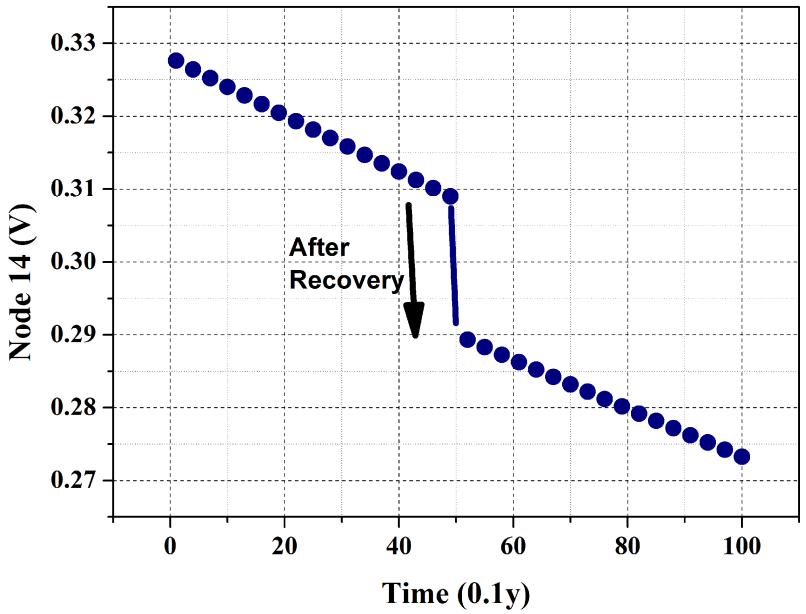

Fig. 8. Signature node 14 is not a reversible signature.

An S&R system should be capable of handling both degradation sensing and healing processes without any interaction. The proposed signature selection procedure is based on detection of degradation and does not take healing into account. However, the healing information is needed to determine whether the recovery operation is satisfied or not. Otherwise, another signature should be selected to ensure the recovery operation and deactivate the S&R system. To illustrate this problem, the behavior of the most efficient signature (node 14) determined in Table 2 after a proper recovery operation is provided in Figure 8.

As seen from the figure, aging signature continues to decrease despite the recovery operation, which means that this signature is not reversible. However, the signature (node 5) shown in Figure 9 is reversible, so it would be more appropriate to use it as the signature for the system. As a result, an efficient signature should have another important property that is called "Reversibility ($\mathcal{RR}$)." To overcome this problem, an additional signature selection should be applied just after the recovery operation to re-evaluate candidate signatures and determine the most efficient signature considering the reversibility property.

The second signature selection results are given in Table 3. Results indicate that the former aging signature loses its relevance after the recovery operation, where node 5 is determined as the most efficient signature. It is important to note that the measurability threshold is reduced to 100μV in this second analysis for the sake of measurement cost. Otherwise, a second sensor would have been needed to determine the success of the recovery operation. Moreover, one should consider that the Brownian distance correlation uses a second-order product-moment correlation and does not consider the direction change in the signature, which may lead to misinterpretation during relevance analysis. To overcome this problem, the proposed tool uses an additional Pearson correlation algorithm during the relevance analysis to capture the direction change in the candidate signatures. In the case of no signature satisfying all the features, the system design would be more complex due to need of different sense circuits for each operation; however, it would not damage the applicability of the proposed approaches. The comparator circuit can be sequentially used

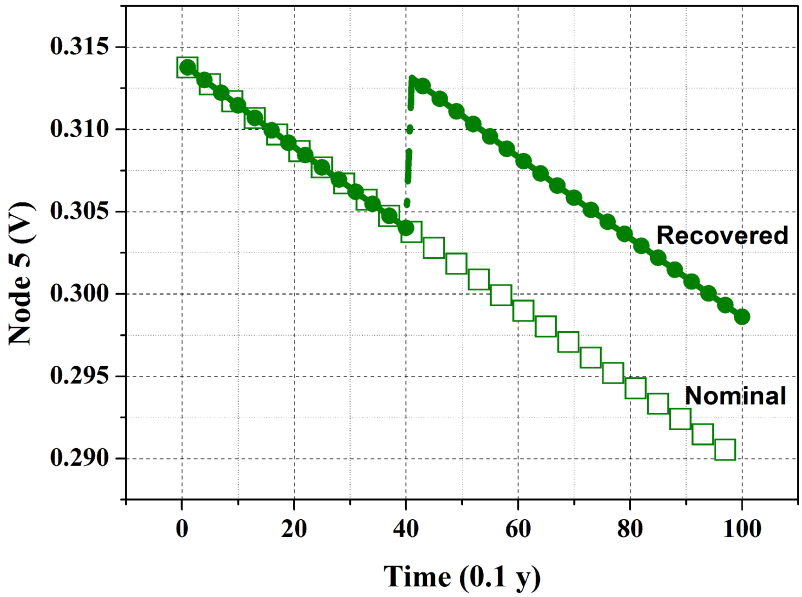

Fig. 9. Signature node 5 satisfies reversibility as well as relevance, measurability, and applicability.

Table 3. Recovery-aware Signature Selection Results

Candidate Signatures (Node Voltages)	2	3	4	5	6	9	10	11	12	13	14
Relevance Score	0	94.3	94.3	97.6	79.3	97.2	77.3	98.1	98.2	0	0
Measurability Score	7.38	28.1	28.02	6.8	5.6	3.3	0	3.1	0	7.39	10.31
Applicability Score	1	0.1	0.1	1	0.5	0.5	0.5	0.1	0.5	1	1
Efficiency Score	0	208	208	**660**	222	32	0	32	0	0	0

during sensing (one clock cycle for aging and the other one for the recovery sensing), since the evaluation takes just a few microseconds.

4 DESIGN AUTOMATION TOOL FOR S&R SYSTEMS

The design process of an S&R system was fully automated by integrating the signature selection and the recovery determination approaches. The general structure of the developed tool is shown in Figure 10.

The framework of the developed tool was implemented on MATLAB. HSPICE/RF is utilized during electrical simulations. Design boundaries are determined by the user considering the circuit specifications. In the case of violation in any circuit specification, the aging analysis is stopped and an ad-hoc recovery operation is applied. There are three default options for the recovery; adaptive biasing, reinforcing the degraded devices, and exchange of them. After the recovery operation, the aging analysis is completed, in meanwhile, signature selection process is performed. The idea behind the recovery determination is to minimize the cost of healing circuit. Namely, the tool initially prefers to recover the circuit with adaptive biasing, which is the most cost-effective option. If it does not work, then it performs reinforcing degraded transistor(s). If the circuit is still not recovered, then the tool exchanges the degraded transistors one by one. Furthermore, the

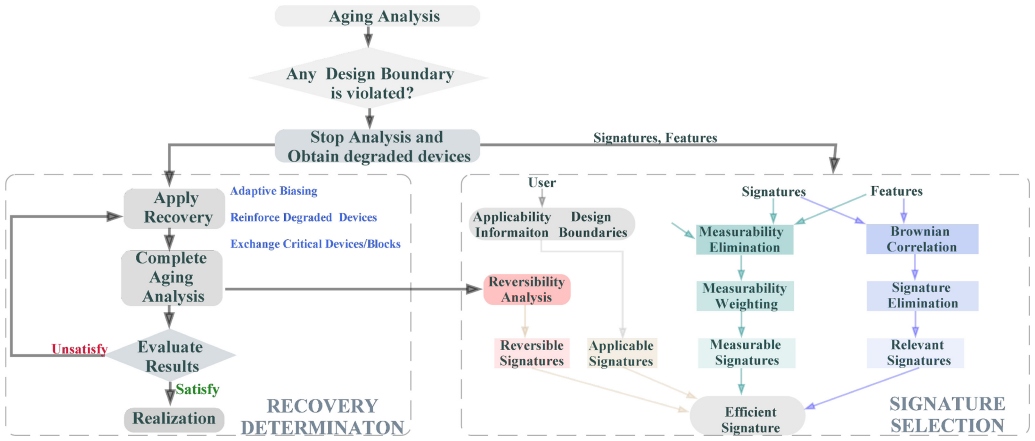

Fig. 10. The general structure of DATSRS, which consists of two different layers: signature selection and recovery determination. These two layers communicates to each other during the reversibility analysis.

developed tool is also capable of applying the possible combinations of these recovery operations when individual trials are not satisfactory. Finally, the tool generates a report that includes the aging simulation results (with/without recovery), the new expected lifetime, efficient signature(s), and the proposed recovery scenario.

5 IMPLEMENTATION EXAMPLES

Operational amplifiers are usually the major blocks in many analog circuits. Therefore, two different sense and react systems were designed and simulated for two different OTA circuits (folded cascode and two-stage OTAs). The DUTs were designed using a commercial 130nm technology. Node voltages were preferred as aging signatures to observe the aging and recovery information from the DUT devices for all systems developed. Therefore, a voltage comparator was utilized as aging sensor.

Conventionally, S&R systems can be designed *Discrete* or *Continuous*. In the discrete mode, S&R system is controlled by an external enable signal; thus, there is no additional power consumption for this approach, since the peripheral devices are nominally dormant and only active for a short period. On the contrary to that, in the continuous approach, peripheral devices always operate concurrently with the actual circuit; thus, they can sense and recover degradations at any time. This approach may not be suitable for modern applications due to increased power consumption. Nevertheless, certain critical applications may require such a system to protect the circuit performance from any type of degradation.

5.1 Case Study I: Folded Cascode Operational Transconductance Amplifier

A comprehensive circuit level schematic of the developed S&R system for the folded cascode OTA is given in Figure 11. The amplifier was designed using 130nm technology, where a single 1.2V power supply was used. By utilizing the developed recovery determination tool, adaptive biasing was determined as the most efficient recovery operation. Reinforcing and the replacement of aged devices by new ones were the other possible solutions, where the adaptive biasing is preferred due to its low cost and ease of use. The idea behind the approach is based on the deactivation of the required number of resistors in the bias resistor block, where the total resistance is divided into small and different valued resistances that are controlled by switches. In that way, NBTI-induced current degradation due to increased threshold voltages of p-type devices can be compensated.

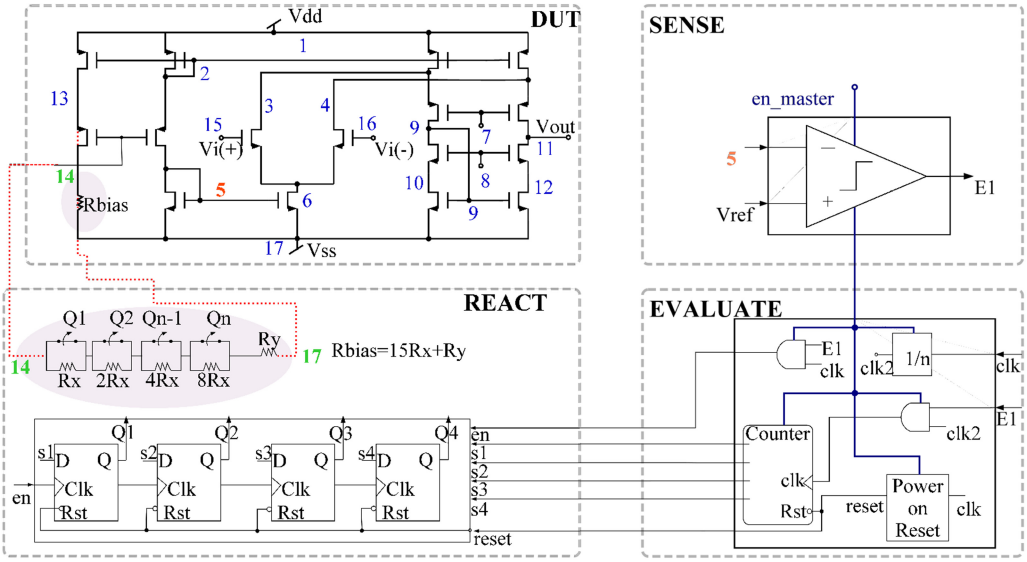

Fig. 11. Circuit level schematic of the developed S&R system for folded cascode OTA, in which adaptive biasing was determined as the most efficient recovery operation.

According to aging signature selection results (recovery considered), node 5 (n_3) was found as the most efficient aging signature. In the sense operation part, this node voltage is compared with a pre-determined reference voltage (V_{ref}). To eliminate the PVT effects, the reference voltage can be determined by performing a single measurement of signature at the beginning. In the evaluation block, a 4 bit binary synchronous counter is utilized to manage the recovery operation. A power on reset circuit is utilized to reset all states when the system is activated. To guarantee the success of the recovery operation, one should consider that the evaluation block operates slower than the react block. For that purpose, a clock divider is utilized to generate a slower clock signal for the counter. The counter drives a flip-flop chain located at the react part, which is triggered by the enable signal (*en*). In the react part, the bias resistor is divided to five resistors; one of them (R_y) is directly connected to the circuit, whereas the other four resistors are valued considering aging and recovery simulation results and controlled by normally on state switches that are driven by the flip-flop outputs ($Q_{1..4}$). The system begins to work when an enable signal is received. Once the aging signature (n_3) becomes lower than the reference signal, the comparator output becomes logic 1 and the evaluation block generates enable signals for the react operation. Meanwhile, the counter starts to count and the first resistor is deactivated. This cycle continues until the comparator generates logic 0, which means that self-healing is satisfied. When the counter stops to count, all enable signals are pushed down to logic 0, and the flip-flop chain saves the last states at the output until a new aging signal is produced by the aging comparator. Here, comparators and logic circuits in the evaluation block are supplied by a different power signal, which is controlled by the user, whereas the flip-flop chain is supplied by the main power signal to maintain the last state.

A simulation output is provided in Figure 12. To simulate the whole system, a degraded model file obtained through the aging simulation was used during simulations. During aging simulations 130nm technology parameters were used. The step size was determined as 500. According to aging simulations, the most sensitive circuit output was determined to be the bandwidth of the OTA, which decreased from 19.8kHz to 16.5kHz due to aging. Conversely, changes in the gain and phase margin are negligible compared to the bandwidth. The nominal value of the aging signature (n_3)

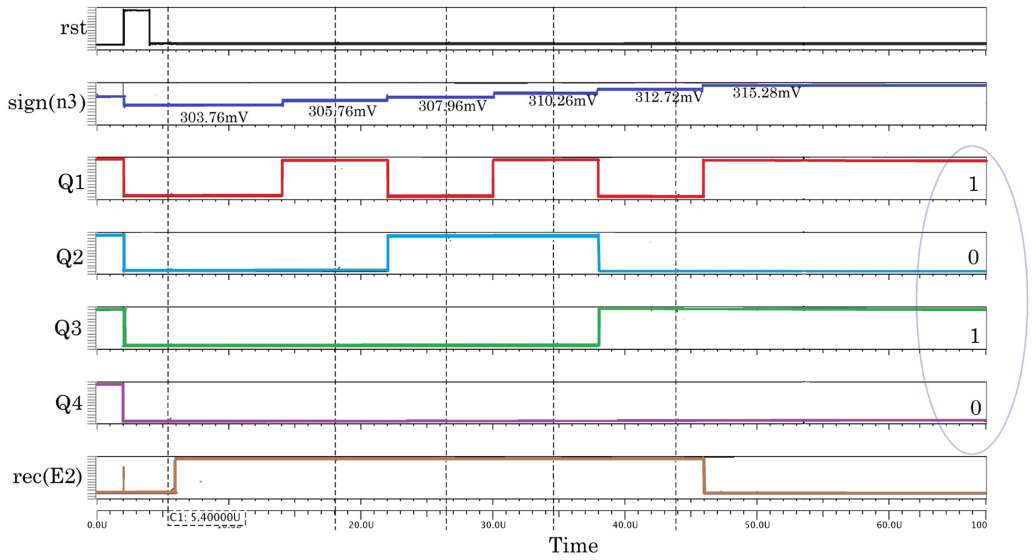

Fig. 12. Simulation output of the developed S&R system for folded cascode OTA.

was 315mV, which was measured to be 303mV after aging. When the system is activated, a master reset signal (*rst*) is generated for a short time period to initialize the all flip-flops, after which the system starts to work. As seen from the simulation results, the counter counted up to 5− > "0101," so a resistor of $5R_x$ was removed from the bias part. The aging signature becomes closer to the initial value (315mV) after the recovery, the aging signal (E_1) becomes logic 0, and the healing system ceases operation. Circuit specifications after the recovery operation are provided in Figure 13.

According to these results, there is no considerable change in gain and phase margin responses, whereas the bandwidth of the amplifier was successfully recovered. Furthermore, it is important to note that the proposed system is suitable for multiple recovery operations; thus, possible further degradations can also be recovered. Whenever a degradation is observed, the recovery part is initialized by the master reset signal, and the recovery part is reconfigured to compensate for the cumulative degradation. The proposed system was compared with a nominal design and an overly designed circuit, which have similar FOMs and the results are provided in Table 4. As expected, the results of the proposed system increases the lifetime of the circuit with a small increase in power consumption, which is due to the enabled switches after recovery operation. Furthermore, increase in the area overhead is negligible compared to the overly designed circuit.

5.2 Case Study II: Two-stage Operational Transconductance Amplifier

The proposed S&R system schematic for the two-stage OTA is given in Figure 14. The amplifier was designed using 130nm technology, where a single 1.2V power supply was used.

Contrary to the folded cascode OTA, the input differential pair of this circuit comprises p-type transistors, whose transconductance degrade over time. Considering recovery operation determination results, the recovery scenario for this circuit is based on the activation of the required number of substitute transistors; thus, the differential pair transistors are reinforced and current degradation is compensated. Sense and evaluation blocks are the same as in the folded cascode example. However, in contrast to the folded cascode example, a transistor chain with different sizes was placed at the recovery part, which are controlled by switches driven by the flip-flop outputs (Q_{1-4}). When an enable signal is received, peripheral devices are powered on and the system starts

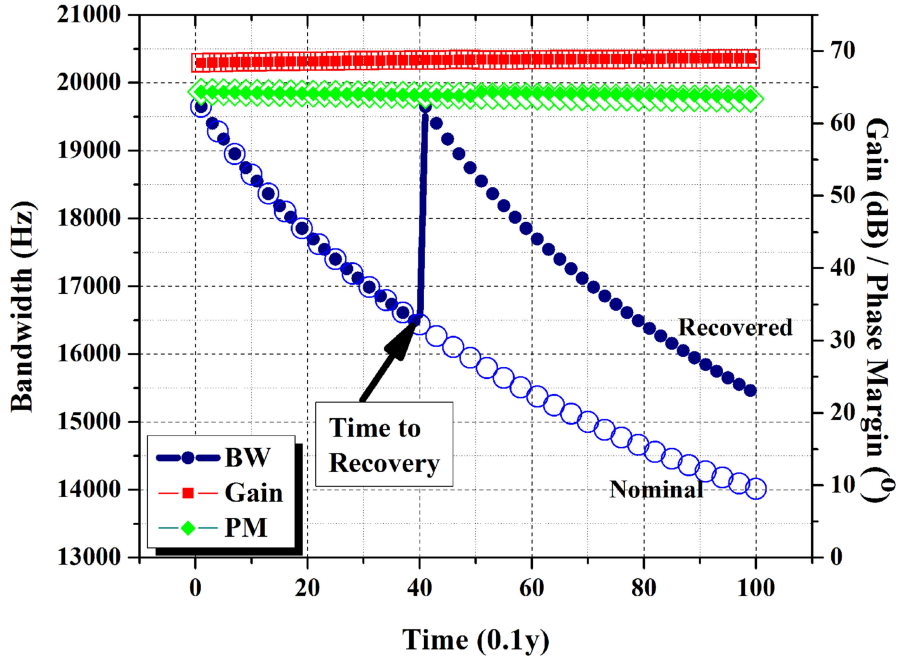

Fig. 13. Circuit specifications after recovery operation, where the lifetime of the circuit almost doubled.

Table 4. Comparison of the Proposed System with Nominal and Over-designs

	Power Cons. (mW)	Chip Area (μm^2)	Lifetime (years)
Nominal	0.5	1,200	4
Overdesign	1.3	2,800	6
Sense and React	0.5	1,500	9

to work. In any case of degradation, the aging signature (n_2) becomes lower than the reference signal, the comparator output becomes logic 1, and the evaluation block generates enable signals for the react operation. Substitute transistors are activated consecutively until the sense block determines that the circuit performance is recovered, where the comparator output becomes 0. The counter stops counting and the flip-flop chain saves the last state at the output until a new degradation is observed. Similarly, comparators and logic circuits in the evaluation block are supplied by a different power signal, which is controlled by an external enable signal, whereas the flip-flop chain is powered by the main power signal to maintain the last state.

To demonstrate the proposed sense and react system, simulation results for the two-stage OTA are given in Figure 15. A degraded transistor model file obtained through aging simulations was included in the design during simulations, where the nominal and the aged values of bandwidth are 9.9kHz and 6.8kHz. Changes in the gain and the phase margin are both negligible.

According to the simulation results, the counter counted up to 6 to recover the circuit, where only the second and the third substitute transistors were activated. The aging signature ($n2$) increased from 263 to 275mV, whose fresh value was around 275mV. The behavior of circuit performances after the recovery operation is provided in Figure 16. The bandwidth of the OTA increased to 8.9kHz, which is very close its nominal value (8.8kHz). Comparison results are provided in Table 5, where all solutions have similar FOM in each approach. As expected, lifetime of the

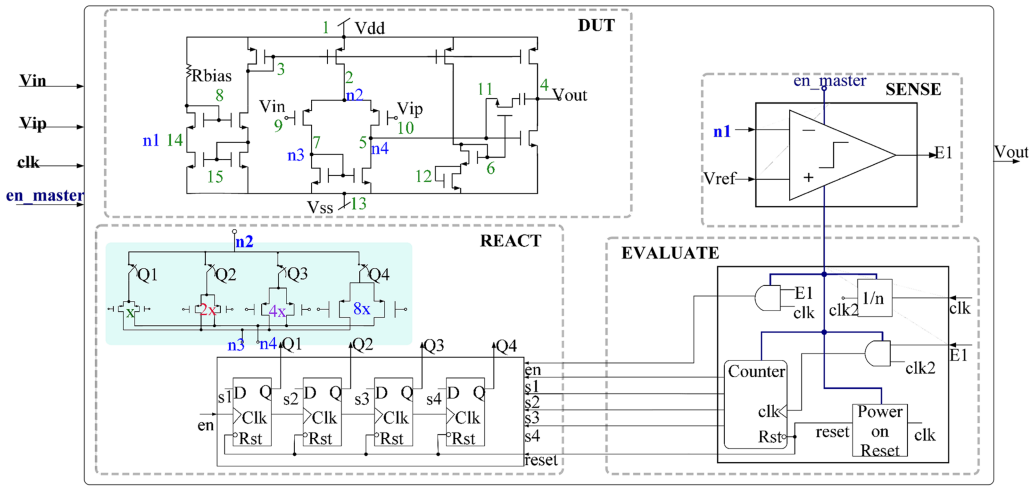

Fig. 14. Circuit level schematic of S&R system for two-stage OTA, where reinforcing was determined as the most efficient recovery operation.

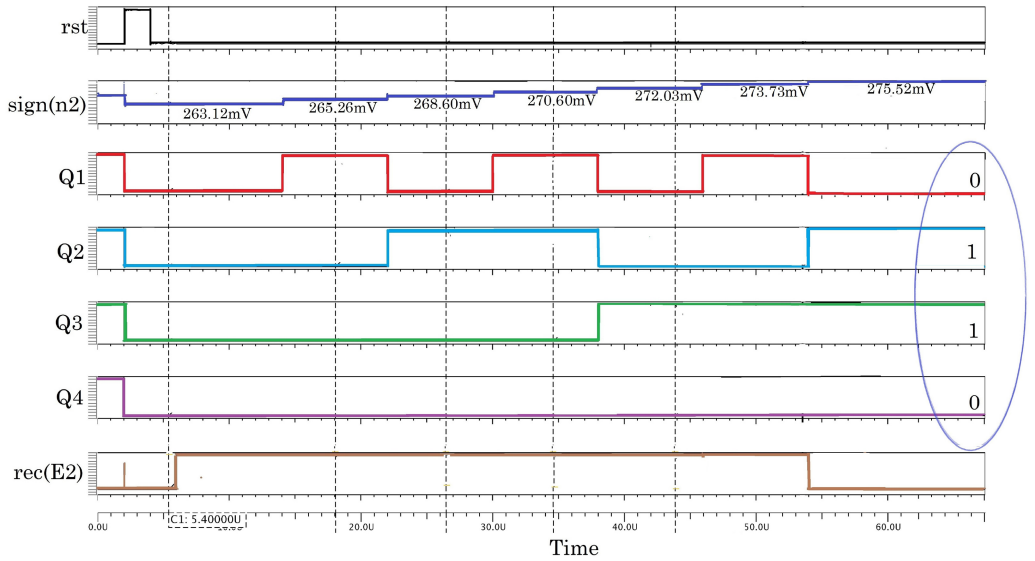

Fig. 15. Simulation results of the developed S&R system for two-stage OTA.

circuit was improved without any additional power consumption in the proposed system while the chip area is considerably smaller compared to the over-design approach.

6 CONCLUSION

Based on the rapid advances in CMOS technology, it has been possible to employ high-performing and low-power analog circuits in smaller chip areas. However, aging has become a threat to such circuits due to increased local electrical stress on devices, which leads to a considerable decrease in lifetime of analog circuits. Overdesign is a popular method to increase the lifetime of ICs, where power consumption is increased for the sake of reliability. However, this approach is not suitable

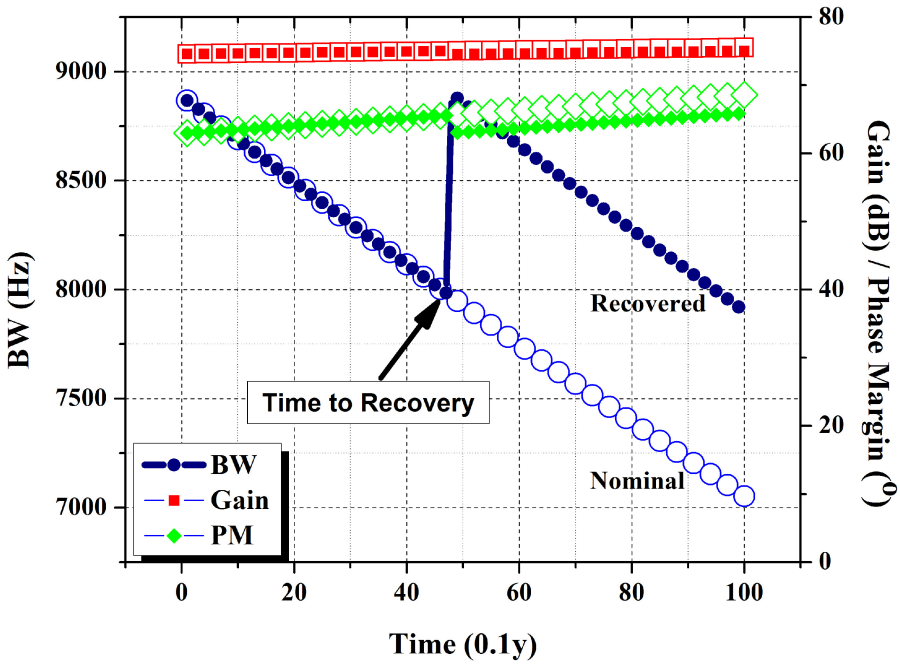

Fig. 16. Circuit behavior after recovery operation. The lifetime of the circuit almost doubles as well as the folded cascode example.

Table 5. Comparison of Self-healing Approach with Nominal and Over-design Results

	Power Cons. (mW)	Chip Area (μm^2)	Lifetime (years)
Nominal	0.6	2,500	4
Overdesign	1.4	3,800	5.5
Sense and React	0.62	2,900	9.5

for modern applications, for which the power consumption is limited energy sources. Considering the trade off between performance, power, and reliability, S&R approaches (re-configurable circuit design) promise the best solution to increase the lifetime of analog circuits. This study provides a comprehensive analysis of the design of S&R systems from degradation sensing to system implementation and proposes novel tools that facilitate the design process. The concept of the most efficient signature has been described and a selection tool has been presented. The developed tool considers only the sense operation during the signature selection process. However, this study demonstrates that the most efficient signature should be determined considering the whole system to avoid severe operating failures. Furthermore, a recovery operation determination approach is introduced to reduce the human effort during this challenging process. By integrating the aging simulator, the signature selection, and the recovery determination approaches, a novel design automation tool for S&R systems was developed; thus, the design process of an S&R system was fully automated. By utilizing the developed tool, two different S&R systems were designed and simulated. The realized systems are suitable for multiple recovery stages; thus, circuits can be healed many times during their lifespans. The proposed systems can also be easily adopted to other circuits with small modifications.

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