LOW POWER CONSUMPTION CONTINUOUS TIME SIGMA-DELTA MODULATOR DESIGN

by

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ABSTRACT

LOW POWER CONSUMPTION CONTINUOUS TIME SIGMA-DELTA MODULATOR DESIGN

Mobile electronic devices have important roles in our daily lives. While they are getting smaller, their functionality is increasing. As the charge capacity of the batteries is limited, it should be spent efficiently. Low power consumption designs respond to high power demand of these multifunctional devices.

Data converters which act as the interface between analog and digital signals are used in most electronic devices. There are many analog to digital converter topologies with respect to the application type used in. Sigma-Delta ADCs are generally preferred for low power consumption and high signal-to-noise ratio.

Type of a Sigma-Delta ADC is determined by the filter/integrator block. Different types of continuous time integrators are presented in system level. Derivation and detailed noise analysis of current-mode differential integrators are demonstrated in this thesis. Feedback analysis is performed and compared with simulations. Simulation results are presented verifying theoretical results. The effect of enhancing DC gain of the integrator on the noise is examined. It is concluded that the positive feedback in the integrator circuit causes high noise levels.

A 2nd order CT current-mode Σ-Δ ADC is designed and manufactured in UMC 130nm technology. Post-layout simulation and measurement results are compared. Observed noise levels on both simulations and tests are high because of the positive feedback effect of current-mode differential integrator used in the filter block.

ÖZET

DÜŞÜK GÜÇ TÜKETİMLİ SÜREKLİ ZAMANLI SİGMA-DELTA MODÜLATÖR TASARIMI

Taşınabilir elektornik cihazların günlük yaşantımızda önemli görevleri vardır. Bu cihazlar gittikçe küçülürken işlevsellikleri artmaktadır. Pillerin yük sığası kısıtlı olduğu için verimli bir şekilde harcanmalıdır. Düşük güç tüketimli tasarımlar bu çok işlevli cihazların yüksek güç talebine cevap vermektedir.

Analog ve sayısal işaretler arasında arayüz görevi gören veri dönüştürücüler birçok elektronik cihazda kullanılmaktadır. Kullanılan uygulama türüne göre çok analog-sayısal dönüştürücü topolojisi vardır. Sigma-Delta analog-sayısal dönüştürücüleri genellikle düşük güç tüketimi ve yüksek işaret gürültü oranı için tercih edilirler.

Bir Sigma-Delta analog-sayısal dönüştürücünün türü süzgeç/integral alıcı blok tarafından belirlenir. Sürekli zamanlı integral alıcıların farklı türleri sistem seviyesinde sunulmuştur. Bu tezde, akım kipli farksal integral alıcıların türetimi ve ayrıntılı gürültü incelemesi gösterilmiştir. Geri bildirim incelemesi yapılmış ve benzetimlerle karşılaştırılmıştır. Sunulan benzetim sonuçları teorik sonuçları doğrulamaktadır. İntegral alıcının doğru akım kazancının arttırılmasının gürültü üzerine etkisi incelenmiştir. İntegral alıcı devredeki pozitif geri bildirimin yüksek gürültü seviyelerine neden olduğu sonucuna varılmıştır.

İkinci derece sürekli zamanlı bir Sigma-Delta analog-sayısal dönüştürücü UMC 130nm teknolojisinde tasarlanmış ve üretilmiştir. Serim sonrası benzetim ve ölçüm sonuçları kıyaslanmıştır. Süzgeç bloğunda kullanılan akım kipli farksal integral alıcının pozitif geri bildirim etkisi nedeniyle benzetim ve deneylerde gözlenen gürültü seviyeleri yüksektir.

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LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
BW	Bandwidth
CT	Continuous Time
DAC	Digital to Analog Converter
DC	Direct Current
DT	Discrete Time
ENOB	Effective Number Of Bits
FFT	Fast Fourier Transform
FoM	Figure of Merit
IC	Integrated Circuit
MASH	Multi-Stage Noise Shaping
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	Negative-channel Metal Oxide Semiconductor
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PMOS	Positive-channel Metal Oxide Semiconductor
PSD	Power Spectral Density
SMA	SubMiniature version A
SNR	Signal to Noise Ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
UMC	United Microelectronics Corporation
VCO	Voltage Controlled Oscillator

1. INTRODUCTION

Demand for mobile and compact devices has been increasing in the last decades. The power need of multifunctional consumer electronic devices such as smart phones, tablets, GPSs etc. is in the tendency to increase as well. One solution is to increase the efficiency of batteries, while the other one is to reduce power consumption of devices. Realization of low power circuits has become crucial in this content.

Analog to digital converters are key building blocks between the real world and the digital domain of electronic devices. ADCs can be studied in two main categories: Nyquist rate ADCs (Full-Flash, Sub-Ranging, Successive Approximation, Pipeline etc.) and Oversampling ADCs (Delta, Sigma-Delta etc.). The main difference between these types is the ratio between the Nyquist frequency ($f_s/2$) and the signal bandwidth (f_B) which is called oversampling ratio as in Equation 1.1. Oversampling ADCs have high OSR values while Nyquist rate ADCs have typically less than 8 [1].

$$OSR = \frac{f_s}{2f_B} \tag{1.1}$$

Nyquist rate and oversampling methods can be compared as in Figure 1.1. Graphs on the left show that the bandwidth of the anti-aliasing filter should be narrow and the total quantization noise is mostly in the input signal band in Nyquist rate ADCs. Anti-aliasing filter specifications are relaxed and the quantization noise is smaller in the signal band in oversampling ADCs as seen in the right graphs of Figure 1.1 [1]. Among other converter types, Sigma-Delta ADCs are preferred in many fields such as sensor systems, digital signal processors, medical applications etc. because they can achieve high signal-to-noise ratio and low power consumption.

The block diagram of a first order Sigma-Delta modulator can be seen in Figure 1.2 [2]. $X(s)$ is analog input and $Y(s)$ is digitized output signal in s-domain. Here, the difference between the input and the output values is integrated and then quantized.

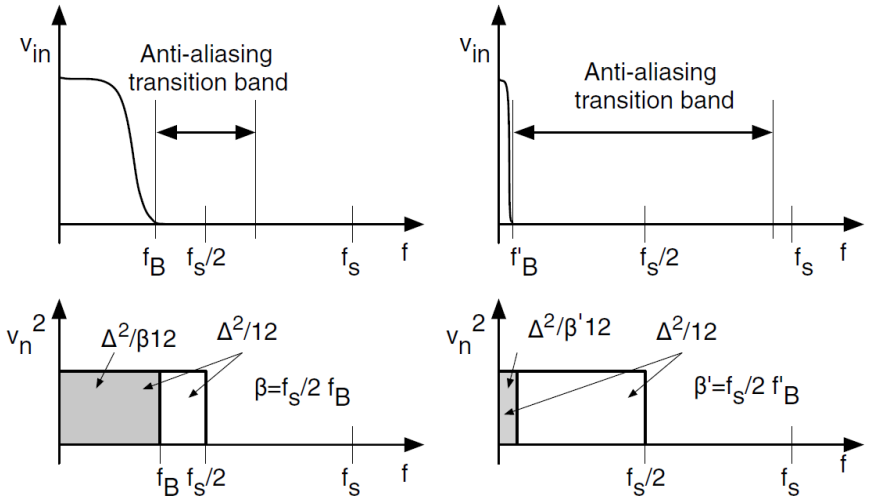

Figure 1.1. Comparison of Nyquist rate and oversampling methods [1].

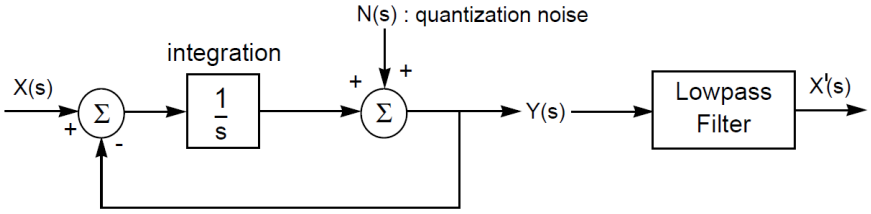

Figure 1.2. Block diagram of a first order Σ-Δ modulator [2].

(The name Sigma-Delta is coming from integration (sigma) of the difference (delta) of signals [1].) Summation symbol after the integration represents the quantizer and $N(s)$ stands for quantization noise which is the difference between the integrated signal and the output of the quantizer. Therefore, it is an error rather than an actual noise source. Signal transfer function $\frac{Y(s)}{X(s)}$ is calculated assuming $N(s) = 0$ as in Equation 1.2.

$$\begin{aligned} Y(s) &= [X(s) - Y(s)] \cdot \frac{1}{s} \\ \frac{Y(s)}{X(s)} &= \frac{1/s}{1 + 1/s} = \frac{1}{s+1} \end{aligned} \tag{1.2}$$

Noise transfer function $\frac{Y(s)}{N(s)}$ is calculated assuming $X(s) = 0$ as in Equation 1.3.

$$\begin{aligned} Y(s) &= -Y(s)\frac{1}{s} + N(s) \\ \frac{Y(s)}{N(s)} &= \frac{1}{1+1/s} = \frac{s}{s+1} \end{aligned} \tag{1.3}$$

As seen from the Equations 1.2 and 1.3, the signal transfer function has low-pass and the noise transfer function has high-pass response. If the modulated signal passes through a digital low-pass filter, the quantization noise beyond the bandwidth will be filtered out and a signal close to the analog input will remain as seen in Figure 1.3.

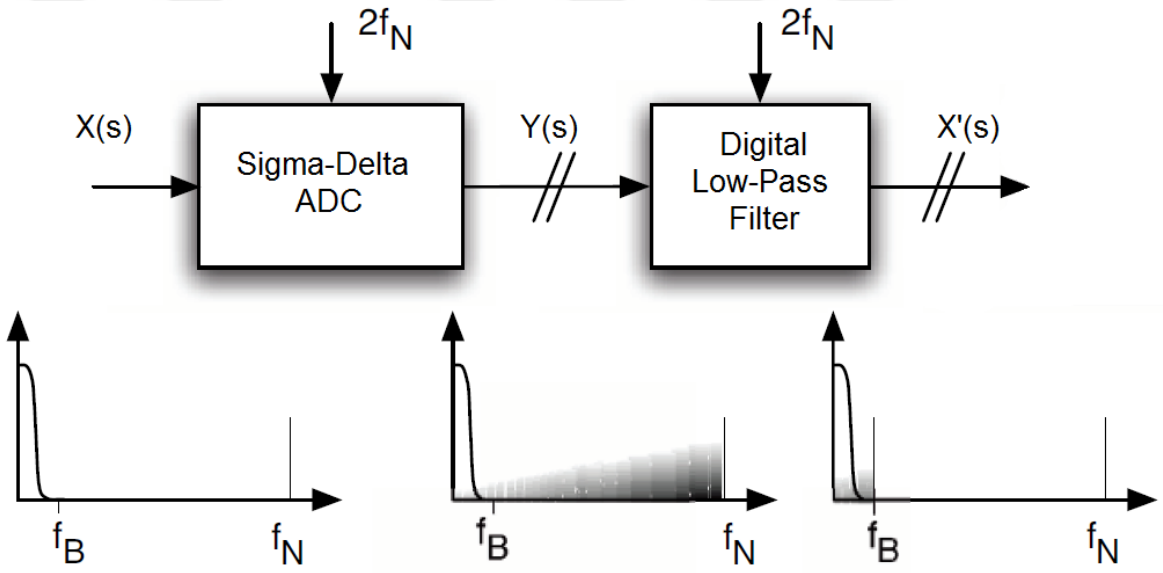

Figure 1.3. Noise shaping on Σ-Δ modulator and out-of-band noise rejection [1].

The signal and the noise transfer functions are calculated in Equations 1.2 and 1.3 assuming the Sigma-Delta modulator is first order as in Figure 1.2. Higher order filters can be used by cascading L integrators according to needed transfer functions as in Figure 1.4. The denominator of the signal and the noise transfer functions will have the term s^L which determines the order of the modulator and the noise shaping as well. Number of bits of the quantizer (n) determines the resolution of the output of the modulator which will be the input of digital low-pass filter. A comparator circuit can be used for 1-bit quantization while full-flash ADCs can be preferred for higher number of bits.

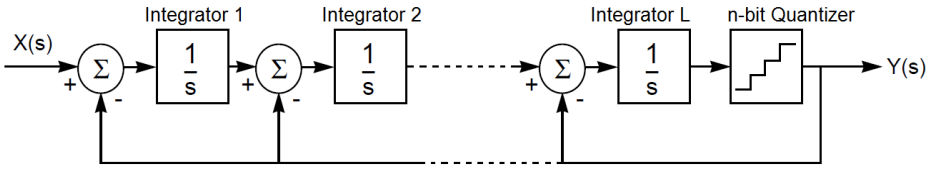

Figure 1.4. Block diagram of higher order Σ-Δ modulator.

SNR of an ADC is the ratio of the power of the input signal to the power of total noise in the circuit. Higher SNR means that the signal is converted successfully and is less noisy. Achievable maximum SNR value with ideal components according to the order of modulator (L), number of bits of the quantizer (n) and OSR is calculated as below [1].

$$SNR = \frac{3}{2}\frac{2L+1}{\pi^{2L}}OSR^{2L+1}2^{n-1} \tag{1.4}$$

$$SNR_{dB} = 1.76 + 3.01(log_2(2L+1) - 2Llog_2\pi + (2L+1)log_2OSR + 2(n-1)) \tag{1.5}$$

Effective number of bits (ENOB) is another specification of ADCs. It shows the resolution (number of bits that ADC can convert) of an ADC and it is directly related with SNR. Every bit of the output contributes SNR approximately 6.02dB as the formula below shows [1].

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} \tag{1.6}$$

Power effectiveness of an ADC is measured with Figure of Merit (FoM). It basically shows the energy consumed by the ADC per conversion. Definition of FoM differs in some sources. Assuming the most power is spent on the bandwidth of the

converted signal, FoM is calculated as below.

$$FoM = \frac{P_{tot}}{2^{ENOB} \cdot 2BW} \tag{1.7}$$

In Nyquist rate converters, sampling frequency(f_s) is used instead of BW [1].

After determining the order and bit number of the quantizer to satisfy the requirements, type of ADC should be determined. Filter block determines the type of Sigma-Delta converter as discrete time (DT), continuous time (CT) and hybrid structure which includes both designs. Discrete time ADCs are designed in z-domain while continuous time ADCs are designed in s-domain. Generally, discrete time designs are preferred in Σ-Δ ADCs. These structures are quite suitable for high frequency applications because they are not affected by clock jitter and excess loop delay. There are some tools prepared for architectural design of discrete time circuits and this makes design easier. Furthermore, one reason of preferring discrete time structures is that they typically utilize switched capacitor circuits which are relatively easier to design. However, this situation requires high supply voltage, so it has negative effect on power consumption.

Contrary to discrete time designs, supply voltages can be lower in continuous time designs because they do not require high voltages to switch-on sampled data paths. This issue helps to keep power consumption of CT designs low. Another advantage of the continuous time ADCs is their relaxed slew rates because there are no step transitions at the input of integrators as in DT circuits which need high slew rates. Even it is difficult to get linear operation in CT filters, the other features are generally advantageous with respect to DT designs especially low power consumption [1]. Furthermore, linearity problem can be solved using current-mode integrators as used in this study.

The study in this thesis focuses on continuous time filter types in Chapter 2. Derivation of continuous time current-mode differential integrator and its noise analysis is discussed in Chapter 3. In the next chapter, design considerations of integrated

circuit design of continuous time current-mode Sigma-Delta modulator and layouts are presented. Post-layout simulation results and chip measurement results are given in Chapter 5 while the following chapter makes the conclusion.

2. CONTINUOUS TIME INTEGRATORS

The most important block of Σ-Δ ADCs is the filter block. In continuous time structures, integrators are used as filter blocks. Integrators have similar transfer functions to low-pass filters with a pole at zero frequency ideally. There are several techniques to design a CT integrator. Various methods are presented in this chapter.

2.1. Passive RC Integrators

The simplest integrator design is passive RC integrators. Circuit schematic is in Figure 2.1. Transfer function is obtained as in Equation 2.1.

$$\frac{Y(s)}{X(s)} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = \frac{1/RC}{s + 1/RC} \tag{2.1}$$

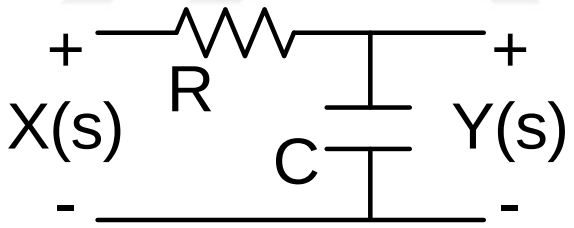

Figure 2.1. Passive RC integrator circuit.

The cut-off frequency w_0 of the filter is $\frac{1}{RC}$ as seen from the transfer function. Resistance and capacitance values should be high in order the pole to be at low frequencies for the integrator can be used in Sigma-Delta ADCs. High resistance causes high thermal noise which makes the integrator not appropriate for a high SNR ADC design while high capacitance means high chip area.

2.2. Active RC Integrators

Active RC integrators are implemented as connecting a resistor to the inverting input of an op-amp and a capacitor as feedback from the output as in Figure 2.2.

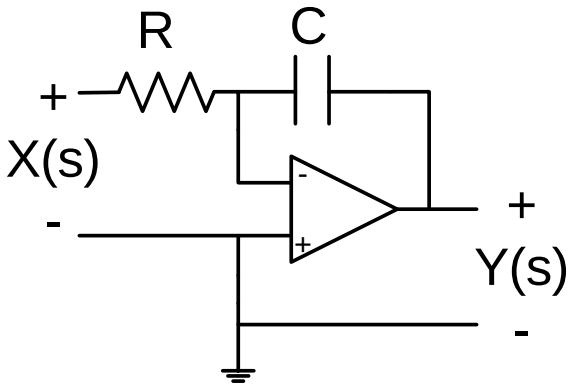

Figure 2.2. Active RC integrator circuit.

Transfer function of the active RC integrator is:

$$\frac{Y(s)}{X(s)} = \frac{\frac{-1}{sC}}{R} = \frac{-1}{sRC} \tag{2.2}$$

If a low-noise op-amp with high gain can be designed, high SNR values are achieved using active RC integrators. However, this situation is valid for lower frequencies where the loop gain is high. Beside the frequency limit, op-amps with high gain generally require high power. Furthermore, absolute accuracy of passive components is low in some technologies and this brings difficulties in design. MOSFETs which are used as tunable resistors can solve this problem as presented in the next section [3].

2.3. MOSFET-C Integrators

When the resistor of active RC integrator is changed with a MOSFET as in Figure 2.3, tuning become possible. R_{DS} resistance of the MOSFET replaces the resistor in the active RC integrator and the time constant can be changed after the production of circuit. The value of R_{DS} is inversely proportional to control voltage V_C when the MOSFET is kept in linear region which means V_{DS} value to be small. For higher values of V_{DS}, the MOSFET goes into saturation region and I_{DS}-V_{DS} characteristics change. This change causes distortion; however, this problem can be solved by using

differential structure. Transfer function of MOSFET-C integrators is same as active RC ones as in Equation 2.2. Beside the bandwidth constraints similar to active RC integrators, MOSFET-C integrators require high supply voltage for a wide range of tuning [3].

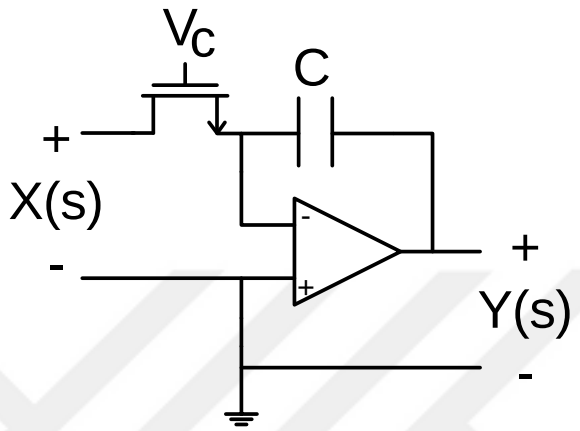

Figure 2.3. MOSFET-C integrator circuit.

2.4. g_m-C Integrators

g_m-C (transconductance-C) integrators are simply composed of an operational transconductance amplifier (OTA) and a capacitor connected to its output as in Figure 2.4. Input voltage creates an output current which is integrated by an integrating capacitance and turns into output voltage. Transfer function of an ideal g_m-C integrator can be calculated as below.

$$\begin{aligned} I_{out}(s) &= V_{in}(s) \cdot g_m \\ V_{out}(s) &= I_{out}(s) \cdot \frac{1}{sC} \\ H(s) = \frac{V_{out}(s)}{V_{in}(s)} &= \frac{I_{out}(s) \cdot \frac{1}{sC}}{\frac{I_{out}(s)}{g_m}} = \frac{g_m}{sC} \end{aligned} \tag{2.3}$$

Any transconductance topology can be applied in the design of g_m-C integrators. Simplified versions of amplifiers are quite suitable for this type of integrator in order to

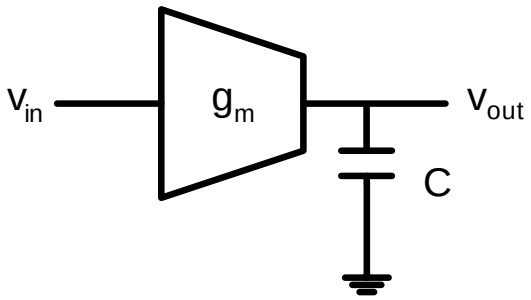

Figure 2.4. g_m-C integrator circuit.

reach high frequencies contrary to active RC and MOSFET-C integrators. Differential structures should be preferred for avoiding the even-order harmonics [3].

2.5. C-g_m Integrators

The last integrator type presented in this chapter is current-mode C-g_m integrator which can be seen in Figure 2.5 basically.

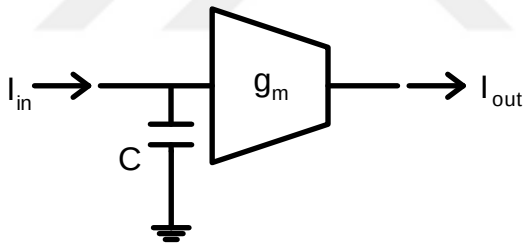

Figure 2.5. C-g_m integrator circuit.

The working principle of this circuit is opposite to that of the g_m-C integrator. Because the input is current, it fills the input capacitance and creates a voltage on it. Then the transconductance circuit turns the input voltage to output current. The name "C-g_m" comes from the operation of the circuit in this order. Transfer function

of this integrator is found as below.

$$\begin{aligned} V_{in}(s) &= I_{in}(s) \cdot \frac{1}{sC} \\ I_{out}(s) &= V_{in}(s) \cdot g_m \\ H(s) = \frac{I_{out}(s)}{I_{in}(s)} &= \frac{V_{in}(s) \cdot g_m}{\frac{V_{in}(s)}{\frac{1}{sC}}} = \frac{g_m}{sC} \end{aligned} \tag{2.4}$$

A differential version of a current-mode C-g_m integrator is implemented and its noise analysis is performed in the next chapter. It is also used in the design of 2nd order continuous time current-mode Sigma-Delta analog-to-digital converter as presented in Chapter 4.

Basic comparison of continuous time integrators can be seen in Table 2.1.

Table 2.1. Comparison of continuous time integrators.

Type	**Operating Mode**	**Linearity**	**Noise**	**Power**	**First Pole Freq.**	**Absolute Accuracy**	**Operation Freq.**
Passive RC	Voltage	Good	High	Low	Nonzero	Low	Wide
Active RC	Voltage	Good	High	High	Zero	Low	Narrow
MOSFET-C	Voltage	Good in a limited range	High	High	Zero	High	Narrow
g_m-C	Voltage	Good in differential mode	Low	Low	Zero	High	Wide
C-g_m	Current	Good in differential mode	Low	Low	Zero	High	Wide

3. CONTINUOUS TIME CURRENT-MODE C-g_m INTEGRATOR AND NOISE ANALYSIS

Noise performance is one of the most important specifications for data converters especially in Σ-Δ ADCs as discussed in previous chapters. Since the integrator is the input stage of the ADC, its noise contribution to the overall system is quite important. Derivation of the continuous time differential C-g_m integrator and its detailed noise analysis is presented in this chapter. Calculations are compared with simulations which are performed on Mentor Graphics ELDO with 130nm process technology.

3.1. Single-Ended C-g_m Integrator

The basic building block of the current-mode continuous-time integrator is the current-mirror circuit as in Figure 3.1 [4]. As seen from the small-signal equivalent circuit, this circuit behaves as a low-pass filter. Its transfer function in s-domain is

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{-\frac{g_{m2}}{C}}{s + \frac{g_{m1}}{C}} \tag{3.1}$$

ignoring parasitic capacitances and the output resistances of transistors. AC analysis results of the filter can be seen in Figure 3.2. Dimensions of NMOS transistors are arranged such that $(\frac{W}{L})_n = \frac{0.3\mu}{5.75\mu}$, so g_m's are equal to 3.10μS with 130nA bias current and 1.5pF capacitance.

In the current-mirror circuit, PMOS transistors can be used as bias current sources as in Figure 3.3. Assuming ideal components and infinite output resistances of PMOS transistors, this circuit has the same small-signal equivalent and the same transfer function as the circuit in Figure 3.1. When the input current or voltage value changes, transconductance of the input transistor g_{m1} changes and the circuit has nonlinear transfer function as seen from Equation 3.1.

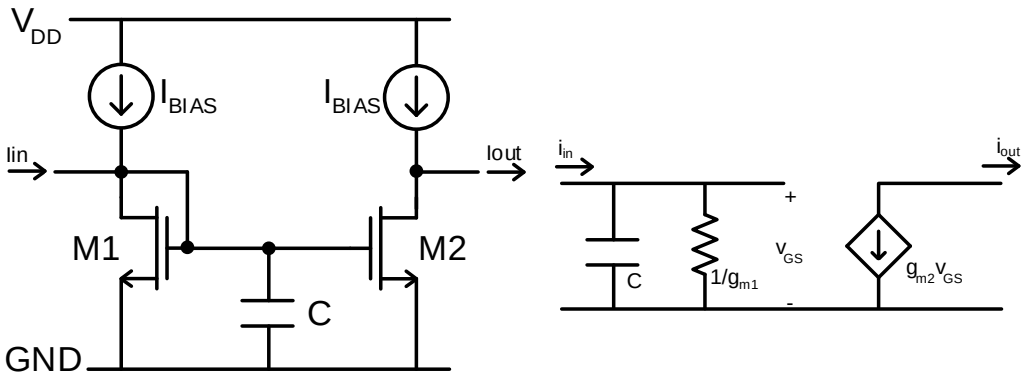

Figure 3.1. Simple current-mirror circuit and its small-signal equivalent [4].

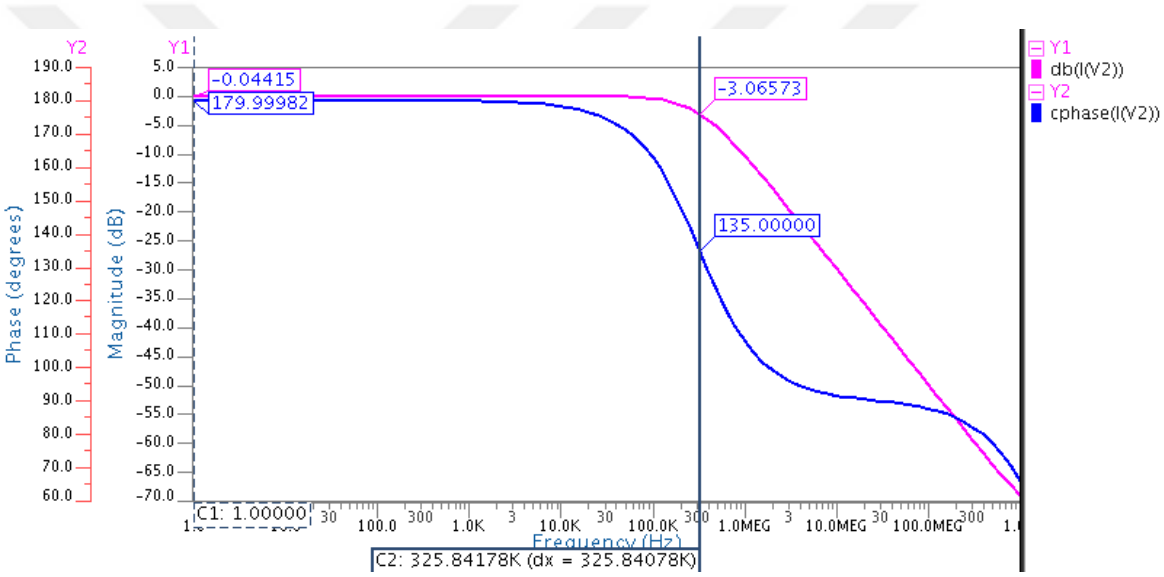

Figure 3.2. AC analysis results of the simple current-mirror circuit.

In order to solve the nonlinearity problem, another configuration as in Figure 3.4 can be used [5]. In this case, the output branch of the integrator resembles the logic inverter circuit. At the input branch, parallel $1/g_{m1}$ and $1/g_{m2}$ resistances contribute an equivalent $\frac{1}{g_{m1}+g_{m2}}$ resistance. For a linear operation, the input resistance should not change with the changes at the input. It requires that $g_{m1} + g_{m2}$ should be constant and MOSFETs should be in saturation region. g_m values of $M1$ and $M2$

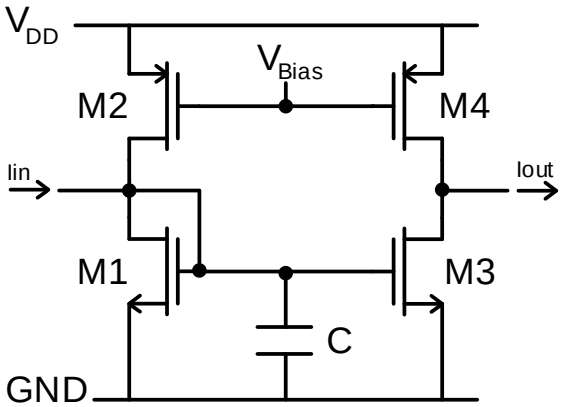

Figure 3.3. Current mirror circuit with PMOS transistors as bias current sources.

transistors are calculated as below.

$$\begin{aligned} g_{m1} &= \mu_n \cdot C_{ox} \cdot (\frac{W}{L})_n \cdot (V_{in} - V_{tn}) \\ g_{m2} &= \mu_p \cdot C_{ox} \cdot (\frac{W}{L})_p \cdot (V_{DD} - V_{in} - V_{tp}) \end{aligned} \tag{3.2}$$

If the coefficients of V_{in} are equal to each other as below, $g_{m1} + g_{m2}$ will be constant independent from the V_{in} value.

$$\mu_n \cdot C_{ox} \cdot (\frac{W}{L})_n = \mu_p \cdot C_{ox} \cdot (\frac{W}{L})_p \tag{3.3}$$

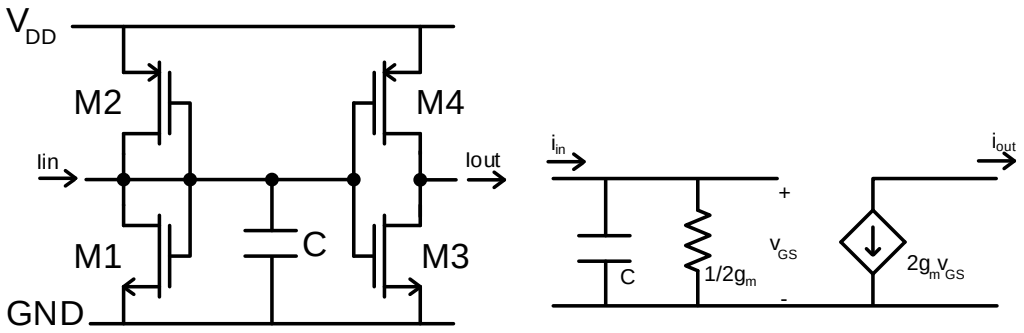

Figure 3.4. Inverter type integrator and its small-signal equivalent.

For ease of design and calculation, all transistors are selected to have equal transconductance g_m. In this way, two parallel $1/g_m$ resistances at the input branch

contribute an equivalent $1/2g_m$ resistance and total $2g_m v_{GS}$ current flows at the output. AC analysis results of the circuit can be seen in Figure 3.5 which has transfer function in s-domain as in Equation 3.4. Dimensions of PMOS transistors are arranged as $(\frac{W}{L})_p = \frac{1.4\mu}{5.35\mu}$ for 130nA bias current and 3.10μS transconductance. Other components are same with the circuit in Figure 3.1.

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{-\frac{2g_m}{C}}{s + \frac{2g_m}{C}} \tag{3.4}$$

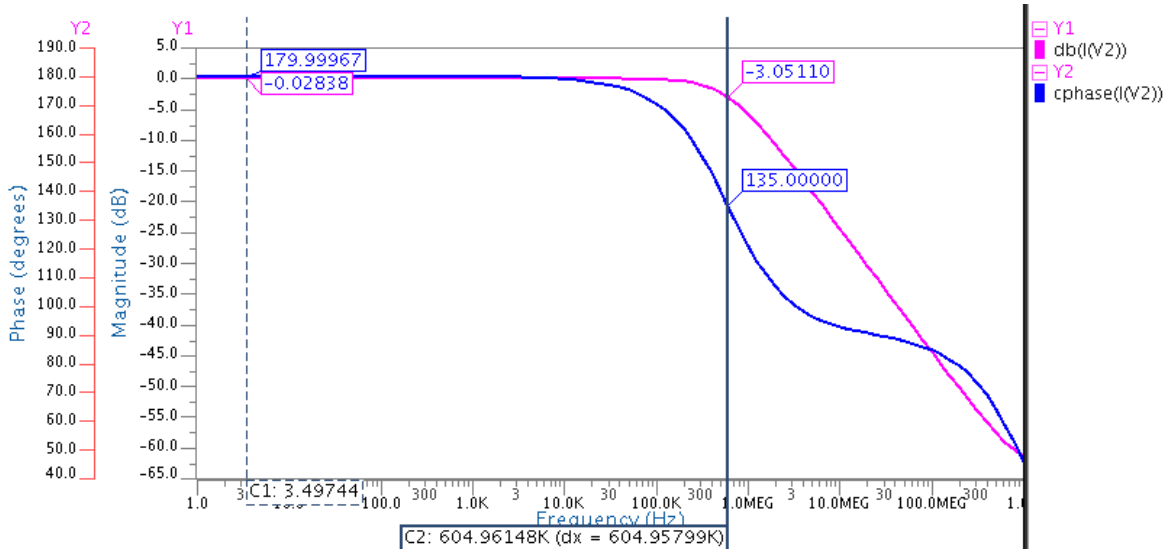

Figure 3.5. AC analysis results of the inverter type integrator circuit.

3.2. Noise Analysis of Single-Ended C-g_m Integrator

Thermal noise of the MOSFET should be studied in detail to make a complete analysis. A MOSFET creates thermal noise due to its resistive channel. This channel noise can be represented by a current noise source $\overline{di_{DS}^2}$ as in the Figure 3.6. The effective channel resistor R_{CH} is equal to $\frac{3}{2g_m}$ [3].

Current noise can be calculated as below where k is the Boltzmann constant and T is the absolute temperature which is typically 300K [3].

$$\overline{di_{DS}^2} = \frac{4kT}{R_{CH}}df = 4kT\frac{2}{3}g_m df \tag{3.5}$$

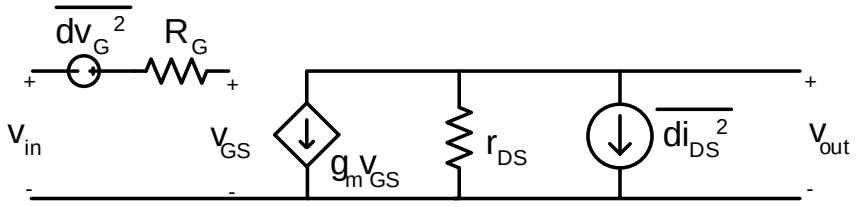

Figure 3.6. Noise modelling of MOSFET [3].

Here, R_G is the poly gate resistor caused by the extension of the Gate line outside the active region. Because the analysis is made on the schematic of the circuit, R_G is ignored in our calculations. Therefore $\overline{dv_G^2}$ is zero according to formula in Equation 3.6 [3].

$$\overline{dv_G^2} = 4kTR_G df. \tag{3.6}$$

The channel noise current is reflected to input voltage by dividing current noise by g_m (g_m^2 for power). Equivalent input noise model can be seen in Figure 3.7.

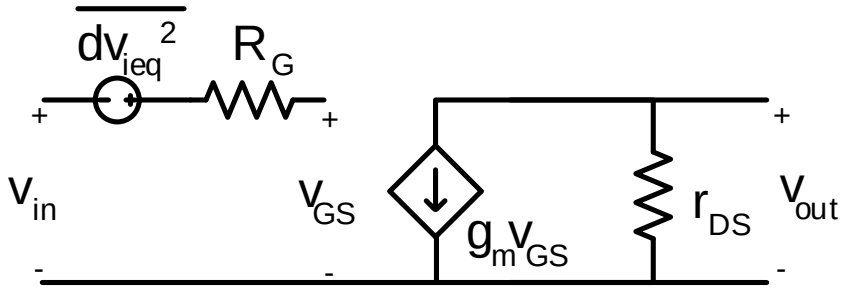

Figure 3.7. Equivalent input noise model [3].

$$\overline{dv_{ieq}^2} = 4kTR_{eff} df \tag{3.7}$$

$$R_{eff} = \frac{2/3}{g_m} + R_G \tag{3.8}$$

Input branch of the inverter type current-mode integrator is in Figure 3.8. Tran-

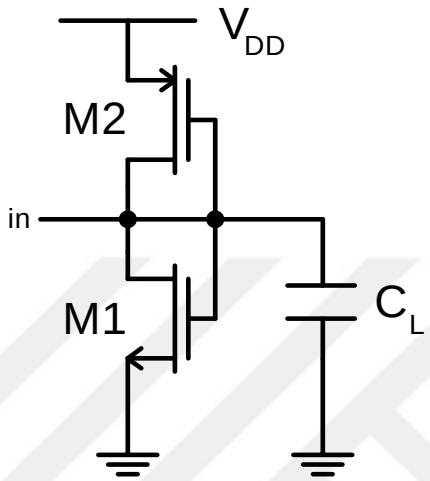

Figure 3.8. Input branch of the inverter type current-mode integrator.

sistor sizes should be selected for g_{m1} and g_{m2} to be equal in order to get a linear operation. Because the noise sources are uncorrelated, current noises can be added.

$$\overline{di_{in}^2} = 4kT\frac{2}{3}(g_{m1} + g_{m2})df \tag{3.9}$$

There are two diode connected MOSFETs in parallel, so the equivalent input resistance is

$$R_{in} = r_{o1}//r_{o2}//\frac{1}{g_{m1} + g_{m2}} \approx \frac{1}{g_{m1} + g_{m2}} \tag{3.10}$$

while output resistances of transistors are very large. Therefore, equivalent input noise can be found by multiplying current noise with R_{in}^2 as below.

$$\overline{dv_{in}^2} = 4kT\frac{2}{3(g_{m1} + g_{m2})}df \tag{3.11}$$

Single-ended part of the integrator is seen in Figure 3.4. Here, the current noise at the input branch is multiplied by the square of current gain and added to the current noise at the output branch. Then, multiplying that value with square of the output resistance gives the equivalent voltage noise at the output. Dimensions of $M_1 = M_3$ and $M_2 = M_4$, so $g_{m1} = g_{m3}$, $g_{m2} = g_{m4}$ and the current gain A_c is approximately equal to 1.

$$\begin{aligned}\overline{di_{out}^2} &= \overline{di_{in}^2}A_c^2 + 4kT\frac{2}{3}(g_{m3} + g_{m4})df \\ &= 4kT\frac{2}{3}(g_{m1} + g_{m2} + g_{m3} + g_{m4})df\end{aligned} \tag{3.12}$$

Since the output resistance R_{out} is equal to $r_{o3}//r_{o4}$, output voltage noise can be obtained as below.

$$\overline{dv_{out}^2} = \overline{di_{out}^2}R_{out}^2 = 4kT\frac{2}{3}(g_{m1} + g_{m2} + g_{m3} + g_{m4})(r_{o3}//r_{o4})^2df \tag{3.13}$$

Noise simulations are performed with the same dimensions of the components such that $(\frac{W}{L})_p = \frac{1.4\mu}{5.35\mu}$, $(\frac{W}{L})_n = \frac{0.3\mu}{5.75\mu}$, so all g_m's are equal to 3.10μS and $r_{op} = 222\text{M}\Omega$, $r_{on} = 63\text{M}\Omega$. When these values are used in Equations 3.11 and 3.13, the results will be as below.

$$\overline{dv_{in}^2} = 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot \frac{2}{3(3.10\mu + 3.10\mu)}df \approx 1.78\text{fV}^2/\text{Hz} \tag{3.14}$$

$$\overline{dv_{out}^2} = 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot \frac{2}{3}(4 \cdot 3.10\mu)(63M//222M)^2df \approx 329.68\text{pV}^2/\text{Hz} \tag{3.15}$$

Noise simulation results for the circuit in Figure 3.4 can be seen in Figure 3.9. Comparison of calculations and simulation results are given in Table 3.1.

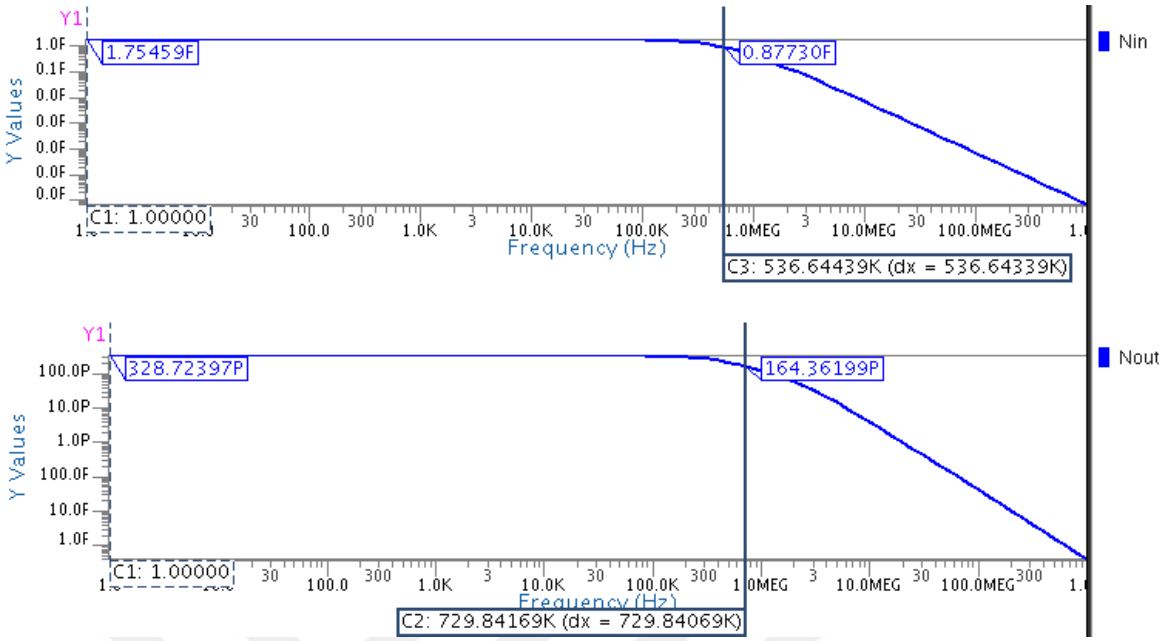

Figure 3.9. Noise simulation results for input and output nodes of the circuit in Figure 3.4.

Table 3.1. Comparison of calculation and simulation results for the noise analysis of the circuit in Figure 3.4.

Noise	**Calculation**	**Simulation**
$\overline{dv_{in}^2}$	1.78 fV^2/Hz	1.75 fV^2/Hz
$\overline{dv_{out}^2}$	329.68 pV^2/Hz	328.72 pV^2/Hz

3.3. Differential C-g_m Integrator

Differential current-mode integrator can be built by cascading two single-ended integrators with the output of the second stage fed back to the input summing node of the first stage as in Figure 3.10. In order for the current to pass to the next stages, current-mirror circuits with the same aspect ratio can be used as output stages of the integrator (M_{111} and M_{222} in the figure). This type of configuration has been proposed in [6–8].

Block diagram of the differential current-mode integrator is shown in Figure 3.11 [4]. H_1 and H_2 are transfer functions of the single-ended integrators which have

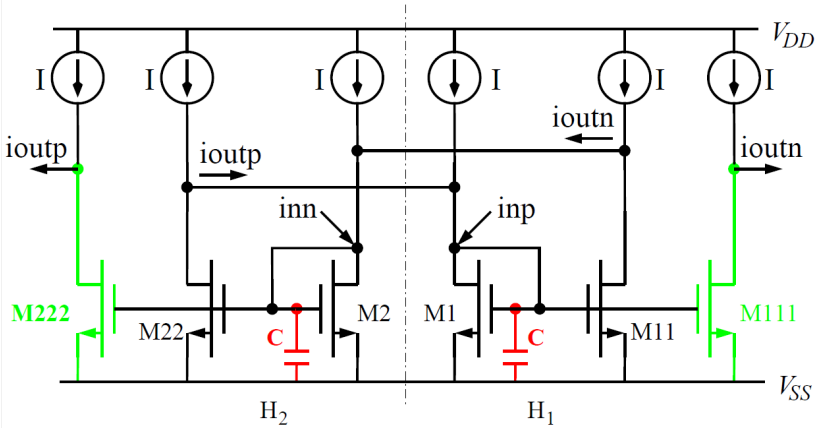

Figure 3.10. Differential current-mode integrator [4].

been calculated in Equation 3.1. Output currents of the cross-coupled integrators are added to the input currents of each other. Assuming both integrators have the same transfer function H and all transistors are matched such that they have equal transconductance g_m, transfer function of the differential current-mode integrator in s-domain is calculated as below [4].

$$\begin{aligned} i_{outn} &= H_1(i_{inp} + i_{outp}) \\ i_{outp} &= H_2(i_{inn} + i_{outn}) \\ H_1 = H_2 = H &= \frac{-g_m}{g_m + sC} \end{aligned} \tag{3.16}$$

Replacing H and i_{outp} in the first formula yields:

$$\begin{aligned} i_{outn} &= H(i_{inp} + H(i_{inn} + i_{outn})) \\ i_{outn} &= \frac{H(i_{inp} + H \cdot i_{inn})}{1 - H^2} \end{aligned} \tag{3.17}$$

In a similar manner, i_{outp} becomes:

$$\begin{aligned} i_{outp} &= H(i_{inn} + H(i_{inp} + i_{outp})) \\ i_{outp} &= \frac{H(i_{inn} + H \cdot i_{inp})}{1 - H^2} \end{aligned} \tag{3.18}$$

Then, differential current transfer function becomes:

$$\begin{aligned} i_{outp} - i_{outn} &= \frac{i_{inp}(H^2 - H) - i_{inn}(H^2 - H)}{1 - H^2} \\ \frac{i_{outp} - i_{outn}}{i_{inp} - i_{inn}} &= \frac{H^2 - H}{1 - H^2} = \frac{-H}{1 + H} = \frac{\frac{g_m}{g_m + sC}}{\frac{g_m + sC - g_m}{g_m + sC}} = \frac{g_m}{sC} \end{aligned} \tag{3.19}$$

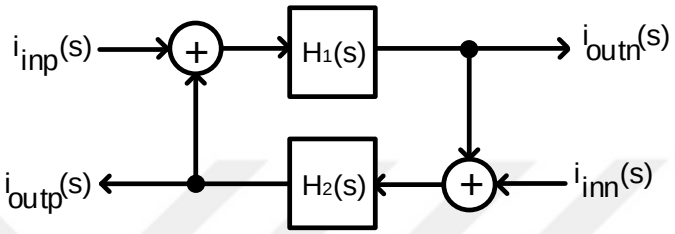

Figure 3.11. Block diagram of the differential current-mode integrator [4].

Comparing Equations 3.1 and 3.19, it is seen that the pole is moved to 0 Hz frequency with differential structure assuming ideally matched g_m's and ignoring output resistances (r_o) of transistors. When the output resistances of transistors are considered, small-signal model of the single-ended integrator in Figure 3.1 is changed as in Figure 3.12. Here, R_L is load impedance which is the input impedance of the other integrator because the integrators are cross-coupled to each other. Calculation of the transfer function of differential integrator with output resistances taken into account is the same as in Equations 3.16 to 3.19 except that:

$$H = \frac{-g_m}{g_m + sC} \cdot \frac{r_o}{r_o + R_L} \tag{3.20}$$

$$R_L = \frac{1}{sC} // \frac{1}{g_m} = \frac{1}{g_m + sC} \tag{3.21}$$

Substitution Equation 3.20 into Equation 3.19 yields:

$$\frac{i_{outp} - i_{outn}}{i_{inp} - i_{inn}} = \frac{H^2 - H}{1 - H^2} = \frac{-H}{1 + H} = \frac{\frac{g_m}{C}}{s + \frac{1}{r_o C}} \tag{3.22}$$

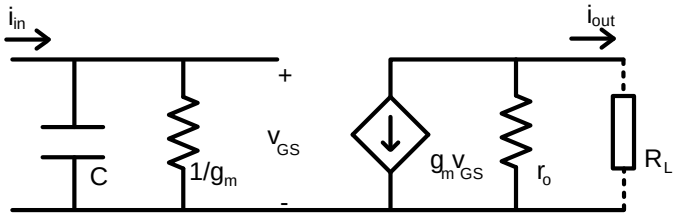

Figure 3.12. Small-signal equivalent of the single-ended integrator with output resistance.

AC analysis results of the differential current-mode integrator can be seen in Figure 3.13.

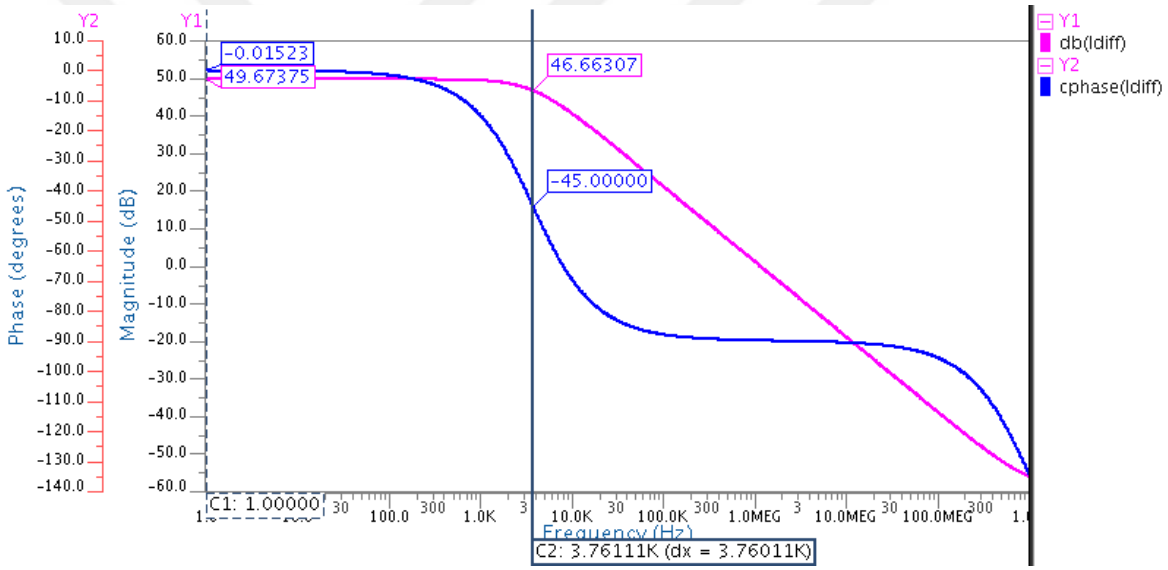

Figure 3.13. AC analysis results of the differential current-mode integrator.

3.4. Noise Analysis of Differential C-g_m Integrator

Noise analysis of differential current-mode integrator is different from the single-ended one. In the literature, the input referred noise power for differential current-mode integrator is calculated as below where N_{tr} is the number of transistors adding noise to the signal [4, 6].

$$\overline{di_{in}^2} = 4kT\frac{2}{3}g_m N_{tr} df \tag{3.23}$$

However, the analysis in this section with the simulation results show that in order to calculate noise of differential integrator, the positive feedback should be taken into account. In order to make a straight feedback analysis, the loop should be broken and the remaining two cascaded single-ended integrators should be examined as in Figure 3.14. Since there are two diode connected MOSFETs M_5 and M_6 at the middle node, $R_{mid} \approx \frac{1}{g_{m5}+g_{m6}}$. R_{in} $[\frac{1}{g_{m1}+g_{m2}}]$ and R_{out} $[r_{o7}//r_{o8}]$ values are same with the previous ones. Transistors again have same dimensions and g_ms, so the current gain A_c is approximately equal to 1 for both stages. Current and voltage noise calculations are as below.

$$\overline{di_{in}^2} = 4kT\frac{2}{3}(g_{m1} + g_{m2})df \tag{3.24}$$

$$\overline{di_{mid}^2} = \overline{di_{in}^2}A_c^2 + 4kT\frac{2}{3}(g_{m3} + g_{m4} + g_{m5} + g_{m6})df \approx 3\overline{di_{in}^2} \tag{3.25}$$

$$\overline{di_{out}^2} = \overline{di_{mid}^2}A_c^2 + 4kT\frac{2}{3}(g_{m7} + g_{m8})df \approx 4\overline{di_{in}^2} \tag{3.26}$$

$$\overline{dv_{in}^2} = 4kT\frac{2}{3(g_{m1} + g_{m2})}df \tag{3.27}$$

$$\overline{dv_{mid}^2} = \overline{di_{mid}^2}R_{mid}^2 \approx 4kT\frac{2}{(g_{m5} + g_{m6})}df \tag{3.28}$$

$$\overline{dv_{out}^2} = \overline{di_{out}^2}R_{out}^2 \approx 4kT\frac{8}{3}(g_{m7} + g_{m8})(r_{o7}//r_{o8})^2df \tag{3.29}$$

Simulations are performed with the same conditions and same dimensions of components used in the circuit in Figure 3.4. When those g_m and output resistance

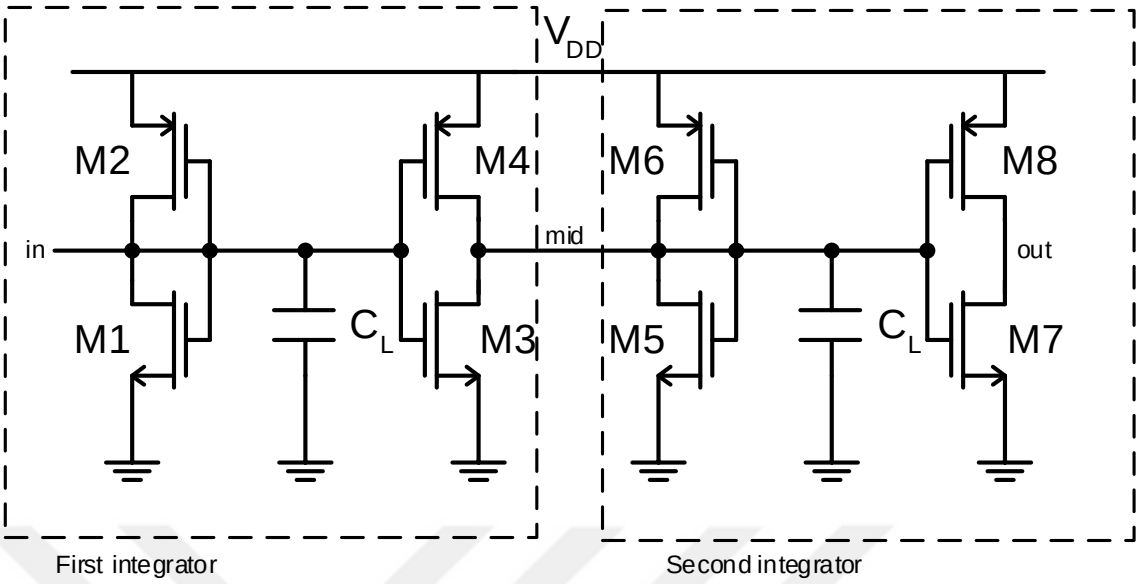

Figure 3.14. Two current-mode integrators in cascade.

values are used in Equations 3.27, 3.28 and 3.29; results will be as seen below.

$$\overline{dv_{in}^2} = 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot \frac{2}{3(3.10\mu + 3.10\mu)} df \approx 1.78\text{fV}^2/\text{Hz} \tag{3.30}$$

$$\overline{dv_{mid}^2} = 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot \frac{2}{(3.10\mu + 3.10\mu)} df \approx 5.34\text{fV}^2/\text{Hz} \tag{3.31}$$

$$\begin{aligned} \overline{dv_{out}^2} &= 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot \frac{8}{3}(3.10\mu + 3.10\mu)(63\text{M}//222\text{M})^2 df \\ &\approx 659.35\text{pV}^2/\text{Hz} \end{aligned} \tag{3.32}$$

Noise simulation results for the circuit in Figure 3.14 can be seen in Figure 3.15. Comparison of calculations and simulation results are given in Table 3.2.

Feedback loop should be closed as the next step of the noise analysis of current-mode differential integrator. Schematic of the circuit can be seen in Figure 3.16 whose block diagram is given in Figure 3.11. There are two identical integrators with voltage

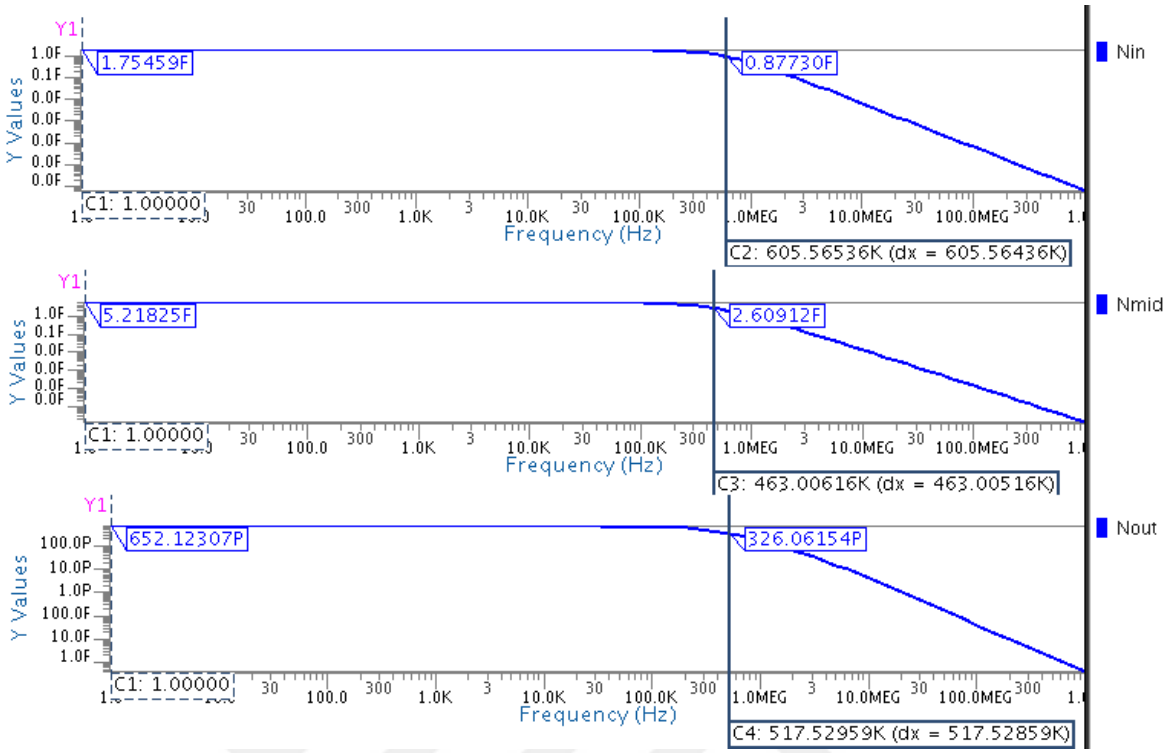

Figure 3.15. Noise simulation results for input, middle and output nodes of the circuit in Figure 3.14 respectively.

gain A_v are cascaded and input is fed back from output for the feedback gain β to be equal to 1. The total voltage noise at the output node is the noise contributed by middle node plus the noise contributed by input node.

It should be noted that A_v is approximately -1V/V and its exact value is taken from the simulation as -0.056dB with -180° phase which is equal to -0.993V/V as seen from Figure 3.17.

Table 3.2. Comparison of calculation and simulation results for the noise analysis of the circuit in Figure 3.14.

Noise	**Calculation**	**Simulation**
$\overline{dv_{in}^2}$	1.78 fV^2/Hz	1.75 fV^2/Hz
$\overline{dv_{mid}^2}$	5.34 fV^2/Hz	5.22 fV^2/Hz
$\overline{dv_{out}^2}$	659.35 pV^2/Hz	652.12 pV^2/Hz

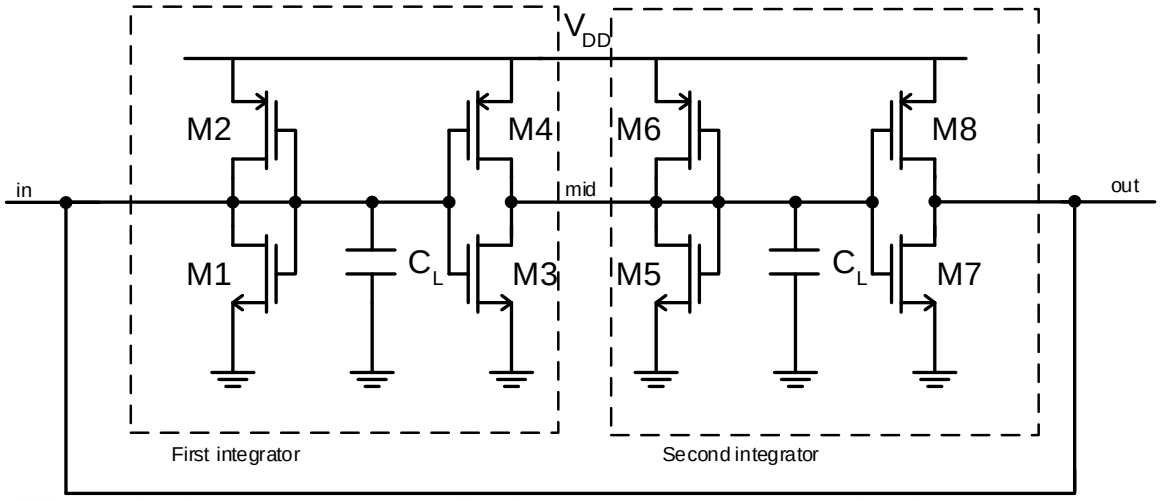

Figure 3.16. Circuit schematic of the differential current-mode integrator.

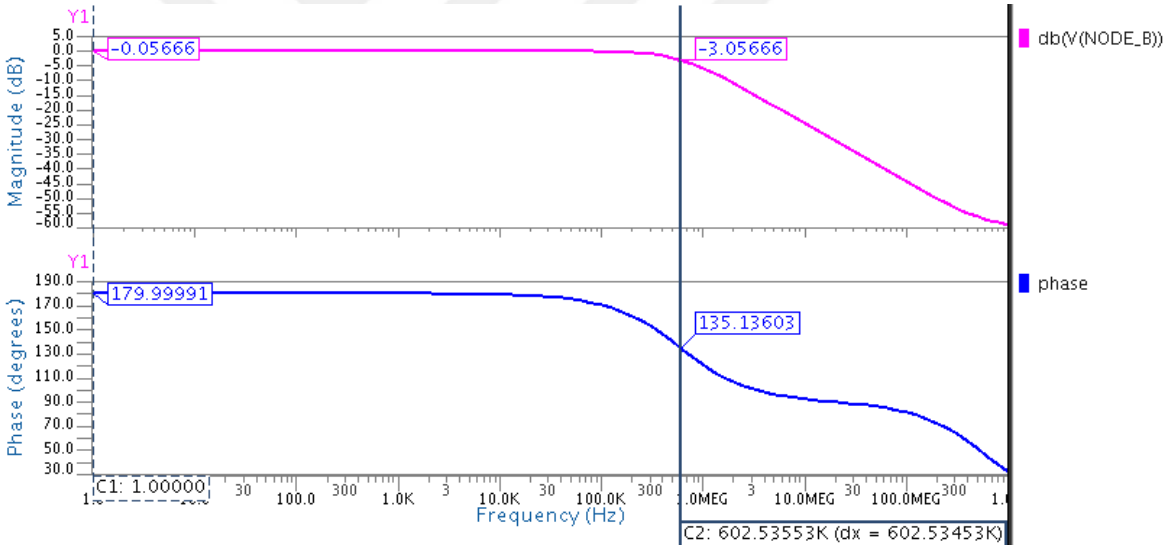

Figure 3.17. AC analysis results for voltage gain A_v.

Because the circuit is symmetric, the noises caused by the transistors at input node and at middle node are equal and can be calculated as done in Equations 3.27 and 3.28 (Because these are not total noise at those nodes, they are shown with N to avoid confusion) as below.

$$\overline{dN_{mid}^2} = 4kT\frac{2}{3}\frac{(g_{m3}+g_{m4}+g_{m5}+g_{m6})}{(g_{m5}+g_{m6})^2}df = 3.56\text{fV}^2/\text{Hz} \tag{3.33}$$

$$\overline{dN_{in}^2} = 4kT\frac{2}{3}\frac{(g_{m1}+g_{m2}+g_{m7}+g_{m8})}{(g_{m1}+g_{m2})^2}df = 3.56\text{fV}^2/\text{Hz} \tag{3.34}$$

Loop gain should be determined to find the closed loop gain.

$$\textit{Loop Gain} = A_{v1}\cdot A_{v2}\cdot\beta = A_v^2\cdot\beta = A_v^2 = (-0.993)^2 = 0.987 \tag{3.35}$$

Closed loop gain from input to output is calculated.

$$A_{i-o} = \frac{A_v^2}{1-A_v^2} = \frac{0.987}{1-0.987} \approx 75.92V/V \tag{3.36}$$

Closed loop gain from middle node to output is calculated.

$$A_{m-o} = \frac{A_v}{1-A_v^2} = \frac{-0.993}{1-0.987} \approx -76.38V/V \tag{3.37}$$

Total voltage noise at the output node is calculated as below.

$$\begin{aligned}\overline{dv_{out}^2} &= \overline{dN_{in}^2}\cdot A_{i-o}^2 + \overline{dN_{mid}^2}\cdot A_{m-o}^2 \\ &= 3.56\cdot 10^{-15}\cdot 75.92^2 + 3.56\cdot 10^{-15}\cdot(-76.38)^2 \\ &= 41.29\text{pV}^2/\text{Hz}\end{aligned} \tag{3.38}$$

$\overline{dv_{mid}^2}$ is equal to $\overline{dv_{out}^2}$ because of the symmetric structure of the circuit. Simulation results can be seen in Figure 3.18. Comparison of calculations and simulation results are given in Table 3.3.

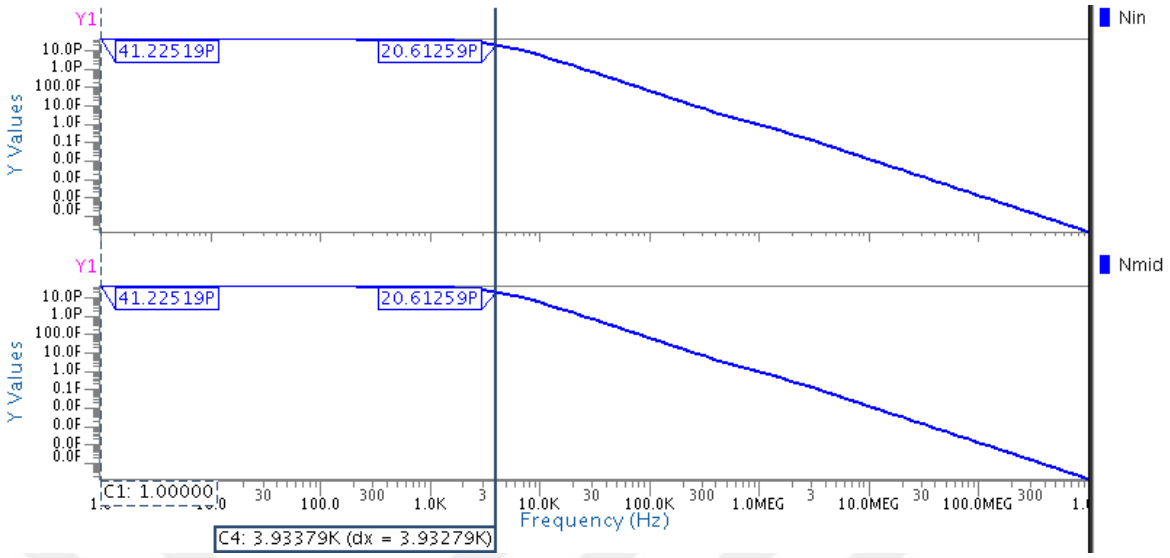

Figure 3.18. Noise simulation results for both nodes of the circuit in Figure 3.16.

Table 3.3. Comparison of calculation and simulation results for the noise analysis of the circuit in Figure 3.16.

Noise	**Calculation**	**Simulation**
$\overline{dv_{in}^2}$	41.29 pV^2/Hz	41.23 pV^2/Hz
$\overline{dv_{mid}^2}$	41.29 pV^2/Hz	41.23 pV^2/Hz

3.5. DC-Gain Enhancement Resistor and Its Effect to Noise

DC-gain is an important factor for integrators [5, 9]. An ideal integrator should have infinite gain at zero frequency as shown in Equation 3.19. In order to increase DC-gain, a tunable resistor R_T can be used in cascode current-mirror based differential current-mode integrators as in Figure 3.19 [10].

DC-gain enhancement technique in Figure 3.19 can be applied to inverter type current-mode integrators as in Figure 3.20. Because there is no cascode structure and the middle of the resistor R_T behaves as virtual ground, that resistor can be divided into two parts and connected between supply nodes and sources of the MOSFETs as R_e [11].

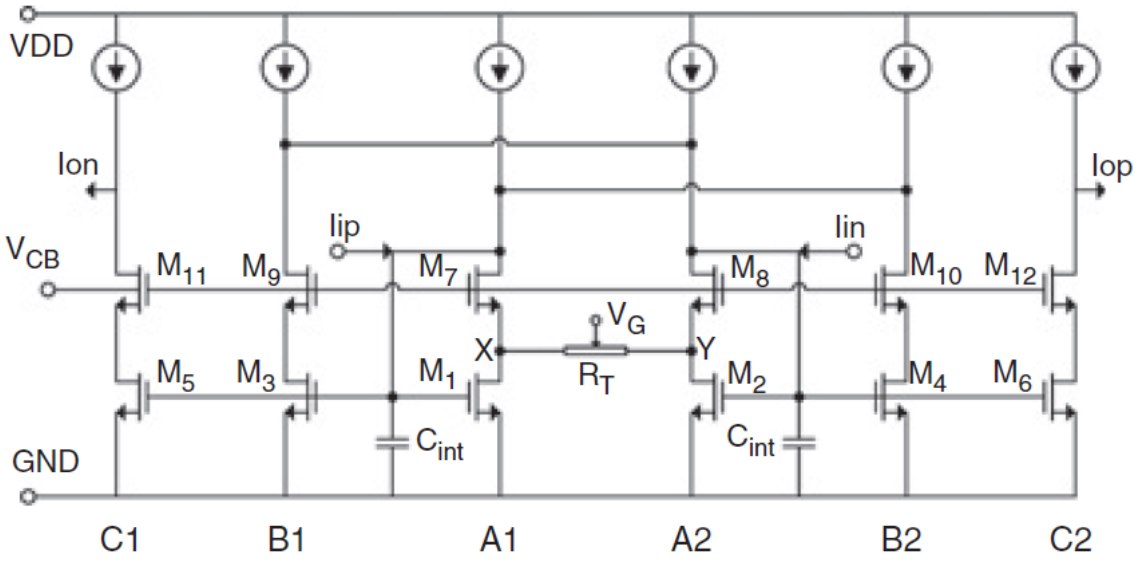

Figure 3.19. Cascode current-mirror based integrator with tunable resistor R_T [10].

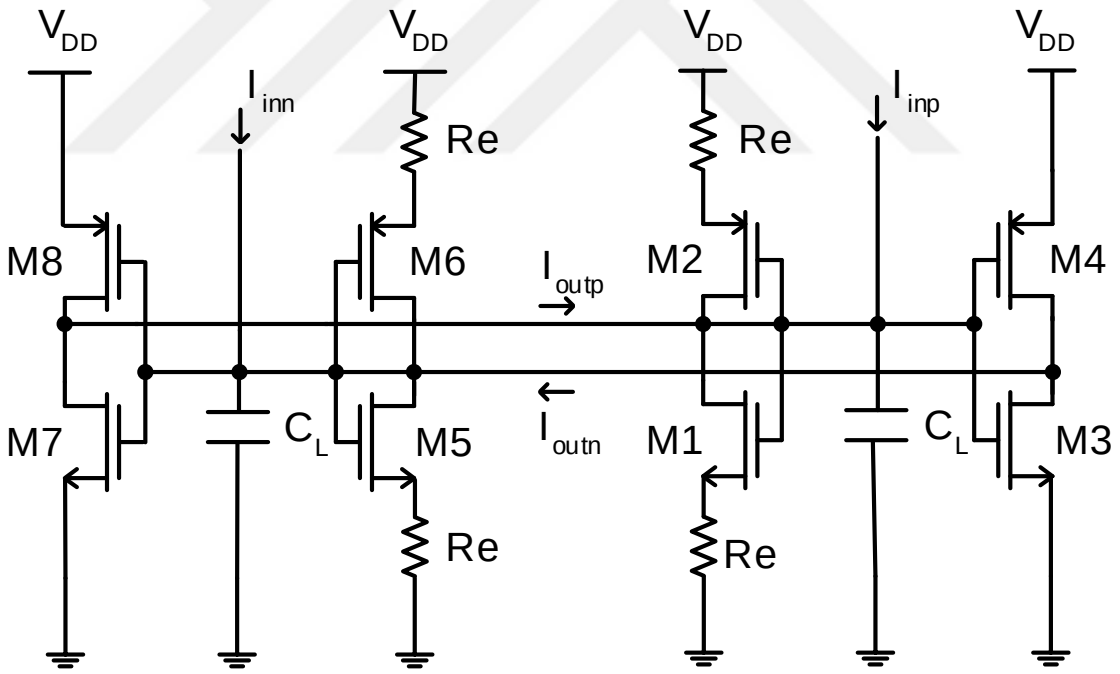

Figure 3.20. Differential integrator with enhancement resistors [11].

The effect of enhancement resistors to the differential current gain can be seen in Figure 3.21. Simulations are made with the same transistor sizes and R_e values are selected to be 500Ω, 750Ω, 1000Ω and 1173Ω. Bigger resistors move the pole to the lower frequencies therefore increase the DC gain of the integrator. Integrator shows

more ideal behavior with these enhancement resistors, therefore A_v is closer to -1V/V. For 500Ω R_e, its exact value is taken from simulations as -0.03246dB with -180° phase which is equal to -0.996V/V which can be seen in Figure 3.22.

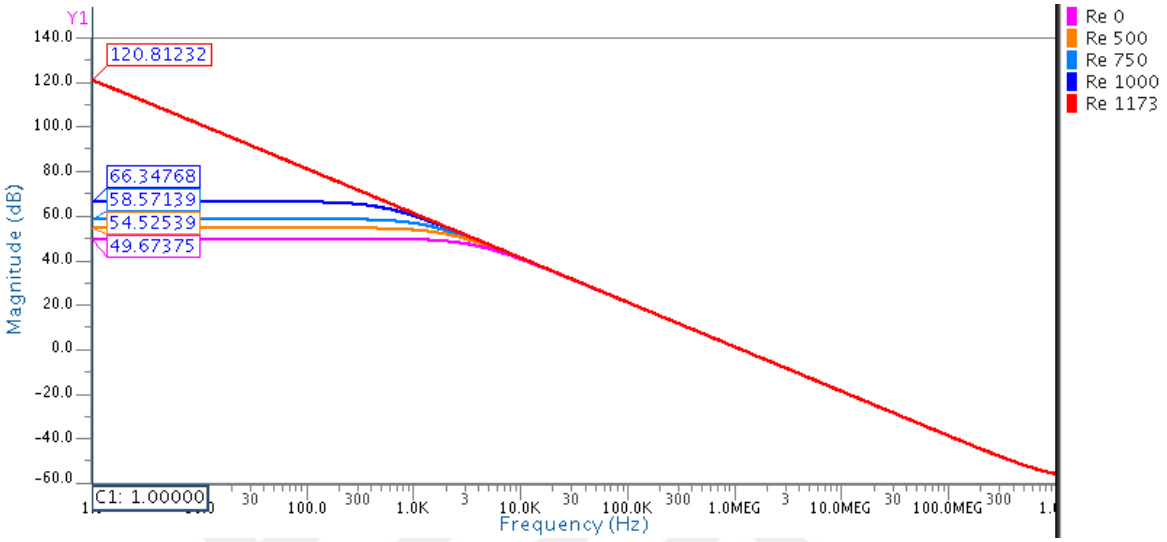

Figure 3.21. Differential current gain for different R_e values.

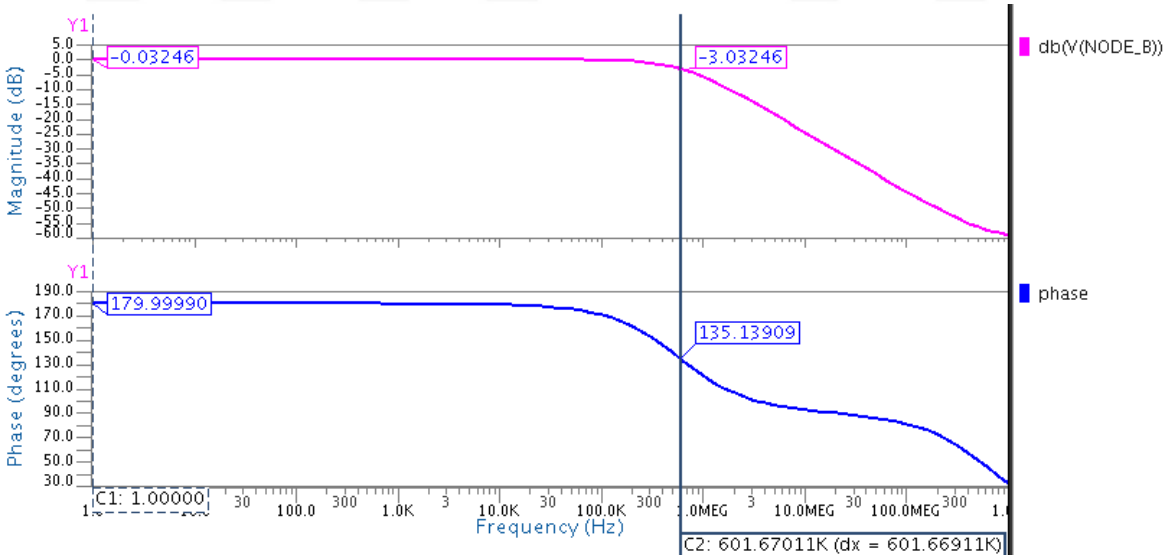

Figure 3.22. AC analysis results for voltage gain A_v with 500Ω R_e.

Resistors R_e are in series with the $1/g_m$ resistors in the T-model of the MOSFET. Because the value of R_e (a few hundred Ω) is very small compared to $1/g_m$ (a few hundred thousand Ω), they can be ignored while calculating the noise. Therefore,

the same equations (3.33 to 3.38) can be used for noise calculation except that A_v is changed to -0.996V/V.

$$\overline{dN_{mid}^2} = 4kT\frac{2}{3}\frac{(g_{m3}+g_{m4}+g_{m5}+g_{m6})}{(g_{m5}+g_{m6})^2}df = 3.56\text{fV}^2/\text{Hz} \tag{3.39}$$

$$\overline{dN_{in}^2} = 4kT\frac{2}{3}\frac{(g_{m1}+g_{m2}+g_{m7}+g_{m8})}{(g_{m1}+g_{m2})^2}df = 3.56\text{fV}^2/\text{Hz} \tag{3.40}$$

Loop gain with enhancement resistors is calculated first.

$$Loop\ Gain = A_{v1}\cdot A_{v2}\cdot\beta = A_v^2\cdot\beta = A_v^2 = (-0.996)^2 = 0.993 \tag{3.41}$$

Closed loop gain from input to output is then calculated.

$$A_{i-o} = \frac{A_v^2}{1-A_v^2} = \frac{0.993}{1-0.993} \approx 133.29V/V \tag{3.42}$$

Closed loop gain from middle node to output is obtained as below.

$$A_{m-o} = \frac{A_v}{1-A_v^2} = \frac{-0.996}{1-0.993} \approx -134.88V/V \tag{3.43}$$

Total voltage noise at the output node is calculated as in Equation 3.44.

$$\begin{aligned}\overline{dv_{out}^2} &= \overline{dN_{in}^2}\cdot A_{i-o}^2 + \overline{dN_{mid}^2}\cdot A_{m-o}^2 \\ &= 3.56\cdot 10^{-15}\cdot 133.29^2 + 3.56\cdot 10^{-15}\cdot(-134.88)^2 \\ &= 128.01\text{pV}^2/\text{Hz}\end{aligned} \tag{3.44}$$

Table 3.4. Comparison of calculation and simulation results for the integrator with enhancement resistors R_e 500Ω for both nodes.

Noise	**Calculation**	**Simulation**
$\overline{dv_{in}^2}$	128.01 pV^2/Hz	125.70 pV^2/Hz
$\overline{dv_{mid}^2}$	128.01 pV^2/Hz	125.70 pV^2/Hz

$\overline{dv_{mid}^2}$ and $\overline{dv_{out}^2}$ are equal because of the symmetric structure of the circuit. Simulation results can be seen in Figure 3.23. Comparison of calculations and simulation results are given in Table 3.4.

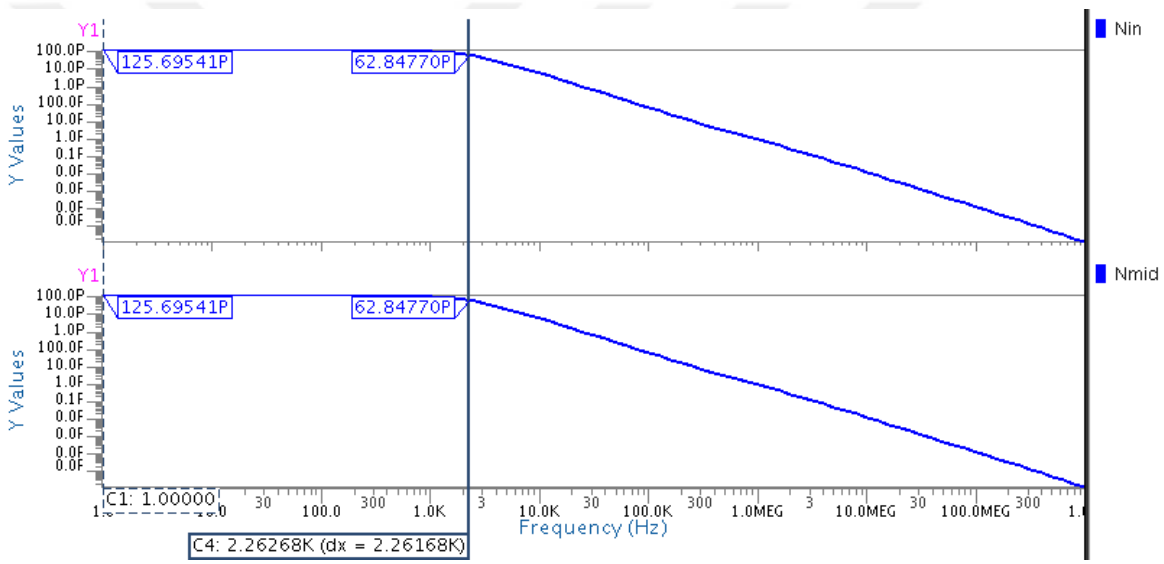

Figure 3.23. Noise simulation results of the integrator with enhancement resistors R_e 500Ω for both nodes.

A theoretical noise analysis for differential current-mode integrators has been performed step-by-step and confirmed with simulations. It can be concluded that the positive feedback in current-mode differential C-g_m integrators cause high noise levels. Furthermore, there is a trade-off between the noise performance and the improved DC-gain of the integrator achieved with enhancement resistors. The results should be considered in the design of current-mode differential integrators.

4. IC DESIGN

A 2nd order continuous-time current-mode differential Σ-Δ modulator is designed using UMC 130nm process technology. The layout is designed and the chip is fabricated. Design considerations of the modulator is presented in this chapter.

Block diagram of the modulator is given in Figure 4.1 [12]. The system has two integrators with integrating coefficients k_1 and k_2 are chosen to be 0.55 to obtain maximum SNR value according to previous studies in the research project [11]. Their inputs and outputs are fully differential currents as presented in the previous chapter and output currents are added via a current adder circuit. This total current is converted to voltage via current-to-voltage gain stage and its output is given to the output through a comparator and a latch circuit. Depending on the digital value of output, feedback current is added to or subtracted from the input via a DAC circuit. In our design, OSR is selected to be 128 for 6.4MHz sampling frequency (f_s) and 25KHz bandwidth according to the formula in Equation 1.1.

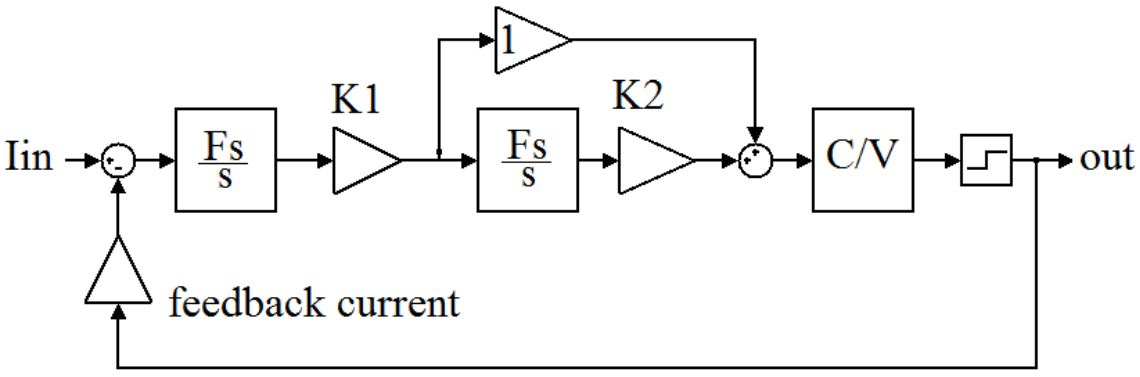

Figure 4.1. Block diagram of current-mode Σ-Δ modulator [12].

4.1. Integrator Circuits

Circuit schematic of the current-mode differential integrator which is used in Σ-Δ modulator is given in Section 3.3. At the system level, the relation between the

integrating coefficient and transfer function of the integrator is in Equation 4.1 [4].

$$H(s) = \frac{kf_s}{s} \tag{4.1}$$

For a proper operation of the modulator, system level transfer function (Eq. 4.1) should be equal to the circuit level transfer function (Eq. 3.19) which yields

$$\begin{aligned} H(s) = \frac{kf_s}{s} &= \frac{g_m}{sC} \\ kf_s &= \frac{g_m}{C} \end{aligned} \tag{4.2}$$

where C is the integrating capacitance and g_m is the equivalent transconductance of MOSFETs.

Circuit schematic of the differential current-mode integrator is given in Figure 4.2. It is the schematic of the first integrator in the modulator. The output stages of the integrator which are formed by M_9, M_{10} and M_{11}, M_{12} transistor pairs are used to feed the inputs of the second integrator. Because the second integrator does not drive any other stages, it dose not have output stages as in Figure 3.16 [4].

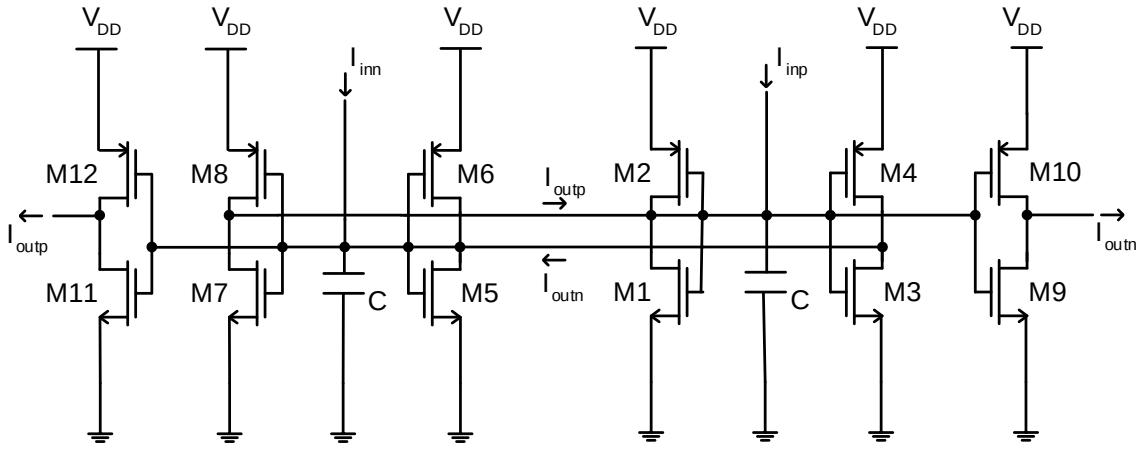

Figure 4.2. Circuit schematic of the first integrator.

In the circuit level design, firstly g_m values of NMOS and PMOS transistors should be matched in order to get a linear operation. Width (W) and channel length

(L) values of transistors can be set by parameters in order to change easily in SPICE. In order to keep power consumption of the modulator low, drain currents of transistors are aimed to be around hundred nanoamperes where the value of V_{DD} is selected 0.75V. In this purpose, dimensions of MOSFETs are arranged such that $(\frac{W}{L})_p = \frac{1.4\mu}{5.35\mu}$, $(\frac{W}{L})_n = \frac{0.3\mu}{5.75\mu}$, so all g_m values are equal to 3.10μS.

After determining the equivalent g_m value of the integrator, integrating capacitance value should be chosen for $k = 0.55$ and $f_s = 6.4$MHz. C value should be chosen such that the differential gain of the integrator at the sampling frequency is $\frac{k}{2\pi}$ (Because the unit of s in Equation 4.2 is rad/s). Ignoring the gate capacitances of MOSFETs, C value is calculated as 1.76pF according to the formula in Equation 4.2. However, the real value of the integrating capacitance is chosen through simulations. The capacitance is set to 1.5pF after making sweep analysis for C value around 1.76pF. AC analysis results for 1.5pF integrating capacitance can be seen in Figure 4.3.

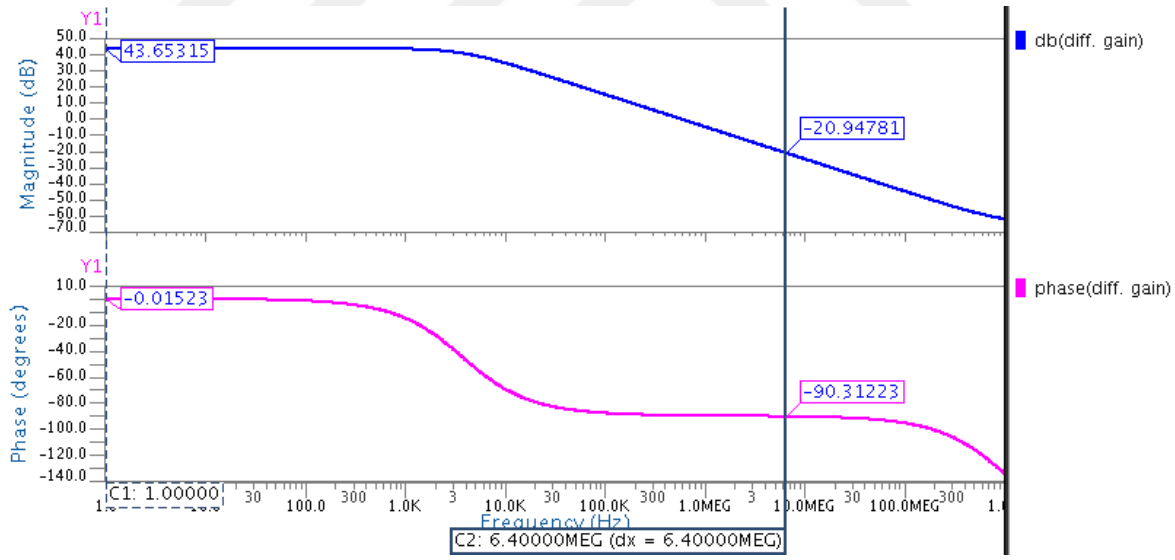

Figure 4.3. Simulation results for differential gain of integrator.

Layout designs of integrators can be seen in Figures 4.4 and 4.5. Layouts are designed to be symmetric as possible in order to reduce the DC offset and harmonic effects. Integrating capacitors are not shown here, they can be seen in the layout of the whole circuit in next sections. Post-layout simulation results of the integrators for 7KHz sinusoidal differential 90nA input current is given in Figure 4.6. When the

feedback loop is closed, kickback noise occurs in the input currents of the integrators as seen in the first and third graphs. This kickback noise does not create an important problem because it occurs in both differential nodes. Taking difference of the differential signals eliminates the glitches. In the second and fourth graphs, voltage variations at the input nodes of integrators is seen.

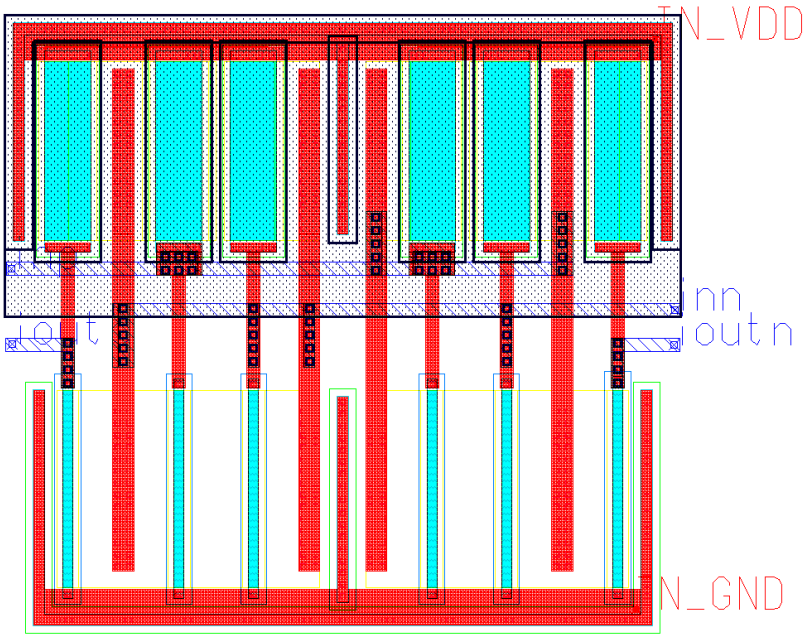

Figure 4.4. Layout of the first integrator.

4.2. Current Adder

Output currents of the integrators are added via a current adder circuitry. Schematic of the circuit can be seen in Figure 4.7. Working principle of this circuit is similar to the inverter type single-ended integrator in Figure 3.4. The difference is that the input current fills C_{GS} capacitors of MOSFETs instead of a big integrating capacitance. The capacitors at the gate of the MOSFETs are filled with input currents and create an AC voltage V_{GS}. Due to the transconductance of MOSFETs, that V_{GS} voltage turns into current at the output of the current adder circuit. Here, g_m values of PMOS and NMOS transistors should be equal as possible in order to get a linear operation similar to single-ended inverter type integrator circuit.

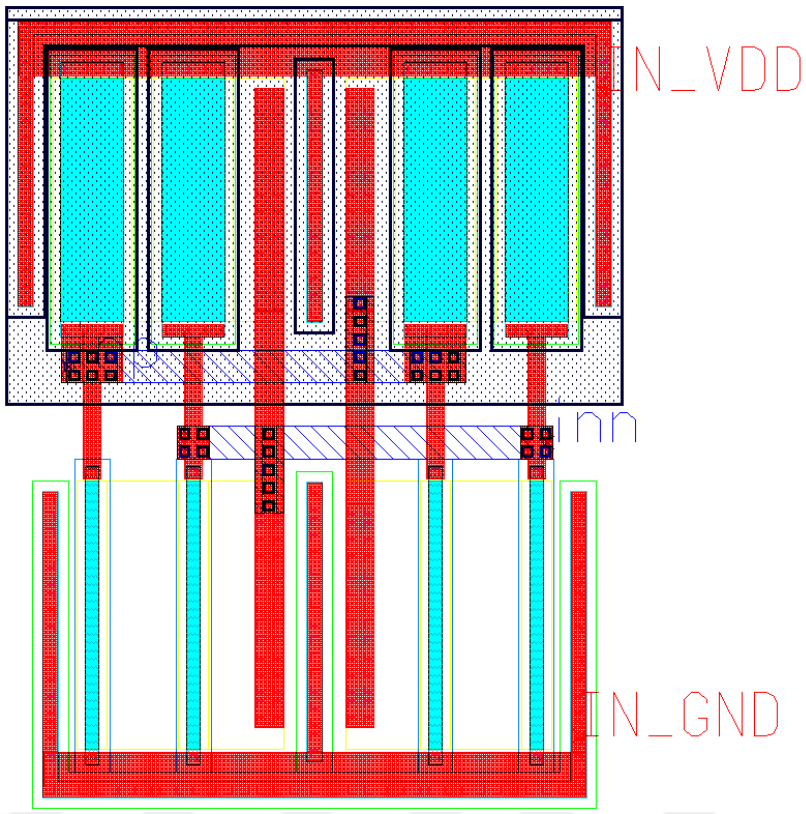

Figure 4.5. Layout of the second integrator.

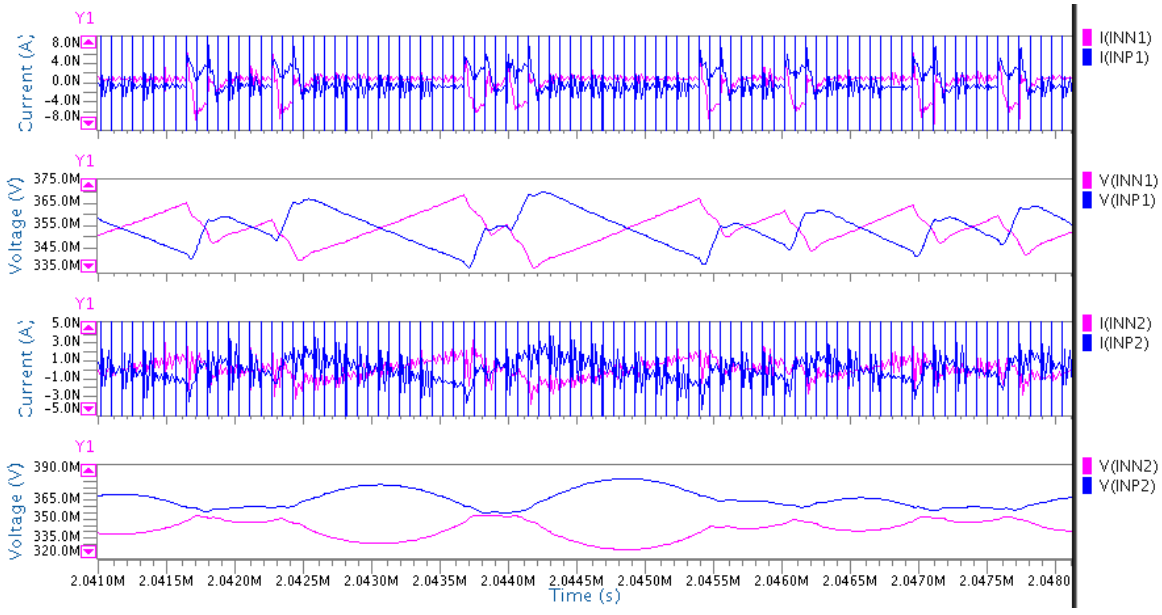

Figure 4.6. Voltage and current variations at the input nodes of integrators.

Transient analysis results of input and output currents of current adder circuit are seen in Figure 4.9. It can be observed that output currents are proportional with

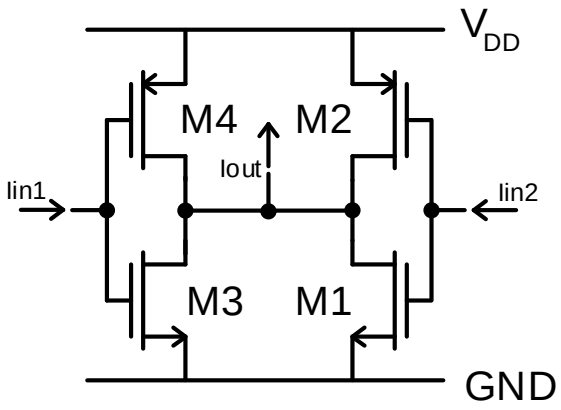

Figure 4.7. Schematic of current adder circuit.

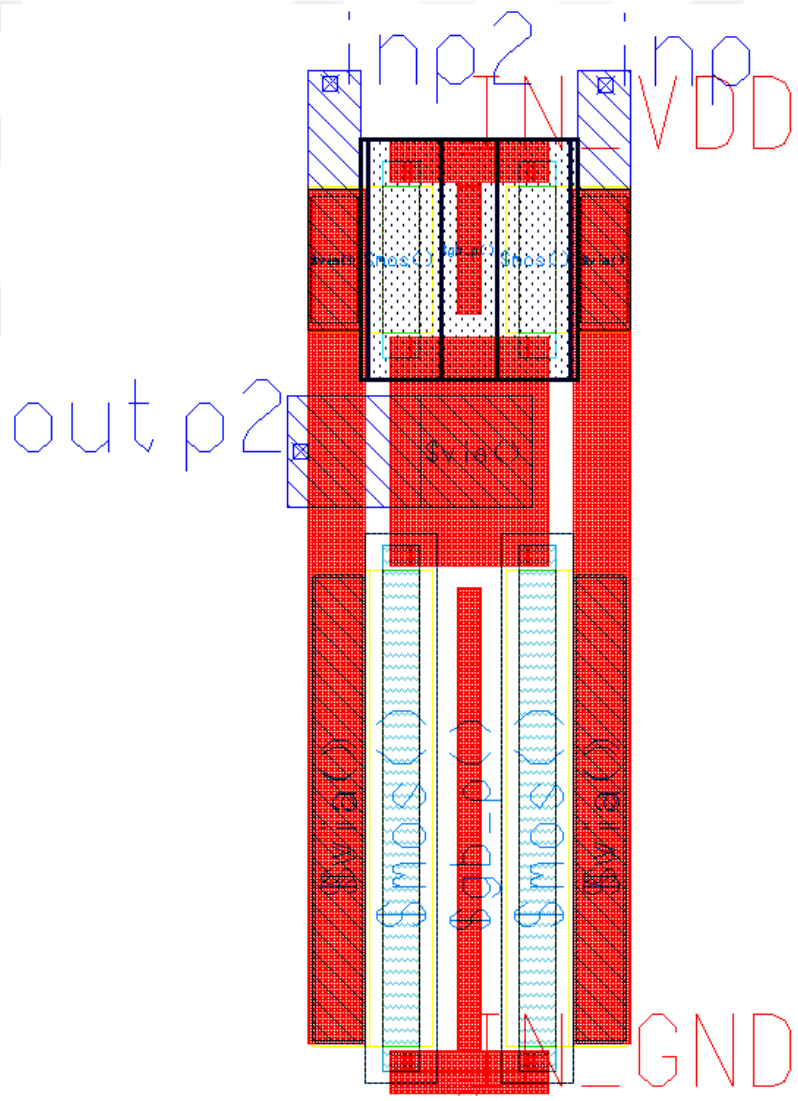

Figure 4.8. Layout of current adder circuit.

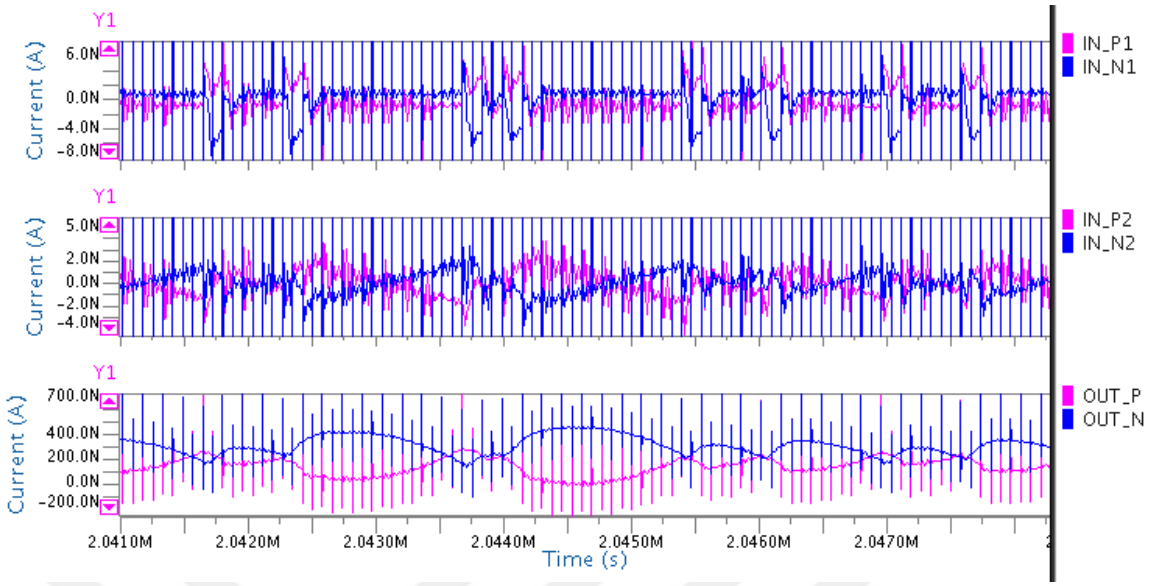

Figure 4.9. Current variations on inputs and outputs of current adder circuit.

input currents. Furthermore, with the help of g_m of the circuit, the difference between differential outputs becomes more distinct when the difference between differential input current values is bigger. The effect of kickback noise can be observed because the loop of Σ-Δ modulator is closed.

4.3. Gain Stage

Differential output currents of current adder circuit should be compared with each other in order for Σ-Δ modulator to give digital outputs. A current-to-voltage converter and a voltage comparator are used as current comparator in this study. Small differences of input current values should be detected sensitively in a Σ-Δ modulator. Current-to-voltage conversion is quite important in this purpose.

Schematic of the gain stage circuit used in current-to-voltage conversion can be seen in 4.10 [13]. There is a source follower structure as input stage, therefore the input resistance is approximately $1/g_m$ where the transistors have the same transconductance value g_m. Applying feedback to the gates is another advantage of using source followers as input stage. CMOS inverter provides a positive feedback such that small voltage variations are amplified to high levels and the voltage difference between input and

output nodes is distinct.

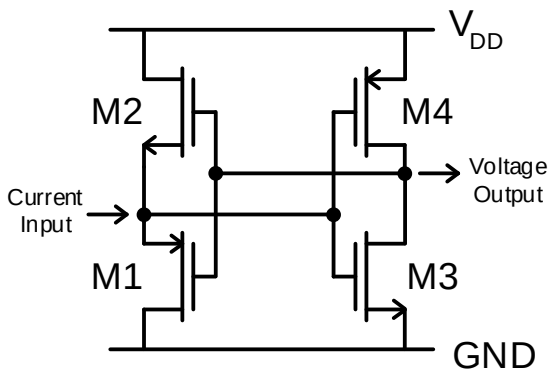

Figure 4.10. Schematic of gain stage circuit [13].

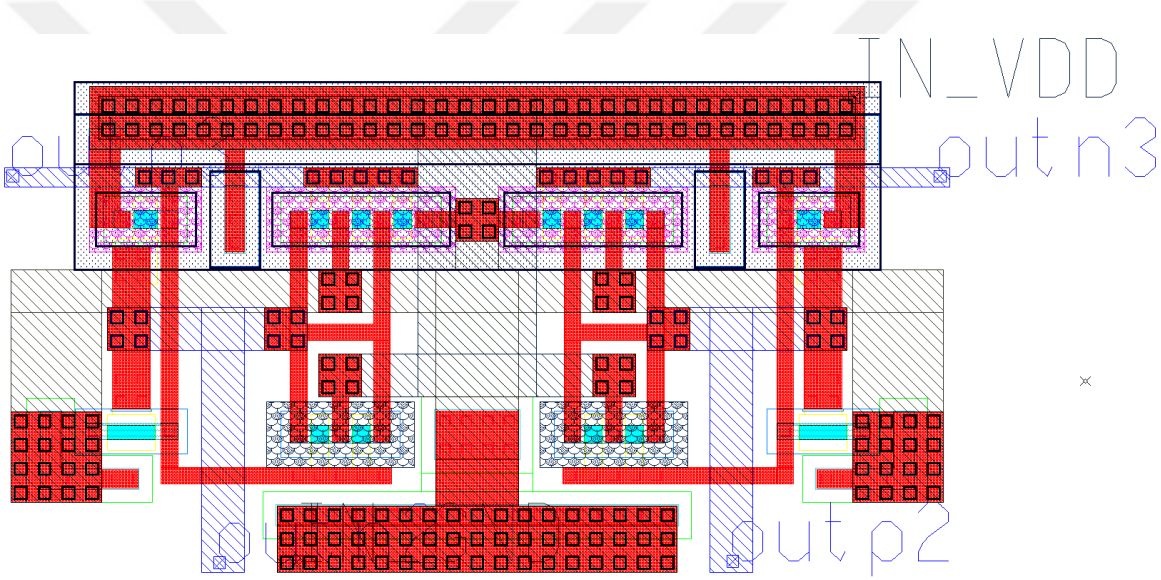

Figure 4.11. Layout of gain stage circuit.

Transient analysis results for input and output voltages of gain stage circuit with the layout as in Figure 4.11 can be seen in Figure 4.12. Input current variations are given as output currents of current adder circuit in Figure 4.9. It is observed that the small difference at the input currents creates high voltages at the output thanks to the low input and high output resistances of the structure.

4.4. Comparator and Latch

The last step of current-mode Σ-Δ analog-to-digital conversion is digitizing the output voltages of the current-to-voltage gain stage. Since the design in this study

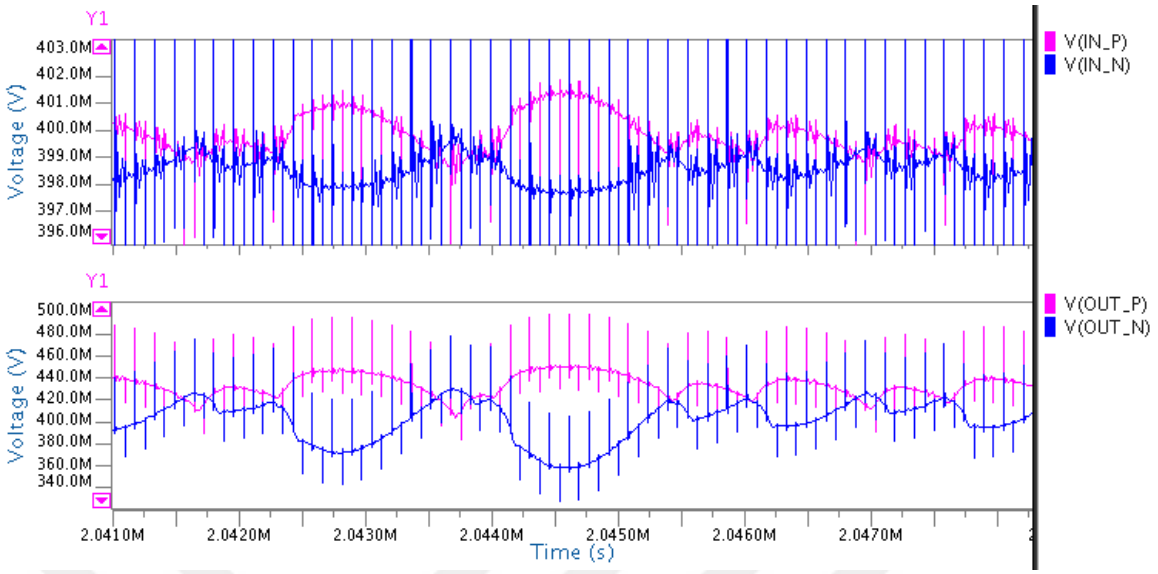

Figure 4.12. Voltage variations for input and output of gain stage.

has one bit digital output, a one-bit quantizer is used. It is composed of a dynamic comparator and an SR latch circuit as shown in Figure 4.13 [14, 15]. Here, $C1$ is the clock signal which has 6.4MHz sampling frequency with 1.2V voltage value. When the clock signal is digitally low, both P and Q are pulled to V_{DD} value. While the clock signal $C1$ becomes high, the voltages of P and Q nodes tend to drop with different rates depend on the input voltages. Cross-coupled inverters help to keep voltages apart from each other. The duty of the SR latch is keeping output values constant until the next clock signal comes.

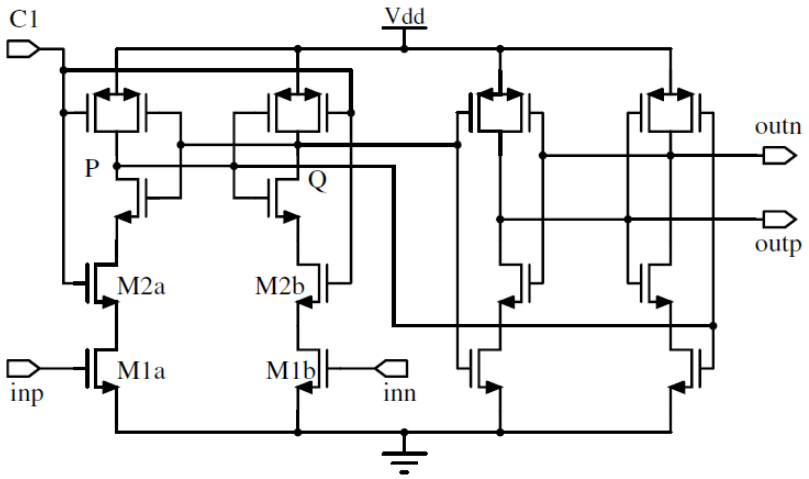

Figure 4.13. Schematic of the comparator and the latch circuit [14].

Because this is a digital circuit, V_{DD} value is selected as 1.2V for proper and faster operation in UMC 130nm process technology. V_{DD} of the digital parts can be seen in layouts as VDD_high. Design of the layout should be quite symmetric as in Figure 4.14. Errors at the output bit due to the input referred offset can be minimized in this way. In order to get output from the chip via the oscilloscope, a buffer big enough to drive the probe is needed. A buffer circuit is designed such that two inverters are cascaded as in Figure 4.15. The first inverter is designed bigger than the output stage of the latch circuit and the size of the second inverter is double the first one for better logical effort [16].

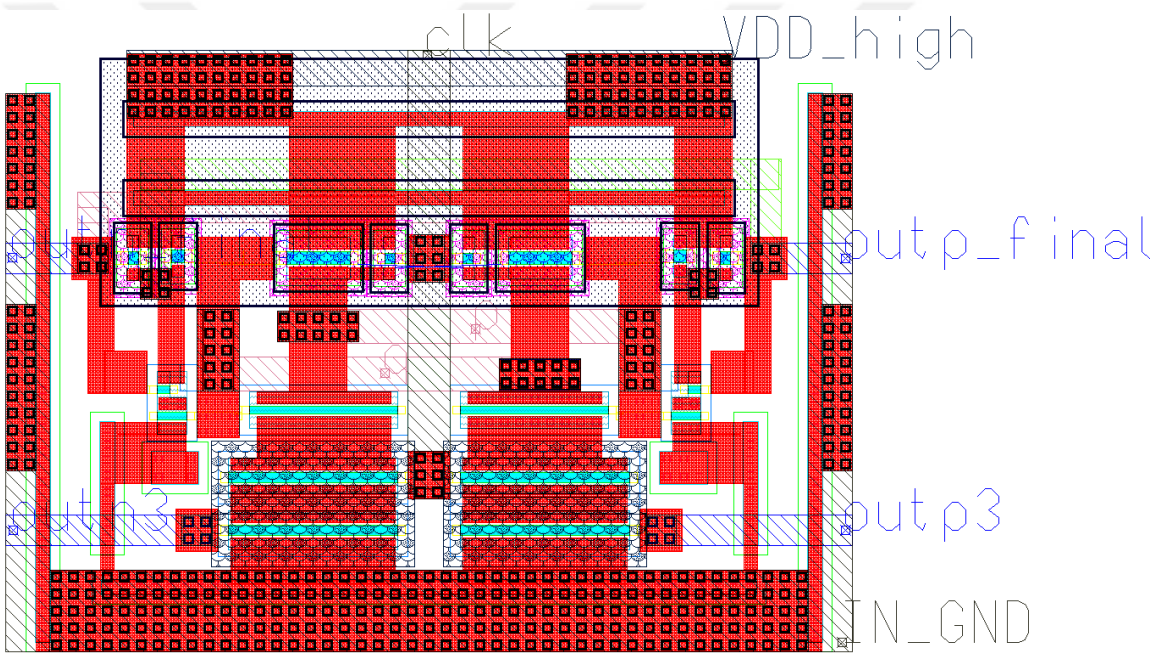

Figure 4.14. Layout of the comparator and the latch circuit.

Figure 4.16 shows transient analysis results of the latch circuit. $V(OUT_P)$ and $V(OUT_N)$ are differential input voltages of the comparator circuit. The output of the latch circuit is $V(OUT_P_LATCH)$ and the output of the buffer stage is $V(OUT_FINAL)$. It can be observed that when the P node has a larger voltage value than the N node, positive output of the latch gives logical high value. Another effect of the buffer stage is getting rid of the kickback noise seen as glitches in the third waveform.

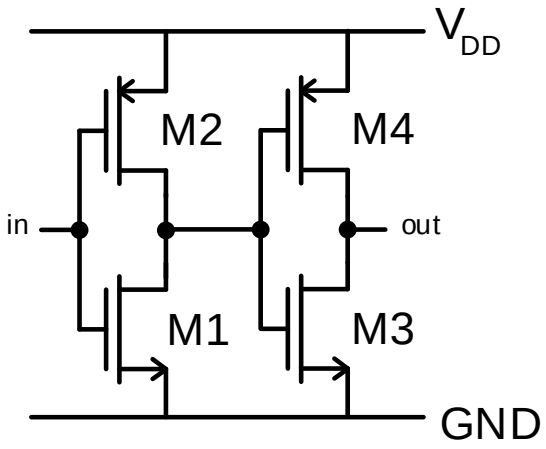

Figure 4.15. Schematic of the buffer circuit.

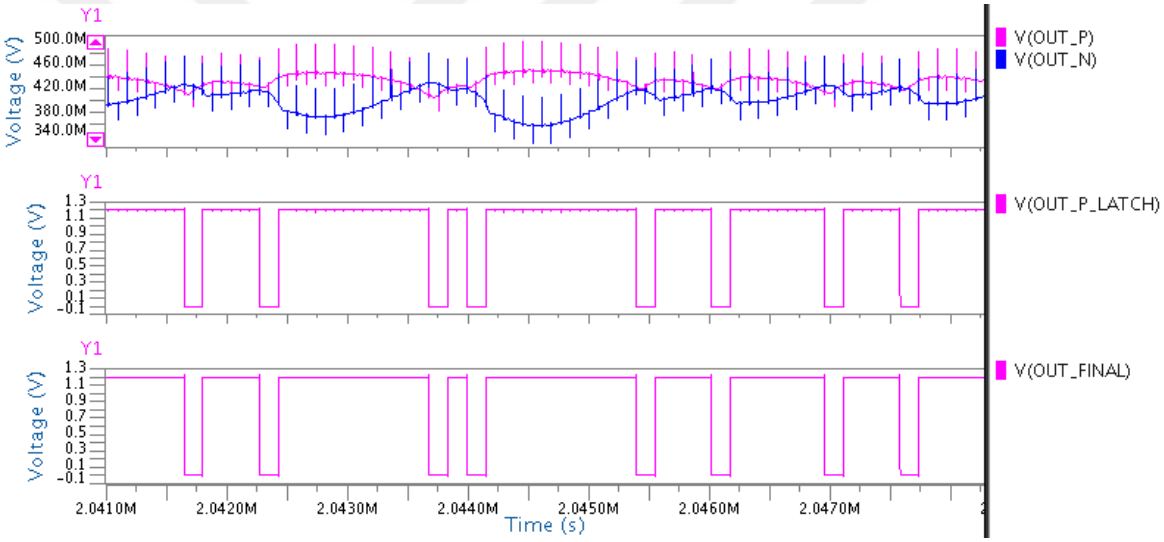

Figure 4.16. Simulation results for inputs and outputs of the latch circuit.

4.5. Current Feedback DAC

Input of the first integrator of Sigma-Delta ADC is the difference between the input current and the feedback current as shown in Figure 4.1. According to the digital value of the output bit, the feedback current is added to or subtracted from the input current. Schematic of the DAC circuit is on Figure 4.17 [4,11]. R_{bias} resistor between the drains of diode connected MOSFETs $M1$ and $M2$ determines the value of bias current (I_{bias}). Value of the R_{bias} resistance is selected in the Megaohms range in order to keep the bias current in Nanoamperes range. Bias current determines the

range of input signal value and the power consumption of the DAC circuit. I_{bias} is mirrored with the same sized PMOS ($M2$, $M9$ and $M10$) and NMOS ($M1$, $M3$ and $M4$) transistors. When the positive output of the latch circuit is digital high, $M8$ turns off, $M7$ turns on and the total current of $M9$ and $M10$ flows through the branch of $M7$ and $M5$. Since $M3$ and $M4$ are biased with the same V_{GS} value with $M1$, I_{bias} flows on both of them. Therefore, $2I_{bias}$ coming from the branch of $M7$ and $M5$ is divided into I_{inn} and I_{M3} equally as I_{bias}. The opposite happens when OUT_N is high and OUT_P is low.

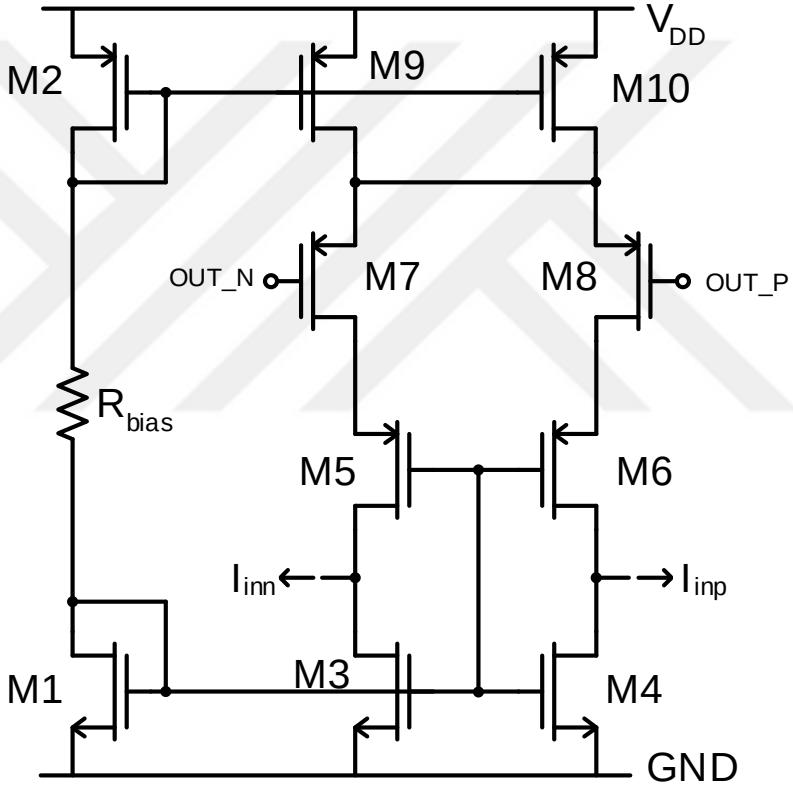

Figure 4.17. Schematic of current feedback DAC circuit [4, 11].

Simulation results of feedback DAC circuit is seen in Figure 4.19. When the positive output of the latch circuit $V(OUT_P_LATCH)$ is digital high, feedback current is subtracted from P input $I(FB_P)$ and added to N input $I(FB_N)$. Value of the feedback current is close to 130nA because the circuit is designed for bias current to be 130nA.

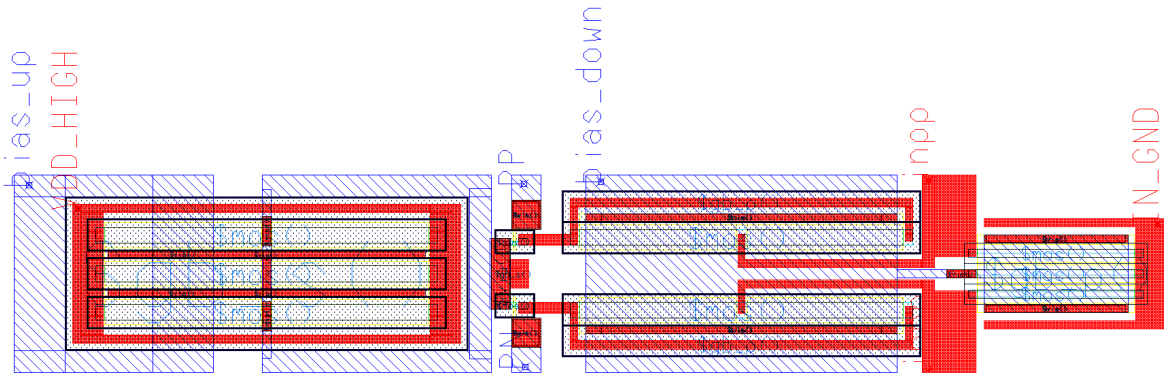

Figure 4.18. Layout of current feedback DAC circuit.

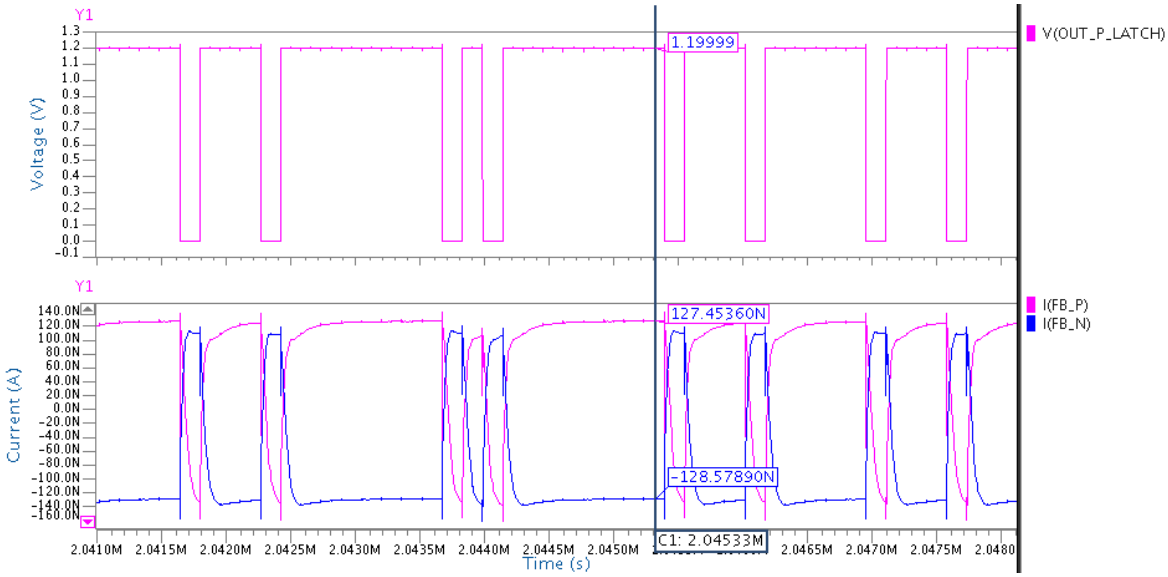

Figure 4.19. Simulation results of current feedback DAC circuit.

5. RESULTS

Post-layout simulation results of the current-mode continuous time Sigma-Delta modulator and measurement results of the produced chip are discussed in this chapter.

5.1. Post-Layout Simulation Results

Layouts of the components of the current-mode continuous time Sigma-Delta modulator are presented in Chapter 4 separately. The whole layout of the circuit including the bias resistor and integrating capacitors in UMC 130nm technology can be seen in Figure 5.1. Dimensions of the layout are 135μm x 175μm, where more than half of the area consists of capacitors and resistors. In order to minimize distortions stemming from the production of the chip, layouts of the components should be designed in common-centroid structure (especially integrators for improving g_m matching) [4, 17]. Allowable area for the circuit is limited because there are other types of Sigma-Delta converter circuits in the tape-out with 1.5mm x 1.5mm dimensions for the same research project as shown in the next section. Therefore, the layout is designed as symmetric as possible with respect to vertical axis in order to avoid production distortions and minimize input referred offset.

After the layout is completed and SPICE parameters are extracted, transient analysis simulations are performed on ELDO of MENTOR Graphics. V_{DD} of analog components are set to be 0.75V and digital ones including the clock signal have 1.2V as V_{DD}_high. Differential and sinusoidal input currents have 90nA amplitudes and 7KHz frequency while the sampling frequency f_s is 6.4MHz. Differential input signals and output of the Σ-Δ modulator for some time interval can be seen in Figure 5.2. It is observed that the frequency of logic high values at the output is high while the input current difference $I(INP)$ - $I(INN)$ difference is high, and vice versa.

In order to examine the SNR and harmonic effects of the Σ-Δ modulator, Fast Fourier Transform (FFT) algorithm is used. The more data points taken from the

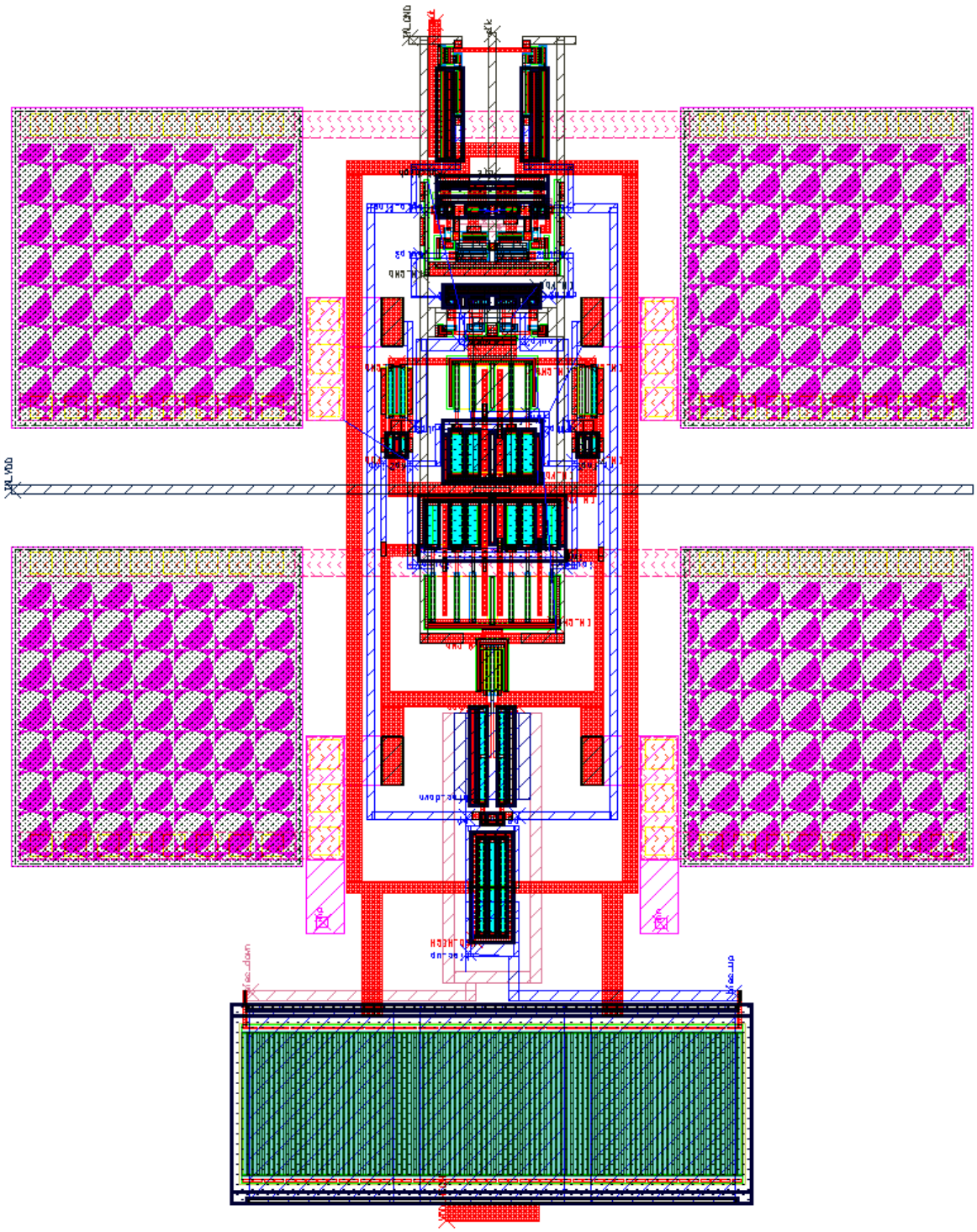

Figure 5.1. Layout of the current-mode continuous time Sigma-Delta modulator.

transient analysis, the more accurate FFT graph is acquired. 65536 data points is taken in approximately 11ms time interval for 6.4MHz sampling frequency. FFT and SNR calculations are made using MATLAB for 25KHz bandwidth. In Mentor Graphics

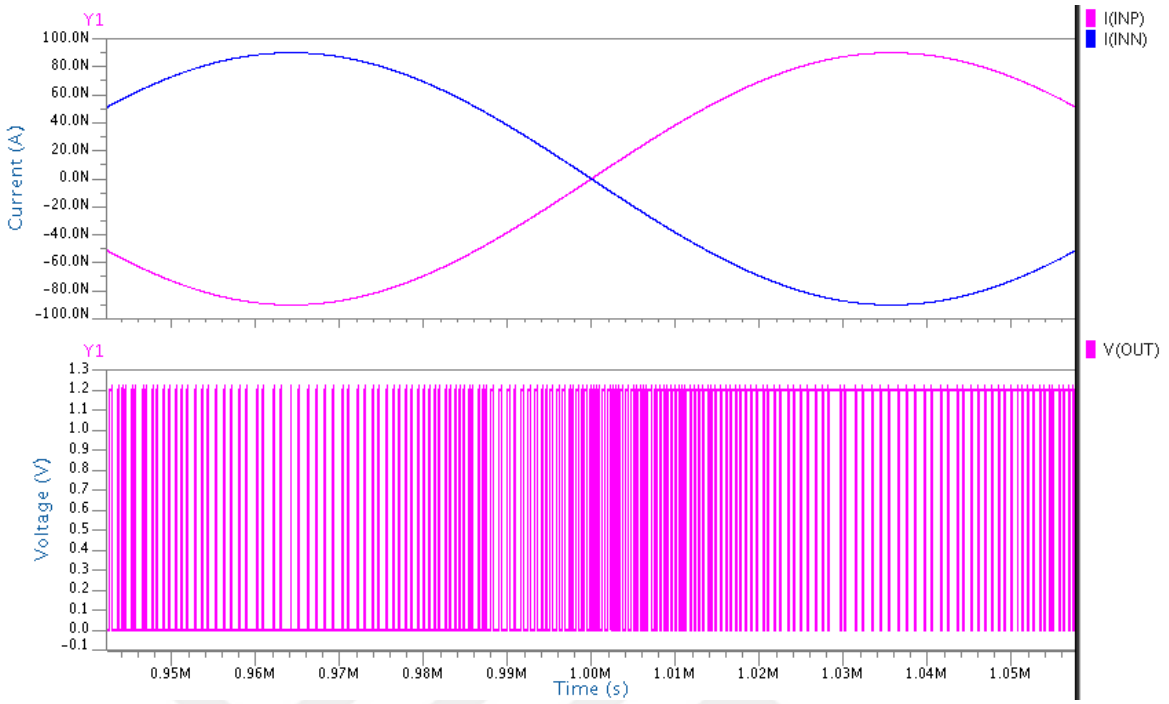

Figure 5.2. Differential input signals and output of the Sigma-Delta modulator.

ELDO software, simulations can be performed including or excluding the transient noise effects of active devices. Figures 5.3 and 5.4 show FFT results for pre-layout simulations of the Sigma-Delta modulator without the noise effects and including the transient noise respectively. Post-layout FFT results of simulations are in Figures 5.5 and 5.6. In order to see the noise effects on FFT clearly, post-layout simulation results on Figures 5.5 and 5.6 are superposed on Figure 5.7.

Comparing the FFT results with and without layout effects, SNR values are quite similar. However, including noise effects of the active devices decrease SNR around 8dB in both pre-layout and post-layout simulations. Furthermore, the third harmonic observed in the pre-layout simulations does not appear in the post-layout simulations. Shaping of the quantization noise in the post-layout simulations is closer to an ideal second order system (40db/decade slope).

SNR of designed continuous time current-mode Sigma-Delta modulator including the noise effects and layout parasitics is 60.4dB which corresponds to 9.74 ENOB according to formula in Equation 1.6. There are two power supplies for analog and

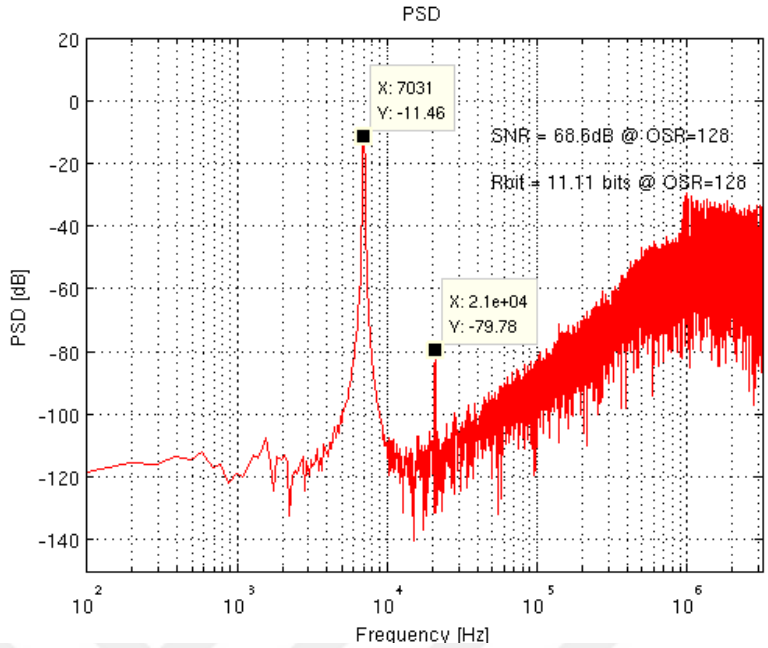

Figure 5.3. FFT of the pre-layout simulation results of the Sigma-Delta modulator without noise effects.

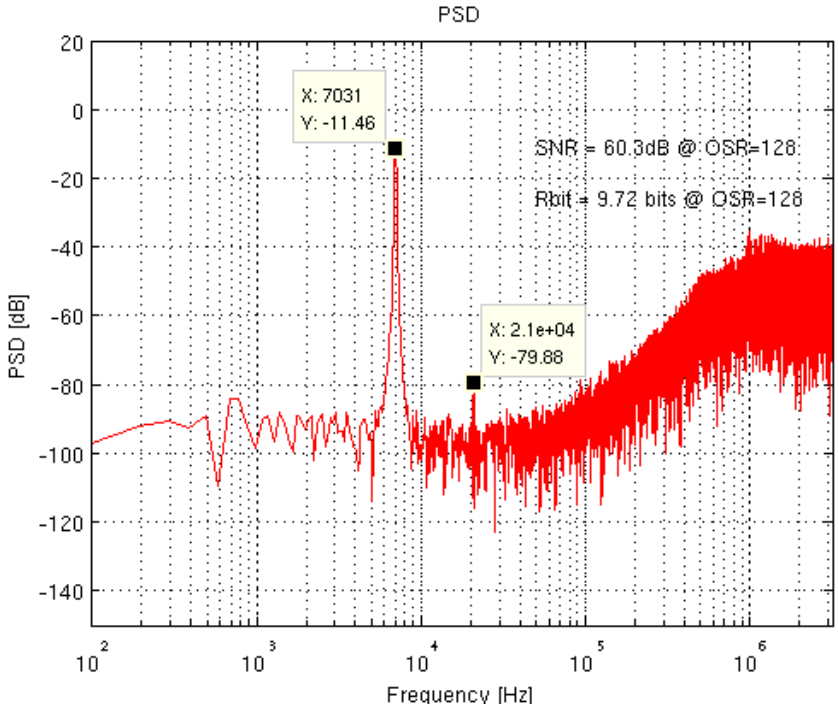

Figure 5.4. FFT of the pre-layout simulation results of the Sigma-Delta modulator with transient noise.

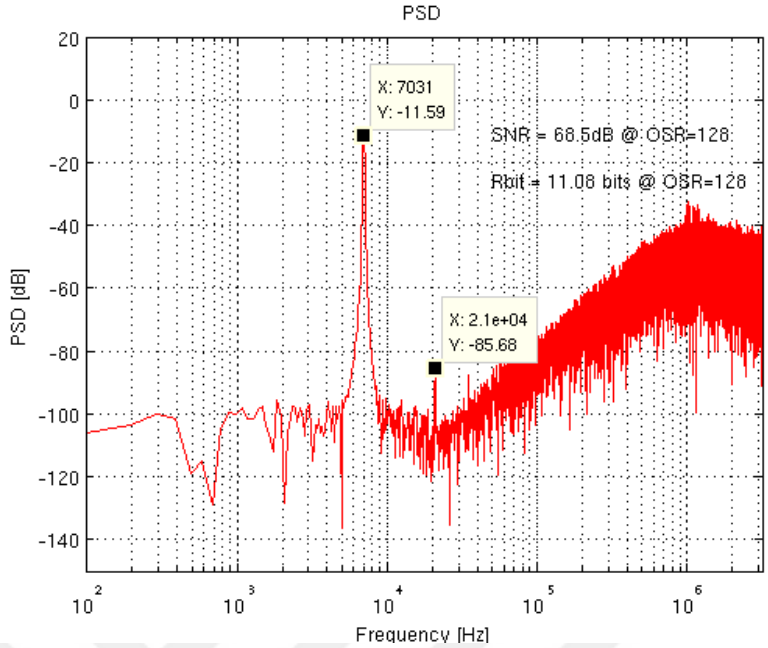

Figure 5.5. FFT of the post-layout simulation results of the Sigma-Delta modulator without noise effects.

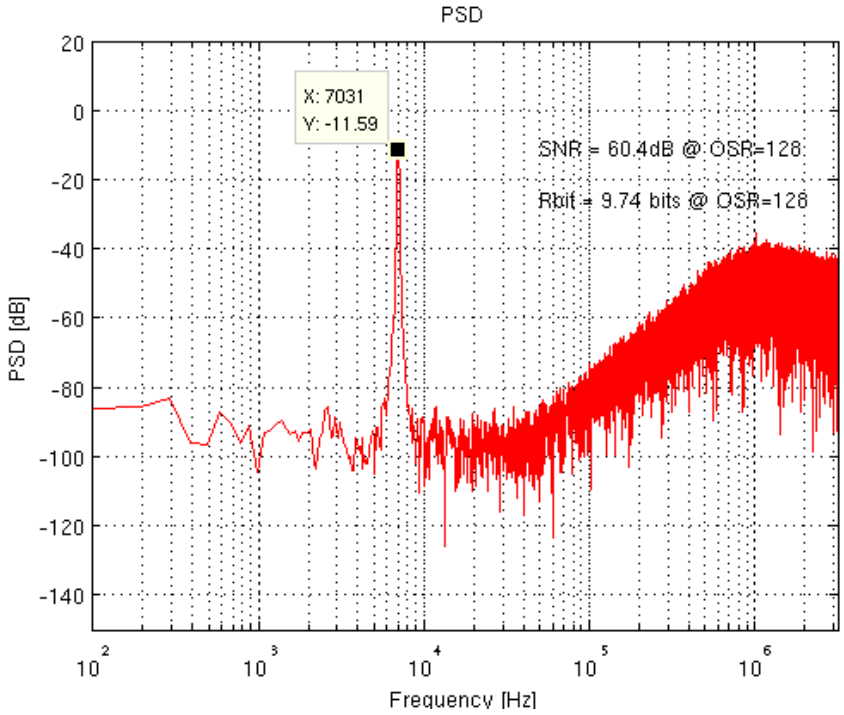

Figure 5.6. FFT of the post-layout simulation results of the Sigma-Delta modulator with transient noise.

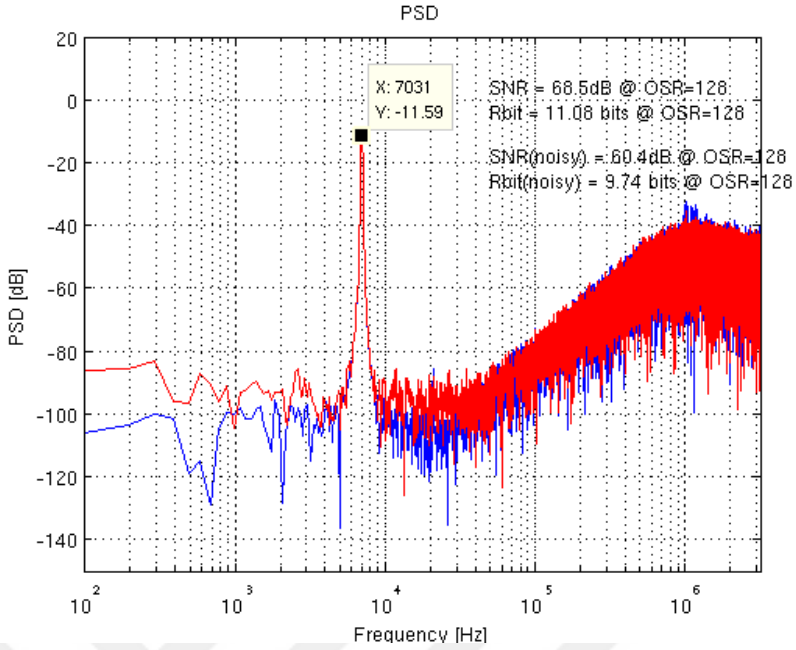

Figure 5.7. FFT of the post-layout simulation results of the Sigma-Delta modulator with and without noise effects.

digital parts of the circuit separately, therefore total power consumption is sum of powers of two sources. Figure 5.8 shows the average current sunk by two power supplies. Total power consumption is calculated below.

$$\begin{aligned} P_{tot} &= V_{DD} \cdot I_{avgVdd} + V_{DDhigh} \cdot I_{avgVddhigh} \\ &= 0.75 \cdot 8.865 \cdot 10^{-6} + 1.2 \cdot 3.795 \cdot 10^{-6} = 11.203\mu\text{W} \end{aligned} \tag{5.1}$$

Figure of merit(FoM) of the continuous time current-mode Sigma-Delta modulator designed in UMC 130nm technology is calculated according to Equation 1.7 as below.

$$FoM = \frac{11.203\mu\text{W}}{2^{9.74} \cdot 2 \cdot 25\text{KHz}} = 262\text{fJ/conversion} \tag{5.2}$$

One objective of this thesis is comparing the results of similar designs in different process technologies. FFT results of the continuous time current-mode Sigma-Delta

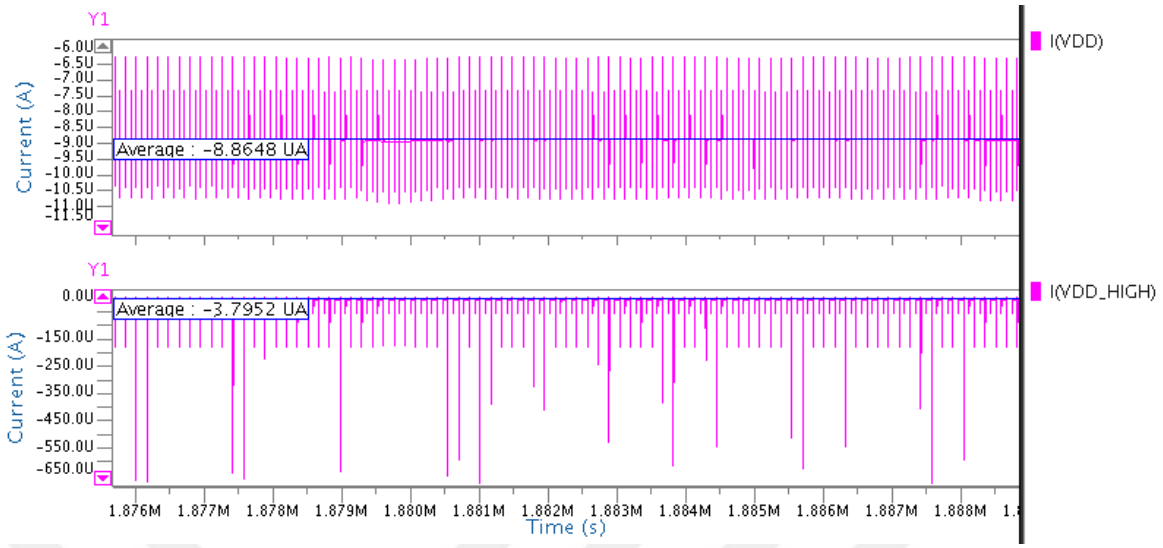

Figure 5.8. Average current values of two power supplies for the design in UMC 130nm.

modulator produced in the previous tape-out with UMC 180nm technology with same input signal, f_s, OSR and BW is in Figure 5.9 [11]. SNR value is 55.9dB and ENOB is 8.99 as calculated with MATLAB.

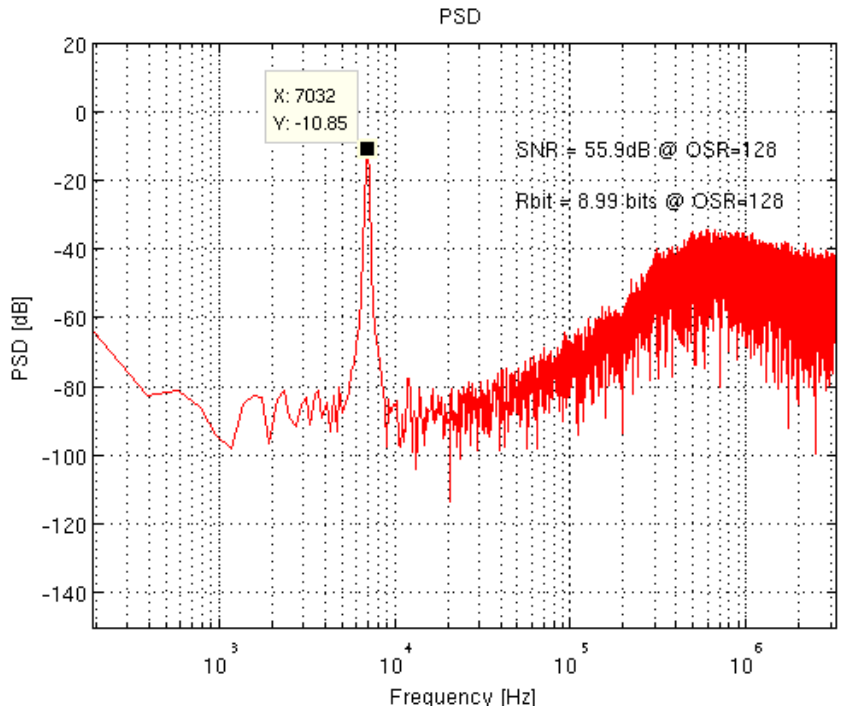

Figure 5.9. FFT of the Sigma-Delta modulator designed in UMC 180nm with noise effects.

V_{DD} for analog parts of the modulator in UMC 180nm is 0.8V. According to the average current values of the V_{DD} and V_{DDhigh} sources as in Figure 5.10, power consumption is calculated as in Equation 5.3.

$$\begin{aligned} P_{tot} &= V_{DD} \cdot I_{avgVdd} + V_{DDhigh} \cdot I_{avgVddhigh} \\ &= 0.8 \cdot 6.446 \cdot 10^{-6} + 1.2 \cdot 3.124 \cdot 10^{-6} = 8.906\mu\text{W} \end{aligned} \tag{5.3}$$

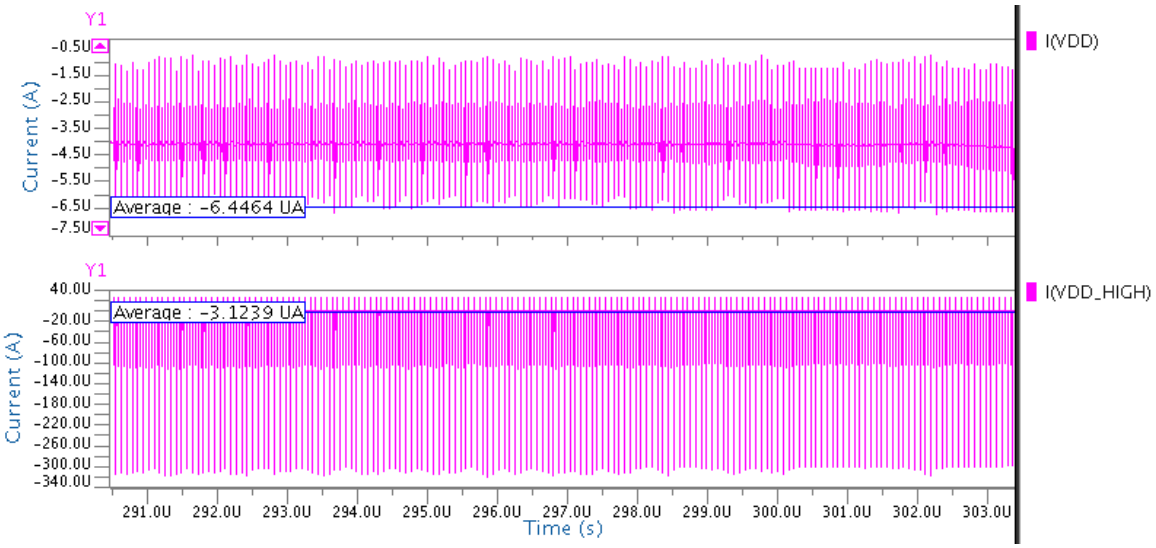

Figure 5.10. Average current values of two power supplies for the design in UMC 180nm.

FoM value of the design in UMC 180nm process is as in Equation 5.4.

$$FoM = \frac{8.906\mu\text{W}}{2^{8.99} \cdot 2 \cdot 25\text{KHz}} = 350\text{fJ/conversion} \tag{5.4}$$

Comparison of the design in this study using UMC 130nm technology, the previous one using UMC 180nm technology and other Sigma-Delta ADCs in the literature with similar technology and signal bandwidth is given in Table 5.1. Even the design in this study has higher Figure of Merit, power consumption is quite low with respect to other designs in the literature. The reason of high FoM is high noise level caused by the positive feedback effect of the differential current-mode integrators as presented in Chapter 3.

Table 5.1. Comparison of designs in this study with the literature.

Σ-Δ ADC	**Technology**	**Type**	**BW**	**OSR**	**Power**	**SNR**	**FoM**
This study	130nm	CT	25KHz	128	11.2μW	60.4dB	262fJ/conv.
Previous study	180nm	CT	25KHz	128	8.9μW	55.9dB	350fJ/conv.
[18]	180nm	CT	24KHz	64	90μW	92.5dB	54fJ/conv.
[19]	90nm	VCO	20KHz	85	0.44μW	47.4dB	57fJ/conv.
[20]	130nm	DT	20KHz	48	34μW	81dB	92fJ/conv.
[21]	130nm	CT	20KHz	64	28.6μW	80.1dB	97fJ/conv.
[22]	180nm	DT	20KHz	100	860μW	84dB	1.66pJ/conv.

5.2. IC Measurement Results

Layout of the designed continuous time current-mode Sigma-Delta ADC is produced in UMC 130nm process technology with the other ADCs in the same tape-out within the same research project. Layout of the whole IC is seen in Figure 5.11. 2nd order CT current-mode Σ-Δ ADC shown in Figure 5.1 is enclosed by a blue rectangle. Other designs are 3-bit feed-forward 2nd order Σ-Δ ADC, 2-1 MASH Σ-Δ ADC, hybrid ADCs (on the same layout with different opamps), 3-bit feed-forward 2nd order Σ-Δ ADC (with different coefficients than the top left design) and 2nd order feed-forward Σ-Δ ADC in clockwise order.

The test PCBs designed for all circuits in the produced IC can be seen in Figure 5.12. Banana plugs are used for connecting power supplies while SMA sockets are used for clock and signal connections. Microfarad scale capacitors are connected between the supply nodes and ground in order to minimize the noise effects coming from the power supply devices. Because the lack of the current signal generator in laboratory, tests of current-mode circuit is performed disconnecting the inputs. Noise level of the circuit can be observed in this way. Voltage signal generators in the laboratory does not generate differential signals, therefore tests of the voltage-mode circuits are performed connecting one input to common-mode DC value and AC voltage signal to other one. Laboratory environment during the tests of ICs can be seen in Figure 5.13.

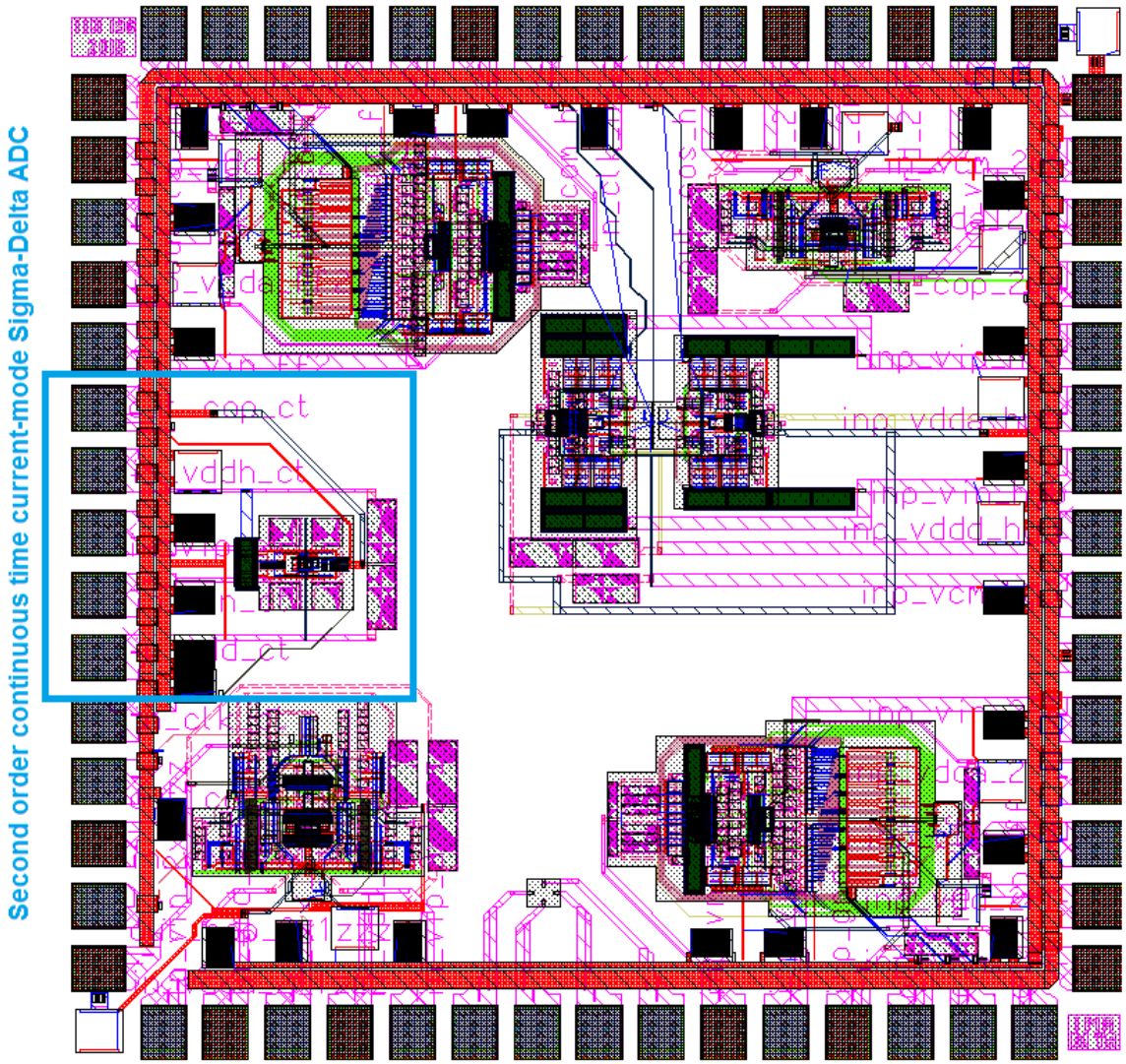

Figure 5.11. Layout of the produced IC.

Twenty of the produced chips are in JLCC68 (Ceramic J-Leaded Chip Carrier with 68 pins) package. In the tests of continuous time current-mode Sigma-Delta ADC, analog 0.75V and digital 1.2V V_{DD}s are supplied with a power supply device. Clock signal is given using a square wave generator as 6.4MHz frequency and 1.2V amplitude with fifty percent duty cycle. Input pins are disconnected in order to see the noise level of the ADCs. Output data and clock signals are saved via an oscilloscope simultaneously. Four million data points are taken from the oscilloscope and transferred to logic values using MATLAB. Some of output data and clock signal taken from the oscilloscope is seen in Figure 5.14 while digitized values is in Figure 5.15. FFT of the output for 65536 clock cycle is seen in Figure 5.16.

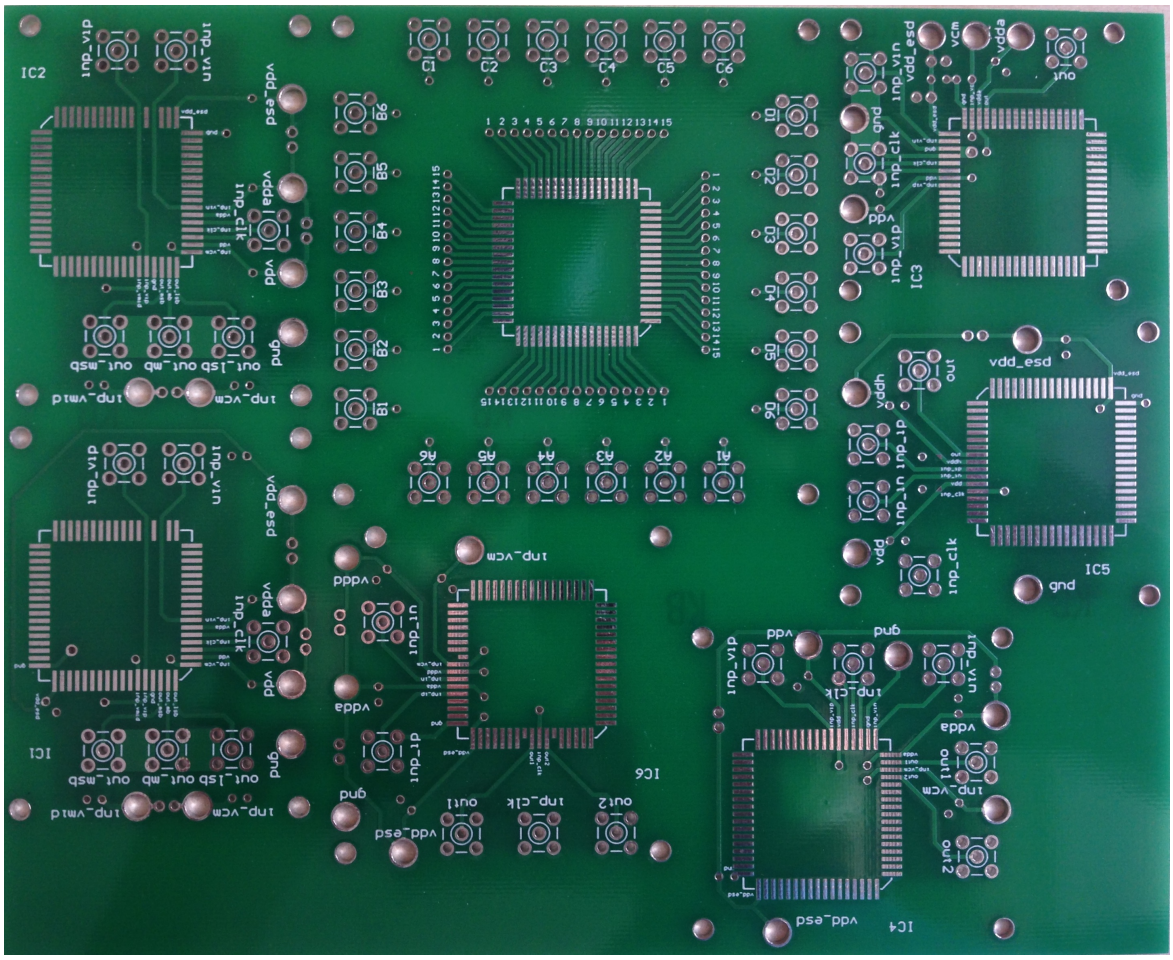

Figure 5.12. Test PCB for all circuits in IC.

A sample FFT result is shown in Figure 5.16. Noise floor of the produced ICs is higher than the simulation results. The component at the lowest frequency in the PSD is caused by offset which is the result of unequal distribution of logic one and zero values in the time interval.

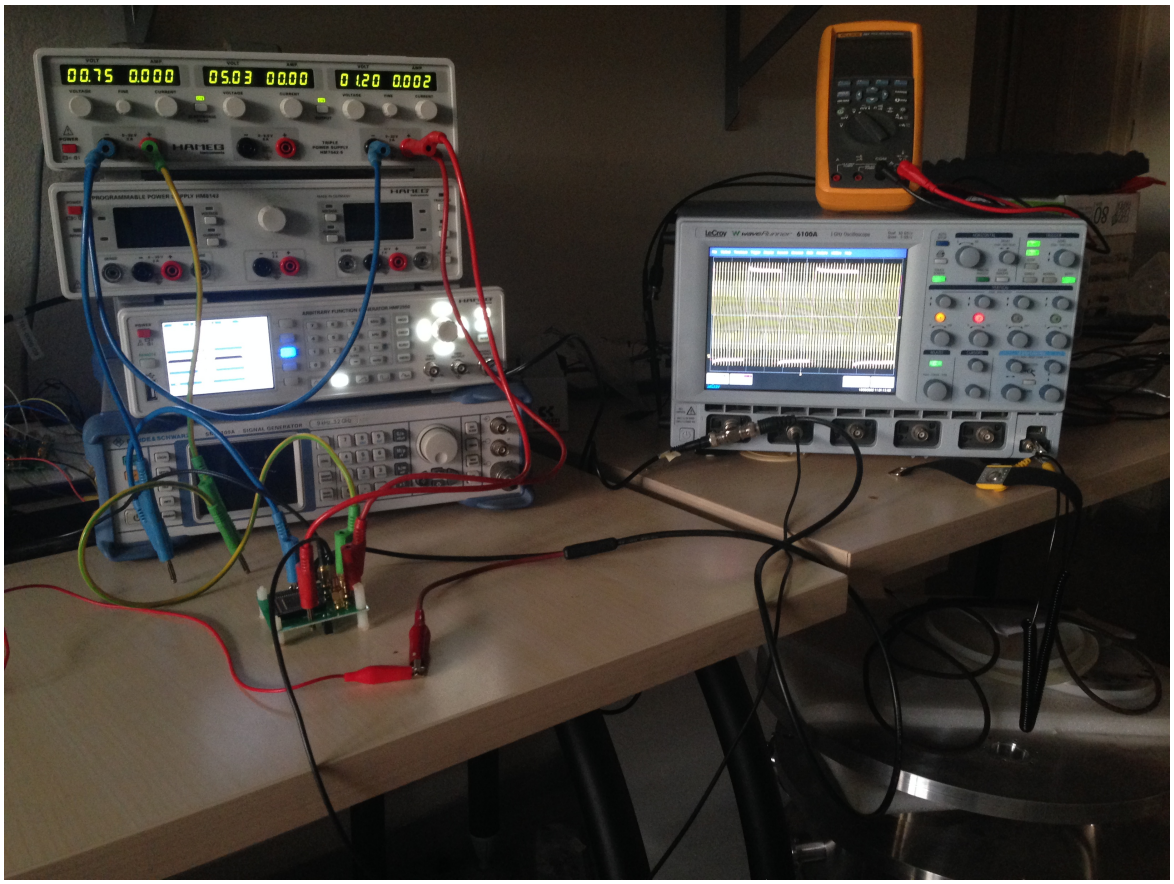

Figure 5.13. Laboratory environment during the tests of ICs.

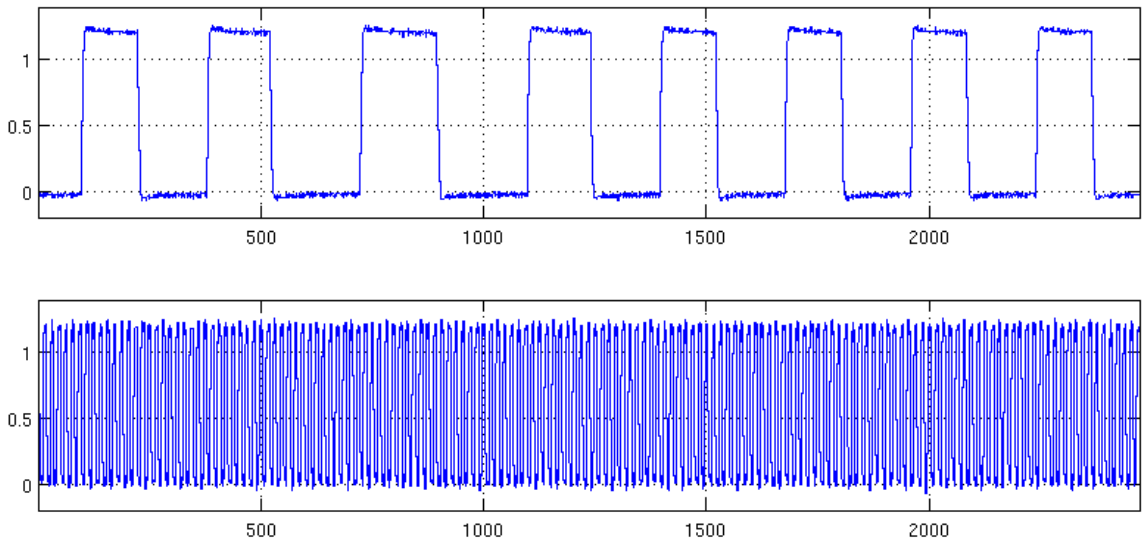

Figure 5.14. Output and clock signal taken from the oscilloscope.

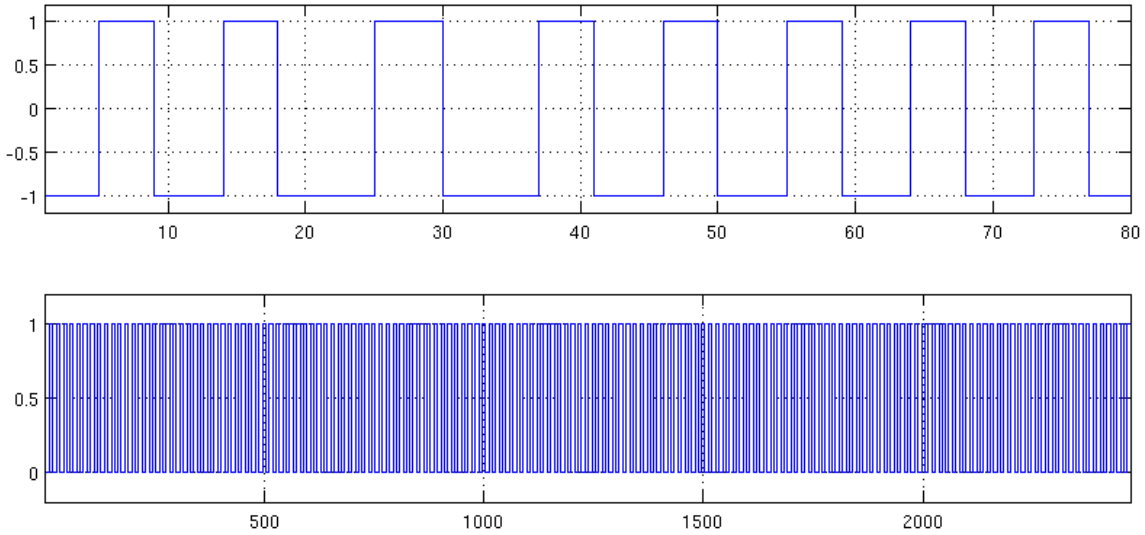

Figure 5.15. Digitized values of output and clock signal.

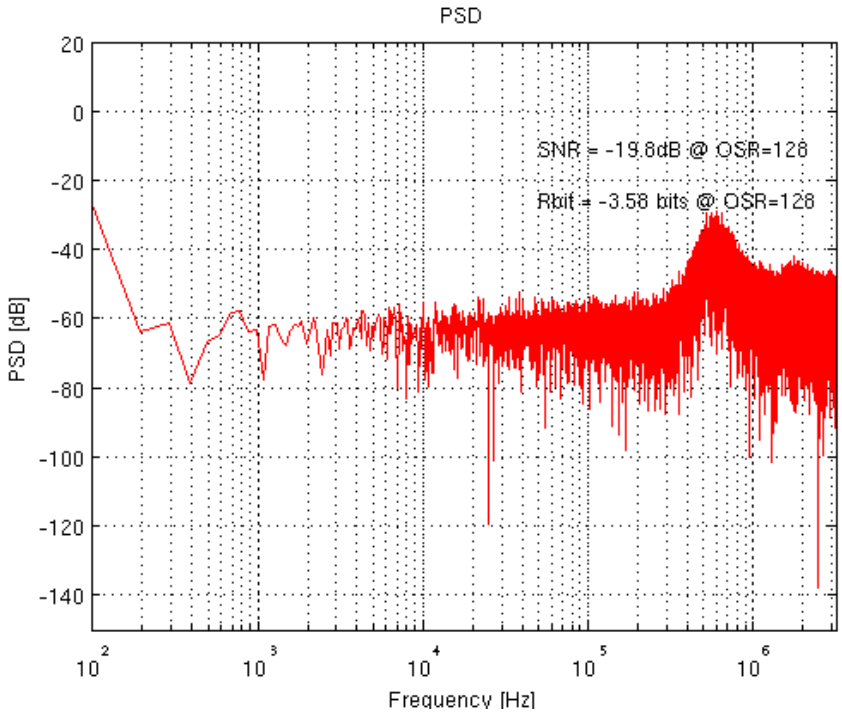

Figure 5.16. FFT results of 2nd order CT current-mode Σ-Δ ADC.

6. CONCLUSION AND FUTURE WORK

In this study, the main differences between Nyquist rate and oversampling analog-to-digital converters are examined. General properties of the Sigma-Delta ADCs are presented. Noise shaping concept is studied, design considerations and specifications of an ADC are explained. Discrete time and continuous time designs are compared conceptually and it is concluded that continuous time structures are more suitable for low power consumption Σ-Δ ADC design.

Several types of continuous time topologies for filter block of ADCs are analysed in terms of SNR and power consumption. Current-mode C-g_m integrator is chosen for the design of 2nd order continuous time current-mode Sigma-Delta ADC. A theoretical noise analysis for differential current-mode integrators has been performed step-by-step and confirmed with simulations. It has been concluded that the noise problem is very serious due to the positive feedback effect. It has also been shown that there is a trade-off between the noise performance and the improved DC-gain of the integrator achieved with enhancement resistors.

A second order continuous time current-mode Sigma-Delta ADC is designed and the layouts of the blocks are presented. Post-layout simulations are performed and 60.4dB SNR is achieved for 25KHz BW with OSR value 128. Even though second order noise shaping is observed in FFT results, noise floor is higher than the expected therefore reduces SNR dramatically. This high noise level probably caused by the differential current-mode integrators. Even the low SNR affects FoM negatively, power consumption of the designed circuit is quite low among other designs in the literature.

The designed continuous time current-mode Sigma-Delta ADC is produced in UMC 130nm process technology. Tests are performed using prepared PCBs. Because there is no laboratory equipment to generate sinusoidal current signal, tests of the current-mode circuit have been done leaving input pins unconnected. Noise floor and noise shaping are observed in this way. Results of all chips are similar and have higher

noise level than the simulations. Because of this high noise level, 2nd order noise shape could not be observed. Reasons of this situation are still being studied.

Cause of the noise in continuous time current-mode Sigma-Delta ADCs is determined as the positive feedback in the differential current-mode integrators. The design of the integrator might be changed in a way to reduce noise or other topologies should be preferred in continuous time Σ-Δ ADC design as future work.

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