DESIGN OF FRONT-END CIRCUITS FOR A HIP IMPLANT IC

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ABSTRACT

DESIGN OF FRONT-END CIRCUITS FOR A HIP IMPLANT IC

Modern CMOS technologies enable the design of low power and compact implantable devices for biomedical applications. In this thesis, a design of front-end circuits for a hip implant IC is presented, which combines MEMS and CMOS technologies. The condition of the implant is monitored in terms of its temperature and acoustic properties to detect problems earlier.

A temperature sensor for temperature measurements between 30°C and 60°C with 1°C sensitivity is designed by utilizing diodes in 0.18μm CMOS technology with a first-order $\Sigma - \Delta$ modulator based on the PTAT method. A mathematical extrapolation formula is realized by the use of MIM capacitors to obtain an adjustable full-scale temperature range. Smaller full-scale range compared to similar studies results in cost-effective design in terms of power and complexity. Dynamic element matching and autozeroing play an important role in minimizing error.

An acoustic sensor is designed to detect audio signals up to 1-2kHz by exploiting a MEMS differential capacitive sensor. Second-order $\Sigma - \Delta$ modulators based on the method in the temperature sensor are implemented. Discrete and continuous systems are compared in terms of power consumption. Different ADCs are analyzed to obtain the best overall design.

ÖZET

KALÇA İMPLANTI TÜMLEŞİK DEVRESİ İÇİN ÖN UÇ DEVRELERİN TASARIMI

Modern CMOS teknolojileri, biyomedikal uygulamalar için düşük güçlü ve kompakt yerleştirilebilir cihazların tasarımına imkan verir. MEMS ve CMOS teknolojilerini birleştiren bir kalça implantı entegre devresi için bir ön uç devre tasarımı sunulmaktadır. İmplantın durumu, sorunları daha erken tespit etmek için sıcaklık ve akustik özellikleri açısından izlenir.

30°C ve 60°C arasında 1°C hassasiyete sahip sıcaklık ölçümleri için bir sıcaklık sensörü mutlak sıcaklıkla orantı yöntemine dayalı birinci dereceden bir $\Sigma-\Delta$ modülatörle, 0.18μm CMOS teknolojisinde diyotlar kullanılarak tasarlanmıştır. Ayarlanabilir bir tam ölçekli sıcaklık aralığı elde etmek için matematiksel bir ekstrapolasyon formülü metal-yalıtkan-metal kapasitörlerinin kullanılmasıyla gerçekleştirilir. Benzer çalışmalara kıyasla daha küçük tam ölçekli aralık, güç ve karmaşıklık açısından uygun maliyetli tasarımla sonuçlanır. Dinamik eleman eşleştirme ve otomatik sıfırlama, hatayı en aza indirmede önemli bir rol oynar.

Bir akustik sensör, bir MEMS diferansiyel kapasitif sensörden yararlanarak 1-2 kHz'e kadar olan ses sinyallerini algılamak için tasarlanmıştır. Sıcaklık sensöründeki yönteme dayalı ikinci dereceden $\Sigma - \Delta$ modülatörleri uygulanır. Ayrık ve sürekli sistemler güç tüketimi açısından karşılaştırılır. En iyi genel tasarımı elde etmek için farklı örneksel sayısal çeviriciler analiz edilir.

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LIST OF SYMBOLS

A	Junction Area
B	Bandwidth
b_s	Bitstream
C_{ox}	Capacitance per Unit Area of the Gate Oxide
D_n	Diffusivity of Electrons
D_p	Diffusivity of Holes
f	Frequency
f_s	Sampling Frequency
I	Current
I_{r0}	Equilibrium Recombination Current
I_s	Saturation Current
J_p	Diffusion Current Density of Holes
k	Boltzman's Constant
k_Z	Temperature sensitivity of Z
L	Length of the Channel of a Transistor
L_n	Diffusion Length of Electrons
L_p	Diffusion Length of Holes
M	Total Number of Bits
m	Ratio between biasing currents
N	Number of Ones in Bit Sequence
N_A	Concentration of Acceptor Atoms
N_D	Concentration of Donor Atoms
n	Non-ideality Factor
n_i	Intrinsic Carrier Concentration
n_p	N-type Minority Carrier Concentration
p_n	P-type Minority Carrier Concentration
q	Electron Charge
T	Absolute Temperature

T_s	Sampling Period
V_{ac}	Acoustic Emission Voltage
V_{cm}	Common-Mode Voltage
V_d	Diode Voltage
V_{DD}	Supply Voltage
V_{GS}	Gate to Source Voltage
V_{PTAT}	Proportional to Absolute Temperature Voltage
V_{ref}	Reference Voltage
V_t	Threshold Voltage
W	Width of the Channel of a Transistor
x	Gain of the Corresponding Block1
x_0	Deformation
x_n	Intersection of the Depletion and the N Regions
x_p	Intersection of the Depletion and the P Regions
y	Gain of the Corresponding Block2
Z	Arbitrary Variable
α	Gain Factor
Δ	Difference
ϵ_0	Permittivity of Free Space
κ	Deformation Sensitivity
κ_V	Voltage Sensitivity
μ_n	Mobility of Electrons
Φ	Clocks

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital Converter
AE	Acoustic Emission
AMR	Antimicrobial Resistant
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CDS	Correlated Double Sampling
CMFB	Common-Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous-Time
CTAT	Complementary to Absolute Temperature
DAC	Digital-to-Analog Converter
DC	Direct Current
DT	Discrete-Time
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
GND	Ground
IC	Integrated Circuit
KVL	Kirchhoff's Voltage Law
MEMS	Micro Electro Mechanical Systems
MIM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
NMOS	N-Channel Metal Oxide Semiconductor
OPAMP	Operational Amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PMOS	P-Channel Metal Oxide Semiconductor
PSD	Power Spectral Density

PTAT	Proportional to Absolute Temperature
SC	Switched-Capacitor
SNR	Signal to Noise Ratio
THR	Total Hip Replacement

1. INTRODUCTION

The quality of healthcare systems is highly increased by recent advances in technology and engineering. The orthopedic implant market is also shaped by these developments. Total hip replacement (THR) is a commonly conducted surgery for those who suffer from hip pain. Rising life expectancy will lead to a dramatic increase in demand for hip implants [1]. The lifespan of modern hip implants is around 10 years [2] due to some factors such as materials used for implants, activities of patients. Typical hip implant failures are dislocation, loosening, and infection, which in turn require revision surgery. Financial costs and possible health problems after a revision surgery make a monitoring and tracking system essential for early detection of failures. Early detection can increase the lifespan of implants and decrease the need for revision surgery. Even though revision surgery may be inevitable, early detection can increase the success rate of the surgery [3]. Recent advances in electronics have enabled the design of a proper monitoring system for a hip implant.

1.1. Monitoring Principles of a Hip Implant

Dislocations and loosening of a hip implant can be detected via physical parameters such as temperature, force, vibration, and acoustic emission. There are many studies dedicated to different monitoring systems [4].

Temperature is a very useful indicator since friction caused by a patient's activities and infection due to antimicrobial resistant (AMR) bacteria result in elevated temperatures. Therefore, the temperature of the implant is a measure of its proper function and it can be utilized as a precaution to loosening [5]. Force sensors also play an important role in exclusively measuring friction. They are beneficial in detecting an upcoming failure together with temperature sensing elements [6].

Vibration and acoustic methods are also monitoring techniques [4]. Growth of undesired bone and misalignment will cause a frequency shift in the resonance frequency in the vibration method. Thus, the amount of frequency shift is regarded as a measure of loosening of the implant. The frequency content of the sound generated around the implant can be adaptively analyzed for possible failure detection when the acoustic method is utilized. Piezoresistive [7] and capacitive sensors [8] are widely utilized for this type of measurement based on design specifications.

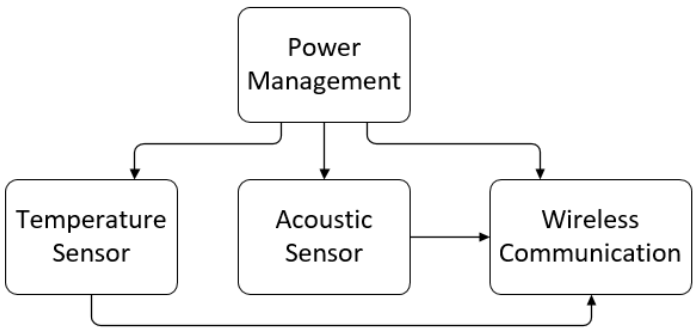

Figure 1.1. Block diagram of the hip implant.

A hip implant IC mainly consists of sensors and their interfaces, and power management, and wireless communication as seen in Figure 1.1, which determine the overall performance of the hip implant. Besides, regulation and standards, and biocompatible design requirements create new challenges. A temperature sensor implies the level of infection due to AMR bacteria. In addition, an acoustic sensor is utilized to understand the degree of loosening. Complementary metal oxide semiconductor (CMOS) compatible micro electro mechanical systems (MEMS) technology relieves design specifications, costs, and production process of these sensors interfaces' electronics.

1.1.1. Temperature Sensing System

On-chip temperature sensors dominate over their off-chip counterparts in recent years [4]. On-chip sensors and their interface electronics on a single chip provide cost-effective fabrication, immunity to noise, and low power operation. A bipolar junction transistor (BJT), or a diode [9] [10] [11], or the polysilicon layer of a Metal Oxide Semiconductor (MOS) transistor [12] can be utilized as a thermal sensor in CMOS technology.

As mentioned above, the temperature of a hip implant changes due to bacteria and friction caused by human activities. The temperature of the implant varies from 35°C to 50°C maximum and 1°C sensitivity will be enough for proper monitoring. Sensing temperature should not be continuous since the power budget is limited for this smart hip implant. In addition, the temperature of the implant changes slowly; therefore it is enough to monitor and track the implant from time to time. In the hip implant's temperature sensor, the aim is to design a medium-level accurate sensing device that does not operate continuously.

1.1.2. Acoustic Sensing System

Undesired bone growth and loosening can cause a shift in the acoustic emission (AE) of the hip implant [13]. In addition to the frequency content of the hip implant, the system includes noise and undesired vibrations that are not related to the condition of the hip implant. An adaptive method can be utilized or data can be compared to that of a patient with a proper functioning implant [14] to eliminate noise and undesired vibrations. In any case, audio band acoustic sensing can be carried out to monitor the implant [15]. In the sensing system, the aim is to design an audio band acoustic sensor, which especially covers the band up to 1 kHz [13] and does not operate continuously due to the power budget.

1.2. Thesis Organization

This thesis is organized as follows:

Chapter 2 defines the design of the temperature sensor and its interface. It starts with the sensor and continues with the required temperature-insensitive current reference for the sensor. Then, it describes details of the sigma-delta analog-to-digital converter (ADC) working principle. Core blocks of this ADC are an integrator, a clocked comparator, and a digital-to-analog converter (DAC), whose details are provided in this chapter. A novel method for obtaining an adjustable range CMOS smart temperature sensor will be presented. Eventually, the chapter concludes with the overall design and its layout, and related simulations, and performance summary.

Chapter 3 is about an acoustic sensor and its related interface electronics. It presents a differential capacitive sensor and its readout circuitry with gain control. It provides the details for a second-order sigma-delta ADC whose design is an improved version of the proposed one in the temperature sensor. Discrete-time (DT) and continuous-time (CT) readout circuits, and second-order sigma-delta ADCs with and without an external reference are combined into four different designs. Their performances are analyzed for the best combination in terms of power, signal-to-noise ratio (SNR), and the effective number of bits (ENOB). Finally, the chapter comes to a close with the overall design and its layout, and related simulations, and performance summary.

Chapter 4 concludes the thesis and proposes possible future work.

2. TEMPERATURE SENSOR AND ITS INTERFACE

Temperature sensors are commonly used in many applications. There are numerous designs for on-chip temperature sensors in the literature [9] and [12]. Proportional to absolute temperature (PTAT) type temperature sensors are also very popular [11], [16] and [17] due to their linearity in many applications such as biomedical designs. A smart sensor and its interface electronics on a single chip provide a cost-effective fabrication. The smart sensor converts the temperature information of a system to a digital representation; therefore, an ADC should be utilized for this purpose. Sigma-delta ADCs are very appropriate ADCs for on-chip low-cost temperature sensor designs since they provide high resolution by trading the speed. Besides, their noise-shaping behavior is beneficial to eliminate noise and unrelated vibrations.

Accuracy is one of the most important issues in temperature sensor designs. A full-scale range ideally between 0K and 600K is provided by PTAT sensors. Smart sensors with $\pm 0.5^{\circ}$C and $\pm 0.1^{\circ}$C sensitivity benefiting from parasitic bipolar transistors or diodes are designed by using various approaches such as dynamic offset cancellation, curvature correction, and dynamic element matching. However, many applications do not require this level of accuracy. For instance, the $\pm 0.1^{\circ}$C inaccuracy sensor design over 600K [16] requires 16 bits resolution for a maximum quantization error, $\pm 0.01^{\circ}$C due to 60000 levels of quantization. Therefore, the system can be realized by at least a second-order sigma-delta ADC. The modulator is still second-order even for higher inaccuracies since the full-scale is 600K [16]. There are some methods to decrease the dynamic range which introduce a higher level of complexity at the expense of two or three-fold decrease in full-scale. The methods in [17] and [18] require new PTAT current sources in the overall current-based design resulting in noise and power problems. Proposed circuit provides a different way to reduce full-scale to 30K. This decrease in full-scale and $\pm 0.1^{\circ}$C maximum quantization error for guaranteeing $\pm 1^{\circ}$C inaccuracy allows using first-order sigma-delta modulator based design without requiring extra current sources and current source related circuitry. In addition, the frequency of

the comparator's clock can be around 2-3 kHz for 128 to 256 oversampling ratio in applications such as long-term medical sensing since the temperature signal changes very slowly, which is nearly a direct current (DC) signal. Such a low clock frequency also decreases the power required to generate it and the power consumed by the ADC; thus, it makes a first-order design acceptable. The main idea is to use a mathematical model benefiting from the linearity of metal-insulator-metal (MIM) capacitors to decrease full-scale to much lower values. Block diagram of the overall temperature sensor is illustrated in Figure 2.1.

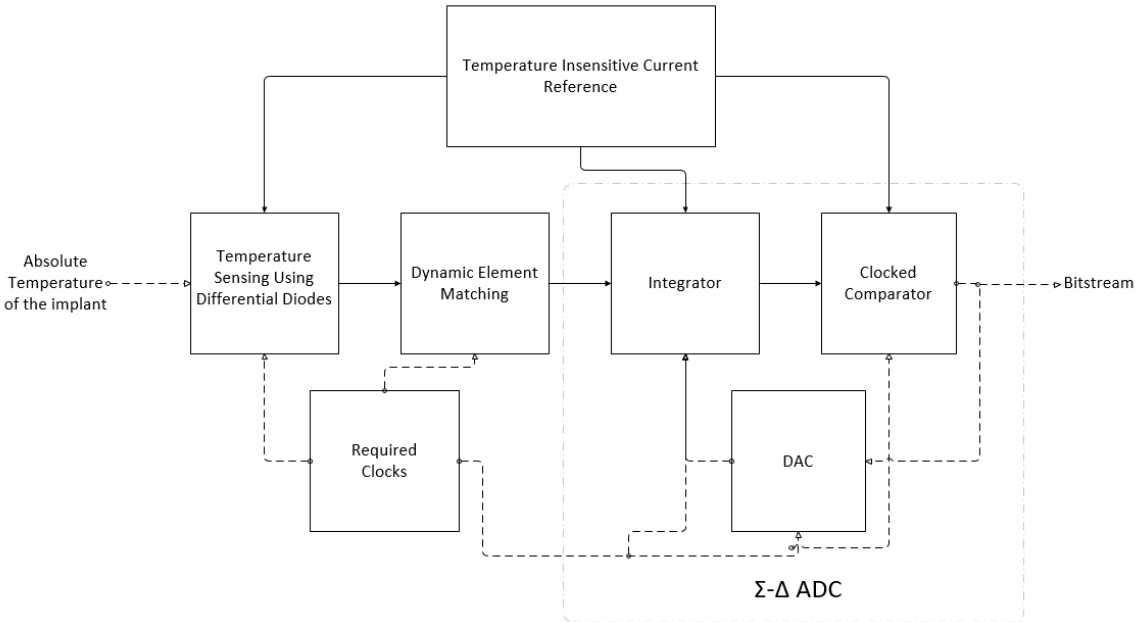

Figure 2.1. Block diagram of the temperature sensor.

2.1. Temperature Sensing Using Differential Diodes

In order to obtain digital data from temperature readings, it is required to have a PTAT voltage and a temperature-independent voltage reference. Two diodes are used to generate diode voltage difference ΔV_d and diode voltage V_d, also denoted as V_{d1}. These voltages will be carefully determined for reference and PTAT voltages as illustrated in Figure 2.2 where x and y are the corresponding gains and α is the gain factor for a temperature-insensitive reference voltage.

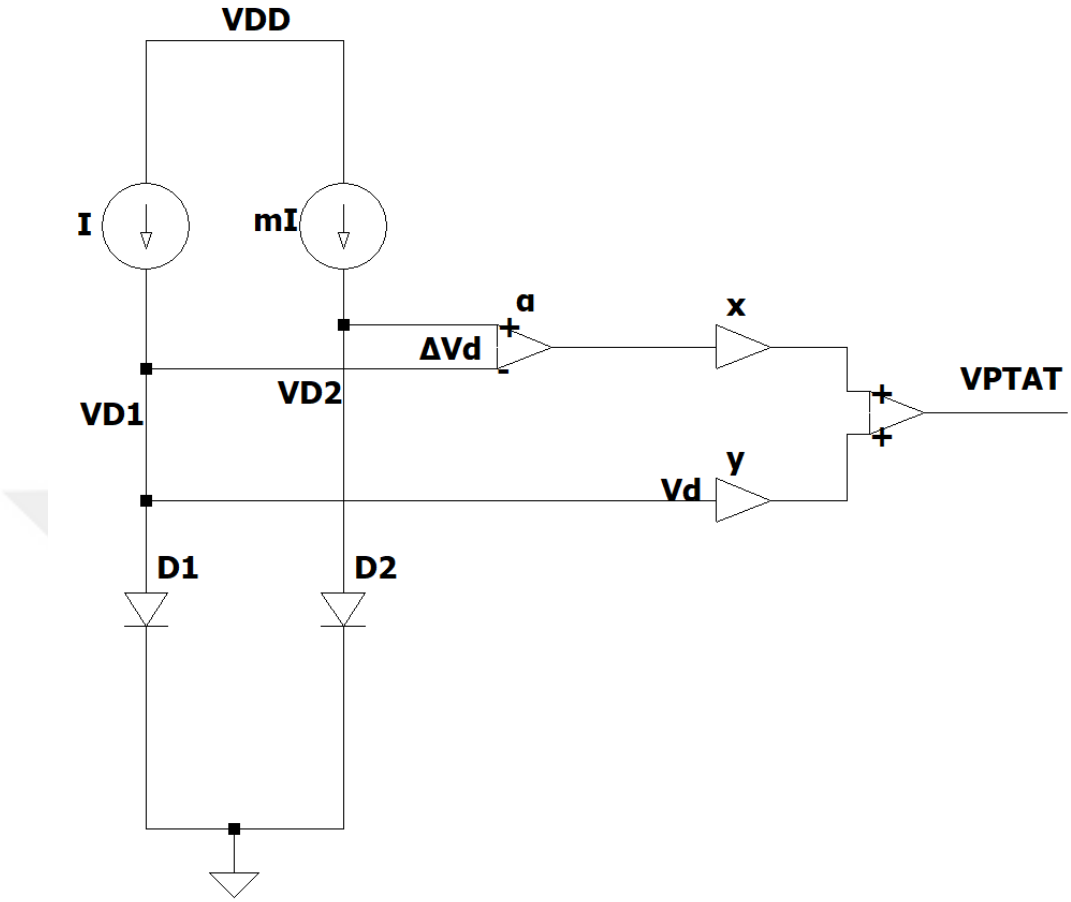

Figure 2.2. Temperature sensing principle.

Reviewing the characteristics of a diode will be helpful to understand its temperature dependence [19].

2.1.1. General Characteristics of the Ideal Diode

For a p-n junction, minority carrier concentration at the edge of the n region and the depletion region p_n can be defined as

$$\begin{aligned} p_n(x_n) &= p_{n0}(\exp(\frac{V_d}{V_T}) - 1) \\ V_T &= \frac{kT}{q} \end{aligned} \tag{2.1}$$

where $p_n(x_n)$ is minority carrier concentration at the edge of the n region and the depletion region, p_{n0} is the equilibrium minority carrier concentration in the n region, x_n is the intersection of the depletion and the n regions, and V_T is the thermal voltage. k stands for Boltzmann's constant, T is the absolute temperature, and q is the electron charge. The diffusion current density of this minority carrier at the edge of the n region and the depletion region J_p is

$$J_p(x_n) = \frac{qD_p}{L_p} p_{n0}(\exp(\frac{V_d}{V_T}) - 1) \tag{2.2}$$

where D_p is the diffusivity of holes and L_p is the diffusion length of holes. Similarly, the diffusion current density of opposite minority carrier at the edge of the p region and the depletion region J_n is

$$J_n(-x_p) = \frac{qD_n}{L_n} n_{p0}(\exp(\frac{V_d}{V_T}) - 1) \tag{2.3}$$

where $-x_p$ is the intersection of the depletion and the p regions, D_n is the diffusivity of electrons, n_{p0} is equilibrium minority carrier concentration in the p region, and L_n is the diffusion length of electrons. Both current densities have their maximum at these edges. They together contribute to the diffusion current, which is the dominant one in the forward-biased case,

$$\begin{aligned} I &= A(J_n + J_p) \\ I &= Aq(\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0})(\exp(\frac{V_d}{V_T}) - 1) \end{aligned} \tag{2.4}$$

where I and A stand for the diffusion current and the junction area, respectively. The diffusion current can be rewritten in terms of the saturation current I_s as,

$$\begin{aligned} I &= I_s(\exp(\frac{V_d}{V_T}) - 1) \\ I_s &= Aq(\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0}) \end{aligned} \tag{2.5}$$

since p_{n0} and n_{p0} can be written in terms of the intrinsic carrier concentration n_i [19], we arrive at

$$I_s = Aqn_i^2(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}) \tag{2.6}$$

where N_A and N_D represent the concentration of acceptor and donor atoms, respectively. I_s changes with T since n_i and diffusivities are dependent on T. However, the strong nonlinear temperature dependence of n_i dominates over the effects of diffusivities. Therefore, it is not possible to obtain a PTAT signal from one diode. For high forward-bias voltage, $V_d >> V_T$, -1 can be neglected; thus, the voltage of a diode for a constant biasing current can be obtained as

$$V_d(T) = \frac{kT}{q}\ln(\frac{I}{I_s(T)}). \tag{2.7}$$

The differential voltage ΔV_d in Figure 2.2 will be

$$\begin{aligned} \Delta V_d &= V_{D2} - V_{D1} \\ \Delta V_d &= \frac{kT}{q}\ln(\frac{mI}{I_s(T)}) - \frac{kT}{q}\ln(\frac{I}{I_s(T)}) \qquad (2.8) \\ \Delta V_d(T) &= \frac{kT}{q}\ln(m) \qquad (2.9) \end{aligned}$$

where m stands for the ratio between biasing currents of diodes. The resulting ΔV_d is a PTAT signal, which is ideally not dependent on any process-related parameters. However, some nonidealities can cause a shift from the ideal operation.

2.1.2. Nonidealities of the Sensing System

Equation (2.9) indicates a linear process-independent PTAT signal when the recombination of hole-electron pairs in the depletion region is ignored. Some of the diffused carriers are recombined in the depletion region; therefore, they contribute to

the recombination current [20]. The recombination current I_r can be defined as [21]

$$I_r = I_{r0} \exp(\frac{qV}{2kT}) \tag{2.10}$$

where I_{r0} is the equilibrium recombination current, which is affected by the intrinsic carrier concentration, the width of the depletion region, and the recombination lifetime. This recombination current adds up to the diffusion current. Since the analytical expression of total current through a diode can not be easily obtained, the resulting total current can be approximated as an empirical formula [21]

$$I = I_s(\exp(\frac{qV}{nkT}) - 1) \tag{2.11}$$

where n is a non-ideality factor, which represents the deviation of the behavior of the diode from the ideal behavior. n gets closer to 1 for a relatively large forward-bias voltage since the diffusion current dominates over the recombination effect and it increases up to 2 for a small forward-bias voltage since the recombination effect dominates over the diffusion current. Even though n is a process-dependent parameter due to the association with I_{r0}, differential diode structure is still applicable since the temperature range of concern is relatively low in our design, which is between 35°C and 50°C within 1°C sensitivity.

2.1.3. Diodes in CMOS Technologies

Diodes can be implemented in two main ways in umc 0.18μm CMOS technology: diode-connected transistors and special diodes provided in the design library. Diode-connected MOS transistors is not an option since their temperature characteristics do not provide the desired operation in our application. Diode-connected BJT transistors are even better than diodes in the CMOS library as temperature sensing elements since the non-ideality factor n is very close to 1 [22], which means a process-independent PTAT voltage. However, there are no external BJTs in standard CMOS processes. Therefore, parasitic BJTs can be utilized as a sensor. Substrate and

lateral BJTs are two types of parasitic BJTs. Substrate pnp transistors are formed between p+/nwell/psubstrate (emitter/base/collector) from a p-channel metal oxide semiconductor (PMOS) transistor. Since their collector is at the ground, they should be modified for a proper temperature sensing [18] [23]. In addition, they have huge base and collector resistances that degrades their performance [21]. Lateral pnp transistors are formed between p+/nwell/p+ (emitter/base/collector) from a PMOS transistor. One of the disadvantages is an extra parasitic BJT formed in the substrate BJT form. In addition, curved currents can cause a deviation in the operation.

The other alternative is to utilize special diodes provided in the design library. N+/psubstrate is one of them whose psubstrate is connected to the ground. For a nwell/p+ diode, the p+ region is drawn inside the nwell. By utilizing the triple-well process to adjust the voltage of the nwell, nwell/p+ diode can be used as a temperature sensor, too. Nwell/psubstrate is another option. However, it can not be utilized as a temperature sensor element.

2.1.4. Simulation of Parameters and Determination of Gains

The temperature behaviour of V_d at a reference temperature 37°C, human body temperature, will have a negative slope of about —2mV/°C [24] due to the effective temperature dependency of the saturation current. By subtracting two diode voltages ΔV_d has a PTAT relationship defined in Equation (2.9)

The ratio between biasing currents m is determined as 5 and the biasing current I is chosen as 5μA in order to guarantee proper operation of diodes for the DC level of the subsequent block, which is the differential PMOS input integrator of the ADC and power considerations. Therefore, the temperature coefficient of ΔV_d is around 0.14 mV/°C by using the formula given in the Equation (2.8). The PTAT voltage which covers a smaller full range is expressed as

$$V_{PTAT} = x(\alpha \Delta V_d) - y(V_d) \tag{2.12}$$

where x and y should be meticulously chosen to yield the desired full-range as illustrated in Figure 2.2. The gain factor α is to cancel out voltage dependency of the reference voltage V_{ref}, which is defined as

$$V_{ref} = \alpha \Delta V_d + V_d. \tag{2.13}$$

By taking the derivative of V_{ref} with respect to the temperature, Equation (2.14) is obtained as follows:

$$\frac{d(V_{ref})}{dT} = \alpha(\frac{d(\Delta V_d)}{dT}) + \frac{d(V_d)}{dT}. \tag{2.14}$$

α should be chosen between 14 and 15 to eliminate temperature dependency of V_{ref} since $\frac{d(V_d)}{dT}$ =—2mV/°C and $\frac{d(\Delta V_d)}{dT}$ =0.14 mV/°C as mentioned. Until now we consider that V_d has a negative linear proportionality with the absolute temperature; however, V_d shows a nonlinear behavior [25], curvature effect. Thus, it causes deviation from the proper operation. This slightly nonlinear behavior of V_d leads us to use V_{ref} whose temperature gradient is a small positive number, which is not zero [16]. Therefore, α is defined as 16 to handle the curvature with regard to the nonlinear behavior of V_d. Thus, the resulting V_{ref} is around 1.4 V, slightly higher than the bandgap voltage, for the bias current. x and y values can be chosen appropriately to specify different full-ranges based on rough extrapolation formulas:

$$\alpha \Delta V_d(T) = \frac{1.4T}{600} \tag{2.15}$$

$$V_d(T) = 1.4 - \frac{1.4T}{600} \tag{2.16}$$

where first-order best-fit curve approximation is used. When x and y are determined as 10, we end up in full scale between 30°C and 60°C, which is 20 times lower than 600°C full-scale value as seen in Figure 2.3. This full-scale range covers the desired temperature spectrum from 35°C and 50°C. 30°C full-scale with 1°C sensitivity only

requires a nine to ten bits modulator design by guaranteeing that errors do not result in deviations more than 0.1°C. Nine to ten bits resolution for a sigma-delta modulator can be easily achieved by a first-order structure [26].

It is possible to obtain more realistic values for x and y after several iterations when different CMOS technologies and all nonidealities are included. When areas of n+/psubstrate and nwell/p+ diodes are adjusted to $720\mu^2$ for a desired output voltage range, and area of nwell/psubstrate diode is $97200\mu^2$ since it is fixed, voltage of diodes for a temperature sweep from 35°C to 50°C for 5μA bias current are illustrated in Figures 2.5, 2.6, and 2.7. N+/psubstrate diode is chosen based on the temperature characteristics. This diode experiences about a 30mV voltage decrease for end-to-end temperature sweep, which is an expected result.

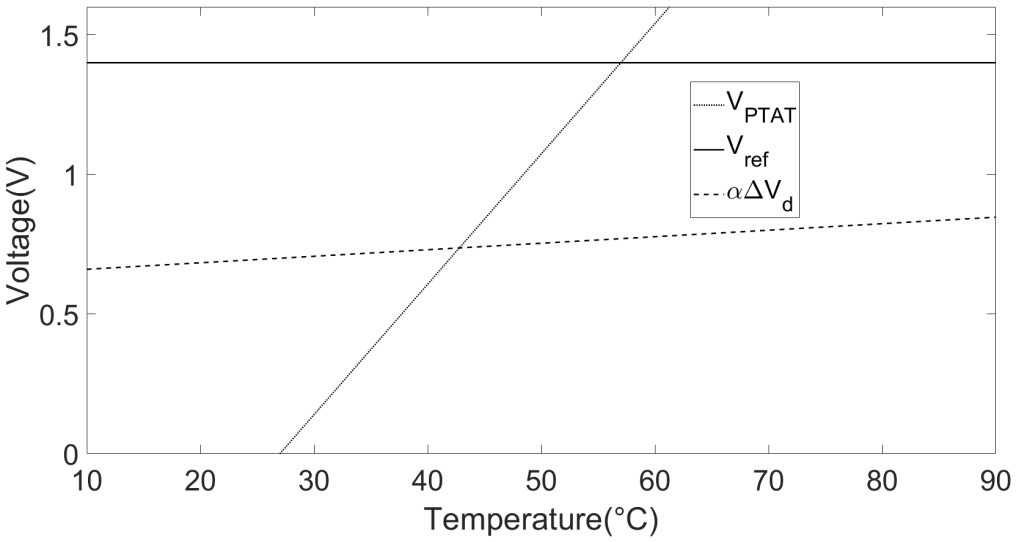

Figure 2.3. Temperature behavior of ideal critical voltages.

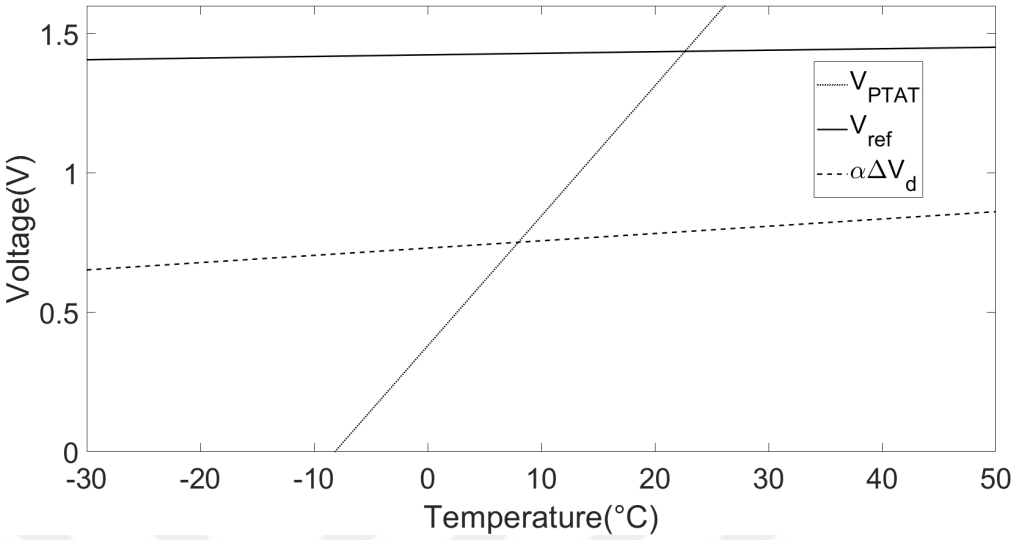

Figure 2.4. Temperature behavior of critical voltages generated by diodes in the CMOS library when x and y are 10.

Simulations of the differential diodes structure in the CMOS library are illustrated in Figure 2.4 when x and y are 10.

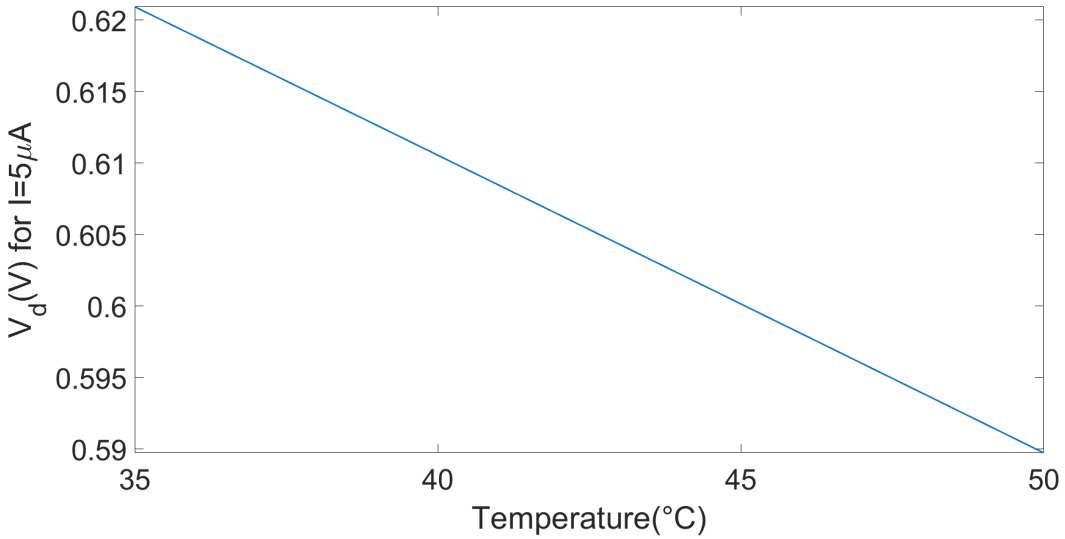

Figure 2.5. Voltage of n+/psubstrate diode for the temperature sweep from 35°C to 50°C.

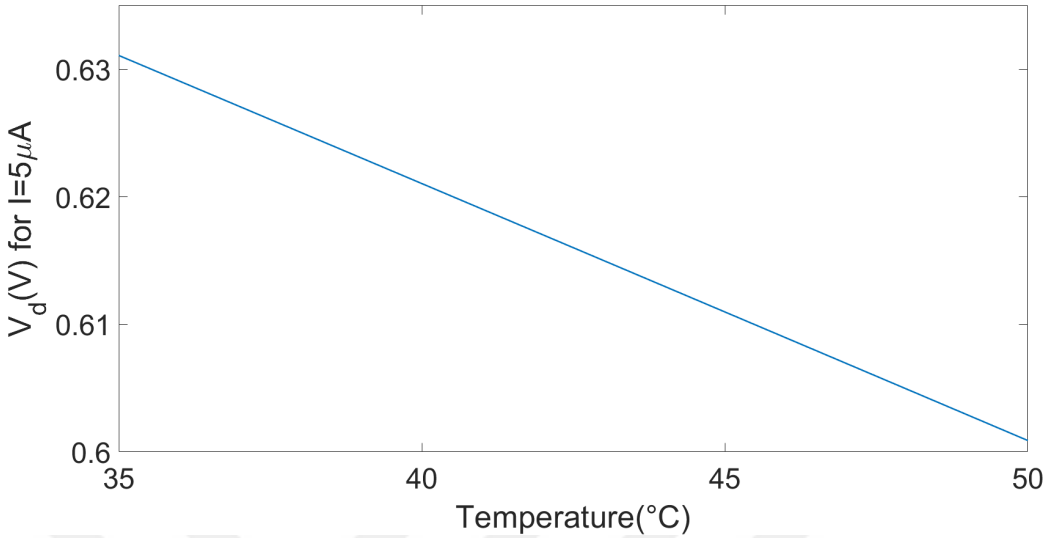

Figure 2.6. Voltage of nwell/p+ diode for the temperature sweep from 35°C to 50°C.

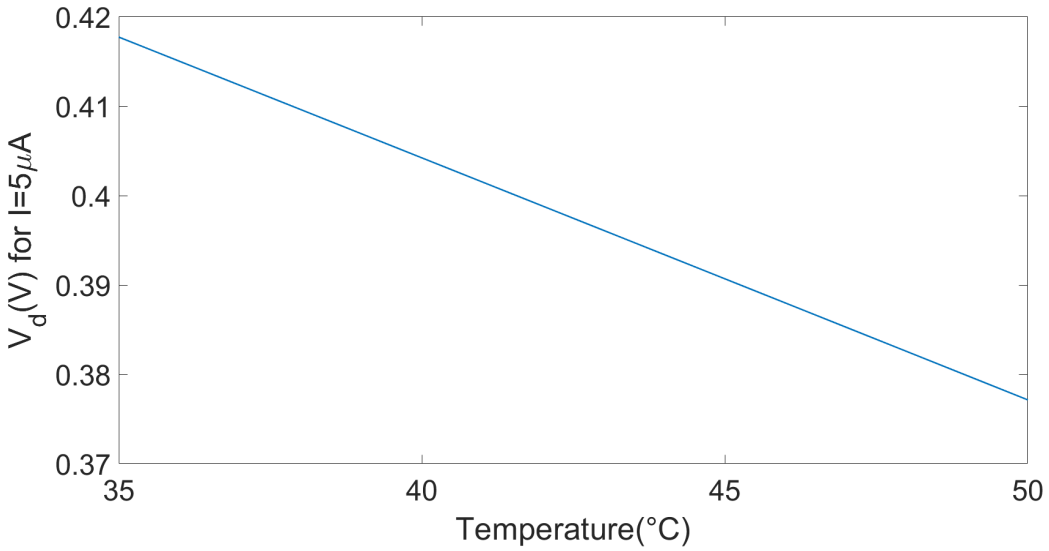

Figure 2.7. Voltage of nwell/psubstrate diode for the temperature sweep from 35°C to 50°C.

It is observed that the corresponding PTAT voltage for the ideal extrapolated values of x and y diverges from the desired range, 35°C to 50°C. When nonidealities related to the extrapolation formula, the technology and the components are corrected

based on simulations of diodes, x and y values are 9.1 and 11.7 for V_{PTAT}, respectively, to cover between 30°C and 60°C as full-scale. The corrected simulations of the differential diodes structure in the CMOS library can be observed in Figure 2.8. How to implement determined x, y, and α values, which is the core of the proposed circuitry, will be shown in the sigma-delta modulator section.

2.2. Temperature-Insensitive Current Reference

Temperature-compensated and supply voltage-insensitive current references are very important for the performance of most analog and digital electronics blocks. Some of the current references are generated based on the bandgap reference circuit where lateral or substrate BJTs mentioned in the previous section are utilized in the CMOS technologies [27] [28] [29] [30]. In addition to the disadvantages mentioned before, the complexity level and the area of the design are quite high.

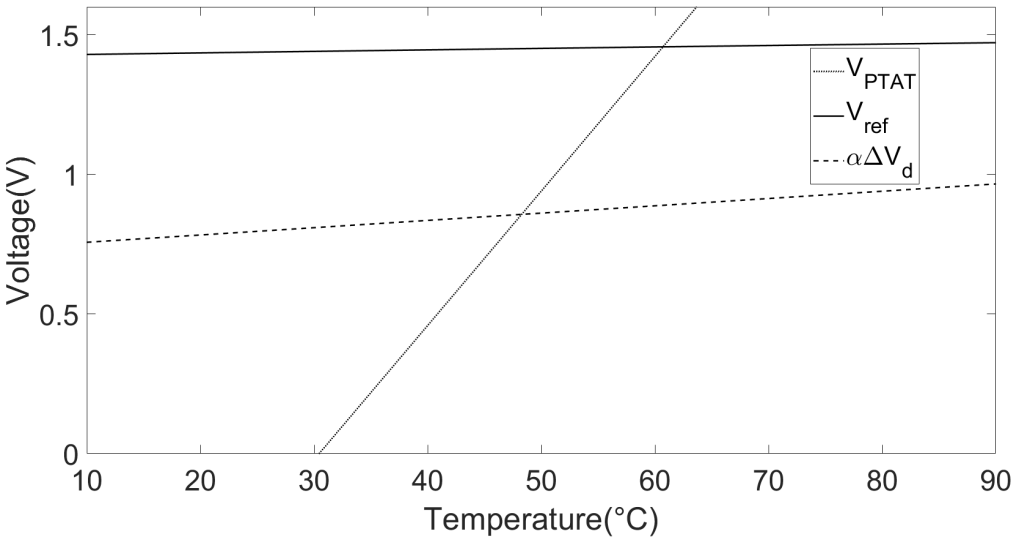

Figure 2.8. Temperature behavior of critical voltages generated by diodes in the CMOS library for the corrected x and y.

Some designers decide to bias MOS transistors at the subthreshold region as an alternative method [31]. However, biasing transistors at the subthreshold region and eliminating the degradation of the performance due to deviations are not so easy. The addition of PTAT and complementary to absolute temperature (CTAT) signals by implementing variable thickness gate transistors also results in a temperature-compensated current reference [32] [33]. These circuits benefit from the temperature characteristics of threshold voltages and mobilities of electrons or holes; however, it is practically impossible to adjust these values since they are process-dependent quantities. Five MOS transistors and a resistor excluding the start-up can be used for a temperature-insensitive current reference [34]. This design can be regarded as a proper method by taking the area and the complexity considerations into account. The operation of the proposed temperature sensor strictly depends on stable and temperature-insensitive currents as observed in Figure 2.2.

2.2.1. Design of the Current Reference

M1 to M5 and the resistor form the desired current reference and M6 to M8 serve as the start-up circuitry as illustrated in Figure 2.9. If we write down the Kirchhoff's Voltage Law (KVL) around M3-M4-M5 and the resistor loop by ignoring the start-up part,

$$V_{GS5} + V_{GS3} - V_{GS4} - mIR = 0 \tag{2.17}$$

where V_{GS} is gate to source voltage. V_{GS} can be written in terms of I,

$$\sqrt{\frac{2I}{\mu_n C_{ox}}}\left(\sqrt{\frac{L_3}{W_3}} + \sqrt{\frac{L_5}{W_5}} - \sqrt{\frac{mL_4}{W_4}}\right) + V_{tn} - mIR = 0 \tag{2.18}$$

where μ_n and C_{ox} stand for the mobility of electrons and the capacitance per unit area of the gate oxide. V_{tn} represents the threshold voltage of an N-Channel Metal Oxide Semiconductor (NMOS) transistor. In addition, W and L are the width and the length of the channel of the transistor, respectively. The first term has a negative

temperature gradient due to the temperature dependence of μ_n. The temperature characteristics of V_{tn} are shaped by the technology; therefore, it is not configurable. However, adjusting the resistance value for a known temperature dependence can result in a temperature-compensated current reference. By taking the temperature derivative of Equation (2.18) [34] and arranging terms, we obtain the required resistance value

$$R = \frac{V_{tn}}{mI} \frac{k_{\mu_n} + 2k_{V_{tn}}}{k_{\mu_n} + 2k_R} \tag{2.19}$$

in which the temperature sensitivity of an arbitrary variable Z, k_Z, can be expressed as [34]

$$k_Z = \frac{1}{Z} \frac{dZ}{dT}. \tag{2.20}$$

Depending on the temperature behavior of the resistor, the schematic in Figure 2.9 can be modified. The resistor can be connected to the source of M5 and the source of the M4 is connected to the ground. The required value of the resistor would be the opposite of Equation (2.19) [34].

2.2.2. Resistors in CMOS Technologies

Designers exploit different types of circuitry which behave like a resistor; however, these MOS transistor based resistor models can not be used in the mentioned current reference since their temperature characteristics are not controllable. Resistors in standard CMOS libraries should be used for this purpose.

Standard low-cost CMOS technologies includes four types of resistors [21]. Polysilicon resistors can have a varying temperature dependency based on the implants used. Even though they are quite linear, they experience voltage-dependent resistance values. Shallow diffusion resistors are generated out of implants for the diffusion in the CMOS process. The generated p-n junction should be isolated for proper functioning;

therefore, it should be reverse biased.

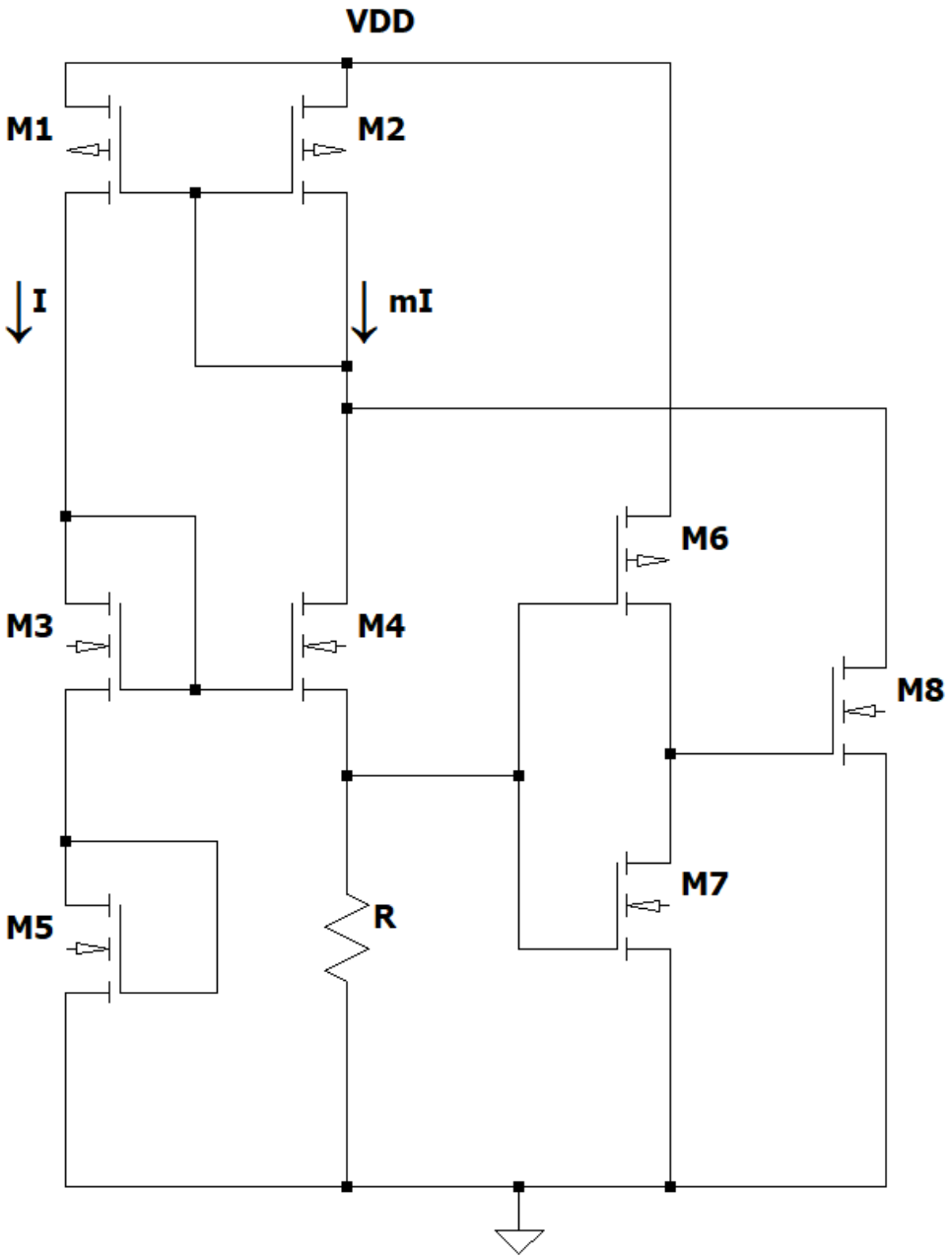

Figure 2.9. Schematics of the temperature-insensitive current reference.

Well resistors can provide huge sheet resistance due to the low doping. However, they can not be utilized with diodes since the resistance is positively correlated to the saturation current of a diode because of the common material used. This positive association degrades the linear temperature sensing property of the design. The last resistor model in CMOS libraries is metal interconnect resistors. They can not be utilized in the current reference since their resistance value is quite low for an acceptable area.

Process-spread, the temperature behavior, and the area considerations decrease resistor options that are provided by libraries. A high resistive poly resistor is chosen as the resistor from our design library by considering the temperature coefficient and the occupied area for a given resistance value at the expense of process sensitivity.

2.2.3. Start-up Circuitry

Start-up circuits are required to obtain the desired stable state from a reference circuit. A reference circuit has two stable states: no current case, the desired state. The start-up circuit should trigger the reference circuit up to the desired state. It should not affect the operation of the reference circuit when the desired state is achieved. M6-M7-M8 in Figure 2.9 form the desired start-up circuit [24]. If the voltage on the resistor is zero, which is the zero current state, the gate of M8 will be pulled up to the high voltage to sink current from M2. Increasing current through M2-M4 and the resistor branch will make the voltage at the common gate of M6 and M7 rise up to mIR. For this voltage, the inverter converts it to zero gate voltage for M8, no current will flow through M8. Therefore, the operation of the reference will not be disturbed after the desired stable state is achieved. The aspect ratio of the M6 must be much lower than that of M7 in order for the inverter to regard the voltage around 0.6V, mIR, as the logic 1. The simulation of the inverter function of the start-up is shown in Figure 2.10.

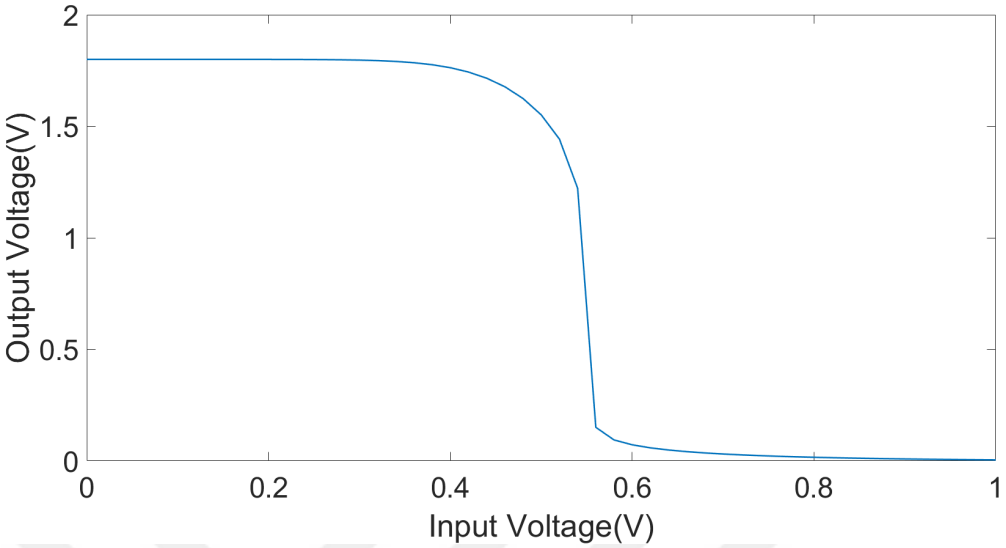

Figure 2.10. Inverter action of the start-up circuit.

2.2.4. Simulation and Layout of Current Reference

The reference current generated is mirrored to obtain bias currents of diodes I and $5I$. The current mirror does not affect the m due to the changing temperature since the operation is based on matching of two devices on the same substrate. Pre-layout and post-layout simulations of the current at different temperatures for the designed temperature-insensitive current reference are illustrated in Figure 2.11 and Figure 2.12. Deviation of 0.68% occurs for bias currents, which does not disturb the proper operation. The layout of the design is shown in Figure 2.13.

The performance of the designed current reference can be analyzed through the supply voltage dependence and process sensitivity of the resistor. The resulting bias currents are shown in Figure 2.14 and Figure 2.15, respectively. The function of the circuit can be regarded as acceptable between 1.2V and 2.1V. Deviation of the resistance value around $\pm 20\%$ causes the bias current whose nominal value is 5μA to change from 4.1μA to 6.6μA. However, the sensor still can operate well as long as diode voltages are in the allowed input range of the following ADC since the current ratio of differential diodes is the same due to the current mirror action.

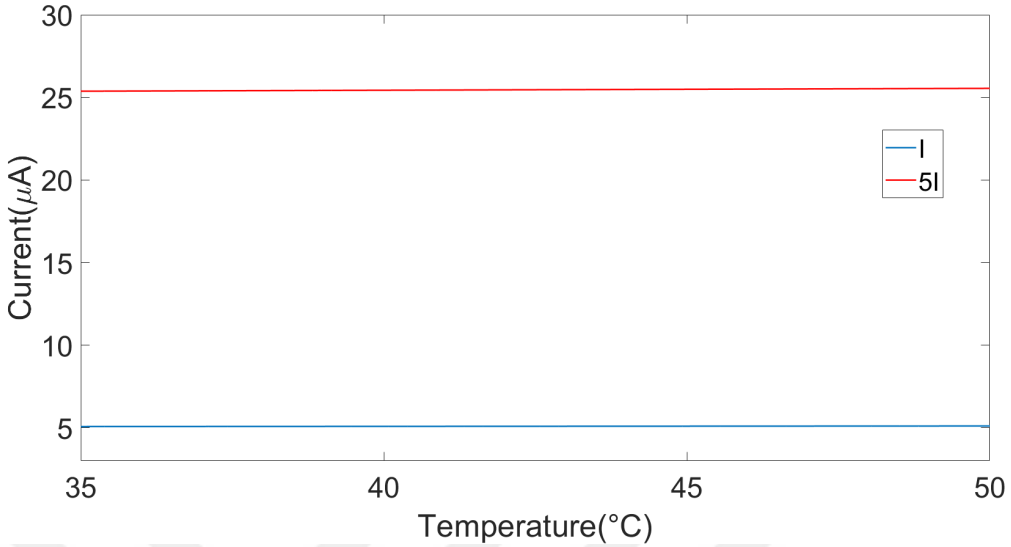

Figure 2.11. Temperature sweep for I and $5I$ for pre-layout.

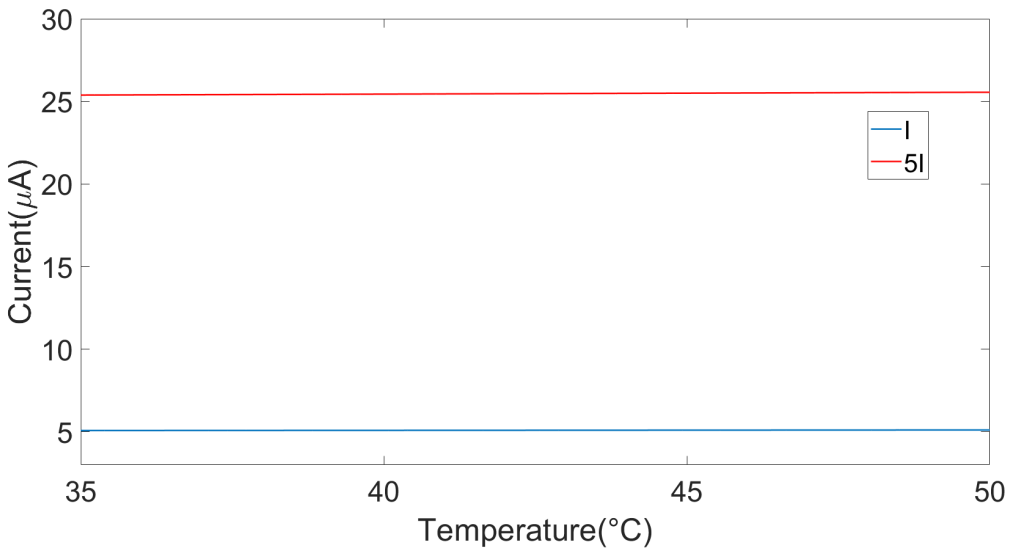

Figure 2.12. Temperature sweep for I and $5I$ for post-layout.

2.3. Sigma-Delta ADC

This section is about how to convert ΔV_d and V_d into digital temperature output by generating V_{PTAT} and V_{ref}. This conversion is held by an ADC and its related

circuits.

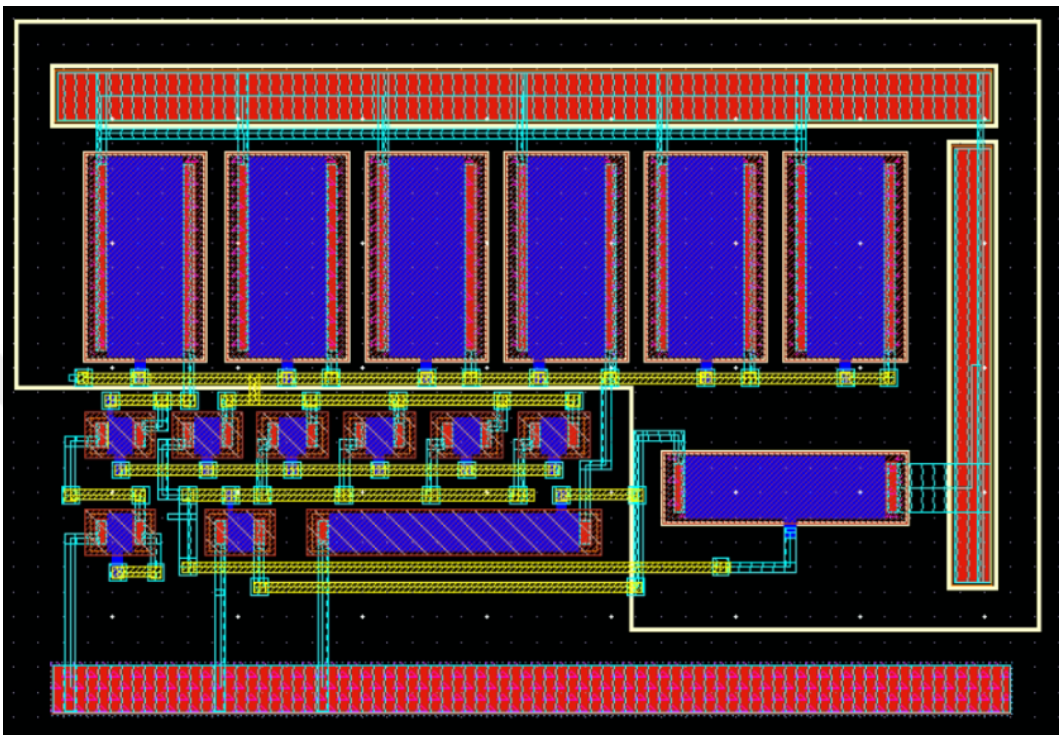

Figure 2.13. Layout of the temperature-insensitive current reference.

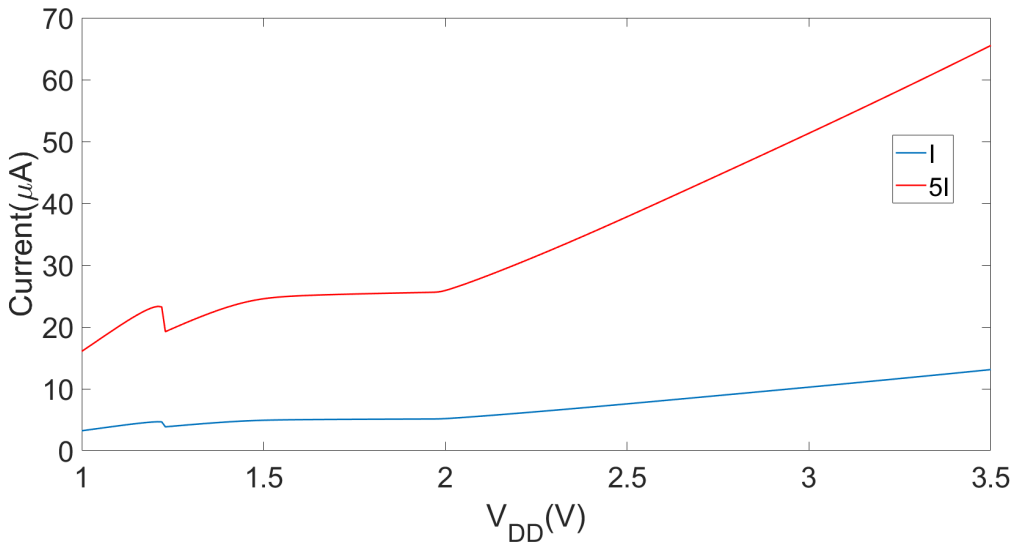

Figure 2.14. Supply voltage dependence of the current reference.

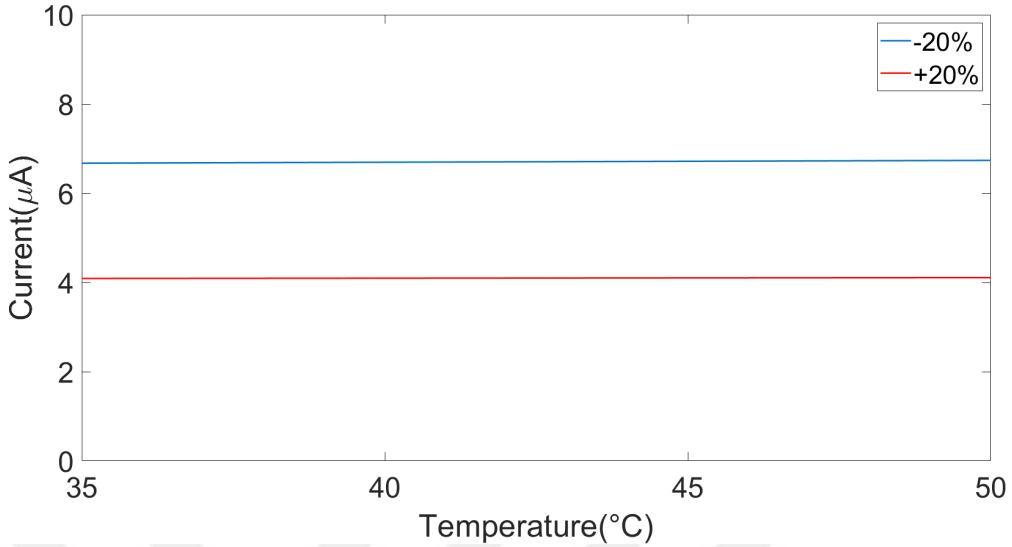

Figure 2.15. Effect of the process-sensitivity of the resistor over the current reference.

Sigma-delta ADC can be considered as the best option for temperature measurements since temperature changes slowly and sigma-delta ADC's are accurate, but slow. The desired resolution can be obtained easily for a relatively low sampling rate and power consumption. The sensitivity of component mismatches is lower than other ADC types [35].

2.3.1. General Requirements

Digitization of temperature readings should be handled based on Equation (2.21).

$$\frac{V_{PTAT}}{V_{ref}} = \frac{N}{M} \tag{2.21}$$

where N is the number of ones in bit sequence and M is the total number of bits. The ratio of $\frac{N}{M}$ should be multiplied by a number in the decimation filter. Since the design is based on the absolute temperature, another number should also be added to the filter to obtain data in degrees Celcius.

Errors bound can be calculated based on the corrected simulations of the differential diodes structure in the CMOS library in Figure 2.8. The full-range of the sensor is between 30°C and 60°C, which covers from 0V to 1.4V. The change of 41.5mV for V_{PTAT} corresponds to one degree Celcius temperature change. Maximum error of 4.2mV, 0.1°C error, in V_{PTAT} can be tolerable. Corresponding error bounds for ΔV_d, V_d and α can be expressed as

$$\begin{aligned} (\Delta V_d)_{absolute\,error} &< 16.4\mu V \\ (V_d)_{absolute\,error} &< 151.9\mu V \\ \alpha_{percentage\,error} &< 3.7\%. \end{aligned} \tag{2.22}$$

These errors are calculated based on 0.1°C maximum error for the required minimum sensitivity of 1°C.

The concerned range of temperature is between 35°C and 50°C and the designed model is capable of measuring temperature between 30°C and 60°C. This range is 20-fold lower than the full absolute temperature range from –273°C and 327°C; therefore, the method increases the resolution of ADC by a factor of 20. For 0.1°C maximum error, ENOB is 7.64. This relatively low ENOB can ease the design of the overall ADC. The bandwidth required is also quite low for temperature measurements since the signal can be considered as a DC signal.

Analog-to-digital converters can be classified into two types in terms of their operation. Some ADCs such as flash ADCs and successive-approximation ADCs divide the reference voltage into quantization levels and digitize the input by comparing it to these levels. Even though they provide high-speed conversion, the performance of these ADCs mainly depends on the component mismatches. Sigma-delta ADCs and dual slope ADCs convert the ratio of the input signal to the reference voltage into a time-domain variable. These ADCs utilize clocks whose frequencies are much higher than the conversion rate of the signal. Their performance is more immune to

the component mismatched compared to the first type of ADCs; however, they do not provide a high-speed conversion. Since the temperature sensing does not require a fast conversion, sigma-delta ADCs are highly exploited in the temperature sensor designs [16] [17] [11].

Sigma-delta ADC can be utilized in synchronous or asynchronous mode. The latter one exploits a comparator with a hysteresis loop. On the other hand, synchronous mode ADC requires a clocked-comparator. The main advantage of the synchronous one is its immunity to the periodic interference [21].

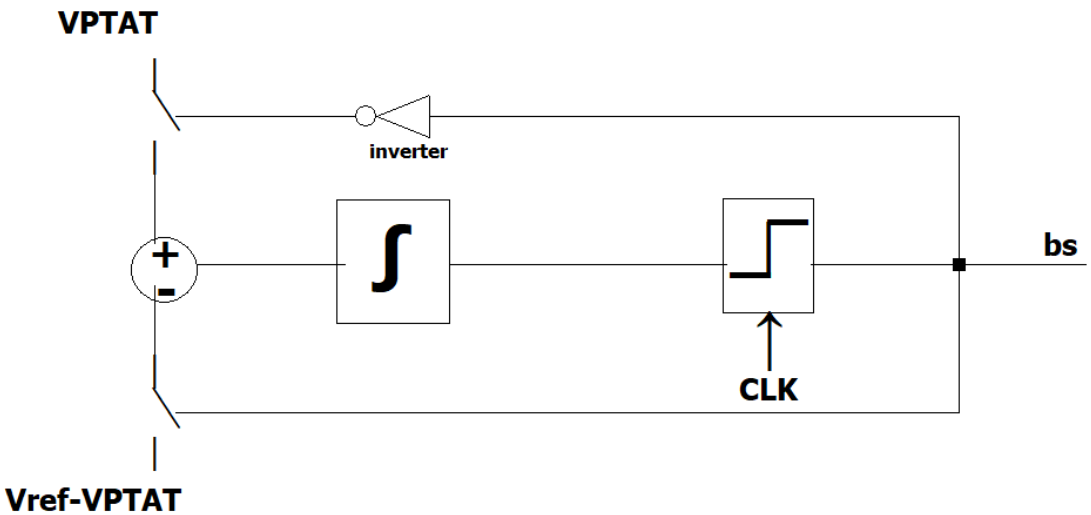

Figure 2.16. Block diagram of the first-order $\Sigma - \Delta$ modulator.

Conversion of the sigma-delta ADCs, which are closed-loop ADCs, is based on the principle of charge balancing. The first-order $\Sigma - \Delta$ modulator mainly consists of a first-order loop filter, integrator, and a clocked comparator as seen in Figure 2.16. When the output of the comparator, bitstream b_s, is zero, V_{PTAT} will be integrated. If b_s goes to one, the integration will be done for $-(V_{ref} - V_{PTAT})$. The negative feedback

will force charge-balancing and it can be illustrated as

$$N(V_{ref} - V_{PTAT}) = (M - N)V_{PTAT}. \tag{2.23}$$

This equation simplifies to Equation (2.21) to find out the ratio of ones in the bitstream.

2.3.2. Analysis of the Operation

Analog-to-digital converters mainly exploit two functions: sampling and quantization. Sampling requires a sampling frequency f_s that is at least two times the signal bandwidth B to eliminate aliasing, Nyquist Criterion. Quantization introduces noise to the system which is modeled as white noise. If f_s goes beyond the Nyquist frequency, this noise will distribute over a wider region; therefore, its magnitude will decrease as observed in Figure 2.17.

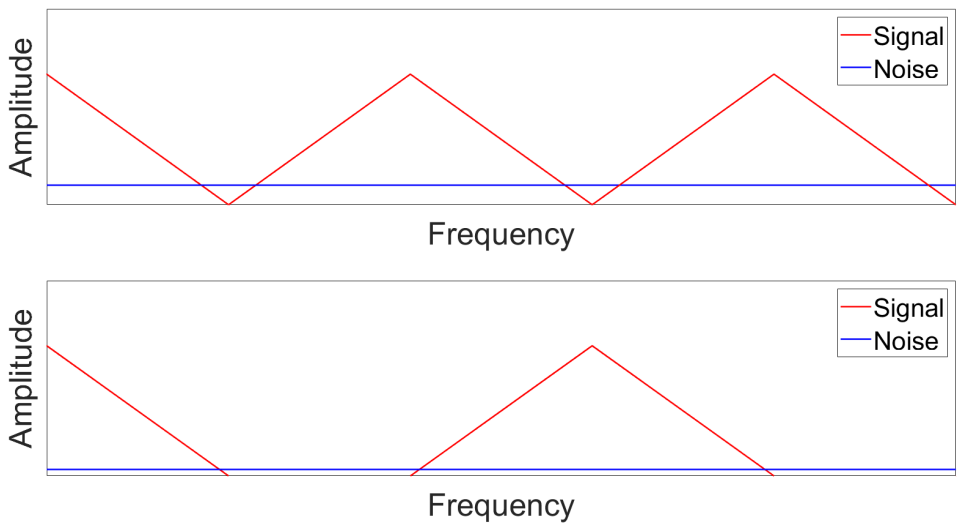

Figure 2.17. Signal and noise spectrums for the Nyquist and oversampling cases.

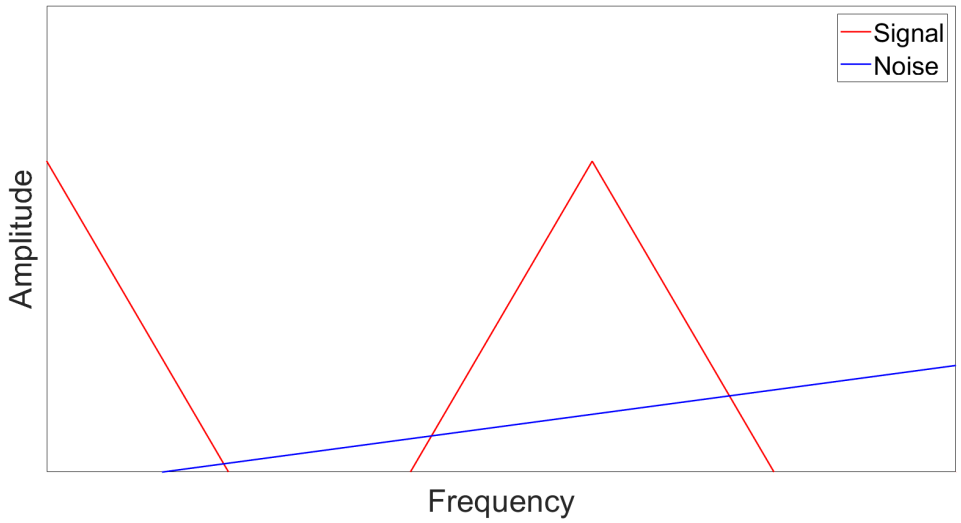

Figure 2.18. Signal and noise spectrums for the noise-shaping oversampling ADC.

The low-pass filter will recover the signal with a lower in-band noise easily since the roll-off of the filter can be smoother, which is easy to implement rather than an ideal square filter response for the Nyquist case. Doubling f_s results in half a bit increase in resolution without noise-shaping.

Noise-shaping oversampling ADCs cause a further decrease in in-band noise as illustrated in Figure 2.18. A two-fold increase in f_s will result in a resolution increase higher than half a bit. A high-speed quantizer is needed for proper performance at high f_s. For one bit case, a clocked-comparator is enough to be utilized as the quantizer. The modulator of the ADC is the integrator for the first-order case. The feedback through the comparator and DAC will shape the noise generated by the comparator. The resolution of a sigma-delta ADC can be developed by increasing the order of the loop filter, utilizing a multiple bit DAC, and using a higher oversampling ratio (OSR), which is $\frac{f_s}{2B}$. The performance of sigma-delta ADC highly depends on the linearity of DAC. Therefore, a one bit DAC, which is a switch, is preferred. The use of higher-order loop filters can also result in instability issues. First or second-order loop filters are acceptable for biomedical applications. Oversampling ratio does not need to be so high

for the temperature sensor whose frequency is quite low and which requires moderate ENOB. The integrator can be DT or CT form. One of the advantages of the CT case is sampling held before the integrator due to the sample-and-hold action. Thus, the loop filter behaves also as an anti-aliasing filter. Its power consumption is generally lower than the DT case since the DT case requires a higher slew rate and leads to impulsive changes at the outputs of the integrator. However, the DT case can operate in various sample frequencies. In addition, the input range and the common-mode rejection ratio are higher than the CT counterpart.

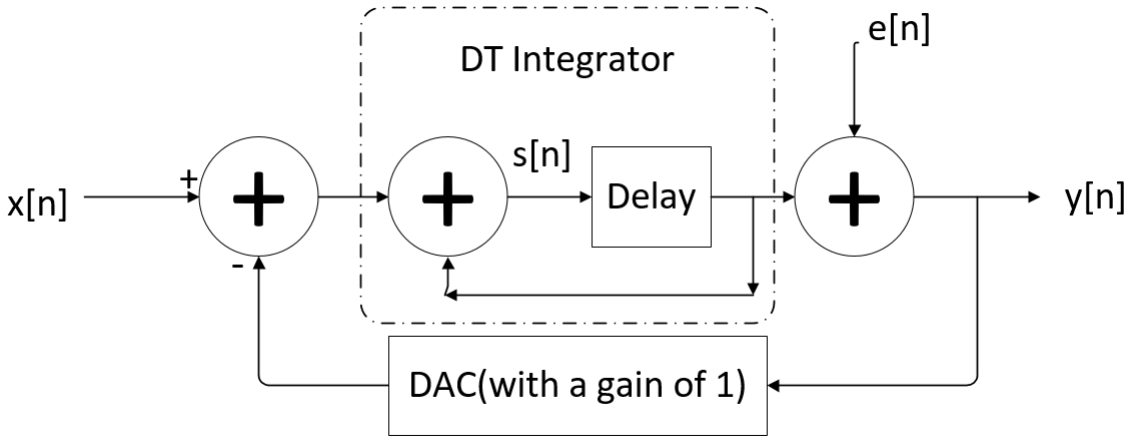

Figure 2.19. Block diagram of the first-order DT $\Sigma - \Delta$ ADC.

The transfer function of the basic DT first-order sigma-delta ADC can be derived easily from the block diagram in Figure 2.19 in which the DT integrator is modeled as the combination of an addition and delay blocks and $e[n]$ symbolizes the quantization error

$$\begin{aligned} s[aT_s] &= x[aT_s] - y[aT_s] + s[aT_s - T_s] \\ y[aT_s] &= e[aT_s] + s[aT_s - T_s]. \end{aligned} \tag{2.24}$$

By writing the intermediate signal $s[aT_s]$ in terms of the input and the output,

$$y[aT_s] = x[aT_s - T_s] - e[aT_s - T_s] + e[aT_s]. \tag{2.25}$$

By taking z-transform of Equation (2.25), resulting responses are

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z). \tag{2.26}$$

The input voltage experiences just a delay; however, the transfer function of the noise is a high-pass response. That is a simple case of how sigma-delta ADCs can shape the noise without disturbing the signal. It should be noted that realistic designs have different transfer functions including gains and nonidealities of blocks; but, they still have negligible distortion of the signal and high-pass noise transfer function.

First-order sigma-delta ADC designed in this thesis for temperature measurement is different from designs used in audio band applications. The ADC operates continuously and digitizes the alternating current (AC) signal overlaid with white noise in the latter one. However, the temperature signal is a DC signal; therefore, the noise is concentrated on some tones rather than having a uniform distribution over the band [36]. For the AC signal case, SNR is the most important performance parameter. For the DC signal case, the linearity of the design is the measure of proper functionality. The modulator will measure the temperature at some intervals, then it is reset until the next measurement.

2.3.3. First-Order Switched-Capacitor Sigma-Delta ADC

The block diagram of a first-order switched-capacitor (SC) sigma-delta ADC was already illustrated in Figure 2.16. The integrator gain is an important parameter since it controls the saturation of the output voltage of the integrator. Linearity of DAC is

no longer an issue since the design exploits one bit DAC, a switch. The comparator decides which voltage will be integrated based on its inputs at the negative edge of its clock. Even though SNR is not as important as in the AC signal case, it still shows the 20dB/decade slope up to $\frac{f_s}{2}$ for the noise in addition to some tonal peaks. Information after $\frac{f_s}{2}$ is just an attenuated replica of the baseband spectrum over intervals whose length is f_s due to the periodic action of the switched-capacitor. Arbitrary tonal noise contributions and periodic bitstreams for a DC signal, which is called a limit cycle, can degrade the resolution. Periodic bitstreams are destroyed by the superposition of very small amplitude sinusoidal signals to the input [37]. These arbitrary noisy elements disturb the undesired periodic patterns; therefore, the resolution is recovered out of the loss associated to limit cycles.

The required clock frequency for sigma-delta ADCs depends on the conversion time and ENOB. For instance, 0.25s conversion time with 10 bits modulator requires about 4kHz sampling frequency. The desired resolution determines ENOB and SNR. The order of the modulator l, number of quantization bits n ,and OSR are chosen based on ENOB and SNR requirements according to Equation (2.27) [26]

$$\begin{aligned} SNR[dB] &= 1.76 + 3.01(\log_2(2l+1) - 2l\log_2\pi + (2l+1)\log_2 OSR + 2(n-1)) \\ ENOB &= \frac{SNR[dB] - 1.76}{6.02}. \end{aligned} \tag{2.27}$$

Maximum quantization error of 0.1°C over 30°C full range means 300 levels of quantization for the subsequent ADC, resulting in 8.23 bits resolution. According to Table 2.1, OSR is chosen as 256 for a first-order one-bit ADC to obtain 11.24 bits resolution considering possible losses.

The integrator open-loop gain is a limiting issue in a first-order switched-capacitor sigma-delta ADC. Relatively low open-loop gains block capacitors to fully discharge together with charge injection through switches. If an operational transconductance amplifier (OTA), which is the core of the integrator, had a gain of around 1000, the

Table 2.1. SNR and ENOB for combinations of l, n, and OSR.

l	n	OSR	SNR	ENOB
1	1	32	41.74	6.64
1	1	64	50.77	8.14
1	1	128	59.80	9.64
1	1	256	68.83	11.14
1	1	512	77.85	12.64
2	1	32	64.12	10.36
2	1	64	79.17	12.86
2	1	128	94.22	15.36
2	1	256	109.27	17.86
2	2	32	70.14	11.36
2	2	64	85.19	13.86
2	2	128	100.24	16.36
2	2	256	115.29	18.86

first-order design could provide ENOB of 10 bits with 256-512 OSR [21].

Switched-capacitor differential sigma-delta modulator is depicted in Figure 2.20 and the nonoverlapping clocks Φ_1 and Φ_2 are illustrated in Figure 2.21. In the phase Φ_1, voltage difference $V_{in1} - V_{in2}$ is sampled on C_1 with respect to the operational amplifier (opamp) offset. Voltage at terminals of the opamp switches to $V_{in2} - V_{in1}$ with respect to the opposite of the opamp offset and it is integrated through C_2 during Φ_2. The corresponding output voltage is

$$\begin{aligned} Vint &= \frac{C_1}{C_2}((V_{in1} - V_{in2} - V_{offset}) + (V_{offset} - V_{in2} + V_{in1})) \\ Vint &= \frac{C_1}{C_2}2(V_{in1} - V_{in2}). \end{aligned} \tag{2.28}$$

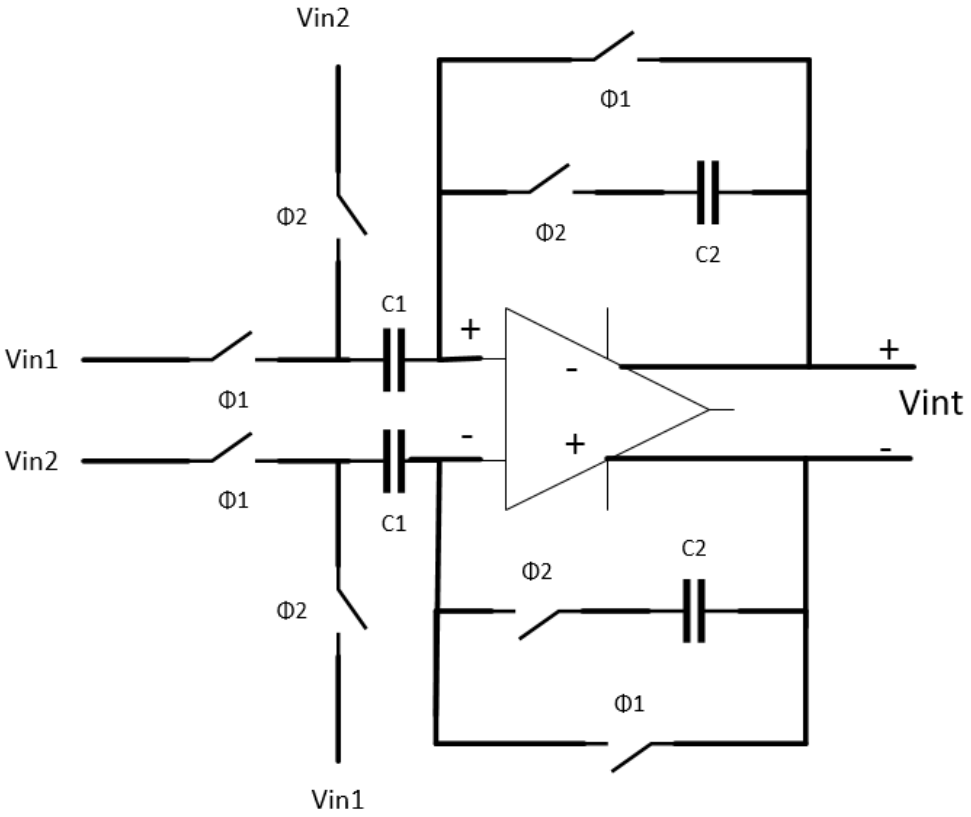

Figure 2.20. Switched-capacitor $\Sigma - \Delta$ modulator.

Opamp's offset and 1/f noise are canceled out up to $\frac{f_s}{2}$ by using the differential approach with a switching network, which is called correlated double sampling (CDS) [38].

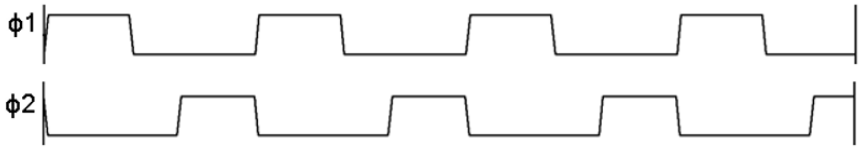

Figure 2.21. Nonoverlapping clocks.

2.3.4. Capacitors in CMOS Technologies

Two types of capacitors in standard CMOS libraries are MOS and MIM capacitors. Metal oxide semiconductor capacitors provide higher capacitance per area; however, their capacitance value is highly affected by the applied voltage up to a factor of four to five [39]. The linearity is crucial for PTAT smart sensors; therefore, MIM capacitors are utilized due to their linearity at the expense of area. However, the designed system requires capacitance values in the Femto range. Thus, the area consumption is not as high as expected in the first place.

Diodes, switches, capacitors, the opamp, and the comparator all contribute to the noise of the overall system. Possible process mismatch for diodes is eliminated via dynamic element matching through switches as shown in Figure 2.33. Dominant noise contributions are kT/C noise and 1/f noise. 1/f noise is alleviated by CDS. kT/C noise determines the speed of the operation. Lower noise can be attained by larger capacitances, trading off speed and area against noise. Bias current also affects the noise. However, it trades off noise magnitude with noise bandwidth [21]. Therefore it does not affect the noise power. In addition to the power budget, the constraint for the current due to the settling of the voltage across sampling capacitors [21] and bounds for capacitance values due to kT/C noise and area do not leave so much space to play with these values.

2.3.5. Integrator in Sigma-Delta ADC

The integrator in the block diagram of the sigma-delta ADC is a fully differential folded-cascode OTA design similar to [40] [24]. It provides low power operation and it does not have any stability issues as opposed to a two-stage Miller OTA. On the other hand, it has lower output swing compared to the two-stage Miller OTA. Even though a telescopic cascode consumes less power, input and output swings are reduced further. Also, it is very difficult to make output and input DC ranges compatible with each other, severely limiting the use of telescopic cascode OTAs in feedback systems.

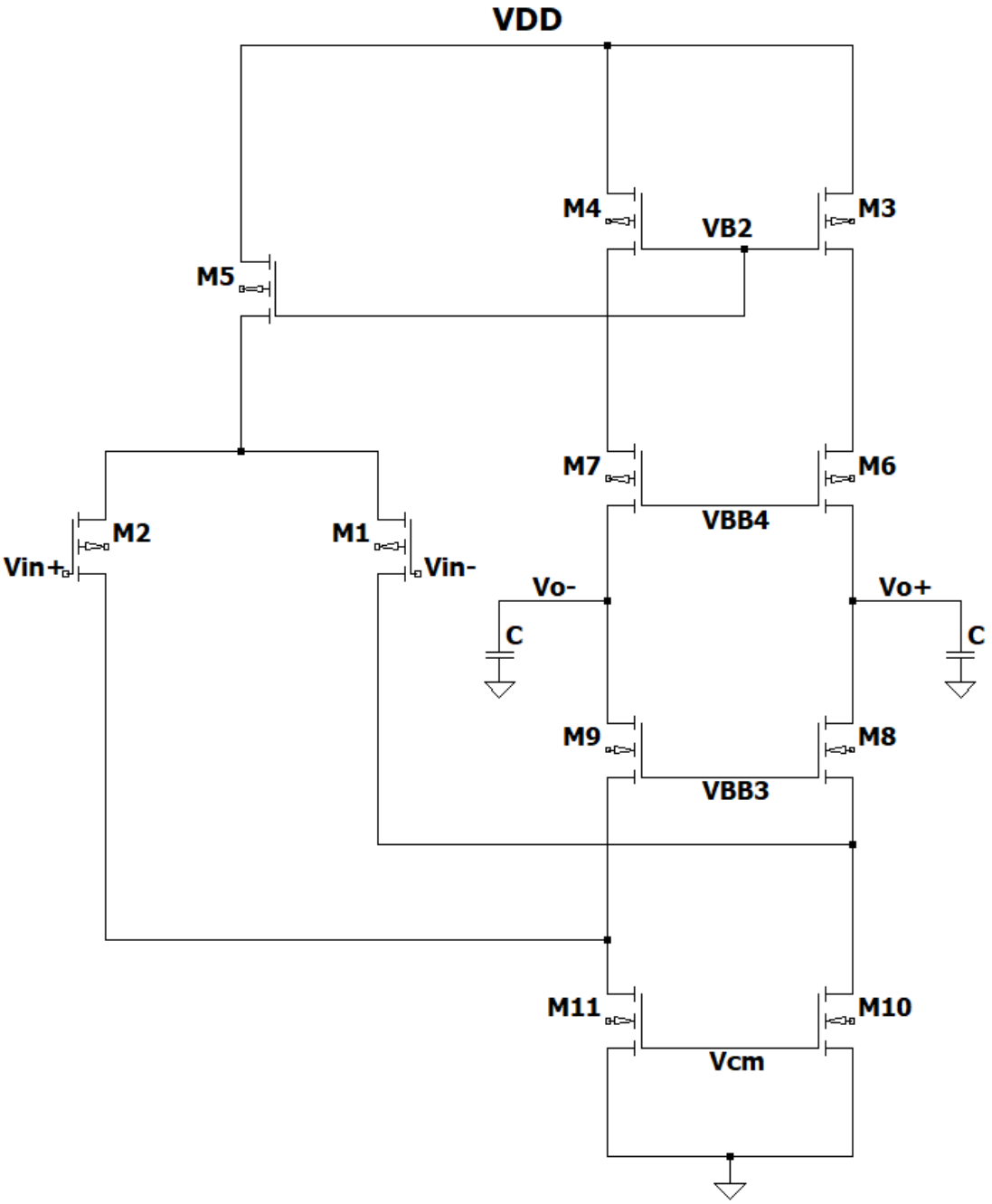

Figure 2.22. Schematic of folded-cascode OTA.

The schematic of a folded-cascode OTA is illustrated in Figure 2.22. M5 is the current source for the PMOS input stage. M3-M4 and M10-M11 are current sources and current sinks, respectively. M6-M7 and M8-M9 are current buffers that increase the output resistance. Transistors should be biased accordingly. Fully differential

OTAs require common-mode feedback (CMFB), which brings the circuit back to the desired state. Common-mode signals can be sensed in various ways: a resistor divider, differential MOS transistors, a MOS transistor in a triode region. These methods degrade the output swing of the OTA by resistive loading. Therefore, a SC CMFB design was implemented since it eliminates the resistive loading of the OTA. Common-mode signals control the gate voltage of the current sink, M10-M11, of the input stage. The deviation of the common-mode of the output voltage is eliminated by the negative feedback through CMFB.

Biasing circuitry and CMFB are shown in Figure 2.24 and Figure 2.23, respectively. Layouts of OTA, CMFB, and bias circuit are illustrated in Figure 2.25, Figure 2.26, and Figure 2.27.

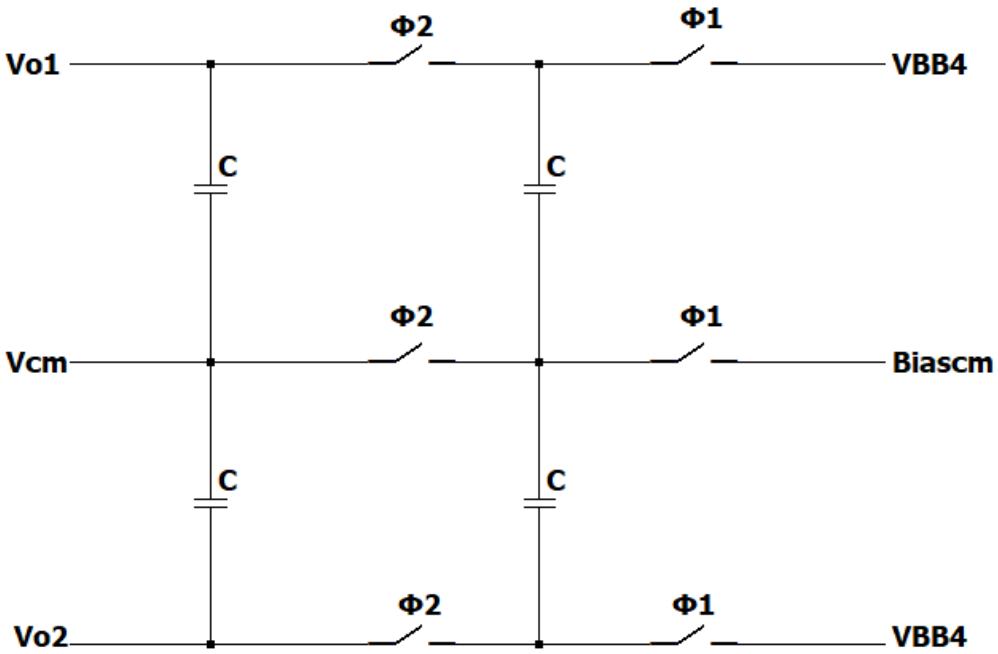

Figure 2.23. Schematic of CMFB.

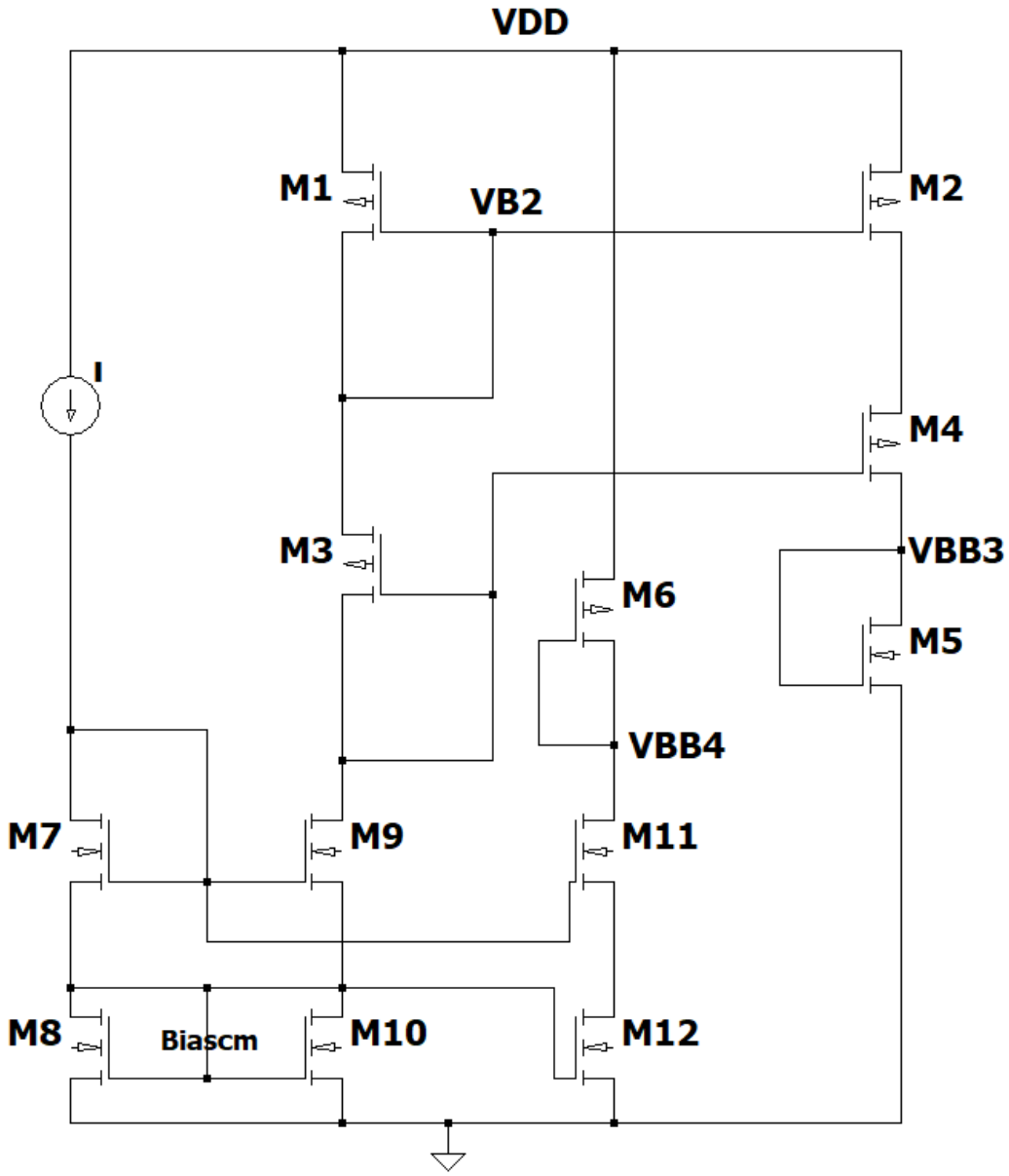

Figure 2.24. Schematic of bias circuit.

The AC simulation of an OTA in an open-loop connection should be handled by connecting very large inductors through negative feedback. The resulting AC simulation is shown in Figure 2.28. The gain is around 1000 (60dB); therefore, it can be exploited in nine to ten bits sigma-delta ADC design as mentioned before. Transient simulation of the OTA is performed to show that CMFB operates as expected. For

0.5mV input, the output in the transient simulation can be analyzed in Figure 2.29. The common mode voltage of the two outputs is around 0.764V after 20μs.

2.3.6. Clocked-Comparator

Implementation of the clocked-comparator includes a preamplifier and a following cross-coupled latch [21] as shown in Figure 2.30. The negative edge comparator generates bitstreams after a NOR operation to outputs of the dynamic latch.

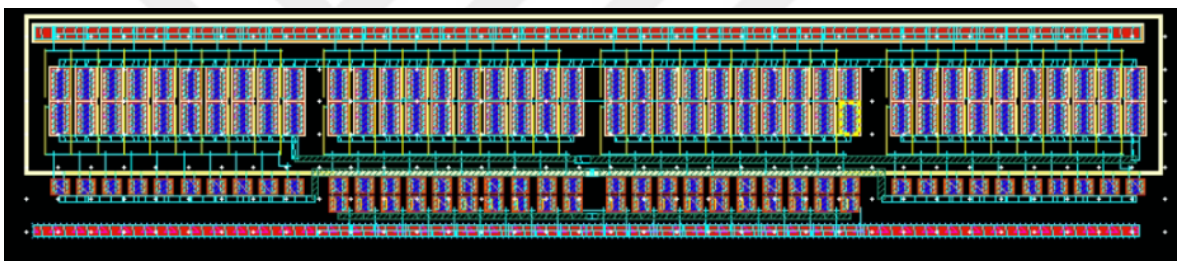

Figure 2.25. Layout of OTA.

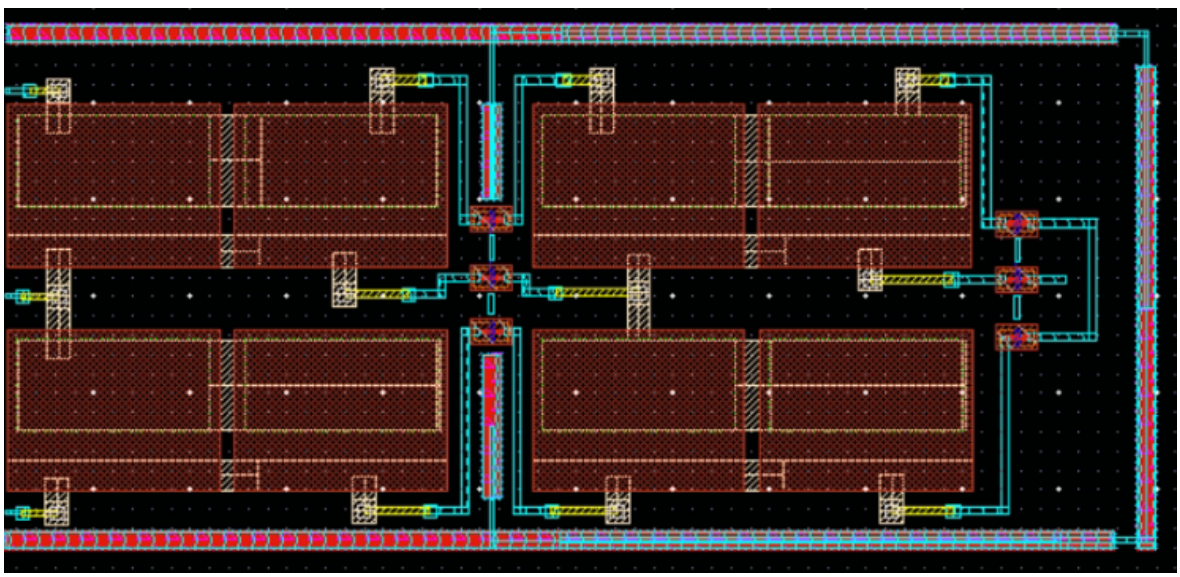

Figure 2.26. Layout of CMFB.

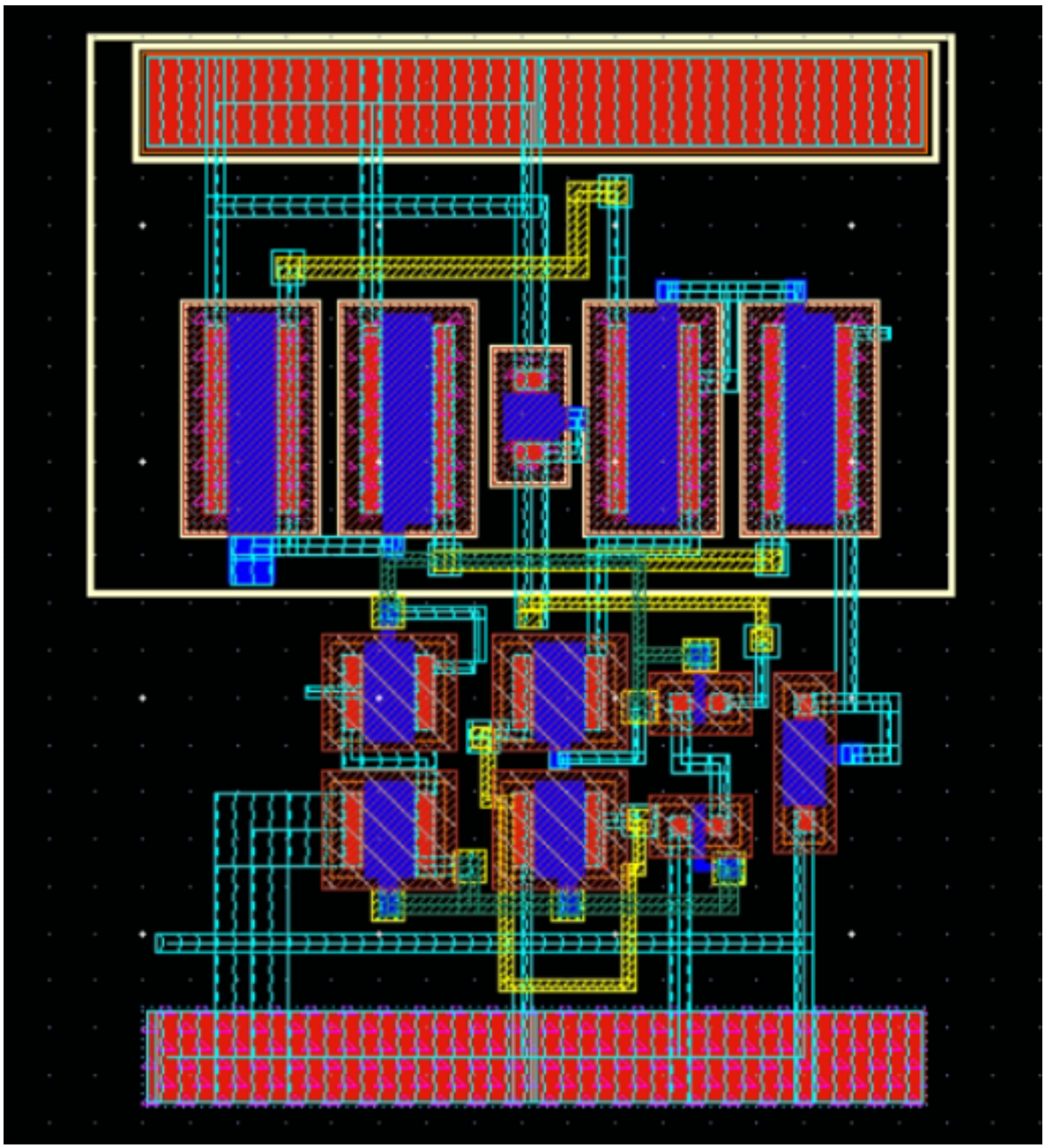

Figure 2.27. Layout of bias circuit.

For the response time of this negative-edge triggered comparator, a slowly changing input with reference to a constant input is applied to the system as shown in Figure 2.31. The comparator senses differences down to 300μV voltage which is quite acceptable for this temperature sensor design. The layout is depicted in Figure 2.32.

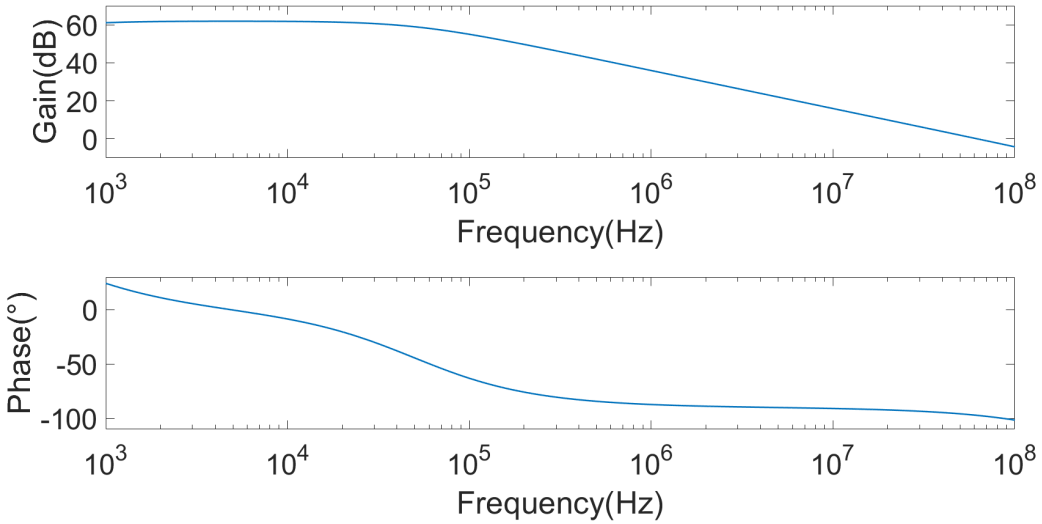

Figure 2.28. AC simulation of OTA.

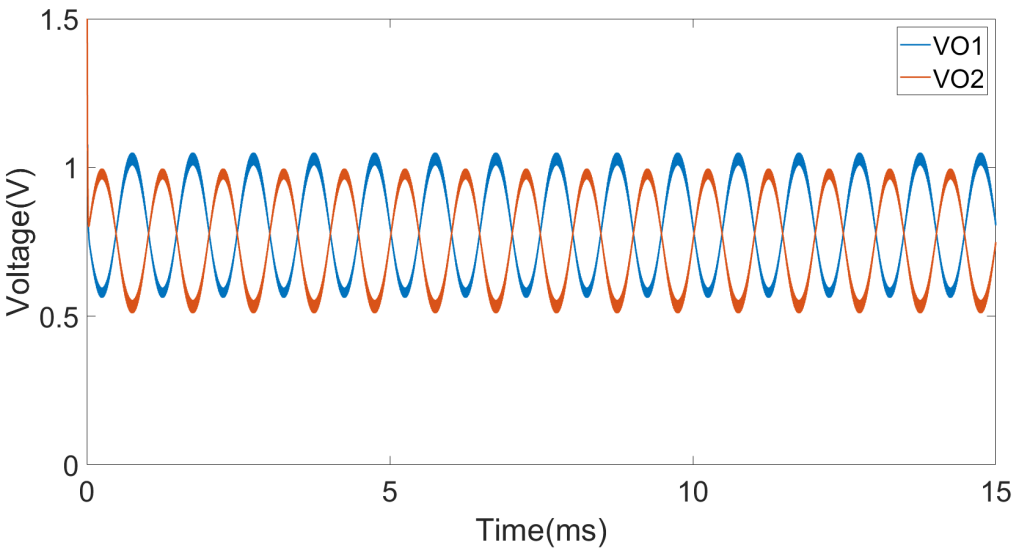

Figure 2.29. Transient simulation of OTA for 0.5mV input.

2.4. Proposed Design of the Temperature Sensor

The reference voltage and the PTAT voltage are not exclusively generated in the design. The main novelty is to decrease full-scale to much lower values compared to [17]

[18] without using any complex circuitry. Full-scale temperature range around 30°C can be easily obtained through different sampling MIM capacitors and the integration of a new clock Φ_3 that can be easily obtained from clock generation circuits.

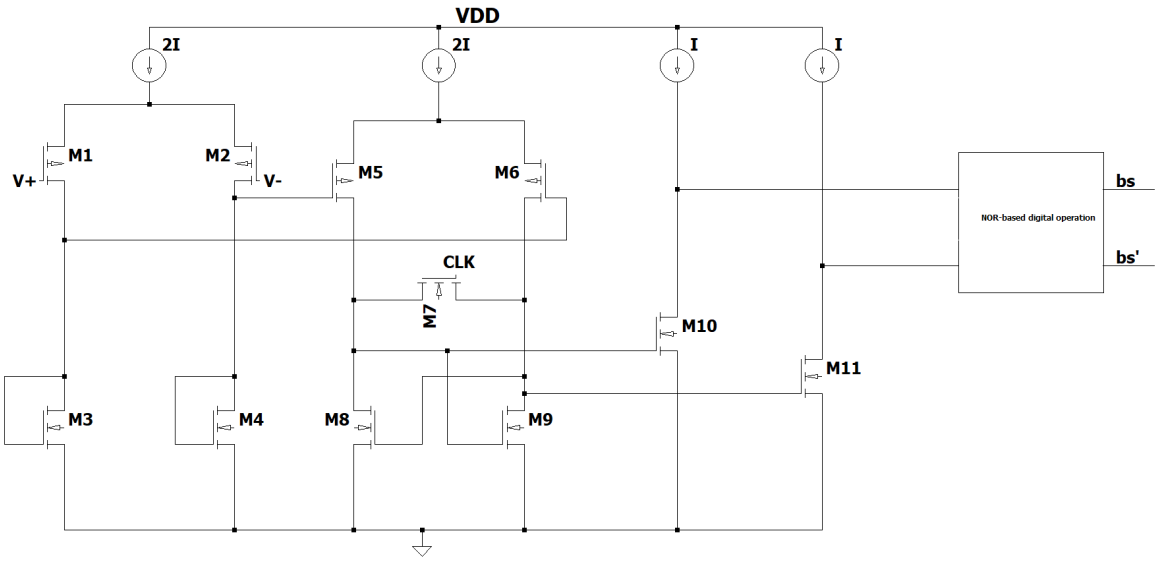

Figure 2.30. Schematic of the clocked-comparator.

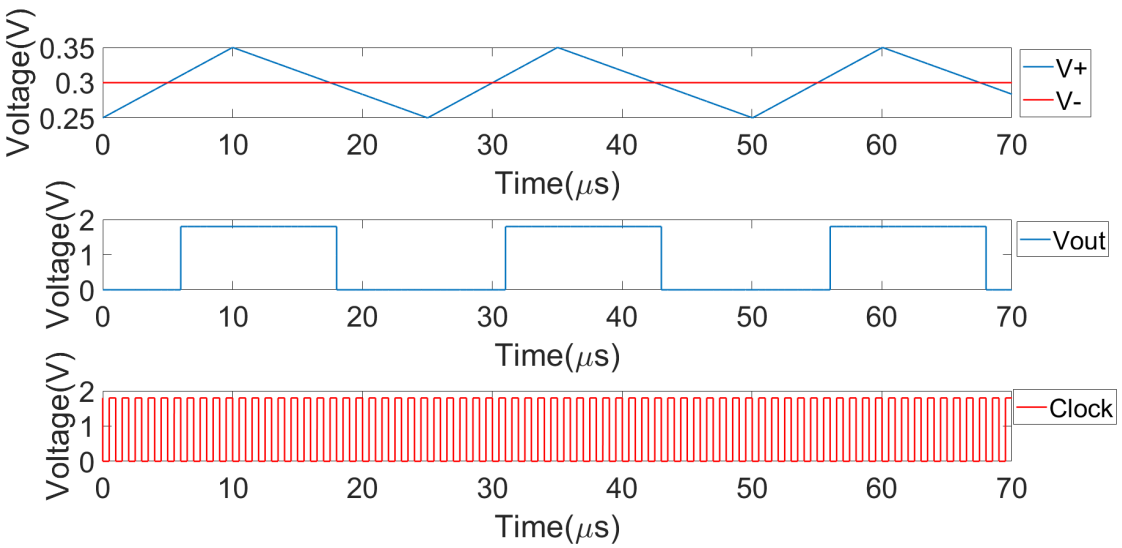

Figure 2.31. Simulation of the clocked-comparator.

The full-scale range can be adjusted to any region depending on the specifications of a design by just changing sampling capacitors. Therefore, that enables the use of the proposed design in different operations.

The overall circuitry and required clocks are depicted in Figure 2.33 and Figure 2.34. When we focus on the first part of the design, current sources are temperature-insensitive current references that are mirrored for 5:1 ratio. The switching network is controlled by non-overlapping clocks Φ_1 and Φ_2; therefore, they switch I and $5I$ to diodes *D1* and *D2* in accordance with these clocks. That is a dynamic element matching that eliminates possible mismatch errors due to diodes.

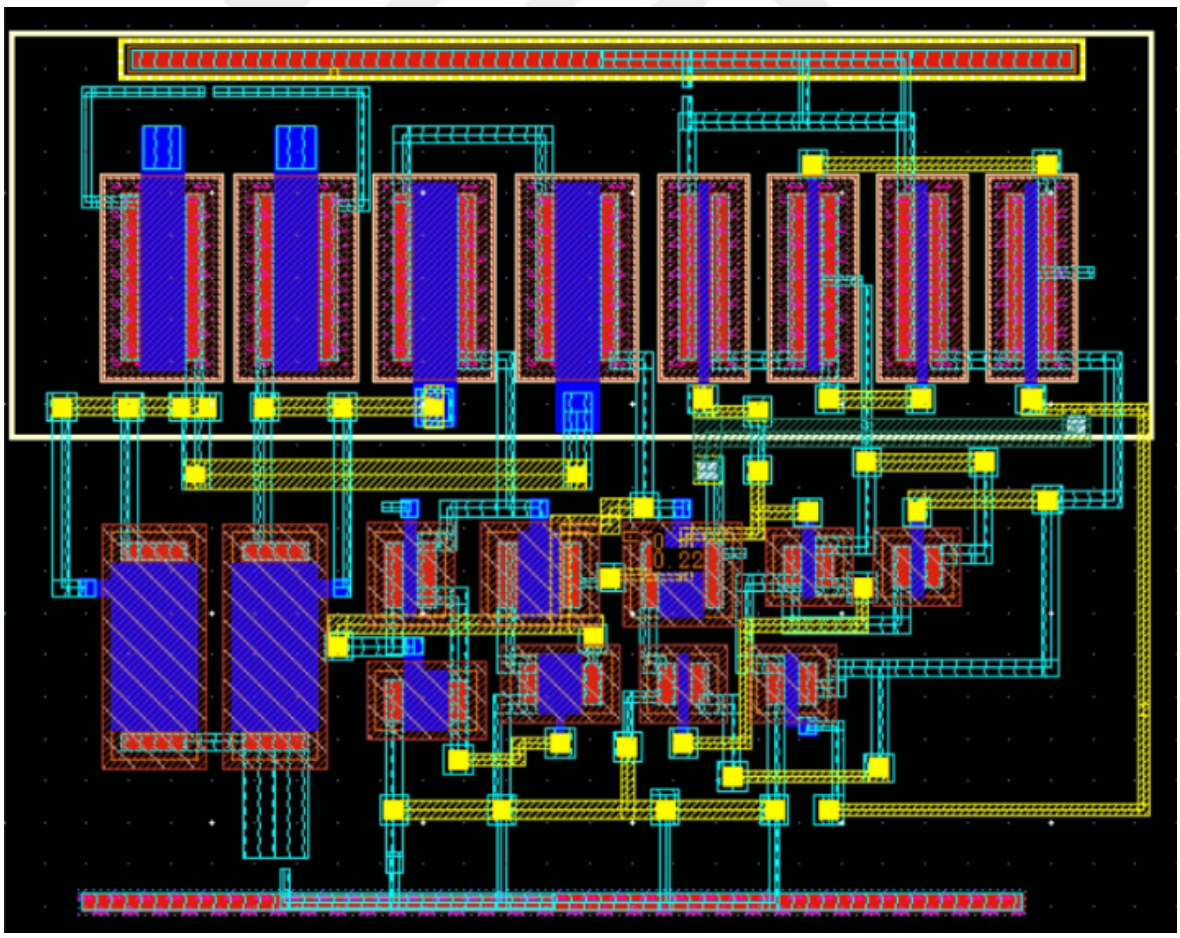

Figure 2.32. Layout of the clocked-comparator.

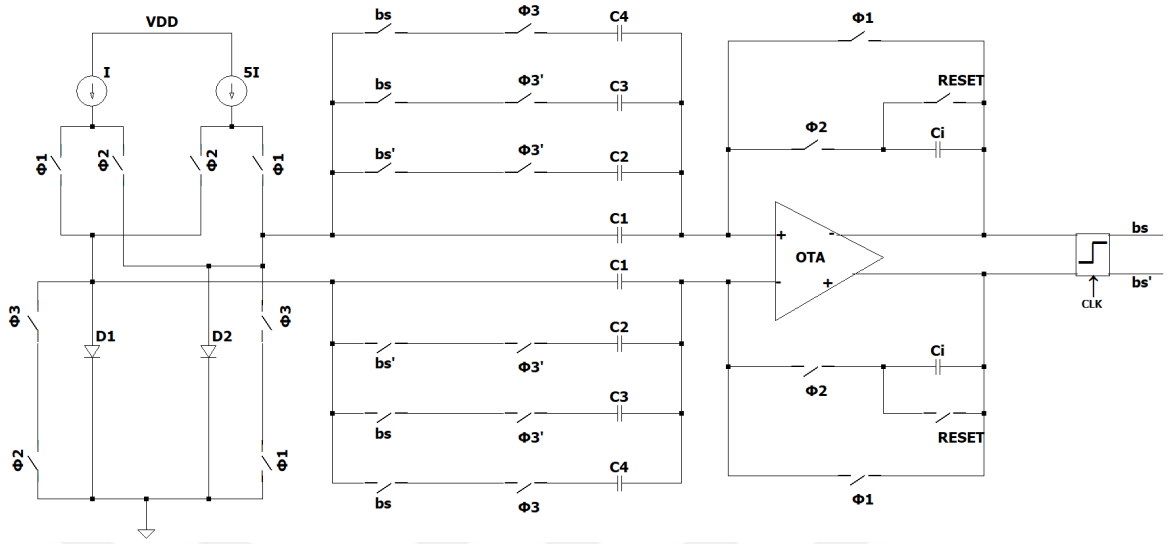

Figure 2.33. The overall circuitry.

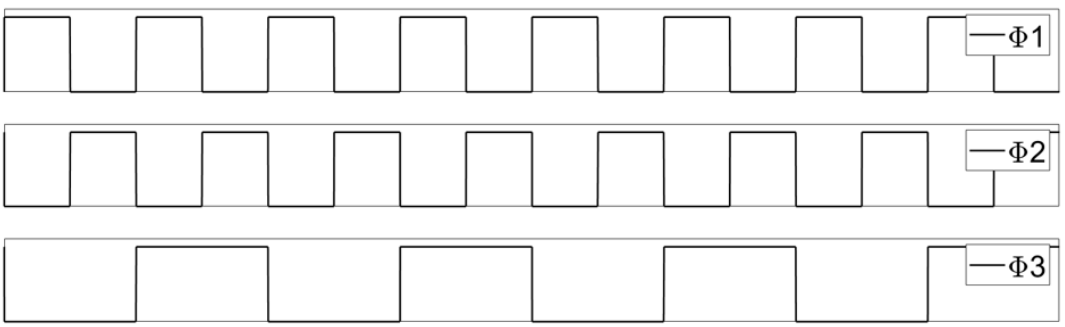

Figure 2.34. Required clocks for the temperature sensor.

The switches parallel to diodes are used to generate ΔV_d or V_d at the input of the integrator depending on the combinations of clocks Φ_1, Φ_2 and Φ_3 .

The second part of the design consists of an integrator and a clocked-comparator. The integrator is designed as a fully differential folded cascode amplifier whose open-loop gain is around 1000. The SC approach is utilized for the integrator and its common-mode feedback as mentioned in the previous section. The different sampling MIM capacitors are the most critical part of the design and their paths are controlled by

b_s, the inverse of the bitstream $\bar{b}_s$ and other clocks. Correlated double sampling is used via Φ_1 in the feedback path. The reset switch over the integrating capacitor eliminates continuous power consumption for conversion. The following element is the clocked comparator which generates b_s and $\bar{b}_s$ as analyzed before. Since the temperature signal changes very slowly, the frequency of the comparator's clock can be around 2-3 kHz for 128 to 256 oversampling ratio in applications such as long-term medical sensing. Such a low clock frequency also decreases the power required to generate it and the power consumed by the system; thus, it makes a first-order design acceptable. Nevertheless, the proposed method is still valid for a second-order design as demonstrated in the following chapter.

2.4.1. Operation of the Proposed Temperature Sensor

When nonidealities related to the extrapolation formula, the technology and the components are corrected, x and y values are 9.1 and 11.7 for V_{PTAT}, respectively, to cover between 30°C and 60°C as full-scale. The operation of the proposed SC Σ-Δ modulator can be divided into four phases. When b_s=0 and Φ_3=0, ΔV_d is observed at the integrator's input and it is sampled at the combination of C_1 and C_2 capacitors with respect to the virtual ground of the integrator during Φ_1. In the phase Φ_2, the opamp input experiences -ΔV_d; therefore, the total change in voltage is $2\Delta V_d$ and the static offset and 1/f noise are cancelled. This voltage change is integrated through the integrating capacitor C_i with gain of $\frac{C_1 \| C_2}{C_i}$. The input voltage at the opamp will shift to -V_d during Φ_1 when Φ_3 is high and b_s is still zero. This voltage is sampled at the capacitor C_1. In the Φ_2 phase, the change in the opamp's input will be —$2V_d$ since input voltages are swapped by the switching network. The integration gain in that phase will be $\frac{C_1}{C_i}$. If b_s=1 and Φ_3=0, $2\Delta V_d$ voltage change in the integrator's input will experience a gain of $\frac{C_1 \| C_3}{C_i}$ during the process of Φ_1 and Φ_2. When b_s=1 and Φ_3=1, this voltage change returns to —$2V_d$ with an integrating gain of $\frac{C_1 \| C_4}{C_i}$. The comparator changes its output at the negative edge of its clock after the end of phase Φ_3 in order not to affect the operation due to the charge injection. The most important thing is to clearly determine these gains to adjust the full-scale range. The governing equation

is as follows:

$$\frac{9.1(\alpha\Delta V_d) - 11.7(V_d)}{\alpha\Delta V_d + V_d} = \frac{N}{M}. \tag{2.29}$$

By substituting 16 for α the final simple form is reduced to

$$N(129.6\Delta V_d - 12.7V_d) = (M - N)(11.7V_d - 145.6\Delta V_d). \tag{2.30}$$

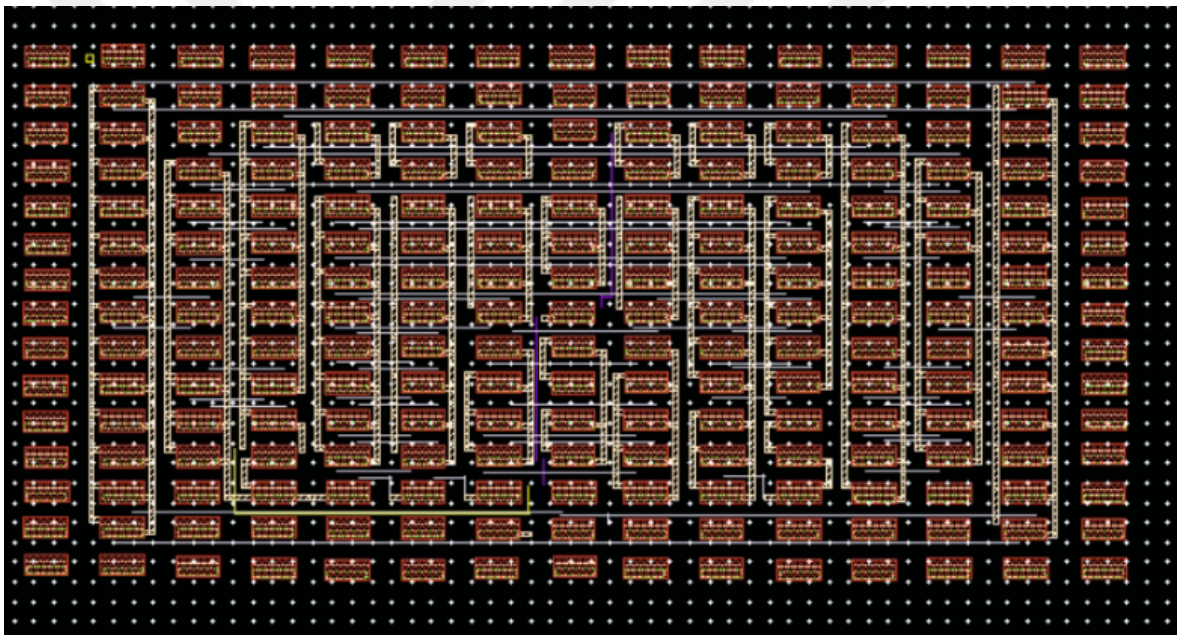

Figure 2.35. Layout of MIM capacitors.

These coefficient values can be obtained by proper adjustment of capacitor ratios. Unit capacitors are exploited to realize sampling capacitors and their layouts are drawn in a common centroid structure to preserve their ratio. The layout of desired capacitors surrounded by unused capacitors to block possible errors due to the layout printing process is shown in Figure 2.35. Even though the process-dependency of MIM capacitors causes deviation of capacitance values, the linearity of MIM capacitors limits the degradation of the performance due to the shift of the full-scale. The corrections

for capacitance values and dynamic element matching will bring the system back to the same range, 30°C- 60°C.

2.4.2. Simulation Results of the Proposed Temperature Sensor

The sensor is designed in 0.18μm technology with MIM unit capacitors for sampling capacitors and with a high-resistive poly resistor for the current reference. Clocks are generated off-chip. The layout of the sensor is illustrated in Figure 2.36. The power spectral density (PSD) of the bitstream of the layout of the sensor can be observed in Figure 2.38. A 7-term Blackman-Harris window is utilized in fast Fourier transform (FFT) since it provides the highest attenuation of side lobes, which is the most important property for ADC characterization [41]. The slope of 20dB/decade can be noticed as it is a first-order noise shaping of the ADC for 40°C case even though some tonal noise peaks occur as expected.

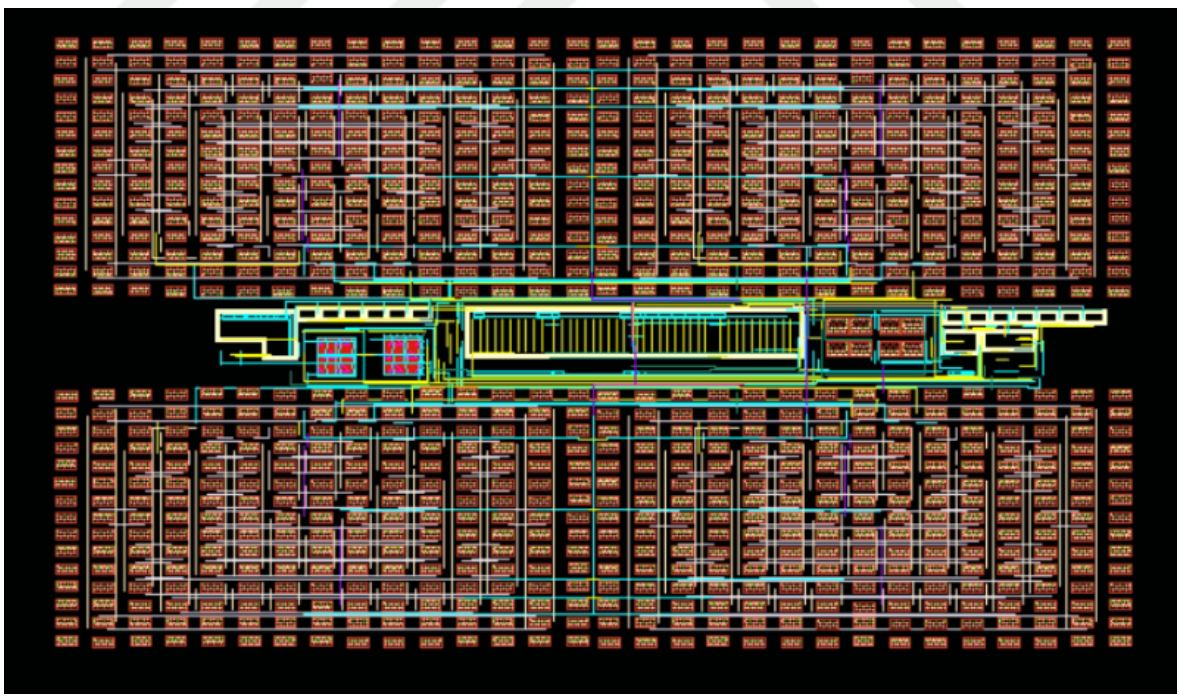

Figure 2.36. Layout of the temperature sensor.

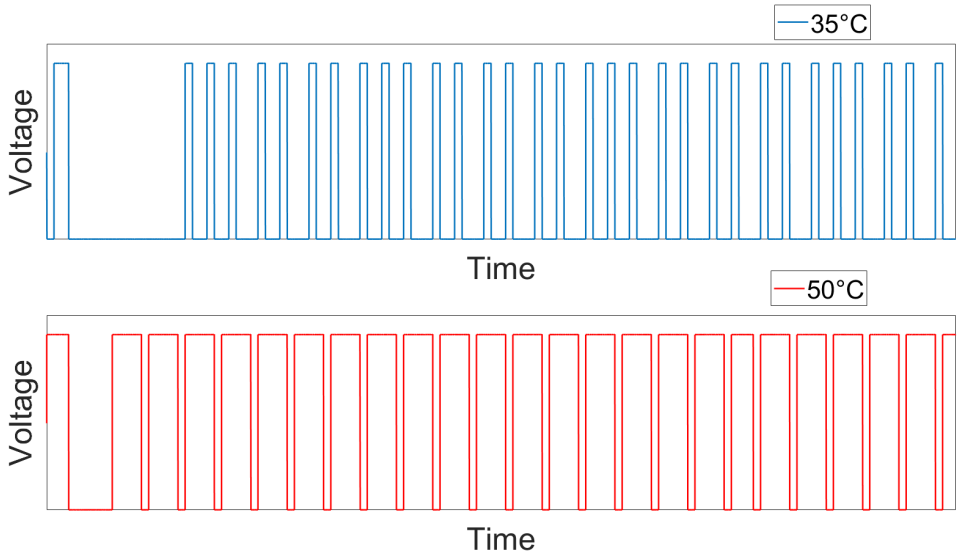

Figure 2.37. Cycles for 35°C and 50°C.

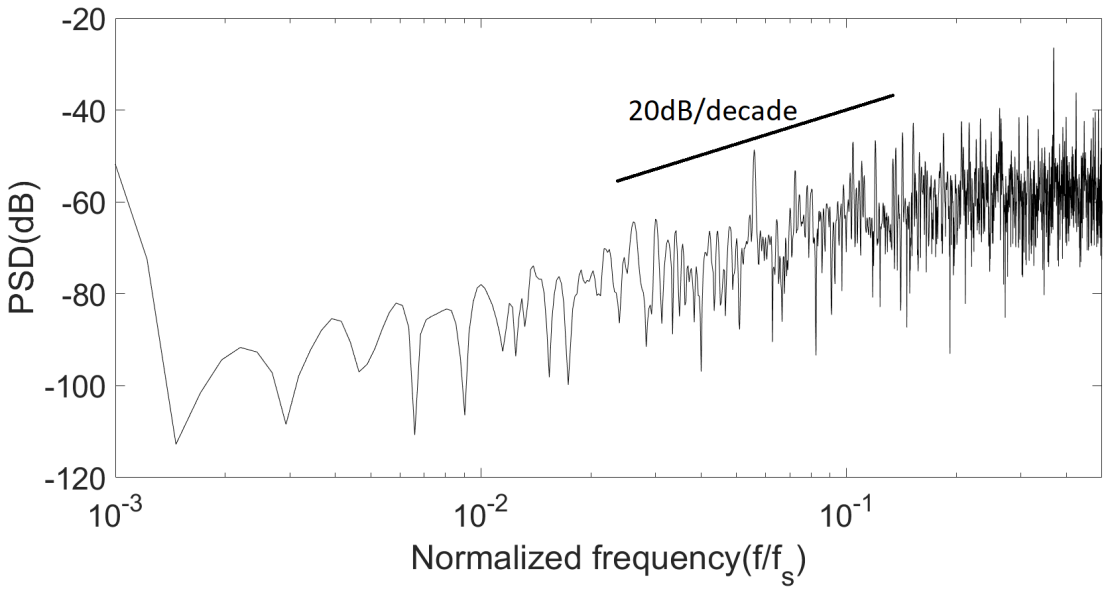

Figure 2.38. Post-layout PSD of the first-order $\Sigma - \Delta$ modulator(16384 points, 7-term Blackman-Harris windowed).

However, the linearity of the ADC is more crucial since a DC signal is applied to the system rather than an AC signal. Bitstream sequences of 35°C and 50°C for 70 clock cycles are illustrated in Figure 2.37. For 1000 cycles, the number of ones

and zeros for different temperatures in the full range can be counted to observe the performance of the temperature sensor. The result is illustrated in Figure 2.39. The corresponding increase in the number of ones in 1000 cycles per degree is 34.5. The linear behavior, which is the critical parameter for the DC sigma-delta ADC case, is obtained as shown in Figure 2.39 inside the full-scale. A decimation filter follows the sigma-delta modulator and reduces the sampling frequency to a lower value. Thanks to this filter, quantization noise is further suppressed. In this thesis, the bitstream is converted to the common weighted binary representation and the number of ones and zeros in the bitstream are counted since the decimation filter is not designed. Nevertheless, the linearity turns out very well.

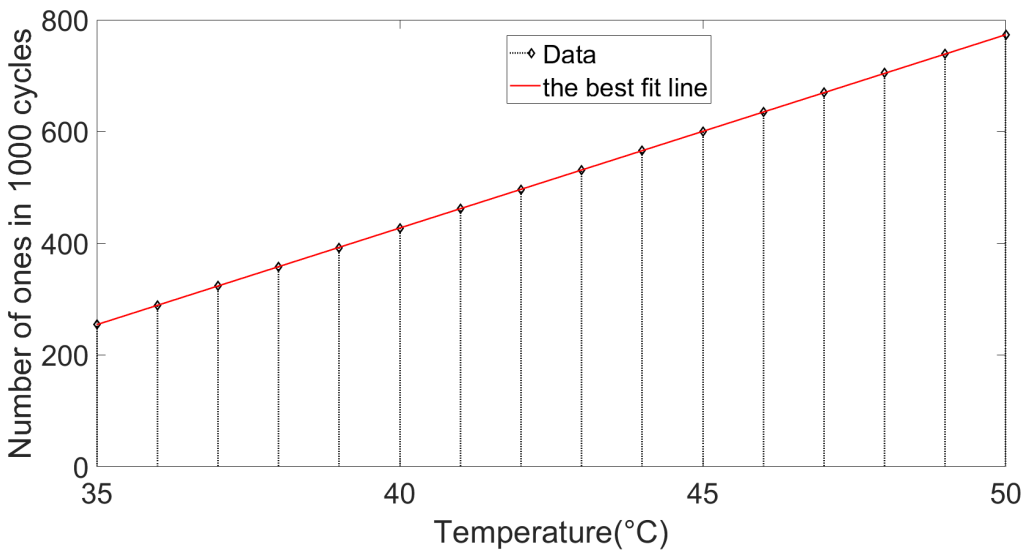

Figure 2.39. Number of ones of corresponding temperatures in 1000 cycles.

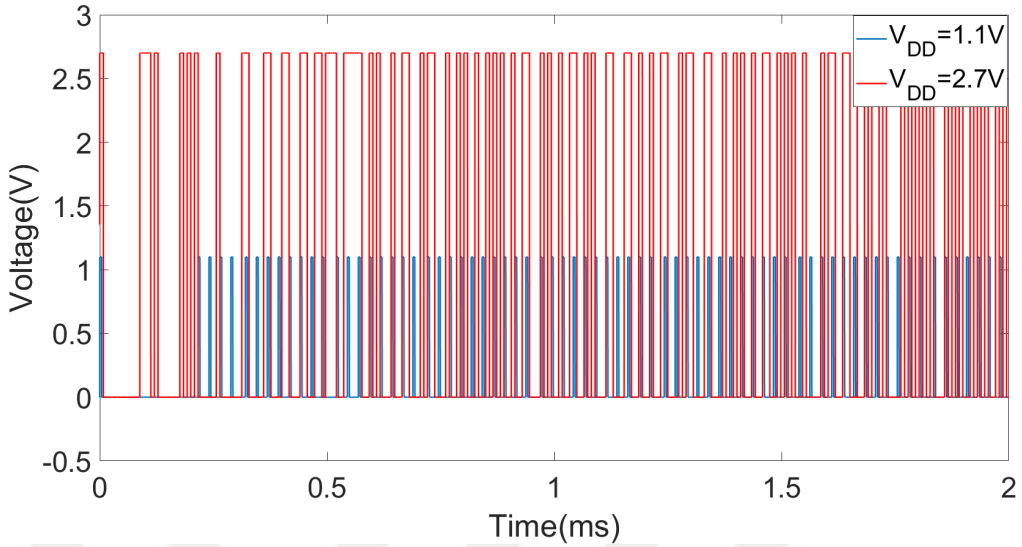

Figure 2.40. Cycles at 35°C for V_{DD}=1.1V and V_{DD}=2.7V.

The circuit operates properly between V_{DD}=1.1V and V_{DD}=2.7V as demonstrated in Figure 2.40. The desired full-scale temperature range has been achieved according to the design specifications. The performance of the proposed temperature sensor is summarized in Table 2.2 and comparison of temperature sensors are shown in Table 2.3.

Table 2.2. Performance Summary of the Temperature Sensor.

Technology	0.18μm CMOS
Layout area	0.18mm^2
Temperature range	30°C- 60°C
Supply voltage	1.1V - 2.7V
Energy required per conversion	828fJ
ENOB	10.20 bits
Resolution	0.03°C

Table 2.3. Comparison of Temperature Sensors.

Reference	Range(°C)	Resolution(°C)	Area(mm^2)	Process
Chen [9]	0-100	0.16	0.175	0.35μm
Tuthill [10]	–55-125	0.25	3.32	0.6μm
Bakker [11]	–40-120	0.625	1.5	2μm
Pertijs [16]	–55-125	0.01	4.5	0.7μm
Pertijs [17]	–50-120	0.03	2.5	0.5μm
Bakker [18]	–40-127	0.25	4.5	0.7μm
Proposed	30-60	0.03	0.18	0.18μm

3. ACOUSTIC SENSOR AND ITS INTERFACE

Dislocation of the hip implant changes the acoustic emission properties of the hip implant. A sound sensor is implemented for early diagnosis of issues related to the hip implant. Sensing is achieved through a differential capacitive microphone. Differential operation eliminates the noise due to the process variation of the microphone. Electret condenser and MEMS microphones are widely exploited in acoustic sensor systems. A MEMS microphone was utilized due to its compatibility with the integrated circuit (IC) design. Differential cantilever performs as the sensing device. The sensor is analytically modeled by varying sensing capacitance and parasitic capacitances whose values are roughly determined by MEMS technology documents. Then, the design is performed using this model rather than the integrated microphone. Full integration of MEMS microphone into IC design is left as a future work since it requires a different level of expertise.

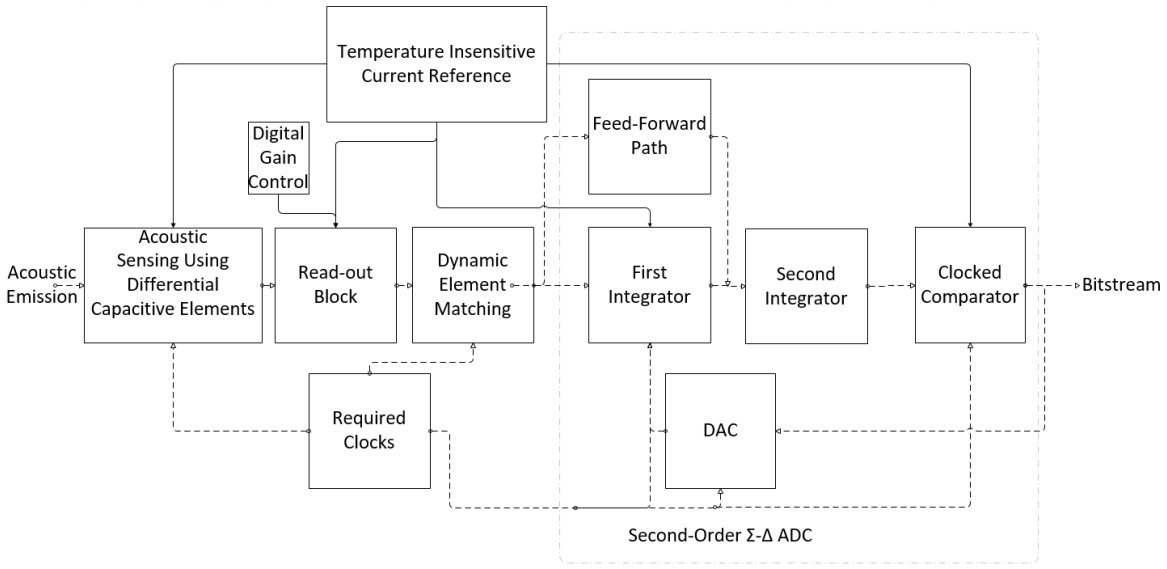

Figure 3.1. Block diagram of the acoustic sensor.

Interface electronics of capacitive sensors can be implemented in various ways. An oscillator-based tuned system can be implemented to sense the capacitive change with the frequency shift of the resonance [42] [43]. A charge transfer method including

a resistor is also utilized as an interface electronic in the literature [44] [45]. In this method, charging time carries the information of the varying capacitor. The charge transfer method can also be utilized with capacitors [46] since the change in charge distribution is a measure of capacitance change. These methods dominate when a direct interface to a microcontroller is required depending on the design specifications. Capacitance-to-voltage converter based on the sigma-delta ADC techniques are also very common [47] [48] [49]. A sigma-delta ADC generally becomes the first choice in biomedical applications where there are numerous noise contributions since this ADC provides noise-shaping. A preamplifier stage is sometimes exploited in addition to the sigma-delta ADC depending on the signal properties. The signal amplitude level of the hip implant [13] requires a preamplifier read-out block to scale the signal to the full range of the ADC. The block diagram of the acoustic sensor is illustrated in Figure 3.1.

The first block is the differential capacitive MEMS sensor as mentioned. The differential AC signals are fed to the preamplifier stage, which includes the read-out block and digital gain control. Digital gain control provides four levels of gain depending on the sensed AC signal magnitude. Digital gain block also enables us to utilize the ADC more efficiently. Read-out DT and CT stages will be analyzed in terms of power. Therefore, we will be able to compare a SC design and a CT design for small and large signals. Dynamic element matching is the same for both cases. For the sound sensor, a second-order sigma-delta ADC is utilized rather than a first-order one. For an audio band system, eight to nine bits ADC is quite acceptable; however, the required OSR necessitates a very high-frequency clock for a first-order design, which consumes a huge amount of power. Therefore, the second-order design is implemented that also minimizes tonal peaks compared to the first-order design. The proposed methodology in Chapter 2 is also applied to the second-order ADC in this chapter to efficiently cover the reference voltage range. The previous ADC does not require an external reference voltage. In this section, two second-order ADCs with and without an external reference voltage will be compared in terms of ADC parameters. Thus, the advantages or disadvantages of a design without a reference voltage [16] will be explored. Switches

have been adjusted accordingly for this system. A feedforward path is added to the second-order system to decrease the swing at the outputs of the integrators. The system is utilized with integrators and the comparator from the previous chapter. The best one out of four design options-combination of two read-out blocks and two ADC types- in terms of power, SNR and ENOB will be exploited in this sensor interface.

3.1. Acoustic Sensing Using Differential Capacitive Elements

Micro electro mechanical systems allow low-cost, small size, and CMOS compatible design [50]. The core of these sensors is a diaphragm that converts the signal from the mechanical domain to the electrical domain. Deflection of the diaphragm can be transduced through piezoelectric, optical, capacitive, and piezoresistive mechanisms.

There are many academic studies about the analysis of MEMS microphones [51] [52] [53] [54]. They are also utilized in implantable human body applications [55].

3.1.1. Analytical Model of Acoustic Sensing Elements

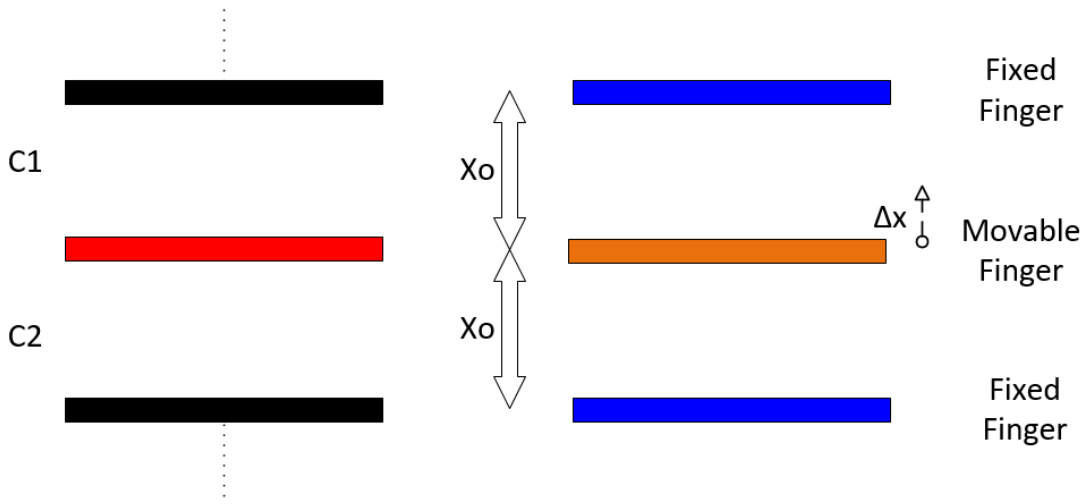

Figure 3.2. Capacitive sensing cell.

A capacitive sensing cell is illustrated in Figure 3.2. The movable finger is free to move up to a point where the pull-in occurs and there is no way back to the proper operation behind this point. However, the deformation Δx is generally too small compared to the distance between a fixed finger and a movable finger x_0. Capacitance values can be represented as

$$\begin{aligned} C_1 &= \frac{\epsilon_0 A}{x_0 - \Delta x} \\ C_2 &= \frac{\epsilon_0 A}{x_0 + \Delta x} \end{aligned} \tag{3.1}$$

where ϵ_0 stands for the permittivity of the free space and A is the area of the capacitive plate. For small Δx, the relationship between the pressure change and the deformation can be regarded as linear [51]

$$\Delta x = \kappa \Delta P \tag{3.2}$$

where ΔP and κ are the change in pressure and the deformation sensitivity, respectively. It is a fixed charge system, Q; therefore, the corresponding voltage signal ΔV is

$$\begin{aligned} \Delta V &= \frac{Q}{C_2} - \frac{Q}{C_1} \\ \Delta V &= \frac{2Q\Delta x}{\epsilon_0 A} \end{aligned} \tag{3.3}$$

in which the fixed charge can be written in terms of the bias DC voltage, V_{bias}

$$Q = \frac{\epsilon_0 A}{x_0} V_{bias}. \tag{3.4}$$

V_{bias} plays an important role in the performance of the capacitive sensor. V_{bias} is in the 5-20V range, which is quite high for modern CMOS technologies. A DC-DC upconverter is required in the design for the generation of V_{bias}, which is left as future

work and externally applied in this system. Besides, ΔV can be defined in terms of V_{bias} and ΔP by using Equation (3.2) and Equation (3.4)

$$\begin{aligned} \Delta V &= \frac{2\kappa V_{bias}}{x_0}\Delta P \\ \kappa_V &= \frac{2\kappa V_{bias}}{x_0} \end{aligned} \tag{3.5}$$

in which κ_V stands for the voltage sensitivity. Undeformed capacitance values are around 3.5pF for x_0=4μm and A=1.6mm^2 which are logical values in these types of applications [53]. The resulting maximum Δx is 0.16μm; therefore, we obtain a capacitance of change $\pm$0.15pF. This system can sense the maximum pressure change that results in the voltage signal around $\pm$50mV. Parasitic capacitances are quite high (around 2-3pF) and the parasitic resistance is in the gigaohm range. The electrical equivalent of the differential capacitive system is shown in Figure 3.3.

3.2. Read-Out Blocks

Amplitude levels of the electrical equivalent of acoustic emission of the hip implant vary from 1mV to 50mV. Thus, a preamplifier stage with digitally controlled gain values is utilized to fully benefit from the ADC. Four equally spaced gain levels will be available from 4 to 32. Depending on the bitstream sequence, the gain of the preamplifier stage will be adjusted by switches S1, S2, S3, and S4 as illustrated in Figure 3.4. Logarithmic ADCs are the most compatible with the auditory system, for which eight to nine bits resolution is adequate [56]. Therefore, higher gain for lower value inputs together with a linear ADC provides a logarithmic behavior. Preamplifier stages can be exploited in DT [57] or CT [58] forms.

3.2.1. DT and CT Read-out Blocks Comparison

A DT amplifier can be superior to a CT amplifier in terms of matching, area, and CMOS compatibility. In addition, the performance of the preamplifier can be easily controlled via the clock frequency. However, charge injection and impulsive changes in

OTA's outputs can increase power consumption.

The DT and the CT capacitive charge preamplifiers are illustrated in Figure 3.4 and Figure 3.5. The DT preamplifier includes an extra capacitor $C_{holding}$ compared to the ordinary DT gain block to minimize the impulsive change at the outputs of OTA since it holds the output voltage close to its previous value during the sampling cycle.

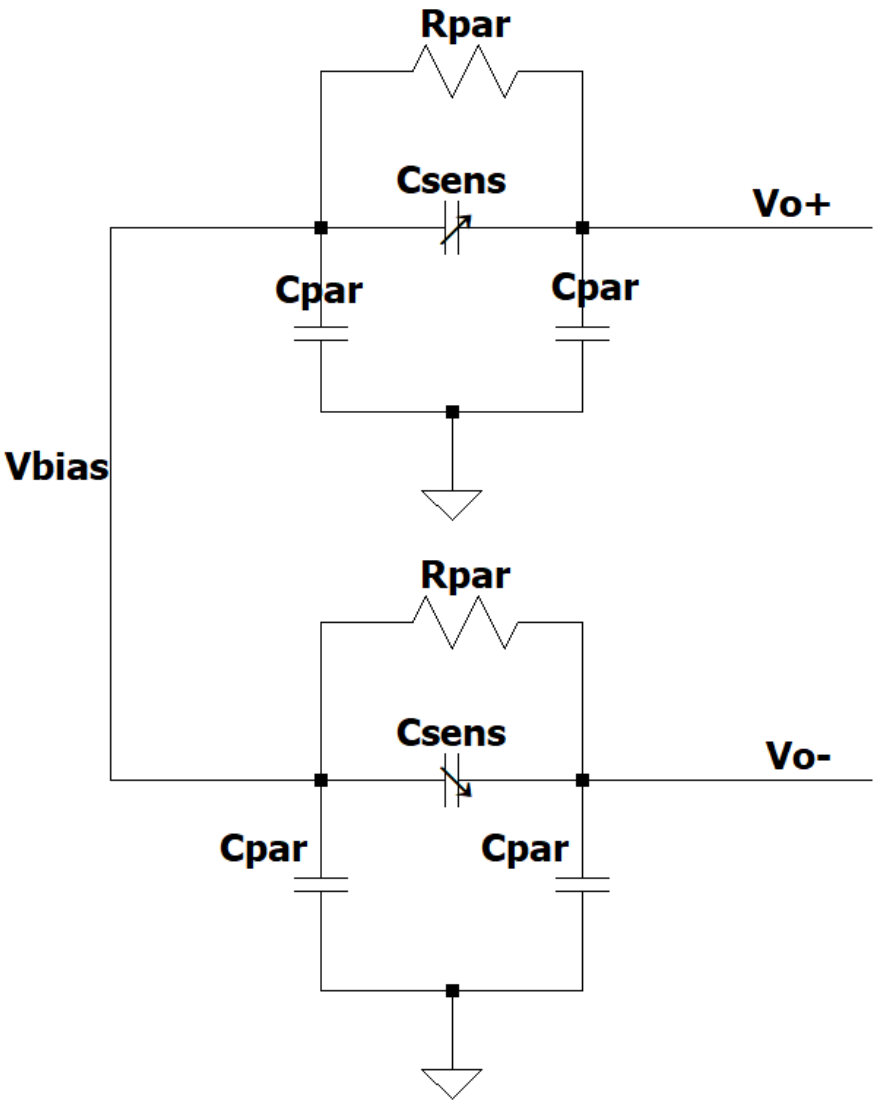

Figure 3.3. Differential capacitor electrical equivalent.

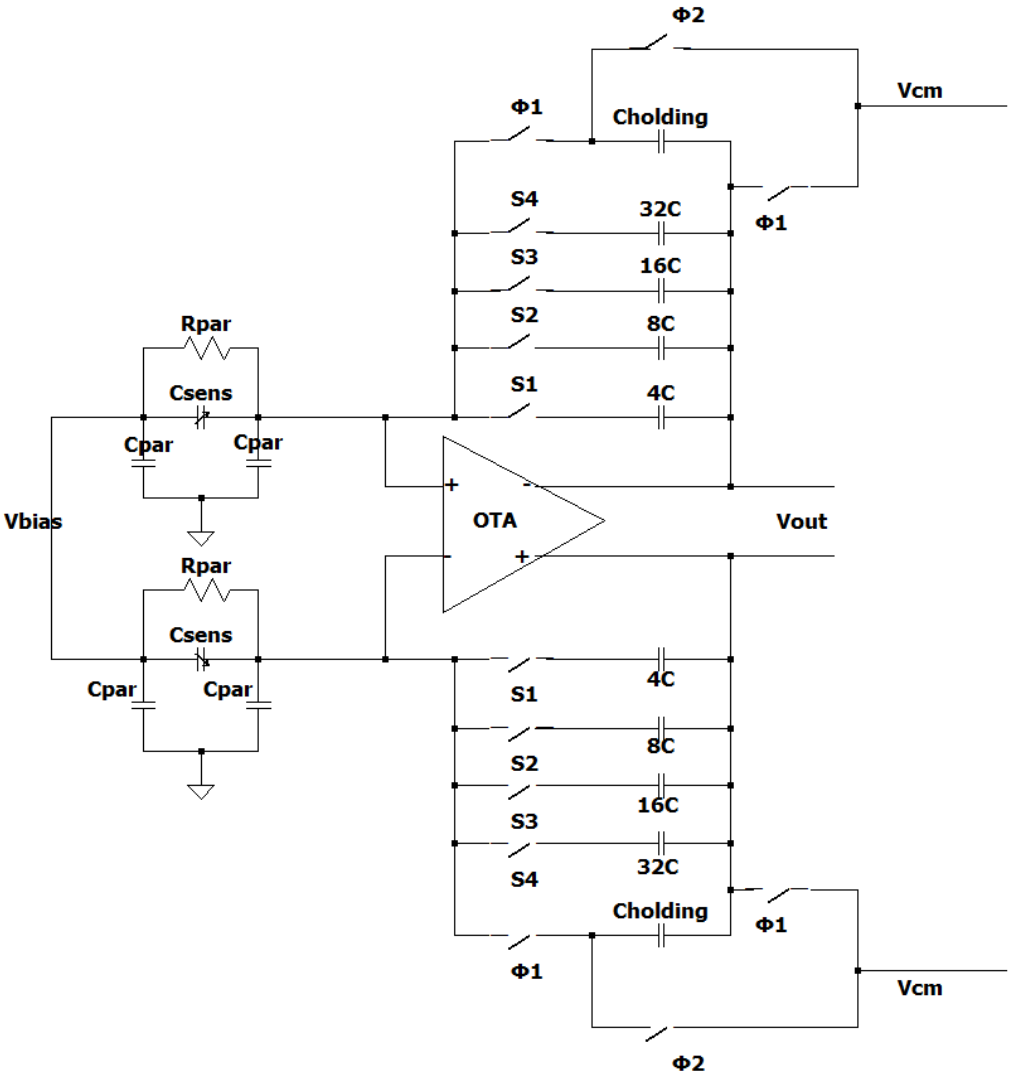

Figure 3.4. DT preamplifier with digitally control gain block.

It also controls the stability of the amplifier without disturbing the normal operation; therefore, it should be adjusted to provide proper operation even when the lowest capacitance branch is utilized. The DT preamplifier also includes a nonoverlapping clock switch next to digital gain control switches for SC operation. That is ignored in the schematic for the simplicity in Figure 3.4.

The CT preamplifier is a simple capacitive amplifier that shows a high-pass behavior. The resistor should be in the gigaohm range to stabilize the OTA when the

lowest capacitance branch is utilized. A resistor in this range can be realized with a series combination of pseudo-MOS transistors [59] for lower chip area in addition to resistor models mentioned in the previous chapter.

3.2.2. Simulations and Results of Read-out Blocks

The corresponding output voltages for the DT and the CT cases for ±50mV 1kHz inputs and for ±1mV 1kHz inputs are shown in Figure 3.6 and Figure 3.7, respectively.

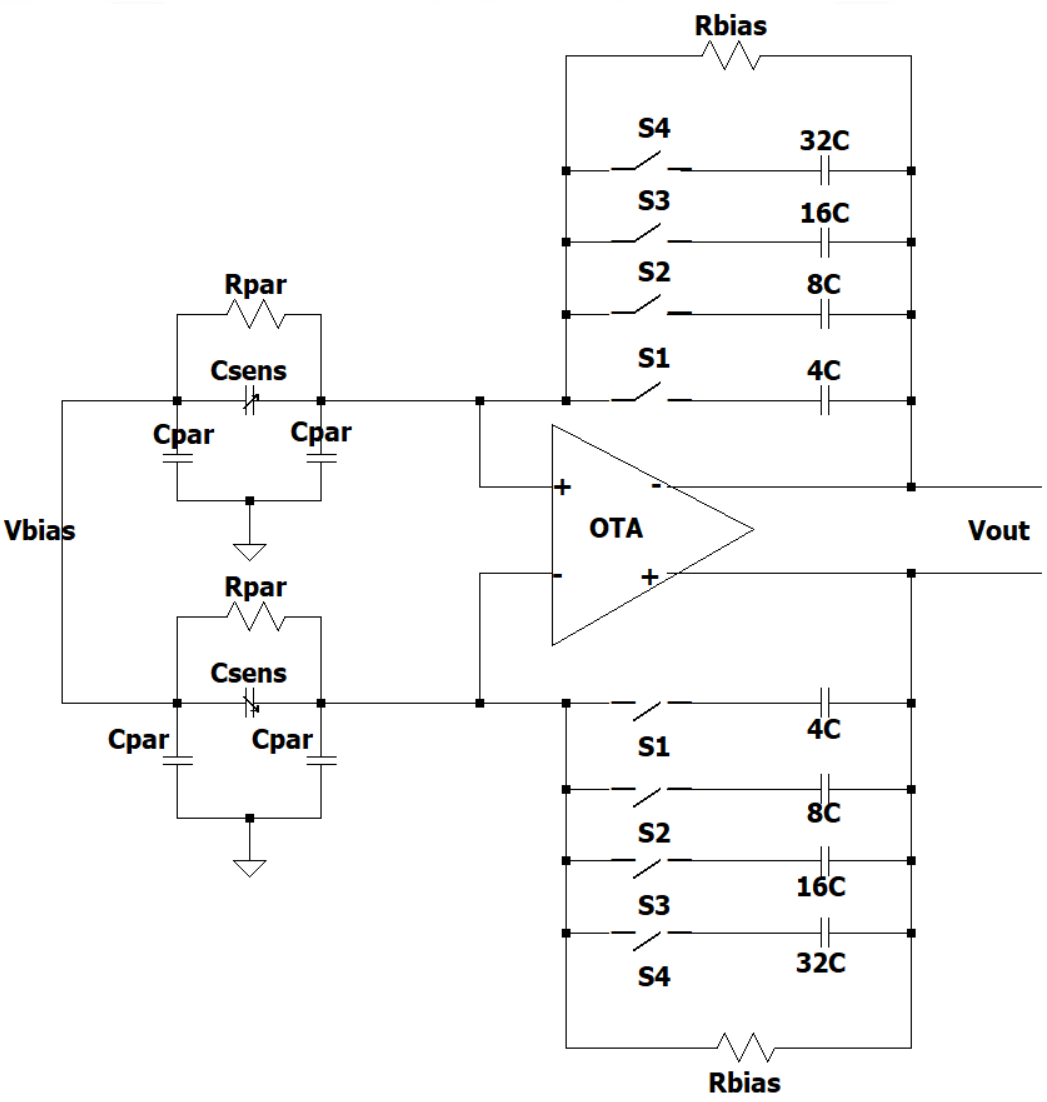

Figure 3.5. CT preamplifier with digitally control gain block.

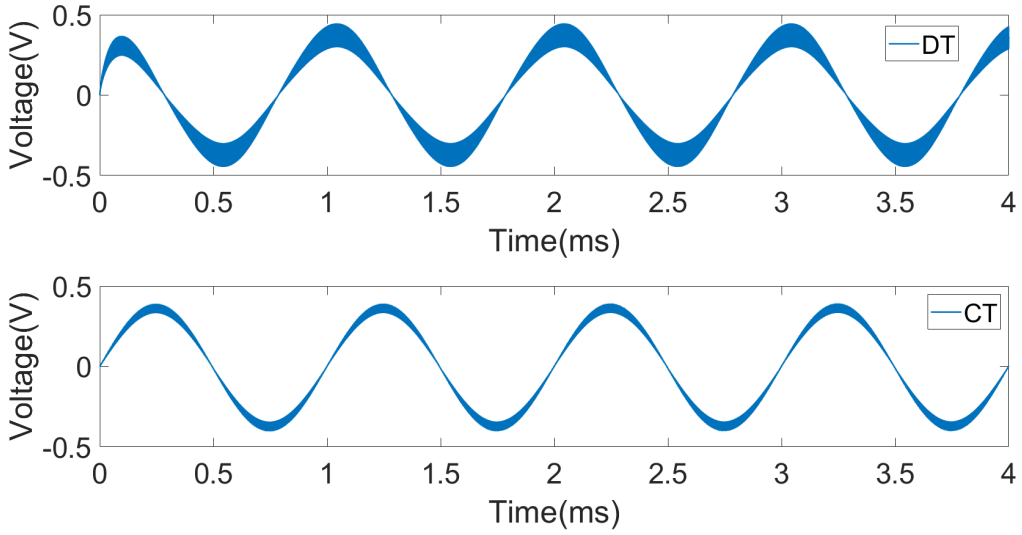

Figure 3.6. Transient simulations for ±50mV inputs in DT and CT cases.

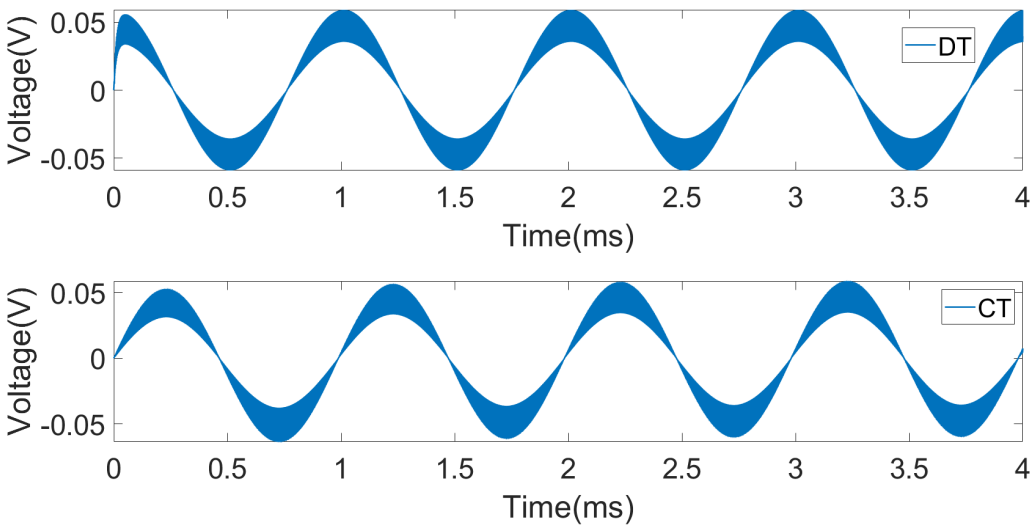

Figure 3.7. Transient simulations for ±1mV inputs in DT and CT cases.

These voltages are for the maximum and minimum gain levels controlled digitally. The power consumed is analyzed by varying the amplitude and frequency values of the sensed deformation in DT and CT cases. The resulting power consumptions are quite similar in both cases where 424.3μW for the DT case 428.9μW for the CT case. The

overall design will be determined according to the best combination out of alternative ADCs mentioned before since the power performances of the preamplifiers are nearly the same.

3.3. Second-Order Sigma-Delta ADC

The acoustic sensing system requires a high-frequency clock if we utilize a first-order system. The second-order system relaxes the clock frequency requirement; therefore, it lowers the power consumption. The characteristics of a second-order system are analyzed in this section.

3.3.1. Analysis of a DT second-order sigma-delta ADC

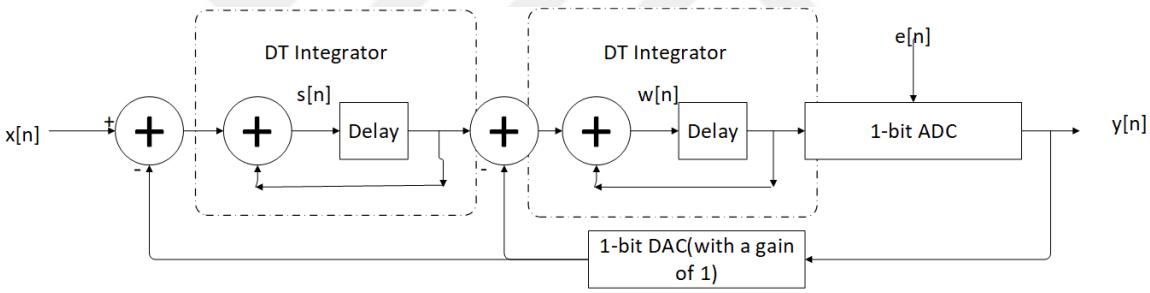

Figure 3.8. Block diagram of the second-order DT $\Sigma - \Delta$ ADC.

A simple DT second-order sigma-delta ADC is shown in Figure 3.8. The transfer function of the system can be obtained by inspection of this block diagram

$$\begin{aligned} s[aT_s] &= x[aT_s] - y[aT_s] + s[aT_s - T_s] \\ w[aT_s] &= s[aT_s - T_s] - y[aT_s] + w[aT_s - T_s] \\ y[aT_s] &= e[aT_s] + w[aT_s - T_s]. \end{aligned} \tag{3.6}$$

By writing the intermediate signals $s[aT_s]$ and $w[aT_s]$ in terms of the input and the output,

$$y[aT_s] = x[aT_s - 2T_s] - 2e[aT_s - T_s] + e[aT_s] + e[aT_s - 2T_s]. \tag{3.7}$$

By taking z-transform of Equation (3.7), resulting responses are

$$\begin{aligned} Y(z) &= z^{-2}X(z) + (1 - 2z^{-1} + z^{-2})E(z) \\ Y(z) &= z^{-2}X(z) + (1 - z^{-1})^2 E(z). \end{aligned} \tag{3.8}$$

The degree of the signal transfer function and the noise transfer function is doubled. That is why a 40dB/decade behavior is observed.

3.3.2. Feedforward Path and Stability

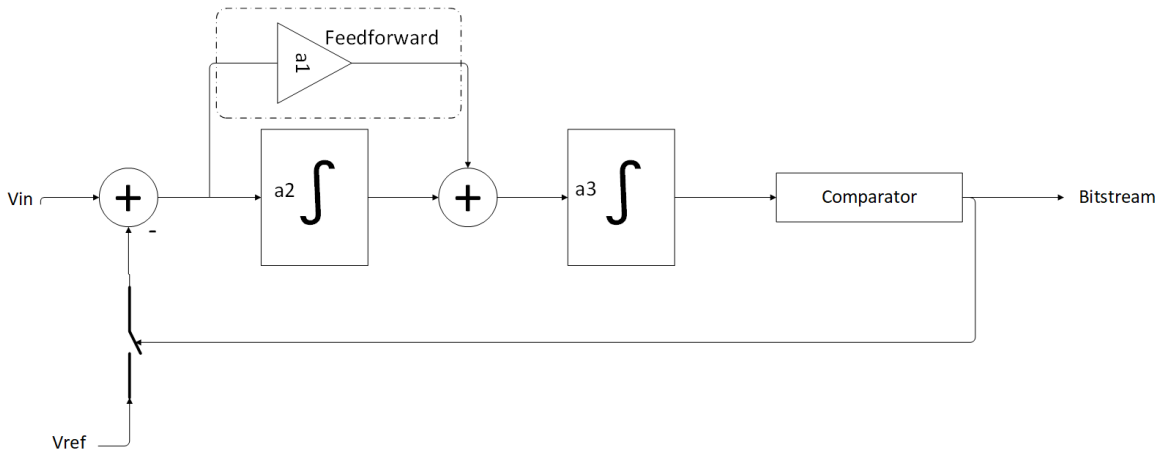

Figure 3.9. Block diagram of the second-order DT $\Sigma - \Delta$ ADC including the feedforward.

A second-order modulator is realized by two integrators with different gains as shown in Figure 3.9. A feedforward path is utilized in the design. This path decreases

the output swing of the first integrator without disturbing the operation too much; therefore, it will decrease the power consumption. Besides, the integration of this path eliminates the requirement of an extra reference voltage for the second integrator [21]. The addition of the feedforward branch modifies the transfer function of the system. Equation (3.8) simplifies to Equation (3.9) when $a1$, $a2$, and $a3$ are 1, 1/2, and 1, respectively

$$Y(z) = [z^{-2} + 2z^{-1}(1 - z^{-1})]X(z) + (1 - z^{-1})^2 E(z). \tag{3.9}$$

The additional high-pass term $2z^{-1}(1 - z^{-1})$ for the input can be compensated in the digital domain. The feedforward branch shifts the average of the outputs of the first integrator to zero; therefore, it prevents the saturation of the outputs of the second integrator.

Gains of integrators and the feedforward path are very critical since they control the stability of the system. In addition, they can be adjusted to bound integrators' outputs. The value of $a1/a2$ is the key ratio for the saturation of the system. For smaller $a1/a2$, outputs jump to the saturation levels. On the other hand, outputs experience clipping in the second modulator due to the large gain through the feedforward path for larger $a1/a2$. The effect of the first modulator becomes negligible for the latter case; therefore, the system behaves like a first-order system. The ideal value is between 2 and 4 [60]. $a3$ is determined to prevent unbounded outputs at the terminals of the second integrator. Sometimes the first integrator is designed as a gain-boosted amplifier to guarantee that no saturation occurs [61].

The second-order system shows better SNR since discrete noise tones are degraded compared to the first-order system. In addition to that, an increase in OSR results in a higher increase in ENOB for a second-order sigma-delta ADC.

3.3.3. Resolution Increase

The resolution of a first-order sigma-delta modulator can be increased by using a second-order modulator [62] or utilizing cascaded first-order modulators [63] or increasing the number of bits in the DAC [64]. Sigma-delta ADC designers try to avoid the third option since it distorts the linearity of the system.

A second-order modulator provides a 40dB/decade slope for the quantization noise at the expense of some portions of the input range. Inputs close to 0 and V_{ref} saturate the integrator outputs creating lower frequency noise tones not desired in an AC application.

Cascaded two first-order integrators are also able to provide 40dB/decade behavior without causing the saturation. The quantization noise of the first integrator is shaped by the second first-order integrator. That's why the full range can be utilized without any saturation issues. However, this resolution increase is highly dependent on component matching. In addition to that, decimation filter design is quite complex in this topology rather than a simple counter. Therefore, the design will be based on the second-order loop filter.

3.3.4. Proposed Designs of the Second-Order Sigma-Delta ADCs

The ADC in the temperature sensor is designed based on a novel adjustable range method in addition to an internally generated reference voltage. The proposed method can be exploited in a second-order system with or without an external reference. In this part, the validity of the proposed method will be shown. Besides, the dynamic properties of an ADC with or without reference voltage will be analyzed. The charge balancing property of a sigma-delta ADC is adjusted to the AC application,

$$\frac{V_{ac1} - V_{ac2} + \frac{V_{ac1}+V_{ac2}}{2}}{V_{ac1} + V_{ac2}} = \frac{N}{M} \tag{3.10}$$

where V_{ac1} and V_{ac2} are dc-coupled out of phase AC signals sensed by the capacitive sensor and amplified by the preamplifier. These signals' AC parts are linearly dependent on the acoustic emission according to Equation (3.5). The DC level of these signals is shifted to the common-mode output DC levels of the OTA. Therefore, V_{ac1} and V_{ac2} are

$$\begin{aligned} V_{ac1} &= V_{cm} + \Delta V \\ V_{ac2} &= V_{cm} - \Delta V \\ \frac{2\Delta V + V_{cm}}{2V_{cm}} &= \frac{N}{M} \end{aligned} \tag{3.11}$$

where V_{cm} is around 0.764V and ΔV stands for the AC excitation whose amplitude is between 32mV and 200mV after the preamplifier stage due to different gain levels for different input levels. The proposed design will roughly cover between 0.36V and 1.16V inside 1.52V internally obtained reference. The related design is illustrated in Figure 3.10.

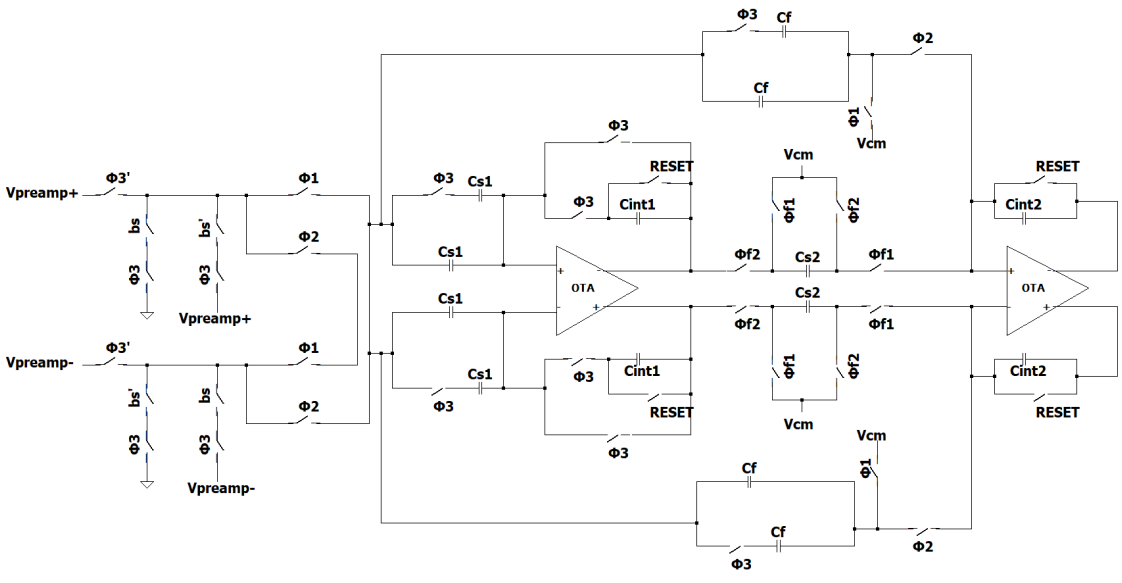

Figure 3.10. Schematic of the second-order DT $\Sigma - \Delta$ ADC without an external reference voltage.

The alternative design including an external reference is quite similar to the method in Figure 3.10. Governing equations are

$$\begin{aligned} \frac{V_{ac1} - V_{ac2} + \frac{V_{ref}}{2}}{V_{ref}} &= \frac{N}{M} \\ \frac{2\Delta V + \frac{V_{ref}}{2}}{V_{ref}} &= \frac{N}{M} \end{aligned} \tag{3.12}$$

where V_{ref} is around 1.10V obtained from the temperature-insensitive current reference. The proposed design will roughly cover between 0.15V and 0.95V inside 1.10V internally obtained reference. The related design is illustrated in Figure 3.11. $a1$, $a2$, and $a3$ will be adjusted by capacitance ratios in both designs

$$\begin{aligned} a1 &= \frac{C_f}{C_{s2}} \\ a2 &= \frac{C_{s1}}{C_{int1}} \\ a3 &= \frac{C_{s2}}{C_{int2}}. \end{aligned} \tag{3.13}$$

Capacitance values are determined by the transfer function of the modulator and the designed load capacitance of the OTA. Required clocks for the second-order ADCs are shown in Figure 3.12.

3.3.5. Simulations of the Second-Order Sigma-Delta ADCs

Outputs of the integrators for the ADC without an external reference are illustrated in Figure 3.13. Those for the ADC with an external reference are demonstrated in Figure 3.14.

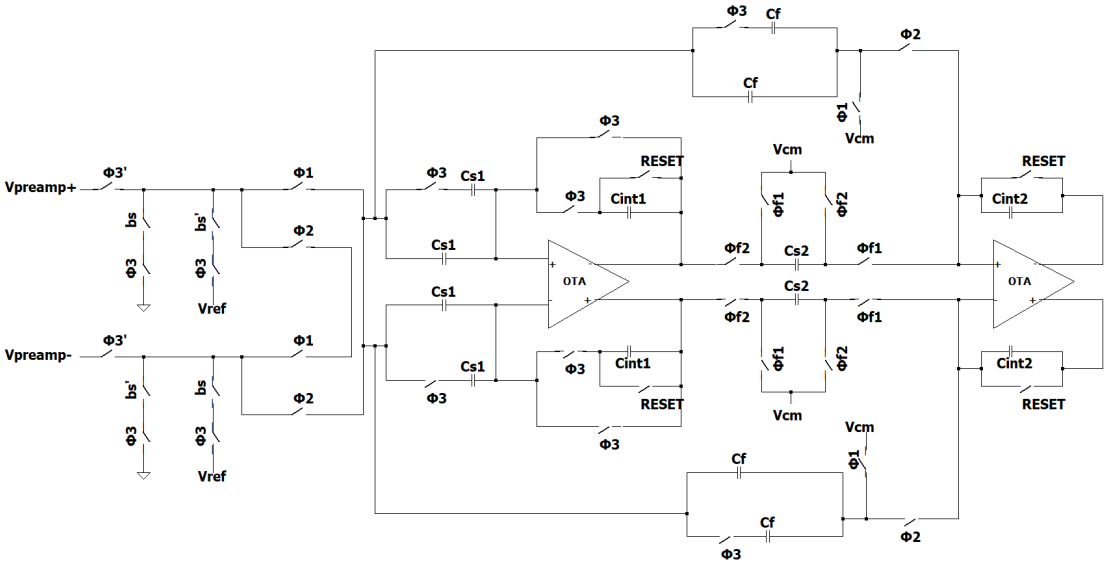

Figure 3.11. Schematic of the second-order DT $\Sigma - \Delta$ ADC with an external reference voltage.

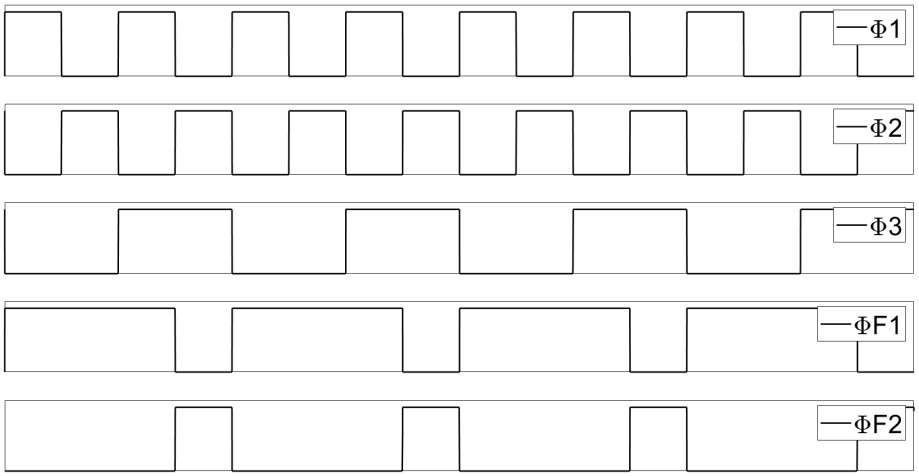

Figure 3.12. Required clocks.

Both ADCs do not experience clipping since gains are adjusted properly. Modulated information of inputs can be observed in transient simulations of ADCs in Figure 3.15 and Figure 3.16.

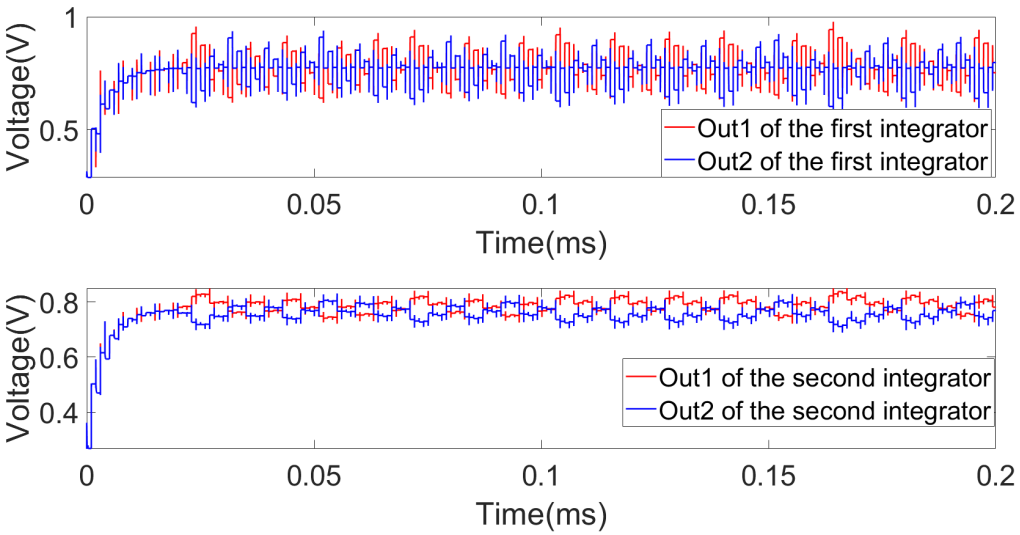

Figure 3.13. Integrator outputs of the second-order DT $\Sigma - \Delta$ ADC without an external reference voltage.

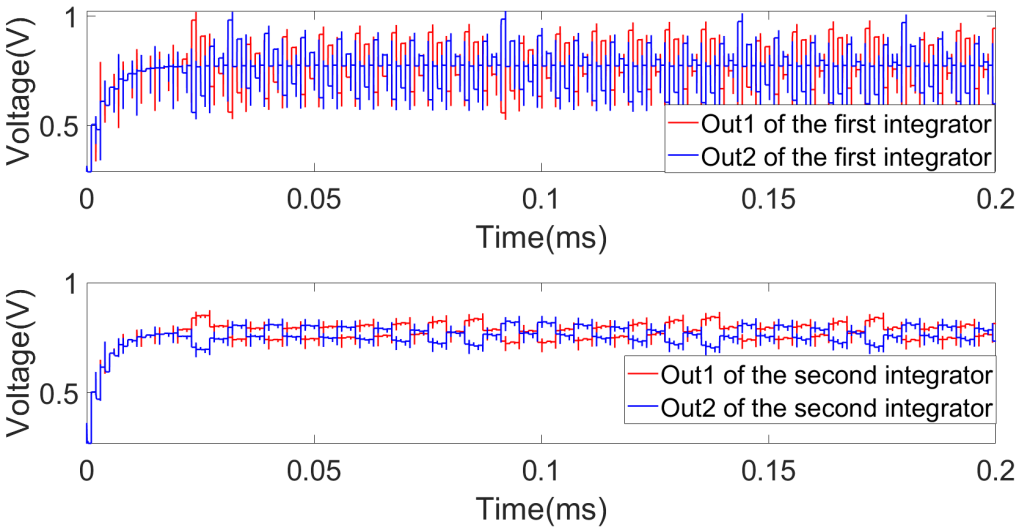

Figure 3.14. Integrator outputs of the second-order DT $\Sigma - \Delta$ ADC with an external reference voltage.

The slope of 40dB/decade is achieved in both designs as observed in Figure 3.17 and Figure 3.18. In the next section, the two types of ADC will be combined with two

types of preamplifiers for four design alternatives. They will be analyzed in terms of SNR, ENOB, and power consumption.

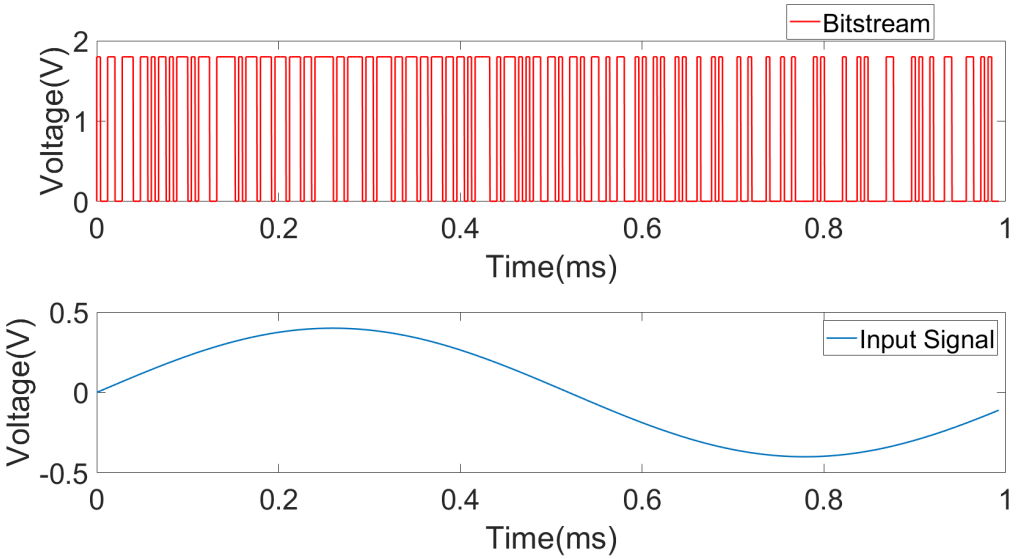

Figure 3.15. Transient analysis of the ADC without an external reference.

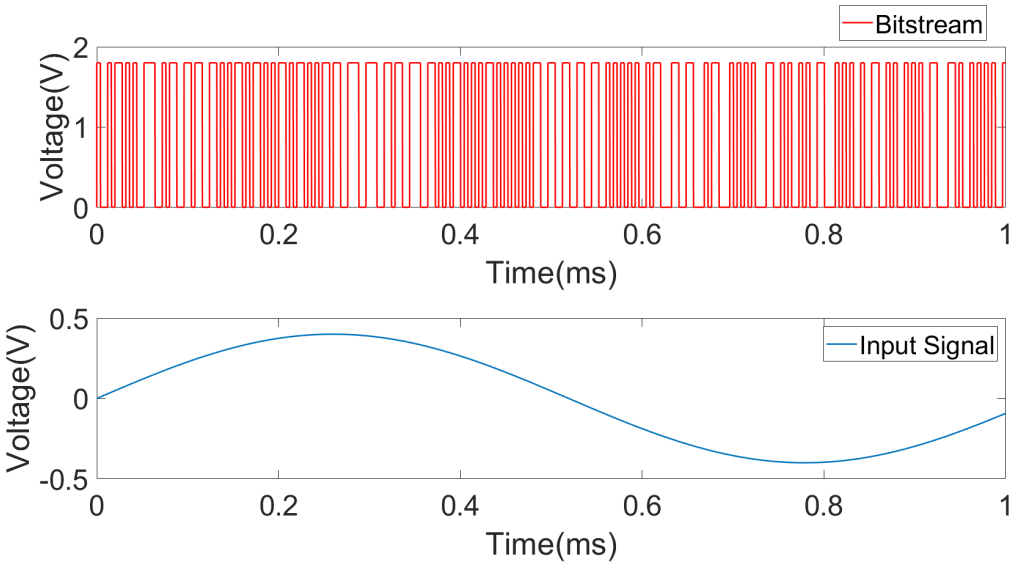

Figure 3.16. Transient analysis of the ADC with an external reference.

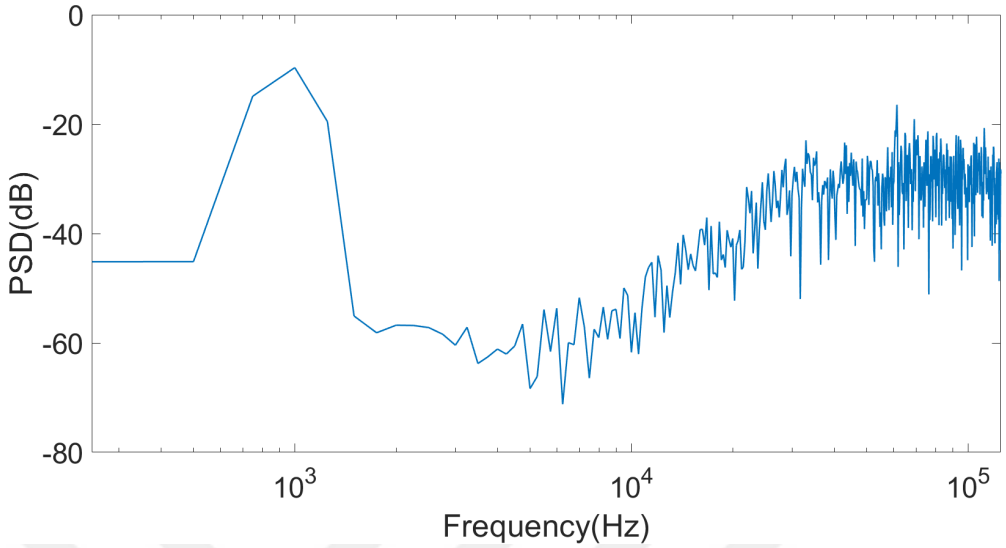

Figure 3.17. PSD of the ADC without an external reference(Hanning windowed).

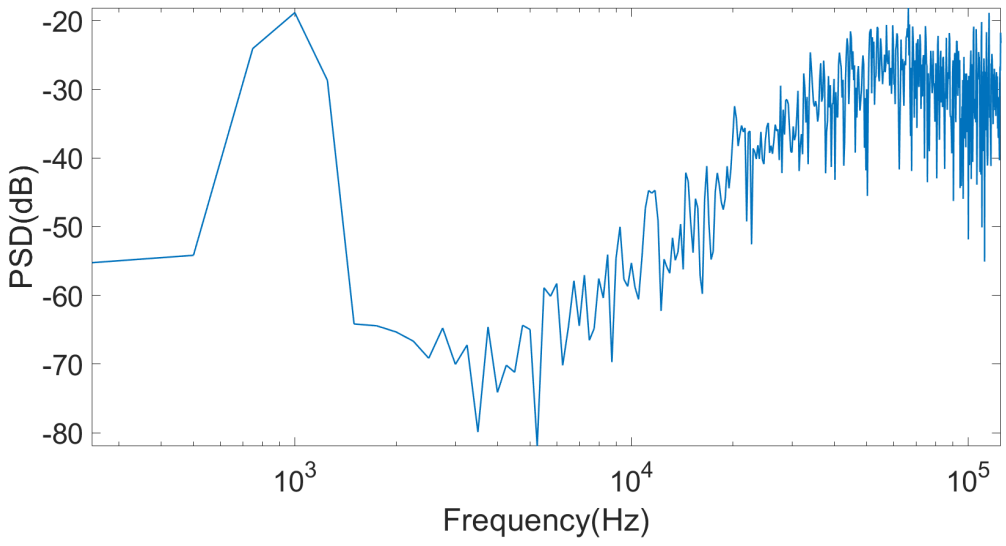

Figure 3.18. PSD of the ADC with an external reference(Hanning windowed).

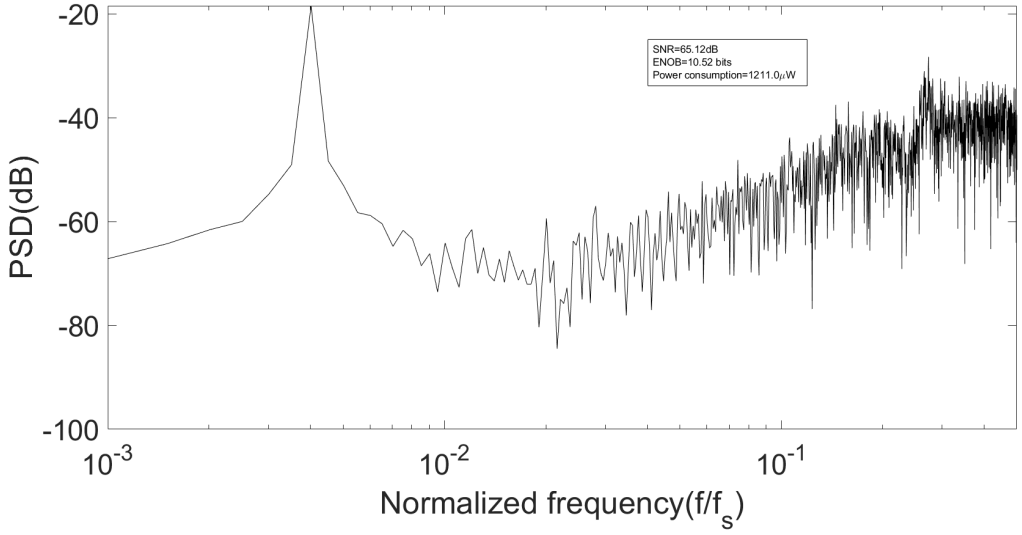

Figure 3.19. PSD of the overall system that includes the CT preamplifier and the second-order SC ADC without an external reference(262144 points, Rectangular windowed).

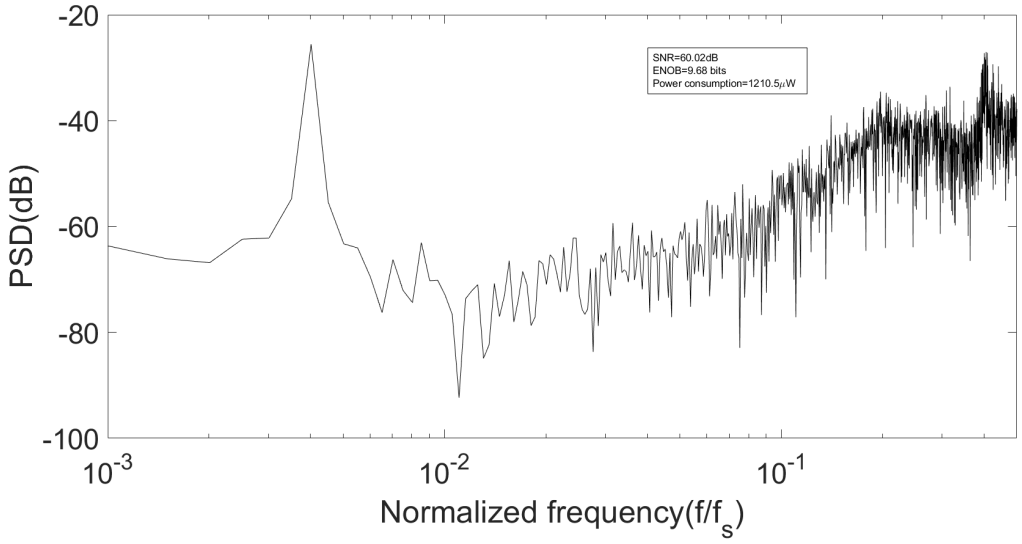

Figure 3.20. PSD of the overall system that includes the DT preamplifier and the second-order SC ADC without an external reference(262144 points, Rectangular windowed).

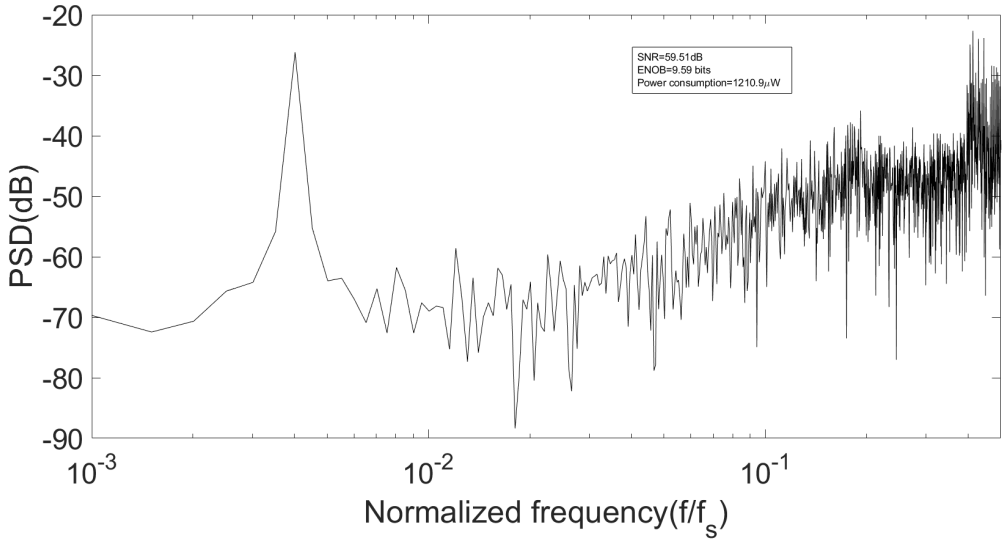

Figure 3.21. PSD of the overall system that includes the CT preamplifier and the second-order SC ADC with an external reference(262144 points, Rectangular windowed).

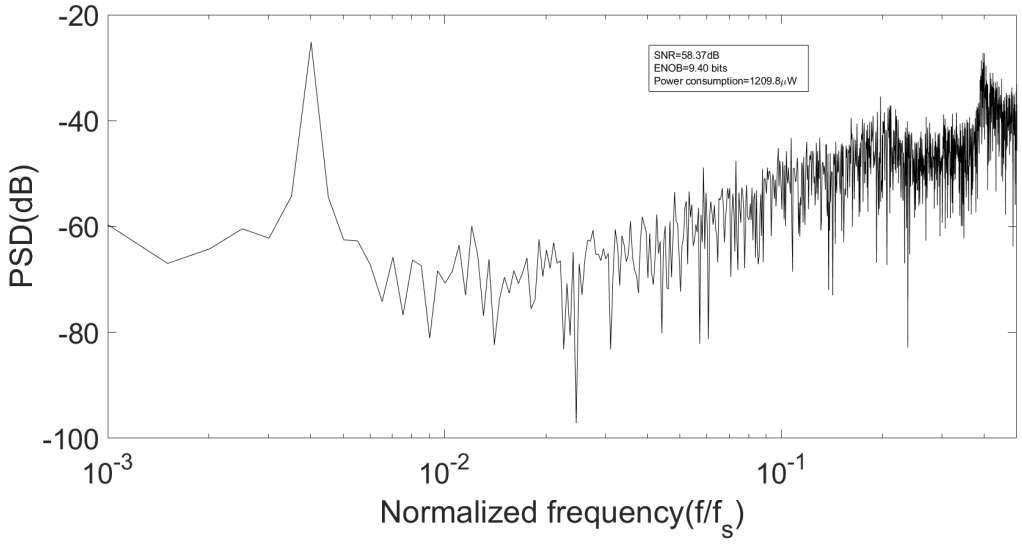

Figure 3.22. PSD of the overall system that includes the DT preamplifier and the second-order SC ADC with an external reference(262144 points, Rectangular windowed).

3.4. Design Alternatives

Two design options are proposed as a preamplifier stage: a DT and a CT interface. Second-order sigma-delta ADC is also implemented in two different ways: with or without an external reference voltage. These alternatives are cascaded for the overall acoustic sensor system. Power consumptions, SNR, and ENOB of these blocks are analyzed for 1kHz ±40mV inputs to determine the best performance when OSR is chosen as 32 according to Table 2.1. Results are illustrated in Figures 3.19, 3.20, 3.21, and 3.22.

The rectangular window is utilized to show the input signal clearly, however, SNR and ENOB calculations are handled with a 7-term Blackman-Harris window since it provides higher attenuation for sidelobes as mentioned in the previous chapter. The slope of 40dB/decade is obtained in both designs, which is a sign of proper second-order behavior. Digital gain control block in the preamplifier further increases the resolution of the system. The combination of the CT preamplifier and the second-order SC ADC without an external reference is regarded as the best design option since it is superior in terms of the dynamic parameters of the ADC as illustrated in Table 3.1. Power consumptions are very close to each other. Even though it seems relatively high for an implantable biomedical application, it should be clarified that sensing systems do not operate continuously. The reset switch mentioned before keeps the system off as long as no sensing is held, which is the dominant operation mode of this system.

Table 3.1. Dynamic Performances of Design Alternatives.

Design alternatives	SNR(dB)	ENOB(bits)	Power(μW)
CT preamp+ADC without a reference	65.12	10.52	1211.0
DT preamp+ADC without a reference	60.02	9.68	1210.5
CT preamp+ADC with a reference	59.51	9.59	1210.9
DT preamp+ADC with a reference	58.37	9.40	1209.8

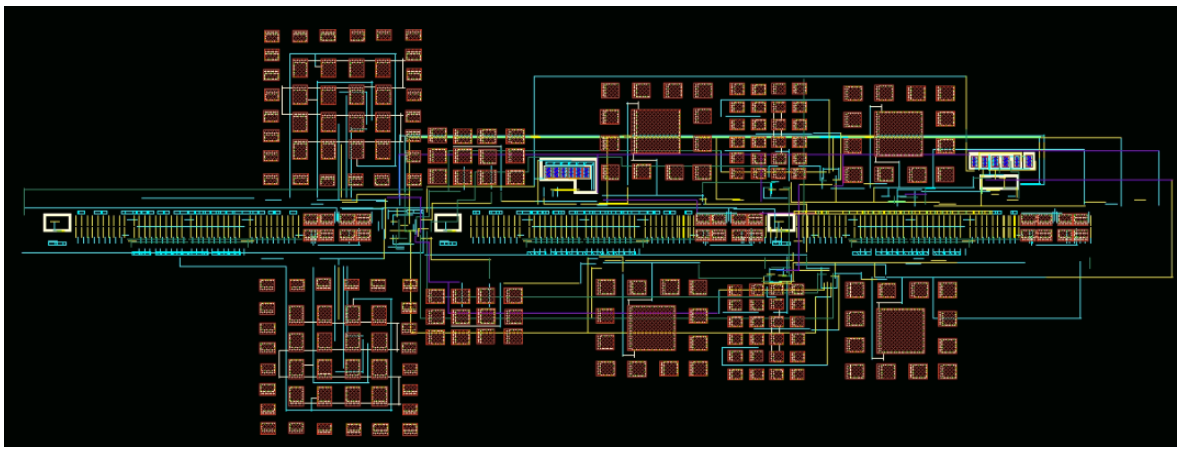

Figure 3.23. Layout of the acoustic sensor.

Table 3.2. Performance Summary of the Acoustic Sensor.

Technology	0.18μm CMOS
Layout area	0.28mm^2
SNR	50.40dB
ENOB	8.08 bits
Energy required per conversion	575fJ
OSR	32
Supply voltage	1.3V - 2.7V

3.5. Overall Acoustic Sensor

The combination of the CT preamplifier and the second-order SC ADC without an external reference is implemented in umc 0.18μm CMOS technology. The resulting layout of the system is depicted in Figure 3.23. The desired operation has been achieved according to the design specifications. The performance of the acoustic sensor is summarized in Table 3.2.

4. CONCLUSION AND FUTURE WORK

In this thesis, the design of front-end circuits for a hip implant IC is realized. The hip implant is monitored in terms of its temperature and its acoustic emission properties to control its proper function. In chapter 2, the literature related to the temperature sensing systems and its interface electronics is reviewed. In addition to designs of required blocks, a novel method to adjust the full-scale range of an ADC is presented. The proposed design is implemented in umc 0.18μm CMOS technology and is analyzed in terms of linearity and power consumption.

In chapter 3, the design of front-end circuits for an acoustic sensor system is handled. In addition to the literature review, the novel method in the temperature sensor system is adapted to the acoustic sensor system with proper adjustments. Discrete-time and continuous-time systems are compared in terms of their performances. Besides, proposed ADCs are analyzed to obtain the best option for an implantable IC design. The proposed design is implemented in umc 0.18μm CMOS technology and achieves design constraints.

4.1. Future Work

The overall design can be improved in many aspects since the hip implant IC design includes nearly all areas in the electronics.

Clocks are provided from outside of the IC. The full integration of the implantable hip implant requires internal clock generation and delay circuits. Moreover, ADCs are analyzed with bitstream generated out of the comparator. Conversion of the bitstream to the common weighted binary representation is handled in MATLAB. Besides, the digital gain control block is implemented manually. Digital block implementations of the design can be integrated into the chip. Mixed-mode analysis can be held in order to obtain a better performance.

The triple-well process should be utilized to draw layouts of diodes in the temperature sensor for more realistic results.

Metal-insulator-metal capacitors are utilized in the novel method mentioned. Even though constraints of the hip implant IC eliminates the obligation of many calibration methods, tuning circuits for MIM capacitors will stabilize the performance in the desired range.

Micro electro mechanical systems capacitive sensors are represented by their macromodels. The monolithic design of MEMS and CMOS can result in better performances in terms of noise and power. However, MEMS sensor should be implemented for more realistic models.

The MEMS sensor requires relatively high bias voltage. Final design determines the exact value for this bias voltage. In addition, the voltage domain of the design can be adjusted to minimize power consumption depending on the exploited power unit. Therefore, the integration of power management electronics into the design will be very beneficial.

Finally, two sensing systems can be incorporated into one system that alternatively senses the desired parameter. We can end up in very low power levels by utilizing an interface switching between temperature sensing, acoustic sensing, and a sleep mode.

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